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XGS 12000, XGS 9400 and XGS 8000 Global Shutter CMOS Image Sensors

XGS Family

Description

The XGS CMOS image sensor family provides high resolution, high performance global shutter image capture. The family comes in different resolutions in a single package; 8.8, 9.4 and 12.6 MP with up to 1-inch optical format. The 21 mm x 20 mm package makes the XGS family particularly suited for integration in 29 mm x 29 mm camera formats. The high speed, 12-bit output maximally leverages interfaces such as USB 3.2, Thunderbolt™ 2 and 10 GigE.

Image data is read out through a column ADC architecture and then transferred over a HiSPi interface. On-chip logic, programmable via the serial interface, generates internal timing for integration and readout control. Up to three register configurations can be programmed and sequentially enabled (frame by frame) using a single command over the control interface.

Table 1. KEY PERFORMANCE PARAMETERS

| Parameter | Typical Value | |
|---------------------|--|-------------------------------|
| Optical Format | XGS 12000 | 1-inch (16.4 mm Diagonal) |
| | XGS 9400 | 1/1.2-inch (13.9 mm Diagonal) |
| | XGS 8000 | 1/1.1-inch (14.8 mm Diagonal) |
| Active Pixels | XGS 12000 | 4096 (H) x 3072 (V) |
| | XGS 9400 | 3072 (H) x 3072 (V) |
| | XGS 8000 | 4096 (H) x 2160 (V) |
| Pixel Size | 3.2 μm | |
| Color Filter Array | Monochrome, Bayer | |
| Shutter Type | Global Shutter | |
| Input Clock | 32.4 MHz | |
| Output Interface | HiSPi (24 Lanes – 777.6 Mbps/lane) | |
| Frame Rate (12-bit) | 24 Lanes (–X1) | |
| | XGS 12000 | 90 fps |
| | XGS 9400 | 90 fps |
| | XGS 8000 | 128 fps |
| | 12 Lanes (–X2) | |
| | XGS 9400 | 56 fps |
| | XGS 8000 | 80 fps |
| | 6 Lanes (–X3) | |
| | XGS 12000 | 28 fps |
| Read Noise | < 4 e ⁻ (1x), 1.9 e ⁻ (4x) | |
| SNR _{MAX} | 40 dB | |
| Dynamic Range | 68 dB | |
| Supply Voltages | 1.2 V, 2.8 V, 3 V (0.4 V, 1.8 V Optional) | |
| Power Consumption | 1 W (Full Speed, Full Resolution) | |
| Operating Temp. | –40°C to 85°C (Junction) | |
| Package | 163-pin CLGA (Ceramic Land Grid Array) | |

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Non-NDA Data Sheet

Interested in what you see? If you would like more detailed information, please request the full version of our data sheet.

[Request Full Data Sheet](#)

Features

- On-chip 12-bit Column ADCs
- 10-bit Mode with Increased Frame Rate of 100 fps (24-lane) at Full Resolution
- Companding and 10-Bit Mode at 60 fps (12-lane) and 30 fps (6-lane)
- Data Interface: 24-lane HiSPi (Scalable Low-Voltage Signaling)
- Configurable Number of HiSPi Lanes: 24, 18, 12 or 6 Lanes
- Two-Wire (I²C) and Four-Wire (SPI) Serial Interface
- Triggered Integration and Readout Control
- Programmable Control for up to 8 Regions of Interest (ROI)
- Context Switching
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Security
- Intelligent Transportation Systems (ITS)
- Broadcasting
- Medical
- Scientific

XGS Family

ORDERING INFORMATION

Table 2. ORDERABLE PART NUMBERS (Notes 1 and 2)

| Part Number | Minimum Order Quantity | Product Description | | | Speed Grade | Resolution (H x V) |
|-------------------|------------------------|---------------------|-------|----------|-------------|--------------------|
| NOIX1SN012KB-LTI | 25 | 12.6 MP | Mono | 0° CRA | 24 Lanes | 4096 x 3072 |
| NOIX1SN012KB-LTI1 | 4 | | | | | |
| NOIX1SE012KB-LTI | 25 | 12.6 MP | Color | 0° CRA | | |
| NOIX1SE012KB-LTI1 | 4 | | | | | |
| NOIX1SF012KB-LTI | 25 | 12.6 MP | Color | 7.3° CRA | | |
| NOIX1SF012KB-LTI1 | 4 | | | | | |
| NOIX3SN012KB-LTI | 25 | 12.6 MP | Mono | 0° CRA | 6 Lanes | |
| NOIX3SN012KB-LTI1 | 4 | | | | | |
| NOIX3SE012KB-LTI | 25 | 12.6 MP | Color | 0° CRA | | |
| NOIX3SE012KB-LTI1 | 4 | | | | | |

| | | | | | | |
|-------------------|----|--------|-------|--------|----------|-------------|
| NOIX1SN9400B-LTI | 25 | 9.4 MP | Mono | 0° CRA | 24 Lanes | 3072 x 3072 |
| NOIX1SN9400B-LTI1 | 4 | | | | | |
| NOIX1SE9400B-LTI | 25 | 9.4 MP | Color | 0° CRA | | |
| NOIX1SE9400B-LTI1 | 4 | | | | | |
| NOIX2SN9400B-LTI | 25 | 9.4 MP | Mono | 0° CRA | 12 Lanes | |
| NOIX2SN9400B-LTI1 | 4 | | | | | |
| NOIX2SE9400B-LTI | 25 | 9.4 MP | Color | 0° CRA | | |
| NOIX2SE9400B-LTI1 | 4 | | | | | |

| | | | | | | |
|-------------------|----|--------|-------|----------|----------|-------------|
| NOIX1SN8000B-LTI | 25 | 8.8 MP | Mono | 0° CRA | 24 Lanes | 4096 x 2160 |
| NOIX1SN8000B-LTI1 | 4 | | | | | |
| NOIX1SE8000B-LTI | 25 | 8.8 MP | Color | 0° CRA | | |
| NOIX1SE8000B-LTI1 | 4 | | | | | |
| NOIX2SF8000B-LTI | 25 | 8.8 MP | Color | 7.3° CRA | 12 Lanes | |
| NOIX2SF8000B-LTI1 | 4 | | | | | |
| NOIX2SN8000B-LTI | 25 | 8.8 MP | Mono | 0° CRA | | |
| NOIX2SN8000B-LTI1 | 4 | | | | | |
| NOIX2SE8000B-LTI | 25 | 8.8 MP | Color | 0° CRA | | |
| NOIX2SE8000B-LTI1 | 4 | | | | | |

1. See the **onsemi** Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.
2. All devices listed in Table 2 are equipped with microlenses.

Table 3. ORDERING INFORMATION EVALUATION KITS

| Part Number | Product Description | Additional Information |
|----------------------|--|--|
| NOIX1SN012KBLFB-GEVB | Sensor Headboard (12.6 MP, Mono, 24-Lane) | Demo Kit Headboard (incl. NOIX1SN012KB-LTI) (Note 3) |
| NOIX1SE012KBLFB-GEVB | Sensor Headboard (12.6 MP, Color, 24-Lane) | Demo Kit Headboard (incl. NOIX1SE012KB-LTI) (Note 3) |
| AGBAN6CS-GEVK | Frame Buffer Demo Board | AP21088 including Power Adapter |
| AGB1N0CS-GEVK | Demo 3 Board | FPGA Base Board including USB Cable and Tripod |

3. Sensors are soldered to the headboard.

XGS Family

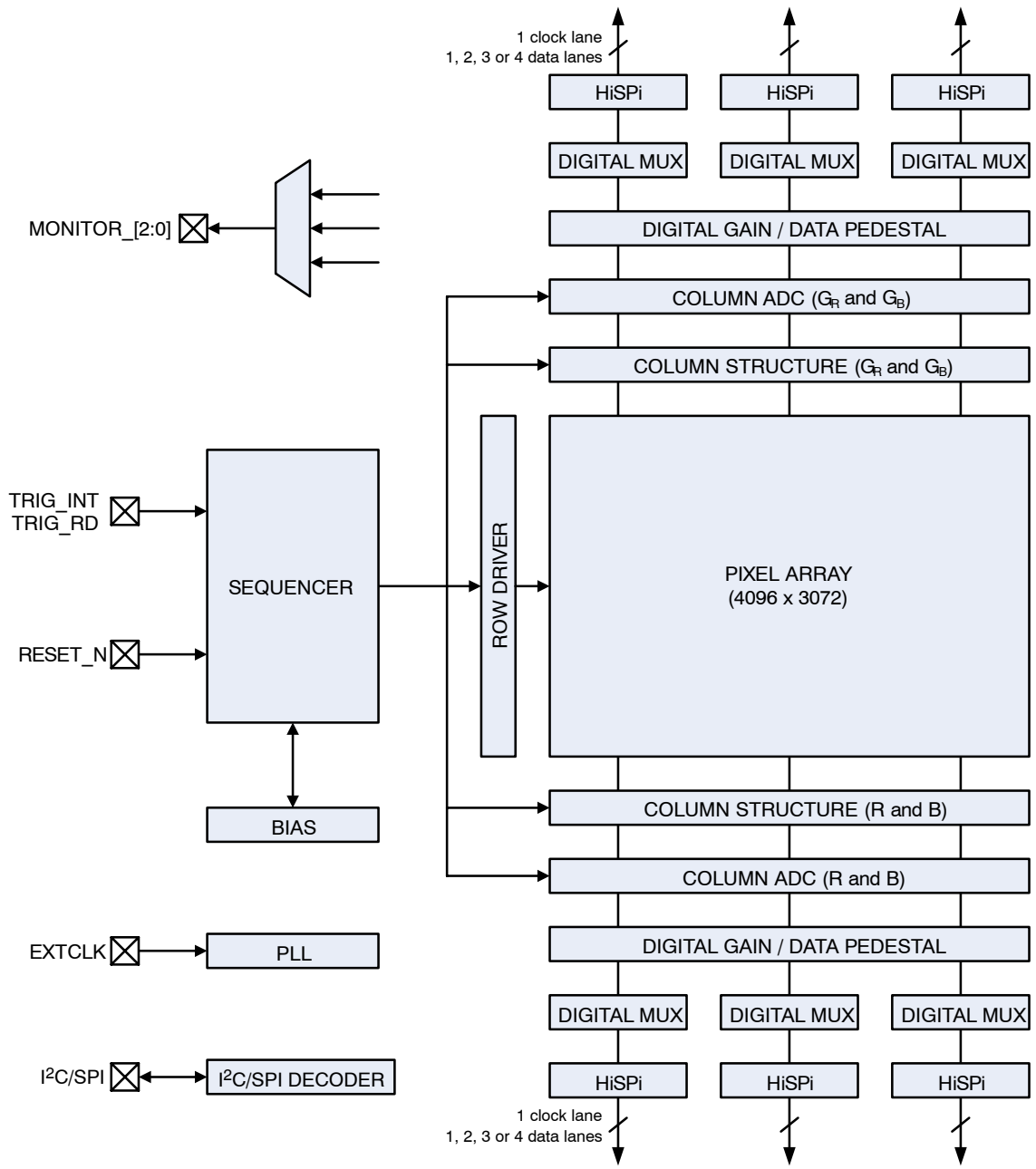
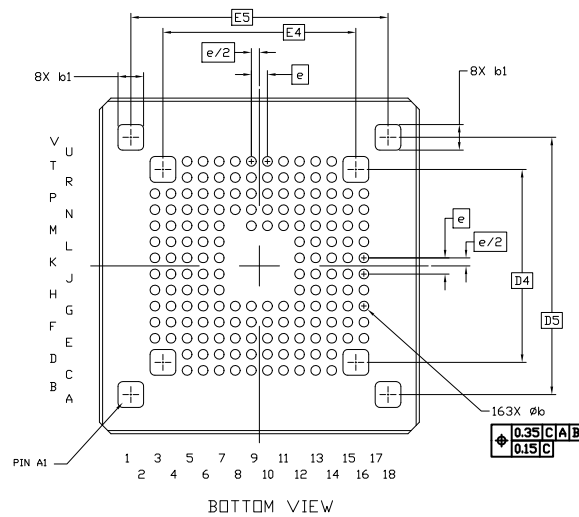
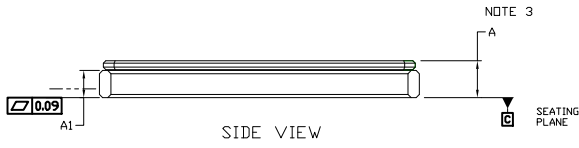
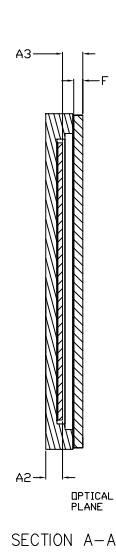
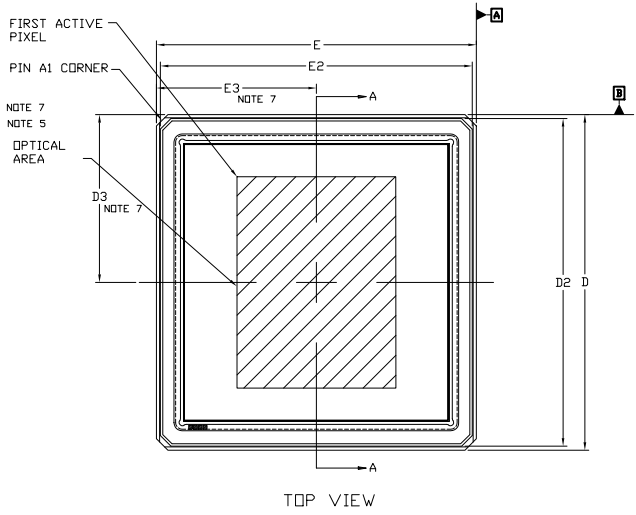


Figure 1. Functional Block Diagram (XGS 12000)

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CASE 621AB
ISSUE A

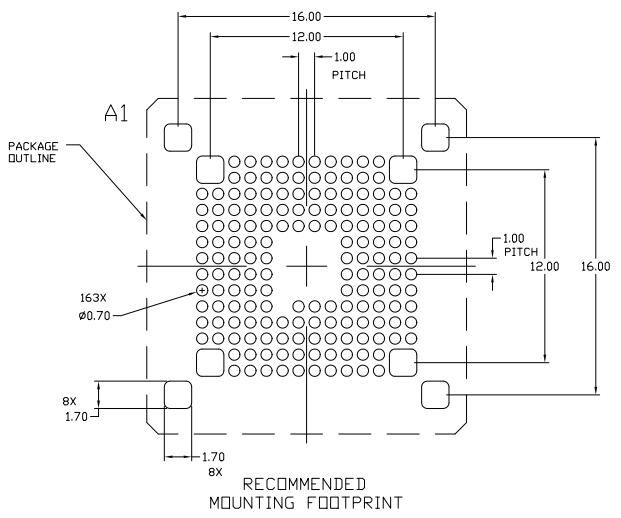
DATE 11 SEP 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. THE LID DEFINED BY DIMENSIONS D2 AND E2 MUST BE LOCATED WITHIN DIMENSIONS D AND E.
5. MAXIMUM ROTATION OF OPTICAL AREA RELATIVE TO PACKAGE EDGES JOINING AT A1 CORNER, WILL BE 0.7°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY. REFER TO THE DEVICE DATA SHEET FOR TOTAL ARRAY AND FIRST PIXEL DEFINITIONS.
6. PARALLELISM APPLIES ONLY TO THE OPTICAL AREA.
7. OPTICAL CENTER OFFSET WITH RESPECT TO THE PACKAGE CENTER IS X= 12.345 MICRONS, Y= 77.63 MICRONS ±200 MICRONS.

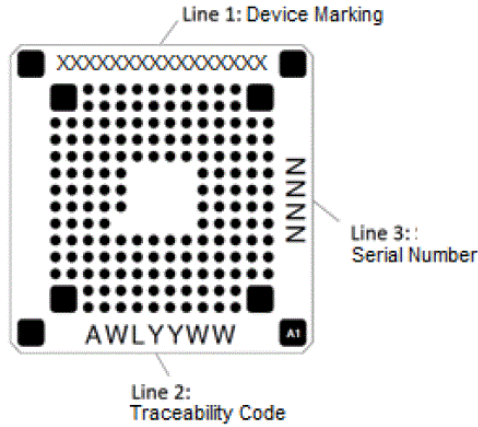
| MILLIMETERS | | |
|-------------|-------|-------|
| DIM | MIN. | MAX. |
| A | --- | 2.54 |
| A1 | 1.61 | 1.89 |
| A2 | 0.91 | 1.19 |
| A3 | 1.05 | 1.45 |
| b | 0.55 | 0.65 |
| b1 | 1.60 | REF |
| D | 20.76 | 21.00 |
| D2 | 20.30 | 20.46 |
| D3 | 10.16 | 10.56 |
| D4 | 12.00 | BSC |
| D5 | 16.00 | BSC |
| E | 19.80 | 20.00 |
| E2 | 19.32 | 19.48 |
| E3 | 9.76 | 10.16 |
| E4 | 12.00 | BSC |
| E5 | 16.00 | BSC |
| e | 1.00 | BSC |
| F | 0.50 | 0.60 |



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**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- NN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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