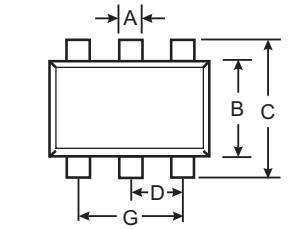


Features

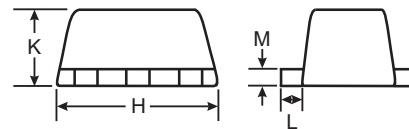
- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Lead Free By Design/RoHS Compliant (Note 3)**

Mechanical Data

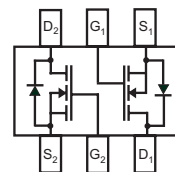
- Case: SOT-563
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208
- Terminals: Lead bearing terminal plating available. See Ordering information Page 2, Note 6
- Marking: See Page 2
- Ordering & Date Code Information: See Page 2
- Weight: 0.006 grams (approximate)



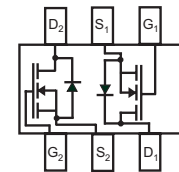
SEE NOTE 1



SOT-563			
Dim	Min	Max	Typ
A	0.15	0.30	0.25
B	1.10	1.25	1.20
C	1.55	1.70	1.60
D	0.50		
G	0.90	1.10	1.00
H	1.50	1.70	1.60
K	0.56	0.60	0.60
L	0.10	0.30	0.20
M	0.10	0.18	0.11
All Dimensions in mm			



2N7002V
(KAS Marking Code)



2N7002VA
(KAY Marking Code)

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V _{DSS}	60	V
Drain-Gate Voltage R _{GS} ≤ 1.0MΩ	V _{DGR}	60	V
Gate-Source Voltage (Note 3)	V _{GSS}	±20	V
		±40	
Drain Current (Note 3)	I _D	280	mA
Drain Current (Note 3)	I _{DM}	1.5	A
Total Power Dissipation	P _d	150	mW
Thermal Resistance, Junction to Ambient	R _{θJA}	833	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

- Notes:
1. Package is non-polarized. Parts may be on reel in orientation illustrated, 180° rotated, or mixed (both ways).
 2. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.
 3. No purposefully added Lead.

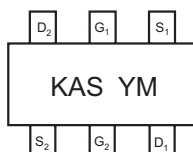
Electrical Characteristics @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 4)						
Drain-Source Breakdown Voltage	BV _{DSS}	60	70	—	V	V _{GS} = 0V, I _D = 10μA
Zero Gate Voltage Drain Current @ T _C = 25°C @ T _C = 125°C	I _{DSS}	—	—	1.0 500	μA	V _{DS} = 60V, V _{GS} = 0V
Gate-Body Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage	V _{GS(th)}	1.0	—	2.5	V	V _{DS} = V _{GS} , I _D = 250μA
Satic Drain-Source On-Resistance	R _{DS (ON)}	— —	— —	7.5 13.5	Ω	V _{GS} = 5V, I _D = 0.05A, V _{GS} = 10V, I _D = 0.5A, T _j = 125°C
On-State Drain Current	I _{D(ON)}	0.5	1.0	—	A	V _{GS} = 10V, V _{DS} = 7.5V
Forward Transconductance	g _{FS}	80	—	—	mS	V _{DS} = 10V, I _D = 0.2A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{iss}	—	—	50	pF	V _{DS} = 25V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C _{rss}	—	—	5.0	pF	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{D(ON)}	—	—	20	ns	V _{DD} = 30V, I _D = 0.2A, R _L = 150Ω, V _{GEN} = 10V, R _{GEN} = 25Ω
Turn-Off Delay Time	t _{D(OFF)}	—	—	20	ns	

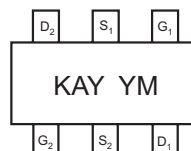
Ordering Information (Note 5)

Device	Packaging	Shipping
2N7002V-7	SOT-563	3000/Tape & Reel
2N7002VA-7	SOT-563	3000/Tape & Reel
2N7002V-7-L	SOT-563	3000/Tape & Reel
2N7002VA-7-L	SOT-563	3000/Tape & Reel

- Notes:
- Short duration test pulse used to minimize self-heating effect.
 - For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.
 - "-L" suffix on part number indicates Pb/Sn terminal plating. "-L" version is a Non Lead-Free, Non RoHS-compliant device.

Marking Information


KAS = 2N7002V Product Type Marking Code
 (See Note 1)
 YM = Date Code Marking
 Y = Year ex: R = 2004
 M = Month ex: 9 = September



KAY = 2N7002VA Product Type Marking Code
 (See Note 1)
 YM = Date Code Marking
 Y = Year ex: R = 2004
 M = Month ex: 9 = September

Date Code Key

Year	2004	2005	2006	2007	2008	2009
Code	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

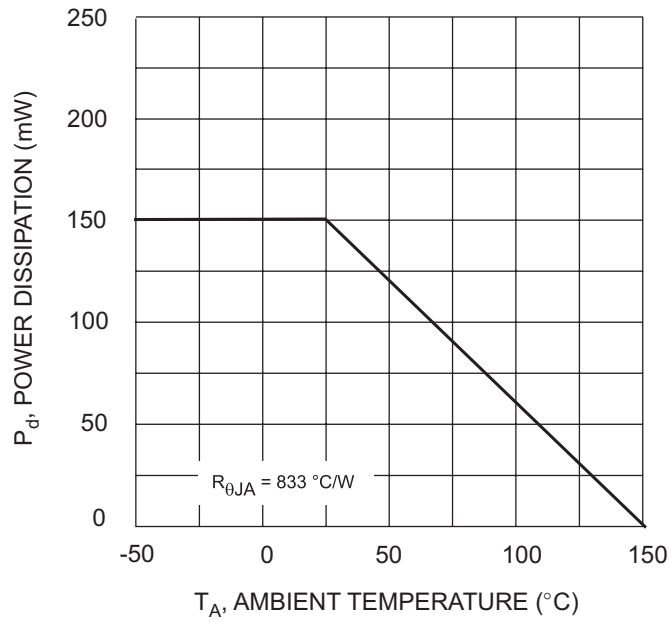


Fig. 1, Derating Curve - Total