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S1D13709
Embedded Memory Graphics LCD Controller

Hardware Functional Specification

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SEIKO EPSON CORPORATION

Rev. 1.1

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1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13709. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

We appreciate your comments on our documentation. Please contact us via email at vdc-documentation@ea.epson.com.

1.2 Overview Description

The S1D13709 is the LCD controller compatible with the S1D13700. It supports TFT LCD interface in addition to the S1D13700 function. The S1D13709 has flexible up-scaler and it can use WVGA TFT LCD with this function.

The S1D13709 can display both text and graphics on an LCD panel. The S1D13709 allows layered text and graphics, scrolling of the display in any direction, and partitioning of the display into multiple screens. It includes 32K bytes of embedded SRAM display memory which is used to store text, character codes, and bit-mapped graphics. The S1D13709 handles display controller functions including: transferring data from the controlling micro-processor to the buffer memory, reading memory data, converting data to display pixels, and generating timing signals for the LCD panel.

The S1D13709 is designed with an internal character generator which supports 160, 5x7 pixel characters in internal mask ROM (CGROM) and 64, 8x8 pixel characters in character generator RAM (CGRAM). When the CGROM is not used, up to 256, 8x16 pixel characters are supported in CGRAM.

2 Features

2.1 Internal Memory

- Embedded 32K bytes of SRAM display memory

2.2 Host CPU Interface

- Direct Address Bus support for:
  - Generic Bus (Z80 family) microprocessor interface
  - MC68K family microprocessor interface
- Indirect Address Bus support for:
  - Generic Bus (Z80 family) microprocessor interface
  - MC68K family microprocessor interface
  - M6800 family microprocessor interface
- 8-bit CPU data bus interface

2.3 Display Support

- STN-LCD
  - 4-bit monochrome LCD interface
  - Maximum resolutions supported:
    640x240 at 1 bpp
    320x240 at 2 bpp
    240x160 at 4 bpp
  - 1/2-duty to 1/256-duty LCD drive
- TFT-LCD
  - 4-bit monochrome LCD interface
  - 6-bit color palette LCD interface
  - Maximum resolutions supported:
    800x480
  - Up-scaler adjusts output image size for various LCD's

2.4 Display Modes

- 1/2/4 bit-per-pixel color depth support
- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Programmable cursor control
- Smooth horizontal scrolling of all or part of the display in monochrome mode
- Smooth vertical scrolling of all or part of the display in all modes
- Color Palette mode for the TFT interface

2.5 Character Generation

- 160, 5x7 pixel characters in embedded mask-programmed character generator ROM (CGROM)
- Up to 64, 8x8 pixel characters in character generator RAM (CGRAM)
- Up to 256, 8x16 pixel characters in embedded character generator RAM (when CGROM is not used)

2.6 Power

- Software initiated power save mode
- Low power consumption
- CORE V_{DD} 3.0 to 5.5 volts
- PLL V_{DD} 3.0 to 5.5 volts
- IO V_{DD} 3.0 to 5.5 volts

2.7 Clock Source

- Two terminal crystal or Single Oscillator input
  Input Clock (maximum 66 MHz)
  STN-Clock (XSCL) (maximum 15 MHz)
  TFT-Clock (FPSHIFT) (maximum 35MHz)

2.8 Package

- TQFP14 - 80-pin Pb-free package (lead free)

3 System Diagrams

3.1 Host Interface Connections

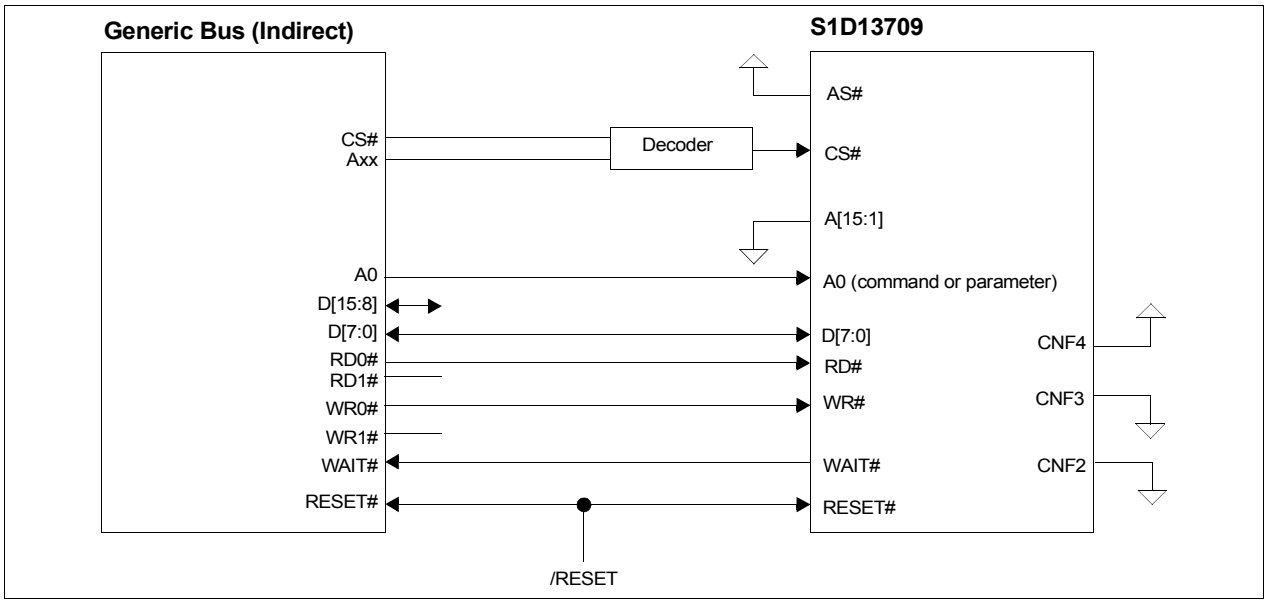


Figure 3-1 Indirect Generic to S1D13709 Interface Example

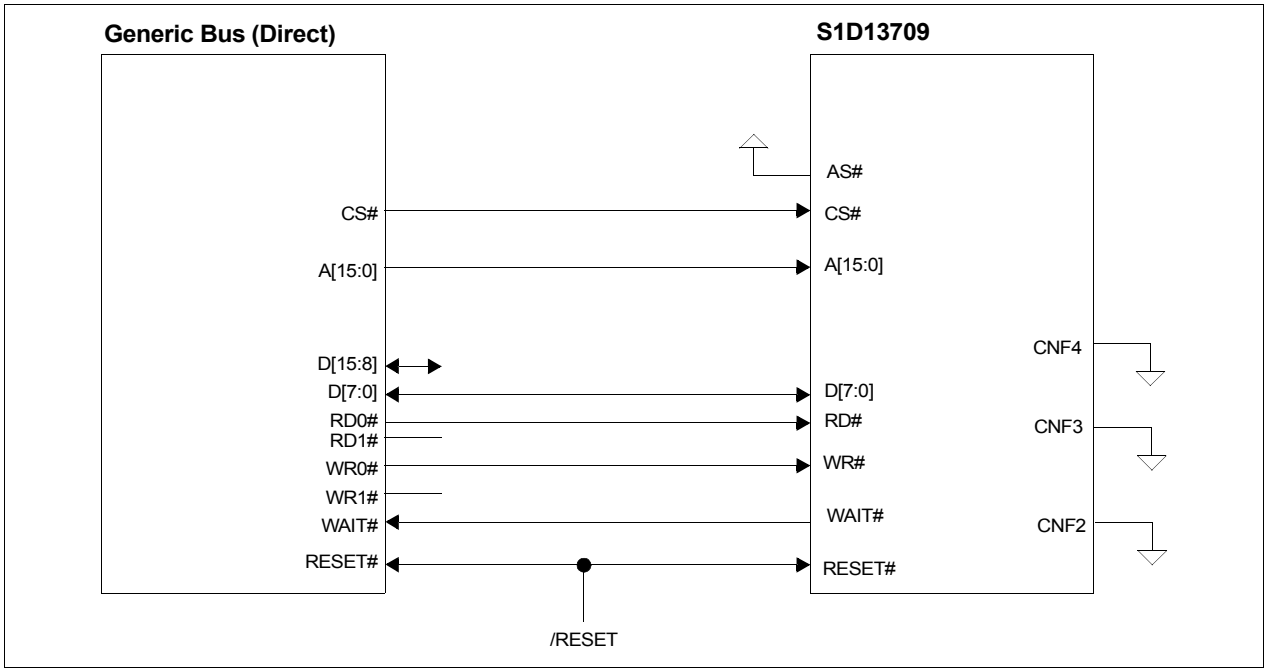


Figure 3-2 Direct Generic to S1D13709 Interface Example

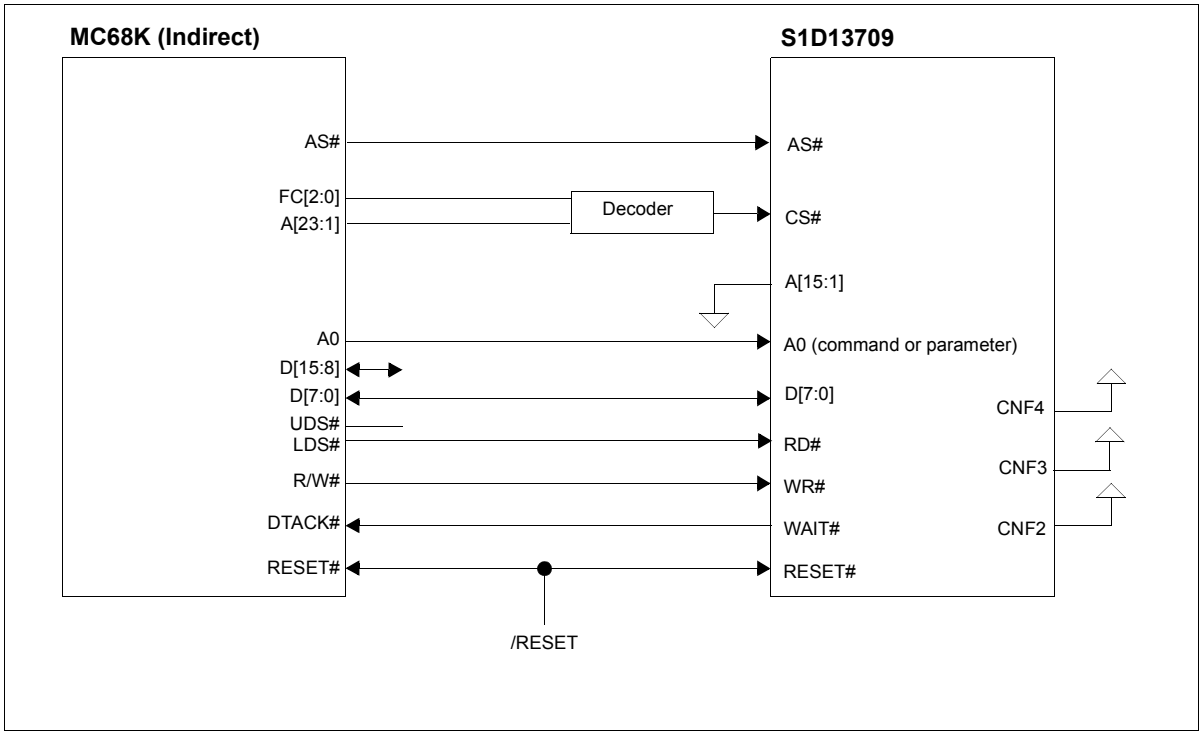


Figure 3-3 Indirect MC68K to S1D13709 Interface Example

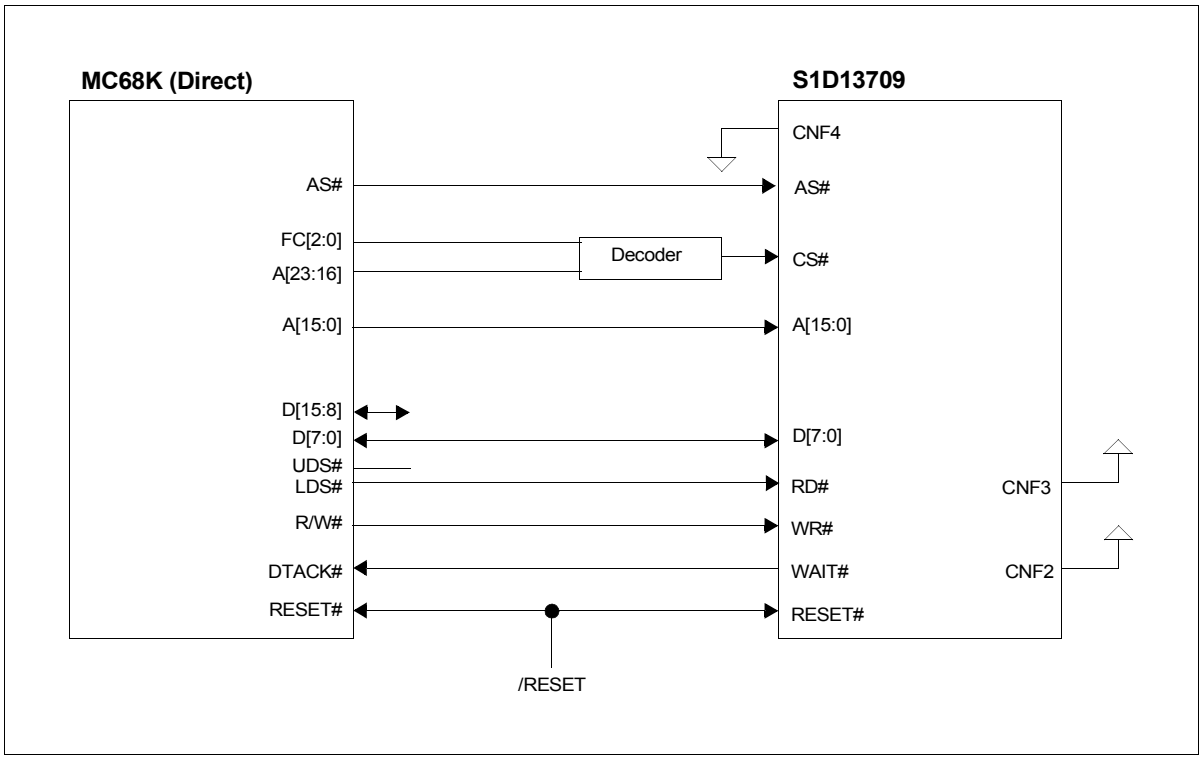


Figure 3-4 Direct MC68K to S1D13709 Interface Example

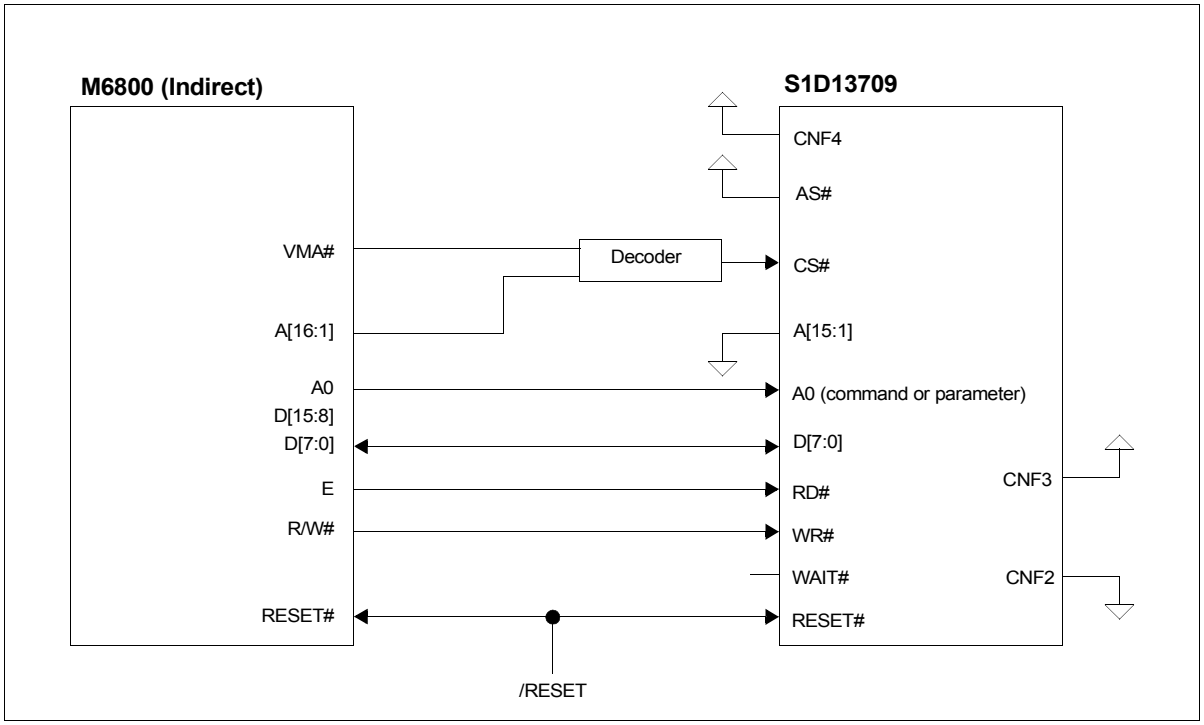


Figure 3-5 Indirect M6800 to S1D13709 Interface Example

3.2 LCD Interface Connections

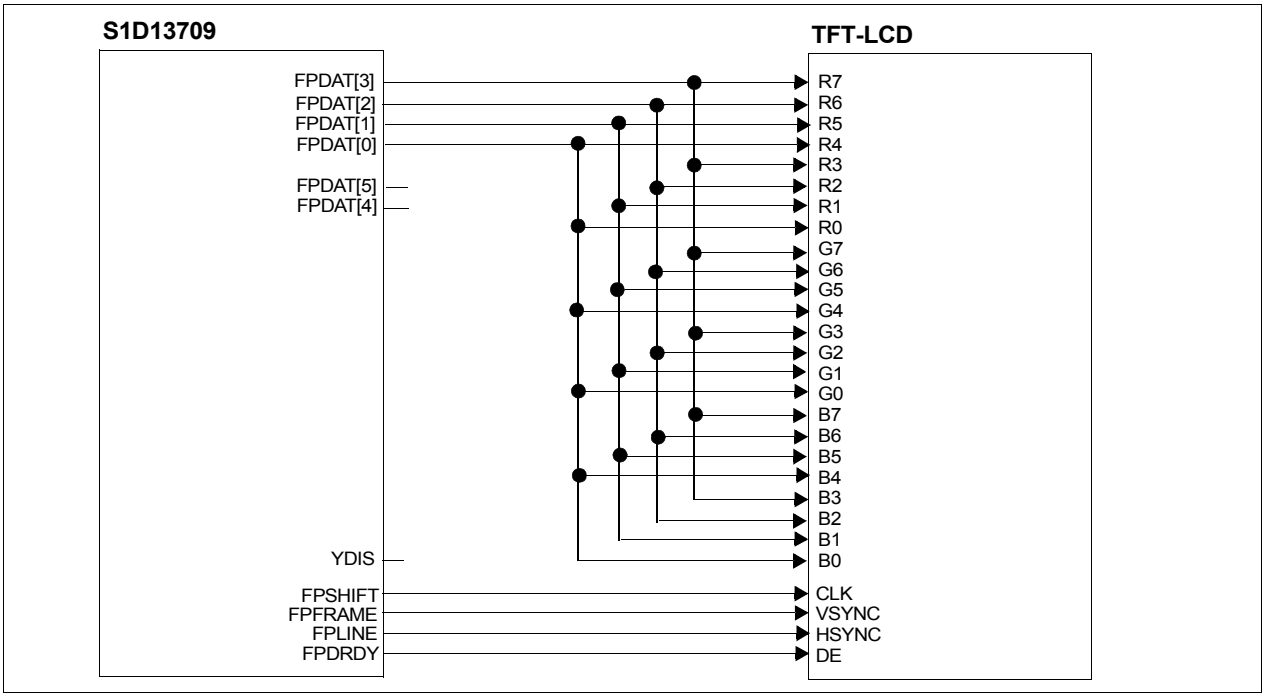


Figure 3-6 S1D13709 to TFT-LCD Example (Gray Scale Mode, REG[34h]bit1 = 0)

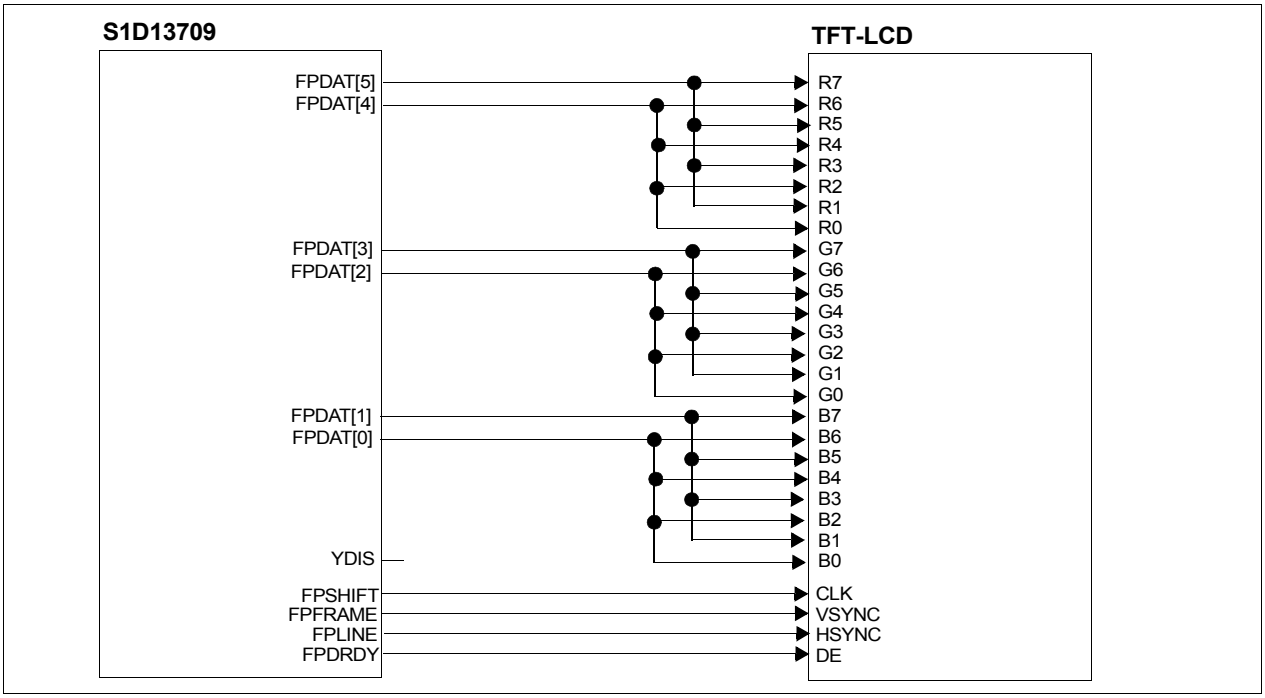


Figure 3-7 S1D13709 to TFT-LCD Example (Color Palette Mode, REG[34h]bit1 = 1)

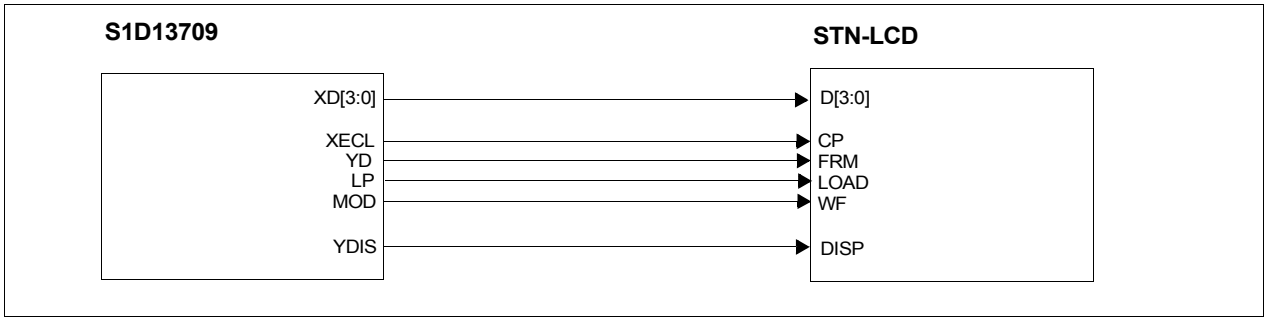


Figure 3-8 S1D13709 to STN-LCD Example

4 Functional Block Diagram

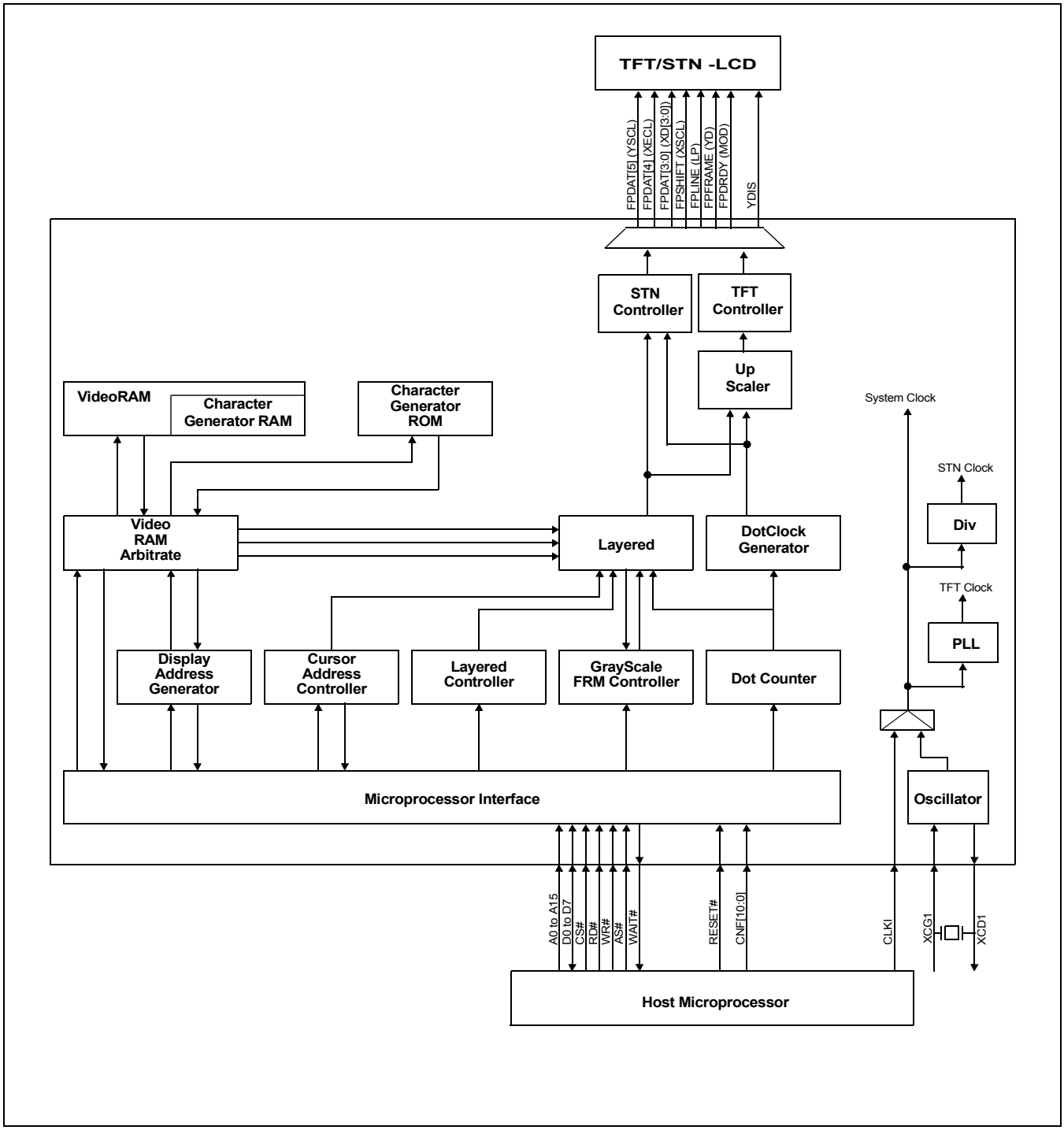


Figure 4-1 Functional Block Diagram

5 Pins

5.1 Pinout Diagram

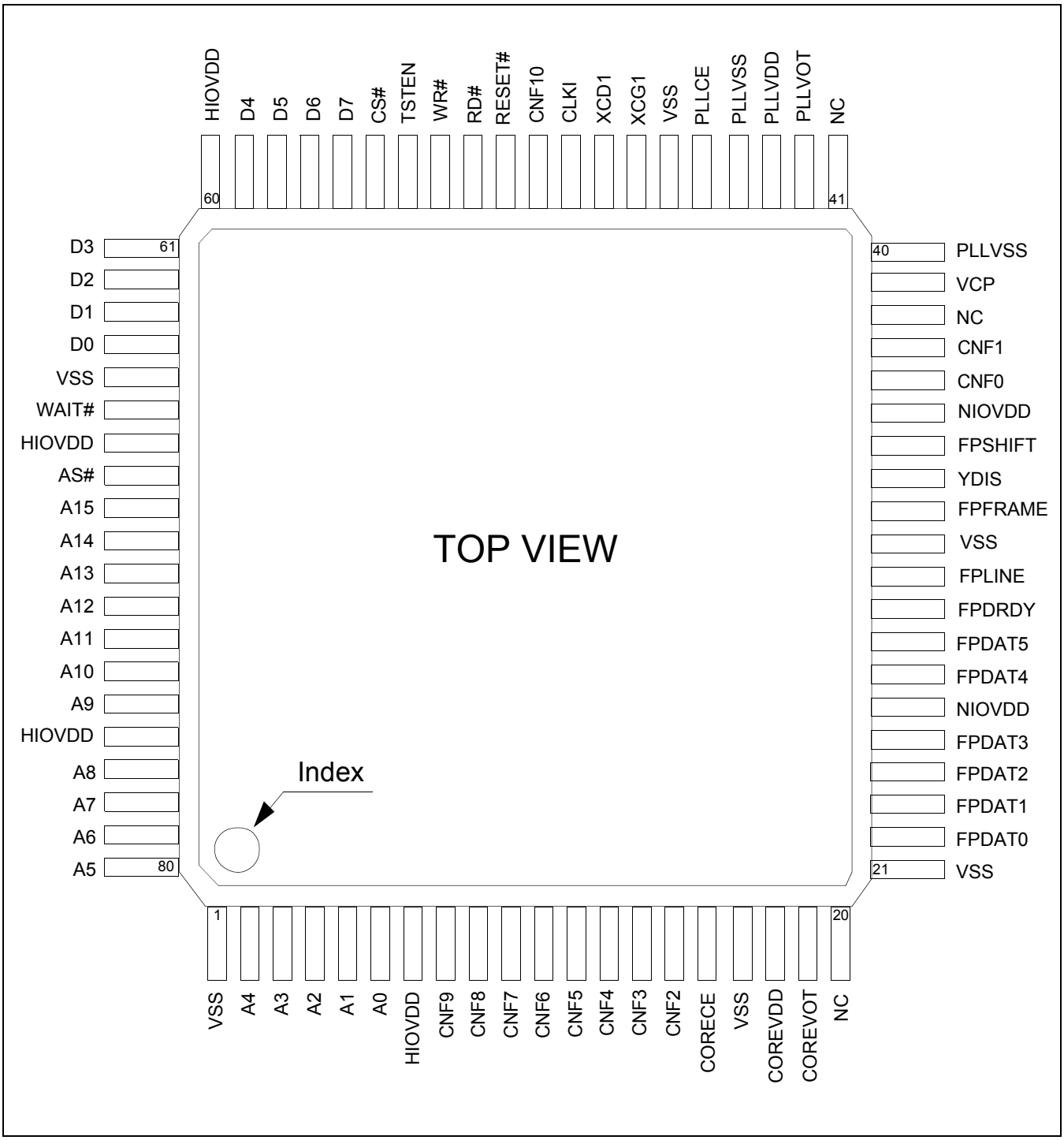


Figure 5-1 Pinout Diagram (TQFP14 - 80 pin)

5.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# and Power On States

Z	=	High Impedance (Hi-Z)
L	=	Low level output
H	=	High level output
0	=	Pull-down control on input
1	=	Pull-up control on input
X	=	Undetermined
—	=	Not applicable

Table 5-1: Cell Descriptions

Item	Description
CI	CMOS input
SI	CMOS Schmitt input
OBSEL	CMOS output buffer with Drive Selector (2mA or 6mA@3.3V, 3mA or 8mA@5V)
IOB	CMOS Input/Output buffer (6mA@3.3V, 8mA@5V)
TOB	Tri-state output buffer (6mA@3.3V, 8mA@5V)
LIN	Transparent input
LOT	Transparent output

5.2.1 Host Interface

Many of the host interface pins have different functions depending on the selection of the host bus interface (see configuration of CNF[4:2] pins in Table 5-7: "Summary of Configuration Options 1," on page 25). For a summary of host interface pins, see Table 5-10: "Host Interface Pin Mapping," on page 27.

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
A15	I	69	CI	HIOVDD	—	System Address pins 15-1. • For Direct addressing mode, these pins are used for the system address bits 15-1. • For Indirect addressing mode, these pins must be connected to ground (VSS).
A14	I	70	CI	HIOVDD	—	
A13	I	71	CI	HIOVDD	—	
A12	I	72	CI	HIOVDD	—	
A11	I	73	CI	HIOVDD	—	
A10	I	74	CI	HIOVDD	—	
A9	I	75	CI	HIOVDD	—	
A8	I	77	CI	HIOVDD	—	
A7	I	78	CI	HIOVDD	—	
A6	I	79	CI	HIOVDD	—	
A5	I	80	CI	HIOVDD	—	
A4	I	2	CI	HIOVDD	—	
A3	I	3	CI	HIOVDD	—	
A2	I	4	CI	HIOVDD	—	
A1	I	5	CI	HIOVDD	—	
A0	I	6	CI	HIOVDD	—	System Address pin 0. • For Direct addressing mode, this pin is used for system address bit 0. • For Indirect addressing mode, this pin in conjunction with RD# and WR# determines the type of data present on the data bus.
D7	IO	56	IOB	HIOVDD	Z	System data bus pins 7-0. These tristate input/output data pins must be connected to the microprocessor data bus.
D6	IO	57	IOB	HIOVDD	Z	
D5	IO	58	IOB	HIOVDD	Z	
D4	IO	59	IOB	HIOVDD	Z	
D3	IO	61	IOB	HIOVDD	Z	
D2	IO	62	IOB	HIOVDD	Z	
D1	IO	63	IOB	HIOVDD	Z	
D0	IO	64	IOB	HIOVDD	Z	

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
CNF10	I	50	SI	HIOVDD	—	These input pins select the TFT-LCD Automatic Setting Mode and must be connected to either HIOVDD or VSS. For further information, see Section 5.3, “Summary of Configuration Options” on page 25.
CNF9	I	8	SI	HIOVDD	—	
CNF8	I	9	SI	HIOVDD	—	
CNF7	I	10	SI	HIOVDD	—	
CNF6	I	11	SI	HIOVDD	—	
CNF5	I	12	SI	HIOVDD	—	
CNF4	I	13	SI	HIOVDD	—	This input pin selects the microprocessor addressing mode and must be connected to either HIOVDD or VSS. The S1D13709 supports both Direct and Indirect addressing modes. For further information, see Section 5.3, “Summary of Configuration Options” on page 25.
CNF3	I	14	SI	HIOVDD	—	These input pins select the host bus interface (microprocessor interface) and must be connected to either HIOVDD or VSS. The S1D13709 supports Generic processors (such as the 8085 and Z80®), the MC68K family of processors (such as the 68000) and the M6800 family of processors (such as the 6800). For further information, see Section 5.3, “Summary of Configuration Options” on page 25.
CNF2	I	15	SI	HIOVDD	—	
CNF1	I	37	SI	NIOVDD	—	These input pins are used for configuration of the XSCL clock cycle time and must be connected to either NIOVDD or VSS. For further information, see Section 5.3, “Summary of Configuration Options” on page 25.
CNF0	I	36	SI	NIOVDD		
RD#	I	52	SI	HIOVDD	—	This input pin has multiple functions. • When the Generic host bus interface is selected, this pin is the active-LOW read strobe (RD#). The S1D13709 data output buffers are enabled when this signal is low. • When the M6800 host bus interface is selected, this pin is the active-high enable clock (E). Data is read from or written to the S1D13709 when this clock goes high. • When the MC68K host bus interface is selected, this pin is the active-low lower data strobe (LDS#). Data is read from or written to the S1D13709 when this signal goes low.
WR#	I	53	SI	HIOVDD	—	This input pin has multiple functions. • When the Generic host bus interface is selected, this signal is the active-low write strobe (WR#). The bus data is latched on the rising edge of this signal. • When the M6800 host bus interface is selected, this signal is the read/write control signal (R/W#). Data is read from the S1D13709 if this signal is high, and written to the S1D13709 if it is low. • When the MC68K host bus interface is selected, this signal is the read/write control signal (RD/WR#). Data is read from the S1D13709 if this signal is high, and written to the S1D13709 if it is low.

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
CS#	I	55	SI	HIOVDD	—	Chip select. This active-low input enables the S1D13709. It is usually connected to the output of an address decoder device that maps the S1D13709 into the memory space of the controlling microprocessor.
WAIT#	O	66	TOB	HIOVDD	Z	This output pin has multiple functions. • When the Generic host bus interface is selected, this pin is WAIT#. During a data transfer, WAIT# is driven active-low to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to a high impedance state after the data transfer is complete. For indirect addressing mode, the WAIT# pin can be used to handshake with the Host. • When the MC68K host bus interface is selected, this pin is DTACK#. During a data transfer, DTACK# is driven active-high to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. DTACK# is released to a high impedance state after the data transfer is complete. For indirect addressing mode, the DTACK# pin can be used to handshake with the Host. • When the M6800 host bus interface is selected, this pin must be left unconnected and floating.
AS#	I	68	CI	HIOVDD	—	This input pin has multiple functions. • When the Generic host bus interface is selected, this pin must be connected to VDD (pulled high). • When the MC68K host bus interface is selected, this pin is the address strobe (AS#). • When the M6800 host bus interface is selected, this pin must be connected to VDD (pulled high).
RESET#	I	51	SI	HIOVDD	—	This active-low input performs a hardware reset of the S1D13709 which sets all internal registers to their default states and forces all signals to their inactive states. Note: Do not trigger a RESET# when the supply voltage is lowered.

5.2.2 LCD Interface

In order to provide effective low-power drive for LCD matrixes, the S1D13709 can directly control both the X and Y-drivers using an enable chain.

Table 5-3 LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
FPDAT5 (YSCL)	O	28	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data output. (FPDAT5) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (YSCL). The falling edge of YSCL latches the data on YD into the input shift registers of the Y-drivers. YSCL is not used with driver ICs which use LP as the Y-driver shift clock.
FPDAT4 (XECL)	O	27	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data output. (FPDAT4) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (XECL). The falling edge of XECL triggers the enable chain cascade for the X-drivers. Every 16th clock pulse is output to the next X-driver.
FPDAT3 (XD3)	O	25	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data output. (FPDAT[3:0]) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN data output (XD[3:0]). XD[3:0] are the 4-bit X-driver (column drive) data outputs and must be connected to the inputs of the X-driver chips.
FPDAT2 (XD2)	O	24	OBSEL	NIOVDD	L	
FPDAT1 (XD1)	O	23	OBSEL	NIOVDD	L	
FPDAT0 (XD0)	O	22	OBSEL	NIOVDD	L	
FPDRDY (MOD)	O	29	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data enable output. (FPDRDY) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (MOD). MOD is the LCD panel backplane bias signal. The MOD period is selected using the SYSTEM SET command.

Table 5-3 LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
FPLINE (LP)	O	30	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT HSYNC output. (FPLINE) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (LP). LP latches the signal in the X-driver shift registers into the output data latches. LP is a falling edge triggered signal, and pulses once every display line. LP must be connected to the Y-driver shift clock on LCD modules.
FPFRAME (YD)	O	32	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT VSYNC output. (FPFRAME) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (YD). YD is the data pulse output for the Y drivers. It is active during the last line of each frame, and is shifted through the Y drivers one by one (by YSCL), to scan the display's common connections.
FPSHIFT (XSCL)	O	34	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT clock output. (FPSHIFT) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN clock output (XSCL). The falling edge of XSCL latches the data on FPDAT[3:0] into the input shift registers of the X-drivers. As XSCL is generated to synchronize with XECL, the total output of the XSCL clock for one line is a multiple of 16. To conserve power, this clock is stopped between LP and the start of the following display line.
YDIS	O	33	OBSEL	NIOVDD	L	This pin is used for the STN interface only (REG[34h] bit 0 =0). This output pin is the power-down output signal. YDIS is high while the display drive outputs are active. YDIS goes low one or two frames after the power save command is written to the S1D13709. All Y-driver outputs are forced to an intermediate level (de-selecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS. When the TFT interface is selected (REG[34h] bit 0 =1), this pin must be left unconnected.

5.2.3 Clock Input

Table 5-4 Clock Input Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
XCG1	I	47	LIN	HIOVDD	—	This input pin is the crystal connection for use with the internal oscillator. This pin must be pulled down when using an external clock source (CLKI). For further information on the use of the internal oscillator, see Section 9.3, “Oscillator Circuit” on page 61.
XCD1	O	48	LOT	HIOVDD	—	This output pin is the crystal connection for use with the internal oscillator. This pin must be left unconnected when using an external clock source (CLKI). For further information on the use of the internal oscillator, see Section 9.3, “Oscillator Circuit” on page 61.
CLKI	I	49	SI	HIOVDD	—	This is the external clock input. This pin must be pulled down when using a crystal with the internal oscillator. For further information on clocks, see Section 9, “Clocks” on page 60.

5.2.4 Miscellaneous

Table 5-5 Miscellaneous Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
TSTEN	I	54	CI	HIOVDD	—	This pin is used for production test only and must be connected to ground (VSS).
COREVOT	O	19	LOT	COREVDD	—	This pin is used for production test only and must be connected to VSS via a 1uF capacitor.
CORECE	I	16	LIN	COREVDD	—	This pin is used for production test only and must be connected to COREVDD.
PLLVOT	O	42	LOT	PLLVDD	—	This pin is used for production test only and must be connected to PLLVSS via a 1uF capacitor.
PLLCE	I	45	LIN	PLLVDD	—	This pin is used for production test only and must be connected to PLLVDD.
VCP	O	39	LOT	PLLVDD	—	This pin is used for production test only and must be left unconnected.

5.2.5 Power And Ground

Table 5-6 Power And Ground Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
HIOVDD	P	7,67,76	P	—	—	IO power supply for the Host (MPU) interface, 3.3/5.0 volts. A 0.1uF bypass capacitor is necessary between each HIOVDD and VSS.
NIOVDD	P	26,35	P	—	—	IO power supply for the LCD interface, 3.3/5.0 volts. A 0.1uF bypass capacitor is necessary between each NIOVDD and VSS.
COREVDD	P	18	P	—	—	Core power supply, 3.3/5.0 volts. A 1uF bypass capacitor is necessary between COREVDD and VSS.
PLLVDD	P	43	P	—	—	PLL power supply, 3.3/5.0 volts. A 1uF bypass capacitor is necessary between PLLVDD and PLLVSS.
VSS	P	1,17,21 ,31,46, 65	P	—	—	Ground for HIOVDD, NIOVDD and COREVDD
PLLVSS	P	40,44	P	—	—	Ground for PLLVDD

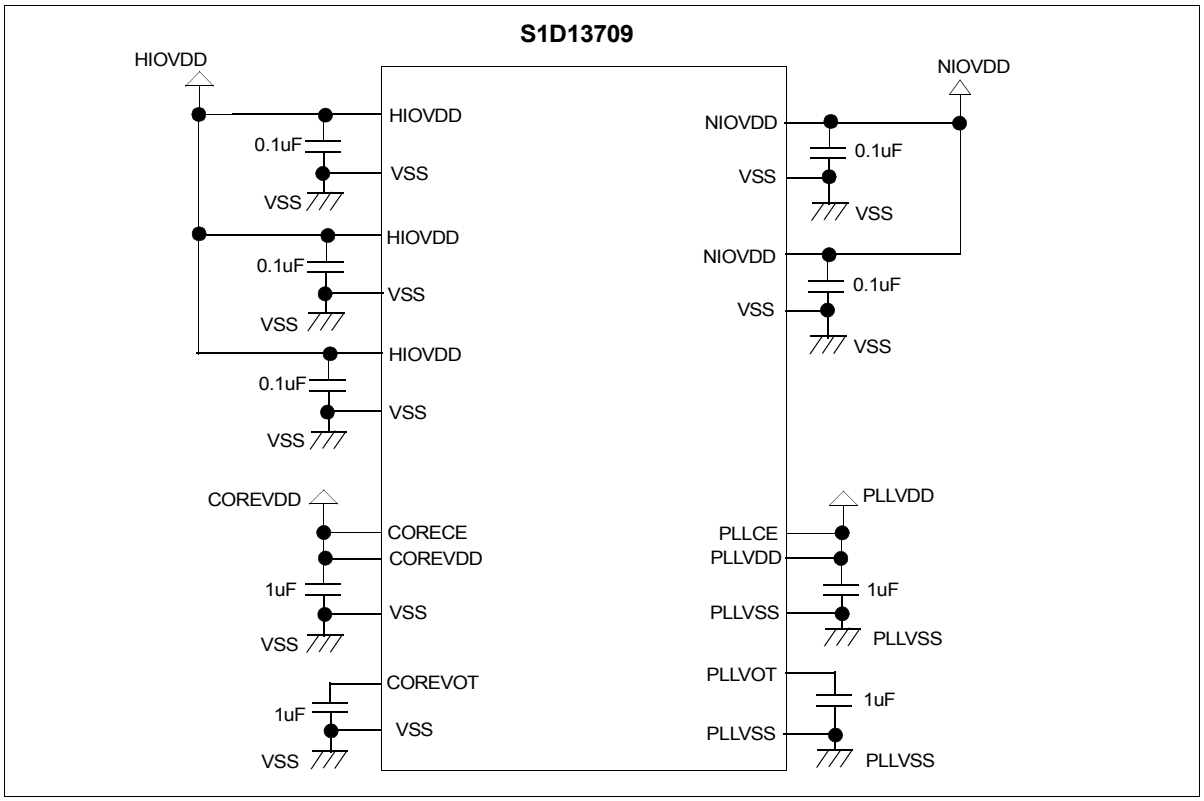


Figure 5-2 Power and Ground Connection

5.3 Summary of Configuration Options

These pins are used for configuration of the chip and must be connected directly to HIOVDD(NIOVDD) or VSS.

Note
The state of CNF[10:0] must be set before the initial sequence.

Table 5-7: Summary of Configuration Options 1

Configuration Input	Configuration State	
	1 (connected to HIOVDD)	**0 (connected to VSS)**
CNF10	CLKI(XCG1) frequency at the TFT-LCD Automatic Setting Mode **CNF10 CLKI(XCG1) Frequency** 0CLKI (XCG1) frequency is 20MHz. 1CLKI (XCG1) frequency is 24MHz. **Note**: This pin is available only when the TFT-LCD Automatic Setting Mode is enabled. (CNF[7:5] = 001, 010, 011 or 100) When the TFT-LCD automatic setting mode is disabled (CNF[7:5]=000), this pin should be 0.	
CNF9	TFT interface output drive control at the TFT-LCD Automatic Setting Mode **CNF9 TFT Interface Output Drive Control** 0 TFT interface output drive is 2mA@3.3V (3mA@5V). 1 TFT interface output drive is 6mA@3.3V (8mA@5V). **Note**: This pin is available only when the TFT-LCD Automatic Setting Mode is enabled. (CNF[7:5] = 001, 010, 011 or 100) When the TFT-LCD automatic setting mode is disabled (CNF[7:5]=000), this pin should be 0.	
CNF8	FPSHIFT Polarity at the TFT-LCD Automatic Setting Mode **CNF8 FPSHIFT Polarity** 0All output video signals change at the falling edge of FPSHIFT. 1All output video signals change at the rising edge of FPSHIFT. **Note**: This pin is available only when the TFT-LCD Automatic Setting Mode is enabled. (CNF[7:5] = 001, 010, 011 or 100) When the TFT-LCD automatic setting mode is disabled (CNF[7:5]=000), this pin should be 0.	
CNF[7:5]	Select the TFT-LCD Automatic Setting Mode. For further details on internal clocks, see Section 15.2, “TFT interface automatic setting mode” on page 172.: **CNF7CNF6 CNF5 TFT-LCD Automatic Setting Mode** 00 0 Disable (Manual setting) 00 1 S1D13700 S/W: QVGA → TFT: QVGA (320 x 240) 01 0 S1D13700 S/W: QVGA → TFT: WQVGA (480 x 272) 01 1 S1D13700 S/W: QVGA → TFT: VGA (640 x 480) 10 0 S1D13700 S/W: QVGA → TFT: WVGA (800 x 480) 10 1 Reserved 11 0 Reserved 11 1 Reserved **Note**: When the STN Interface is used (REG[34h] bit0 = 0), CNF[7:5] should be 000.	

Table 5-8: Summary of Configuration Options 2

Configuration Input	Configuration State	
	1 (connected to HIOVDD)	**0 (connected to VSS)**
CNF4	Indirect Addressing Mode: 1-bit address bus 8-bit data bus 9 pins are used	DIrect Addressing Mode: 16-bit address bus 8-bit data bus 24 pins are used
CNF[3:2]	Select the host bus interface as follows: **CNF3CNF2Host Bus** 00 Generic Bus 01 Reserved 10 M6800 Family Bus Interface 11 MC68K Family Bus Interface	

Table 5-9: Summary of Configuration Options 3

Configuration Input	Configuration State	
	1 (connected to NIOVDD)	**0 (connected to VSS)**
CNF[1:0]	Select the XSCL cycle time (XSCL:Clock Input) as follows: For 1bpp mode (REG[20h] bits 1-0 = 00) **CNF1CNF0XSCL Cycle Time** 00 4:1 01 8:1 10 16:1 11 Reserved For 2bpp mode (REG[20h] bits 1-0 = 01) **CNF1CNF0XSCL Cycle Time** 00 8:1 01 16:1 10 32:1 11 Reserved For 4bpp mode (REG[20h] bits 1-0 = 10) **CNF1CNF0XSCL Cycle Time** 00 16:1 01 32:1 10 64:1 11 Reserved **Note**: When the TFT Interface is used (REG[34h] bit0 =1), CNF[1:0] should be 00.	

5.4 Host Bus Interface Pin Mapping

Table 5-10: Host Interface Pin Mapping

Pin Name	Generic Direct	Generic Indirect	MC68K Direct	MC68K Indirect	M6800 Direct	M6800 Indirect
A[15:1]	A[15:1]	Connected to VSS	A[15:1]	Connected to VSS	Not supported	Connected to VSS
A0	A0	A0	A0	A0		A0
D[7:0]	D[7:0]	D[7:0]	D[7:0]	D[7:0]		D[7:0]
CS#	CS#	CS#	External Decode	External Decode		External Decode
AS#	Connected to HIOVDD	Connected to HIOVDD	AS#	AS#		Connected to HIOVDD
RD#	RD#	RD#	LDS#	LDS#		E
WR#	WR#	WR#	RD/WR#	RD/WR#		R/W#
WAIT#	WAIT# or Unconnected		DTACK# or Unconnected			Unconnected
RESET#	RESET#	RESET#	RESET#	RESET#		RESET#
CNF4	Connected to VSS	Connected to HIOVDD	Connected to VSS	Connected to HIOVDD		Connected to HIOVDD
CNF3	Connected to VSS	Connected to VSS	Connected to HIOVDD	Connected to HIOVDD		Connected to HIOVDD
CNF2	Connected to VSS	Connected to VSS	Connected to HIOVDD	Connected to HIOVDD		Connected to VSS
CNF[1:0]	See Note	See Note	See Note	See Note		See Note

Note

CNF[1:0] are used to configure the XSCL cycle time and must be set according to the requirements of the specific implementation.

6 D.C. Characteristics

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
CORE V_{DD}	Supply Voltage	V_{SS} - 0.3 to 7.0	V
PLL V_{DD}	Supply Voltage	$PLLV_{SS}$ - 0.3 to 7.0	V
IO V_{DD}	Supply Voltage	V_{SS} - 0.3 to 7.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} - 0.3 to IO V_{DD} + 0.5	V
Iout_io	Digital Output Signal Current	±10	mA
Tstg	Storage Temperature	-65 ~ 150	°C

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Supply Voltage	V_{SS} = 0 V	3.0	3.3	5.5	V
PLL V_{DD}	Supply Voltage	$PLLV_{SS}$ = 0 V	3.0	3.3	5.5	V
HIO V_{DD}	Host Bus IO Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
			4.5	5.0	5.5	V
NIO V_{DD}	Panel IO Supply Voltage	V_{SS} = 0 V	3.0	3.3	3.6	V
			4.5	5.0	5.5	V
HIO V_{IN}	Host Input Voltage		V_{SS}		HIO V_{DD}	V
NIO V_{IN}	Non-Host Input Voltage		V_{SS}		NIO V_{DD}	V
T_{OPR}	Operating Temperature		-40	25	85	° C

Table 6-3 Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QH}	Core Quiescent Current	Power save mode enabled	—	—	150	µA
	IO Quiescent Current	Power save mode enabled	—	—	5	µA
I_{LZ}	Input Leakage Current		-1	—	1	µA
I_{OZ}	Off state Leakage Current		-1	—	1	µA
V_{OH}	High Level Output Voltage	$HIOV_{DD}$ = min. $NIOV_{DD}$ = min. I_{OH} = -2mA (Type1) I_{OH} = -6mA (Type2)	$HIOV_{DD}$-0.4 $NIOV_{DD}$-0.4	—	—	V
V_{OL}	Low Level Output Voltage	$HIOV_{DD}$ = min. $NIOV_{DD}$ = min. I_{OL} = 2mA (Type1) I_{OH} = 6mA (Type2)	—	—	0.4	V
V_{IH1}	High Level Input Voltage	CMOS Level, $HIOV_{DD}$ = max $NIOV_{DD}$ = max	2.2	—	—	V

Table 6-3 Electrical Characteristics for VDD = 3.3V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL1}	Low Level Input Voltage	CMOS Level, $HIOV_{DD}$ = min. $NIOV_{DD}$ = min.	—	—	0.8	V
V_{T+}	High Level Input Voltage	CMOS Schmitt	1.2	—	2.52	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt	0.75	—	1.98	V
V_{H1}	Hysteresis Voltage	CMOS Schmitt	0.3	—	—	V

Table 6-4 Electrical Characteristics for VDD = 5.0V typical

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QH}	Core Quiescent Current	Power save mode enabled	—	—	150	µA
	IO Quiescent Current	Power save mode enabled	—	—	10	µA
I_{LZ}	Input Leakage Current		-1	—	1	µA
I_{OZ}	Output Leakage Current		-1	—	1	µA
V_{OH}	High Level Output Voltage	$HIOV_{DD}$ = min. $NIOV_{DD}$ = min. I_{OH} = -3mA (Type1) I_{OH} = -8mA (Type2)	$HIOV_{DD}$-0.4 $NIOV_{DD}$-0.4	—	—	V
V_{OL}	Low Level Output Voltage	$HIOV_{DD}$ = min. $NIOV_{DD}$ = min. I_{OL} = 3mA (Type1) I_{OH} = 8mA (Type2)	—	—	0.4	V
V_{IH}	High Level Input Voltage	CMOS Level, $HIOV_{DD}$ = max $NIOV_{DD}$ = max	3.5	—	—	V
V_{IL}	Low Level Input Voltage	CMOS Level, $HIOV_{DD}$ = min. $NIOV_{DD}$ = min.	—	—	1.0	V
V_{T+}	High Level Input Voltage	CMOS Schmitt	2.0	—	4.0	V
V_{T-}	Low Level Input Voltage	CMOS Schmitt	0.8	—	3.1	V
V_H	Hysteresis Voltage	CMOS Schmitt	0.3	—	—	V

The following electrical characteristics from Table 6-3 “Electrical Characteristics for VDD = 3.3V typical,” on page 28 and Table 6-4 “Electrical Characteristics for VDD = 5.0V typical,” on page 29 apply to the following cell types.

Table 6-5 Cell Type Reference

Electrical Characteristic	Cell Type
V_{OH} / V_{OL}	OBSEL IOB TOB
V_{IH} / V_{IL}	CI IOB
V_{T+} / V_{T-}	SI
V_H	SI

6.1 Power Estimation Guidelines

The following information provides typical current consumption values for a variety of color depths and configurations. Current consumption is defined as ($I_{COREVDD}$ + I_{PLLVDD} + I_{HIOVDD} + I_{NIOVDD}). The following measurements are for COREVDD = 3.3V, HIOVDD = 3.3V, NIOVDD = 3.3V.

Table 6-6: STN Interface Typical Current Consumption Measurements (XSCL Clock Ratio = 1/4)

Panel Size	Clock Input		4 Bpp	2 Bpp	1 Bpp	Power Save	CORE VDD (mA)	PLL VDD (mA)	HIO VDD (mA)	NIO VDD (mA)
	CLKI (MHz)	Crystal (MHz)								
320 x 240	—	24			X	X	0.02	0.02	0.01	0.01
					X	—	2.44	0.02	0.01	3.16
				X		—	2.65	0.02	0.01	3.71
			X			—	2.54	0.02	0.01	1.46
	20	—			X	X	0.20 (Note)	0.02	0.06	0.01
					X	—	1.67	0.02	0.06	2.61
				X		—	1.86	0.02	0.06	3.11
			X			—	1.76	0.02	0.06	1.22

Note
Measured under MCLK active condition.

Table 6-7: TFT Interface Typical Current Consumption Measurements

Panel Size	Clock Input		4 Bpp	2 Bpp	1 Bpp	Power Save	CORE VDD (mA)	PLL VDD (mA)	HIO VDD (mA)	NIO VDD (mA)
	CLKI (MHz)	Crystal (MHz)								
800 x 480	—	24			X	X	0.02	0.02	0.01	0.01
					X	—	3.26	2.22	0.01	2.71
				X		—	3.33	2.22	0.01	2.94
			X			—	3.44	2.22	0.01	2.98
	20	—			X	X	0.20 (Note)	0.02	0.06	0.01
					X	—	2.36	1.89	0.06	2.33
				X		—	2.42	1.89	0.06	2.5
			X			—	2.51	1.89	0.06	2.52

Note
Measured under MCLK active condition.

7 A.C. Characteristics

Conditions: Core V_{DD} = 3.3V ± 10%
IO V_{DD} = 3.3V ± 10% or 5.0V ± 10%

T_{OPR} = -40° C to 85° C
T_{rise} and T_{fall} for all inputs must be ≤ 5 nsec (10% ~ 90%)
C_L = 30pF (Bus/MPU Interface)
C_L = 50pF (LCD Panel Interface)

Note

C_L includes a maximum pin capacitance of 5pF.

7.1 Power Sequence Timing

7.1.1 Power-on Sequence Timing

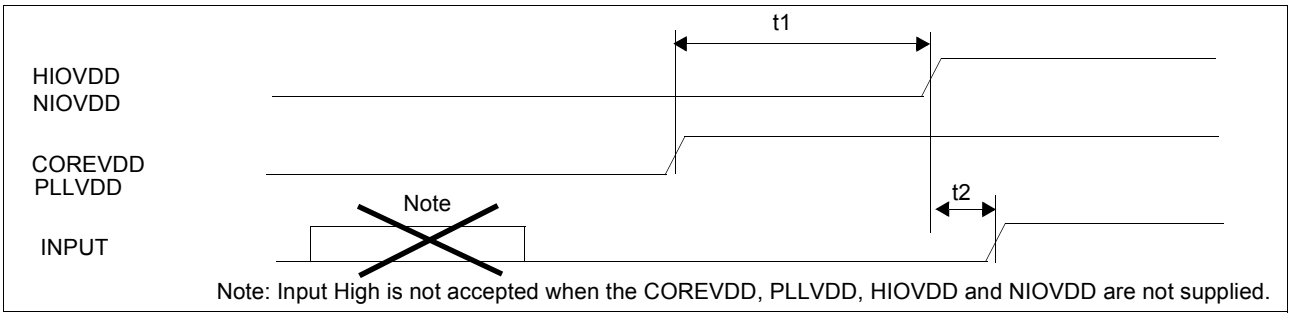


Figure 7-1: Power-on Sequence Timing

Table 7-1: Power-on Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	COREVDD rise to HIOVDD and NIOVDD rise	0	100 (Note)	ms
t2	HIOVDD and NIOVDD rise to all Inputs rise	0	-	ms

Note
During this time, there will be shoot through current.

7.1.2 Power-off Sequence Timing

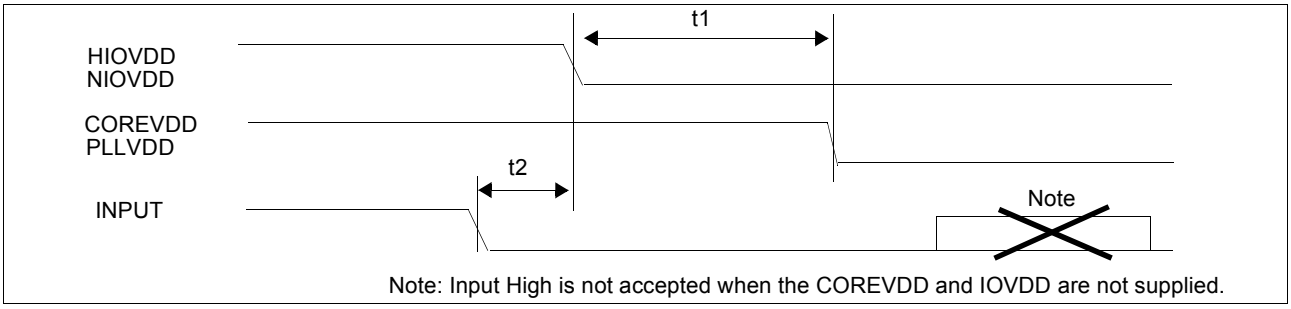


Figure 7-2: Power-off Sequence Timing

Table 7-2: Power-off Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	HIOVDD and NIOVDD fall to COREVDD fall	0	100	ms
t2	All inputs fall to HIOVDD and NIOVDD fall	0	-	ms

Note
During this time, there will be shoot through current.

7.2 Clock Timing

7.2.1 Input Clock (System Clock)

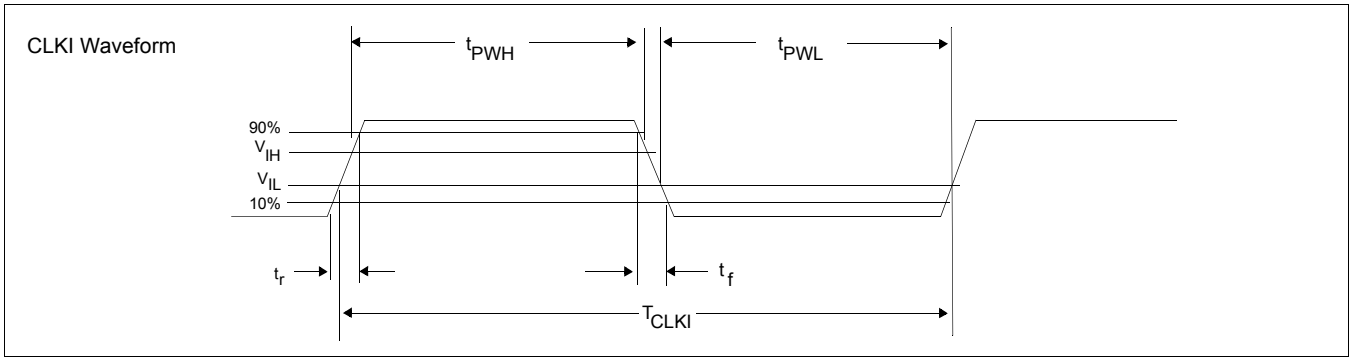


Figure 7-3 Clock Input Requirements

Table 7-3 Clock Input Requirements

Symbol	Parameter	3.0V		5.0V		Units
		Min	Max	Min	Max	
f_{CLKI}	Input Clock Frequency (CLKI)	10 (Note1,2)	66	10 (Note1,2)	66	MHz
T_{CLKI}	Input Clock period (CLKI)	$1/f_{CLKI}$	—	$1/f_{CLKI}$	—	ns
t_{PWH}	Input Clock Pulse Width High (CLKI)	$0.4T_{CLKI}$	—	$0.4T_{CLKI}$	—	ns
t_{PWL}	Input Clock Pulse Width Low (CLKI)	$0.4T_{CLKI}$	—	$0.4T_{CLKI}$	—	ns
t_f	Input Clock Fall Time (10% - 90%)	—	2	—	2	ns
t_r	Input Clock Rise Time (10% - 90%)	—	2	—	2	ns

Note

1. When the TFT interface is used (REG[34h] bit 0 =1), Minimum CLKI frequency depends on the TFT clock frequency. For further details on internal clocks, see Section Table 7-16:, “TFT-LCD interface Timing 1” on page 58.
2. When the TFT interface is used (REG[34h] bit 0 =1) and 4bpp is selected (REG[20h] bits 1-0 = 10), CLKI frequency must be equal or greater than 24MHz.

7.3 Reset Timing

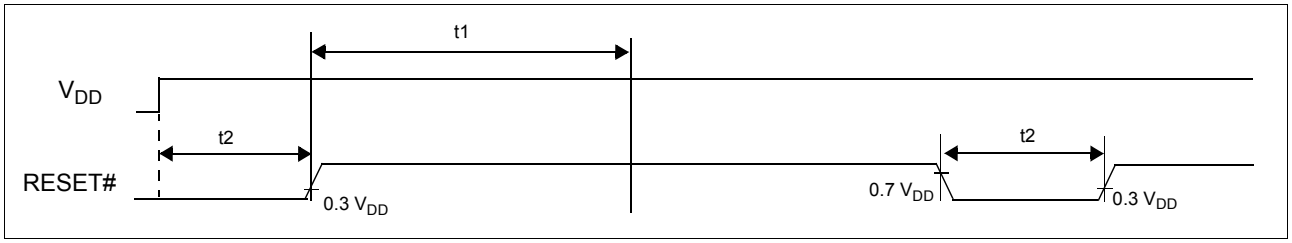


Figure 7-4 Reset Timing When Using An External Oscillator

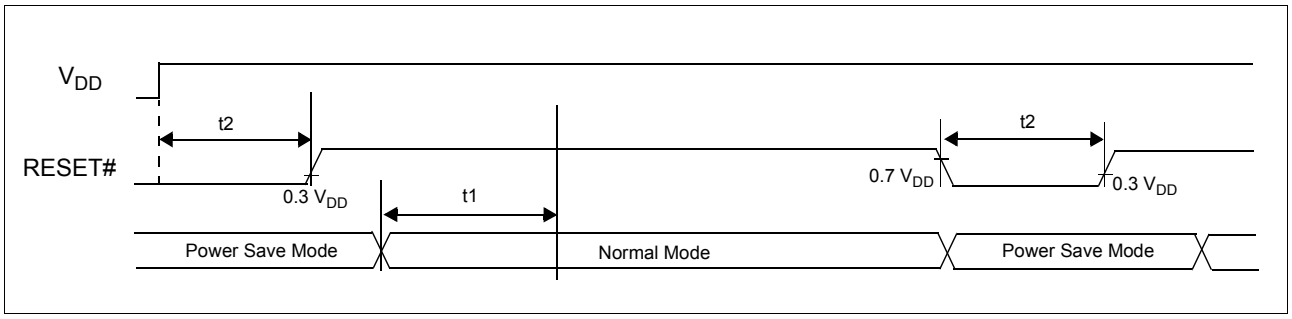


Figure 7-5 Reset Timing When Using Internal Oscillator With External Crystal

Table 7-4 Reset Timing

Symbol	Parameter	Min	Max	Units
t1	Oscillator stable delay	Note 1	—	ms
t2	Reset pulse duration	100 (Note 2)	—	ns

1. When using an external oscillator, a delay is required following the rising edges of both RESET# and VDD to allow for system stabilization. This delay allows the clock used by the internal oscillator circuit to become stable before use. The delay time depends on a crystal. The S1D13709 must not be accessed before the oscillation circuit is stable.

   When using the internal oscillator with an external crystal, a delay is required after exiting power save mode. For direct mode, writing REG[08h] bit 0 will exit power save mode and start the internal oscillator.
   For indirect mode, writing the SYSTEM SET command will exit power save mode and start the internal oscillator.

2. The S1D13709 requires a reset pulse of at least 100 ns after power-on in order to re-initialize its internal state. For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the S1D13709 is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

   Note that during the reset period the S1D13709 cannot receive commands. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals FPDAT, LP and FR are halted.

7.4 CPU Interface Timing

7.4.1 Generic Bus Indirect Interface with WAIT# Timing

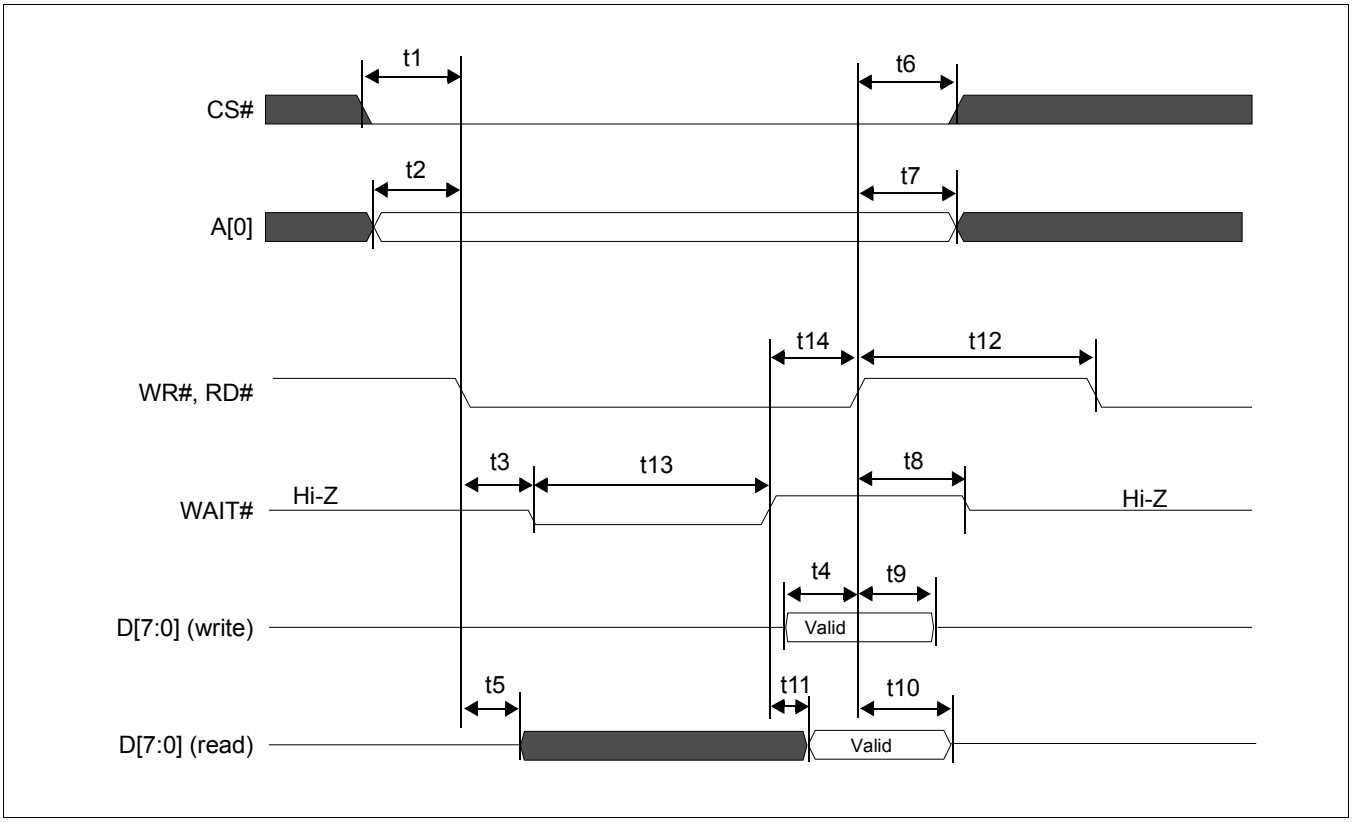


Figure 7-6 Generic Bus Indirect Interface with WAIT# Timing

Table 7-5 Generic Bus Indirect Interface with WAIT# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[0] setup time	5	—	5	—	ns
t3	WR#, RD# falling edge to WAIT# driven low	2	15	2	15	ns
t4	D[7:0] setup time to WR# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t5	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t6	CS# hold time	7	—	7	—	ns
t7	A[0] hold time	7	—	7	—	ns
t8	RD#, WR# rising edge to WAIT# high impedance	2	10	2	10	ns
t9	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t10	D[7:0] hold time from RD# rising edge (read cycle)	2	14	2	14	ns
t11	WAIT# rising edge to valid Data	—	0	—	0	ns
t12	RD#, WR# pulse inactive time	Note 2	—	Note 2	—	ns
t13	WAIT# pulse active time	—	Note 3	—	Note 3	ns
t14	WAIT# rising edge to WR#, RD# rising edge	0	—	0	—	ns

1. Ts = System clock period
2. t12min = 2Ts (for a write cycle followed by a write cycle)
   = 1Ts + 1 (for a write cycle followed by a read cycle)
   = 2Ts (for a read cycle followed by a write cycle)
   = 1Ts + 1 (for a read cycle followed by a read cycle)
3. t13max = 2Ts (for a register write cycle)
   = 2Ts (for a register read cycle)
   = 2Ts (for a display memory write cycle)
   = 7Ts (for a display memory read cycle)

7.4.2 Generic Bus Direct Interface with WAIT# Timing

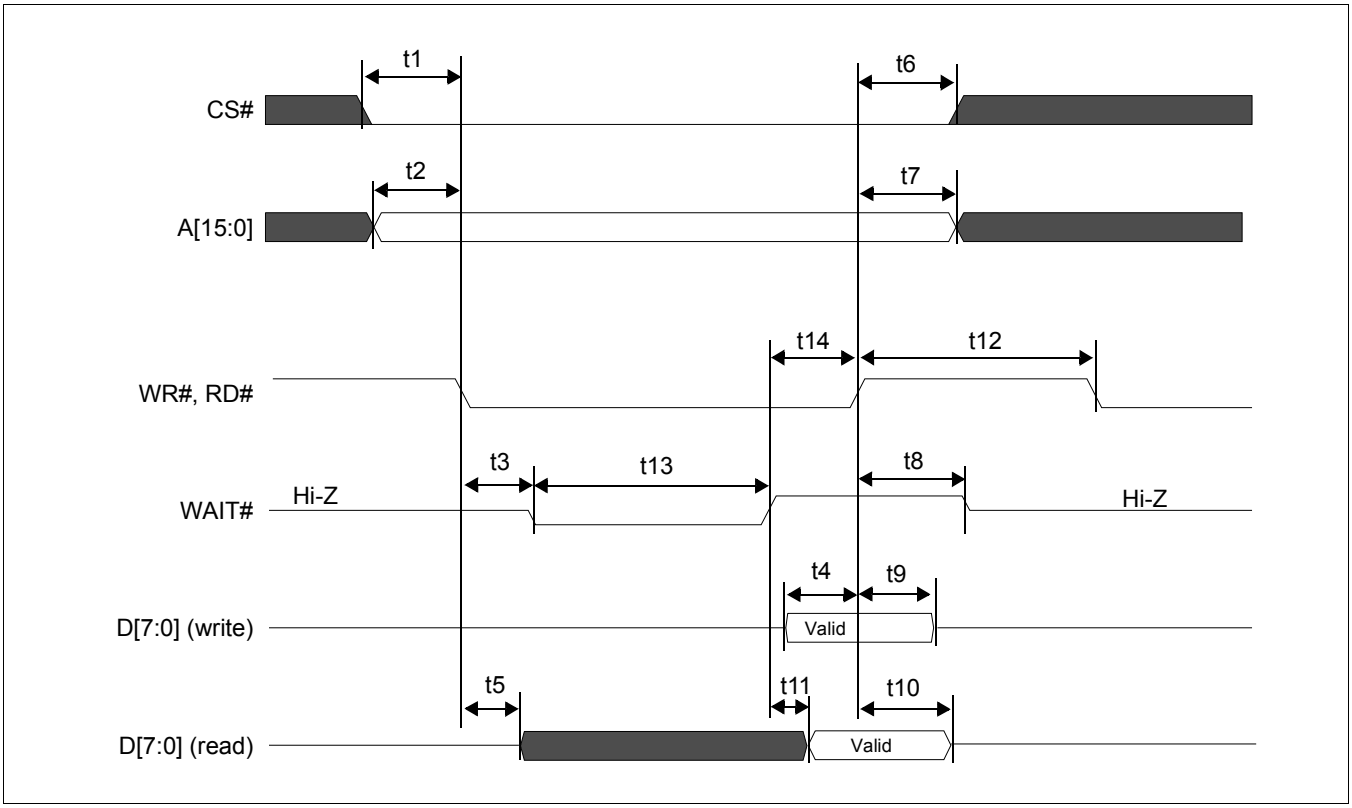


Figure 7-7 Generic Bus Direct Interface with WAIT# Timing

Table 7-6 Generic Bus Direct Interface with WAIT# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	WR#, RD# falling edge to WAIT# driven low	2	15	2	15	ns
t4	D[7:0] setup time to WR# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t5	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t6	CS# hold time	7	—	7	—	ns
t7	A[15:0] hold time	7	—	7	—	ns
t8	RD#, WR# rising edge to WAIT# high impedance	2	10	2	10	ns
t9	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t10	D[7:0] hold time from RD# rising edge (read cycle)	2	14	2	14	ns
t11	WAIT# rising edge to valid Data	—	0	—	0	ns
t12	RD#, WR# pulse inactive time	Note 2	—	Note 2	—	ns
t13	WAIT# pulse active time	—	Note 3	—	Note 3	ns
t14	WAIT# rising edge to WR#, RD# rising edge	0	—	0	—	ns

1. Ts = System clock period
2. t12min = 4Ts (for a write cycle followed by a write cycle)
   = 1Ts + 1 (for a write cycle followed by a read cycle)
   = 2Ts (for a read cycle followed by a write cycle)
   = 1Ts + 1 (for a read cycle followed by a read cycle)
3. t13max = 2Ts (for a register write cycle)
   = 2Ts (for a register read cycle)
   = 2Ts (for a display memory write cycle)
   = 7Ts (for a display memory read cycle)

7.4.3 Generic Bus Indirect Interface without WAIT# Timing

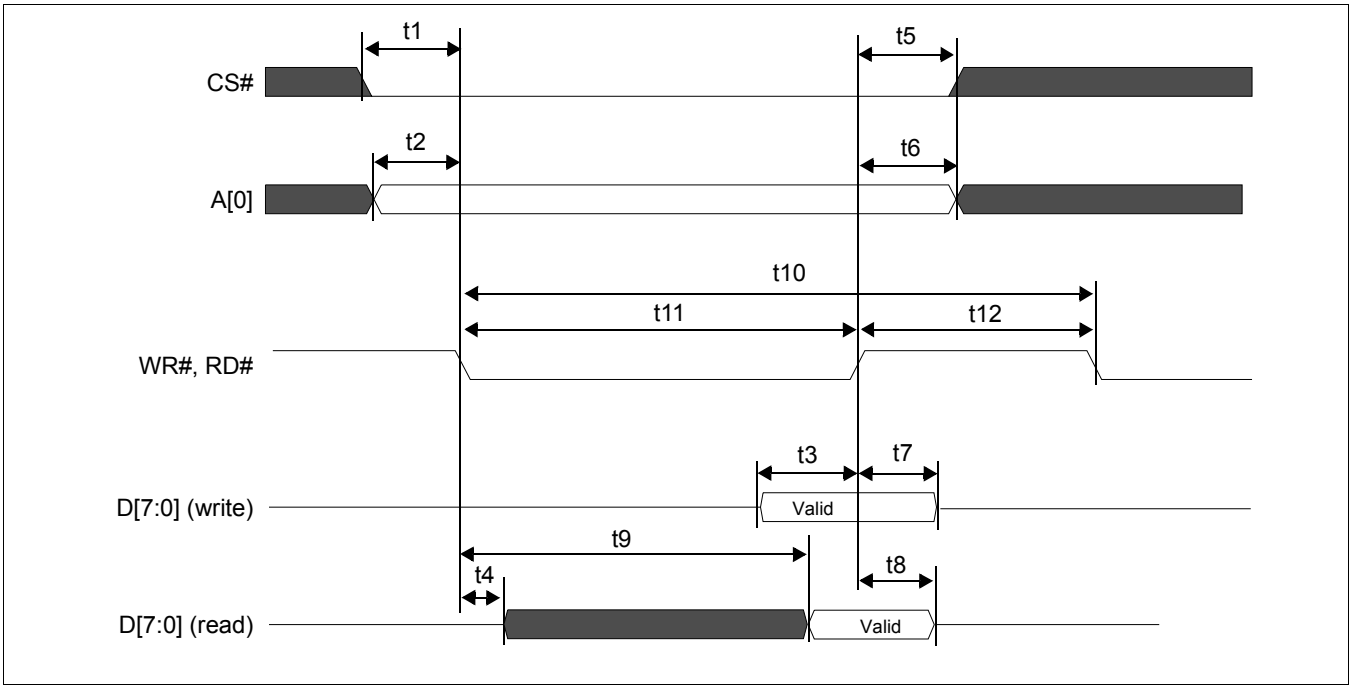


Figure 7-8 Generic Bus Indirect Interface without WAIT# Timing

Table 7-7 Generic Bus Indirect Interface without WAIT# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to WR# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	2	14	2	14	ns
t9	RD# falling edge to valid Data (read cycle)	—	Note 2	—	Note 2	ns
t10	RD#, WR# cycle time	Note 3	—	Note 3	—	ns
t11	RD#, WR# pulse active time	Note 4	—	Note 4	—	ns
t12	RD#, WR# pulse inactive time	Note 5	—	Note 5	—	ns

1. Ts = System clock period
2. t9max = 2Ts + 19 (for a register read cycle)
   = 6Ts + 19 (for a display memory read cycle)
3. t10min = 4Ts + 1 (for a register write cycle)
   = 4Ts + 1 (for a register read cycle)
   = 4Ts + 1 (for a display memory write cycle)
   = 7Ts + 11 (for a display memory read cycle)
4. t11min = 3Ts (for a register write cycle)
   = 3Ts (for a register read cycle)
   = 3Ts (for a display memory write cycle)
   = 6Ts + 10 (for a display memory read cycle)
5. t12min = 2Ts (for a write cycle followed by a write cycle)
   = 1Ts + 1 (for a write cycle followed by a read cycle)
   = 2Ts (for a read cycle followed by a write cycle)
   = 1Ts + 1 (for a read cycle followed by a read cycle)

7.4.4 Generic Bus Direct Interface without WAIT# Timing

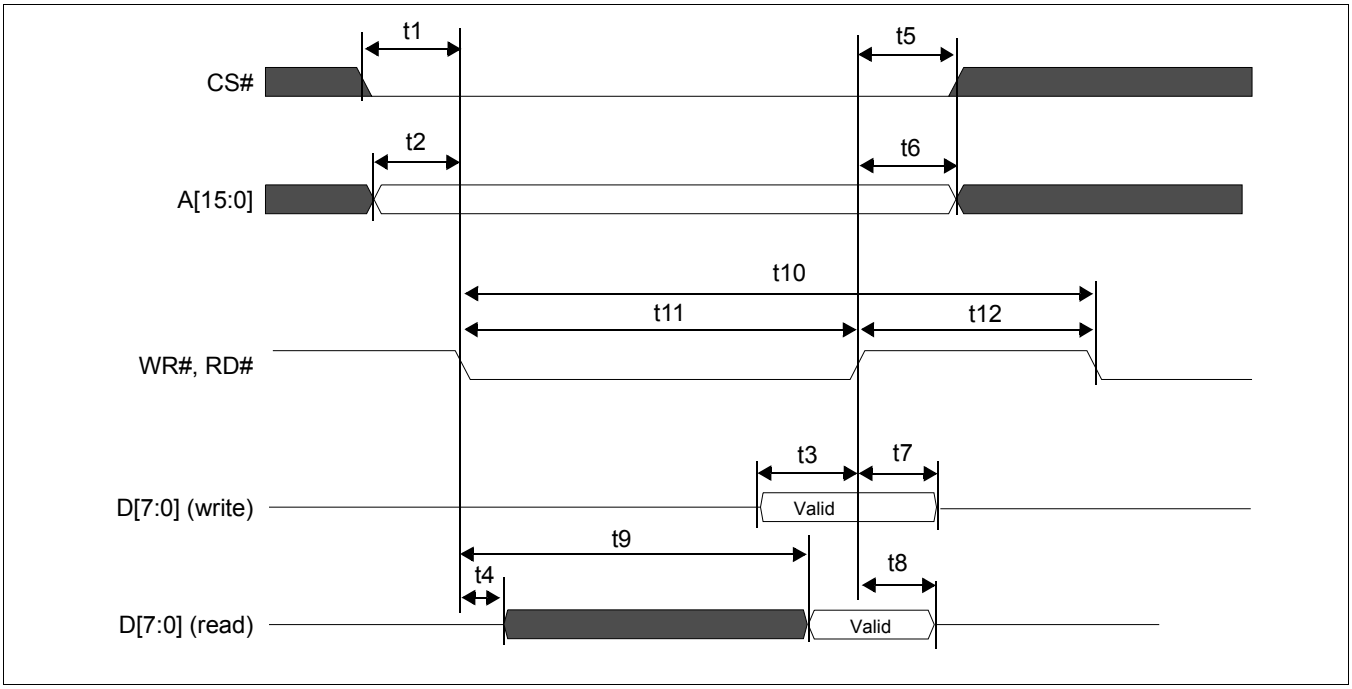


Figure 7-9 Generic Bus Direct Interface without WAIT# Timing

Table 7-8 Generic Bus Direct Interface without WAIT# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to WR# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from WR# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	2	14	2	14	ns
t9	RD# falling edge to valid Data (read cycle)	—	Note 2	—	Note 2	ns
t10	RD#, WR# cycle time	Note 3	—	Note 3	—	ns
t11	RD#, WR# pulse active time	Note 4	—	Note 4	—	ns
t12	RD#, WR# pulse inactive time	2Ts	—	2Ts	—	ns

1. Ts = System clock period
2. t9max = 2Ts + 19 (for a register read cycle)
   = 6Ts + 19 (for a display memory read cycle)
3. t10min = 5Ts (for a register write cycle)
   = 5Ts (for a register read cycle)
   = 5Ts (for a display memory write cycle)
   = 8Ts + 10 (for a display memory read cycle)
4. t11min = 3Ts (for a register write cycle)
   = 3Ts (for a register read cycle)
   = 3Ts (for a display memory write cycle)
   = 6Ts + 10 (for a display memory read cycle)

7.4.5 MC68K Family Bus Indirect Interface with DTACK# Timing

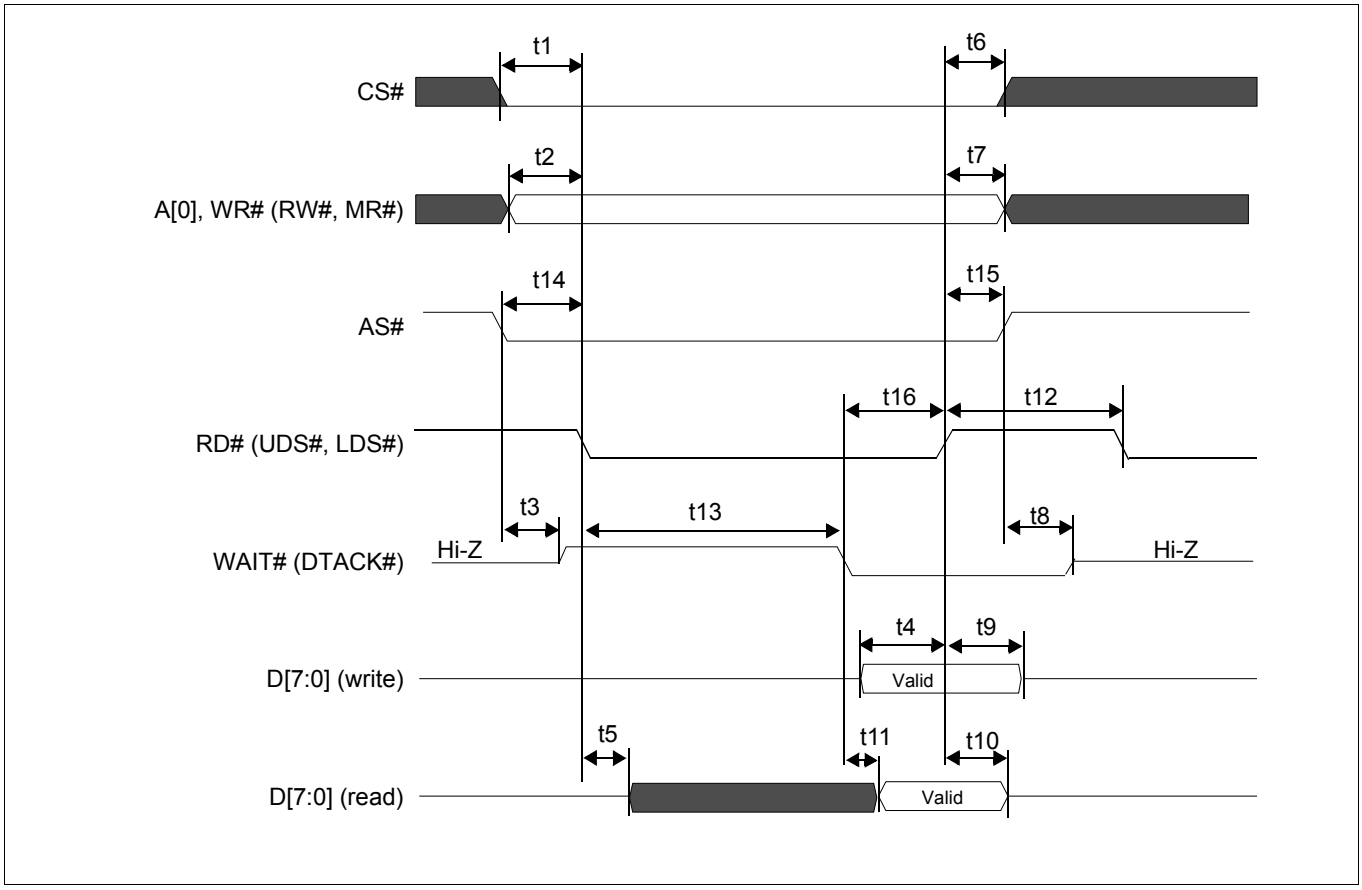


Figure 7-10 MC68K Family Bus Indirect Interface with DTACK# Timing

Table 7-9 MC68K Family Bus Indirect Interface with DTACK# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[0] setup time	5	—	5	—	ns
t3	AS# falling edge to DTACK# driven	2	15	2	15	ns
t4	D[7:0] setup time to RD# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t5	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t6	CS# hold time	7	—	7	—	ns
t7	A[0] hold time	7	—	7	—	ns
t8	AS# rising edge to DTACK# high impedance	2	10	2	10	ns
t9	D[7:0] hold time from RD# rising edge (write cycle)	5	—	5	—	ns
t10	D[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t11	DTACK# falling edge to valid Data	—	0	—	0	ns
t12	RD# pulse inactive time	Note 2	—	Note 2	—	ns
t13	DTACK# pulse inactive time from RD# falling edge	—	Note 3	—	Note 3	ns
t14	AS# setup time	0	—	0	—	ns
t15	AS# hold time	0	—	0	—	ns
t16	WAIT# falling edge to RD# rising edge	0	—	0	—	ns

1. Ts = System clock period
2. t12min = 2Ts (for a write cycle followed by a write cycle)
   = 1Ts + 1 (for a write cycle followed by a read cycle)
   = 2Ts (for a read cycle followed by a write cycle)
   = 1Ts + 1 (for a read cycle followed by a read cycle)
3. t13max = 2Ts (for a register write cycle)
   = 2Ts (for a register read cycle)
   = 2Ts (for a display memory write cycle)
   = 7Ts (for a display memory read cycle)

7.4.6 MC68K Family Bus Direct Interface with DTACK# Timing

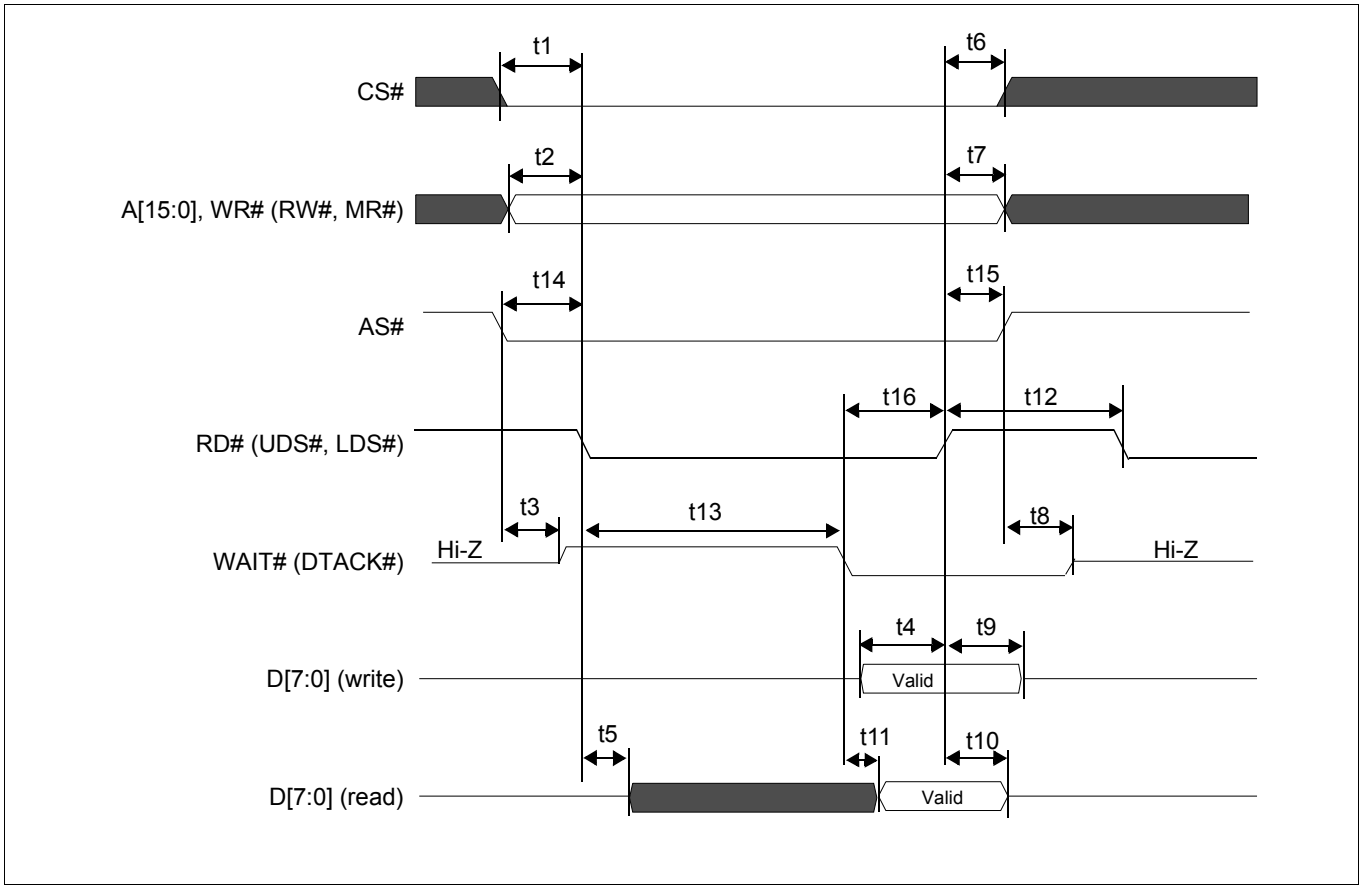


Figure 7-11 MC68K Family Bus Direct Interface with DTACK# Timing

Table 7-10 MC68K Family Bus Direct Interface with DTACK# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	AS# falling edge to DTACK# driven	2	15	2	15	ns
t4	D[7:0] setup time to RD# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t5	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t6	CS# hold time	7	—	7	—	ns
t7	A[15:0] hold time	7	—	7	—	ns
t8	AS# rising edge to DTACK# high impedance	2	10	2	10	ns
t9	D[7:0] hold time from RD# rising edge (write cycle)	5	—	5	—	ns
t10	D[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t11	DTACK# falling edge to valid Data	—	0	—	0	ns
t12	RD# pulse inactive time	Note 2	—	Note 2	—	ns
t13	DTACK# pulse inactive time from RD# falling edge	—	Note 3	—	Note 3	ns
t14	AS# setup time	0	—	0	—	ns
t15	AS# hold time	0	—	0	—	ns
t16	WAIT# falling edge to RD# rising edge	0	—	0	—	ns

1. Ts = System clock period
2. t12min = 4Ts (for a write cycle followed by a write cycle)
   = 1Ts + 1 (for a write cycle followed by a read cycle)
   = 2Ts (for a read cycle followed by a write cycle)
   = 1Ts + 1 (for a read cycle followed by a read cycle)
3. t13max = 2Ts (for a register write cycle)
   = 2Ts (for a register read cycle)
   = 2Ts (for a display memory write cycle)
   = 7Ts (for a display memory read cycle)

7.4.7 MC68K Family Bus Indirect Interface without DTACK# Timing

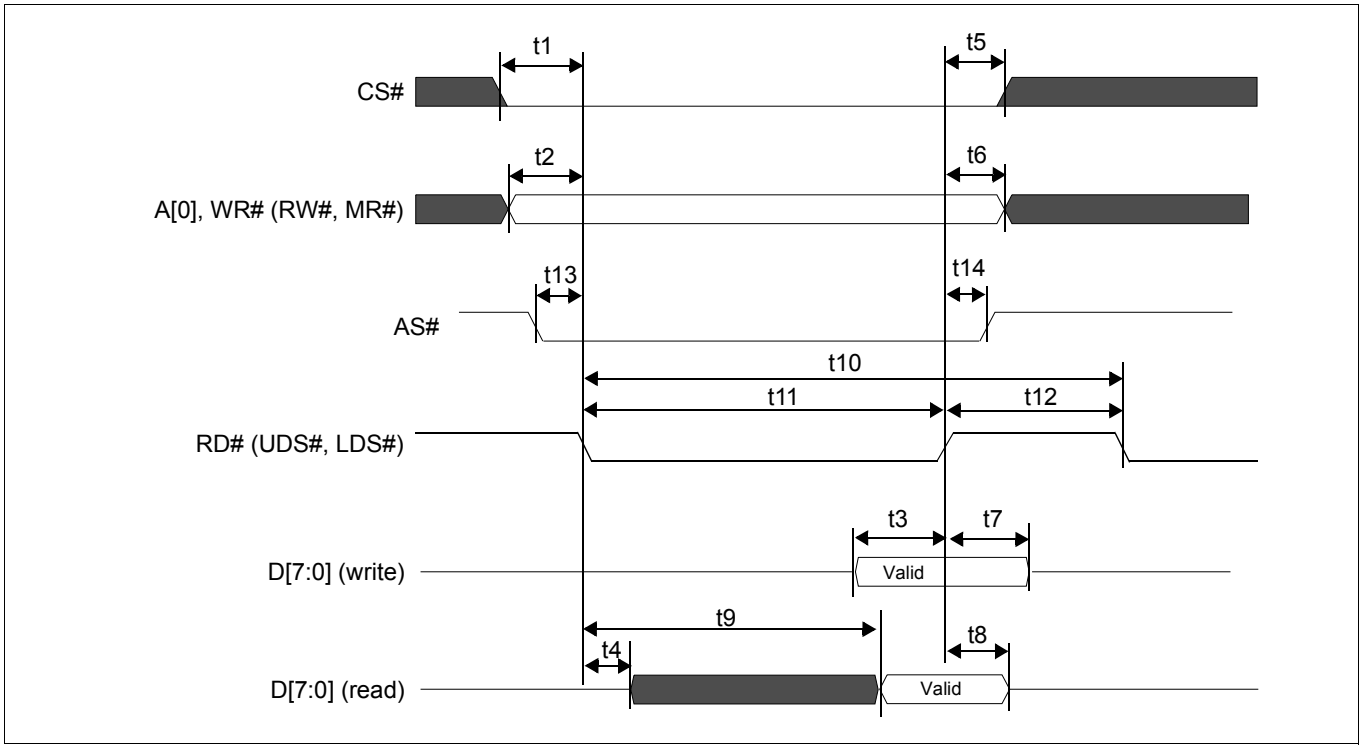


Figure 7-12 MC68K Family Bus Indirect Interface without DTACK# Timing

Table 7-11 MC68K Family Bus Indirect Interface without DTACK# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to RD# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from RD# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t9	RD# falling edge to valid Data	—	Note 2	—	Note 2	ns
t10	RD# cycle time	Note 3	—	Note 3	—	ns
t11	RD# pulse active time	Note 4	—	Note 4	—	ns
t12	RD# pulse inactive time	Note 5	—	Note 5	—	ns
t13	AS# setup time	0	—	0	—	ns
t14	AS# hold time	0	—	0	—	ns

1. Ts = System clock period
2. t9max = 2Ts + 19 (for a register read cycle)
   = 6Ts + 19 (for a display memory read cycle)
3. t10min = 4Ts + 1 (for a register write cycle)
   = 4Ts + 1 (for a register read cycle)
   = 4Ts + 1 (for a display memory write cycle)
   = 7Ts + 11 (for a display memory read cycle)
4. t11min = 3Ts (for a register write cycle)
   = 3Ts (for a register read cycle)
   = 3Ts (for a display memory write cycle)
   = 6Ts + 10 (for a display memory read cycle)
5. t12min = 2Ts (for a write cycle followed by a write cycle)
   = 1Ts + 1 (for a write cycle followed by a read cycle)
   = 2Ts (for a read cycle followed by a write cycle)
   = 1Ts + 1 (for a read cycle followed by a read cycle)

7.4.8 MC68K Family Bus Direct Interface without DTACK# Timing

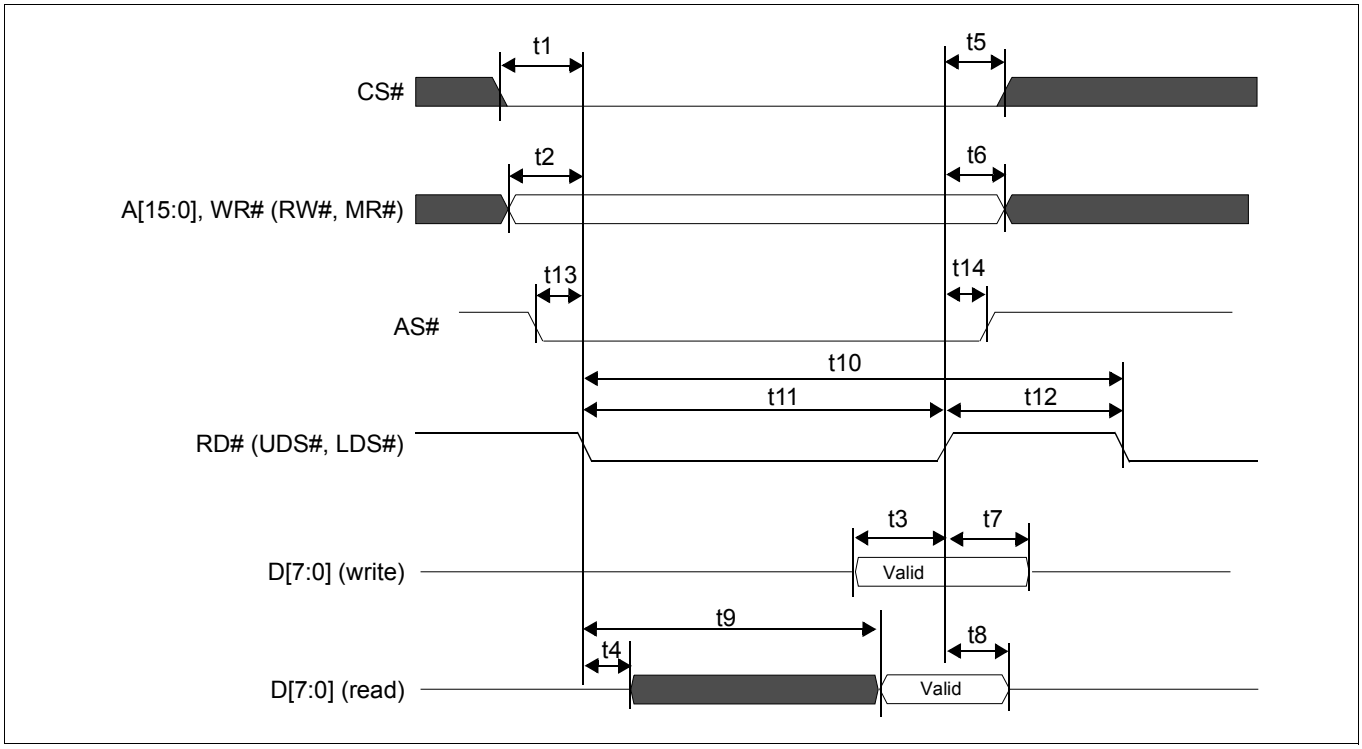


Figure 7-13 MC68K Family Bus Direct Interface without DTACK# Timing

Table 7-12 MC68K Family Bus Direct Interface without DTACK# Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[15:0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to RD# rising edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t4	RD# falling edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[15:0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from RD# rising edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# rising edge (read cycle)	2	55	2	55	ns
t9	RD# falling edge to valid Data	—	Note 2	—	Note 2	ns
t10	RD# cycle time	Note 3	—	Note 3	—	ns
t11	RD# pulse active time	Note 4	—	Note 4	—	ns
t12	RD# pulse inactive time	2Ts	—	2Ts	—	ns
t13	AS# setup time	0	—	0	—	ns
t14	AS# hold time	0	—	0	—	ns

1. Ts = System clock period
2. t9max = 2Ts + 19 (for a register read cycle)
   = 6Ts + 19 (for a display memory read cycle)
3. t10min = 5Ts (for a register write cycle)
   = 5Ts (for a register read cycle)
   = 5Ts (for a display memory write cycle)
   = 8Ts + 10 (for a display memory read cycle)
4. t11min = 3Ts (for a register write cycle)
   = 3Ts (for a register read cycle)
   = 3Ts (for a display memory write cycle)
   = 6Ts + 10 (for a display memory read cycle)

7.4.9 M6800 Family Bus Indirect Interface Timing

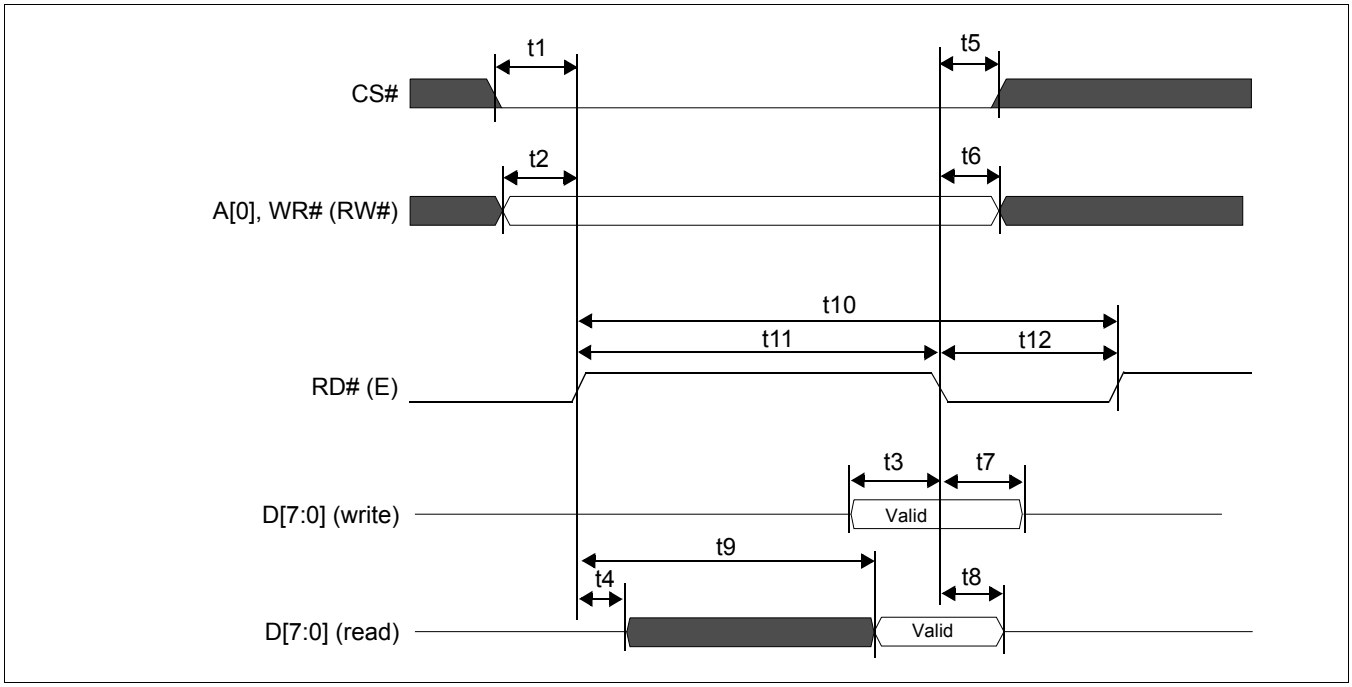


Figure 7-14 M6800 Family Bus Indirect Interface Timing

Table 7-13 M6800 Family Bus Indirect Interface Timing

Symbol	Parameter	3.3 Volt		5.0 Volt		Units
		Min	Max	Min	Max	
t1	CS# setup time	5	—	5	—	ns
t2	A[0] setup time	5	—	5	—	ns
t3	D[7:0] setup time to RD# falling edge (write cycle)	1Ts (Note1)	—	1Ts (Note1)	—	ns
t4	RD# rising edge to D[7:0] driven (read cycle)	3	—	3	—	ns
t5	CS# hold time	7	—	7	—	ns
t6	A[0] hold time	7	—	7	—	ns
t7	D[7:0] hold time from RD# falling edge (write cycle)	5	—	5	—	ns
t8	D[7:0] hold time from RD# falling edge (read cycle)	2	55	2	55	ns
t9	RD# rising edge to valid Data	—	Note 2	—	Note 2	ns
t10	RD# cycle time	Note 3	—	Note 3	—	ns
t11	RD# pulse active time	Note 4	—	Note 4	—	ns
t12	RD# pulse inactive time	Note 5	—	Note 5	—	ns

1. Ts = System clock period
2. t9max = 2Ts + 19 (for a register read cycle)
   = 6Ts + 19 (for a display memory read cycle)
3. t10min = 4Ts + 1 (for a register write cycle)
   = 4Ts + 1 (for a register read cycle)
   = 4Ts + 1 (for a display memory write cycle)
   = 7Ts + 11 (for a display memory read cycle)
4. t11min = 3Ts (for a register write cycle)
   = 3Ts (for a register read cycle)
   = 3Ts (for a display memory write cycle)
   = 6Ts + 10 (for a display memory read cycle)
5. t12min = 2Ts (for a write cycle followed by a write cycle)
   = 1Ts + 1 (for a write cycle followed by a read cycle)
   = 2Ts (for a read cycle followed by a write cycle)
   = 1Ts + 1 (for a read cycle followed by a read cycle)

7.5 Power Save Mode/Display Enable Timing

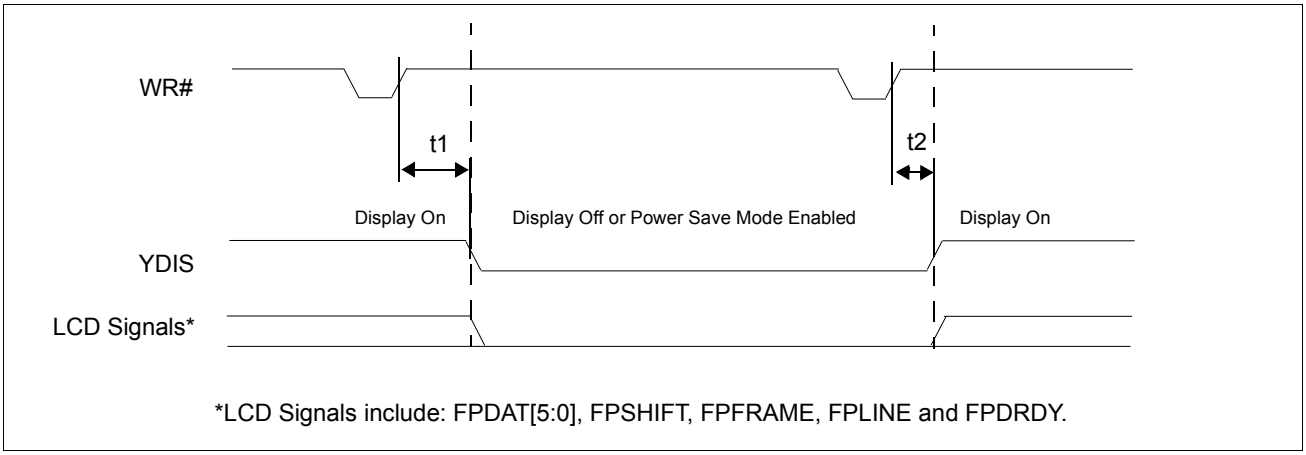


Figure 7-15 Power Save Mode/Display Enable Timing

Note

When using an external crystal with the internal oscillator, a delay is required after exiting power save mode for system stabilization. For further information, refer to Section 7.3, "Reset Timing" on page 34.

Table 7-14 Power Save Mode/Display Enable Timing

Symbol	Parameter	3.0 Volt		5.0 Volt		Units
		Min.	Max.	Min.	Max.	
t1a	YDIS falling edge delay for Power Save Mode Enable in Indirect Mode (see Note 2)	—	2	—	2	Frames
t1b	YDIS falling edge delay for Display Off in Indirect Mode (58h)	—	2Ts + 10	—	2Ts + 10	ns
t1c	YDIS falling edge delay for Display Off in Direct Mode (see Note 3)	—	2Ts + 10	—	2Ts + 10	ns
t2	YDIS rising edge delay for Display On (see Note 3)	—	2Ts + 10	—	2Ts + 10	ns

1. Ts = System Clock Period
2. Power Save Mode is controlled by the Power Save Mode Enable bit, REG[08h] bit 0.
3. Display On/Off is controlled by the Display Enable bit, REG[09h] bit 0.

7.6 Display Interface

7.6.1 STN-LCD Interface Timing

The timing parameters required to drive a STN-LCD flatpanel display are shown below.

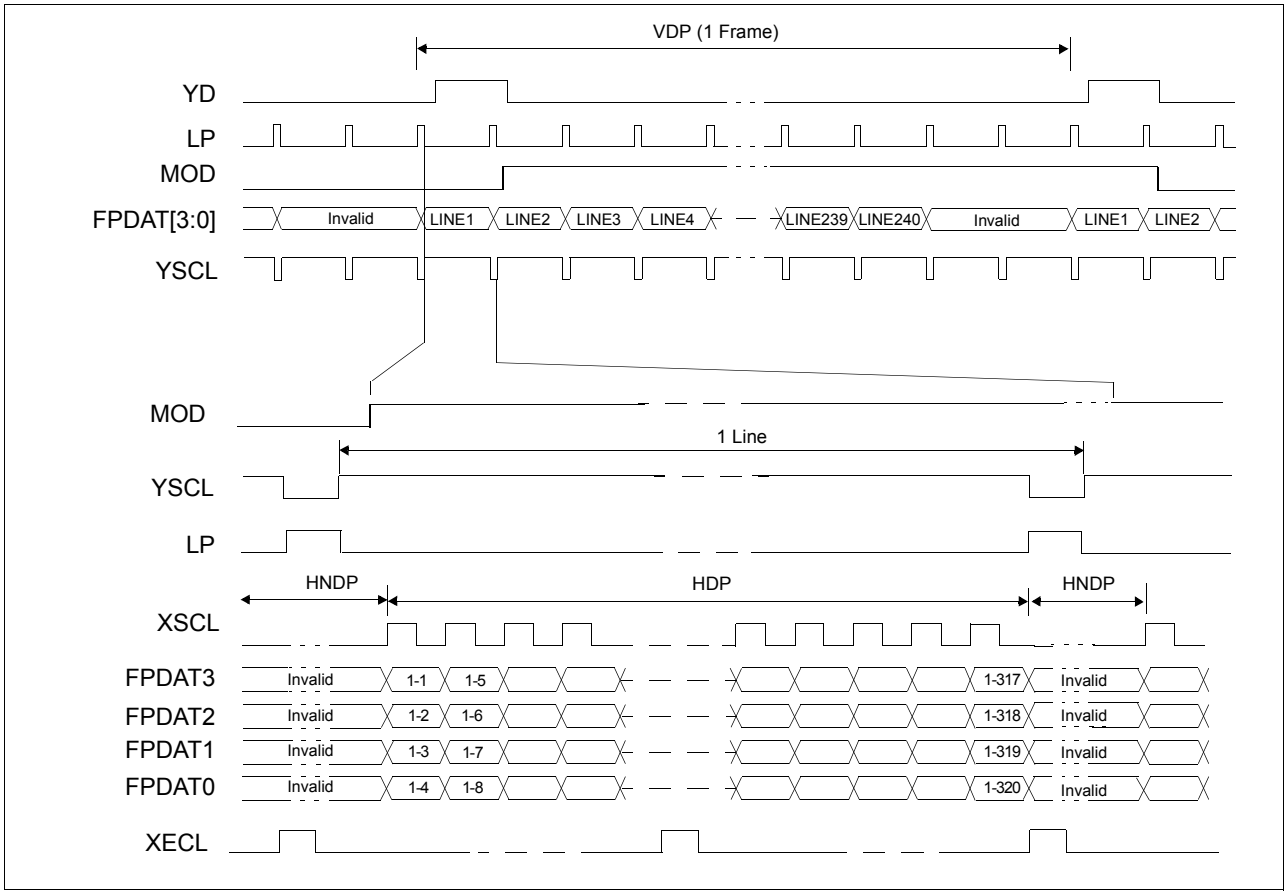


Figure 7-16: Monochrome 4-Bit STN Panel Timing

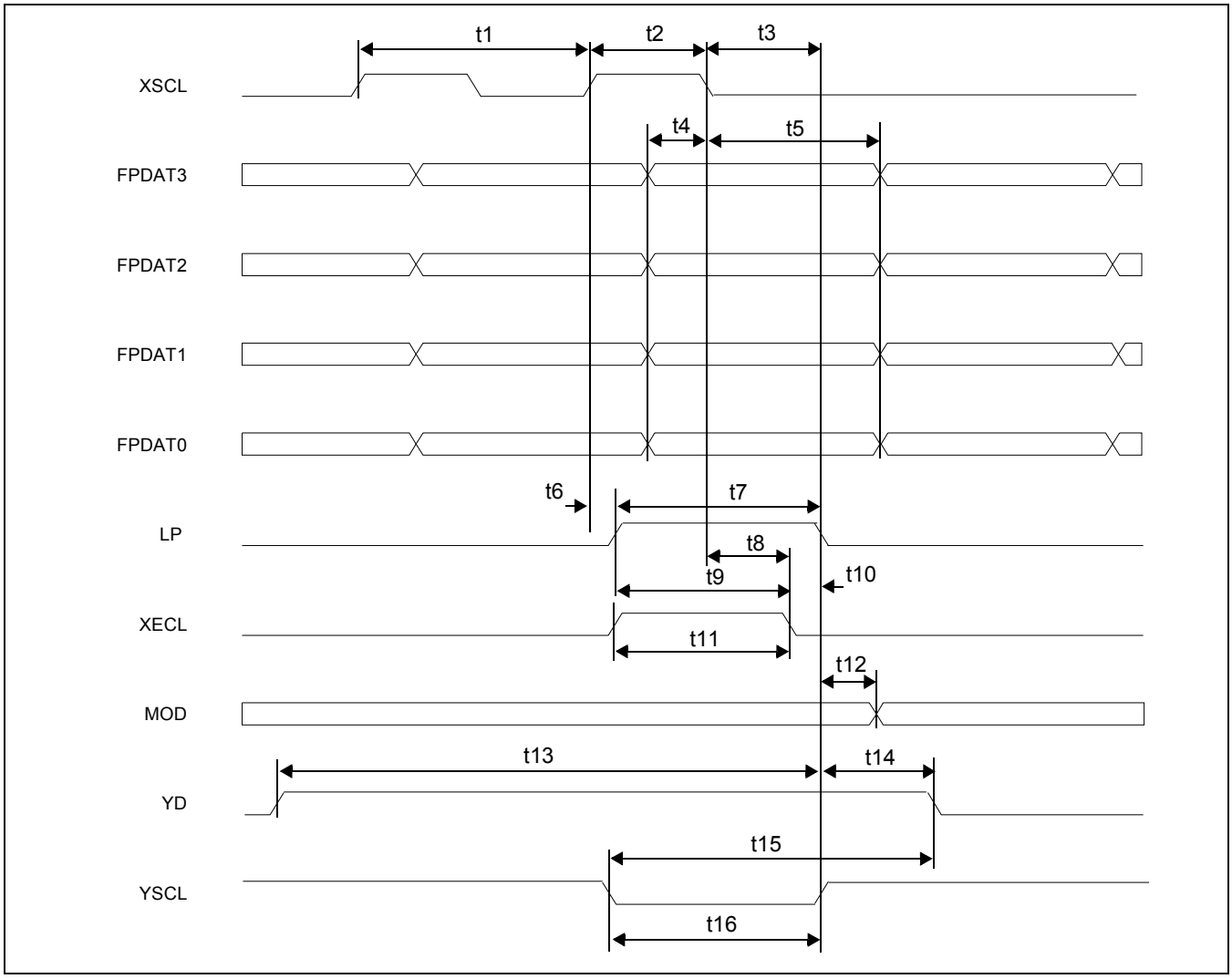

t1
t2
t3
XSCL
t4
t5
FPDAT3
FPDAT2
FPDAT1
FPDAT0
t6
t7
LP
t8
t9
t10
XECL
t11
t12
MOD
t13
t14
YD
t15
YSCL
t16

Table 7-15: Single Monochrome 4-Bit Panel A.C. Timing

Symbol	Parameter	3.3 Volts		5.0 Volts		Units
		Min	Max	Min	Max	
t1	XSCL cycle time	1	—	1	—	Tc (Note 1)
t2	XSCL pulse width	0.5Tc - 5	—	0.5Tc - 4	—	ns
t3	Latch data setup time from XSCL falling edge	0.5Tc - 5	—	0.5Tc - 4	—	ns
t4	FPDAT[3:0] setup to XSCL falling edge	0.5Tc - 5	—	0.5Tc - 4	—	ns
t5	FPDAT[3:0] hold from XSCL falling edge	0.5Tc - 5	—	0.5Tc - 4	—	ns
t6	LP rising edge delay from XSCL rising edge	0	4	0	4	ns
t7	Latch pulse width	Tc - 5	—	Tc - 4	—	ns
t8	XECL falling edge setup time to XSCL falling edge	0.25Tc -5	—	0.25Tc - 4	—	ns
t9	XECL falling edge setup time from LP rising edge	0.75Tc - 5	—	0.75Tc - 4	—	ns
t10	XECL falling edge hold time to LP falling edge	Note 2	—	Note 2	—	ns
t11	XECL pulse width	0.75Tc - 5	—	0.75Tc - 4	—	ns
t12	Permitted MOD delay time	—	4	—	4	ns
t13	LP falling edge from YDYD rising edge	2Tc - 10	—	2Tc - 10	—	ns
t14	LP falling edge to YD falling edge	2Tc	—	2Tc	—	ns
t15	YD falling edge hold time from YSCL falling edge	3Tc - 10	—	3Tc - 10	—	ns
t16	YSCL pulse width	Tc - 5	—	Tc - 4	—	ns

1. Tc = XSCL cycle time
   = 4Ts when CNF[1:0] = 00
   = 8Ts when CNF[1:0] = 01
   = 16Ts when CNF[1:0] = 10
2. t10min = 0.25Tc - 8

7.6.2 TFT-LCD Interface Timing

The timing parameters required to drive a TFT-LCD flat panel display are shown below.

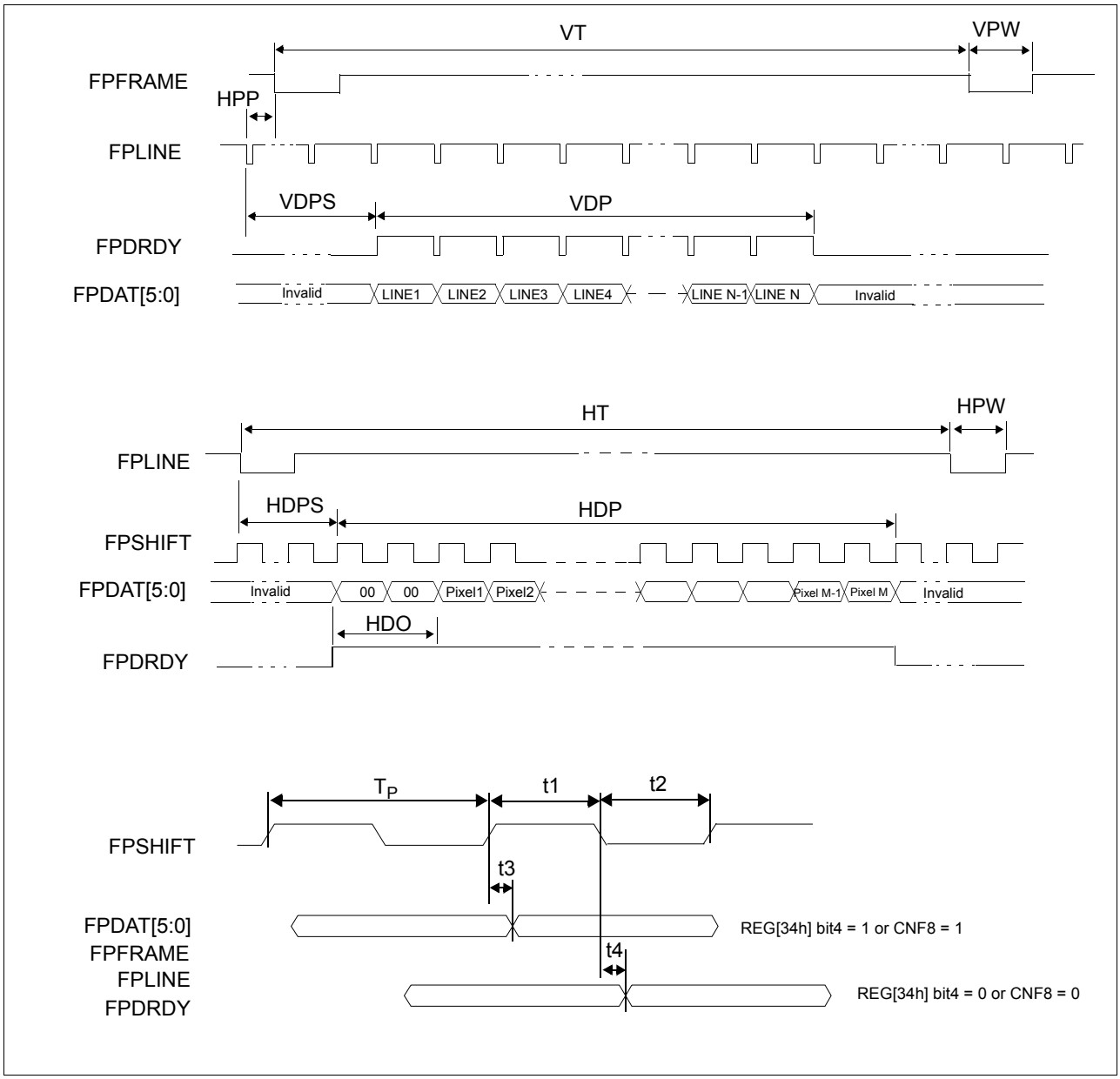


Figure 7-17: TFT-LCD Interface Timing

Table 7-16: TFT-LCD interface Timing 1

Symbol	Parameter	3.3 Volts		5.0 Volts		Units
		Min	Max	Min	Max	
T_P	FPSHIFT clock period	28.5	500	28.5	500	ns
f_P	FPSHIFT frequency	$1/T_P$ (Note)				Hz
t1	FPSHIFT pulse width high (REG[73h] bit 6 = 0 or CNF9 = 0)	Tp x 0.39	Tp x 0.50	Tp x 0.45	Tp x 0.55	ns
	FPSHIFT pulse width high (REG[73h] bit 6 = 1or CNF9 = 1)	Tp x 0.39	Tp x 0.50	Tp x 0.45	Tp x 0.55	ns
t2	FPSHIFT pulse width low (REG[73h] bit 6 = 0 or CNF9 = 0)	Tp x 0.50	Tp x 0.61	Tp x 0.45	Tp x 0.55	ns
	FPSHIFT pulse width low (REG[73h] bit 6 = 1or CNF9 = 1)	Tp x 0.50	Tp x 0.61	Tp x 0.45	Tp x 0.55	ns
t3	FPSHIFT rising edge to FPDAT[5:0],FPFRAME,FPLINE and FPDRDY delay time (REG[73h] = 00h or CNF9 = 0)	-4	1	-2	2	ns
	FPSHIFT rising edge to FPDAT[5:0],FPFRAME,FPLINE and FPDRDY delay time (REG[73h] = FFh or CNF9 = 1)	-4	1	-2	2	ns
t4	FPSHIFT falling edge to FPDAT[5:0],FPFRAME,FPLINE and FPDRDY delay time (REG[73h] = 00h or CNF9 = 0)	-2	3	-2	2	ns
	FPSHIFT falling edge to FPDAT[5:0],FPFRAME,FPLINE and FPDRDY delay time (REG[73h] = FFh or CNF9 = 1)	-2	3	-2	2	ns

Note

$f_{SYSCLK} \leq 7 \times f_P$

where: f_{SYSCLK} is CLKI or Crystal Oscillator clock frequency.

Table 7-17: TFT-LCD interface Timing 2

Symbol	Description	Derived From	Min	Max	Units
HT	Horizontal Total	{REG[36h]bits2-0,REG[35h]bits7-0}+1	(Note 2,3)	2048	Tp (Note1)
HDP	Horizontal Display Period	{REG[38h]bits2-0,REG[37h]bits7-0}+1	64	1280	Tp
HDPS	Horizontal Display Period Start Position	{REG[3Ah]bits2-0,REG[39h]bits7-0}	16	1280	Tp
HPW	HSYNC Pulse Width	(REG[42h] bits 7-0) + 1	1	256	Tp
HPP	HSYNC Pulse Position	{REG[44h]bits2-0,REG[43h]bits7-0}	0	1279	Tp
HDO	Horizontal Display Offset	{REG[4Ah]bits2-0,REG[49h]bits7-0}	0	HDP/2	Tp
VT	Vertical Total	{REG[3Ch]bits2-0,REG[3Bh]bits7-0}+1	(Note 4)	2048	Lines
VDP	Vertical Display Period	{REG[3Eh]bits2-0,REG[3Dh]bits7-0}+1	64	1280	Lines
VDPS	Vertical Display Period Start Position	{REG[40h]bits2-0,REG[3Fh]bits7-0}	1	1280	Lines
VPW	VSYNC Pulse Width	(REG[41h] bits 7-0) + 1	1	256	Lines

Note

1. Tp = FPSHIFT Clock Period
2. [HT] ≥ [HDP] + [HDPS] + 1
3. [HT] ≥ 8 x ([TCR] + 4) x [LF] x $T_{SYSCLK} \div T_P \div$ [VDP]
4. [VT] ≥ [VDP] + [VDPS] + {16 x ([TCR] +4) x $T_{SYSCLK} \div T_P \div$ [HT]}

Where:

T_{SYSCLK} = CLKI or Crystal Oscillator clock period

[TCR] = Total Character Bytes Per Row (REG[04h] - 1)

[LF] = Frame Height (REG[05h] + 1)

8 Memory Mapping

The S1D13709 includes 32K bytes of embedded SRAM. The memory is used for the display data, the registers and the CGROM. Display Memory area are not accessible at sleep mode. For further information, see Section 17, “Power Save Mode” on page 186.

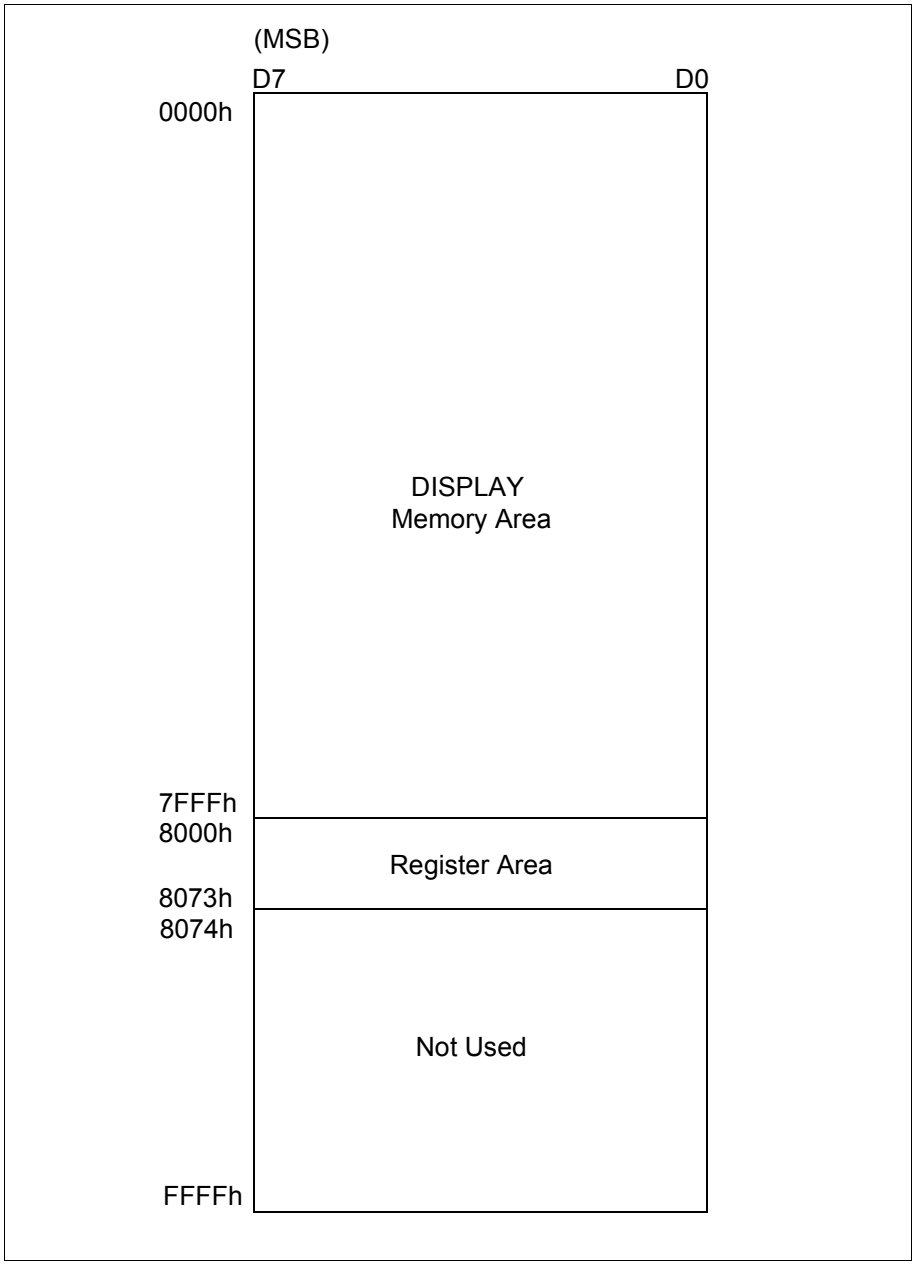


Figure 8-1 S1D13709 Memory Mapping

9 Clocks

9.1 Clock Diagram

The following figure shows the clock tree of the S1D13709.

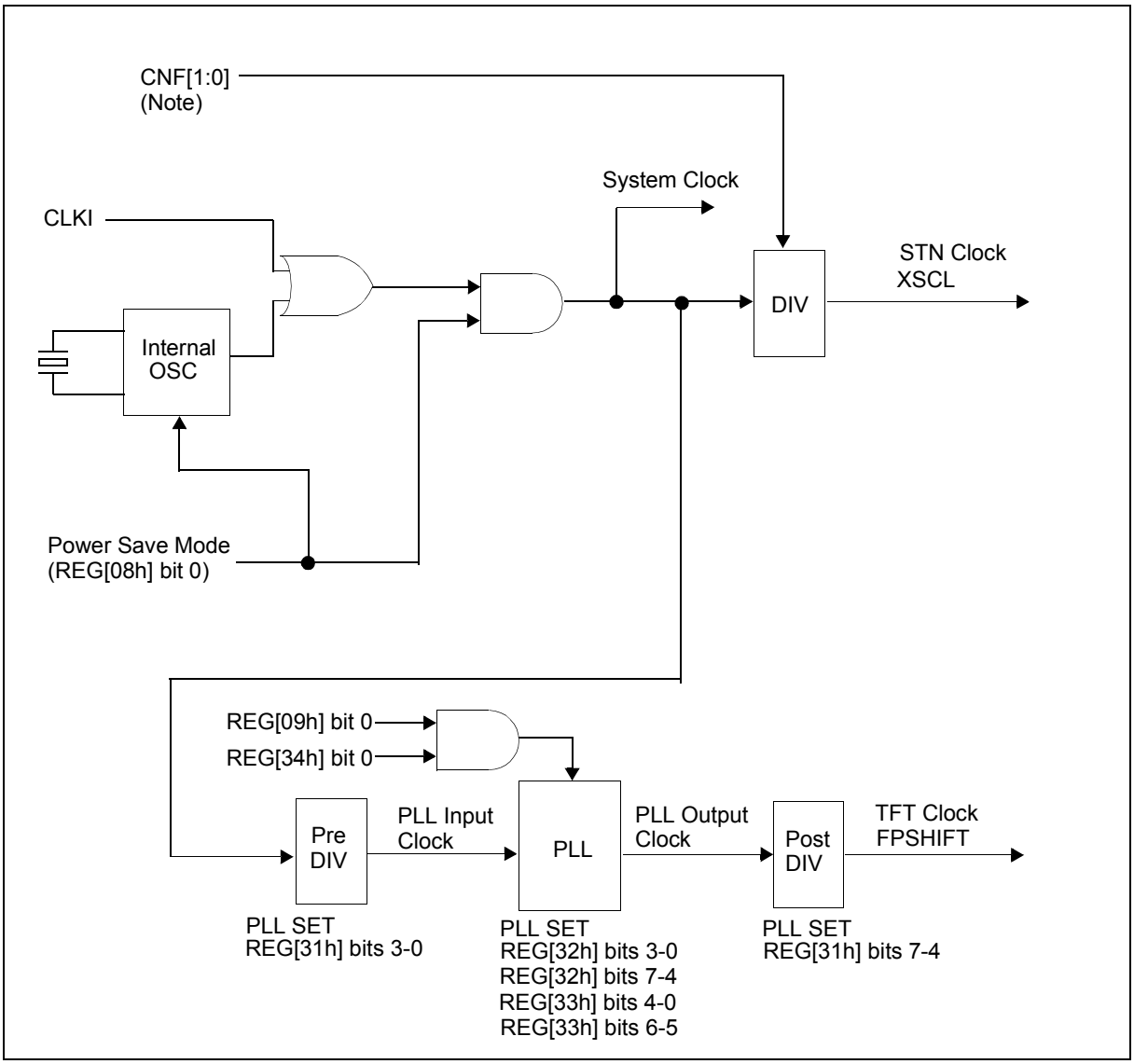


Figure 9-1: Clock Diagram

Note

The XSCL Cycle Time is configured using the CNF[1:0] pins. For further information, see Section 5.3, “Summary of Configuration Options” on page 25.

9.2 Clock Descriptions

9.2.1 System Clock

The maximum frequency of the system clock is 66MHz. The system clock source can be either an external clock source (i.e. oscillator) or the internal oscillator (with external crystal). If an external clock source is used, the crystal input (XCG1) must be pulled down and the crystal output (XCD1) must be left unconnected. If the internal oscillator (with external crystal) is used, the CLKI pin must be pulled down.

9.2.2 STN Clock

The STN clock, XSCL is derived from the internal system clock as shown in Figure 9-1: "Clock Diagram," on page 60. The maximum frequency possible for XSCL clock is 15MHz.

As XSCL is generated to synchronize with XECL, the total output of the XSCL clock for one line is a multiple of 16.

9.2.3 TFT Clock

The TFT clock, FPSHIFT is derived from the internal system clock and PLL as shown in Figure 9-1: "Clock Diagram," on page 60. The maximum frequency possible for FPSHIFT clock is 35MHz.

9.3 Oscillator Circuit

The S1D13709 design incorporates an oscillator circuit. A stable oscillator can be constructed by connecting an AT-cut crystal, two capacitors, and two resistors to XCG1 and XCD1, as shown in the figure below. If the oscillator frequency is increased, Cd and Cg should be decreased proportionally.

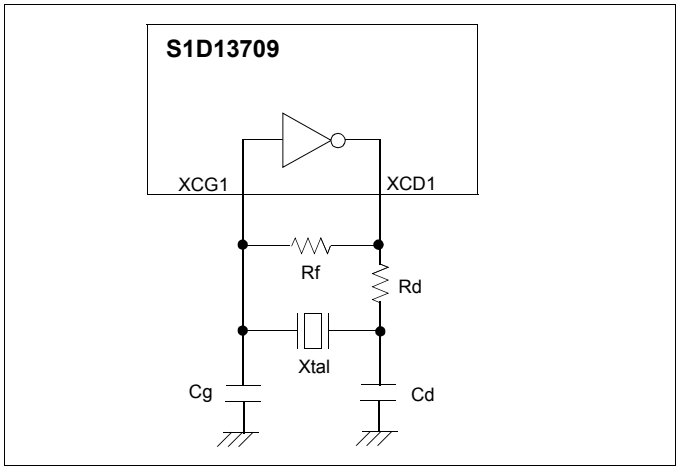


Figure 9-2 Crystal Oscillator

Table 9-1 Crystal Oscillator Circuit Frequency Range

Symbol	Min	Typ	Max	Units
f_{OSC}	18 (Note 1,2)	24	40	MHz

Note

1. When the TFT interface is used (REG[34h] bit 0 =1), Minimum OSC frequency depends on the TFT clock frequency. For further details on internal clocks, see Section Table 7-16:, "TFT-LCD interface Timing 1" on page 58.
2. When the TFT interface is used (REG[34h] bit 0 =1) and 4bpp is selected (REG[20h] bits 1-0 = 10), OSC frequency must be equal or greater than 24MHz.

The oscillation characteristics depend on the components used in the circuit (Xtal, Rf, Rd, Cg, Cd, condition of board). An example circuit and example component values are shown below.

Table 9-2 Example of Crystal Oscillator Circuit Parameters

Frequency	Rf	Rd	Cg	Cd	Crystal
20MHz	10MΩ	0Ω	10pF	10pF	EPSON FA-238 20MHz CL=9pF
24MHz	10MΩ	0Ω	10pF	10pF	EPSON FA-238 24MHz CL=9pF

Note

1. For optimum results, the component values used in this circuit should be evaluated for each specific application.
2. The circuit board lines to XCG1 and XCD1 must be as short as possible to prevent wiring capacitance from changing the oscillator frequency or increasing the power consumption.

10 Registers

10.1 Register Set

The S1D13709 registers are listed in the following table.

Table 10-1: S1D13709 Register Set

Register	Pg	Register	Pg
LCD Register Descriptions (Offset = 8000h)			
System Control Registers			
REG[00h] Memory Configuration Register	65	REG[01h] Horizontal Character Size Register	69
REG[02h] Vertical Character Size Register	70	REG[03h] Character Bytes Per Row Register	70
REG[04h] Total Character Bytes Per Row Register	71	REG[05h] Frame Height Register	71
REG[06h] Horizontal Address Range Register 0	72	REG[07h] Horizontal Address Range Register 1	72
REG[08h] Power Save Mode Register	73		
Display Control Registers			
REG[09h] Display Enable Register	74	REG[0Ah] Display Attribute Register	74
REG[0Bh] Screen Block 1 Start Address Register 0	76	REG[0Ch] Screen Block 1 Start Address Register 1	76
REG[0Dh] Screen Block 1 Size Register	76	REG[0Eh] Screen Block 2 Start Address Register 0	77
REG[0Fh] Screen Block 2 Start Address Register 1	77	REG[10h] Screen Block 2 Size Register	77
REG[11h] Screen Block 3 Start Address Register 0	78	REG[12h] Screen Block 3 Start Address Register 1	78
REG[13h] Screen Block 4 Start Address Register 0	78	REG[14h] Screen Block 4 Start Address Register 1	78
REG[15h] Cursor Width Register	82	REG[16h] Cursor Height Register	82
REG[17h] Cursor Shift Direction Register	83	REG[18h] Overlay Register	84
REG[19h] Character Generator RAM Start Address Register 0	86	REG[1Ah] Character Generator RAM Start Address Register 1	86
REG[1Bh] Horizontal Pixel Scroll Register	87		
Drawing Control Registers			
REG[1Ch] Cursor Write Register 0	89	REG[1Dh] Cursor Write Register 1	89
REG[1Eh] Cursor Read Register 0	90	REG[1Fh] Cursor Read Register 1	90
GrayScale Register			
REG[20h] Bit-Per-Pixel Select Register	91		
Production Register			
REG[30h] Production Code Register	92		
TFT Interface Registers			
REG[31h] TFT PLL Setting Register 0	92	REG[32h] TFT PLL Setting Register 1	93
REG[33h] TFT PLL Setting Register 2	94	REG[34h] TFT Interface Configuration Register	96
REG[35h] TFT Horizontal Total Period Register 0	98	REG[36h] TFT Horizontal Total Period Register 1	98
REG[37h] TFT Horizontal Display Period Register 0	99	REG[38h] TFT Horizontal Display Period Register 1	99
REG[39h] TFT Horizontal Display Period Start Position Register 0	99	REG[3Ah] TFT Horizontal Display Period Start Position Register 1	99
REG[3Bh] TFT Vertical Total Period Register 0	100	REG[3Ch] TFT Vertical Total Period Register 1	100
REG[3Dh] TFT Vertical Display Period Register 0	100	REG[3Eh] TFT Vertical Display Period Register 1	100
REG[3Fh] TFT Vertical Display Period Start Position Register 0	100	REG[40h] TFT Vertical Display Period Start Position Register 1	100
REG[41h] TFT FPFRAME Pulse Width Register	101	REG[42h] TFT FPLINE Pulse Width Register	101

Table 10-1: S1D13709 Register Set

Register	Pg	Register	Pg
REG[43h] TFT FPLINE Pulse Position Register 0	101	REG[44h] TFT FPLINE Pulse Position Register 1	101
REG[45h] TFT Horizontal Scale Ratio Register 0	102	REG[46h] TFT Horizontal Scale Ratio Register 1	102
REG[47h] TFT Vertical Scale Ratio Register 0	102	REG[48h] TFT Vertical Scale Ratio Register 1	102
REG[49h] TFT Horizontal Display Offset Register 0	103	REG[4Ah] TFT Horizontal Display Offset Register 1	103
REG[4Bh] Horizontal Pixel Scroll Frame Sync Enable Register	103		
REG[63h] TFT Color Palette 0 Register	104	REG[64h] TFT Color Palette 1 Register	104
REG[65h] TFT Color Palette 2 Register	104	REG[66h] TFT Color Palette 3 Register	105
REG[67h] TFT Color Palette 4 Register	105	REG[68h] TFT Color Palette 5 Register	105
REG[69h] TFT Color Palette 6 Register	105	REG[6Ah] TFT Color Palette 7 Register	105
REG[6Bh] TFT Color Palette 8 Register	106	REG[6Ch] TFT Color Palette 9 Register	106
REG[6Dh] TFT Color Palette 10 Register	106	REG[6Eh] TFT Color Palette 11 Register	106
REG[6Fh] TFT Color Palette 12 Register	106	REG[70h] TFT Color Palette 13 Register	107
REG[71h] TFT Color Palette 14 Register	107	REG[72h] TFT Color Palette 15 Register	107
REG[73h] LCD Pin Output Drive Control Register	107		

10.2 Register Restrictions

All reserved bits must be set to 0 unless otherwise specified. Writing a value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect.

10.3 Register Descriptions

10.3.1 System Control Registers

The following registers initialize the S1D13709, set the window sizes, and select the LCD interface format. Incorrect configuration of these registers may cause other commands to operated incorrectly. For an example initialization of the S1D13709, see Section 15.1.3, “Initialization Example for STN Interface” on page 151.

SYSTEM SET

The SYSTEM SET command is used to configure the S1D13709 for the display used and to exit power save mode **when indirect addressing is used**. The values from REG[00h] through REG[07h] are passed as parameters when the SYSTEM SET command is issued. For further information on the SYSTEM SET command, see Section 11.1.1, “SYSTEM SET” on page 110.

REG[00h] Memory Configuration Register
Address = 8000h Default = 10h Read/Write

n/a		Screen Origin Compensation	Reserved	STN Panel Drive Select	Character Height	Reserved	Character Generator Select
7	6	5	4	3	2	1	0

Note

When REG[00h] is written to, the S1D13709 automatically performs the following functions.

1. Resets the internal timing generator
2. Disables the display
3. When indirect addressing mode is selected, completes and exits power save mode

bit 5 Screen Origin Compensation (IV)

This bit controls Screen Origin Compensation which is used for inverse display and is usually set to 1. A common method of displaying inverted characters is to Exclusive-OR the text layer with the graphics back-ground layer. However when this is done, the inverted characters at the top or left of the screen become difficult to read. This is because the character origin is at the top-left of its bitmap and there are no background pixels either above or to the left of these characters.

This bit causes the S1D13709 to offset the text screen against the graphics back layer by one vertical pixel. To shift the text screen horizontally, the horizontal pixel scroll function (REG[1Bh] or the HDOT SCR command for indirect addressing) can be used to shift the text screen 1 to 7 pixels to the right. If both of these functions are enabled, all characters have the appropriate surrounding back-ground pixels to ensure easy reading of the inverted characters.

When this bit = 0, screen origin compensation is done.

When this bit = 1, screen origin compensation is not done.

The following figure shows an example of screen origin compensation and the HDOT SCR command in use.

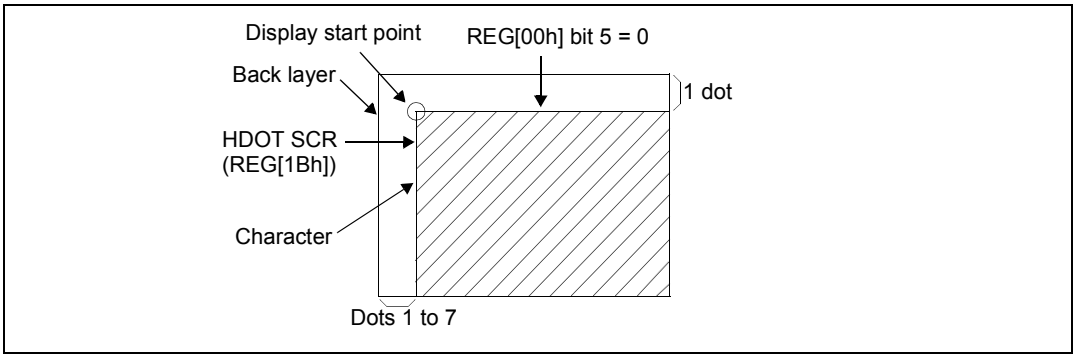


Figure 10-1 Screen Origin Compensation and HDOT SCR Adjustment

Note

Screen origin compensation has no effect on CGRAM characters. To align the CGRAM characters with the rest of the image when screen origin compensation is done, CGRAM must be re-programmed so that the characters align with the rest of the image.

bit 4 Reserved

The default value for this bit is 1.

bit 3 STN Panel Drive Select (W/S)
This bit specifies the STN-LCD panel drive method.
When this bit = 0, a single panel drive is selected.
When this bit = 1, a dual panel drive is selected.

The following diagrams show examples of the possible drive methods.

Note
This bit is for the STN interface only. (REG[34h] bit 0 = 0)
For the TFT interface, this bit must be set to 0.

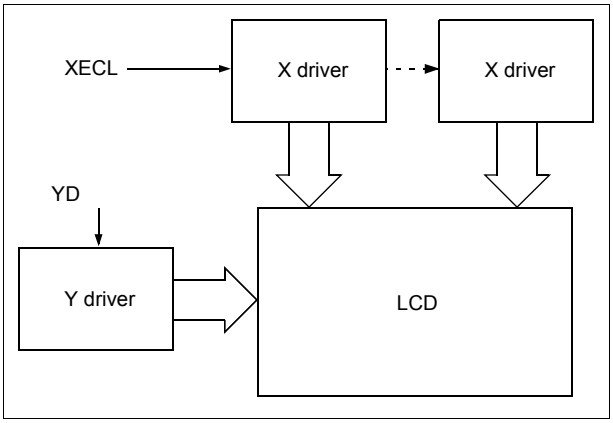


Figure 10-2 Single Drive Panel Display

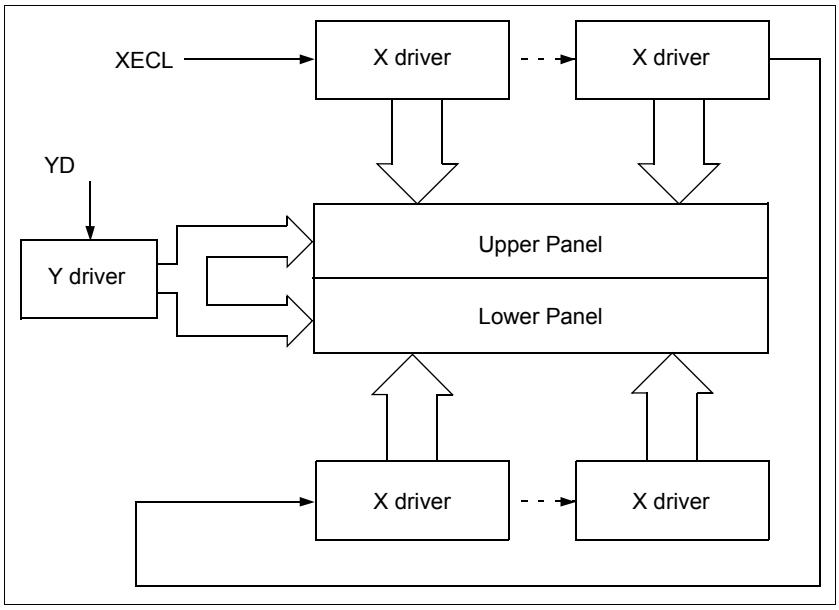


Figure 10-3 Dual Drive Panel Display

The following table summarizes the parameters that must be configured for correct operation of an LCD panel.

Table 10-2 LCD Parameter Summary

Parameter	Single Panel (REG[00h] bit 3 = 0)		Dual Panel (REG[00h] bit 3 = 1)	
	REG[00h] bit 5 = 1 (IV)	REG[00h] bit 5 = 0 (IV)	REG[00h] bit 5 = 1 (IV)	REG[00h] bit 5 = 0 (IV)
CR	REG[03h] bits 7-0	REG[03h] bits 7-0	REG[03h] bits 7-0	REG[03h] bits 7-0
TCR	REG[04h] bits 7-0	REG[04h] bits 7-0	REG[04h] bits 7-0	REG[04h] bits 7-0
LF	REG[05h] bits 7-0	REG[05h] bits 7-0	REG[05h] bits 7-0	REG[05h] bits 7-0
SL1	00h to REG[05h] bits 7-0	00h to REG[05h] bits 7-0 (See Note)	[REG[05h] bits 7-0 + 1] ÷ 2 - 1	[REG[05h] bits 7-0 + 1] ÷ 2 - 1
SL2	00h to REG[05h] bits 7-0	00h to REG[05h] bits 7-0 (See Note)	[REG[05h] bits 7-0 + 1] ÷ 2 - 1	[REG[05h] bits 7-0 + 1] ÷ 2 - 1
SAD1	First screen block (Start Address = REG[0Bh], REG[0Ch])			
SAD2	Second screen block (Start Address = REG[0Eh], REG[0Fh])			
SAD3	Third screen block (Start Address = REG[11h], REG[12h])			
SAD4	Invalid		Fourth screen block (Start Address = REG[13h], REG[14h])	
Cursor movement range	Continuous movement over whole screen		Above-and-below configuration: continuous movement over whole screen	

Note

Screen Origin Compensation shifts the character font down by one pixel row. If the bottom pixel row of the font is at the bottom of the Screen Block, that row disappears when REG[00h] bit 5 = 0. To compensate for the bad visual effect, SL can be increased by one.

bit 2 — Character Height (M2)

This bit selects the height of the character bitmaps. It is possible to display characters greater than 16 pixels high by creating a bitmap for each portion of each character and using graphics mode to reposition them.
When this bit = 0, the character height is 8 pixels.
When this bit = 1, the character height is 16 pixels.

bit 1 — Reserved

The default value for this bit is 0.

bit 0 — Character Generator Select (M0)

This bit determines whether characters are generated by the internal character generator ROM (CGROM) or character generator RAM (CGRAM). The CGROM contains 160, 5x7 pixel characters which are fixed at fabrication. The CGRAM can contain up to 256 user-defined characters which are mapped at the CG Start Address (REG[1Ah] - REG[19h]). However, when the CGROM is used, the CGRAM can only contain up to 64, 8x8 pixel characters.
When this bit = 0, the internal CGROM is selected.
When this bit = 1, the internal CGRAM is selected.

REG[01h] Horizontal Character Size Register Address = 8001h Default = 00h Read/Write							
MOD	n/a			Horizontal Character Size bits 3-0			
7	6	5	4	3	2	1	0

bit 7 MOD

This bit selects the AC frame drive waveform period. MOD is typically set to 1.
When this bit = 0, 16-line AC drive is selected.
When this bit = 1, two-frame AC drive is selected.

In two-frame AC drive, the MOD period is twice the frame period. In 16-line AC drive, MOD inverts every 16 lines. Although 16-line AC drive gives a more readable display, horizontal lines may appear when using high LCD drive voltages or at high viewing angles.

Note

This bit is for the STN interface only. (REG[34h] bit 0 = 0)
For the TFT interface, this bit is ignored.

bits 3-0 Horizontal Character Size (FX) bits [3:0]

These bits define the horizontal size, or width, of each character, in pixels.

REG[01h] bits 3-0 = Horizontal Character Size in pixels - 1

The S1D13709 handles display data in 8-bit units, therefore characters larger than 8 pixels wide must be formed from 8-pixel segments. The following diagram shows an example of a character requiring two 8-pixel segments where the remainder of the second eight bits are not displayed. This also applies to the second screen layer. In graphics mode, the normal character field is also eight pixels. If a wider character field is used, any remainder in the second eight bits is not displayed.

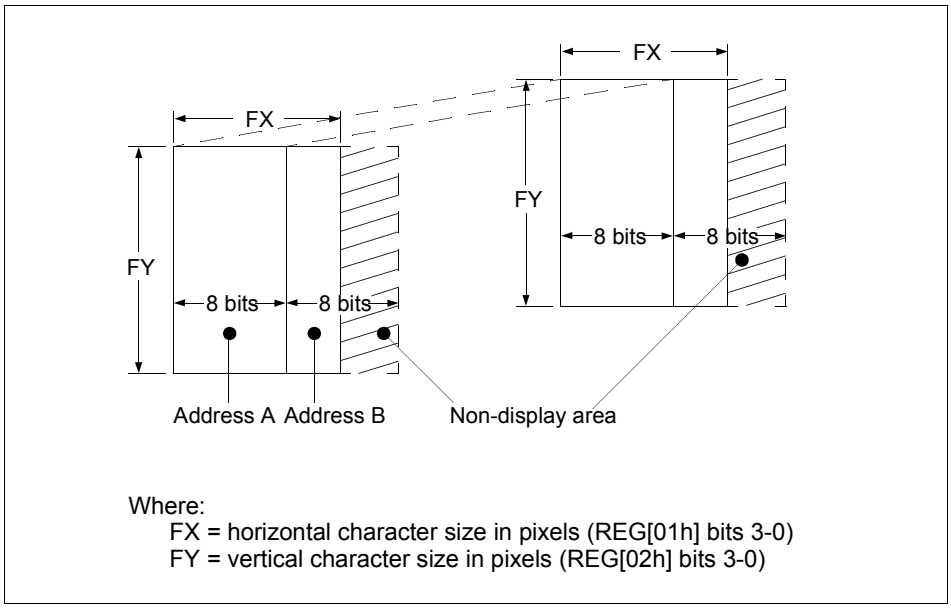


Figure 10-4 Horizontal and Vertical Character Size Example

REG[02h] Vertical Character Size Register							
Address = 8002h Default = 00h							Read/Write
n/a				Vertical Character Size bits 3-0			
7	6	5	4	3	2	1	0

bit 3-0 Vertical Character Size (FY) bits [3:0]
These bits define the vertical size, or height, of each character, in pixels.
REG[02h] bits 3-0 = Vertical Character Size in pixels - 1

Note
When [FY] > 8, the Character Height (M2) should be 16-bit. (REG[00h] bit 2 = 1)

REG[03h] Character Bytes Per Row Register							
Address = 8003h Default = 00h							Read/Write
Character Bytes Per Row bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Character Bytes Per Row (CR) bits [7:0]
These bits determine the size of each character row (or display line), in bytes, to a maximum of 253. The value of these bits is defined in terms of CR which is calculated in Section 15.1.1, “SYSTEM SET Command and Parameters for STN interface” on page 147.
REG[03h] bits 7-0 = ([CR] x bpp) - 1

REG[04h] Total Character Bytes Per Row Register							
Address = 8004h Default = 00h							Read/Write
Total Character Bytes Per Row bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Total Character Bytes Per Row (TCR) bits [7:0]

These bits set the length of one line, including horizontal blanking, in bytes, to a maximum of 255. The value of these bits is defined in terms of TCR which is calculated in Section 15.1.1, "SYSTEM SET Command and Parameters for STN interface" on page 147. TCR can be adjusted to hold the frame period constant and minimize jitter for any given the system clock frequency, f_{SYSCLK}.

REG[04h] bits 7-0 = [TCR] - 1

Note

TCR must be programmed such that the following formulas are valid.

$[TCR] \geq [CR] + 2$

$2 \leq TCR \leq 255$

REG[05h] Frame Height Register							
Address = 8005h Default = 00h							Read/Write
Frame Height bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Frame Height (LF) bits [7:0]

These bits determine the frame height, in lines. The maximum frame height is 256 lines.

REG[05h] bits 7-0 = frame height in lines - 1.

Note

If the Panel Drive Select bit is set for a dual drive panel (REG[00h] bit 3 = 1), the frame height must be an even number of lines resulting in an odd number value for REG[05h] bits 7-0.

REG[06h] Horizontal Address Range Register 0							
Address = 8006h Default = 00h							Read/Write
Horizontal Address Range bits 7-0							
7	6	5	4	3	2	1	0

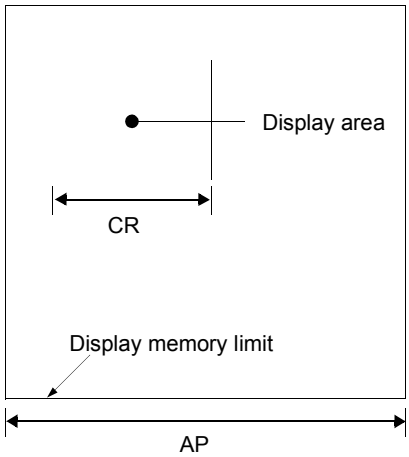
REG[07h] Horizontal Address Range Register 1							
Address = 8007h Default = 00h							Read/Write
	Horizontal Address Range bits 14-8						
7	6	5	4	3	2	1	0

bits 14-0 Horizontal Address Range (AP) bits [14:0]

These bits define the horizontal address range of the virtual screen. The maximum value for this register is 7FFFh.

REG[07h] bits 6-0, REG[06h] bits 7-0 = Addresses per line

The following diagram demonstrates the relationship between the Horizontal Address Range and the Character Bytes Per Row value.



Where:

CR = character bytes per row (REG[03h] bits 7-0)

AP = horizontal address range (REG[06h] bits 7-0, REG[07h] bits 6-0)

Figure 10-5 Horizontal Address Range and Character Bytes Per Row Relationship

POWER SAVE

The POWER SAVE command is used to enter power save mode on the S1D13709 when indirect addressing is used. For further information on the POWER SAVE command, see Section 11.1.2, “POWER SAVE” on page 112.

Note

When indirect addressing is used, the SYSTEM SET command is used to exit power save mode. For further information on the SYSTEM SET command, see Section 11.1.1, “SYSTEM SET” on page 110.'

REG[08h] Power Save Mode Register
Address = 8008h Default = 01h Read/Write

n/a							Power Save Mode Enable
7	6	5	4	3	2	1	0

bit 0 Power Save Mode Enable

This bit controls the state of the software initiated power save mode. When power save mode is disabled, the S1D13709 is operating normally. When power save mode is enabled, the S1D13709 is in a power efficient state where all internal operations, including the oscillator, are stopped. For more information on the condition of the S1D13709 during Power Save Mode, see Section 17, “Power Save Mode” on page 186.
When this bit = 0, power save mode is disabled (see note).
When this bit = 1, power save mode is enabled (default).

Note

Enabling power save mode automatically clears the Display Enable bit (REG[09h] bit 0). After power save mode is disabled, the Display Enable bit must be set (REG[09h] bit 0 = 1) in order to turn on the display again.

Note

After power save mode is enabled (REG[08h]bit 0 = 1), a 50ms wait is required before power save mode is disable again (REG[08h]bit 0 = 0).

10.3.2 Display Control Registers

These registers enable/disable the display, and control the cursor and layered screens.

DISP ON/OFF

The DISP ON/OFF command is used to enable/disable the display and display attributes when indirect addressing is used. The values from REG[0Ah] are passed as parameters when the DISP ON/OFF command is issued. For further information on the DISP ON/OFF command, see Section 11.1.3, “DISP ON/OFF” on page 112.

REG[09h] Display Enable Register
Address = 8009h Default = 00h Read/Write

n/a							Display Enable
7	6	5	4	3	2	1	0

bit 0 Display Enable
This bit controls the LCD display, including the cursor and all layered screens. The display enable bit takes precedence over the individual attribute bits in the Display Attribute register, REG[0Ah]. For information on LCD pin states when the display is off (REG[09h] bit 0 = 0), see Table 17-1 “State of LCD Pins and Crystal During Power Save Mode,” on page 187.
When this bit = 0, the display is off.
When this bit = 1, the display is on.

Note
After the display is turned off (REG[09h]bit 0 = 0), a 50ms wait is required before the display is turned on again (REG[09h]bit 0 = 1).

REG[0Ah] Display Attribute Register
Address = 800Ah Default = 00h Read/Write

SAD3 Attribute bits 1-0		SAD2 Attribute bits 1-0		SAD1 Attribute bits 1-0		Cursor Attribute bits 1-0	
7	6	5	4	3	2	1	0

bits 7-6 SAD3 Attribute (FP 5-4) bits [1:0]
These bits control the attributes of the third screen block (SAD3) as follows.

Table 10-3 Screen Block 3 Attribute Selection

Third Screen Block (SAD3)			
REG[0Ah] bit 7	**REG[0Ah] bit 6**	**Attributes**	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

bits 5-4 SAD2 Attribute (FP 3-2) bits [1:0]

These bits control the attributes of the second screen block (SAD2). These bits also control the attributes of the fourth screen block (SAD4) when it is enabled by setting the Panel Drive Select bit to dual panel mode (REG[00h] bit 3 = 1). In this mode, the attributes of the second screen block (SAD2) and the fourth screen block (SAD4) share the same settings and cannot be set independently.

Table 10-4 Screen Block 2/4 Attribute Selection

Second Screen Block (SAD2, SAD4)			
REG[0Ah] bit 5	**REG[0Ah] bit 4**	**Attributes**	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

bits 3-2 SAD1 Attribute (FP 1-0) bits [1:0]

These bits control the attributes of the first screen block (SAD1) as follows.

Table 10-5 Screen Block Attribute Selection

First Screen Block (SAD1)			
REG[0Ah] bit 3	**REG[0Ah] bit 2**	**Attributes**	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0		Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1		Flash at f_{FR}/4 Hz (approx. 16 Hz)

bits 1-0 Cursor Attribute (FC) bits [1:0]

These bits control the cursor and set the flash rate. The cursor flashes with a 70% duty cycle (ON 70% of the time and OFF 30% of the time).

Table 10-6 Cursor Flash Rate Selection

Bit 1	Bit 0	Cursor Display	
0	0	OFF (Blank)	
0	1	ON	No Flashing
1	0	ON	Flash at f_{FR}/32 Hz (approx. 2 Hz)
1	1	ON	Flash at f_{FR}/64 Hz (approx. 1 Hz)

Note

When the cursor is disabled, a write to memory automatically enables the cursor and places the cursor at the next memory location. A read from memory does not enable the cursor, however, it still places the cursor at the next memory location.

SCROLL

The SCROLL command is used to configure the display start addresses for the various screen blocks when indirect addressing is used. The values from REG[0Bh] through REG[14h] are passed as parameters when the SCROLL command is issued. For further information on the SCROLL command, see Section 11.1.4, “SCROLL” on page 113.

REG[0Bh] Screen Block 1 Start Address Register 0 Address = 800Bh Default = 00h Read/Write							
Screen Block 1 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[0Ch] Screen Block 1 Start Address Register 1 Address = 800Ch Default = 00h Read/Write							
SAD1 Indirectly Update Enable	Screen Block 1 Start Address bits 14-8 (MSB)						
7	6	5	4	3	2	1	0

REG[0Ch] bit 7 SAD1 Indirectly Update Enable

This bit controls SAD1 updating for scrolling function. For further information on this bit, see Section 15.4, “Smooth Horizontal Scrolling” on page 175.

When this bit = 0, updated SAD1 is reflected to the display function regardless of REG[1Bh] bit 7.

When this bit = 1, updated SAD1 is reflected to the display function only when REG[1Bh] bit 7 is 1.

REG[0Ch] bits 6-0, REG[0Bh] bits 7-0

Screen Block 1 Start Address (SAD1) bits [14:0]

These bits determine the memory start address of screen block 1.

Note

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

REG[0Dh] Screen Block 1 Size Register Address = 800Dh Default = 00h Read/Write							
Screen Block 1 Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Screen Block 1 Size (SL1) bits [7:0]

These bits determine the size of screen block 1, in lines.

REG[0Dh] bits 7-0 = screen block 1 size in number of lines - 1

Note

The relationship between the screen block start address (SADx), screen block size (SLx), and the display mode is described in Table 10-7 “Display Modes,” on page 79.

REG[0Eh] Screen Block 2 Start Address Register 0							
Address = 800Eh Default = 00h							Read/Write
Screen Block 2 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[0Fh] Screen Block 2 Start Address Register 1							
Address = 800Fh Default = 00h							Read/Write
SAD2 Indirectly Update Enable	Screen Block 2 Start Address bits 14-8 (MSB)						
7	6	5	4	3	2	1	0

REG[0Fh] bit 7 SAD2 Indirectly Update Enable

This bit controls SAD2 updating for scrolling function. For further information on this bit, see Section 15.4, “Smooth Horizontal Scrolling” on page 175.

When this bit = 0, updated SAD2 is reflected to the display function regardless of REG[1Bh] bit 7.

When this bit = 1, updated SAD2 is reflected to the display function only when REG[1Bh] bit 7 is 1.

REG[0Fh] bits 6-0, REG[0Eh] bits 7-0

Screen Block 2 Start Address (SAD2) bits [14:0]

These bits determine the memory start address of screen block 2.

Note

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

REG[10h] Screen Block 2 Size Register							
Address = 8010h Default = 00h							Read/Write
Screen Block 2 Size bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Screen Block 2 Size (SL2) bits [7:0]

These bits determine the size of screen block 2, in lines.

REG[10h] bits 7-0 = screen block 2 size in number of lines - 1

Note

The relationship between the screen block start address (SADx), screen block size (SLx), and the display mode is described in Table 10-7 “Display Modes,” on page 79.

REG[11h] Screen Block 3 Start Address Register 0							
Address = 8011h Default = 00h							Read/Write
Screen Block 3 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[12h] Screen Block 3 Start Address Register 1							
Address = 8012h Default = 00h							Read/Write
SAD3 Indirectly Update Enable	Screen Block 3 Start Address bits 14-8 (MSB)						
7	6	5	4	3	2	1	0

REG[12h] bit 7 SAD3 Indirectly Update Enable

This bit controls SAD3 updating for scrolling function. For further information on this bit, see Section 15.4, “Smooth Horizontal Scrolling” on page 175.

When this bit = 0, updated SAD3 is reflected to the display function regardless of REG[1Bh] bit 7.

When this bit = 1, updated SAD3 is reflected to the display function only when REG[1Bh] bit 7 is 1.

REG[12h] bits 6-0, REG[11h] bits 7-0

Screen Block 3 Start Address (SAD3) bits [14:0]

These bits determine the memory start address of screen block 3.

Note

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

REG[13h] Screen Block 4 Start Address Register 0							
Address = 8013h Default = 00h							Read/Write
Screen Block 4 Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[14h] Screen Block 4 Start Address Register 1							
Address = 8014h Default = 00h							Read/Write
SAD4 Indirectly Update Enable	Screen Block 4 Start Address bits 14-8 (MSB)						
7	6	5	4	3	2	1	0

REG[14h] bit 7 SAD4 Indirectly Update Enable

This bit controls SAD4 updating for scrolling function. For further information on this bit, see Section 15.4, “Smooth Horizontal Scrolling” on page 175.

When this bit = 0, updated SAD4 is reflected to the display function regardless of REG[1Bh] bit 7.

When this bit = 1, updated SAD4 is reflected to the display function only when REG[1Bh] bit 7 is 1.

REG[14h] bits 6-0, REG[13h] bits 7-0

Screen Block 4 Start Address (SAD4) bits [14:0]

These bits determine the memory start address of screen block 4.

Note

When the start address is changed, the LSB must be programmed before the MSB. The start address does not change until the MSB is written.

The following table summaries the required settings for each possible display mode.

Table 10-7 Display Modes

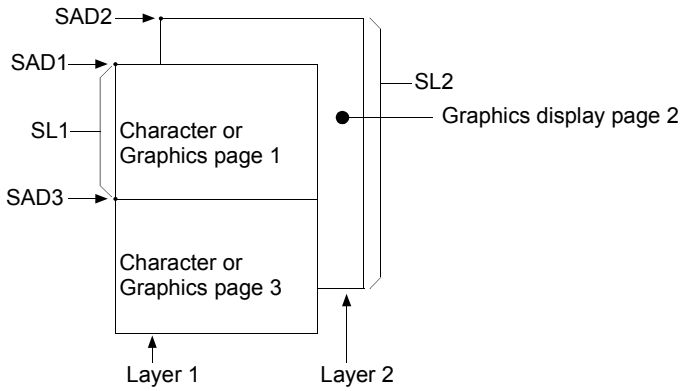
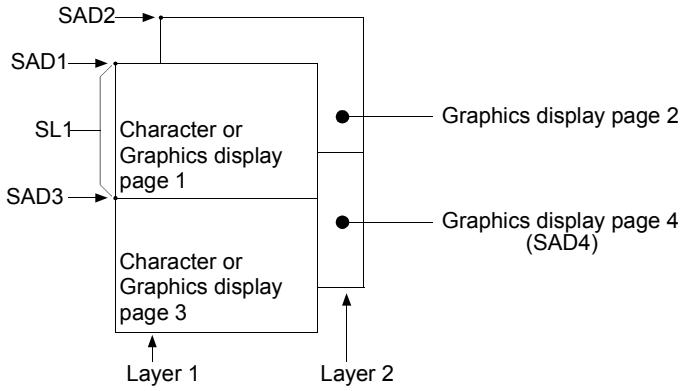
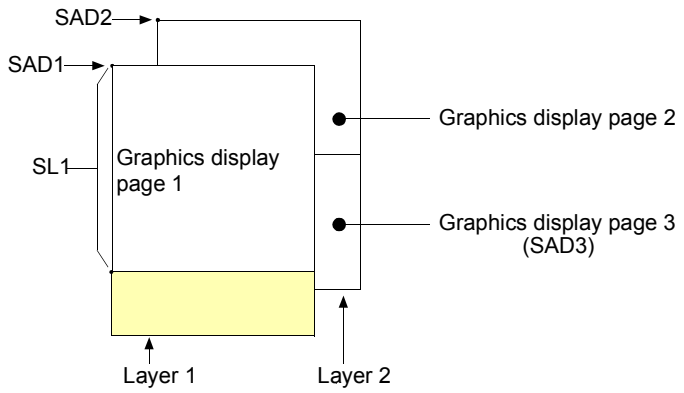
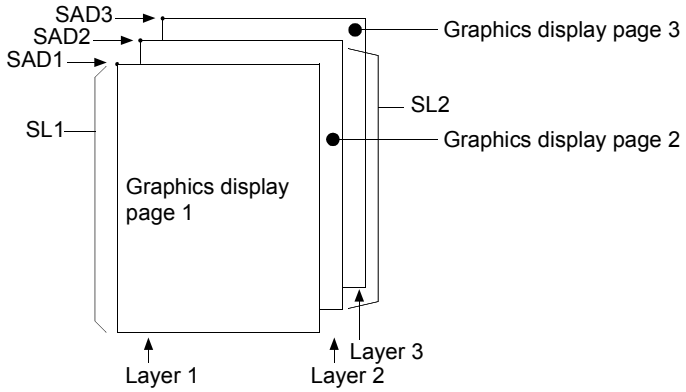
REG[00h] bit 3 (W/S)	Screen	First Layer	Second Layer
0	First Screen Block	SAD1	SAD2
	Second Screen Block	SL1	SL2
	Third Screen Block (partitioned screen)	SAD3 (see note 1) Set both SL1 and SL2 to LF + 1 if not using a partitioned screen.	
	Screen Configuration Example  		
1	First Screen Block	SAD1, SL1	SAD2, SL2
	Second Screen Block	SAD3 (see note 2)	SAD4 (see note 2)
	Set both SL1 and SL2 to ([LF] ÷ 2 + 1)		
	Screen Configuration Example  		

Table 10-7 Display Modes (Continued)

REG[00h] bit 3 (W/S)	Screen	First Layer	Second Layer
0	First Screen Block	SAD1, SL1	SAD2, SL2
	Second Screen Block	—	SAD3 (see note 2)
	Set SL1 > SL2		
	Screen Configuration Example		



REG[00h] bit 3 (W/S)	Screen	First Layer	Second Layer	Third Layer
0	Three-Layer Configuration	SAD1, SL1 = LF + 1	SAD2, SL2 = LF + 1	SAD3
	Screen Configuration Example			



Note

[1]The size of screen block 3, in lines, is automatically set to the size of the screen block with the least number of lines (either SL1 or SL2).

[2]The parameters corresponding to SL3 and SL4 are fixed by REG[05h] bits 7-0 (LF) and do not have to be set.

[3]If a dual panel is selected (REG[00h] bit 3 = 1), the differences between SL1 and (LF + 1) ÷ 2, and between SL2 and (LF + 1) ÷ 2, are blanked.

[3]W/S = 1 is supported for the STN interface only.

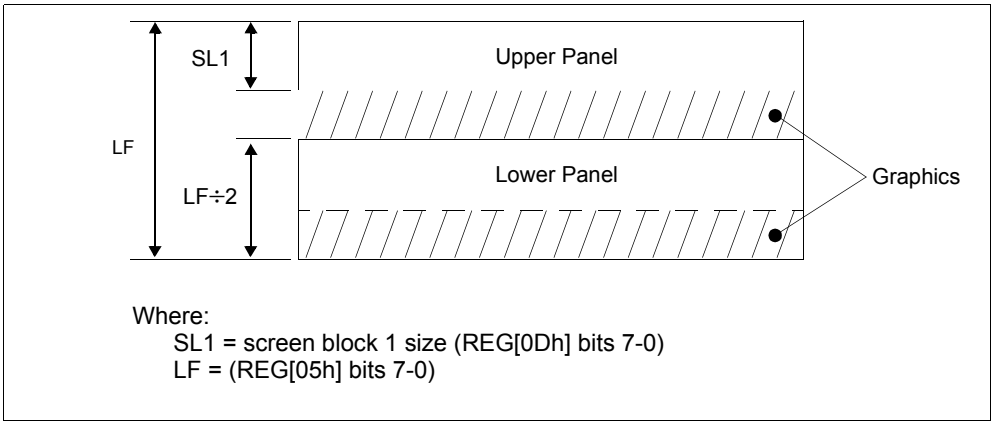


Figure 10-6 STN Dual Panel Display Height

CSRFORM

The CSRFORM command is used to configure the S1D13709 cursor when indirect addressing is used. The values from REG[15h] through REG[16h] are passed as parameters when the CSRFORM command is issued. For further information on the CSRFORM command, see Section 11.1.5, “CSRFORM” on page 113.

The cursor registers are used to set the size, shape, and position of the cursor. Although the cursor is normally only used for text displays, it may be used for graphics displays when displaying special characters.

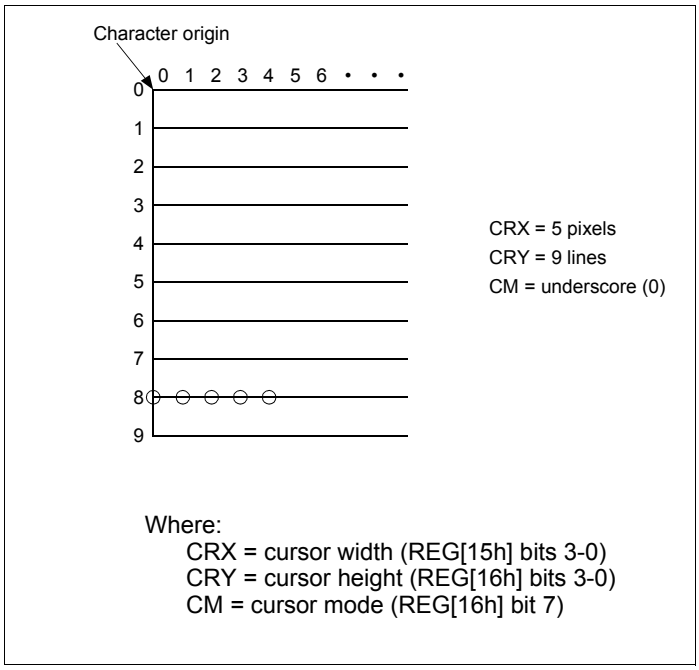


Figure 10-7 Cursor Size and Position

REG[15h] Cursor Width Register
Address = 8015h Default = 00h Read/Write

Automatically Enabling Cursor Disable	n/a			Cursor Width bits 3-0			
7	6	5	4	3	2	1	0

bit 7 Automatically Enabling Cursor Disable
This bit controls the automatically cursor enabling feature.
When this bit = 0b and the cursor is off (REG[0Ah] bits 1-0 = 00b), the cursor is enabled automatically (REG[0Ah] bits 1-0 = 01b) when the display memory is written or read from the host.
When this bit = 1b and the cursor is off (REG[0Ah] bits 1-0 = 00b), the cursor stays off regardless of access to the display memory from the host.

bits 3-0 Cursor Width (CRX) bits[3:0]
These bits specify the width (or horizontal size) of the cursor, in pixels from the character origin (see Figure 10-7 “Cursor Size and Position,” on page 81).
REG[15h] bits 3-0 = cursor width in pixels - 1

Note
The cursor width must be less than or equal to the horizontal character size.
(REG[16h] bits 3-0 <= REG[01h] bits 3-0)

REG[16h] Cursor Height Register
Address = 8016h Default = 00h Read/Write

Cursor Mode	n/a			Cursor Height bits 3-0			
7	6	5	4	3	2	1	0

bit 7 Cursor Mode (CM)
This bit determines the cursor mode. When graphics mode is selected, this bit must be set to 1.
When this bit = 0, an underscore cursor (_) is selected.
When this bit = 1, a block cursor (n) is selected.

bits 3-0 Cursor Height (CRY) bits [3:0]
For an underscore cursor (REG[16h] bit 7 = 0), these bits set the location of the cursor, in lines from the character origin (see Figure 10-7 “Cursor Size and Position,” on page 81).
For a block cursor (REG[16h] bit 7 = 1), these bits set the height (or vertical size) of the cursor, in lines from the character origin (see Figure 10-7 “Cursor Size and Position,” on page 81).
REG[16h] bits 3-0 = cursor height in lines - 1

Note
The vertical cursor size must be less than or equal to the vertical character size.
(REG[16h] bits 3-0 <= REG[02h] bits 3-0)

CSRDIR

The CSRDIR command controls cursor movement when indirect addressing is used. The values from REG[17h] are passed as part of the command when the CSRDIR command is issued. For further information on the CSRDIR command, see Section 11.1.6, “CSRDIR” on page 114.

REG[17h] Cursor Shift Direction Register Address = 8017h Default = 00h Read/Write							
n/a						Cursor Shift Direction bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 Cursor Shift Direction bits [1:0]

These bits are only used in Indirect Addressing mode.

These bits set the direction of automatic cursor increment when the cursor is automatically moved after a memory access (read or write). The cursor can move left/right by one character or up/down by the number of bytes specified by the horizontal address range (or address pitch), REG[06h] - REG[07h]. When reading from and writing to display memory, this automatic cursor increment controls the display memory address increment on each read or write.

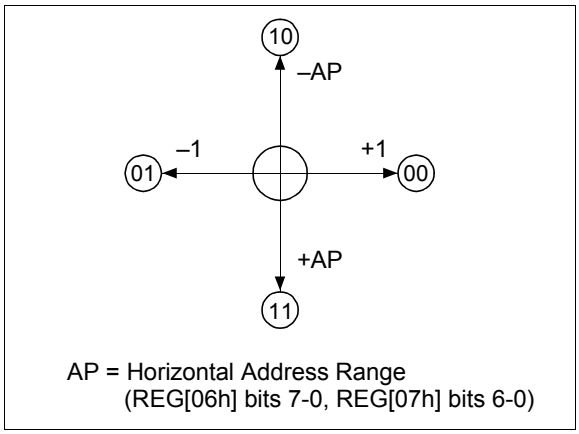


Figure 10-8 Cursor Direction

Table 10-8 Cursor Shift Direction

Direct Mode		Indirect Mode Command	Shift Direction
Bit 1	Bit 0		
0	0	4C	Right
0	1	4D	Left
1	0	4E	Up
1	1	4F	Down

Note

The cursor moves in address units even if horizontal character size is equal to 9 (REG[01h] bits 3-0 = 9), therefore the cursor address increment must be preset for movement in character units. For further information, see Section 12.3, “Cursor Control” on page 129.

OVLAY

The OVLAY command selects layered screen composition and screen text/graphics mode when indirect addressing is used. The values from REG[18h] are passed as parameters when the OVLAY command is issued. For further information on the OVLAY command, see Section 11.1.7, “OVLAY” on page 114.

REG[18h] Overlay Register
Address = 8018h Default = 00h Read/Write

n/a			3 Layer Overlay Select	Screen Block 3 Display Mode	Screen Block 1 Display Mode	Layer Composition Method bits 1-0	
7	6	5	4	3	2	1	0

bit 4 3 Layer Overlay Select (OV)
This bit determines how many layers are used when graphics mode is enabled. For mixed text and graphics, this bit must be set to 0.
When this bit = 0, two layers are used.
When this bit = 1, three layers are used.

bit 3 Screen Block 3 Display Mode (DM1)
This bit determines the display mode for screen block 3.
When this bit = 0, screen block 3 is configured for text mode.
When this bit = 1, screen block 3 is configured for graphics mode.

Note

Screen blocks 2 and 4 can display graphics only.

Note

When text mode is selected, only 1bpp is supported (REG[20h] bits 1-0 = 00).

bit 2 Screen Block 1 Display Mode (DM0)
This bit determines the display mode for screen block 1.
When this bit = 0, screen block 1 is configured for text mode.
When this bit = 1, screen block 1 is configured for graphics mode.

Note

Screen blocks 2 and 4 can display graphics only.

Note

When text mode is selected, only 1bpp is supported (REG[20h] bits 1-0 = 00).

bits 1-0 Layer Composition Method (MX) bits [1:0]
These bits select the layered screen composition method, which can be OR, AND, or Exclusive-OR. Since the screen composition is organized in layers and not by screen blocks, when using a layer divided into two screen blocks, different composition methods cannot be specified for the individual screen blocks.

Table 10-9 Composition Method Selection

REG[18h] bit 1	REG[18h] bit 0	Function	Composition Method	Applications
0	0	L1 ∪ L2 ∪ L3	OR	Underlining, rules, mixed text and graphics
0	1	(L1 ⊕ L2) ∪ L3	Exclusive-OR	Inverted characters, flashing regions, underlining
1	0	(L1 ∩ L2) ∪ L3	AND	Simple animation, three-dimensional appearance
1	1	—	—	Reserved

Note
L1: First layer (text or graphics). If text is selected, layer L3 cannot be used.
L2: Second layer (graphics only)
L3: Third layer (graphics only)

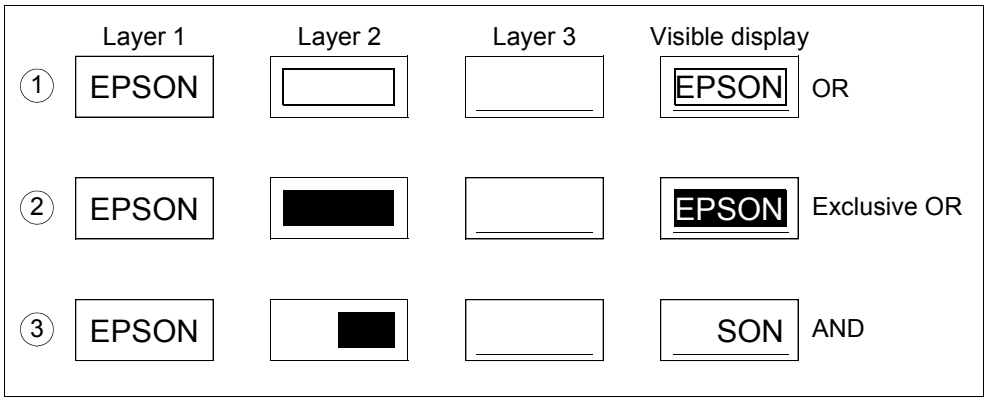


Figure 10-9 Combined Layer Display Examples

Note
L1: Not flashing
L2: Flashing at 1 Hz
L3: Flashing at 2 Hz

CGRAM ADR

The CGRAM ADR command sets the start address of the character generator RAM (CGRAM) when indirect addressing is used. The values from REG[19h] through REG[1Ah] are passed as parameters when the CGRAM ADR command is issued. For further information on the CGRAM ADR command, see Section 11.1.8, “CGRAM ADR” on page 114.

REG[19h] Character Generator RAM Start Address Register 0							
Address = 8019h Default = 00h							Read/Write
CGRAM Start Address bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[1Ah] Character Generator RAM Start Address Register 1							
Address = 801Ah Default = 00h							Read/Write
n/a	CGRAM Start Address bits 14-8 (MSB)						
7	6	5	4	3	2	1	0

bits 14-0 Character Generator RAM Start Address bits [14:0]
These bits determine the memory start address of the Character Generator RAM (CGRAM). The exact memory location of the start of each character stored in CGRAM can be calculated by multiplying the character code index by the character height and adding the total to the CGRAM start address.

For example, to determine the address of a 8x8 character at character code index 80h with a CGRAM start address of 6000h, the following calculation can be used.

character start = (character code index x character height) + CGRAM start address
= (80h x 8) + 6000h
= 400h + 6000h
= 6400h

The character starts in RAM at address 6400h and takes 8 memory locations.

HDOT SCR

The HDOT SCR command sets the horizontal scroll position when indirect addressing is used. The values from REG[1Bh] are passed as parameters when the HDOT SCR command is issued. For further information on the HDOT SCR command, see Section 11.1.9, "HDOT SCR" on page 115.

Normal scrolling on text screens allows scrolling of entire characters only. The HDOT SCR command provides horizontal pixel scrolling for text screens. HDOT SCR cannot be used on individual layers.

Note

HDOT SCR must be set to zero for all display modes except 1 bpp (REG[20h] Bit-Per-Pixel Select Register bits 1-0 = 0).

REG[1Bh] Horizontal Pixel Scroll Register

Address = 801Bh Default = 00h Read/Write

SADx Update Enable	n/a				Horizontal Pixel Scroll bits 2-0		
7	6	5	4	3	2	1	0

bit 7 SADx Update Enable

This bit enables SDA1, SAD2, SAD3 and SAD4 updating. In order to make smooth horizontal scrolling, it is recommended to update SAD and Horizontal Pixel Scroll bits at the same time. For further information, see Section 15.4, "Smooth Horizontal Scrolling" on page 175.

When this bit = 0, SADx is not updated.

When this bit = 1, SADx is updated.

Note

Before setting this bit to 1, SAD indirectly enable bit should be set 1 (REG[0Ch] bit 7, REG[0Fh] bit 7, REG[12h] bit 7 and REG[14h] bit 7).

bits 2-0 Horizontal Pixel Scroll bits [2:0]

These bits specify the number of horizontal pixels to scroll the display. The character bytes per row (CR), REG[03h] bits 7-0, must be set to one more than the actual number of horizontal characters before using horizontal pixel scroll. Smooth scrolling can be simulated by repeatedly changing the value of REG[1Bh] bits 2-0. See Section 12.5.6, "Horizontal Pixel Scrolling (HDOTSCR)" on page 140 for more information on scrolling the display.

Note

Before setting these bits, REG[4Bh] bit 7 should be set to select these bits update timing.

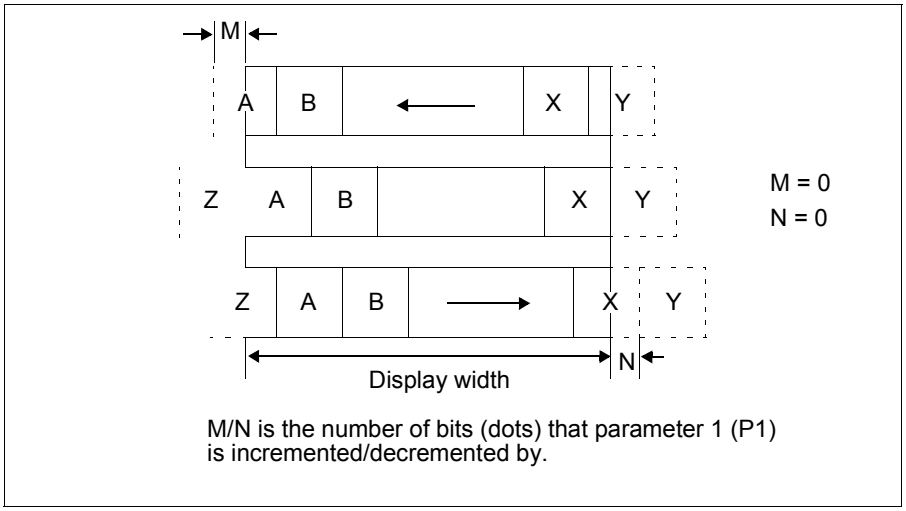


Figure 10-10 Horizontal Scrolling

10.3.3 Drawing Control Registers

CSRW

The CSRW command sets the cursor address when indirect addressing is used. The values from REG[1Ch] through REG[1Dh] are passed as parameters when the CSRW command is issued. For further information on the CSRW command, see Section 11.1.10, “CSRW” on page 115.

REG[1Ch] Cursor Write Register 0 Address = 801Ch Default = 00h							Write Only
Cursor Write bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[1Dh] Cursor Write Register 1 Address = 801Dh Default = 00h							Write Only
n/a	Cursor Write bits 14-8 (MSB)						
7	6	5	4	3	2	1	0

bits 14-0 Cursor Write (CSRW) bits [14:0]
These bits are only used in Indirect Addressing mode.
These bits set the display memory address to the data at the cursor position as shown in Figure 12-11 “Cursor Movement,” on page 131.

Note
The host cannot directly access the display memory in indirect addressing mode. The MREAD and MWRITE commands use the address in this register when in indirect mode. The cursor address register can only be modified by the CSRW command, and by the automatic increment after an MREAD or MWRITE command. It is not affected by display scrolling.
If a new address is not set, display memory accesses are from the last set address or the address after previous automatic increments.

CSRR

The CSRR command reads the cursor address when indirect addressing is used. The values from REG[1Eh] through REG[1Fh] are passed as parameters when the CSRR command is issued. For further information on the CSRR command, see Section 11.1.11, “CSRR” on page 115.

REG[1Eh] Cursor Read Register 0
Address = 801Eh Default = 00h Read Only

Cursor Read bits 7-0 (LSB)							
7	6	5	4	3	2	1	0

REG[1Fh] Cursor Read Register 1
Address = 801Fh Default = 00h Read Only

	Cursor Read bits 14-8 (MSB)						
7	6	5	4	3	2	1	0

bits 14-0 Cursor Read (CSRR) bits [14:0]
These bits are only used in Indirect Addressing mode.
These bits indicate the memory address where the cursor is currently located. After issuing the command, the data read address is read twice. Once for the low byte and then again for the high byte of the register.

10.3.4 Gray Scale Register

GRAYSCALE

The GRAYSCALE command selects the gray scale depth, in bits-per-pixel (bpp), when indirect addressing is used. The values from REG[20h] are passed as parameters when the GRAYSCALE command is issued. For further information on the GRAYSCALE command, see Section 11.1.12, “GRAYSCALE” on page 116.

REG[20h] Bit-Per-Pixel Select Register Address = 8020h Default = 00h							Read/Write
n/a						Bit-Per-Pixel Select bits 1-0	
7	6	5	4	3	2	1	0

bits 1-0 Bit-Per-Pixel Select bits [1:0]
These bits select the bit-per-pixel mode as follows.

Table 10-10 Bit-Per-Pixel Selection

REG[20h] bits 1-0	Bits-Per-Pixel
00	1
01	2
10	4
11	Reserved

Note
The TEXT mode is for 1bpp only. When the TEXT mode is selected (REG[18h] bit 2, bit3), these bits must be set to 00.

Note
When 2bpp or 4bpp is selected, the horizontal character size (REG[01h] bits 3-0) must be set to 7h and the Horizontal Pixel Scroll bits (REG[1Bh] bits 2-0) must be set to 0.

Note
When a graphics screen and a graphics screen with Gray Scale enabled are overlaid, both layers are configured to the same color depth. For example, when these bits are 01, the first layer and second layer are 2 bpp.

10.3.5 Production Code Register

ID

The ID command reads the production code of the S1D13709. For further information on the ID command, see Section 11.1.13, “ID” on page 116.

REG[30h] Production Code Register Address = 8030h Default = 59h Read Only							
Production Code bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Product Code bits [7:0] (Read Only)
These read-only bits indicate the product code. The product code for the S1D13709 is 059h.

10.3.6 TFT Interface Registers

All TFT interface registers except TFT color palette registers (REG[31h] - [4Ah]) should not be changed during displaying a TFT-LCD. (REG[09h] bit 0 = 1 and REG[34h] bit 0 = 1)

PLL SET

The PLL SET command sets the PLL parameter to generate a clock for the TFT interface. The values from REG[31h] through REG[33h] are passed as parameters when the PLLSET command is issued. For further information on the PLL SET command, see Section 11.1.14, “PLL SET” on page 116.

REG[31h] TFT PLL Setting Register 0 Address = 8031h Default = E1h Read/Write							
PLL Output Clock Divide Select bits 3-0				PLL Input Clock Divide Select bits 3-0			
7	6	5	4	3	2	1	0

bits 7-4 PLL Output Clock Divide Select bits [3:0]
These bits determine the divide ratio between the PLL output clock and the TFT clock.

Table 10-11 PLL Output Clock Divide Ratio Selection

REG[31h] bits 7-4	Divide Ratio (POR)
0h	1
1h	2
2h	3
...	...
Dh	14
Eh	15
Fh	16

Note
The TFT clock frequency (f_P) must be between 2MHz and 35MHz.

Where:
$f_{PLLI} = f_{SYSCLK} / PIR$
$f_{PLLO} = f_{PLLI} \times N$
$f_{VCO} = f_{PLLO} \times V$
$f_P = f_{PLLO} / POR$

f_{SYSCLK}= System clock (CLKI or Crystal Oscillator) frequency
f_{PLLI} = PLL input clock frequency
f_{PLLO} = PLL output clock frequency
f_{VCO} = VCO clock frequency
f_P = TFT clock (FPSHIFT) frequency
PIR = PLL input clock divide ratio (REG[31h] bits 3-0)
N = N-Counter (REG[32h] bits 3-0)
V = V-Divider (REG[33h] bits 6-5)

bits 3-0 PLL Input Clock Divide Select bits [3:0]
These bits determine the divide ratio between the System clock (CLKI or Crystal Oscillator) and the actual PLL input clock.

Table 10-12 PLL Input Clock Divide Ratio Selection

REG[31h] bits 3-0	Divide Ratio (PIR)
0h	1
1h	2
2h	3
...	...
Ah	11
Bh	12
Ch	13
Ch - Fh	Reserved

Note
The PLL input clock to the PLL (f_{PLLI}) must be between 5MHz and 66MHz.

Where:
$f_{PLLI} = f_{SYSCLK} / PIR$

f_{SYSCLK} = System clock (CLKI or Crystal Oscillator) frequency
f_{PLLI} = PLL input clock frequency

REG[32h] TFT PLL Setting Register 1
Address = 8032h Default = 99h Read/Write

PLL RS bits 3-0				PLL N-Counter bits 3-0			
7	6	5	4	3	2	1	0

bits 7-4 PLL RS bits [3:0]
These bits specify the RS value used for configuring the PLL and are set according to the PLL input frequency.

Table 10-13 PLL RS Selection

PLL Input Clock Frequency (f_{PLLI})	REG[32h] bits 7-4 (RS)
$5M \le f_{PLLI} < 20MHz$	9h
$20M \le f_{PLLI} < 50MHz$	7h
$50M \le f_{PLLI} \le 66MHz$	5h

bits 3-0 PLL N-Counter bits [3:0]
These bits specify the N-Counter value used for configuring the PLL and determine PLL output clock frequency.

Table 10-14 PLL N-Counter Selection

REG[32h] bits 3-0	N-Counter (N)
0h	1
1h	2
2h	3
...	...
Dh	14
Eh	15
Fh	16

Note
The PLL output clock (f_{PLLO}) must be between 20MHz and 110MHz.

Where:
$f_{PLLI} = f_{SYSCLK} / PIR$
$f_{PLLO} = f_{PLLI} \times N$

f_{SYSCLK} = System clock (CLKI or Crystal Oscillator) frequency
f_{PLLI} = PLL input clock frequency
f_{PLLO} = PLL output clock frequency
PIR = PLL input clock divide ratio (REG[31h] bits 3-0)

REG[33h] TFT PLL Setting Register 2
Address = 8033h Default = 24h Read/Write

Reserved	PLL V-Divider bits 1-0		PLL VC bits 4-0				
7	6	5	4	3	2	1	0

bit 7 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

bits 6-5 PLL V-Divider bits [1:0]

These bits specify the V-Divider value used for configuring the PLL and determine VCO clock frequency.

Table 10-15 PLL V-Divider Selection

REG[33h] bits 6-5	V-Divider (V)
00	Reserved
01	2
10	4
11	8

Note

The VCO clock frequency (f_{VCO}) must be between 100MHz and 400MHz.

Where:

$f_{PLLI} = f_{SYSCLK} / PIR$
$f_{PLLO} = f_{PLLI} \times N$
$f_{VCO} = f_{PLLO} \times V$

f_{SYSCLK} = System clock (CLKI or Crystal Oscillator) frequency
f_{PLLI} = PLL input clock frequency
f_{PLLO} = PLL output clock frequency
f_{VCO} = VCO clock frequency
PIR = PLL input clock divide ratio (REG[31h] bits 3-0)
N = N-Counter (REG[32h] bits 3-0)

bits 4-0 PLL VC bits [4:0]

These bits specify the VC value used for configuring the PLL and are set according to the VCO clock frequency.

Table 10-16 PLL VC Selection

VCO Clock Frequency (f_{VCO})	REG[33h] bits 4-0 (VC)
$100M \le f_{VCO} < 110MHz$	1h
$110M \le f_{VCO} < 145MHz$	2h
$145M \le f_{VCO} < 180MHz$	3h
$180M \le f_{VCO} < 215MHz$	4h
$215M \le f_{VCO} < 250MHz$	5h
$250M \le f_{VCO} < 285MHz$	6h
$285M \le f_{VCO} < 320MHz$	7h
$320M \le f_{VCO} < 350MHz$	9h
$350M \le f_{VCO} < 375MHz$	Bh
$375M \le f_{VCO} < 400MHz$	Ch

TFT-IF SET 1

The TFT-IF SET 1 command is used to configure the TFT interface. The value of REG[34h] is passed as parameters when the TFT-IF SET 1 command is issued. For further information on the TFT-IF SET 1 command, see Section 11.1.15, “TFT-IF SET 1” on page 116.

REG[34h] TFT Interface Configuration Register
Address = 8034h Default = 24h Read/Write

FPFRAME Polarity Select	FPLINE Polarity Select	FPDRDY Polarity Select	FPSHIFT Polarity Select	Reserved	TFT Up-Scaler Method Select	TFT Color Mode Select	TFT Interface Enable
7	6	5	4	3	2	1	0

bit 7 FPFRAME Polarity Select
This bit selects the FPFRAME polarity.
When this bit = 0b, the FPFRAME is active low (default).
When this bit = 1b, the FPFRAME is active high.

bit 6 FPLINE Polarity Select
This bit selects the FPLINE polarity.
When this bit = 0b, the FPLINE is active low (default).
When this bit = 1b, the FPLINE is active high.

bit 5 FPDRDY Polarity Select
This bit selects the FPDRDY polarity.
When this bit = 0b, the FPDRDY is active low.
When this bit = 1b, the FPDRDY is active high. (default)

bit 4 FPSHIFT Polarity Select
This bit selects the FPSHIFT polarity.
When this bit = 0b, FPDAT[5:0], FPFRAME, FPLINE and FPDRDY change at the falling edge of FPSHIFT (default).
When this bit = 1b, FPDAT[5:0], FPFRAME, FPLINE and FPDRDY change at the rising edge of FPSHIFT.

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value this bit is 0b.

bit 2 TFT Up-Scaler Method Select.
This bit selects the TFT up-scaler method.
When this bit = 0b, the bilinear method is selected.
When this bit = 1b, the nearest neighbor method is selected. (default)

Note
When the Bit-Per-Pixel is 1bpp or 2bpp, the nearest neighbor method is recommended.
When the Bit-Per-Pixel is 4bpp, the bilinear method is recommended.

bit 1 TFT Color Mode Select
This bit selects the TFT color mode.
When this bit = 0b, the Gray Scale Mode is selected.
When this bit = 1b, the Color Palette Mode is selected.

Table 10-17 Gray Scale Mode (REG[34h] bit1 = 0)

Bit-Per-Pixel (REG[20h] bits 1-0)	Pixel Data	FPDAT[3:0] (FPDAT[5:4] are not used)
1 bpp	0	LLLL
	1	HHHH
2 bpp	00	LLLL
	01	LHLH
	10	HLHL
	11	HHHH
4 bpp	0000	LLLL
	0001	LLLH
	0010	LLHL
	0011	LLHH
	:	:
	1101	HHLH
	1110	HHHL
	1111	HHHH

Note

For information of the FPDAT pin connection, see Section Figure 3-6, “S1D13709 to TFT-LCD Example (Gray Scale Mode, REG[34h]bit1 = 0)” on page 13.

Table 10-18 Color Palette Mode (REG[34h] bit1 = 1)

Bit-Per-Pixel (REG[20h] bits 1-0)	Pixel Data	FPDAT[5:0]
1 bpp	0	REG[63h] bits 5-0
	1	REG[64h] bits 5-0
2 bpp	00	REG[63h] bits 5-0
	01	REG[64h] bits 5-0
	10	REG[65h] bits 5-0
	11	REG[66h] bits 5-0

Table 10-18 Color Palette Mode (REG[34h] bit1 = 1)

Bit-Per-Pixel (REG[20h] bits 1-0)	Pixel Data	FPDAT[5:0]
4 bpp	0000	REG[63h] bits 5-0
	0001	REG[64h] bits 5-0
	0010	REG[65h] bits 5-0
	0011	REG[66h] bits 5-0
	0100	REG[67h] bits 5-0
	0101	REG[68h] bits 5-0
	0110	REG[69h] bits 5-0
	0111	REG[6Ah] bits 5-0
	1000	REG[6Bh] bits 5-0
	1001	REG[6Ch] bits 5-0
	1010	REG[6Dh] bits 5-0
	1011	REG[6Eh] bits 5-0
	1100	REG[6Fh] bits 5-0
	1101	REG[70h] bits 5-0
	1110	REG[71h] bits 5-0
	1111	REG[72h] bits 5-0

Note

For information of the FPDAT pin connection, see Section Figure 3-7, “S1D13709 to TFT-LCD Example (Color Palette Mode, REG[34h]bit1 = 1)” on page 13.

bit 0 TFT Interface Enable
This bit enables the TFT interface.
When this bit = 0b, the TFT-LCD interface is disabled. (STN-LCD is enabled.)
When this bit = 1b, the TFT-LCD interface is enabled.

TFT-IF SET 2

The TFT-IF SET 2 command is used to configure the TFT interface. The values from REG[34h] through REG[4Ah] are passed as parameters when the TFT-IF SET 2 command is issued. For further information on the TFT-IF SET 2 command, see Section 11.1.16, “TFT-IF SET 2” on page 117.

REG[35h] TFT Horizontal Total Period Register 0
Address = 8035h Default = 97h Read/Write

7	6	5	4	3	2	1	0
TFT Horizontal Total Period bits 7-0							

REG[36h] TFT Horizontal Total Period Register 1
Address = 8036h Default = 01h Read/Write

7	6	5	4	3	2	1	0
n/a				Reserved	TFT Horizontal Total Period bits 10-8		

REG[35h] bits 7-0

REG[36h] bits 2-0 TFT Horizontal Total Period bits 10-0
These bits specify the Horizontal Total (HT), or FPLINE period for the TFT interface, in pixels. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.
{REG[36h] bits 2-0, REG[35h] bits 7-0} = [HT] in pixels - 1

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[37h] TFT Horizontal Display Period Register 0
Address = 8037h Default = 3Fh Read/Write

TFT Horizontal Display Period bits 7-0							
7	6	5	4	3	2	1	0

REG[38h] TFT Horizontal Display Period Register 1
Address = 8038h Default = 01h Read/Write

n/a				Reserved	TFT Horizontal Display Period bits 10-8		
7	6	5	4	3	2	1	0

REG[37h] bits 7-0

REG[38h] bits 2-0 TFT Horizontal Display Period bits 10-0
These bits specify the Horizontal Display Period (HDP) for the TFT interface, in pixels. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.
{REG[38h] bits 2-0, REG[37h] bits 7-0} = [HDP] in pixels - 1

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[39h] TFT Horizontal Display Period Start Position Register 0
Address = 8039h Default = 46h Read/Write

TFT Horizontal Display Period Start Position bits 7-0							
7	6	5	4	3	2	1	0

REG[3Ah] TFT Horizontal Display Period Start Position Register 1
Address = 803Ah Default = 00h Read/Write

n/a				Reserved	TFT Horizontal Display Period Start Position bits 10-8		
7	6	5	4	3	2	1	0

REG[39h] bits 7-0

REG[3Ah] bits 2-0 TFT Horizontal Display Period Start Position bits 10-0
These bits specify the Horizontal Display Period Start Position (HDPS) for the TFT interface, in pixels. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.
{REG[3Ah] bits 2-0, REG[39h] bits 7-0} = [HDPS] in pixels

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[3Bh] TFT Vertical Total Period Register 0							
Address = 803Bh Default = 07h							Read/Write
TFT Vertical Total Period bits 7-0							
7	6	5	4	3	2	1	0

REG[3Ch] TFT Vertical Total Period Register 1							
Address = 803Ch Default = 01h							Read/Write
n/a				Reserved	TFT Vertical Total Period bits 10-8		
7	6	5	4	3	2	1	0

REG[3Bh] bits 7-0

REG[3Ch] bits 2-0 TFT Vertical Total Period bits 10-0
These bits specify the Vertical Total (VT), or FPFRAME period for the TFT interface, in lines. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.
{REG[3Ch] bits 2-0, REG[3Bh] bits 7-0} = [VT] in lines - 1

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[3Dh] TFT Vertical Display Period Register 0							
Address = 803Dh Default = EFh							Read/Write
TFT Vertical Display Period bits 7-0							
7	6	5	4	3	2	1	0

REG[3Eh] TFT Vertical Display Period Register 1							
Address = 803Eh Default = 00h							Read/Write
n/a				Reserved	TFT Vertical Display Period bits 10-8		
7	6	5	4	3	2	1	0

REG[3Dh] bits 7-0

REG[3Eh] bits 2-0 TFT Vertical Display Period bits 10-0
These bits specify the Vertical Display Period (VDP) for the TFT interface, in lines. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.
{REG[3Eh] bits 2-0, REG[3Dh] bits 7-0} = [VDP] in lines - 1

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[3Fh] TFT Vertical Display Period Start Position Register 0							
Address = 803Fh Default = 0Dh							Read/Write
TFT Vertical Display Period Start Position bits 7-0							
7	6	5	4	3	2	1	0

REG[40h] TFT Vertical Display Period Start Position Register 1							
Address = 8040h Default = 00h							Read/Write
n/a				Reserved	TFT Vertical Display Period Start Position bits 10-8		
7	6	5	4	3	2	1	0

REG[3Fh] bits 7-0

REG[40h] bits 2-0 TFT Vertical Display Period Start Position bits 10-0
These bits specify the Vertical Display Period Start Position (VDPS) for the TFT interface, in lines. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.

{REG[40h] bits 2-0, REG[3Fh] bits 7-0} = [VDPS] in lines

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[41h] TFT FPFRAME Pulse Width Register
Address = 8041h Default = 02h Read/Write

TFT FPFRAME Pulse Width bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 TFT FPFRAME Pulse Width bits 7-0
These bits specify the width of the vertical pulse signal (VPW) for the TFT interface, in lines. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.

REG[41h] bits 7-0 = [VPW] in lines - 1

REG[42h] TFT FPLINE Pulse Width Register
Address = 8042h Default = 07h Read/Write

TFT FPLINE Pulse Width bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 TFT FPLINE Pulse Width bits 7-0
These bits specify the width of the horizontal pulse signal (HPW) for the TFT interface, in pixels. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.

REG[42h] bits 7-0 = [HPW] in pixels - 1

REG[43h] TFT FPLINE Pulse Position Register 0
Address = 8043h Default = 00h Read/Write

TFT FPLINE Pulse Position bits 7-0							
7	6	5	4	3	2	1	0

REG[44h] TFT FPLINE Pulse Position Register 1
Address = 8044h Default = 00h Read/Write

n/a				Reserved	TFT FPLINE Pulse Position bits 10-8		
7	6	5	4	3	2	1	0

REG[43h] bits 7-0

REG[44h] bits 2-0 TFT FPLINE Pulse Position bits 10-0
These bits specify the start position of the FPLINE pulse (HPP) for the TFT interface, in pixels. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.

{REG[44h] bits 2-0, REG[43h] bits 7-0} = [HPP] in pixels

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[45h] TFT Horizontal Scale Ratio Register 0
Address = 8045h Default = 00h Read/Write

TFT Horizontal Scale Ratio bits 7-0							
7	6	5	4	3	2	1	0

REG[46h] TFT Horizontal Scale Ratio Register 1
Address = 8046h Default = 04h Read/Write

n/a				Reserved	TFT Horizontal Scale Ratio bits 10-8		
7	6	5	4	3	2	1	0

REG[45h] bits 7-0

REG[46h] bits 2-0 TFT Horizontal Scale Ratio bits 10-0
These bits determine the horizontal scaling factor (HSR) for the Up-scalar and must be programmed based on the following formula.

{REG[46h] bits 2-0, REG[45h] bits 7-0} = 1024 x (1 ÷ [HSR])

Example: For a scaling ratio of x3.51, REG[45h] and REG[46h] should be programmed as follows.

{REG[46h] bits 2-0, REG[45h] bits 7-0}
= 1024 x (1 ÷ [HSR])
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

bit 3 Reserved
This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[47h] TFT Vertical Scale Ratio Register 0
Address = 8047h Default = 00h Read/Write

TFT Vertical Scale bits 7-0							
7	6	5	4	3	2	1	0

REG[48h] TFT Vertical Scale Ratio Register 1
Address = 8048h Default = 04h Read/Write

n/a				Reserved	TFT Vertical Scale Ratio bits 10-8		
7	6	5	4	3	2	1	0

REG[47h] bits 7-0

REG[48h] bits 2-0 TFT Vertical Scale Ratio bits 10-0

These bits determine the vertical scaling factor (VSR) for the Up-scalar and must be programmed based on the following formula.

{REG[48h] bits 2-0, REG[47h] bits 7-0} = 1024 x (1 ÷ [VSR])

Example: For a scaling ratio of x3.51, REG[47h] and REG[48h] should be programmed as follows.

{REG[48h] bits 2-0, REG[47h] bits 7-0}
= 1024 x (1 ÷ [VSR])
= 1024 x (1 ÷ 3.51)
= 291 (round down)
= 123h

bit 3 Reserved

This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

REG[49h] TFT Horizontal Display Offset Register 0

Address = 8049h Default = 00h Read/Write

TFT Horizontal Display Offset bits 7-0							
7	6	5	4	3	2	1	0

REG[4Ah] TFT Horizontal Display Offset Register 1

Address = 804Ah Default = 00h Read/Write

n/a				Reserved	TFT Horizontal Display Offset bits 10-8		
7	6	5	4	3	2	1	0

REG[49h] bits 7-0

REG[4Ah] bits 2-0 TFT Horizontal Display Offset bits 10-0

These bits specify the Horizontal Display Offset (HDO) for the TFT interface, in pixels. For further information, see Section 7.6.2, “TFT-LCD Interface Timing” on page 57.

{REG[4Ah] bits 2-0, REG[49h] bits 7-0} = [HDO] in pixels - 1

bit 3 Reserved

This bit is Reserved and must not be changed from the default value. The default value for this bit is 0b.

HDOT SCR SYNC

The HDOT SCR SYNC command is used to control update timing of the horizontal pixel scroll. The value of REG[4Bh] is passed as parameters when the HDOT SCR SYNC command is issued. For further information on the HDOT SCR SYNC command, see Section 11.1.17, “HDOT SCR SYNC” on page 118.

REG[4Bh] Horizontal Pixel Scroll Frame Sync Enable Register

Address = 804Bh Default = 00h Read/Write

Horizontal Pixel Scroll Frame Sync Enable	Reserved						
7	6	5	4	3	2	1	0

bit 7 — Horizontal Pixel Scroll Frame Sync Enable
This bit selects reflect timing of Horizontal Pixel Scroll bits (REG[1Bh] bits 2-0).
When this bit = 0b, the updated Horizontal Pixel Scroll bits (REG[1Bh] bits 2-0) are reflected to the display function immediately.
When this bit = 1b, the updated Horizontal Pixel Scroll bits (REG[1Bh] bits 2-0) are reflected to the display function synchronized with FPFRAME pulse.

bit 6-0 — Reserved
These bits are Reserved and must not be changed from the default value. The default value for these bits is 000000b.

REG[53h] is Reserved

This register is Reserved and must not be changed from the default value. The default value for this register is 00h.

PALETTE

The PALETTE command is used to set color palette for the TFT interface. The values from REG[63h] through REG[72h] are passed as parameters when the PALETTE command is issued. For further information on the PALETTE command, see Section 11.1.18, “PALETTE” on page 118.

REG[63h] TFT Color Palette 0 Register
Address = 8063h Default = 00h Read/Write

n/a		TFT Color Palette 0 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 — TFT Color Palette 0 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[64h] TFT Color Palette 1 Register
Address = 8064h Default = 03h Read/Write

n/a		TFT Color Palette 1 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 — TFT Color Palette 1 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[65h] TFT Color Palette 2 Register
Address = 8065h Default = 0Ch Read/Write

n/a		TFT Color Palette 2 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 2 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[66h] TFT Color Palette 3 Register
Address = 8066h Default = 30h Read/Write

n/a		TFT Color Palette 3 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 3 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[67h] TFT Color Palette 4 Register
Address = 8067h Default = 0Fh Read/Write

n/a		TFT Color Palette 4 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 4 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[68h] TFT Color Palette 5 Register
Address = 8068h Default = 3Ch Read/Write

n/a		TFT Color Palette 5 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 5 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[69h] TFT Color Palette 6 Register
Address = 8069h Default = 33h Read/Write

n/a		TFT Color Palette 6 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 6 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[6Ah] TFT Color Palette 7 Register
Address = 806Ah Default = 01h Read/Write

n/a		TFT Color Palette 7 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 7 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[6Bh] TFT Color Palette 8 Register
Address = 806Bh Default = 04h Read/Write

n/a		TFT Color Palette 8 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 8 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[6Ch] TFT Color Palette 9 Register
Address = 806Ch Default = 10h Read/Write

n/a		TFT Color Palette 9 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 9 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[6Dh] TFT Color Palette 10 Register
Address = 806Dh Default = 05h Read/Write

n/a		TFT Color Palette 10 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 10 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[6Eh] TFT Color Palette 11 Register
Address = 806Eh Default = 14h Read/Write

n/a		TFT Color Palette 11 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 11 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[6Fh] TFT Color Palette 12 Register
Address = 806Fh Default = 11h Read/Write

n/a		TFT Color Palette 12 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 12 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[70h] TFT Color Palette 13 Register Address = 8070h Default = 15h Read/Write							
n/a		TFT Color Palette 13 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 13 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[71h] TFT Color Palette 14 Register Address = 8071h Default = 17h Read/Write							
n/a		TFT Color Palette 14 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 14 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

REG[72h] TFT Color Palette 15 Register Address = 8072h Default = 3Fh Read/Write							
n/a		TFT Color Palette 15 bits 5-0					
7	6	5	4	3	2	1	0

bits 5-0 TFT Color Palette 15 bits 5-0
These bits specify the pixel data output from FPDAT[5:0] pins. These bits are available only when TFT color palette mode is selected (REG[34h] bit 1 = 1b).

10.3.7 LCD Pin Output Drive Control Register

OUTDRIVE

The OUTDRIVE command is used to set the drive level of LCD output pin. The values of REG[73h] are passed as parameters when the OUTDRIVE command is issued. For further information on the OUTDRIVE command, see Section 11.1.19, “OUTDRIVE” on page 119.

REG[73h] LCD Pin Output Drive Control Register Address = 8073h Default = 00h Read/Write							
SYNC Output Driver Select	FPSHIFT Output Driver Select	FPDAT5 Output Driver Select	FPDAT4 Output Driver Select	FPDAT3 Output Driver Select	FPDAT2 Output Driver Select	FPDAT1 Output Driver Select	FPDAT0 Output Driver Select
7	6	5	4	3	2	1	0

bit 7 SYNC Output Drive Select
This bit determines the drive level, in mA, for the FPFRAME, FPLINE and FPDRDY pins.
When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected.
When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.

bit 6	FPSHIFT Output Drive Select This bit determines the drive level, in mA, for the FPSHIFT pin. When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected. When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.
bit 5	FPDAT5 Output Drive Select This bit determines the drive level, in mA, for the FPDAT5 pin. When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected. When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.
bit 4	FPDAT4 Output Drive Select This bit determines the drive level, in mA, for the FPDAT4 pin. When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected. When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.
bit 3	FPDAT3 Output Drive Select This bit determines the drive level, in mA, for the FPDAT3 pin. When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected. When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.
bit 2	FPDAT2 Output Drive Select This bit determines the drive level, in mA, for the FPDAT2 pin. When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected. When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.
bit 1	FPDAT1 Output Drive Select This bit determines the drive level, in mA, for the FPDAT1 pin. When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected. When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.
bit 0	FPDAT0 Output Drive Select This bit determines the drive level, in mA, for the FPDAT0 pin. When this bit = 0b, the 2mA@3.3V(3mA@5V) Type-1 driver is selected. When this bit = 1b, the 6mA@3.3V (8mA@5V) Type-2 driver is selected.

11 Indirect Addressing

Table 11-1 Indirect Addressing Command Set

Class	Direct Interface Address	Command	Register Description	Control Byte Value	No. of Bytes
System Control	8000h - 8007h	SYSTEM SET	Initializes device and display	40h	8
	8008h	POWER SAVE	Enters standby mode	53h	0
Display Control	8009h - 800A	DISP ON/OFF	Enables/disables display and display attributes	58h 59h	1
	800Bh - 8014h	SCROLL	Sets screen block start addresses and sizes	44h	10
	8015h - 8016h	CSRFORM	Sets cursor type	5Dh	2
	8017h	CSRDIR	Sets direction of cursor movement	4Ch - 4Fh	0
	8018h	OVLAY	Sets display overlay format	5Bh	1
	8019h - 801Ah	CGRAM ADR	Sets start address of character generator RAM	5Ch	2
	801Bh	HDOT SCR	Sets horizontal scroll position	5A	1
Drawing Control	801Ch - 801Dh	CSRW	Sets cursor address	46h	2
	801Eh - 801Fh	CSRR	Reads cursor address	47h	2
Display Control	8020h	GRAYSCALE	Sets the Grayscale depth (bpp)	60h	1
System Control	8000h - 8007h	SYSTEM SET	Initializes device and display	40h	8
	8008h	POWER SAVE	Enters standby mode	53h	0
ID	8030h	ID	Reads ID	61h	0
TFT-IF Control	8031h - 8033h	PLL SET	Initializes PLL	62h	3
	8034h	TFT-IF SET 1	Initializes TFT Interface	63h	1
	8035h - 804Ah	TFT-IF SET 2	Initializes TFT Interface	64h	22
Scroll Option	804Bh	HDOT SCR SYNC	Sets scroll option	65h	1
Color Palette	8063h - 8072h	PALETTE	Sets color palette	67h	16
Pin Drive	8073h	OUTDRIVE	Sets output pin drive	68h	1
Memory Control	0000h - 7FFFh	MEMWRITE	Writes to memory	42h	n/a
		MEMREAD	Reads from memory	43h	

Table 11-2 Generic Indirect Addressing Command/Write/Read

A0	$\overline{WR}$	$\overline{RD}$	
1	0	1	Command write
1	1	0	Display data and cursor address read
0	0	1	Display data and parameter write

Table 11-3 M6800 Indirect Addressing Command/Write/Read

A0	R/$\overline{W}$	E	
1	0	1	Command write
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write

Table 11-4 M68K Indirect Addressing Command/Write/Read

A0	R/$\overline{W}$	LDS#	
1	0	0	Command write
1	1	0	Display data and cursor address read
0	0	0	Display data and parameter write

11.1 System Control

See Section 15.1.3, “Initialization Example for STN Interface” on page 151 for the initialization sequence.

11.1.1 SYSTEM SET

See “SYSTEM SET” on page 65 for further information.

Note

1. If the S1D13709 is in power save mode (at power up or after a POWER SAVE command), the SYSTEM SET command will exit power save mode. After writing the SYSTEM SET command and its 8 parameters, the S1D13709 will be in normal operation.
2. When using a crystal, after writing SYSTEM SET command wait a stability period for the crystal to allow the internal clock to become stable before writing the remaining eight parameters.

Table 11-5 SYSTEM SET Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	0	0	0	0	0	0	C	W
0	0	IV[1]	1	W/S[2]	M2[3]	0	M0[4]	P1	W
MOD[5]	0	0	0	REG[01h] bits 3-0				P2	W
0	0	0	0	REG[02h] bits 3-0				P3	W
REG[03h] bits 7-0								P4	W

Table 11-5 SYSTEM SET Command and Parameters

MSB		LSB		
	REG[04h] bits 7-0		P5	W
	REG[05h] bits 7-0		P6	W
	REG[06h] bits 7-0		P7	W
0	REG[07h] bits 6-0		P8	W

Note

[1] IV is the Screen Origin Compensation bit, REG[00h] bit 5.
[2] W/S is the Panel Drive Select bit, REG[00h] bit 3.
[3] M2 is the Character Height bit, REG[00h] bit 2.
[4] M0 is the Character Generator Select bit, REG[00h] bit 0.
[5] MOD is defined by REG[01h] bit 7.

11.1.2 POWER SAVE

See “POWER SAVE” on page 73 for further information.

Table 11-6 POWER SAVE Command

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	0	1	0	0	1	1	C	W

11.1.3 DISP ON/OFF

The following parameters are used for the DISP ON command. For further details, see DISP ON/OFF on page 74.

Table 11-7 DISP ON Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	0	1	1	0	0	1	C	W
REG[0Ah] bits 7-0								P1	W

The following parameters are used for the DISP OFF command. For further details, see DISP ON/OFF on page 74.

Table 11-8 DISP OFF Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	0	1	1	0	0	0	C	W
REG[0Ah] bits 7-0								P1	W

11.1.4 SCROLL

See “SCROLL” on page 76 for further information.

Table 11-9 SCROLL Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Command/ Parameter	Write/ Read
0	1	0	0	0	1	0	0		C	W
A7	A6	A5	A4	A3	A2	A1	A0	REG[0Bh] bits 7-0	P1	W
IUE	A14	A13	A12	A11	A10	A9	A8	REG[0Ch] bits 6-0	P2	W
L7	L6	L5	L4	L3	L2	L1	L0	REG[0Dh] bits 7-0	P3	W
A7	A6	A5	A4	A3	A2	A1	A0	REG[0Eh] bits 7-0	P4	W
IUE	A14	A13	A12	A11	A10	A9	A8	REG[0Fh] bits 6-0	P5	W
L7	L6	L5	L4	L3	L2	L1	L0	REG[10h] bits 7-0	P6	W
A7	A6	A5	A4	A3	A2	A1	A0	REG[11h] bits 7-0	P7	W
IUE	A14	A13	A12	A11	A10	A9	A8	REG[12h] bits 6-0	P8	W
A7	A6	A5	A4	A3	A2	A1	A0	REG[13h] bits 7-0	P9	W
IUE	A14	A13	A12	A11	A10	A9	A8	REG[14h] bits 6-0	P10	W

Note

Set parameters P9 and P10 only if both dual panel (REG[00h] bit 3 = 1) and two-layer configuration are selected. SAD4 is the fourth screen block display start address.

11.1.5 CSRFORM

See “CSRFORM” on page 81 for further information.

Table 11-10 CSRFORM Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Command/ Parameter	Write/ Read
0	1	0	1	1	1	0	1	C	W
0	0	0	0	REG[15h] bits 3-0 X3	X2	X1	X0	P1	W
CM[1]	0	0	0	REG[16h] bits 3-0 Y3	Y2	Y1	Y0	P2	W

Note
[1] CM is the Cursor Mode bit, REG[16h] bit 7.

11.1.6 CSRDIR

See “CSRDIR” on page 83 for further information.

Table 11-11 CSRDIR Command

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Command/ Parameter	Write/ Read
0	1	0	0	1	1	REG[17h] bits 1-0 CD1	CD0	C	W

11.1.7 OVLAY

See “OVLAY” on page 84 for further information.

Table 11-12 OVLAY Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Command/ Parameter	Write/ Read
0	1	0	1	1	0	1	1	C	W
0	0	0	OV[1]	DM2[2]	DM1[2]	MX1[3]	MX0[3]	P1	W

Note
[1] OV is the 3 Layer Overlay Select bit, REG[18h] bit 4.
[2] DM2 and DM1 are the Screen Block 3/1 Display Mode bits, REG[18h] bits 3-2.
[3] MX1 and MX0 are the Layer Composition Method bits, REG[18h] bits 1-0.

11.1.8 CGRAM ADR

See “CGRAM ADR” on page 86 for further information.

Table 11-13 CGRAM ADR Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Command/ Parameter	Write/ Read
0	1	0	1	1	1	0	0		C	W
A7	A6	A5	A4	A3	A2	A1	A0	(SAGL)	P1	W
0	A14	A13	A12	A11	A10	A9	A8	(SAGH)	P2	W

11.1.9 HDOT SCR

See “HDOT SCR” on page 87 for further information.

Table 11-14 HDOT SCR Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Command/ Parameter	Write/ Read
0	1	0	1	1	0	1	0	C	W
SUE	0	0	0	0	D2	D1	D0	P1	W

11.1.10 CSRW

See “CSRW” on page 89 for further information.

Table 11-15 CSRW Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Command/ Parameter	Write/ Read
0	1	0	0	0	1	1	0		C	W
A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)	P1	W
0	A14	A13	A12	A11	A10	A9	A8	(CSRH)	P2	W

11.1.11 CSRR

See “CSRR” on page 90 for further information.

Table 11-16 CSRR Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0		Command/ Parameter	Write/ Read
0	1	0	0	0	1	1	1		C	W
A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)	P1	R
0	A14	A13	A12	A11	A10	A9	A8	(CSRH)	P2	R

11.1.12 GRAYSCALE

See “GRAYSCALE” on page 91 for further information.

Table 11-17 Gray Scale Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Command/ Parameter	Write/ Read
0	1	1	0	0	0	0	0	C	W
0	0	0	0	0	0	BPP1	BPP0	P1	W

11.1.13 ID

See “ID” on page 92 for further information.

Table 11-18 ID Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Command/ Parameter	Write/ Read
0	1	1	0	0	0	0	1	C	W
0	1	0	1	1	0	0	1	P1	R

11.1.14 PLL SET

See “PLL SET” on page 92 for further information.

Table 11-19 PLL SET Command and Parameters

MSB bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB bit 0	Command/ Parameter	Write/ Read
0	1	1	0	0	0	1	0	C	W
POR3	POR2	POR1	POR0	PIR3	PIR2	PIR1	PIR0	P1	W
RS3	RS2	RS1	RS0	N3	N2	N1	N0	P2	W
0	V1	V0	VC4	VC3	VC2	VC1	VC0	P3	W

11.1.15 TFT-IF SET 1

See “TFT-IF SET 1” on page 96 for further information.

Table 11-20 TFT-IF SET 1 Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	1	0	0	0	1	1	C	W
VP	HP	DEP	CKP	0	UMS	CME	LSEL	P1	W

11.1.16 TFT-IF SET 2

See “TFT-IF SET 2” on page 98 for further information.

Table 11-21 TFT-IF SET 2 Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	1	0	0	1	0	0	C	W
HT7	HT6	HT5	HT4	HT3	HT2	HT1	HT0	P1	W
0	0	0	0	0	HT10	HT9	HT8	P2	W
HDP7	HDP6	HDP5	HDP4	HDP3	HDP2	HDP1	HDP0	P3	W
0	0	0	0	0	HDP10	HDP9	HDP8	P4	W
HDPS7	HDPS6	HDPS5	HDPS4	HDPS3	HDPS2	HDPS1	HDPS0	P5	W
0	0	0	0	0	HDPS 10	HDPS9	HDPS8	P6	W
VT7	VT6	VT5	VT4	VT3	VT2	VT1	VT0	P7	W
0	0	0	0	0	VT10	VT9	VT8	P8	W
VDP7	VDP6	VDP5	VDP4	VDP3	VDP2	VDP1	VDP0	P9	W
0	0	0	0	0	VDP10	VDP9	VDP8	P10	W
VDPS7	VDPS6	VDPS5	VDPS4	VDPS3	VDPS2	VDPS1	VDPS0	P11	W
0	0	0	0	0	VDPS 10	VDPS9	VDPS8	P12	W
VPW7	VPW6	VPW5	VPW4	VPW3	VPW2	VPW1	VPW0	P13	W
HPW7	HPW6	HPW5	HPW4	HPW3	HPW2	HPW1	HPW0	P14	W
HPP7	HPP6	HPP5	HPP4	HPP3	HPP2	HPP1	HPP0	P15	W
0	0	0	0	0	HPP10	HPP9	HPP8	P16	W
HSR7	HSR6	HSR5	HSR4	HSR3	HSR2	HSR1	HSR0	P17	W

Table 11-21 TFT-IF SET 2 Command and Parameters

0	0	0	0	0	HSR10	HSR9	HSR8	P18	W
VSR7	VSR6	VSR5	VSR4	VSR3	VSR2	VSR1	VSR0	P19	W
0	0	0	0	0	VSR10	VSR9	VSR8	P20	W
HDO7	HDO6	HDO5	HDO4	HDO3	HDO2	HDO1	HDO0	P21	W
0	0	0	0	0	HDO10	HDO9	HDO8	P22	W

11.1.17 HDOT SCR SYNC

See “HDOT SCR SYNC” on page 103 for further information.

Table 11-22 HDOT SCR SYNC Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	1	0	0	1	0	1	C	W
SYN	0	0	0	0	0	0	0	P1	W

11.1.18 PALETTE

See “PALETTE” on page 104 for further information.

Table 11-23 PALETTE Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	1	0	0	1	1	1	C	W
0	0	PT0_5	PT0_4	PT0_3	PT0_2	PT0_1	PT0_0	P1	W
0	0	PT1_5	PT1_4	PT1_3	PT1_2	PT1_1	PT1_0	P2	W
0	0	PT2_5	PT2_4	PT2_3	PT2_2	PT2_1	PT2_0	P3	W
0	0	PT3_5	PT3_4	PT3_3	PT3_2	PT3_1	PT3_0	P4	W
0	0	PT4_5	PT4_4	PT4_3	PT4_2	PT4_1	PT4_0	P5	W
0	0	PT5_5	PT5_4	PT5_3	PT5_2	PT5_1	PT5_0	P6	W
0	0	PT6_5	PT6_4	PT6_3	PT6_2	PT6_1	PT6_0	P7	W
0	0	PT7_5	PT7_4	PT7_3	PT7_2	PT7_1	PT7_0	P8	W
0	0	PT8_5	PT8_4	PT8_3	PT8_2	PT8_1	PT8_0	P9	W

Table 11-23 PALETTE Command and Parameters

0	0	PT9_5	PT9_4	PT9_3	PT9_2	PT9_1	PT9_0	P10	W
0	0	PT10_5	PT10_4	PT10_3	PT10_2	PT10_1	PT10_0	P11	W
0	0	PT11_5	PT11_4	PT11_3	PT11_2	PT11_1	PT11_0	P12	W
0	0	PT12_5	PT12_4	PT12_3	PT12_2	PT12_1	PT12_0	P13	W
0	0	PT13_5	PT13_4	PT13_3	PT13_2	PT13_1	PT13_0	P14	W
0	0	PT14_5	PT14_4	PT14_3	PT14_2	PT14_1	PT14_0	P15	W
0	0	PT15_5	PT15_4	PT15_3	PT15_2	PT15_1	PT15_0	P16	W

11.1.19 OUTDRIVE

See “OUTDRIVE” on page 107 for further information.

Table 11-24 OUTDRIVE Command and Parameters

MSB							LSB		
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**	**Command/ Parameter**	**Write/ Read**
0	1	1	0	1	0	0	0	C	W
SYDR	CKDR	D5DR	D4DR	D3DR	D2DR	D1DR	D0DR	P1	W

11.1.20 Memory Control

See “Drawing Control Registers” on page 89 for further information.

12 Display Control Functions

12.1 Character Configuration

The origin of each character bitmap is the top left corner as shown in Figure 12-1. Adjacent bits in each byte are horizontally adjacent in the corresponding character image.

Although the size of the bitmap is fixed by the character generator, the actual displayed size of the character field can be varied in both dimensions.

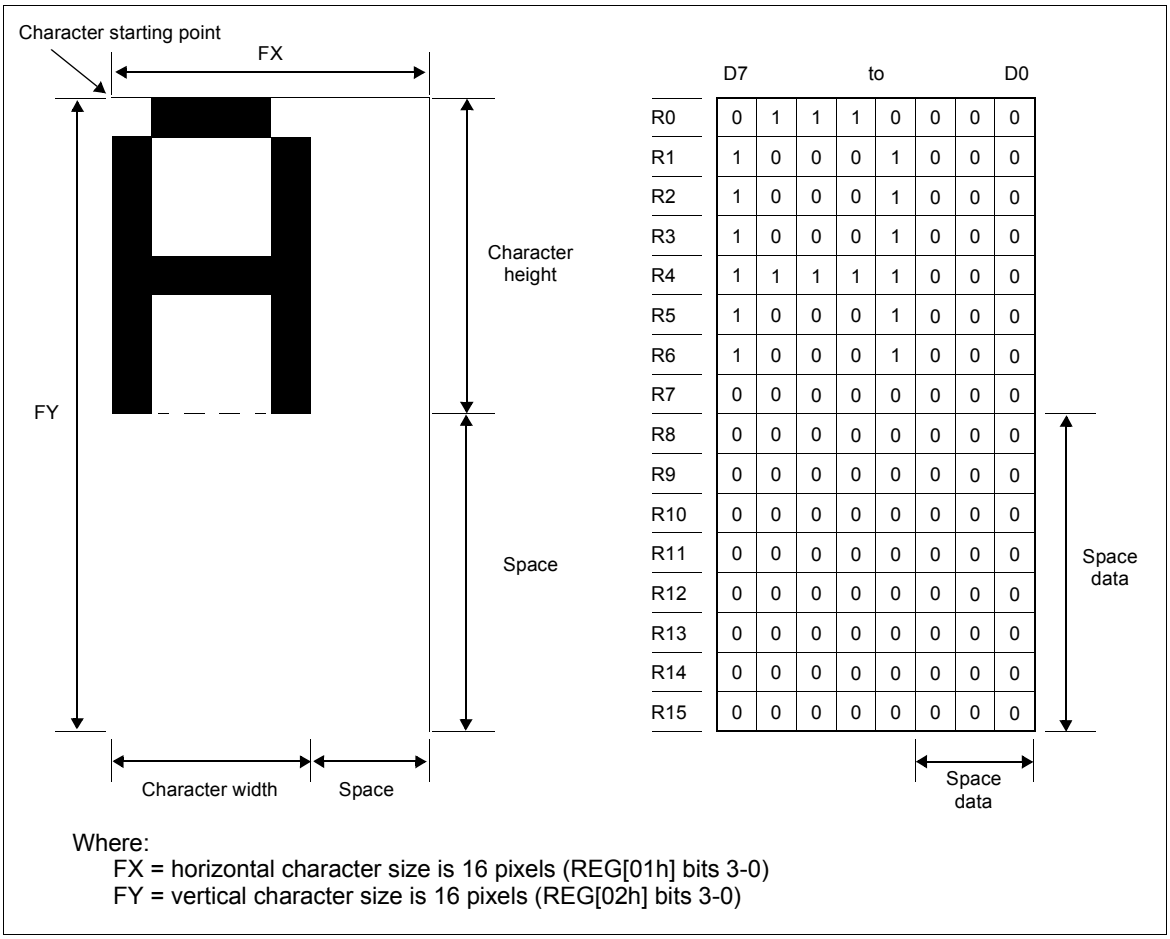


Figure 12-1 Example of Character Display from Generator Bitmap (when [FX] ≤ 8)

If the area outside the character bitmap contains only zeros, the displayed character size can be increased by increasing the horizontal character size (REG[01h] bits 3-0) and the vertical character size (REG[01h] bits 3-0). The zeros ensure that the extra space between displayed characters is blank.

The displayed character width can be set to any value up to 16 even if each horizontal row of the bitmap is two bytes wide.

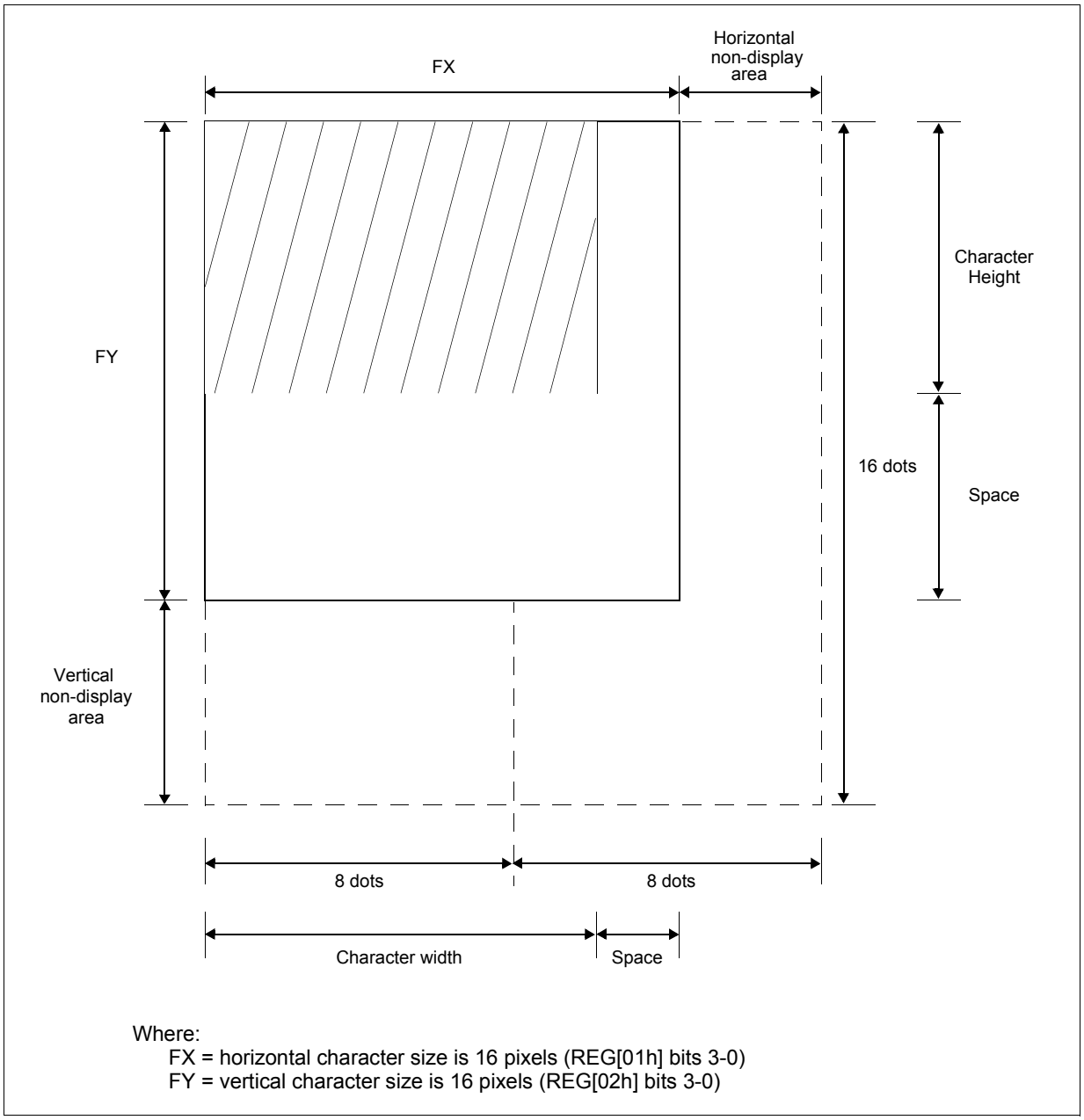


Figure 12-2 Character Width Greater than One Byte Wide ([FX] = 9)

Note

The S1D13709 does not automatically insert spaces between characters. If the displayed character size is 8 pixels or less and the space between character origins is nine pixels or more, the bitmap must use two bytes per row, even though the character image requires only one.

12.2 Screen Configuration

12.2.1 Screen Configuration

The S1D13709 can be configured for a single text screen, overlapping text screens, or overlapping graphics screens. Graphics screens use eight times as much display memory as a text screen in 1 bpp. Figure 12-3 shows the relationship between the virtual screens and the physical screen.

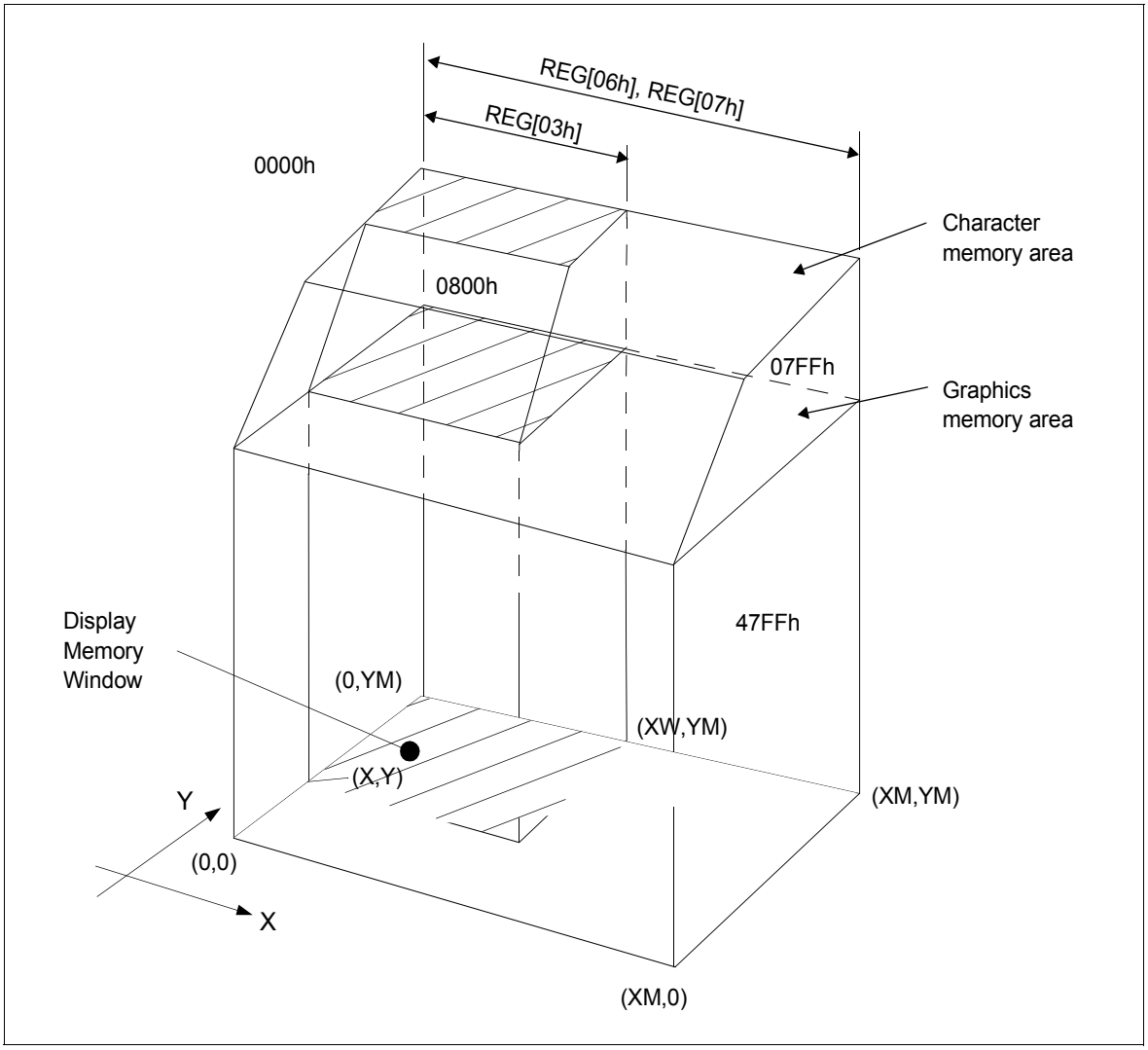
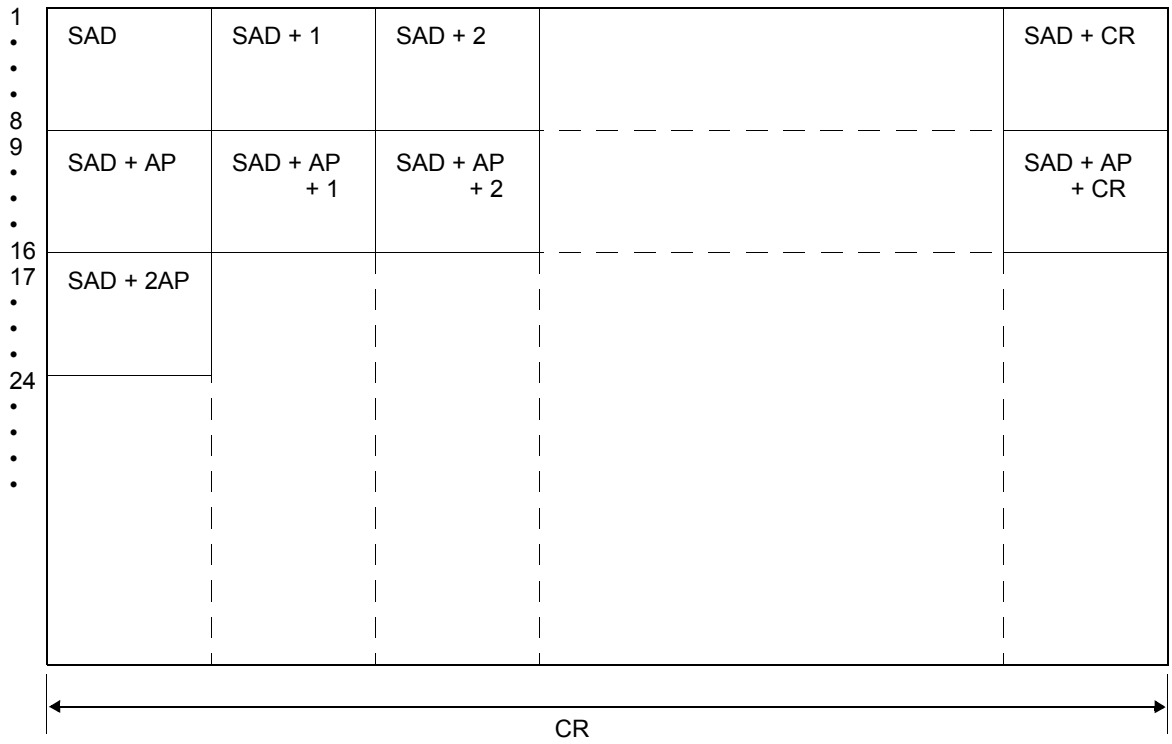


Figure 12-3 Virtual and Physical Screen Relationship

12.2.2 Display Address Scanning

The S1D13709 scans the display memory in the same way as a raster scan CRT screen. Each row is scanned from left to right until the address range equals CR, REG[03h] bits 7-0. Rows are scanned from top to bottom. When in graphics mode, at the start of each line the address counter is set to the address at the start of the previous line plus the horizontal address range (or address pitch), REG[06h] - REG[07h].

In text mode, the address counter is set to the same start address, and the same character data is read, for each row in the character bitmap. However, a new row of the character generator output is used each time. Once all the rows in the character bitmap have been displayed, the address counter is set to the start address plus the horizontal address range (or address pitch) and the next line of text is displayed.

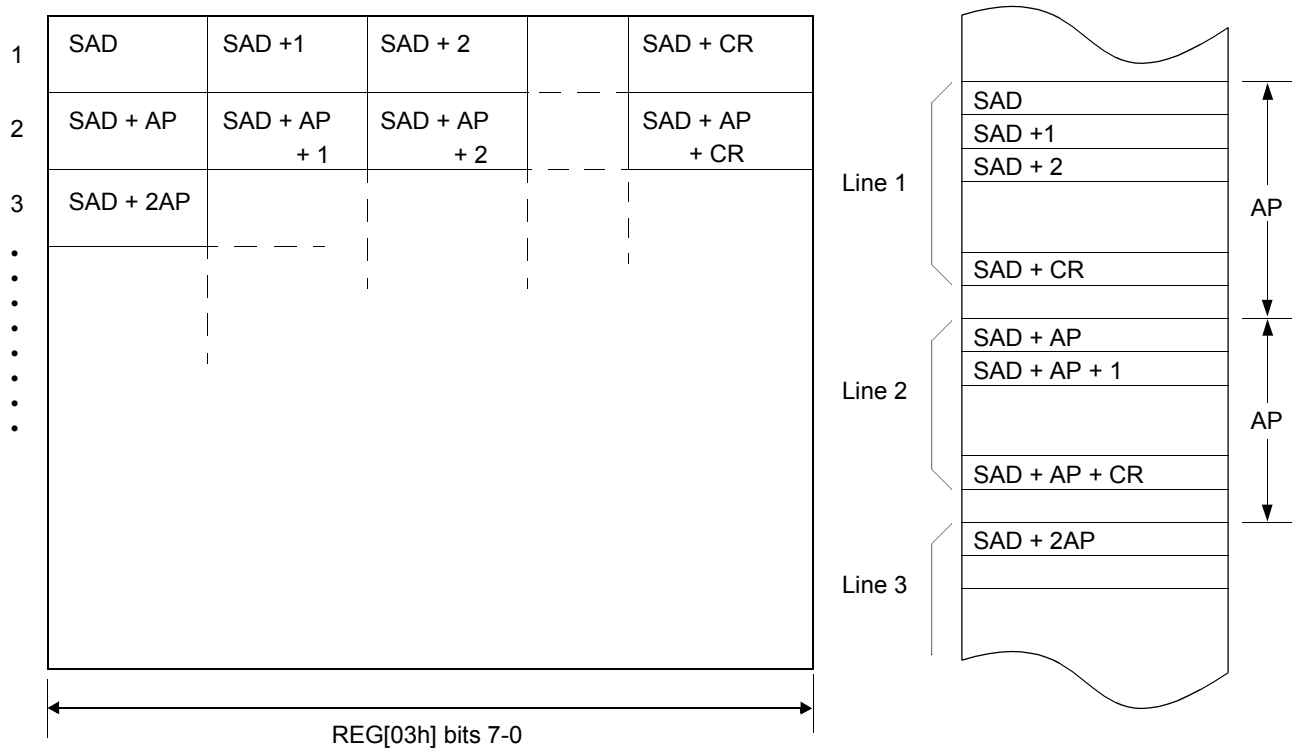


Where:
SAD = start address of the screen block
AP = horizontal address range (REG[06h], REG[07h])
CR = number of character bytes per row (REG[03h])

Note
Assumes REG[00h] bit 3 = 0, REG[01h] bits 3-0 = 8, REG[02h] bits 3-0 = 8

Figure 12-4 Display Addressing in Text Mode Example

Note
One byte of display memory corresponds to one character.



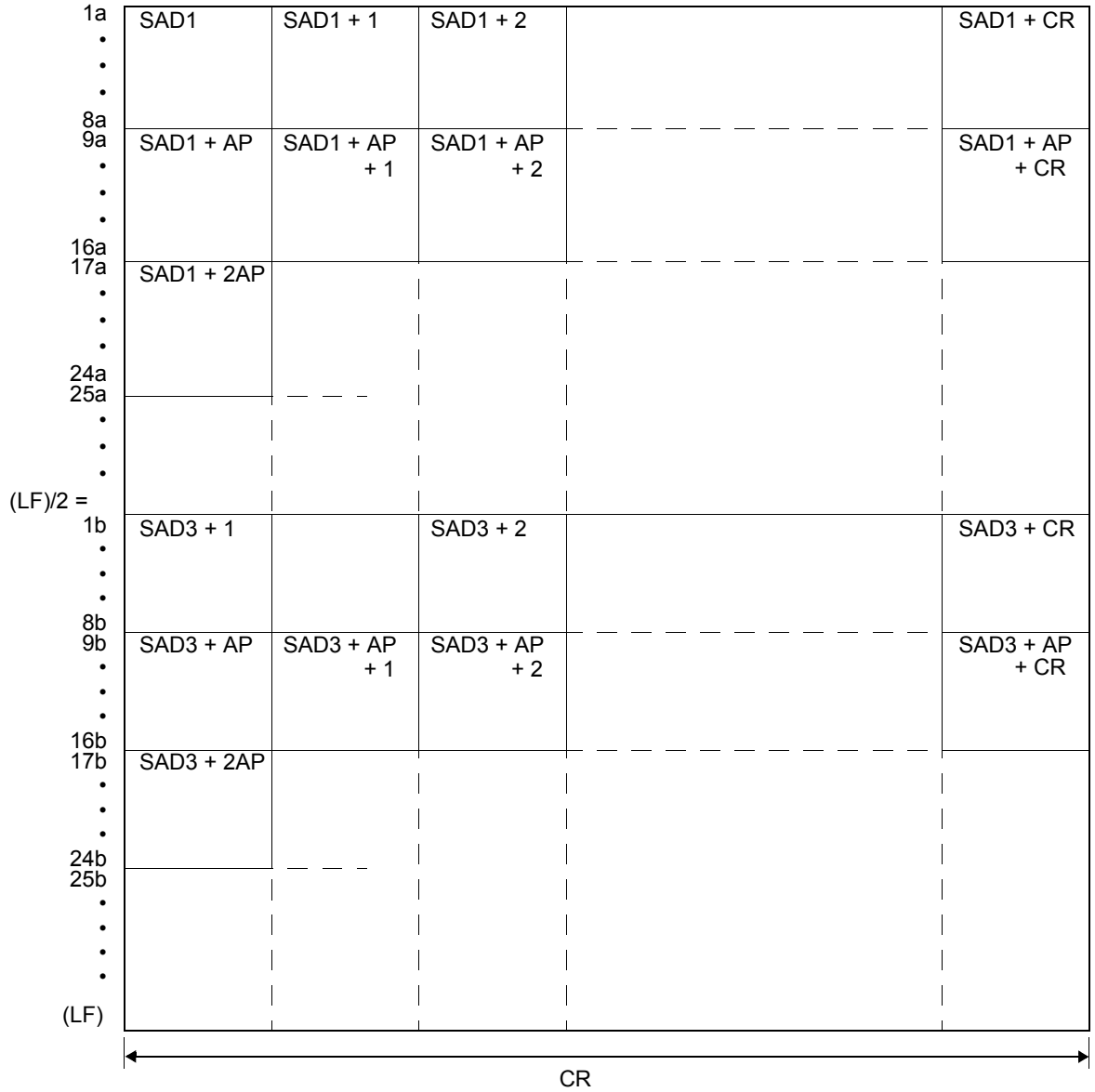
Where:
SAD = start address of the screen block
AP = horizontal address range (REG[06h], REG[07h])
CR = number of character bytes per row (REG[03h])

Note
Assumes REG[00h] bit 3 = 0, REG[01h] bits 3-0 = 8

Figure 12-5 Display Addressing in Graphics Mode Example

Note

In 1 bpp, one bit of display memory corresponds to one pixel. Therefore, 1 byte of display memory corresponds to 8 pixels. In 2 bpp, 1 byte corresponds to 4 pixels. In 4 bpp, 1 byte corresponds to 2 pixels.



Where:
- SAD = start address of the screen block
- AP = horizontal address range (REG[06h], REG[07h])
- CR = number of character bytes per row (REG[03h])
- LF = frame height in lines (REG[05h])

Note
- Assumes REG[00h] bit 3 = 0, REG[01h] bits 3-0 = 8, REG[02h] bits 3-0 = 8

Figure 12-6 Dual Panel Display Address Indexing in Text Mode

Note

In dual panel drive, the S1D13709 reads line 1a and line 1b as one cycle. The upper and lower panels are thus read alternately, one line at a time.

12.2.3 Display Scan Timing

During display scanning, the S1D13709 pauses at the end of each line for TCR - CR ((REG[04h] bits 7-0) - (REG[03h] bits 7-0)) display memory read cycles, although the LCD drive signals are still generated. TCR may be set to any value within the constraints imposed by CR, Input Clock (CLK), f_{FR}, and the size of the LCD panel. This pause may be used to fine tune the frame frequency.

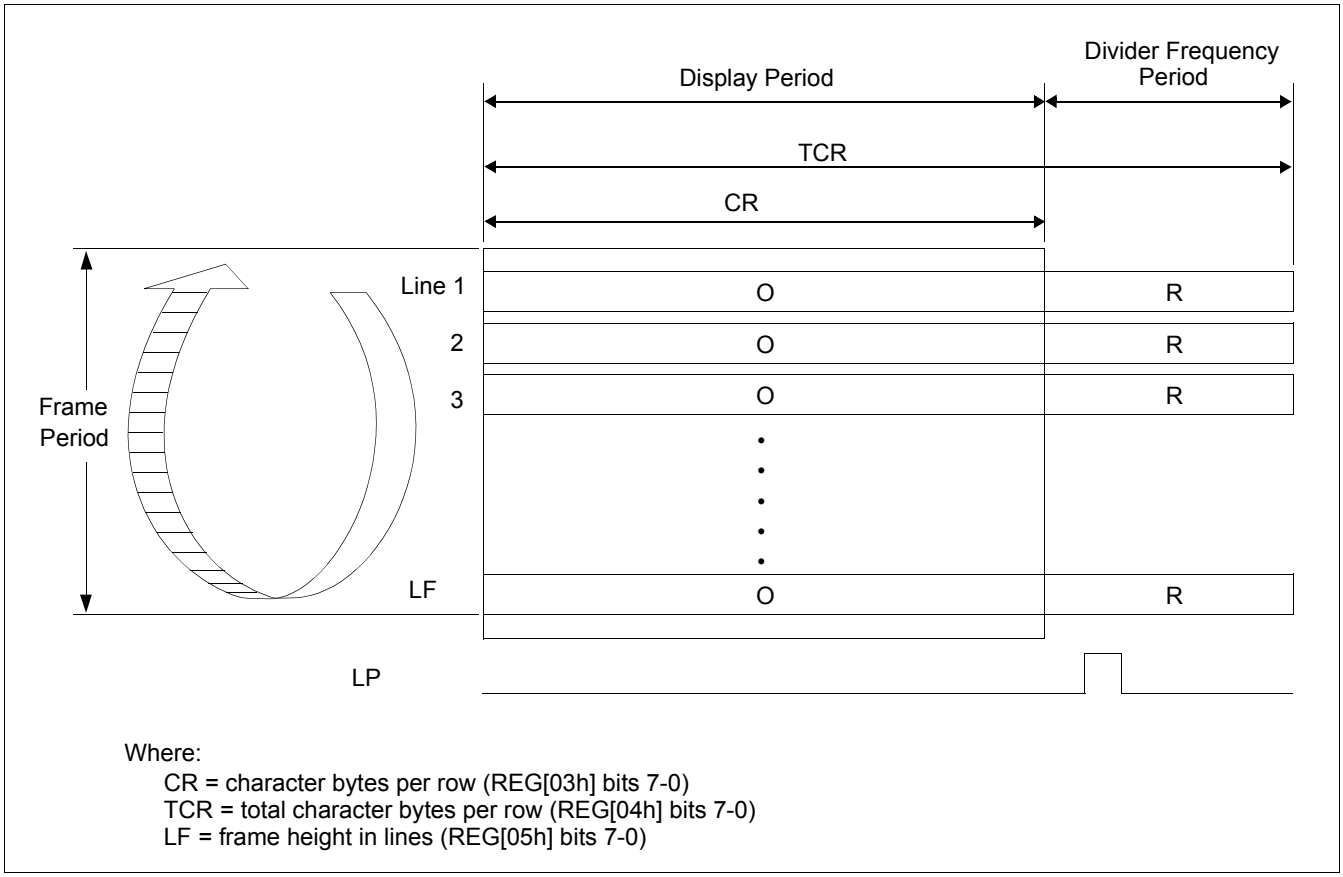


Figure 12-7 Relationship Between Total Character Bytes Per Row and Character Bytes Per Row

Note

The divider adjustment interval (R) applies to both the upper and lower screens even if a dual panel drive is selected, REG[00h] bit 3 = 1. In this case, LP is active only at the end of the lower screen's display interval.

12.2.4 TFT Interface Configuration

For the TFT interface, REG[31h] - [72h] should be set appropriately.
REG[31h]-[33h] configure the PLL to generate TFT clock (FPSHIFT) from System clock (CLKI or Crystal Oscillator). For further information, see Figure 9-1: “Clock Diagram,” on page 60.
REG[34h]-[4Ah] configure the TFT interface output timing. For further information, see Figure 7-17: “TFT-LCD Interface Timing,” on page 57.

Note

When the TFT interface is used, setting of REG[00h]-[20h] is required as well as the STN interface.

The TFT interface supports up to WVGA TFT panel using up-scaler function. The source image is defined by FX, CR and LF as well as the STN interface.

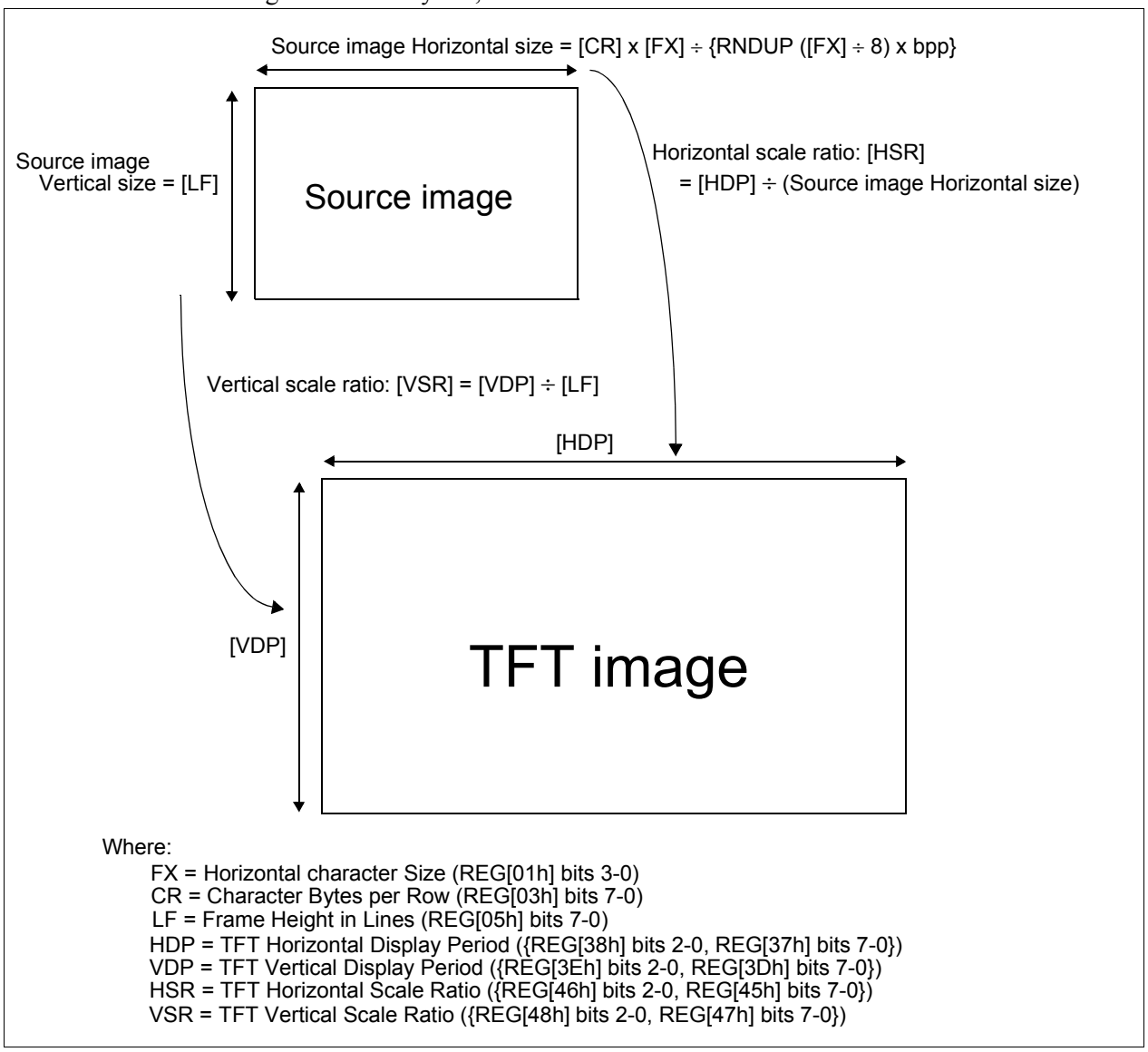


Figure 12-8 Up-Scaled TFT Image

For TFT displays, two types of color mode, Gray Scale and Color Palette mode are selectable (REG[34h] bit 1). When the Color Palette mode is used, REG[63h]-[72h] should be set appropriately. For further information, see Figure 10-17 “Gray Scale Mode (REG[34h] bit1 = 0),” on page 97 and Figure 10-18 “Color Palette Mode (REG[34h] bit1 = 1),” on page 97.

Note

The FPDAT pins connection with TFT panels is different between Gray Scale and Color Palette mode. For further information, see Figure 3-6 “S1D13709 to TFT-LCD Example (Gray Scale Mode, REG[34h]bit1 = 0),” on page 13 and Figure 3-7 “S1D13709 to TFT-LCD Example (Color Palette Mode, REG[34h]bit1 = 1),” on page 13.

12.3 Cursor Control

12.3.1 Cursor Write Register Function

The Cursor Write register (REG[1Ch] - REG[1Dh]) functions as both the displayed cursor position address register and, in indirect addressing mode, the display memory access address register. When accessing display memory outside the actual visible screen memory, the Cursor Write register should be saved before accessing the memory and then restored after the memory access is complete. This is done to prevent the cursor from visibly disappearing outside the display area.

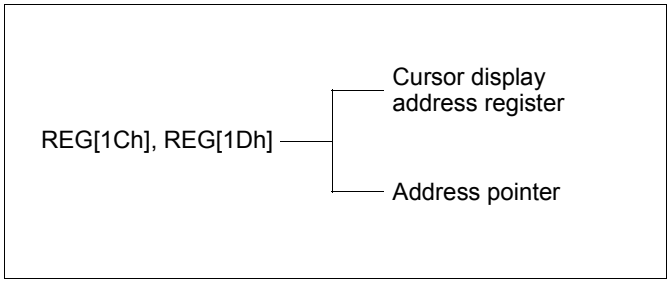


Figure 12-9 Cursor Addressing

Note

The cursor may disappear from the display if the cursor address remains outside the displayed screen memory for more than a few hundred milliseconds.

12.3.2 Cursor Movement

On each memory access, the Cursor Write register (REG[1Ch] - REG[1Dh]) is changed by the amount specified by the CSRDIR command (see REG[17h] bits 1-0) which automatically moves the cursor to the desired location.

12.3.3 Cursor Display Layers

Although the S1D13709 can display up to three layers, the cursor is displayed in only one of these layers. For a two layer configuration (REG[18h] bit 4 = 0), the cursor is displayed in the first layer (L1). For a three layer configuration (REG[18h] bit 4 = 1), the cursor is displayed in the third layer (L3).

The cursor is not displayed if the address is moved outside of the memory for its layer. If it is necessary to display the cursor in a layer other than the present one, the layers may be swapped, or the cursor layer can be moved within the display memory.

Although the cursor is normally displayed for character data, the S1D13709 may also display a dummy cursor for graphical characters. This is only possible if a graphics screen is displayed, the text screen is turned off, and the microprocessor generates the cursor control address.

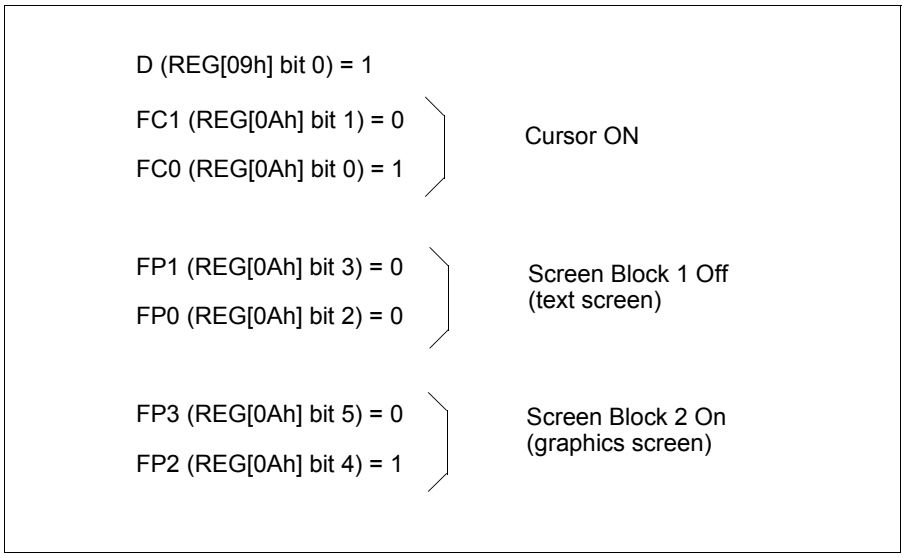


Figure 12-10 Cursor Display Layers

For example, if Chinese characters are displayed on a graphics screen, the cursor address is set to the second screen block in order to write the “graphics” display data. However, the cursor is not displayed. To display the cursor, the cursor address must be set to an address within the blank text screen block.

Since the automatic cursor increment is in address units, not character units, the controlling microprocessor must set the Cursor Write register (REG[1Ch] - REG[1Dh]) when moving the cursor over the graphical characters.

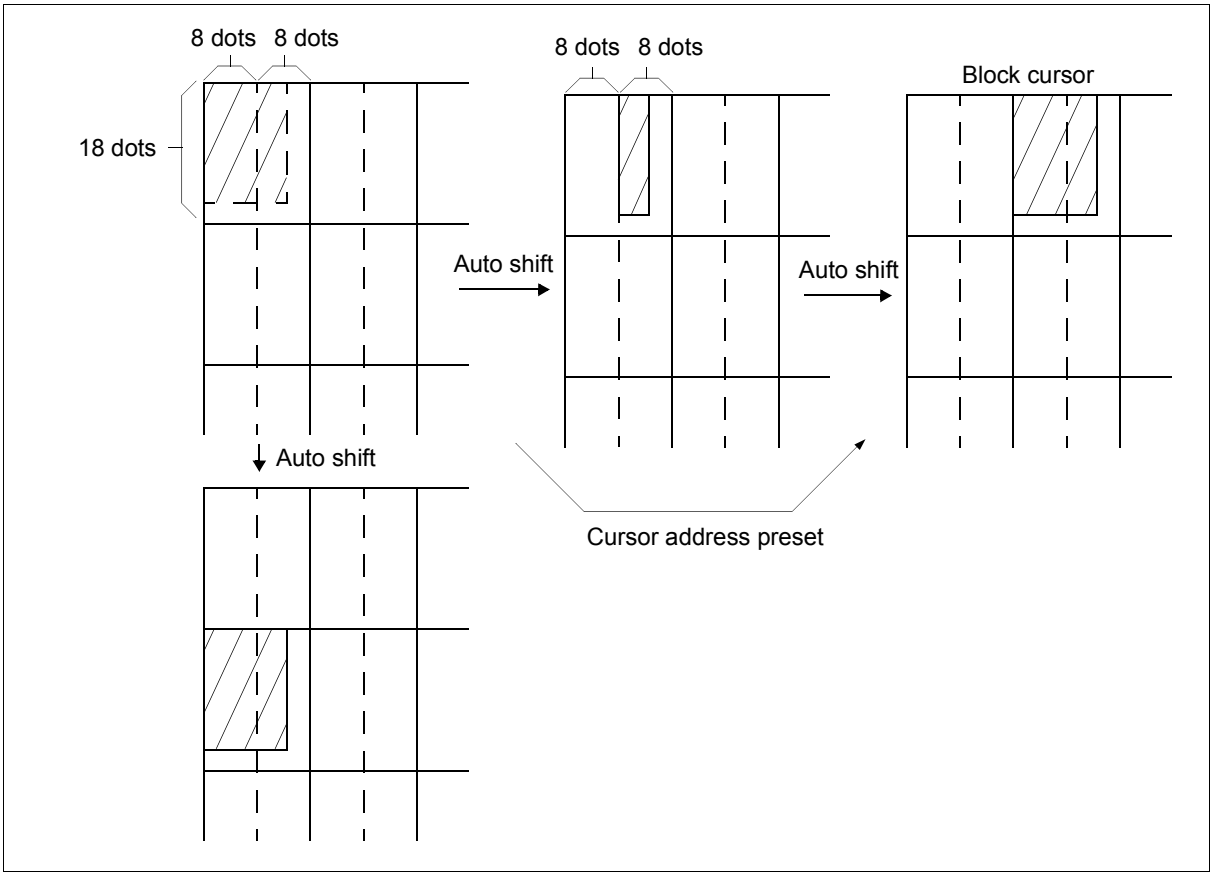


Figure 12-11 Cursor Movement

If no text screen is displayed, only a bar cursor can be displayed at the cursor address.

If the first layer is a mixed text and graphics screen and the cursor shape is set to a block cursor, the S1D13709 automatically decides which cursor shape to display. On the text screen it displays a block cursor, and on the graphics screen, a bar cursor.

12.4 Memory to Display Relationship

The S1D13709 supports virtual screens that are larger than the physical size of the LCD panel address range (CR), REG[03h] bits 7-0. A layer of the S1D13709 can be considered as a window into the larger virtual screen held in display memory. This window can be divided into two blocks, with each block able to display a different portion of the virtual screen.

For example, this allows one block to dynamically scroll through a data area while the other block is used as a status message display area.

For examples of the memory to display relationships, see Figure 12-12 “Screen Layers and Memory Relationship,” on page 132 and Figure 12-13 “Virtual Display (Display Window to Memory Relationship),” on page 133, and Figure 12-14 “Memory Map and Magnified Characters,” on page 134.

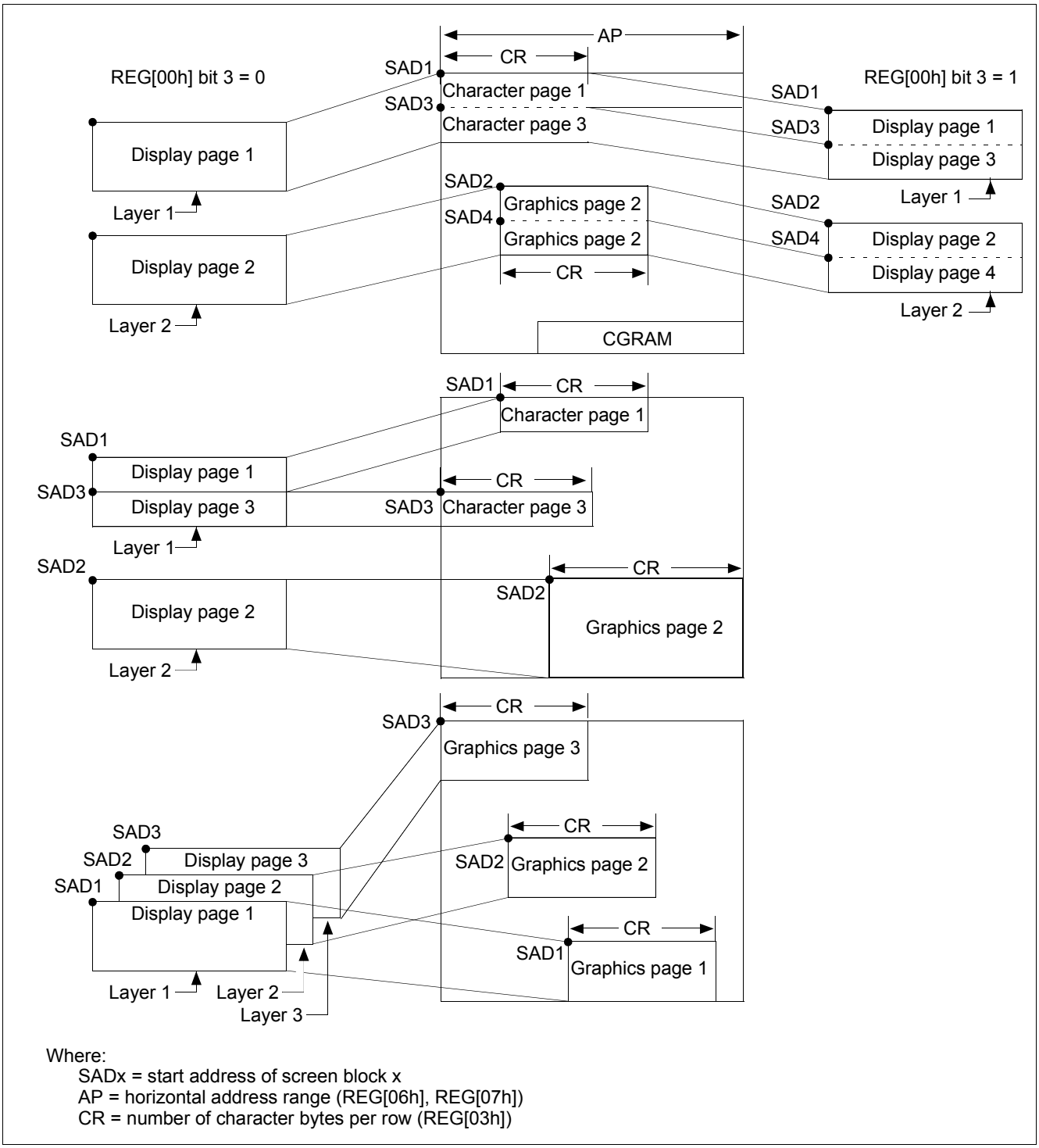
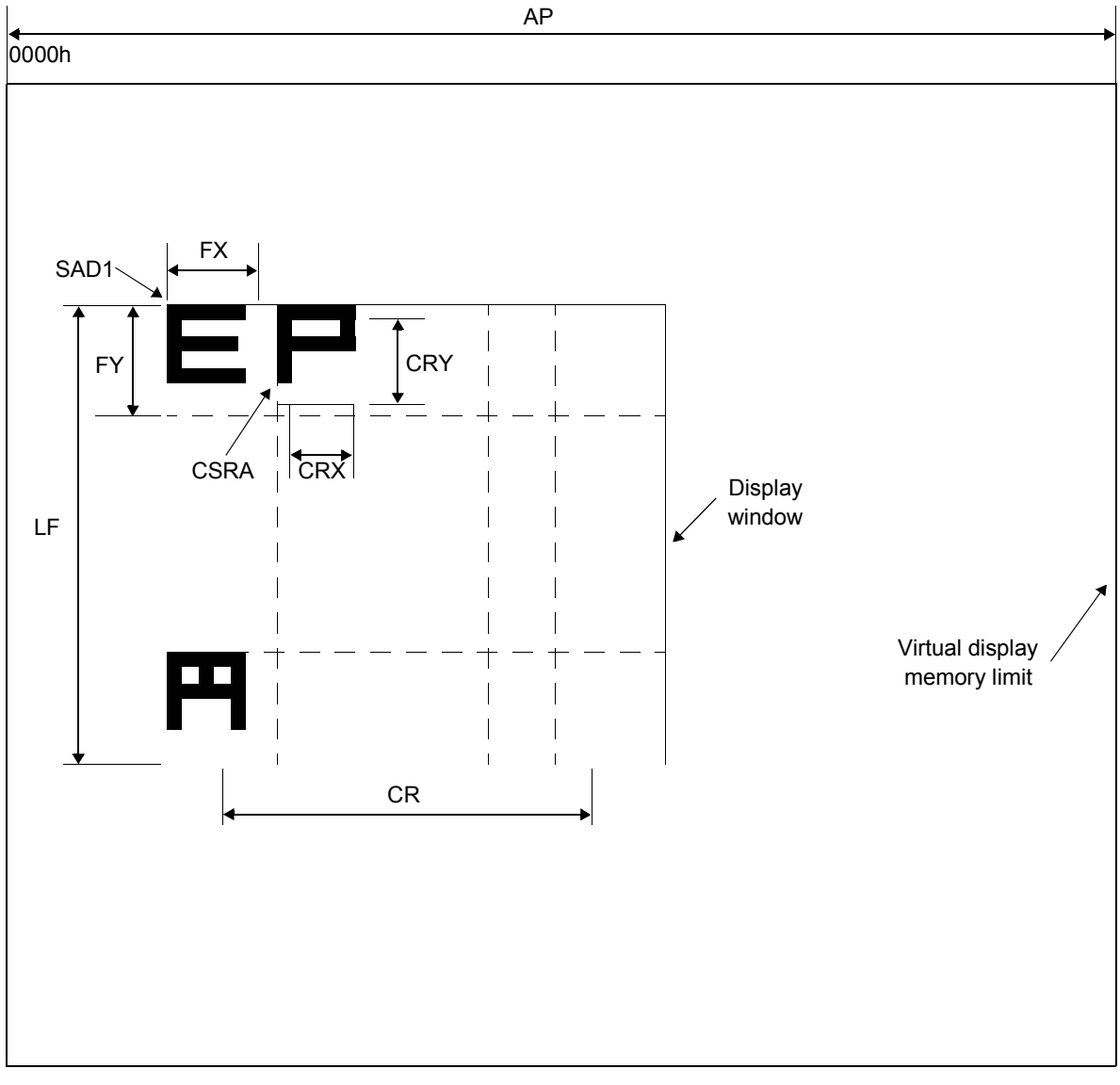


Figure 12-12 Screen Layers and Memory Relationship



Where:

FX = horizontal character size is 16 pixels (REG[01h] bits 3-0)
FY = vertical character size is 16 pixels (REG[02h] bits 3-0)
CRX = cursor width is 16 pixels (REG[15h] bits 3-0)
CRY = cursor height is 16 pixels (REG[16h] bits 3-0)
CR = character bytes per row is 240 bytes (REG[03h] bits 7-0)
LF = frame height is 256 (REG[05h] bits 7-0)
AP = horizontal address range (or address pitch) is 64K bytes (REG[06h] bits 7-0, REG[07h] bits 6-0)

Figure 12-13 Virtual Display (Display Window to Memory Relationship)

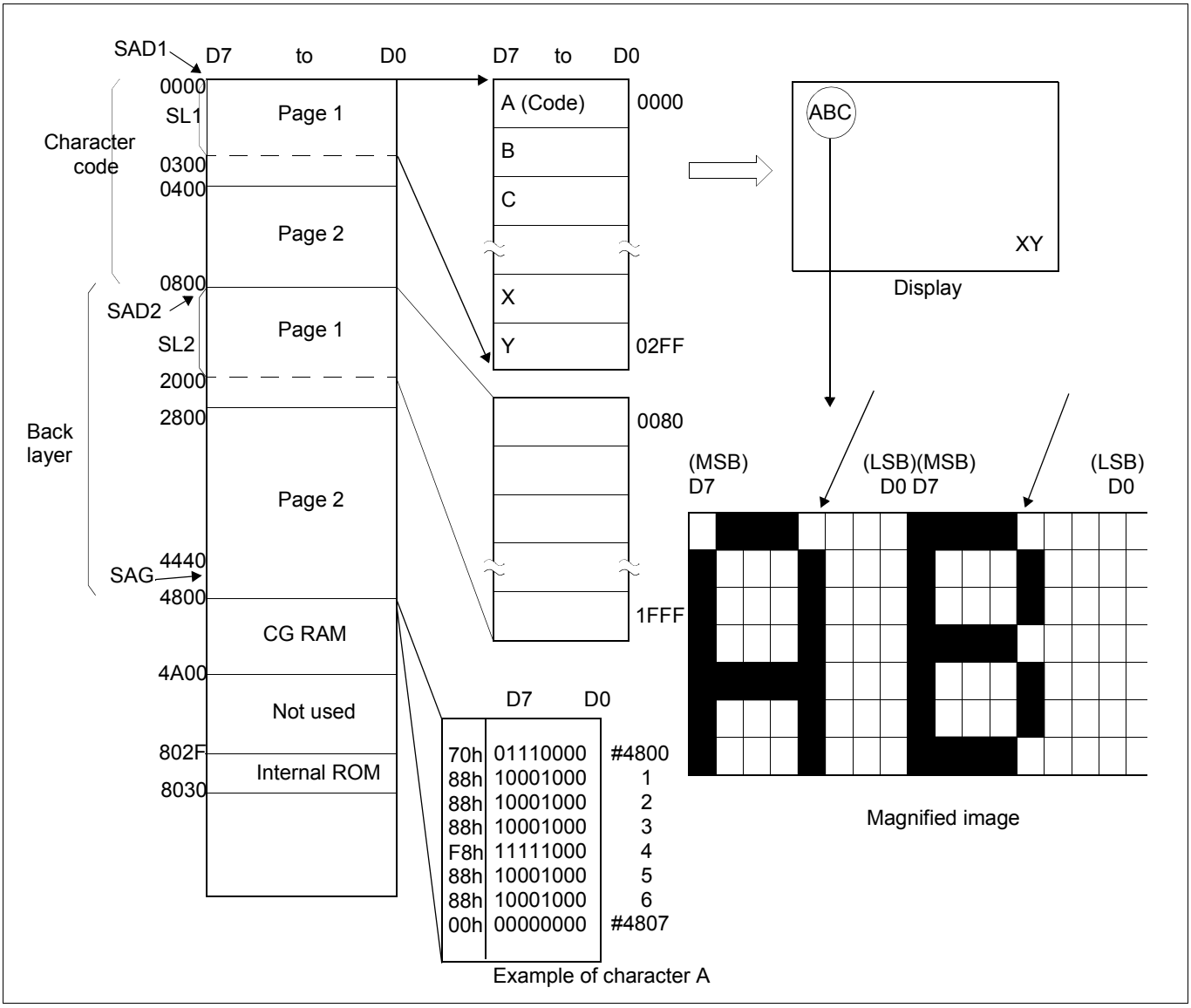


Figure 12-14 Memory Map and Magnified Characters

12.5 Scrolling

The microprocessor can control S1D13709 scrolling modes by writing the scroll address registers for each screen block, REG[0Bh] - REG[14h]. This is referred to as address scrolling and can be used for both text and graphic screen blocks, if the display memory capacity is greater than one screen.

12.5.1 On-Page Scrolling

The normal method of scrolling within a page is to move the whole display up one line and erase the bottom line. However, the S1D13709 does not automatically erase the bottom line, so it must be erased with blanking data when changing the scroll address register.

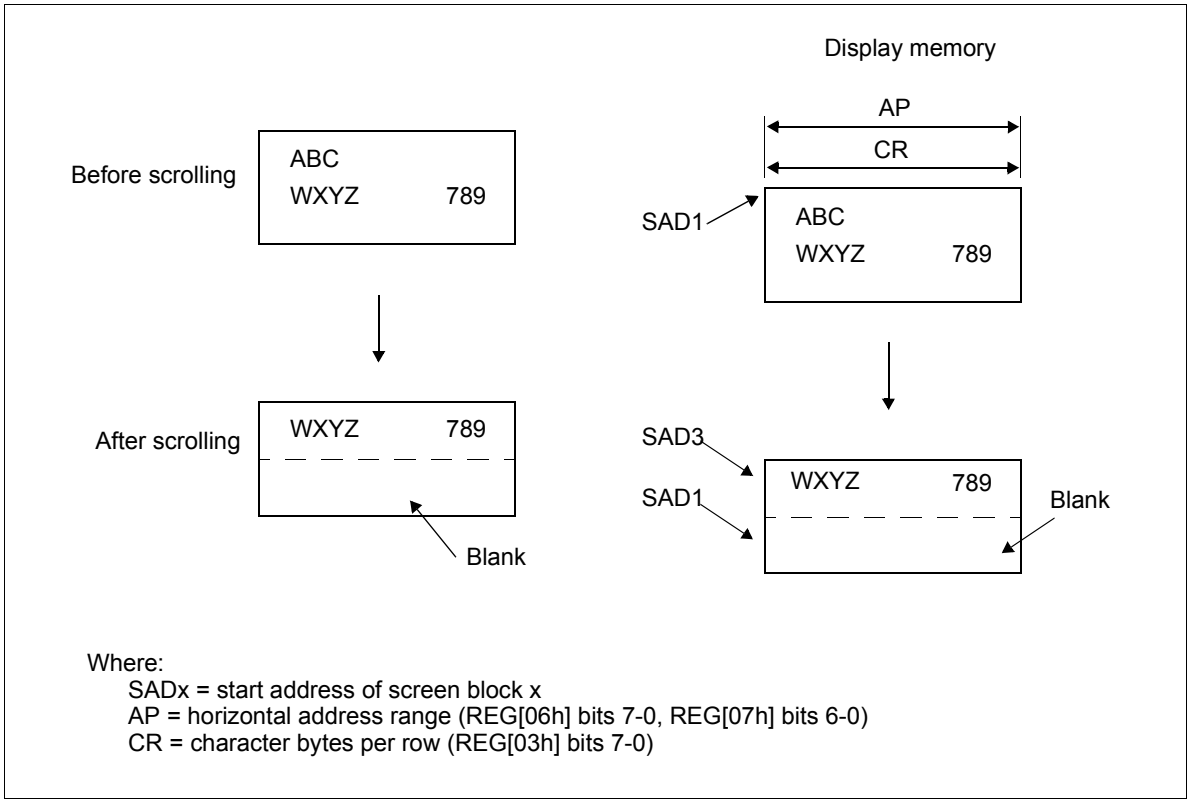


Figure 12-15 On-Page Scrolling

12.5.2 Inter-Page Scrolling

Scrolling between pages and page switching can be performed only if the display memory capacity is greater than one screen. To scroll down one line/character, add the value of the horizontal address range (or address pitch), REG[06h] - REG[07h], to the current SADx. To scroll up, subtract the value of the horizontal address range from SADx.

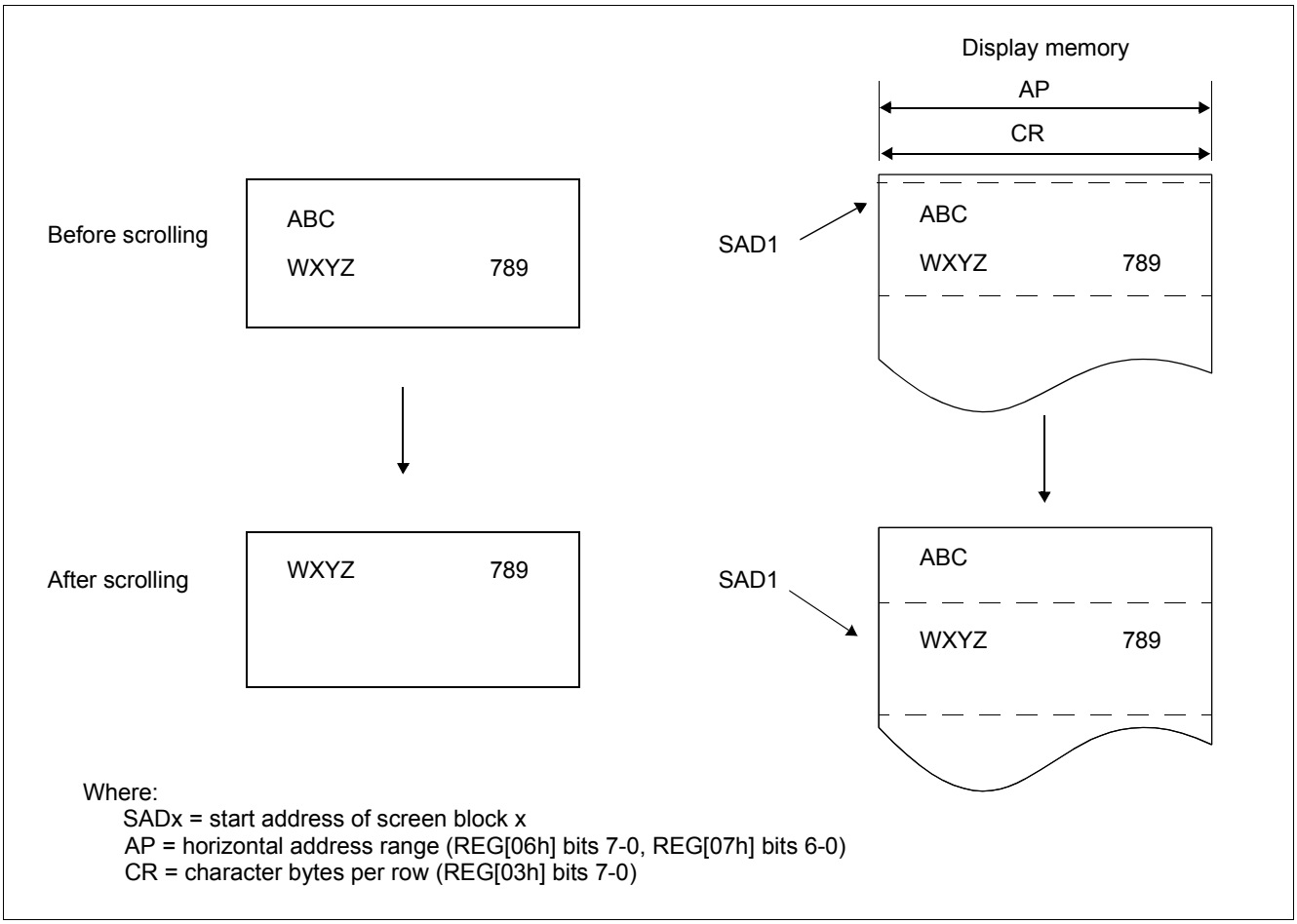


Figure 12-16 Inter-Page Scrolling

12.5.3 Horizontal Wraparound Scrolling

For screen block in text mode, the display can be scrolled horizontally in one character units, regardless of the display memory capacity.

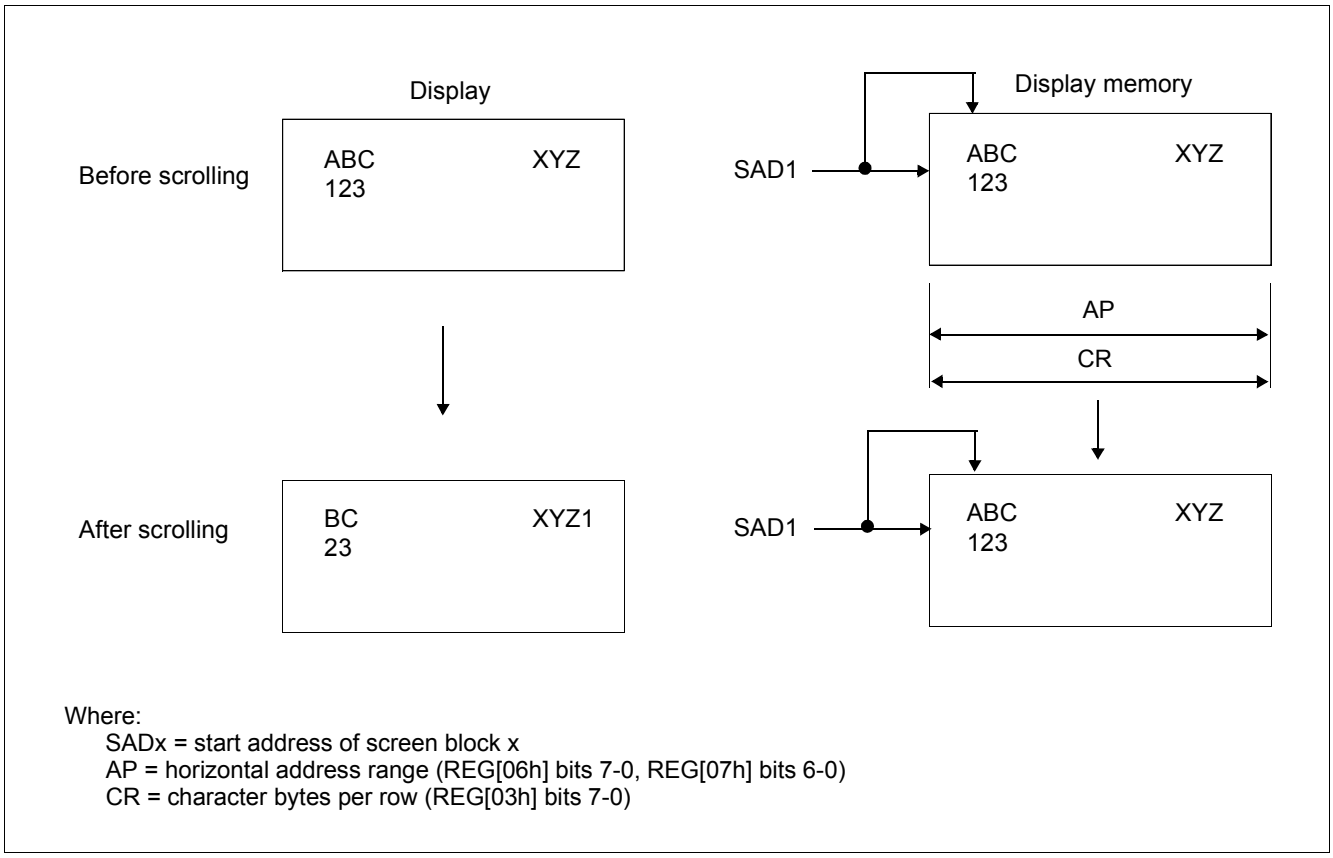


Figure 12-17 Horizontal Wraparound Scrolling

12.5.4 Bi-directional Scrolling

Bi-directional scrolling can be performed only if the display memory is larger than the physical screen in both the horizontal (REG[06h], REG[07h] > REG[03h]) and vertical directions. Scrolling is normally done in single-character units, however the HDOT SCR command (see REG[1Bh] bits 2-0) allows horizontal scrolling in pixel units (for text blocks only). Single pixel horizontal scrolling can be performed using both the SCROLL and HDOT SCR commands. For more information, see Section 15.4, “Smooth Horizontal Scrolling” on page 175.

Note

In 2 bpp and 4 bpp grayscale mode REG[1Bh] bits 2-0 (HDOT SCR) must be set to 0, so horizontal scrolling can only be done in single character units (not pixel units).

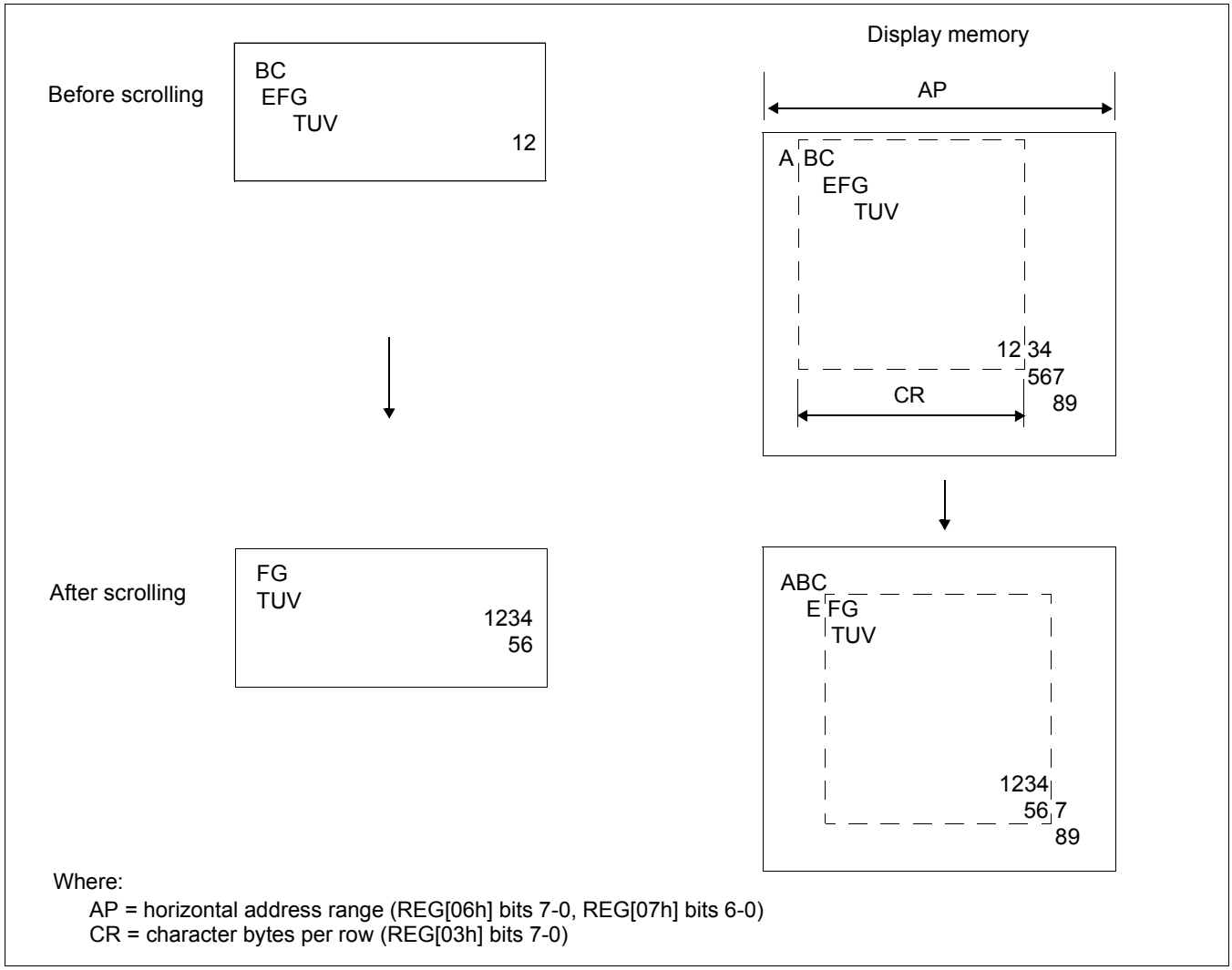


Figure 12-18 Bi-Directional Scrolling

12.5.5 Scroll Units

The following table summarizes the units, or steps, that can be scrolled for each mode.

Table 12-1 Scrolling Unit Summary

Mode	Vertical	Horizontal
Text	Characters	Pixels or Characters
Graphics	Pixels	Pixels

Note

In a divided screen, each block cannot be independently scrolled horizontally in pixel units.

12.5.6 Horizontal Pixel Scrolling (HDOTSCR)

When enabling HDOTSCR (REG[1Bh] bits 2-0 > 0h), the CR value should be increased by 1 (CR = CR + 1) from an exact horizontal dimensional fit of the LCD display (exact number of clocks for the display's row drivers). For example, a display 40 characters wide should have a CR value of 41 characters, when HDOTSCR is enabled. Otherwise, a blank character is retrieved (the next character is not displayed) and a blank space will be displayed on the right column of the display.

The following use cases demonstrate some examples of horizontal pixel scrolling.

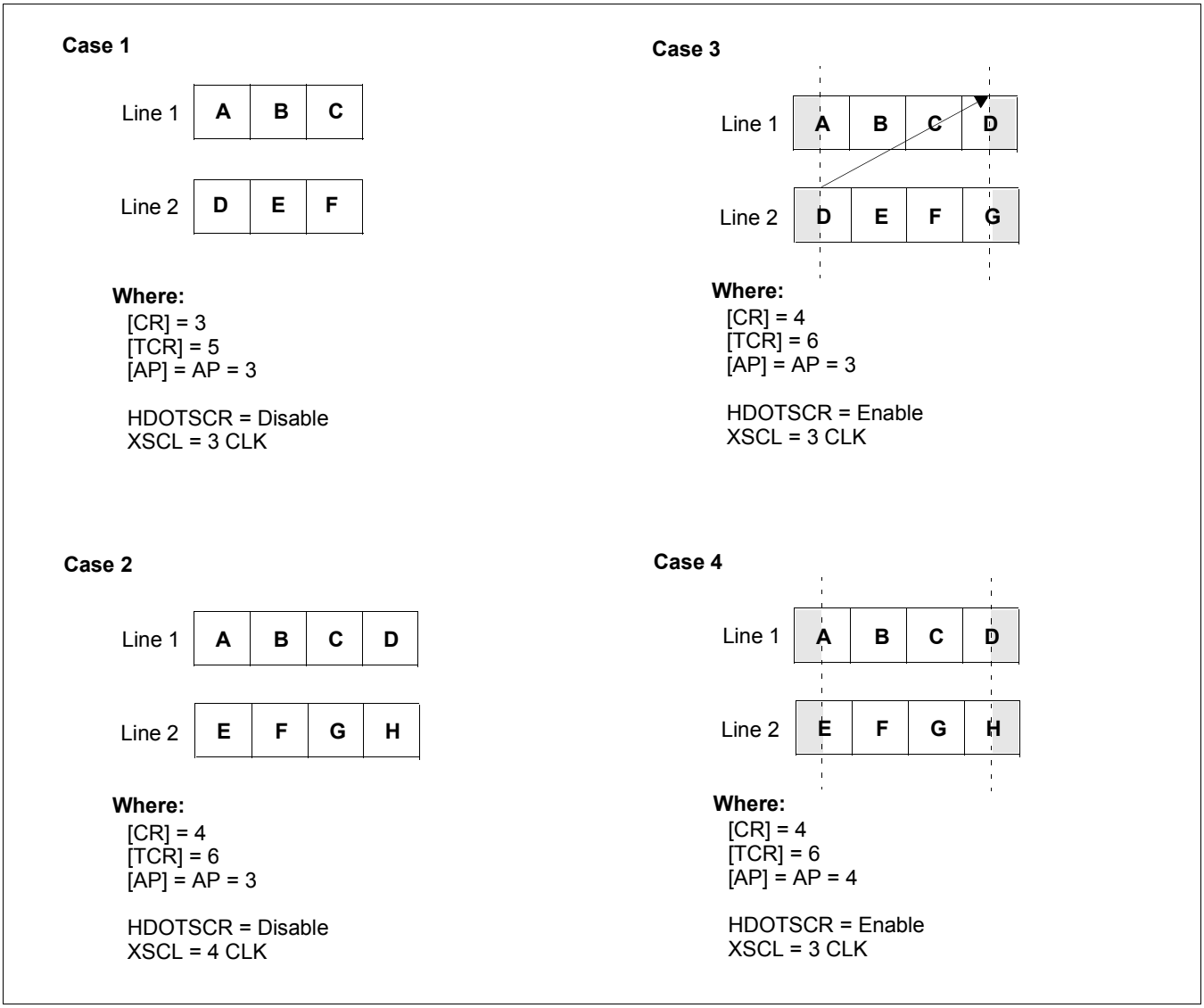


Figure 12-19 Horizontal Pixel Scrolling Use Cases

13 Character Generator

13.1 CG Characteristics

13.1.1 Internal Character Generator

The internal character generator is recommended for minimum system configurations containing a S1D13709, display RAM, LCD panel, single-chip microprocessor and power supply. Since the internal character generator uses a CMOS mask ROM, it is also recommended for low-power applications.

- 5 x 7 pixel font (See Section 16, “Internal Character Generator Font” on page 185)
- 160 JIS standard characters
- Can be mixed with character generator RAM (maximum of 64 CGRAM characters)
- Can be automatically spaced out up to 8 x 16 pixels

13.1.2 Character Generator RAM

The character generator RAM can be used for storing graphics characters. The character generator RAM can be mapped to any display memory location by the microprocessor, allowing effective usage of unused address space.

- Up to 8 x 8 pixel characters when REG[00h] bit 2 = 0 and 8 x 16 characters when REG[00h] bit 2 = 1
- Can be mapped anywhere in display memory address space if used with the character generator ROM (REG[00h] bit 0 = 0)

13.2 Setting the Character Generator Address

The CGRAM addresses in the display memory address space are not mapped directly from the address in the Character Generator RAM Start Address registers, REG[19h] - REG[1Ah]. The data to be displayed is at a CGRAM address calculated from (REG[19h] - REG[1Ah]) + character code + ROW select address. For the ROW select address, see Figure 13-1 “Row Select Address,” on page 143.

The following tables show the address mapping for CGRAM addresses.

Table 13-1 Character Fonts Where Number of Lines ≤ 8 (REG[00h] bit 2 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character Code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ROW Select Address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CGRAM Address	0	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Table 13-2 Character Fonts Where Number of Lines ≤ 16 (REG[00h] bit 2 = 1)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character Code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ROW Select Address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CGRAM Address	0	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Row	R3	R2	R1	R0
Row 0	0	0	0	0
Row 1	0	0	0	1
Row 2	0	0	1	0
↓	↓	↓	↓	↓
Row 7	0	1	1	1
Row 8	1	0	0	0
↓	↓	↓	↓	↓
Row 14	1	1	1	0
Row 15	1	1	1	1

Line 1

Line 2

Figure 13-1 Row Select Address

Note

Lines = 1: lines in the character bitmap ≤ 8.
Lines = 2: lines in the character bitmap ≥ 9.

13.2.1 CGRAM Addressing Example

Example 1: Define a pattern for the "A" in Figure 12-1 on page 120. The CGRAM table start address is 4800h. The character code for the defined pattern is 80h (the first character code in the CGRAM area).

As the character codes in Figure 13-2 "On-Chip Character Codes," on page 145 show, codes 80h to 9Fh and E0h to FFh are allocated to the CGRAM and can be used as desired. 80h is the first code for the CGRAM. As characters cannot be used if only using graphics mode, there is no need to set the CGRAM data.

Table 13-3 Character Data Example

CGRAM ADR	5Ch	Reverse the CGRAM address calculation to calculate SAG
P1	00h	
P2	40h	
CSRDIR	4Ch	Set cursor shift direction to right
CSRW	46h	CGRAM start address is 4800h
P1	00h	
P2	48h	
MWRITE	42h	
P	70h	Write ROW 0 data
P2	88h	Write ROW 1 data
P3	88h	Write ROW 2 data
P4	88h	Write ROW 3 data
P5	F8h	Write ROW 4 data
P6	88h	Write ROW 5 data
P7	88h	Write ROW 6 data
P8	00h	Write ROW 7 data
P9	00h	Write ROW 8 data
↓	↓	↓
P16	00h	Write ROW 15 data

13.3 Character Codes

The following figure shows the character codes and the codes allocated to CGRAM. All codes can be used by the CGRAM if not using the internal ROM (REG[00h] bit 0 = 1).

	Upper 4 bits															
Lower 4 bits	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		■		0	@	P	'	p				ー	ﾀ	ﾐ		
1		■	!	1	A	Q	a	q			｡	ｱ	ﾁ	ﾑ		
2		■	"	2	B	R	b	r			｢	ｲ	ﾂ	ﾒ		
3		■	#	3	C	S	c	s			｣	ｳ	ﾃ	ﾓ		
4		■	$	4	D	T	d	t			､	ｴ	ﾄ	ﾔ		
5		■	%	5	E	U	e	u			･	ｵ	ﾅ	ﾕ		
6		■	&	6	F	V	f	v			ｦ	ｶ	ﾆ	ﾖ		
7		■	'	7	G	W	g	w			ｧ	ｷ	ﾇ	ﾗ		
8		■	(	8	H	X	h	x			ｨ	ｸ	ﾈ	ﾘ		
9		■	)	9	I	Y	i	y			ｩ	ｹ	ﾉ	ﾙ		
A		■	*	:	J	Z	j	z			ｪ	ｺ	ﾊ	ﾚ		
B		■	+	;	K	[	k	{			ｫ	ｻ	ﾋ	ﾛ		
C		■	,	<	L	¥	l	¦			ｬ	ｼ	ﾌ	ﾜ		
D		■	.	=	M	]	m	}			ｭ	ｽ	ﾍ	ﾝ		
E		■	-	>	N	^	n	→			ｮ	ｾ	ﾎ	ﾞ		
F		■	/	?	O	_	o	←			ｯ	ｿ	ﾏ	ﾟ		

CGRAM1 ↑ ↑ CGRAM2 ↑ ↑

Figure 13-2 On-Chip Character Codes

14 Microprocessor Interface

14.1 System Bus Interface

CNF[4:0], A[15:1], A0, D[7:0], RD#, WR#, AS and CS are used as control signals for the microprocessor data bus. A0 is normally connected to the lowest bit of the system address bus. CNF[4:2] change the operation of the RD# and WR# pins to enable interfacing to either a Generic (Z80), M6800, or MC68K family bus, and should be pulled-up or pulled-down according to Table 5-7: "Summary of Configuration Options 1," on page 25.

14.1.1 Generic

The following table shows the signal states for each function.

Table 14-1 Generic Interface Signals

A0	RD#	WR#	Function
1	0	1	Display data and cursor address read
0	1	0	Display data and parameter write
1	1	0	Command write

14.1.2 M6800 Family

The following table shows the signal states for each function.

Table 14-2 M6800 Family Interface Signals

A0	R/W#	E	Function
1	1	1	Display data and cursor address read
0	0	1	Display data and parameter write
1	0	1	Command write

14.1.3 MC68K Family

The following table shows the signal states for each function.

Table 14-3 MC68K Family Interface Signals

A0	RD/WR#	LDS#	Function
1	1	0	Display data and cursor address read
0	0	0	Display data and parameter write
1	0	0	Command write

15 Application Notes

15.1 Register Initialization/Initialization Parameters

Square brackets around a parameter name indicate the number represented by the parameter, rather than the value written to the parameter register. For example, [FX] = FX + 1.

15.1.1 SYSTEM SET Command and Parameters for STN interface

- FX
  The horizontal character field size is determined from the horizontal display size in pixels [VD] and the number of characters per line [VC].

  [VD] ÷ [VC] = [FX]

- CR

  CR can be determined from VC and FX.

  [CR] = RNDUP ([FX] ÷ 8) [VC] x bpp

  Where RNDUP(x) denotes rounded up to the next highest integer. [CR] is the number of bytes per line, not the number of characters.

- TCR

  TCR must satisfy the condition [TCR] ≥ [CR] + 2.

- LF

  The number of lines per frame is determined by the display vertical resolution.

- f_{SYSCLK} and f_{FR}

  Once TCR has been set, the frame frequency, f_{FR}, and lines per frame [LF] will also have been set. Depending on number of gray shades (bpp) selected and the horizontal character field size, [FX], the system clock frequency f_{SYSCLK} is given by one of the following formula:

For 1 Bpp and [FX] ≥ 8:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [LF] x F (Hz)

where
A = [TCR] - [CR]
B = RNDDN([CR] x [FX] ÷ 8)
C = 16 x RNDUP(B ÷ 16)
D = C - B
E = (B x 16 ÷ [FX] + D) ÷ 2
F = A + E

For 1 Bpp and [FX] < 8:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [LF] x F (Hz)

where
A = [TCR] - [CR]
B = RNDDN([CR] x [FX] ÷ 4)
C = 16 x RNDUP(B ÷ 16)
D = C - B
E = (B x 8 ÷ [FX] + D) ÷ 2
F = A + E

For 2 Bpp:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [LF] x (A + C +1) (Hz)

where
A = [TCR] - [CR] + 1
B = RNDDN([CR] x [FX] ÷ 8)
C = 16 x RNDUP(B ÷ 16)

For 4 Bpp:

f_{SYSCLK} = 2 x [ClockDiv] x Ffr x [LF] x (A + 2 x C + 2) (Hz)

where
A = [TCR] - [CR] + 2
B = RNDDN([CR] x [FX] ÷ 16)
C = 16 x RNDUP(B ÷ 16)

For all cases above where:

ClockDiv	4, 8, or 16
Ffr	Frame Rate

If no standard crystal close to the calculated value of f_{SYSCLK} exists, a higher frequency crystal can be used and the value of TCR revised using one of the above equations.

- Symptoms of an incorrect TCR setting are listed below. If any of these appears, check the value of TCR and modify it if necessary.
  - Vertical scanning halts and a high-contrast horizontal line appears.
  - All pixels are on or off.
  - The LP output signal is absent or corrupted.
  - The display is unstable.

Table 15-1 Panel Calculations

Product Resolution (X × Y)	[FX]	[FY]	[CR]	[TCR]	f_{SYSCLK} (MHz) See note 2
256 x 64	[FX] = 6 pixels: 256 ÷ 6 = 42 remainder 4 = 4 blank pixels	8 or 16, depending on the screen	[CR] = 42 bytes. When using HDOT SCR, [CR] = 43 bytes	46	1.66
512 x 64	[FX] = 6 pixels: 512 ÷ 6 = 85 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[CR] = 85 bytes. When using HDOT SCR, [CR] = 86 bytes	98	3.52
256 x 128	[FX] = 8 pixels: 256 ÷ 8 = 32 remainder 0 = no blank pixels	8 or 16, depending on the screen	[CR] = 32 bytes. When using HDOT SCR, [CR] = 33 bytes	36	2.5
512 x 128	[FX] = 10 pixels: 256 ÷ 10 = 51 remainder 2 = 2 blank pixels	8 or 16, depending on the screen	[CR] = 102 bytes. When using HDOT SCR, [CR] = 103 bytes	120	8.6

Note

[1] The remaining pixels on the right-hand side of the display are automatically blanked by the S1D13709. There is no need to zero the display memory corresponding to these pixels.

[2] Assumes a frame frequency of 70 Hz, 1 bpp, and a clock divide of 4.

15.1.2 SYSTEM SET Command and Parameters for TFT interface

- FX

  The horizontal character field size of the source image is determined from the horizontal source image size in pixels [VD] and the number of characters per source image line [VC].

  [VD] ÷ [VC] = [FX]

- CR

  CR can be determined from VC and FX.

  [CR] = RNDUP ([FX] ÷ 8) x [VC] x bpp

Where RNDUP(x) denotes rounded up to the next highest integer. [CR] is the number of bytes per line, not the number of characters.

- TCR

  TCR must satisfy the condition [TCR] ≥ [CR] + 2.

- LF

  The number of lines per frame is determined by the display vertical resolution.

- f_P and f_{FR}

  The TFT clock (FPSHIFT) frequency, f_P is determined from [HT], [VT] and the frame frequency Ffr.

  f_P = [VT] x [HT] x Ffr

  The TFT clock is generated by the PLL. For further information, see REG[31h] - REG[33h].

- f_{SYSCLK}

  For the system clock frequency, f_{SYSCLK}, 20 or 24MHz is recommended.

Note

1. When 4bpp is selected (REG[20h] bits 1-0 = 10), f_{SYSCLK} must be equal or greater than 24MHz.
2. The following formula is required.

$f_{SYSCLK} \leq 7 \times f_P$

$f_{SYSCLK} \geq 8$ ([TCR] + 4) x [LF] x f_P ÷ [VDP] ÷ [HT]

$f_{SYSCLK} \geq 16$ x ([TCR] + 4) x f_P ÷ [HT] ÷ ([VT] - [VDP] - [VDPS])

where

[VT] = TFT Vertical Total ({REG[3Ch]bits2-0, REG[3Bh]bits7-0}+1)

[VDP] = TFT Vertical Display Period ({REG[3Eh]bits2-0, REG[3Dh]bits7-0}+1)

[VDPS] = TFT Vertical Display Period Start Position ({REG[40h]bits2-0, REG[3Fh]bits7-0})

[HT] = TFT Horizontal Total ({REG[36h]bits2-0, REG[35h]bits7-0}+1)

15.1.3 Initialization Example for STN Interface

The initialization example shown below is for a S1D13709 with an 8-bit microprocessor interface bus and an STN-LCD 512 × 128 pixels.

Indirect Addressing

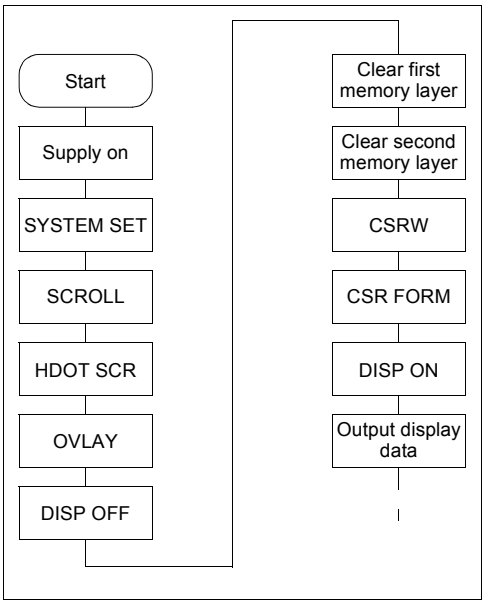


Figure 15-1 Initialization Procedure

Note

Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20h (text screen only) or 00h (graphics screen only). Determining which memory to clear is explained in Section 15.1.5, "Display Mode Setting Example 1: Combining Text and Graphics" on page 163.

Table 15-2 Indirect Addressing Initialization Procedure

No.	Command	Operation
1	Set CNF[10:0] pins	
2	release RESET#	
3	SYSTEM SET C = 40h	
	Wait a crystal stabilization time	If using a crystal, insert a delay here for crystal stabilization. The delay time depends on a crystal. If using an external oscillator, the delay is not required.
	P1 = 38h	M0: Internal CGROM (REG[00h] bit 0) M2: 8 lines per character (REG[00h] bit 2) W/S: Two-panel drive (REG[00h] bit 3)

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

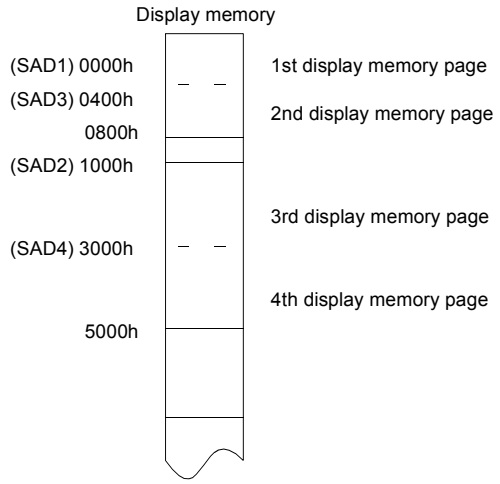
No.	Command	Operation
		IV: Sets top-line compensation to none (REG[00h] bit 5)
	P2 = 87h	FX: Horizontal character size = 8 pixels (REG[01h] bits 3-0)
		MOD: Two-frame AC drive (REG[01h] bit 7)
	P3 = 07h	FY: Vertical character size = 8 pixels (REG[02h] bits 3-0
	P4 = 3Fh	CR: 64 display addresses per line (REG[03h] bits 7-0)
	P5 = 59h	TCR: Total address range per line = 90 (REG[04h] bits 7-0)
		f_{SYSCLK} = 6.5 MHz, fFR = 70 Hz
	P6 = 7Fh	LF: 128 display lines (REG[05h] bits 7-0
	P7 = 80h	AP: Virtual screen horizontal size is 128 addresses (REG[06h] bits 7-0, REG[07h] bits 6-0)
	P8 = 00h	
4	SCROLL	
	C = 44h	
	P1 = 00h	First screen block start address (REG[0Bh] bits 7-0, REG[0Ch] bits 6-0)
	P2 = 00h	Set to 0000h
	P3 = 40h	Display lines in first screen block = 64 (REG[0Dh] bits 7-0)
	P4 = 00h	Second screen block start address (REG[0Eh] bits 7-0, REG[0Fh] bits 6-0)
	P5 = 10h	Set to 1000h
	P6 = 40h	Display lines in second screen block = 64 (REG[10h] bits 7-0)
	P7 = 00h	Third screen block start address (REG[11h] bits 7-0, REG[12h] bits 6-0)
	P8 = 04h	Set to 0400h
	P9 = 00h	Fourth screen block start address (REG[13h] bits 7-0, REG[14h] bits 6-0)
	P10 = 30h	Set to 3000h
		
5	HDOT SCR	
	C = 5Ah	
	P1 = 00h	Set horizontal pixel shift to zero (REG[1Bh] bits 2-0)
6	OVLAY	
	C = 5Bh	

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

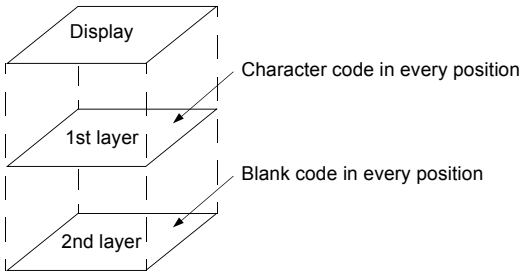
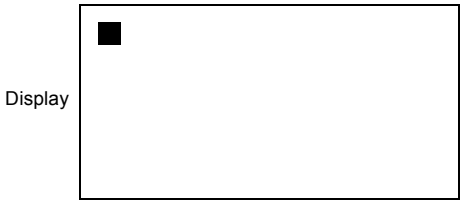
No.	Command	Operation
	P1 = 01h	MX 1, MX 0: Inverse video superposition (REG[18h] bits 1-0)
		DM 1: First screen block is text mode (REG[18h] bit 2)
		DM 2: Third screen block is text mode (REG[18h] bit 3)
7	DISP ON/OFF	
	C = 58h	D: Display OFF (REG[09h] bit 0)
	P1 = 56h	FC1, FC0: Flash cursor at 2 Hz (REG[0Ah] bits 1-0)
	FP1, FP0:	First screen block ON (REG[0Ah] bits 3-2)
	FP3, FP2:	Second and fourth screen blocks ON (REG[0Ah] bits 5-4)
	FP5, FP4:	Third screen block ON (REG[0Ah] bits 7-6)
8	Clear data in first layer	Fill first screen layer memory with 20h (space character)
9	Clear data in second layer	Fill second screen layer memory with 00h (blank data)
		
10	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to start of first screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 00h	
11	CSR FORM	
	C = 5Dh	
	P1 = 04h	CRX: Horizontal cursor size = 5 pixels (REG[15h] bits 3-0)
	P2 = 86h	CRY: Vertical cursor size = 7 pixels (REG[16h] bits 3-0)
		CM: Block cursor (REG[16h] bit 7)
12	DISP ON/OFF	
	C = 59h	Display ON
	P1 = 56h	
13	CSR DIR	
	C = 4Ch	Set cursor shift direction to right (REG[17h] bits 1-0)
14	MWRITE	
	C = 42h	
	P1 = 20h	‘ ’

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

No.	Command	Operation
	P2 = 45h	'E'
	P3 = 50h	'P'
	P4 = 53h	'S'
	P5 = 4Fh	'O'
	P6 = 4Eh	'N'
		EPSON■
15	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to start of second screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 10h	
16	CSR DIR	
	C = 4Fh	Set cursor shift direction to down (REG[17h] bits 1-0)
17	MWRITE	
	C = 42h	
	P1 = FFh	Fill in a square to the left of the 'E'
	↓	
	P9 = FFh	
		■EPSON
18	CSRW	
	C = 46h	
	P1 = 01h	Set cursor address to 1001h (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 10h	
19	MWRITE	
	C = 42h	
	P1 = FFh	Fill in the second screen block in the second column of line 1
	↓	
	P9 = FFh	
20	CSRW	Repeat operations 18 and 19 to fill in the background under 'EPSON' (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)

Table 15-2 Indirect Addressing Initialization Procedure (Continued)

No.	Command	Operation
↓		Inverse display EPSON
29	MWRITE	
30	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to line three of the first screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 01h	
31	CSR DIR	
	C = 4Ch	Set cursor shift direction to right (REG[17h] bits 1-0)
32	MWRITE	
	C = 42h	
	P1 = 44h	'D'
	P2 = 6Fh	'o'
	P3 = 74h	't'
	P4 = 20h	' '
	P5 = 4Dh	'M'
	P6 = 61h	'a'
	P7 = 74h	't'
	P8 = 72h	'r'
	P9 = 69h	'i'
	P10 = 78h	'x'
	P11 = 20h	' '
	P12 = 4Ch	'L'
	P13 = 43h	'C'
	P14 = 44h	'D'
		Inverse display EPSON Dot matrix LCD

15.1.4 Initialization Example for TFT Interface

The initialization example shown below is for a S1D13709 with an 8-bit microprocessor interface bus and an TFT-LCD WVGA 800 × 480 pixels. The source image in the display memory is 320 x 240 pixels.

Indirect Addressing

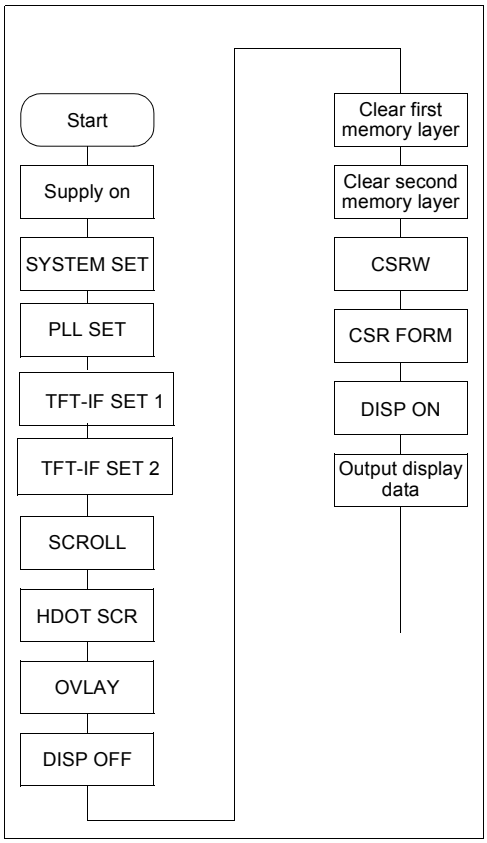


Figure 15-2 Initialization Procedure

Note

Set the cursor address to the start of each screen's layer memory, and use MWRITE to fill the memory with space characters, 20h (text screen only) or 00h (graphics screen only). Determining which memory to clear is explained in Section 15.1.5, "Display Mode Setting Example 1: Combining Text and Graphics" on page 163.

Table 15-3 Indirect Addressing Initialization Procedure

No.	Command	Operation
1	Set CNF[10:0] pins	
2	release RESET#	
3	SYSTEM SET	
	C = 40h	
	Wait a crystal stabilization time	If using a crystal, insert a delay here for crystal stabilization. The delay time depends on a crystal. If using an external oscillator, the delay is not required.
	P1 = 30h	M0: Internal CGROM (REG[00h] bit 0)
		M2: 8 lines per character (REG[00h] bit 2)
		W/S: For TFT interface, set to 0. (REG[00h] bit 3)
		IV: Sets top-line compensation to none (REG[00h] bit 5)
	P2 = 07h	FX: Horizontal character size = 8 pixels (REG[01h] bits 3-0)
		MOD: For TFT interface, this bit does not care. (REG[01h] bit 7)
	P3 = 07h	FY: Vertical character size = 8 pixels (REG[02h] bits 3-0
	P4 = 27h	CR: 40 display addresses per line (REG[03h] bits 7-0)
	P5 = 36h	TCR: Total address range per line = 55 (REG[04h] bits 7-0)
		f_{SYSCLK} =20 MHz, fFR = 60 Hz
	P6 = EFh	LF: 240 display lines (REG[05h] bits 7-0
	P7 = 50h	AP: Virtual screen horizontal size is 80 addresses (REG[06h] bits 7-0, REG[07h] bits 6-0)
	P8 = 00h	
4	PLL SET	
	C = 62h	
	P1 = 21h	PIR: 2 (REG[31h] bits 3-0), f_{PLLI} = 20 MHz ÷ 2 = 10 MHz
		POR: 3 (REG[31h] bits 7-4), f_P = 100 MHz ÷ 3 = 33.3 MHz
	P2 = 99h	N: 10 (REG[32h] bits 3-0), f_{PLLIO} = 10 MHz x 10= 100 MHz
		RS: 9 (REG[32h] bits 7-4)
	P2 = 24h	VC: 4 (REG[33h] bits 4-0)
		V: 2 (REG[33h] bits 6-5), f_{VCO} = 100 MHz x 2 = 200 MHz
5	TFT-IF SET 1	
	C = 63	
	P1 = 25h	TFT interface: Enable (REG[34h] bit 0)
		TFT Color Mode: Gray (REG[34h] bit 1)
		TFT Up-Scaler Method: Nearest Neighbor (REG[34h] bit 2)
		FPSHIFT Polarity: The signals change at the falling edge of FPSHIFT (REG[34h] bit 4)
		FPDRDY Polarity: Active High (REG[34h] bit 5)
		FPLINE Polarity: Active Low (REG[34h] bit 6)
		FPFRAME Polarity: Active Low (REG[34h] bit 7)
6	TFT-IF SET 2	

Table 15-3 Indirect Addressing Initialization Procedure (Continued)

No.	Command	Operation
	C = 64h	
	P1 = 1Fh	TFT Horizontal Total Period = 1056 (REG[36h] bits 2-0, REG[35h] bits 7-0)
	P2 = 04h	Set to 041Fh
	P3 = 1Fh	TFT Horizontal Display Period = 800 (REG[38h] bits 2-0, REG[37h] bits 7-0)
	P4 = 03h	Set to 031Fh
	P5 = 2Eh	TFT Horizontal Display Start Position = 46 (REG[3Ah] bits 2-0, REG[39h] bits 7-0)
	P6 = 00h	Set to 031Fh
	P7 = 0Fh	TFT Vertical Total Period = 528 (REG[3Ch] bits 2-0, REG[3Bh] bits 7-0)
	P8 = 02h	Set to 020Fh
	P9 = DFh	TFT Vertical Display Period = 480 (REG[3Eh] bits 2-0, REG[3Dh] bits 7-0)
	P10 = 01h	Set to 01DFh
	P11 = 17h	TFT Vertical Display Start Position = 23 (REG[40h] bits 2-0, REG[3Fh] bits 7-0)
	P12 = 00h	Set to 0017h
	P13 = 02h	TFT FPFRAME Pulse Width = 3 (REG[41h] bits 7-0)
	P14 = 07h	TFT FPLINE Pulse Width = 8 (REG[42h] bits 7-0)
	P15 = 00h	TFT FPLINE Pulse Position = 0 (REG[44h] bits 2-0, REG[43h] bits 7-0)
	P16 = 00h	Set to 0000h
	P17 = 99h	TFT Horizontal Scale Ratio = 800 ÷ 320 = 2.5 (REG[46h] bits 2-0, REG[45h] bits 7-0)
	P18 = 01h	Set to 0199h
	P19 = 00h	TFT Vertical Scale Ratio = 480 ÷ 240 = 2 (REG[48h] bits 2-0, REG[47h] bits 7-0)
	P20 = 02h	Set to 0200h
	P21 = 00h	TFT Horizontal Delay Offset = 0 (REG[4Ah] bits 2-0, REG[49h] bits 7-0)
	P22 = 00h	Set to 0000h
7	SCROLL	
	C = 44h	
	P1 = 00h	First screen block start address (REG[0Bh] bits 7-0, REG[0Ch] bits 6-0)
	P2 = 00h	Set to 0000h
	P3 = 7Fh	Display lines in first screen block = 128 (REG[0Dh] bits 7-0)
	P4 = 00h	Second screen block start address (REG[0Eh] bits 7-0, REG[0Fh] bits 6-0)
	P5 = 20h	Set to 2000h
	P6 = EFh	Display lines in second screen block = 240 (REG[10h] bits 7-0)
	P7 = 00h	Third screen block start address (REG[11h] bits 7-0, REG[12h] bits 6-0)
	P8 = 01h	Set to 1000h
	P9 = 00h	Fourth screen block start address (REG[13h] bits 7-0, REG[14h] bits 6-0) is not used.

Table 15-3 Indirect Addressing Initialization Procedure (Continued)

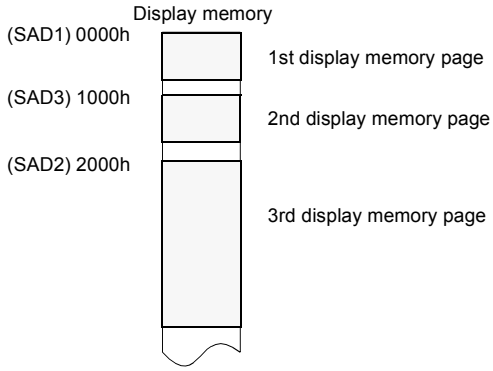
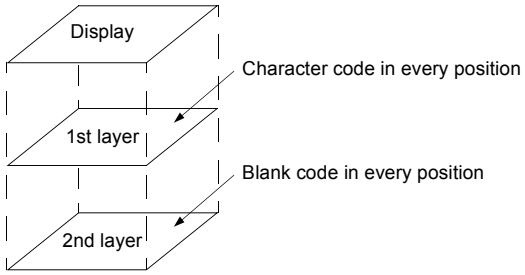
No.	Command	Operation
	P10 = 00h	Set to 0000h 
8	HDOT SCR	
	C = 5Ah	
	P1 = 00h	Set horizontal pixel shift to zero (REG[1Bh] bits 2-0)
9	OVLAY	
	C = 5Bh	
	P1 = 01h	MX 1, MX 0: Inverse video superposition (REG[18h] bits 1-0)
		DM 1: First screen block is text mode (REG[18h] bit 2)
		DM 2: Third screen block is text mode (REG[18h] bit 3)
10	DISP ON/OFF	
	C = 58h	D: Display OFF (REG[09h] bit 0)
	P1 = 56h	FC1, FC0: Flash cursor at 2 Hz (REG[0Ah] bits 1-0)
	FP1, FP0:	First screen block ON (REG[0Ah] bits 3-2)
	FP3, FP2:	Second screen blocks ON (REG[0Ah] bits 5-4)
	FP5, FP4:	Third screen block ON (REG[0Ah] bits 7-6)
11	Clear data in first layer	Fill first screen layer memory with 20h (space character)
12	Clear data in second layer	Fill second screen layer memory with 00h (blank data) 
13	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to start of first screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 00h	
14	CSR FORM	
	C = 5Dh	

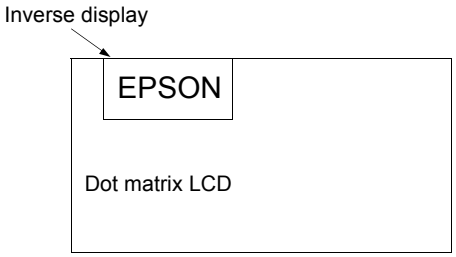
Table 15-3 Indirect Addressing Initialization Procedure (Continued)

No.	Command	Operation
	P1 = 04h	CRX: Horizontal cursor size = 5 pixels (REG[15h] bits 3-0)
	P2 = 86h	CRY: Vertical cursor size = 7 pixels (REG[16h] bits 3-0)
		CM: Block cursor (REG[16h] bit 7)
15	DISP ON/OFF	
	C = 59h	Display ON
	P1 = 56h	Display ■
16	CSR DIR	
	C = 4Ch	Set cursor shift direction to right (REG[17h] bits 1-0)
17	MWRITE	
	C = 42h	
	P1 = 20h	‘ ’
	P2 = 45h	‘E’
	P3 = 50h	‘P’
	P4 = 53h	‘S’
	P5 = 4Fh	‘O’
	P6 = 4Eh	‘N’
		EPSON■
18	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to start of second screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 10h	
19	CSR DIR	
	C = 4Fh	Set cursor shift direction to down (REG[17h] bits 1-0)
20	MWRITE	
	C = 42h	
	P1 = FFh	Fill in a square to the left of the ‘E’
	↓	

Table 15-3 Indirect Addressing Initialization Procedure (Continued)

No.	Command	Operation
	P9 = FFh	
		■EPSON
21	CSRW	
	C = 46h	
	P1 = 01h	Set cursor address to 1001h (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 10h	
22	MWRITE	
	C = 42h	
	P1 = FFh	Fill in the second screen block in the second column of line 1
	↓	
	P9 = FFh	
23	CSRW	Repeat operations 21 and 22 to fill in the background under 'EPSON' (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
		Inverse display
↓		EPSON
32	MWRITE	
33	CSRW	
	C = 46h	
	P1 = 00h	Set cursor to line three of the first screen block (REG[1Ch] bits 7-0, REG[1Dh] bits 7-0)
	P2 = 01h	
34	CSR DIR	
	C = 4Ch	Set cursor shift direction to right (REG[17h] bits 1-0)
35	MWRITE	
	C = 42h	
	P1 = 44h	'D'
	P2 = 6Fh	'o'
	P3 = 74h	't'
	P4 = 20h	' '
	P5 = 4Dh	'M'
	P6 = 61h	'a'

Table 15-3 Indirect Addressing Initialization Procedure (Continued)

No.	Command	Operation
	P7 = 74h	't'
	P8 = 72h	'r'
	P9 = 69h	'i'
	P10 = 78h	'x'
	P11 = 20h	' '
	P12 = 4Ch	'L'
	P13 = 43h	'C'
	P14 = 44h	'D'
		

15.1.5 Display Mode Setting Example 1: Combining Text and Graphics

Conditions

- STN LCD: 320 × 200 pixels, single panel drive (1/200 duty cycle)
  TFT LCD: 800 × 480 pixels
- First layer: text display
- Second layer: graphics display
- 8 × 8-pixel character font
- CGRAM not required

Display memory allocation

- First layer (text): 320 ÷ 8 = 40 characters per line, 240 ÷ 8 = 30 lines. Required memory size = 40 × 30 = 1200 bytes.
- Second layer (graphics): 320 ÷ 8 = 40 characters per line, 240 ÷ 1 = 240 lines. Required memory size = 40 × 240 = 9600 bytes.

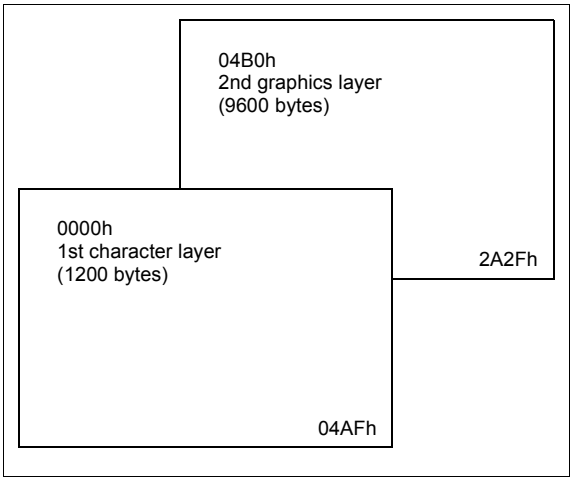


Figure 15-3 Character Over Graphics Layers

Register Setup Procedure

SYSTEM SET	TCR calculation
C = 40h	
add a delay here if using a crystal (Delay time depends on a crystal)	
P1 = 30h	For the STN interface: f_{SYSCLK} = 6.5 MHz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters for STN interface” on page 147) For the TFT interface: f_{SYSCLK} = 20 MHz (refer to Section 15.1.2, “SYSTEM SET Command and Parameters for TFT interface” on page 149)
P2 = 87h	fFR = 60 Hz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters for STN interface” on page 147)
P3 = 07h	
P4 = 27h	
P5 = 33h	[TCR] = 52, so TCR = 33h
P6 = EFh	
P7 = 28h	
P8 = 00h	
PLL SET	This command is for the TFT interface only.
C = 62h	
P1 = 21h	
P2 = 99h	
P2 = 24h	
TFT-IF SET 1	This command is for the TFT interface only.
C = 63	
P1 = 25h	
TFT-IF SET 2	This command is for the TFT interface only.
C = 64h	
P1 = 1Fh	
P2 = 04h	
P3 = 1Fh	
P4 = 03h	
P5 = 2Eh	
P6 = 00h	
P7 = 0Fh	
P8 = 02h	
P9 = DFh	
P10 = 01h	
P11 = 17h	
P12 = 00h	
P13 = 02h	
P14 = 07h	

P15 = 00h
P16 = 00h
P17 = 99h
P18 = 01h
P19 = 00h
P20 = 02h
P21 = 00h
P22 = 00h

SCROLL

C = 44h
P1 = 00h
P2 = 00h
P3 = EFh
P4 = AFh
P5 = 04h
P6 = EFh
P7 = Xh
P8 = Xh
P9 = Xh
P10 = Xh

CSRFORM

C = 5Dh
P1 = 04h
P2 = 86h

HDOT SCR

C = 5Ah
P1 = 00h

OVLAY

C = 5Bh
P1 = 00h

DISP ON/OFF

C = 59h
P1 = 16h

X = Don’t care

15.1.6 Display Mode Setting Example 2: Combining Graphics and Graphics

Conditions

- STN LCD: 320 × 200 pixels, single panel drive (1/200 duty cycle)
  TFT LCD: 800 × 480 pixels
- First layer: graphics display
- Second layer: graphics display

Display memory allocation

- First layer (graphics): 320 ÷ 8 = 40 characters per line, 240 ÷ 1 = 240 lines. Required memory size = 40 × 240 = 9600 bytes.
- Second layer (graphics): 320 ÷ 8 = 40 characters per line, 240 ÷ 1 = 240 lines. Required memory size = 9600 bytes.

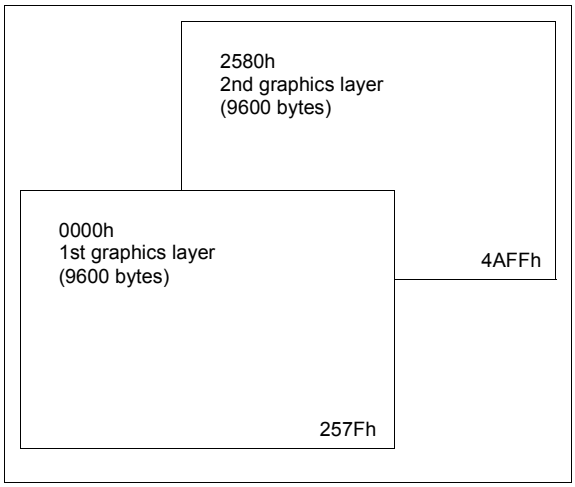


Figure 15-4 Two-Layer Graphics

Register setup procedure

SYSTEM SET	TCR calculation
C = 40h	
add a delay here if using a crystal (Delay time depends on a crystal)	
P1 = 30h	For the STN interface: f_{SYSCLK} = 6.5 MHz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters for STN interface” on page 147) For the TFT interface: f_{SYSCLK} = 20 MHz (refer to Section 15.1.2, “SYSTEM SET Command and Parameters for TFT interface” on page 149)
P2 = 87h	f_{FR} = 60 Hz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters for STN interface” on page 147)
P3 = 07h	
P4 = 27h	
P5 = 33h	[TCR] = 52, so TCR = 33h
P6 = EFh	
P7 = 28h	
P8 = 00h	
PLL SET	This command is for the TFT interface only.
C = 62h	
P1 = 21h	
P2 = 99h	
P2 = 24h	
TFT-IF SET 1	This command is for the TFT interface only.
C = 63	
P1 = 25h	
TFT-IF SET 2	This command is for the TFT interface only.
C = 64h	
P1 = 1Fh	
P2 = 04h	
P3 = 1Fh	
P4 = 03h	
P5 = 2Eh	
P6 = 00h	
P7 = 0Fh	
P8 = 02h	
P9 = DFh	
P10 = 01h	
P11 = 17h	
P12 = 00h	

P13 = 02h
P14 = 07h
P15 = 00h
P16 = 00h
P17 = 99h
P18 = 01h
P19 = 00h
P20 = 02h
P21 = 00h
P22 = 00h

SCROLL
C = 44h
P1 = 00h
P2 = 00h
P3 = EFh
P4 = 80h
P5 = 25h
P6 = EFh
P7 = Xh
P8 = Xh
P9 = Xh
P10 = Xh

CSRFORM
C = 5Dh
P1 = 07h
P2 = 87h

HDOT SCR
C = 5Ah
P1 = 00h

OVLAY
C = 5Bh
P1 = 0Ch

DISP ON/OFF
C = 59h
P1 = 16h

X = Don’t care

15.1.7 Display Mode Setting Example 3: Combining Three Graphics Layers

Conditions

- STN LCD: 320 × 200 pixels, single panel drive (1/200 duty cycle)
  TFT LCD: 800 × 480 pixels
- First layer: graphics display
- Second layer: graphics display
- Third layer: graphics display

Display memory allocation

- All layers (graphics): 320 ÷ 8 = 40 characters per line, 240 ÷ 1 = 240 lines. Required memory size = 40 × 240 = 9600 bytes.

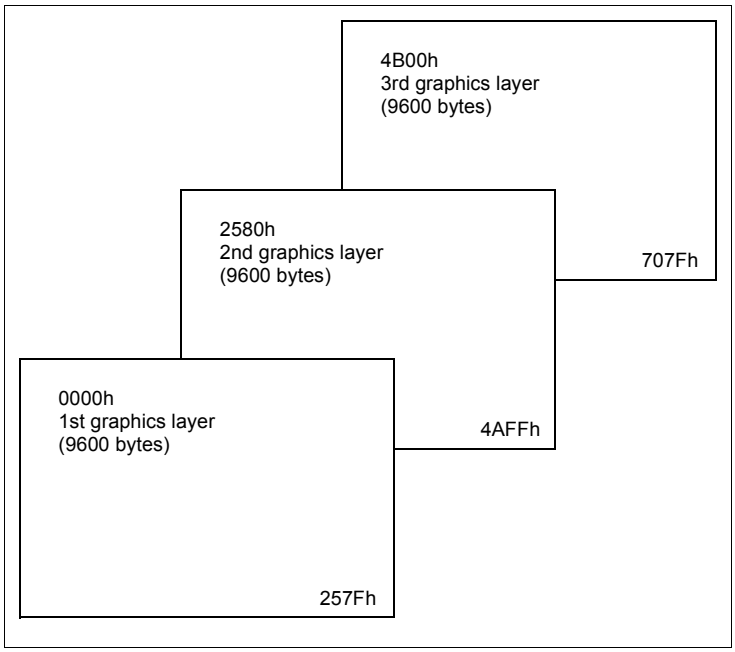


Figure 15-5 Three-Layer Graphics

Register setup procedure

SYSTEM SET	TCR calculation
C = 40h	
add a delay here if using a crystal (Delay time depends on a crystal)	
P1 = 30h	For the STN interface: f_{SYSCLK} = 6.5 MHz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters for STN interface” on page 147) For the TFT interface: f_{SYSCLK} = 20 MHz (refer to Section 15.1.2, “SYSTEM SET Command and Parameters for TFT interface” on page 149)
P2 = 87h	f_{FR} = 60 Hz (refer to Section 15.1.1, “SYSTEM SET Command and Parameters for STN interface” on page 147)
P3 = 07h	
P4 = 27h	
P5 = 33h	[TCR] = 52, so TCR = 33h
P6 = EFh	
P7 = 28h	
P8 = 00h	
PLL SET	This command is for the TFT interface only.
C = 62h	
P1 = 21h	
P2 = 99h	
P2 = 24h	
TFT-IF SET 1	This command is for the TFT interface only.
C = 63	
P1 = 25h	
TFT-IF SET 2	This command is for the TFT interface only.
C = 64h	
P1 = 1Fh	
P2 = 04h	
P3 = 1Fh	
P4 = 03h	
P5 = 2Eh	
P6 = 00h	
P7 = 0Fh	
P8 = 02h	
P9 = DFh	
P10 = 01h	
P11 = 17h	
P12 = 00h	
P13 = 02h	

P14 = 07h
P15 = 00h
P16 = 00h
P17 = 99h
P18 = 01h
P19 = 00h
P20 = 02h
P21 = 00h
P22 = 00h

SCROLL
C = 44h
P1 = 00h
P2 = 00h
P3 = EFh
P4 = 80h
P5 = 25h
P6 = EFh
P7 = 00h
P8 = 4Bh
P9 = Xh
P10 = Xh

CSR FORM
C = 5Dh
P1 = 07h
P2 = 87h

HDOT SCR
C = 5Ah
P1 = 00h

OVLAY
C = 5Bh
P1 = 1Ch

DISP ON/OFF
C = 59h
P1 = 16h

X = Don’t care

15.2 TFT interface automatic setting mode

All registers except for the TFT interface are compatible with the S1D13700. When the STN interface is used, the S1D13700 software can be used with S1D13709. When the TFT interface is used, settings for the TFT interface must be added to the S1D13700 software. However, when the S1D13700 software is programmed for a “QVGA” STN display and the setting is single panel drive (REG[00h] bit 3 = 0), the S1D13700 software can be used with S1D13709 in TFT interface automatic setting Mode.

Note

When the S1D13700 software is programmed for dual panel drive mode (REG[00h] bit 3= 1), the TFT interface automatic setting mode is not available.

CNF[10:5] pins configure TFT interface Auto-setting Mode.
CNF[7:5] select the TFT panel size, QVGA, WQVGA, VGA and WVGA.
CNF8 selects the TFT clock (FPSHIFT) polarity.
CNF9 selects the TFT interface pins output drive.
CNF10 selects input clock (CLKI, XCG1) frequency.
For further information on the CNF[10:5], see Section Table 5-7:, “Summary of Configuration Options 1” on page 25.

The TFT clock frequency is determined by CNF[7:5] and CNF[10] as below.

Table 15-4 TFT Clock Frequency at TFT Interface Automatic setting Mode

CNF[10]	CNF[7:5]	FPSHIFT Frequency			Units
		Min	Typ	Max	
0 (CLKI/XCG1 = 20.00MHz)	001 (QVGA to QVGA)	6.5	6.7	6.8	MHz
1 (CLKI/XCG1 = 24.00MHz)	001 (QVGA to QVGA)	6.8	6.9	7.1	MHz
0 (CLKI/XCG1 = 20.00MHz)	010 (QVGA to WQVGA)	8.2	8.3	8.5	MHz
1 (CLKI/XCG1 = 24.00MHz)	010 (QVGA to WQVGA)	8.5	8.7	8.9	MHz
0 (CLKI/XCG1 = 20.00MHz)	011 (QVGA to VGA)	24.5	25.0	25.5	MHz
1 (CLKI/XCG1 = 24.00MHz)	011 (QVGA to VGA)	25.5	26.0	26.6	MHz
0 (CLKI/XCG1 = 20.00MHz)	100 (QVGA to WVGA)	32.7	33.3	34.0	MHz
1 (CLKI/XCG1 = 24.00MHz)	100 (QVGA to WVGA)	34.0	34.7	35.4	MHz

The TFT interface automatic setting flow is below.

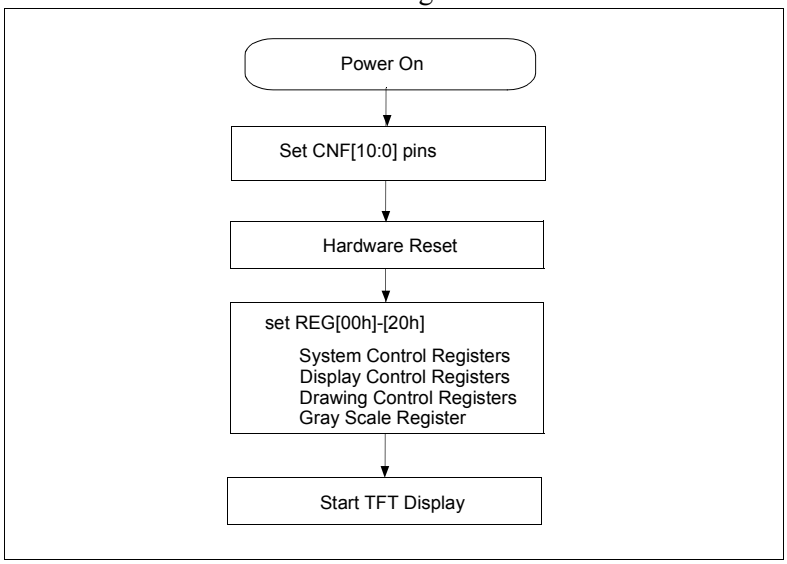


Figure 15-6 TFT interface Automatic setting Flowchart

CNF[10:5] configure REG[31h]-[73h] to the below value. When the TFT interface automatic setting mode is enabled (SEL[7:5] = 001, 010, 011 or 100), the REG[31h]-[73h] can not be changed by Host access.

Table 15-5 TFT interface Register Automatic Setting Value

Register	Automatically Setting Value			
	CNF[7:5] = 001 to QVGA	**CNF[7:5] = 010 to WQVGA**	**CNF[7:5] = 011 to VGA**	**CNF[7:5] = 100 to WVGA**
REG[31h]	E1h (SEL10 = 0) E2h (SEL10 = 1)	B1h (SEL10 = 0) B2h (SEL10 = 1)	31h (SEL10 = 0) 32h (SEL10 = 1)	21h (SEL10 = 0) 22h (SEL10 = 1)
REG[32h]	99h (SEL10 = 0) 9Ch (SEL10 = 1)	99h (SEL10 = 0) 9Ch (SEL10 = 1)	99h (SEL10 = 0) 9Ch (SEL10 = 1)	99h (SEL10 = 0) 9Ch (SEL10 = 1)
REG[33h]	24h	24h	24h	24h
REG[34h] (Note)	25h (SEL8 = 0) 35h (SEL8 = 1)	25h (SEL8 = 0) 35h (SEL8 = 1)	25h (SEL8 = 0) 35h (SEL8 = 1)	25h (SEL8 = 0) 35h (SEL8 = 1)
REG[35h]	97h	0Fh	1Fh	1Fh
REG[36h]	01h	02h	03h	04h
REG[37h]	3Fh	DFh	7Fh	1Fh
REG[38h]	01h	01h	02h	03h
REG[39h]	46h	28h	90h	2Eh
REG[3Ah]	00h	00h	00h	00h
REG[3Bh]	07h	1Fh	0Fh	0Fh
REG[3Ch]	01h	01h	02h	02h
REG[3Dh]	EFh	0Fh	DFh	DFh
REG[3Eh]	00h	01h	01h	01h
REG[3Fh]	0Dh	08h	23h	17h
REG[40h]	00h	00h	00h	00h
REG[41h]	02h	02h	02h	02h
REG[42h]	07h	07h	07h	07h
REG[43h]	00h	00h	00h	00h
REG[44h]	00h	00h	00h	00h
REG[45h]	00h	AAh	00h	99h
REG[46h]	04h	02h	02h	01h
REG[47h]	00h	87h	00h	00h
REG[48h]	04h	03h	02h	02h
REG[49h]	00h	00h	00h	00h
REG[4Ah]	00h	00h	00h	00h
REG[4Bh],[63h]-[72h]	Not Available			
REG[73h]	00h (SEL9 = 0) FFh (SEL9 = 1)	00h (SEL9 = 0) FFh (SEL9 = 1)	00h (SEL9 = 0) FFh (SEL9 = 1)	00h (SEL9 = 0) FFh (EL9 = 1)

Note

In TFT interface automatic setting mode, Gray scale mode is selected (REG[34h] bit 1 = 0). For Gray scale mode pin connection information, see Section Figure 3-6, “S1D13709 to TFT-LCD Example (Gray Scale Mode, REG[34h]bit1 = 0)” on page 13.

15.3 System Overview

Section 3, “System Diagrams” on page 10 shows some typical S1D13709 implementations where the microprocessor issues instructions to the S1D13709, and the S1D13709 drives the LCD panel. Since the S1D13709 integrates all required LCD control circuits, minimal external components are required to construct a complete medium- resolution liquid crystal display solution.

15.4 Smooth Horizontal Scrolling

The S1D13709 supports smooth horizontal scrolling to the left as shown in Figure 15-7 “HDOT SCR Example,” on page 176. When scrolling left, the screen is effectively moving to the right over the larger virtual screen.

Instead of changing the screen block start address (SADx) and shifting the display by eight pixels, smooth scrolling is achieved by repeatedly changing the horizontal pixel scroll parameter of the HDOT SCR command (REG[1Bh] bits 2-0). When the display has been scrolled seven pixels, the horizontal pixel scroll parameter is reset to zero and screen block start address is incremented by one. Repeating this operation at a suitable rate gives the appearance of smooth scrolling.

Note
To scroll the display to the right, the procedure is reversed.

When the edge of the virtual screen is reached, the microprocessor must take appropriate steps to avoid corrupting the display. For example, scrolling must be stopped or the display must be modified.

Note
The HDOT SCR command cannot be used to scroll individual layers.

Note
When in 2 bpp or 4 bpp mode, smooth horizontal scrolling in pixel units is not supported.

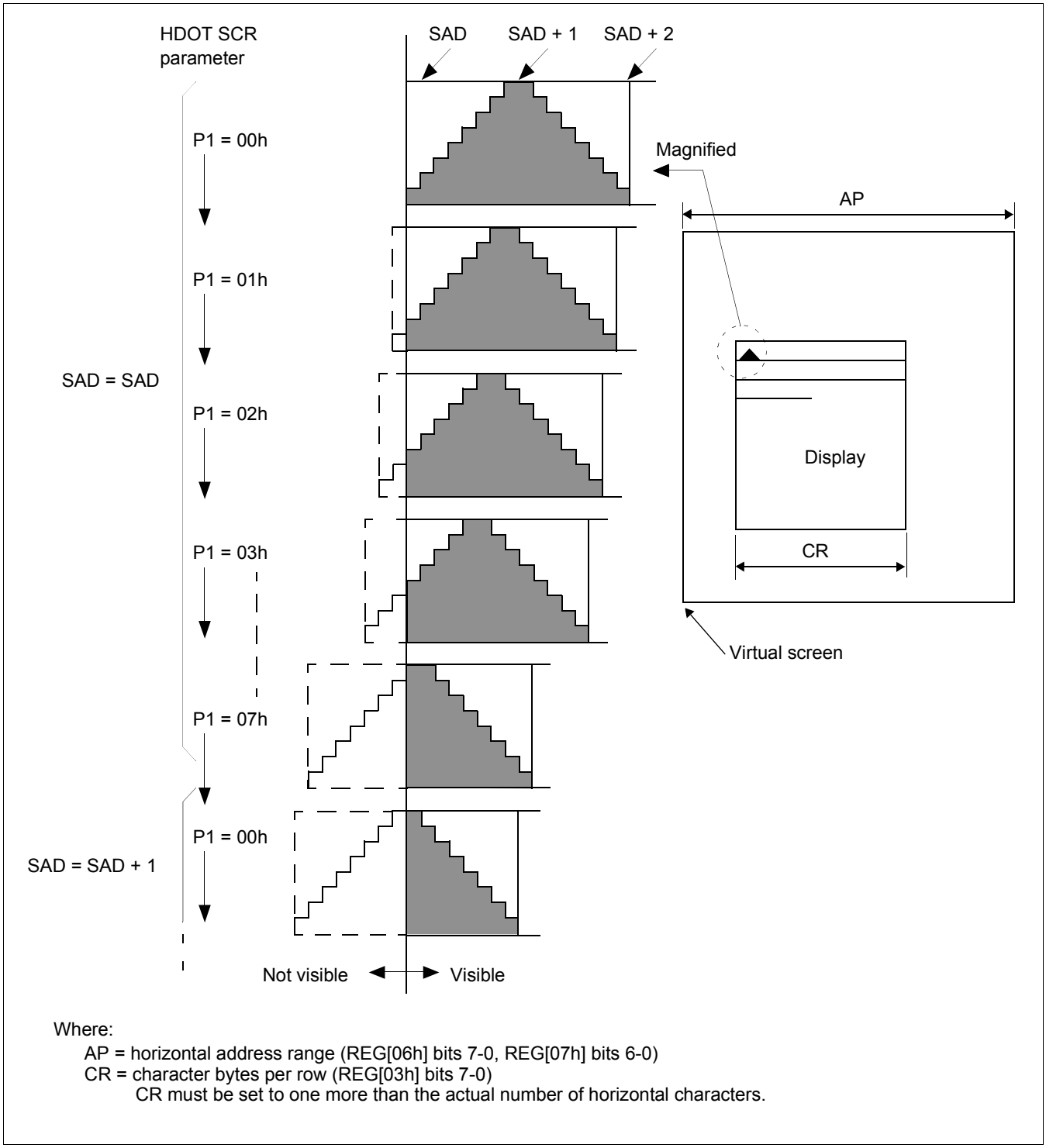


Figure 15-7 HDOT SCR Example

Note

The response time of LCD panels changes considerably at low temperatures. Smooth scrolling under these conditions may make the display difficult to read.

For combination of HDOT SCR and SAD scrolling, the following flow is recommended to prevent a display flicker caused by difference of each registers update timing.

Figure 15-8 HDOT SCR and SADx Simultaneously Update

15.5 Layered Display Attributes

S1D13709 incorporates a number of functions for enhancing displays using monochrome LCD panels. It allows the display of inverse characters, half-intensity menu pads and flashing of selected screen areas. These functions are controlled by REG[18h] Overlay Register and REG[0Ah] Display Attribute Register.

Attribute	MX1	MX0	Combined Layer Display	1st Layer Display	2nd Layer Display
Reverse	0	1	IV EPSON	IV EPSON	
Half-tone	0	0	ME Yes, No	ME Yes, No	
Local flashing	0 0	0 1	BL Error	BL	Error
Ruled line	0 0	0 1	RL LINE LINE	RL LINE LINE	

Figure 15-9 Layer Synthesis

These effects can be achieved in different ways, depending on the display configuration. The following sections describe these functions.

Note
Not all functions can be used in one layer at the same time.

15.5.1 Inverse Display

For inverse display where the first layer is text and the second layer is graphics.

1. CSRW, CSRDIR, MWRITE

   Write to the graphics screen at the area to be inverted.

2. OVLAY: MX0 = 1, MX1 = 0 (REG[18h] bits 1-0)

   Set the layer compensation method of the two layers to Exclusive-OR.

3. DISP ON/OFF: FP0 = 1, FP1 = 0, FP2 = 1, FP3 = 0.

   Turn on layers 1 and 2 with no flashing.

15.5.2 Half-Tone Display

The FP parameter (display attributes) can be used to generate a half-intensity display by flashing the display at 17Hz. Note that this mode may cause flicker problems with certain LCD panels.

Menu Pad Display

Turn flashing off for the first layer, on at 17 Hz for the second layer, and combine the screens using the OR function.

1. REG[18h] Overlay Register = 00h
2. REG[0Ah] Display Attribute Register = 34h

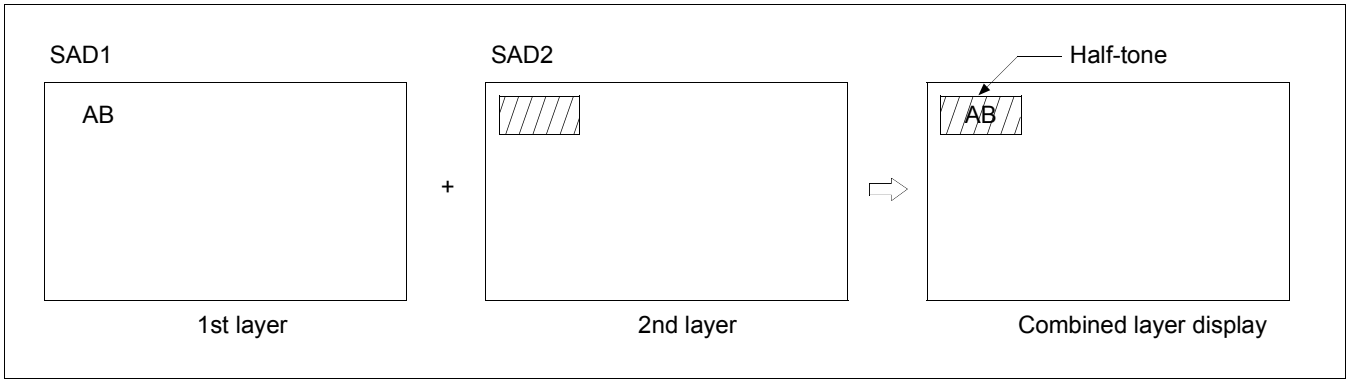


Figure 15-10 Half-Tone Character And Graphics

Graph Display

To display two overlaid graphs on the screen, configure the display in the same manner as for menu pad display and put one graph on each screen layer. The difference in contrast between the half and full intensity displays make it easy to distinguish between the two graphs and create an attractive display.

1. REG[18h] Overlay Register = 00h
2. REG[0Ah] Display Attribute Register = 34h

15.5.3 Flash Attribute

Small Area

To flash selected characters, the MPU can alternately write the characters as character codes and blank characters at intervals of 0.5 to 1.0 seconds.

Large Area

Divide both layer 1 and layer 2 into two screen blocks each, layer 2 being divided into the area to be flashed and the remainder of the screen. Flash the layer 2 screen block at 2 Hz for the area to be flashed and combine the layers using the OR function.

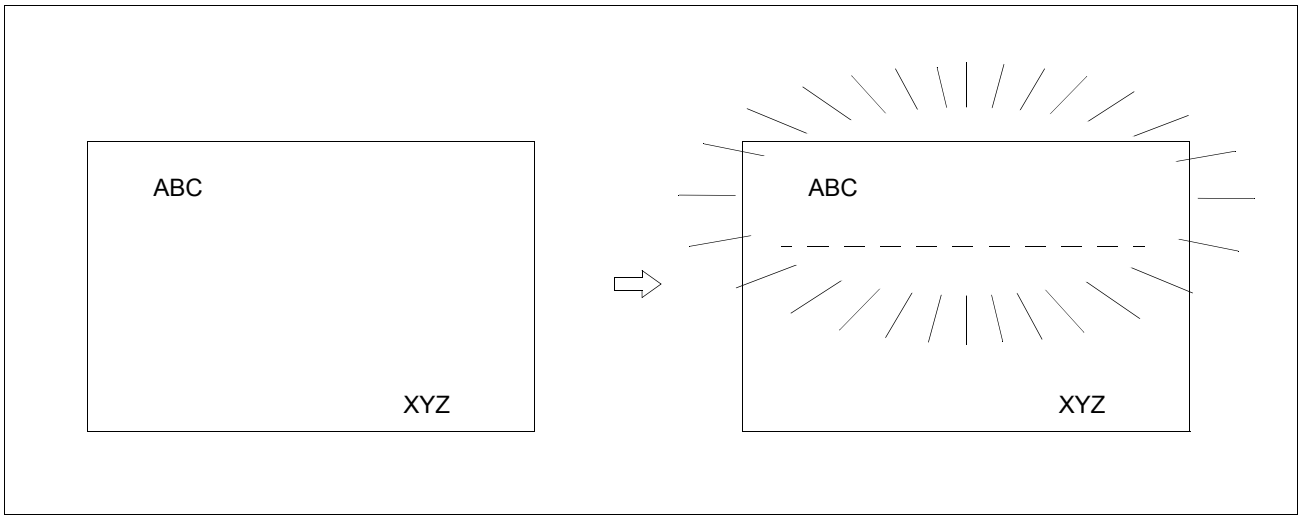


Figure 15-11 Flash Attribute for a Large Area

15.6 16x16-Dot Graphic Display

15.6.1 Command Usage

To display 16 × 16 pixel characters, use the following procedure.

1. Set the cursor address, REG[1Ch] - REG[1Dh]
2. Set the cursor shift direction, REG[17h] bits 1-0
3. Write to the display memory

15.6.2 Kanji Character Display

To write large characters, use the following procedure. For further information, see the flowchart in Figure 15-12 “Graphics Address Indexing,” on page 182.

1. Reads the character data from the CGRAM
2. Set the display address
3. Writes to the display memory

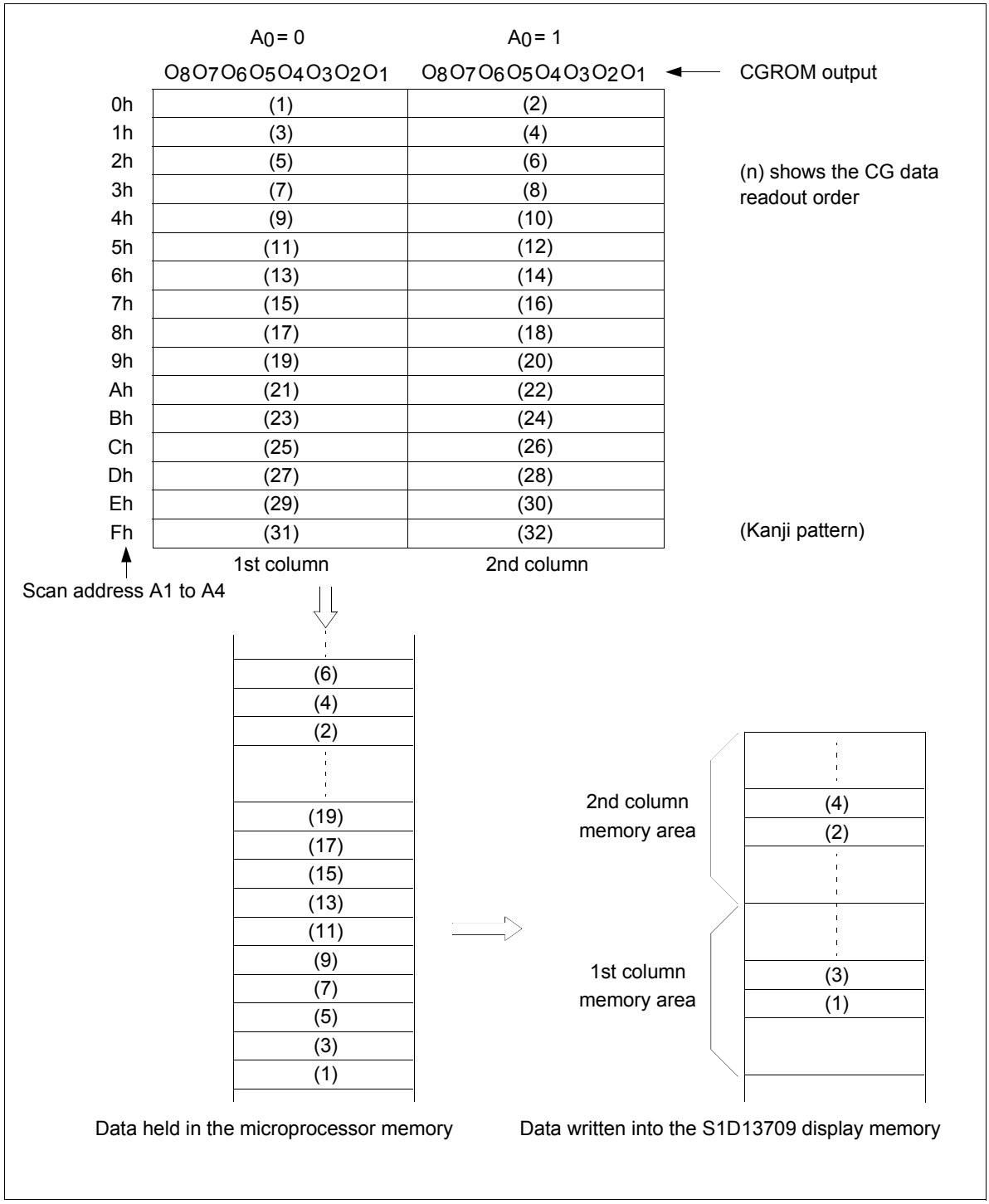


Figure 15-12 Graphics Address Indexing

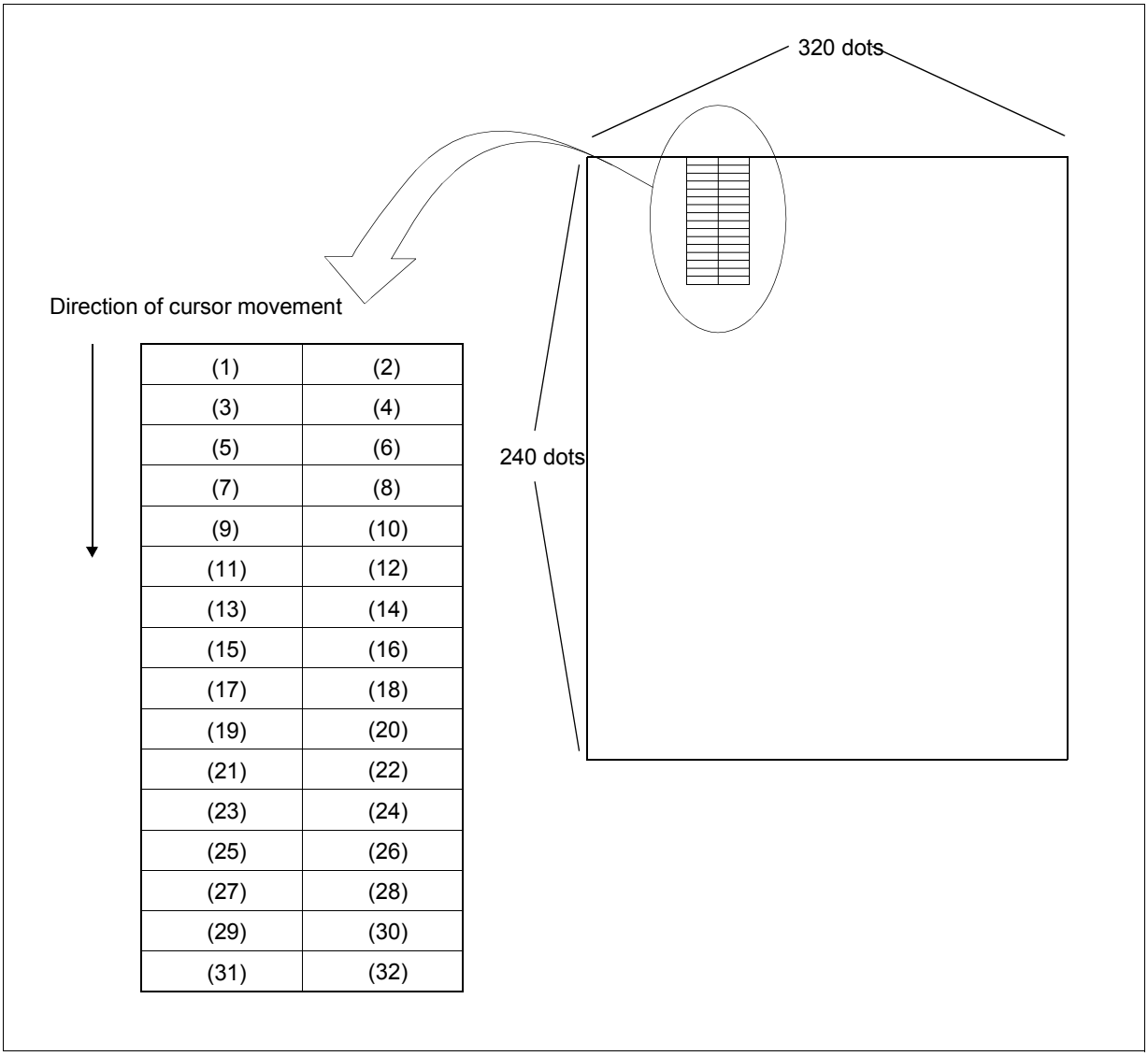
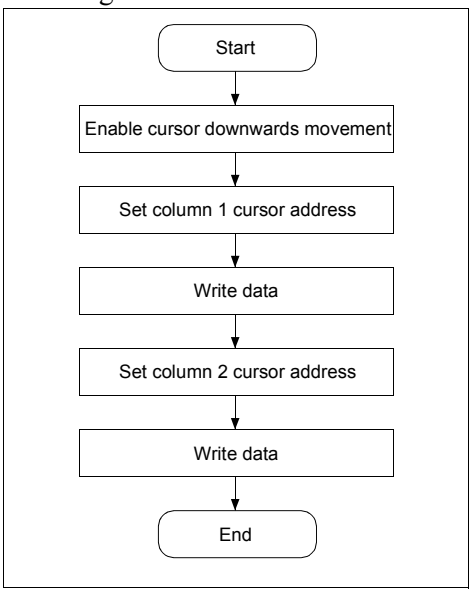


Figure 15-13 Graphics Bit Map

Using an external character generator RAM an 8 × 16 pixel font can be used, which allows a 16 × 16 pixel character to be displayed in two segments. The CGRAM data format is described in Figure 13 “Character Generator,” on page 141. This allows the display of up to 128, 16 × 16 pixel characters. If CGRAM is also used, 96 fixed characters and 32 bank-switchable characters are also be supported.

For Direct Addressing Mode



For Indirect Addressing Mode

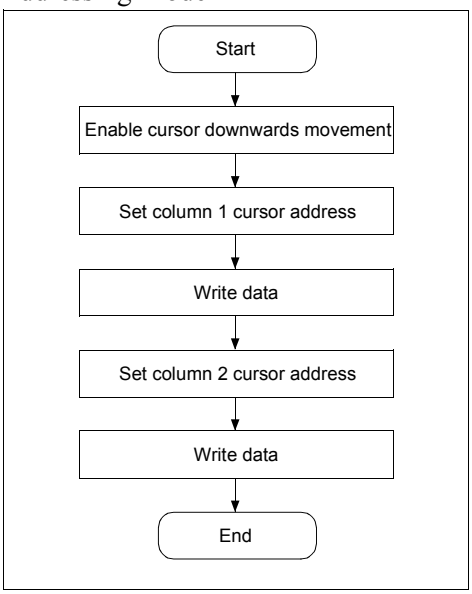


Figure 15-14 16 × 16-Dot Display Flowchart

16 Internal Character Generator Font

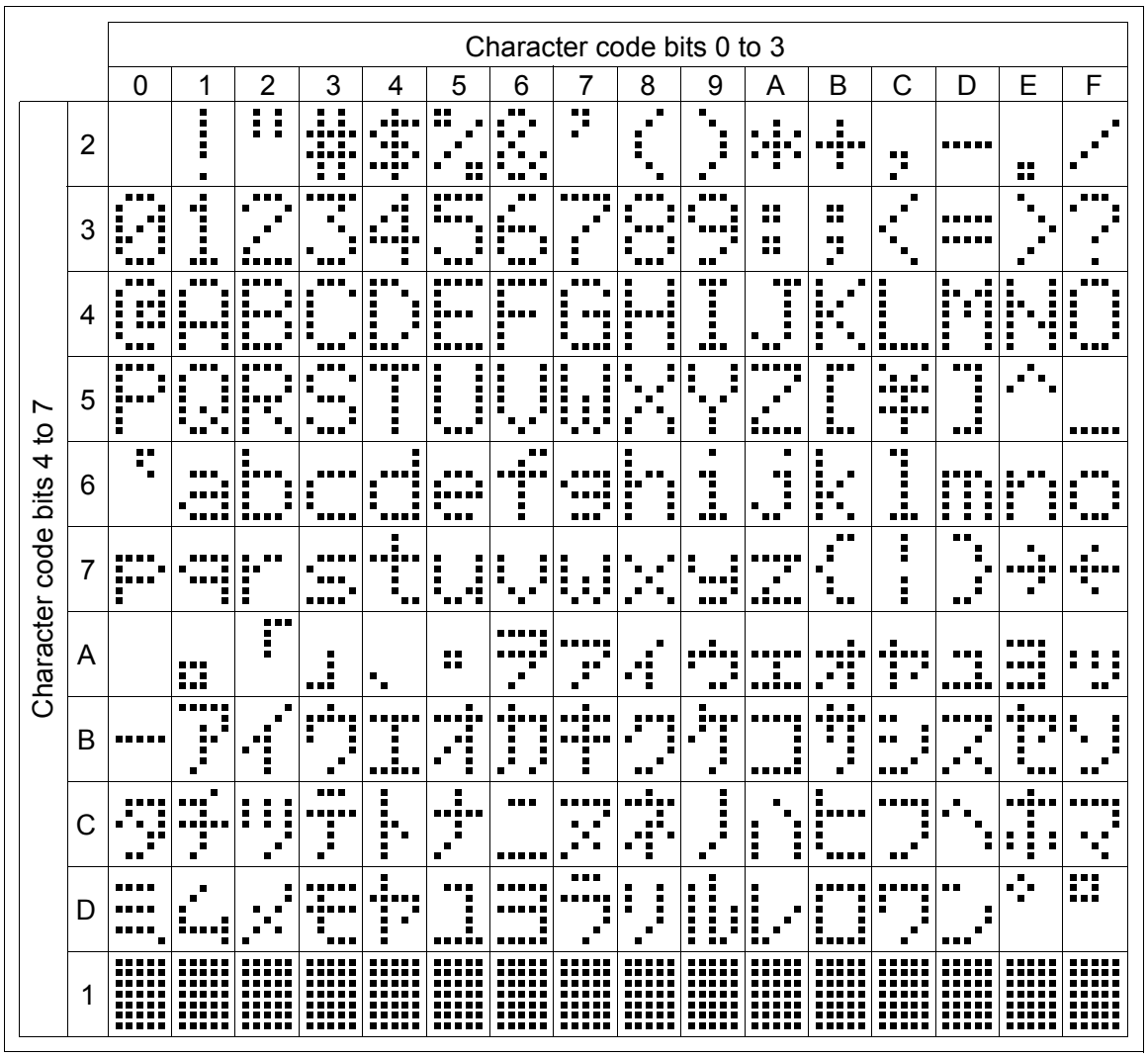


Figure 16-1 On-Chip Character Set

Note

The shaded positions indicate characters that have the whole 6 × 8 bitmap blackened.

17 Power Save Mode

The S1D13709 supports a power save mode that places it into a power efficient state. Power save mode is controlled by the Power Save Mode Enable bit, REG[08h] bit 0. The S1D13709 enters power save mode at least one or two blank frame after the enable bit is set.

The internal registers of the S1D13709 maintain their values during the power save state and the display memory control pins maintain their logic levels to ensure that the display memory is not corrupted.

The S1D13709 is removed from power save mode by writing a 0 the Power Save Mode Enable bit, REG[08h] bit 0.

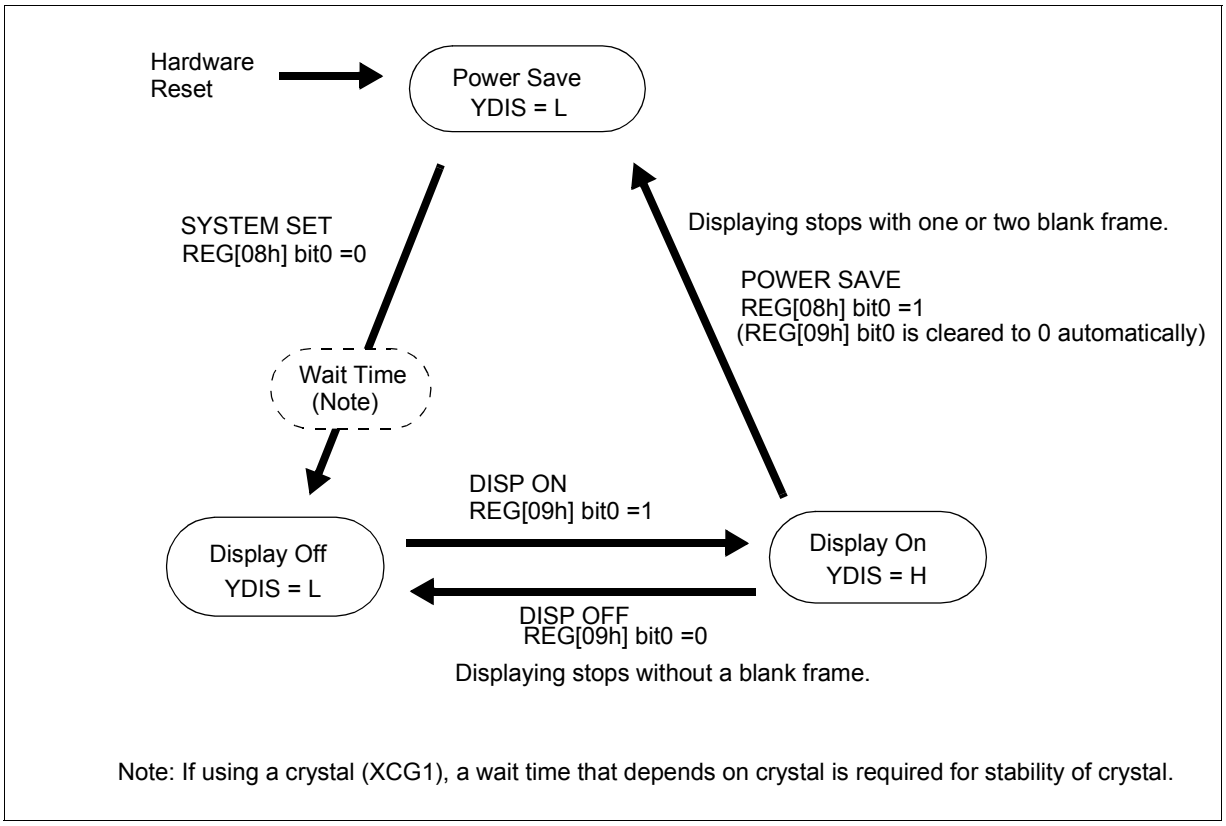


Figure 17-1 Power Save Mode State Sequence

For indirect addressing mode, the POWER SAVE command has no parameter bytes. For indirect addressing mode, the SYSTEM SET command exits power save mode.

1. The YDIS signal goes LOW between one and two frames after the power save command is received. Since YDIS forces all display driver outputs to go to the deselected output voltage, YDIS can be used as a power down signal for the LCD unit. This can be done by having YDIS turn off the relatively high power LCD drive supplies at the same time as it blanks the display.

2. Since all internal clocks in the S1D13709 are halted while power save mode is enabled, a DC voltage is applied to the LCD panel if the LCD drive supplies remain on. If reliability is a prime consideration, turn off the LCD drive supplies before issuing the power save command.

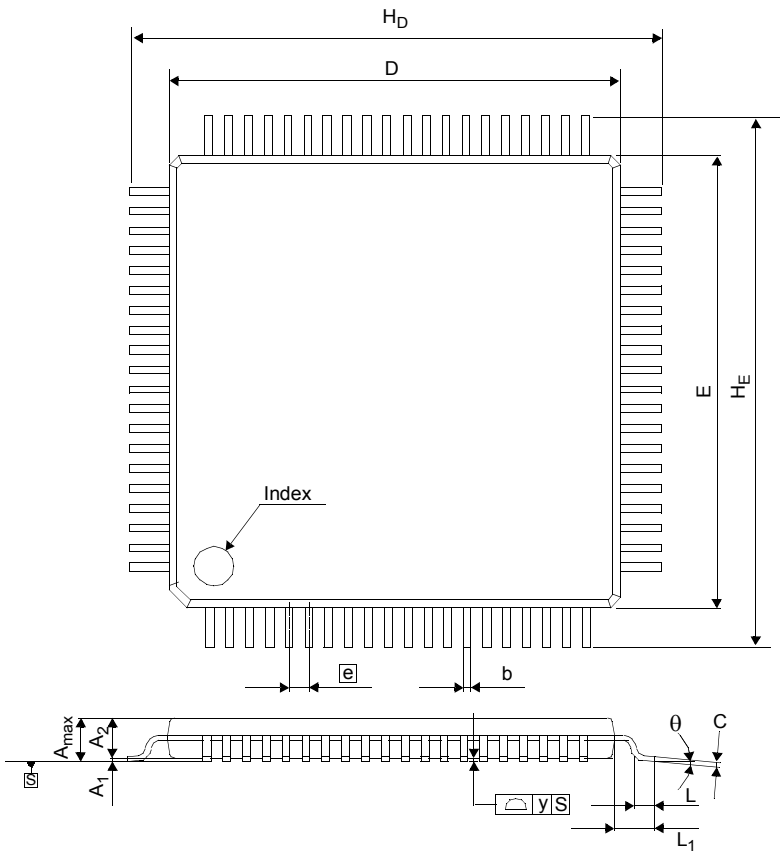
Table 17-1 State of LCD Pins and Crystal During Power Save Mode

LCD Pin	State During Power Save Mode	State During Display Off	State During Display On
YDIS	Low	Low	High
FPSHIFT (XSCL)	Low	Low or High	Active
FPFRAME (YD)	Low	Low	Active
FPLINE (LP)	Low	Low	Active
FPDRDY (MOD)	Low	Low	Active
FPDAT[5] (YSCL)	Low	Low	Active
FPDAT[4] (XECL)	Low	Low	Active
FPDAT[3:0]	Low	Low	Active
XCD1 / XCG1	Stopped	Running	Running

Table 17-2 Condition of Host Interface During Power Save Mode

LCD Pin	State During Power Save Mode	State During Display Off	State During Display On
Register access	Available	Available	Available
Display memory access	Not available	Available	Available

18 Mechanical Data



Symbol	Min.	Nom.	Max
E	—	12	—
D	—	12	—
A_{max}	—	—	1.2
A_1	—	0.1	—
A_2	—	1	—
e	—	0.5	—
b	0.17	—	0.27
c	0.09	—	0.2
θ	0°	—	8°
L	0.3	—	0.75
L_1	—	1	—
H_E	—	14	—
H_D	—	14	—
y	—	—	0.08

All dimensions in mm

Figure 18-1 Mechanical Drawing TQFP14 - 80 pin

19 Change Record

Revision 1.1 - Issued: March 16, 2018

- updated Sales and Technical Support Section
- updated some formatting

Revision 1.0- Issued: January 20, 2014

20 Sales and Technical Support

For more information on Epson Display Controllers, visit the Epson Global website.

https://global.epson.com/products_and_drivers/semicon/products/display_controllers/

For Sales and Technical Support, contact the Epson representative for your region.

https://global.epson.com/products_and_drivers/semicon/information/support.html