EVB-LAN9355

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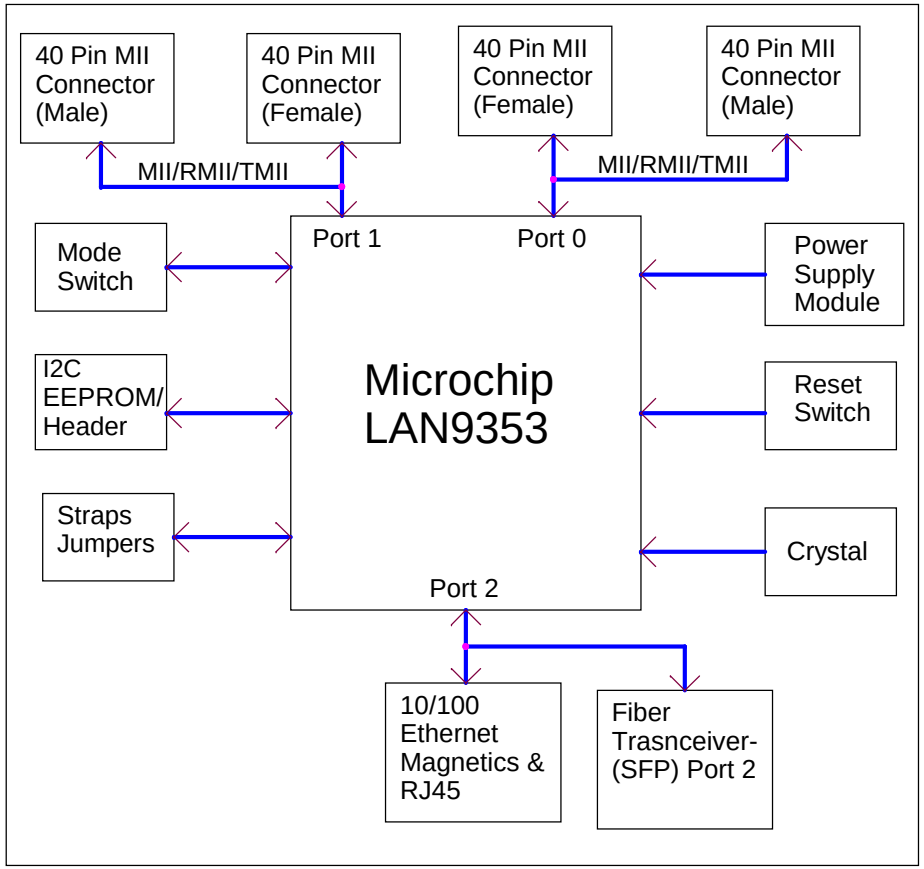
EVB-LAN9355 Block Diagram



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Part Number:	EVB-LAN9355	Page:	Block Diagram
Size: B	Project Name: LAN9355	Board Name:	EVB-LAN9355-REV-A
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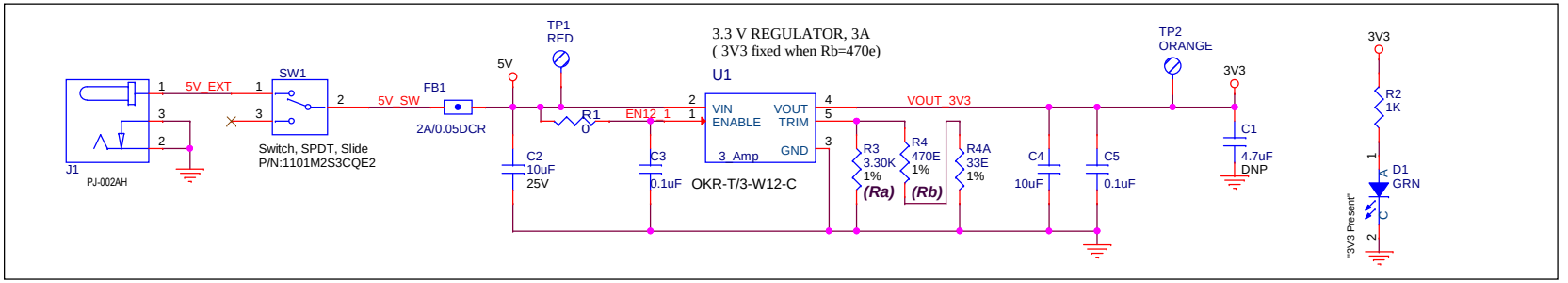
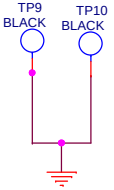
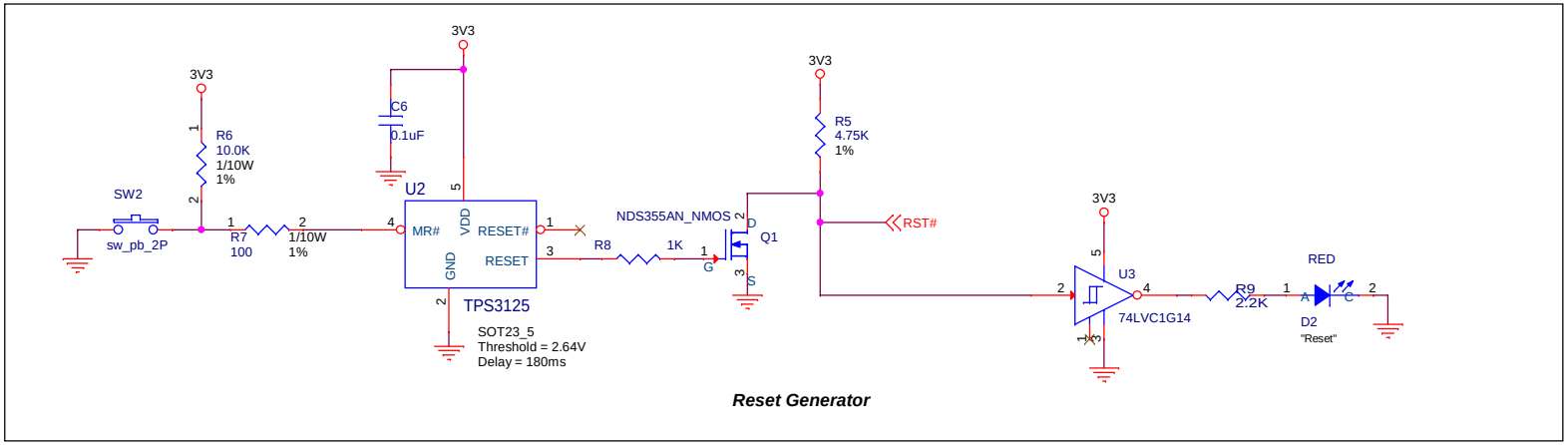
POWER SUPPLY







Reset Generator

Part Number:	EVB-LAN9355	Page:	Power Supply & RST
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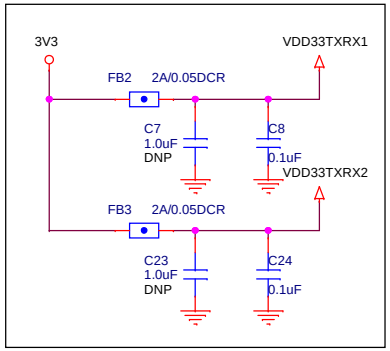

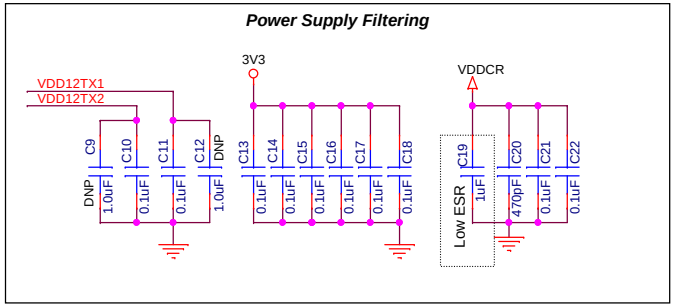

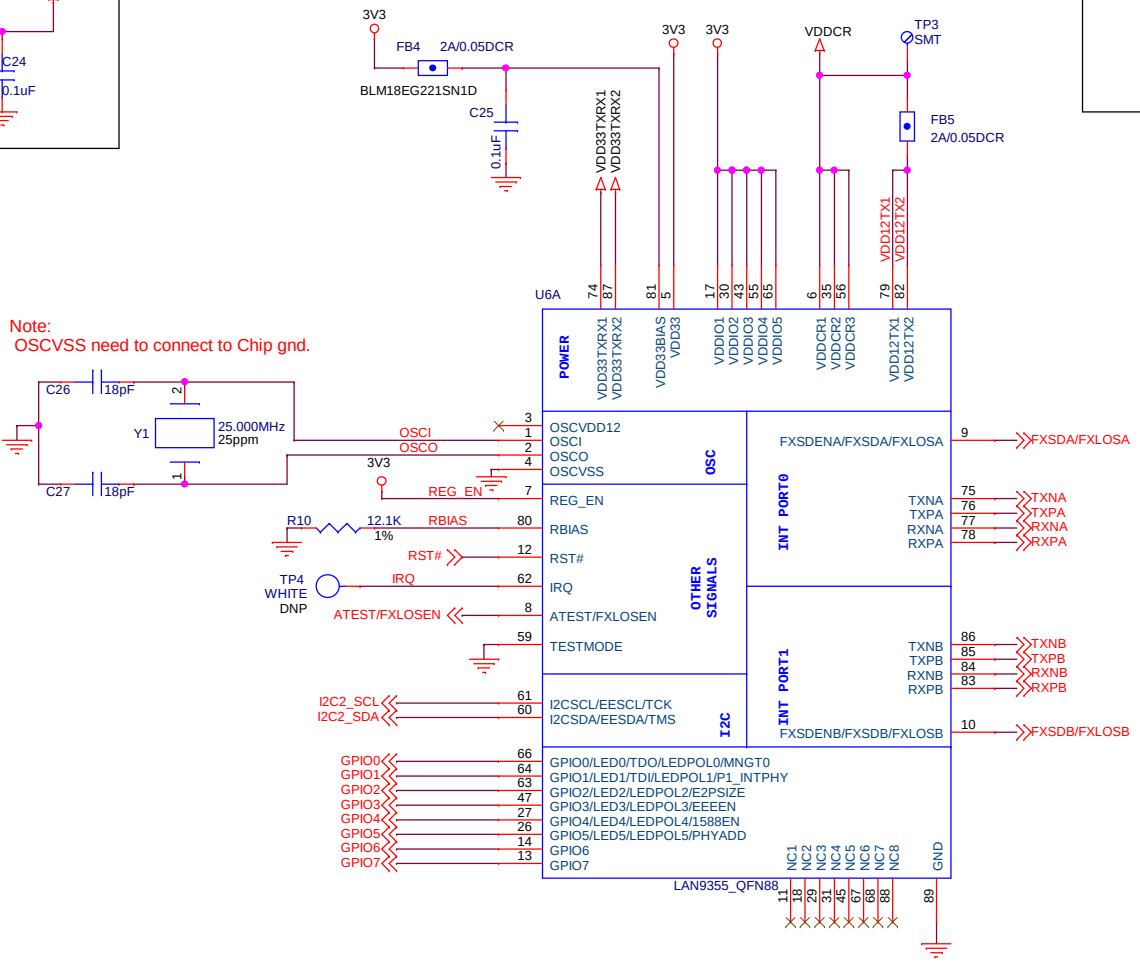

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Part Number:	EVB-LAN9355		Page:	LAN9355 (Part1)	
Size: B	Project Name:	LAN9355	Board Name:	EVB-LAN9355-REV-A	Rev A
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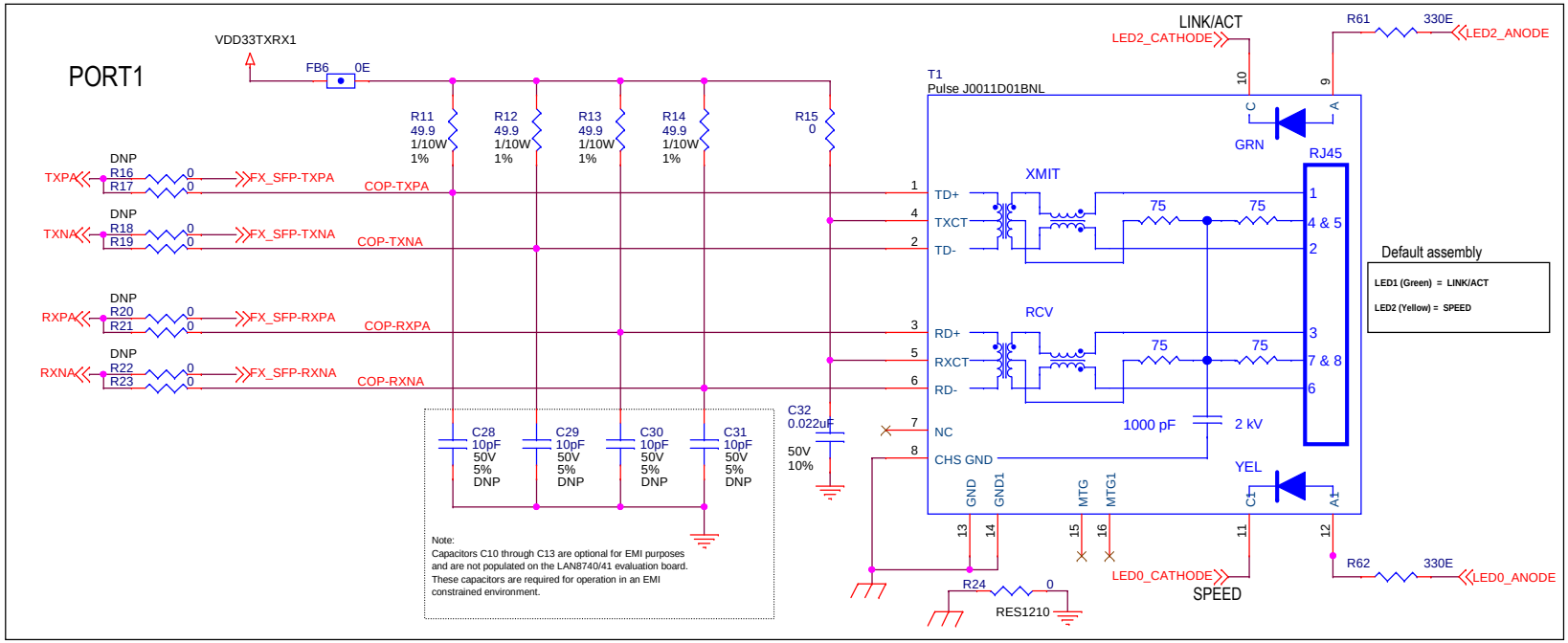

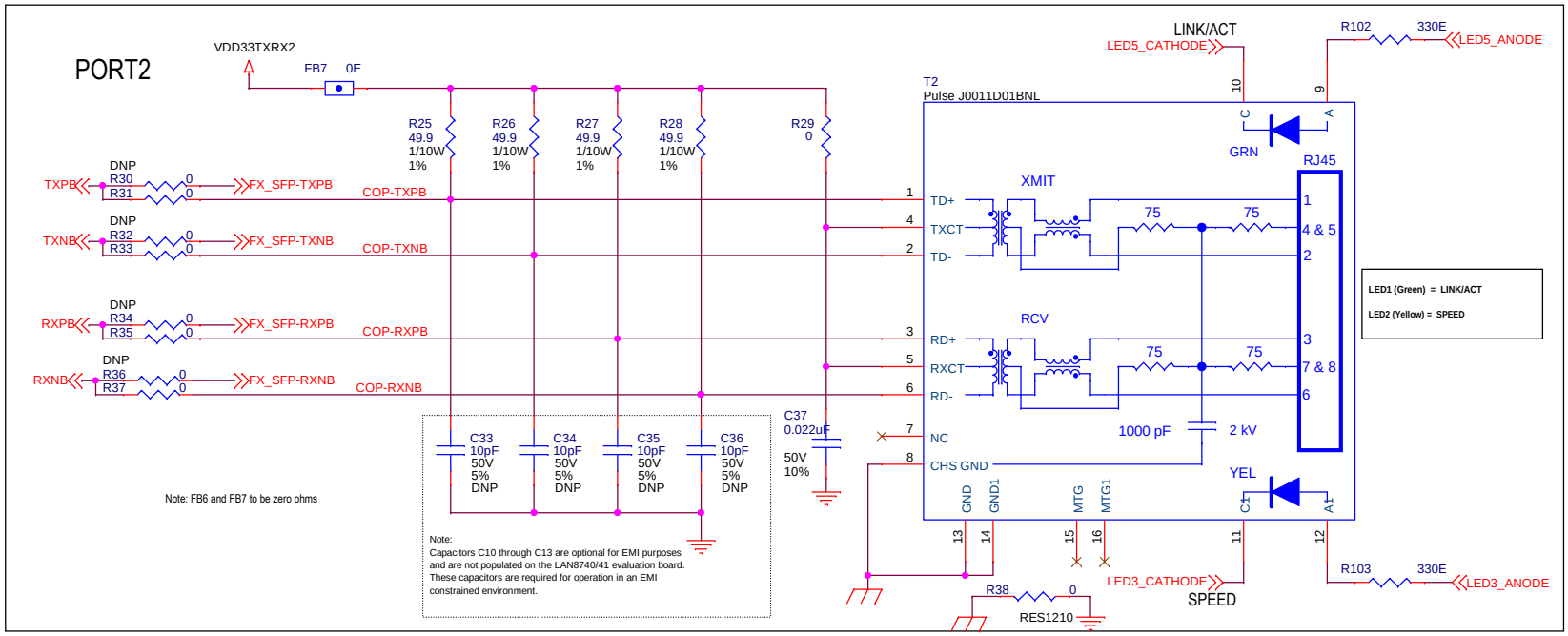

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Part Number:	EVB-LAN9355	Page:	Copper Mode Interface
Size: B	Project Name: LAN9355	Board Name:	EVB-LAN9355-REV-A
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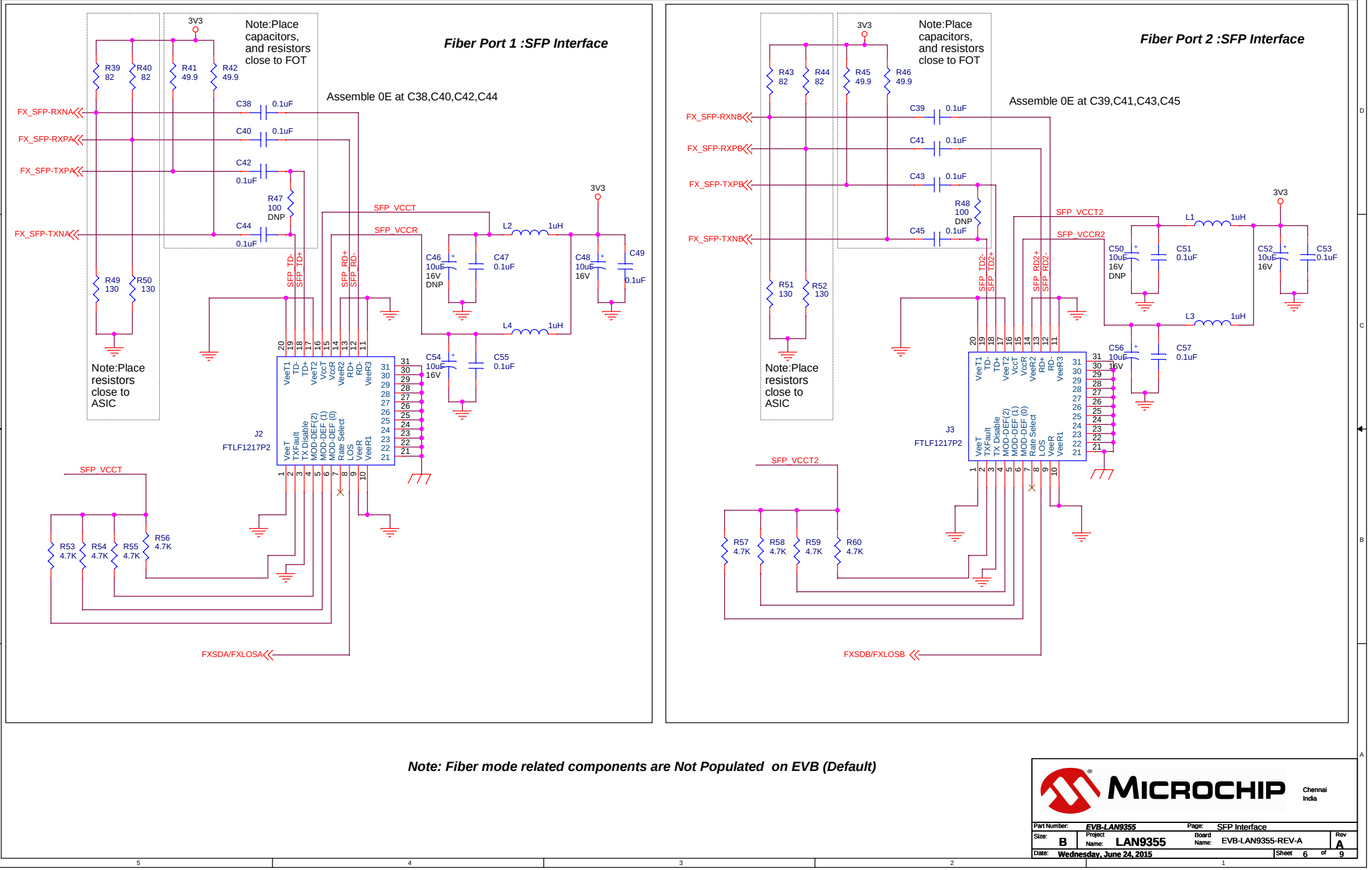

Note: Fiber mode related components are Not Populated on EVB (Default)

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Part Number:	EVB-LAN9355	Page:	SFP Interface
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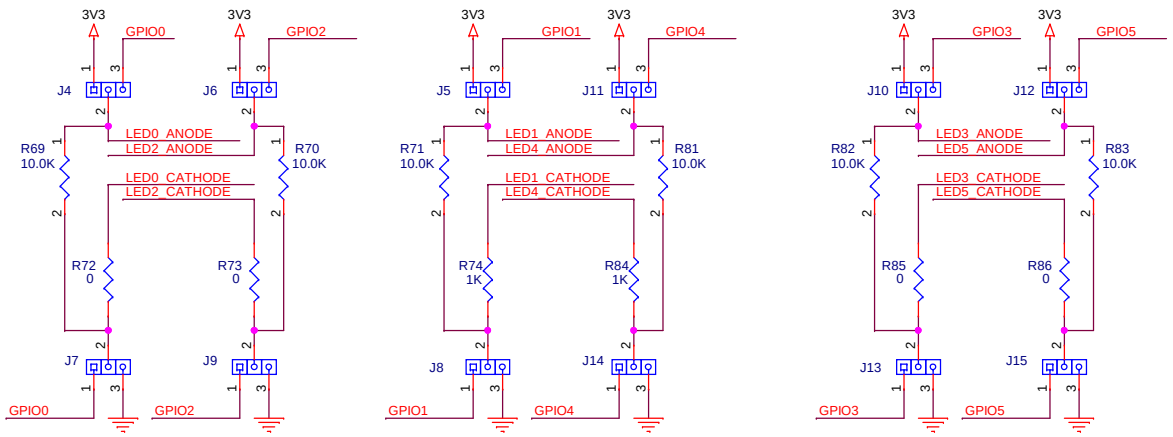
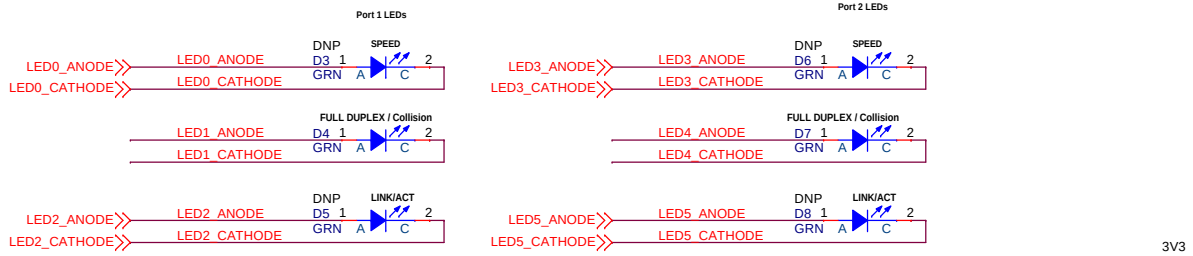
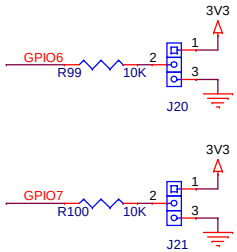
GPIO [0:5] & LED_POL_Strap

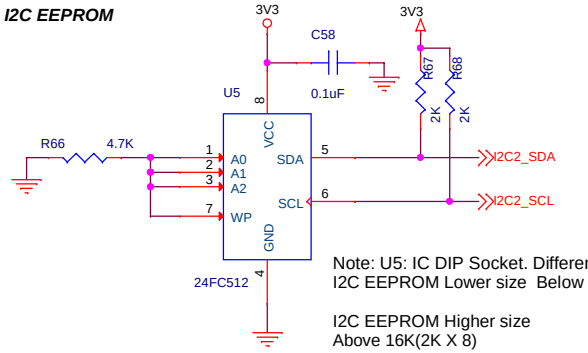






Strap Name	Logic	Connector	LED Polarity Strap
LED0/GPIO0/MNGT0	0	J4,J7 (2&3)	The LED is set as active high.
	1	J4,J7 (1&2) (Default)	The LED is set as active low,
LED1/GPIO1/ P1_INTPHY	0	J5,J8 (2&3) (Default)	The LED is set as active high.
	1	J5,J8 (1&2)	The LED is set as active low,
LED2/GPIO2/E2PSIZE	0	J6,J9 (2&3)	The LED is set as active high. EEPROM Size=1K bits (128 x 8) through 16K bits (2K x 8)
	1	J6,J9 (1&2) (Default)	The LED is set as active low, EEPROM Size=32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8) (LAN9252 only)
LED3/GPIO3/EEEEN	0	J10,J13 (2&3)	The LED is set as active high. EEE Disable
	1	J10,J13 (1&2) (Default)	The LED is set as active low, EEE Enable
LED4/GPIO4/1588EN	0	J11,J14 (2&3)	The LED is set as active high. 1588 Disable
	1	J11,J14 (1&2) (Default)	The LED is set as active low, 1588 Enable
LED5/GPIO5/PHYADD	0	J12,J15 (2&3) (Default)	The LED is set as active high. PHYADD=0,1,2
	1	J12,J15 (1&2)	The LED is set as active low, PHYADD =1,2,3

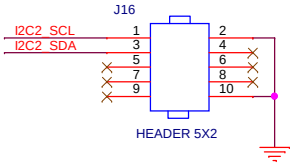
I2C EEPROM



Note: U5: IC DIP Socket. Different sizes can be mounted
I2C EEPROM Lower size Below 16K(2K X 8)

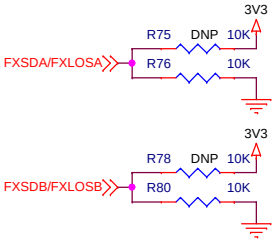
I2C EEPROM Higher size
Above 16K(2K X 8)
[Default-512KBIT]

Aardvark - I2C Connector



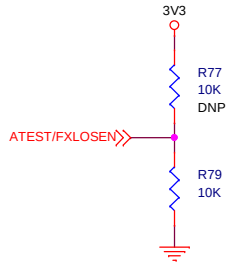
FX_Mode_Strap_1 & 2

PORT	MODE	Poupulate
PORT1	Copper (Default)	R76
	Fiber	R75
PORT2	Copper (Default)	R80
	Fiber	R78



FX_Los_Strap_1 & 2

R77	R79	Ref.Voltage	Function
Poupulate	DNP	3V3	Above 2 V selects FX-LOS for ports 1 and 2
Poupulate	Poupulate	1V5	Level of 1.5 V selects FX-LOS for port 1 and FX-SD/copper twisted pair for port 2 further determined by FXSDB
DNP (Default)	Poupulate (Default)	0 (Default)	Level of 0V Selects FX-SD / copper twisted pair for ports A and B further determined by FXSDA and FXSDB.



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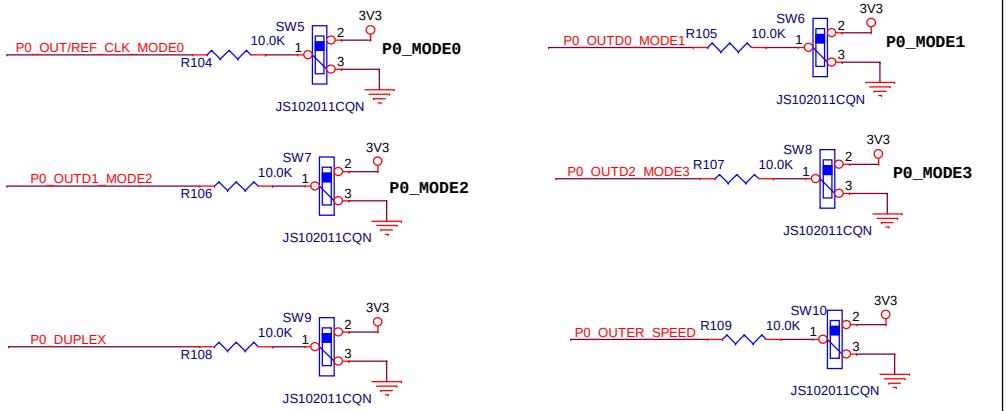
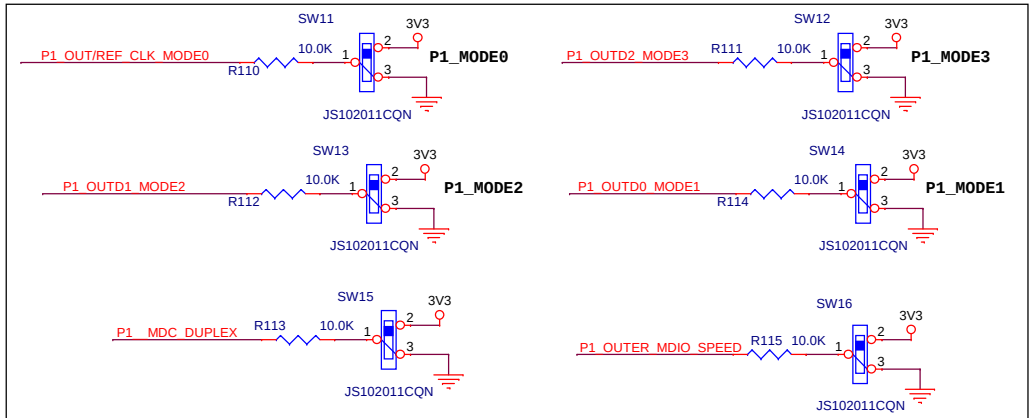


Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa .

PORT 0 MODE STRAP MAPPING

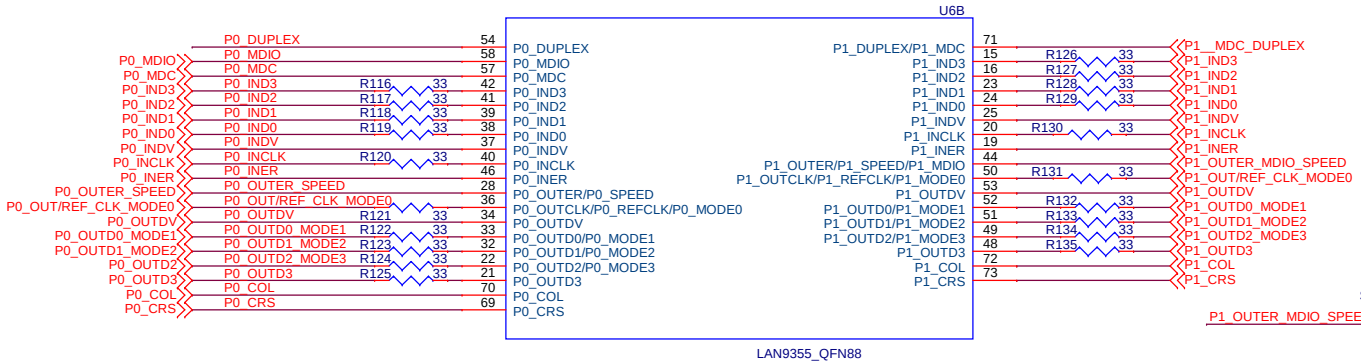
P1_INTPHY (J5 & J8)	P0_MODE3 (SW8)	P0_MODE2 (SW7)	P0_MODE1 (SW6)	P0_MODE0 (SW5)	Port 0 Mode
x	0	0	x	x	MII MAC (Default)
x	0	1	0	x	MII PHY
x	0	1	1	0	Turbo MII PHY 12 ma
x	0	1	1	1	Turbo MII PHY 16 ma
x	1	0	0	x	RMII MAC clock in
x	1	0	1	0	RMII MAC clock out 12ma
x	1	0	1	1	RMII MAC clock out 16ma
x	1	1	0	x	RMII PHY clock in
x	1	1	1	0	RMII PHY clock out 12ma
x	1	1	1	1	RMII PHY clock out 16ma

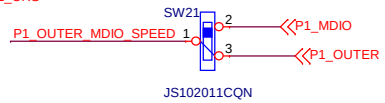


Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa .

PORT 1 MODE STRAP MAPPING

P1_INTPHY (J5 & J8)	P1_MODE3 (SW12)	P1_MODE2 (SW13)	P1_MODE1 (SW14)	P1_MODE0 (SW11)	Port 1 Mode
0	0	0	x	x	MII MAC (Default)
0	0	1	0	x	MII PHY
0	0	1	1	0	Turbo MII PHY 12 ma
0	0	1	1	1	Turbo MII PHY 16 ma
0	1	0	0	x	RMII MAC clock in
0	1	0	1	0	RMII MAC clock out 12ma
0	1	0	1	1	RMII MAC clock out 16ma
0	1	1	0	x	RMII PHY clock in
0	1	1	1	0	RMII PHY clock out 12ma
0	1	1	1	1	RMII PHY clock out 16ma
1	x	x	x	x	Internal PHY





P1 MDIO or OUTER selection switch Default (1-2)

Emulated Link Partner Default Advertised Ability

SW9 (P0_DUPLEX) / SW15 (P1_DUPLEX)	SW10 (P0_SPEED) / SW16 (P1_SPEED)	ADVERTISED LINK PARTNER ABILITY (Bits 8,7,6,5)
1	0	10BASE-T full-duplex (0010)
1	1	100BASE-X full-duplex (1000) (Default)
0	0	10BASE-T half-duplex (0001)
0	1	100BASE-X half-duplex (0100)

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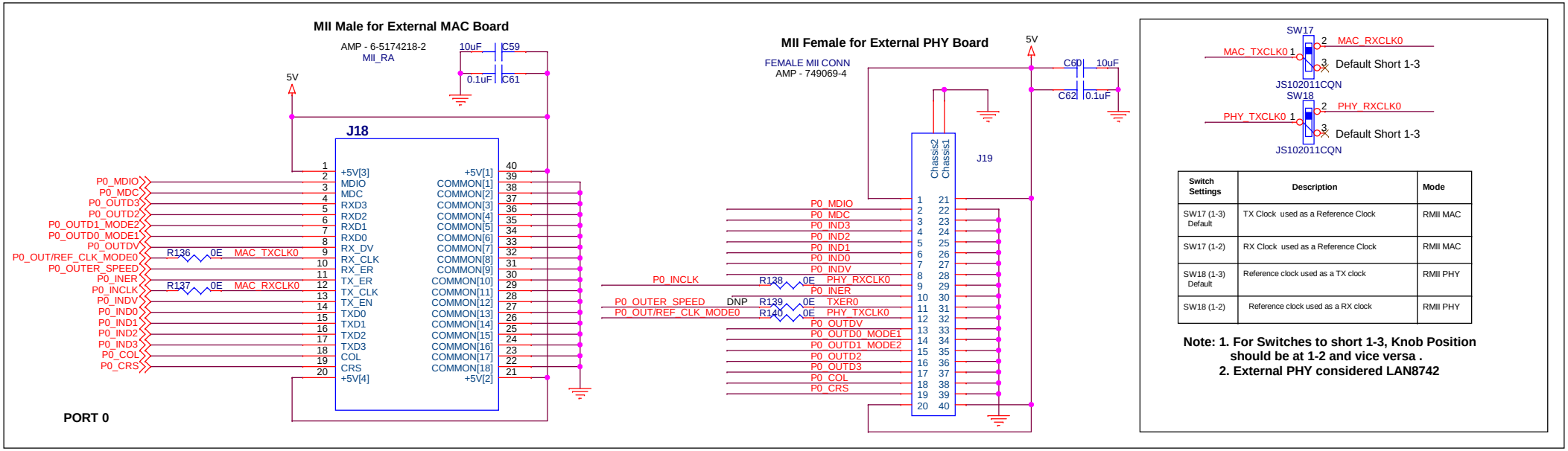
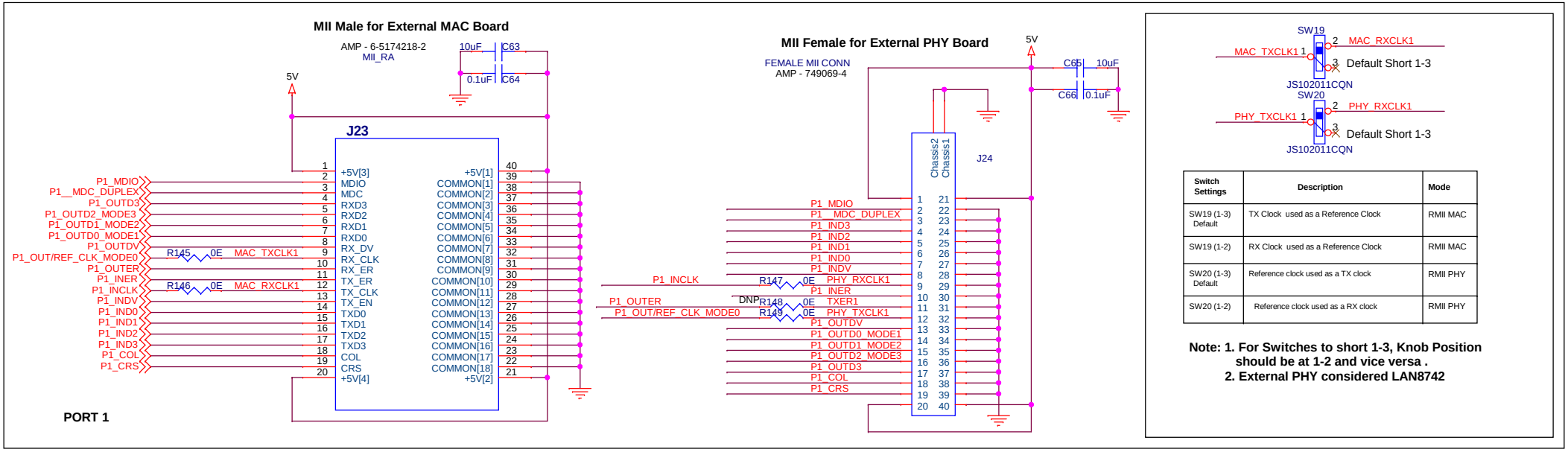


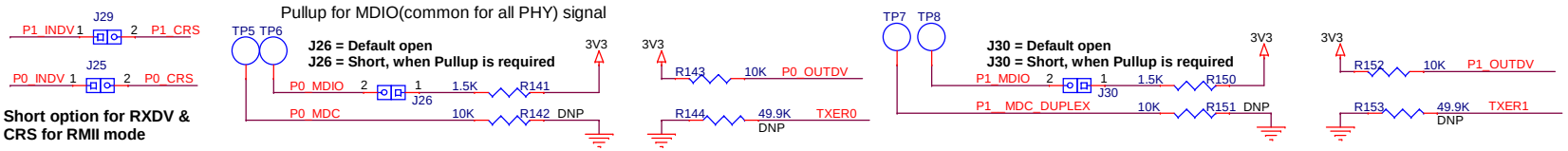
Switch Settings	Description	Mode
SW17 (1-3) Default	TX Clock used as a Reference Clock	RMII MAC
SW17 (1-2)	RX Clock used as a Reference Clock	RMII MAC
SW18 (1-3) Default	Reference clock used as a TX clock	RMII PHY
SW18 (1-2)	Reference clock used as a RX clock	RMII PHY

Note: 1. For Switches to short 1-3, Knob Position should be at 1-2 and vice versa .
2. External PHY considered LAN8742



Switch Settings	Description	Mode
SW19 (1-3) Default	TX Clock used as a Reference Clock	RMII MAC
SW19 (1-2)	RX Clock used as a Reference Clock	RMII MAC
SW20 (1-3) Default	Reference clock used as a TX clock	RMII PHY
SW20 (1-2)	Reference clock used as a RX clock	RMII PHY

Note: 1. For Switches to short 1-3, Knob Position should be at 1-2 and vice versa .
2. External PHY considered LAN8742



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