

## 250V Low Charge Injection 8-Channel High Voltage Analog Switch

### Features

- ▶ HVCMOS® technology for high performance
- ▶ Very low quiescent power dissipation -10µA
- ▶ Low parasitic capacitances
- ▶ DC to 10MHz analog signal frequency
- ▶ -60dB typical output off isolation at 5MHz
- ▶ -60dB typical off-isolation at 5MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ On-chip shift register, latch and clear logic circuitry
- ▶ Flexible high voltage supplies
- ▶ Surface mount packages

### Applications

- ▶ Medical ultrasound imaging
- ▶ Non-destructive evaluation
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

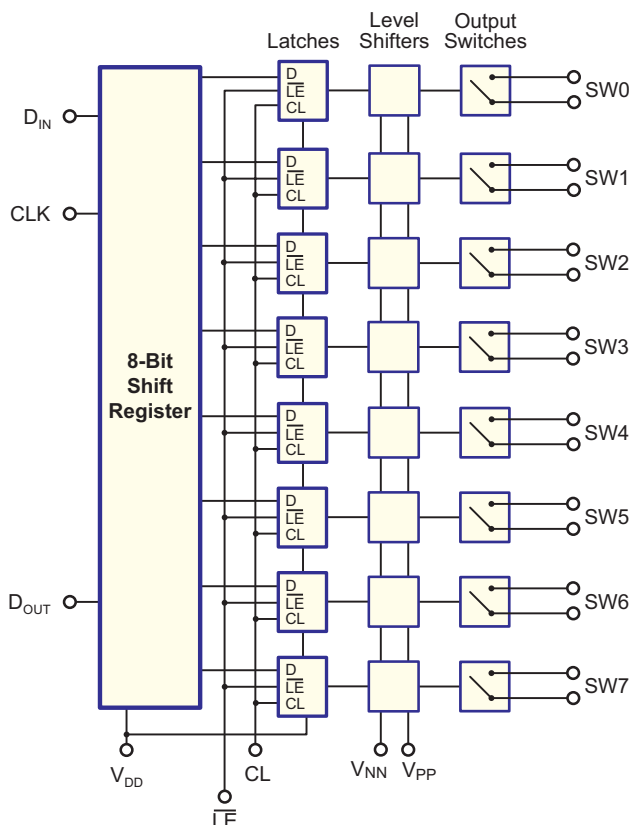
### General Description

The Supertex HV214 is a low charge injection 8-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers, inkjet printer heads and optical MEMS modules.

Input data is shifted into an 8-bit shift register that can then be retained in an 8-bit latch. To reduce any possible clock feedthrough noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS® technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-210V, +125V/-125V, +210V/-40V.

### Block Diagram



## Ordering Information

| Package Options |              |                          |
|-----------------|--------------|--------------------------|
| Device          | 28-Lead PLCC | 48-Lead LQFP/TQFP(1.4mm) |
| HV214           | HV214PJ      | HV214FG                  |
|                 | HV214PJ-G    | HV214FG-G                |

-G indicates the part is RoHS compliant (Green)



## Absolute Maximum Ratings

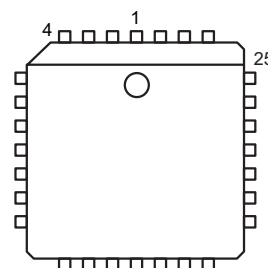
| Parameter                             | Value                    |
|---------------------------------------|--------------------------|
| $V_{DD}$ logic power supply voltage   | -0.5V to +15V            |
| $V_{PP} - V_{NN}$ supply voltage      | 260V                     |
| $V_{PP}$ positive high voltage supply | -0.5V to $V_{NN} + 250V$ |
| $V_{NN}$ negative high voltage supply | +0.5V to -260V           |
| Logic input voltages                  | -0.5V to $V_{DD} + 0.3V$ |
| Analog signal range                   | $V_{NN}$ to $V_{PP}$     |
| Peak analog signal current/channel    | 2.5A                     |
| Storage temperature                   | -65°C to +150°C          |
| Power dissipation:                    |                          |
| 28-Lead PLCC                          | 1.2W                     |
| 48-Lead LQFP/ TQFP (1.4mm)            | 1.0W                     |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

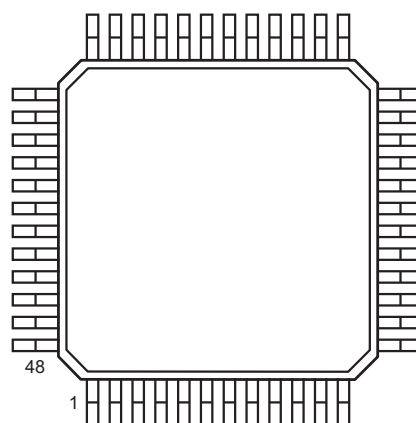
## Operating Conditions

| Symbol    | Parameter                          | Value                            |
|-----------|------------------------------------|----------------------------------|
| $V_{DD}$  | Logic power supply voltage         | 4.5V to 13.2V                    |
| $V_{PP}$  | Positive high voltage supply       | 40V to $V_{NN} + 250V$           |
| $V_{NN}$  | Negative high voltage supply       | -40V to -210V                    |
| $V_{IH}$  | High level input logic voltage     | $V_{DD} - 1.5V$ to $V_{DD}$      |
| $V_{IL}$  | Low-level input logic voltage      | 0V to 1.5V                       |
| $V_{SIG}$ | Analog signal voltage peak-to-peak | $V_{NN} + 10V$ to $V_{PP} - 10V$ |
| $T_A$     | Operating free air temperature     | 0°C to 70°C                      |

## Pin Configurations



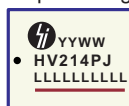
28-Lead (J) PLCC (PJ)  
(top view)



48-Lead LQFP (FG)  
(7x7x1.4mm)  
(top view)

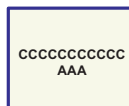
## Product Marking

Top Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
C = Country of Origin  
A = Assembler ID\*  
— = "Green" Packaging

Bottom Marking



\*May be part of top marking

28-Lead PLCC (PJ)

Top Marking



YY = Year Sealed  
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— = "Green" Packaging

Bottom Marking



\*May be part of top marking

48-Lead LQFP (FG)

**DC Electrical Characteristics** ( $T_A = 25^\circ\text{C}$ , over recommended operating conditions unless otherwise noted)

| Sym                     | Parameter                                  | Min | Typ | Max  | Units            | Conditions                                                                                      |
|-------------------------|--------------------------------------------|-----|-----|------|------------------|-------------------------------------------------------------------------------------------------|
| $R_{\text{ONS}}$        | Small signal switch on-resistance          | -   | -   | 55   | $\Omega$         | $I_{\text{SIG}} = 5.0\text{mA}$ $V_{\text{PP}} = +40\text{V}$                                   |
|                         |                                            | -   | -   | 49   |                  | $I_{\text{SIG}} = 200\text{mA}$ $V_{\text{NN}} = -160\text{V}$                                  |
|                         |                                            | -   | -   | 42   |                  | $I_{\text{SIG}} = 5.0\text{mA}$ $V_{\text{PP}} = +125\text{V}$                                  |
|                         |                                            | -   | -   | 36   |                  | $I_{\text{SIG}} = 200\text{mA}$ $V_{\text{NN}} = -100\text{V}$                                  |
|                         |                                            | -   | -   | 38   |                  | $I_{\text{SIG}} = 5.0\text{mA}$ $V_{\text{PP}} = +210\text{V}$                                  |
|                         |                                            | -   | -   | 32   |                  | $I_{\text{SIG}} = 200\text{mA}$ $V_{\text{NN}} = -40\text{V}$                                   |
| $\Delta R_{\text{ONS}}$ | Small signal switch On-resistance matching | -   | -   | 20   | %                | $I_{\text{SIG}} = 5\text{mA}$ , $V_{\text{PP}} = +125\text{V}$ , $V_{\text{NN}} = -125\text{V}$ |
| $R_{\text{ONL}}$        | Large signal switch On-resistance          | -   | 23  | -    | $\Omega$         | $V_{\text{SIG}} = V_{\text{PP}} - 10\text{V}$ , $I_{\text{SIG}} = 1\text{A}$                    |
| $I_{\text{SOL}}$        | Switch off leakage per switch              | -   | -   | 10   | $\mu\text{A}$    | $V_{\text{SIG}} = V_{\text{PP}} - 10\text{V}$ & $V_{\text{NN}} + 10\text{V}$                    |
|                         | DC offset switch off                       | -   | -   | 300  | mV               | $R_{\text{LOAD}} = 100\text{K}\Omega$                                                           |
|                         | DC offset switch on                        | -   | -   | 500  | mV               | $R_{\text{LOAD}} = 100\text{K}\Omega$                                                           |
| $I_{\text{PPQ}}$        | Quiescent $V_{\text{PP}}$ supply current   | -   | -   | 50   | $\mu\text{A}$    | All switches off                                                                                |
| $I_{\text{NNQ}}$        | Quiescent $V_{\text{NN}}$ supply current   | -   | -   | -50  | $\mu\text{A}$    | All switches off                                                                                |
| $I_{\text{PPQ}}$        | Quiescent $V_{\text{PP}}$ supply current   | -   | -   | 50   | $\mu\text{A}$    | All switches on, $I_{\text{SW}} = 5.0\text{mA}$                                                 |
| $I_{\text{NNQ}}$        | Quiescent $V_{\text{NN}}$ supply current   | -   | -   | -50  | $\mu\text{A}$    | All switches on, $I_{\text{SW}} = 5.0\text{mA}$                                                 |
|                         | Switch output peak current                 | -   | -   | 2.0  | A                | $V_{\text{SIG}}$ duty cycle 0.1%                                                                |
| $f_{\text{SW}}$         | Output switch frequency                    | -   | -   | 50   | kHz              | Duty cycle = 50%                                                                                |
| $I_{\text{PP}}$         | Average $V_{\text{PP}}$ supply current     | -   | -   | 7.0  | mA               | $V_{\text{PP}} = +40\text{V}$<br>$V_{\text{NN}} = -160\text{V}$                                 |
|                         |                                            | -   | -   | 5.0  |                  | $V_{\text{PP}} = +100\text{V}$<br>$V_{\text{NN}} = -100\text{V}$                                |
|                         |                                            | -   | -   | 5.0  |                  | $V_{\text{PP}} = +160\text{V}$<br>$V_{\text{NN}} = -40\text{V}$                                 |
| $I_{\text{NN}}$         | Average $V_{\text{NN}}$ supply current     | -   | -   | -7.0 | mA               | $V_{\text{PP}} = +40\text{V}$<br>$V_{\text{NN}} = -160\text{V}$                                 |
|                         |                                            | -   | -   | -5.0 |                  | $V_{\text{PP}} = +100\text{V}$<br>$V_{\text{NN}} = -100\text{V}$                                |
|                         |                                            | -   | -   | -5.0 |                  | $V_{\text{PP}} = +160\text{V}$<br>$V_{\text{NN}} = -40\text{V}$                                 |
| $I_{\text{DD}}$         | Average $V_{\text{DD}}$ supply current     | -   | -   | 10   | mA               | $f_{\text{CLK}} = 5\text{MHz}$ , $V_{\text{DD}} = 5.0\text{V}$                                  |
| $I_{\text{DDQ}}$        | Quiescent $V_{\text{DD}}$ supply current   | -   | -   | 4.0  | $\mu\text{A}$    | ---                                                                                             |
| $I_{\text{SOR}}$        | Data out source current                    | 45  | -   | -    | mA               | $V_{\text{OUT}} = V_{\text{DD}} - 0.7\text{V}$                                                  |
| $I_{\text{SINK}}$       | Data out sink current                      | 45  | -   | -    | mA               | $V_{\text{OUT}} = 0.7\text{V}$                                                                  |
| $C_{\text{IN}}$         | Large input capacitance                    | -   | -   | 10   | pF               | ---                                                                                             |
| $T_A$                   | Ambient temperature range                  | 0   | -   | 70   | $^\circ\text{C}$ | ---                                                                                             |

**AC Electrical Characteristics** ( $V_{DD} = 5.0V$ ,  $T_A = 25^\circ C$ , over recommended operating conditions unless otherwise noted)

| Sym           | Parameter                                | Min | Typ | Max | Units   | Conditions                                                  |
|---------------|------------------------------------------|-----|-----|-----|---------|-------------------------------------------------------------|
| $t_{SD}$      | Set-up time before $\overline{LE}$ rises | 150 | -   | -   | ns      | ---                                                         |
| $t_{WLE}$     | Time width of $\overline{LE}$            | 150 | -   | -   | ns      | ---                                                         |
| $t_{DO}$      | Clock delay time to data out             | -   | -   | 150 | ns      | ---                                                         |
| $t_{WCL}$     | Time width of CL                         | 150 | -   | -   | ns      | ---                                                         |
| $t_{SU}$      | Set-up time data to clock                | 15  | 8.0 | -   | ns      | ---                                                         |
| $t_H$         | Hold time data from clock                | 35  | -   | -   | ns      | ---                                                         |
| $f_{CLK}$     | Clock frequency                          | -   | -   | 5.0 | MHz     | 50% duty cycle, $f_{DATA} = f_{CLK}/2$                      |
| $t_R, t_F$    | Clock rise and fall times                | -   | -   | 50  | ns      | ---                                                         |
| $T_{ON}$      | Turn-on time                             | -   | -   | 5.0 | $\mu s$ | $V_{SIG} = V_{PP} - 10V$ , $R_{LOAD} = 10K\Omega$           |
| $T_{OFF}$     | Turn-off time                            | -   | -   | 5.0 | $\mu s$ | $V_{SIG} = V_{PP} - 10V$ , $R_{LOAD} = 10K\Omega$           |
| dv/dt         | Maximum $V_{SIG}$ slew rate              | -   | -   | 20  | V/ns    | $V_{PP} = +40V$ , $V_{NN} = -160V$                          |
|               |                                          | -   | -   | 20  |         | $V_{PP} = +125V$ , $V_{NN} = -100V$                         |
|               |                                          | -   | -   | 20  |         | $V_{PP} = +210V$ , $V_{NN} = -40V$                          |
| KO            | Off isolation                            | -30 | -   | -   | dB      | $F = 5MHz$ ,<br>1K $\Omega$ /15pF load                      |
|               |                                          | -58 | -   | -   |         | $F = 5MHz$ , 50 $\Omega$ load                               |
| $K_{CR}$      | Switch crosstalk                         | -60 | -   | -   | dB      | $F = 5MHz$ , 50 $\Omega$ load                               |
| $I_{ID}$      | Output switch isolation diode current    | -   | -   | 300 | mA      | 300ns pulse width, 2% duty cycle                            |
| $C_{SG(OFF)}$ | Off capacitance SW to GND                | 5.0 | 12  | 17  | pF      | 0V, $f = 1MHz$                                              |
| $C_{SG(ON)}$  | On capacitance SW to GND                 | 25  | 38  | 50  | pF      | 0V, $f = 1MHz$                                              |
| $+V_{SPK}$    | Output voltage spike                     | -   | -   | 200 | mV      | $V_{PP} = +40V$ , $V_{NN} = -210V$ , $R_{LOAD} = 50\Omega$  |
| $-V_{SPK}$    |                                          | -   | -   | 200 |         |                                                             |
| $+V_{SPK}$    |                                          | -   | -   | 200 |         | $V_{PP} = +100V$ , $V_{NN} = -125V$ , $R_{LOAD} = 50\Omega$ |
| $-V_{SPK}$    |                                          | -   | -   | 200 |         |                                                             |
| $+V_{SPK}$    |                                          | -   | -   | 200 |         | $V_{PP} = +160V$ , $V_{NN} = -40V$ , $R_{LOAD} = 50\Omega$  |
| $-V_{SPK}$    |                                          | -   | -   | 200 |         |                                                             |

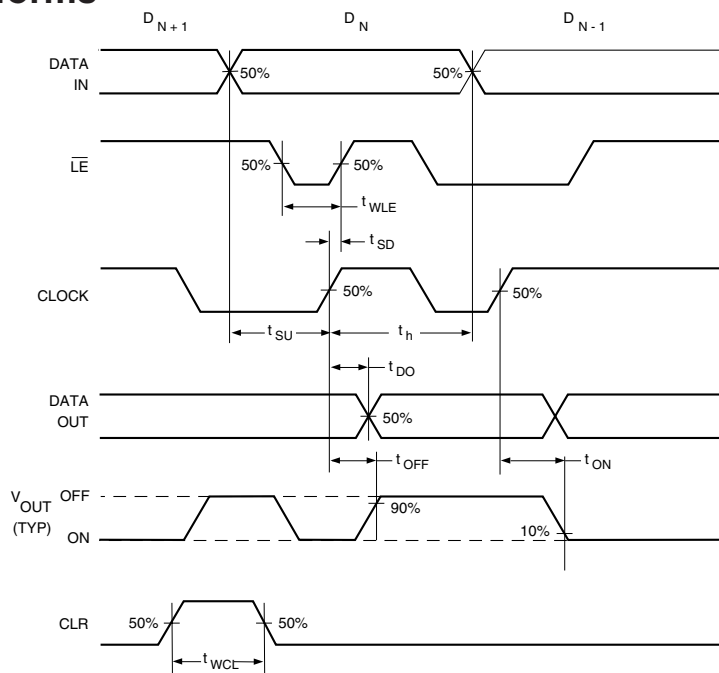
## Truth Table

| Data in 8-Bit Shift Register |    |    |    |    |    |    |    | $\overline{LE}$ | CL | Output Switch State |     |     |     |     |     |     |     |
|------------------------------|----|----|----|----|----|----|----|-----------------|----|---------------------|-----|-----|-----|-----|-----|-----|-----|
| D0                           | D1 | D2 | D3 | D4 | D5 | D6 | D7 |                 |    | SW0                 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |
| L                            |    |    |    |    |    |    |    | L               | L  | OFF                 |     |     |     |     |     |     |     |
| H                            |    |    |    |    |    |    |    | L               | L  | ON                  |     |     |     |     |     |     |     |
|                              | L  |    |    |    |    |    |    | L               | L  |                     | OFF |     |     |     |     |     |     |
|                              | H  |    |    |    |    |    |    | L               | L  |                     | ON  |     |     |     |     |     |     |
|                              |    | L  |    |    |    |    |    | L               | L  |                     |     | OFF |     |     |     |     |     |
|                              |    | H  |    |    |    |    |    | L               | L  |                     |     | ON  |     |     |     |     |     |
|                              |    |    | L  |    |    |    |    | L               | L  |                     |     |     | OFF |     |     |     |     |
|                              |    |    | H  |    |    |    |    | L               | L  |                     |     |     | ON  |     |     |     |     |
|                              |    |    |    | L  |    |    |    | L               | L  |                     |     |     |     | OFF |     |     |     |
|                              |    |    |    | H  |    |    |    | L               | L  |                     |     |     |     | ON  |     |     |     |
|                              |    |    |    |    | L  |    |    | L               | L  |                     |     |     |     |     | OFF |     |     |
|                              |    |    |    |    | H  |    |    | L               | L  |                     |     |     |     |     | ON  |     |     |
|                              |    |    |    |    |    | L  |    | L               | L  |                     |     |     |     |     |     | OFF |     |
|                              |    |    |    |    |    | H  |    | L               | L  |                     |     |     |     |     |     | ON  |     |
|                              |    |    |    |    |    |    | L  | L               | L  |                     |     |     |     |     |     |     | OFF |
|                              |    |    |    |    |    |    | H  | L               | L  |                     |     |     |     |     |     |     | ON  |
| X                            | X  | X  | X  | X  | X  | X  | X  | H               | L  | Hold Previous State |     |     |     |     |     |     |     |
| X                            | X  | X  | X  | X  | X  | X  | X  | X               | H  | OFF                 | OFF | OFF | OFF | OFF | OFF | OFF | OFF |

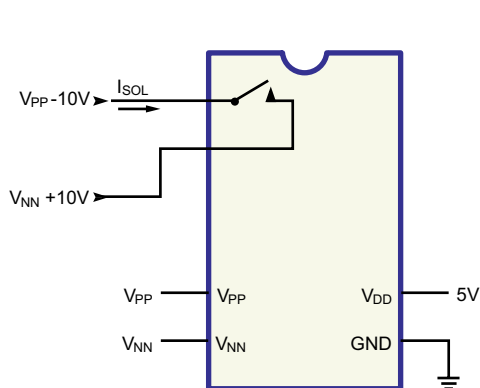
### Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L→H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of  $\overline{LE}$ . When  $\overline{LE}$  is low the shift register data flows through the latch.
4.  $D_{OUT}$  is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if  $\overline{LE}$  is H.
6. The clear input overrides all other inputs.

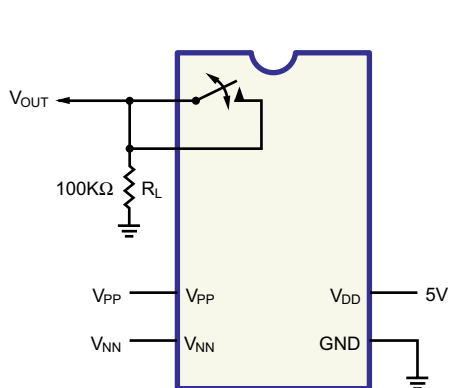
## Logic Timing Waveforms



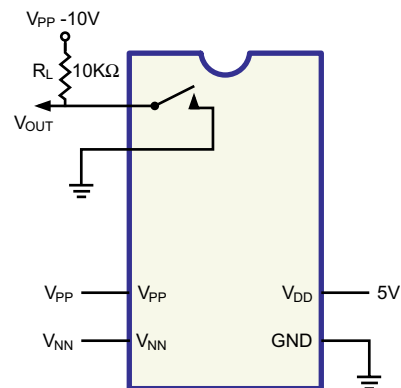
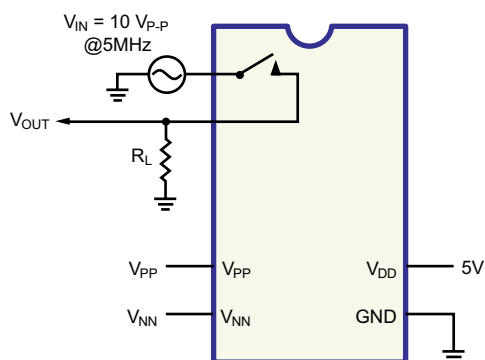
## Test Circuits



Switch OFF Leakage

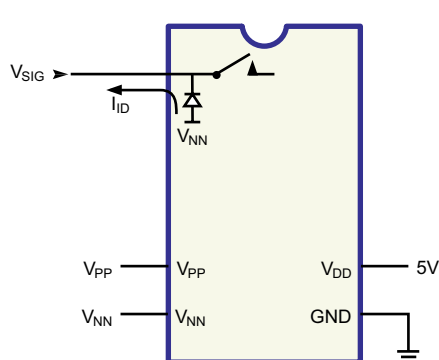


DC Offset ON/OFF

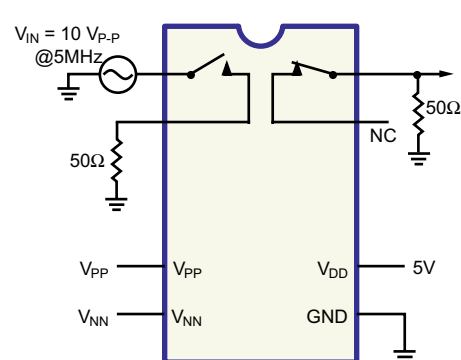
 $T_{ON}/T_{OFF}$  Test Circuit

$$K_O = 20 \log \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

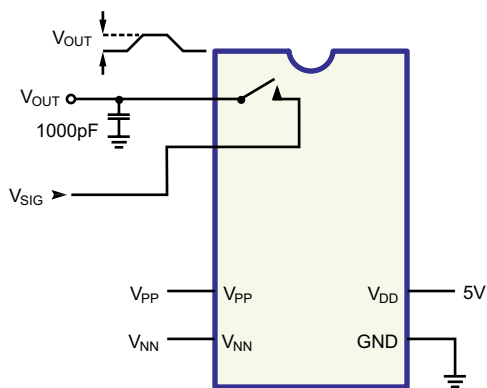


Isolation Diode Current



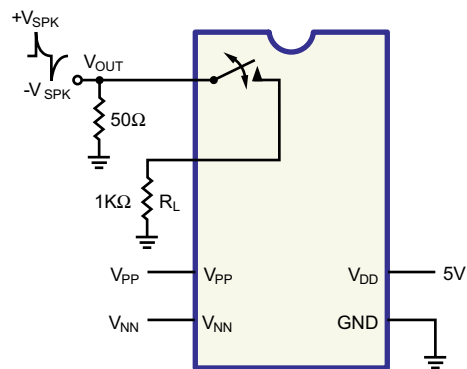
$$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Crosstalk



$$Q = 1000pF \times V_{OUT}$$

Charge Injection



Output Voltage Spike

## 28-Lead (J-Lead) PLCC (PJ) Pin Description

| Pin | Function | Pin | Function        | Pin | Function               | Pin | Function |
|-----|----------|-----|-----------------|-----|------------------------|-----|----------|
| 1   | SW3      | 8   | SW0             | 15  | NC                     | 22  | SW7      |
| 2   | SW3      | 9   | NC              | 16  | D <sub>IN</sub>        | 23  | SW6      |
| 3   | SW2      | 10  | V <sub>PP</sub> | 17  | CLK                    | 24  | SW6      |
| 4   | SW2      | 11  | NC              | 18  | $\overline{\text{LE}}$ | 25  | SW5      |
| 5   | SW1      | 12  | V <sub>NN</sub> | 19  | CL                     | 26  | SW5      |
| 6   | SW1      | 13  | GND             | 20  | D <sub>OUT</sub>       | 27  | SW4      |
| 7   | SW0      | 14  | V <sub>DD</sub> | 21  | SW7                    | 28  | SW4      |

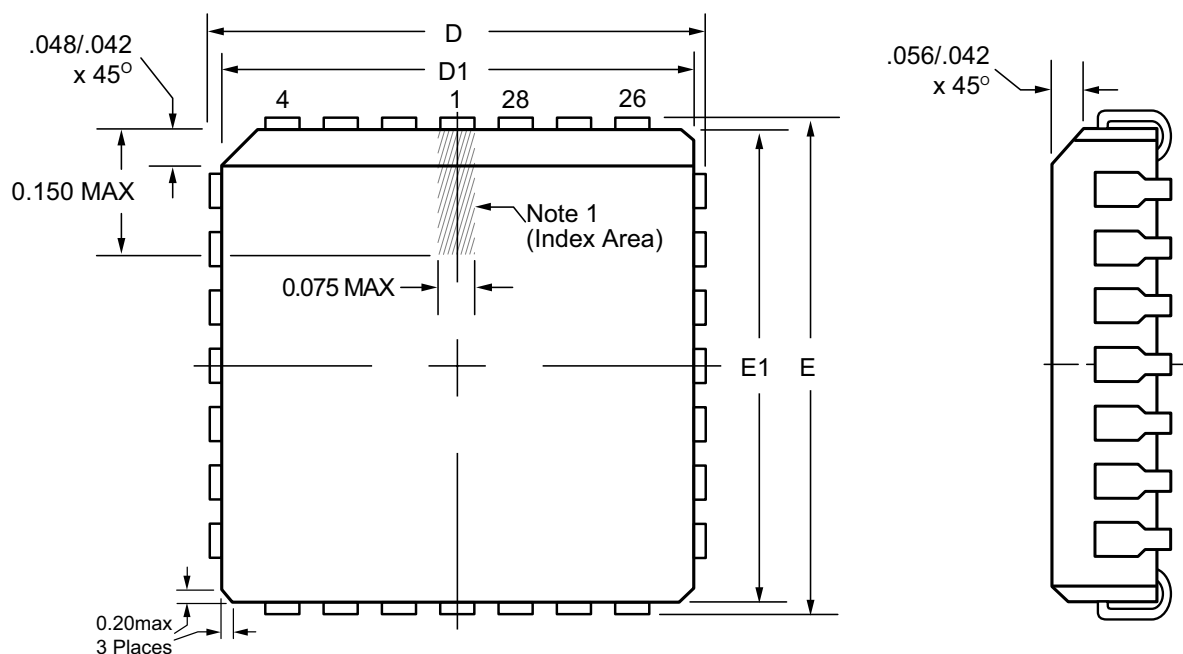
## 48-Lead LQFP/TQFP (FG) Pin Description

| Pin | Function | Pin | Function        | Pin | Function               | Pin | Function         |
|-----|----------|-----|-----------------|-----|------------------------|-----|------------------|
| 1   | SW5      | 13  | NC              | 25  | V <sub>NN</sub>        | 37  | D <sub>OUT</sub> |
| 2   | NC       | 14  | SW2             | 26  | NC                     | 38  | NC               |
| 3   | SW4      | 15  | NC              | 27  | NC                     | 39  | SW7              |
| 4   | NC       | 16  | SW1             | 28  | GND                    | 40  | NC               |
| 5   | SW4      | 17  | NC              | 29  | V <sub>DD</sub>        | 41  | SW7              |
| 6   | NC       | 18  | SW1             | 30  | NC                     | 42  | NC               |
| 7   | NC       | 19  | NC              | 31  | NC                     | 43  | SW6              |
| 8   | SW3      | 20  | SW0             | 32  | NC                     | 44  | NC               |
| 9   | NC       | 21  | NC              | 33  | D <sub>IN</sub>        | 45  | SW6              |
| 10  | SW3      | 22  | SW0             | 34  | CLK                    | 46  | NC               |
| 11  | NC       | 23  | NC              | 35  | $\overline{\text{LE}}$ | 47  | SW5              |
| 12  | SW2      | 24  | V <sub>PP</sub> | 36  | CLR                    | 48  | NC               |

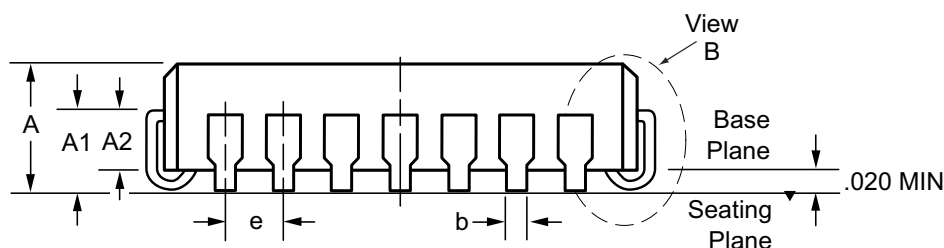
## Power Up/Down Sequence:

1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2. V<sub>SIG</sub> must be V<sub>NN</sub> ≤ V<sub>SIG</sub> ≤ V<sub>PP</sub> or floating during power up/down transistion.
3. Rise and fall times of power supplies V<sub>DD</sub>, V<sub>PP</sub>, and V<sub>NN</sub> should not be less than 1.0msec.

## 28-Lead PLCC Package Outline (PJ)



**Top View**



**Side View**

**Note 1:**

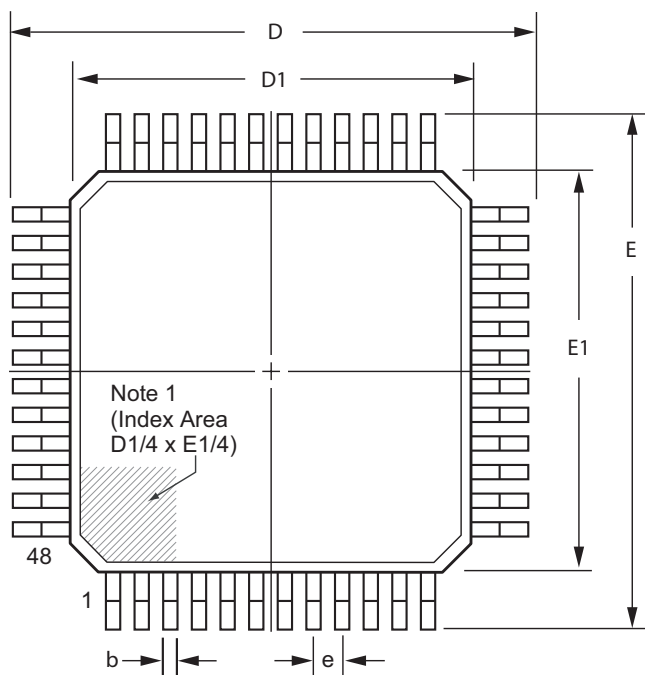
A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

| Symbol             |     | A    | A1   | A2   | b    | D    | D1   | E    | E1   | e           |
|--------------------|-----|------|------|------|------|------|------|------|------|-------------|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .485 | .450 | .485 | .450 | .050<br>BSC |
|                    | NOM | .172 | .105 | -    | -    | .490 | .453 | .490 | .453 |             |
|                    | MAX | .180 | .120 | .083 | .021 | .495 | .456 | .495 | .456 |             |

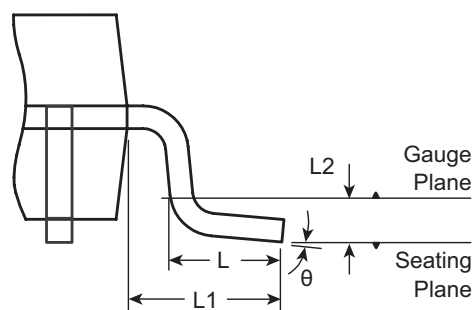
JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

Drawings not to scale.

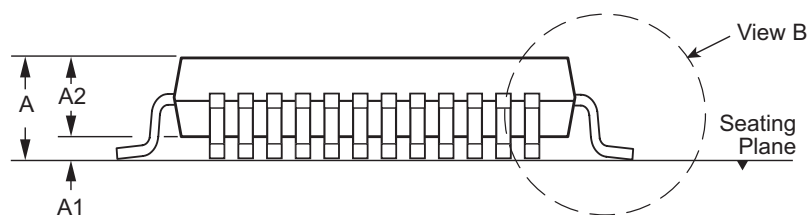
# 48-Lead LQFP/TQFP (1.4mm) Package Outline (FG)



**Top View**



**View B**



**Side View**

**Note 1:**

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

| Symbol         | A   | A1   | A2   | b    | D    | D1       | E        | E1       | e        | L        | L1       | L2       | θ    |
|----------------|-----|------|------|------|------|----------|----------|----------|----------|----------|----------|----------|------|
| Dimension (mm) | MIN | 1.40 | 0.05 | 1.35 | 0.17 | 9.00 BSC | 7.00 BSC | 9.00 BSC | 7.00 BSC | 0.50 BSC | 1.00 REF | 0.25 BSC | 0°   |
|                | NOM | -    | -    | 1.40 | 0.22 |          |          |          |          |          |          |          | 3.5° |
|                | MAX | 1.60 | 0.15 | 1.45 | 0.27 |          |          |          |          |          |          |          | 7°   |

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

**Drawings not to scale.**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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**Supertex inc.**

1235 Bordeaux Drive, Sunnyvale, CA 94089

TEL: (408) 222-8888 / FAX: (408) 222-4895

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