

Features

- AM/FM Tuner Front End with Integrated PLL
- AM Up-conversion System (AM-IF: 10.7 MHz)
- FM Down-conversion System (FM-IF: 10.7 MHz)
- IF Frequencies up to 25 MHz
- Fine-tuning Steps: AM = 1 kHz and FM = 50 kHz/25 kHz/12.5 kHz
- Fast Fractional PLL (Lock Time < 1 ms) Inclusive Spurious Compensation
- Fast RF-AGC, Programmable in 1-dB Steps
- Fast IF-AGC, Programmable in 2-dB Steps
- Fast Frequency Change by 2 Programmable N-divider
- Two DACs for Automatic Tuner Alignment
- High S/N Ratio
- 3-wire Bus (Enable, Clock and Data; 3V and 5V Microcontrollers-compatible)

1. Description

The T4260 is an advanced AM/FM receiver with integrated fast PLL as a single-chip solution based on Atmel®'s high-performance BICMOS II technology. The low-impedance driver at the IF output is designed for the A/D of a digital IF. The fast tuning concept realized in this part is based on patents held by Atmel and allows lock times less than 1 ms for a jump over the FM band with a step width of 12.5 kHz. The AM up-conversion and the FM down-conversion allows an economic filter concept. An automatic tuner alignment is provided by built-in DACs for gain and offset compensation. The frequency range of the IC covers the FM broadcasting band as well as the AM band. The low current consumption helps the designers to achieve economic power consumption concepts and helps to keep the power dissipation in the tuner low.

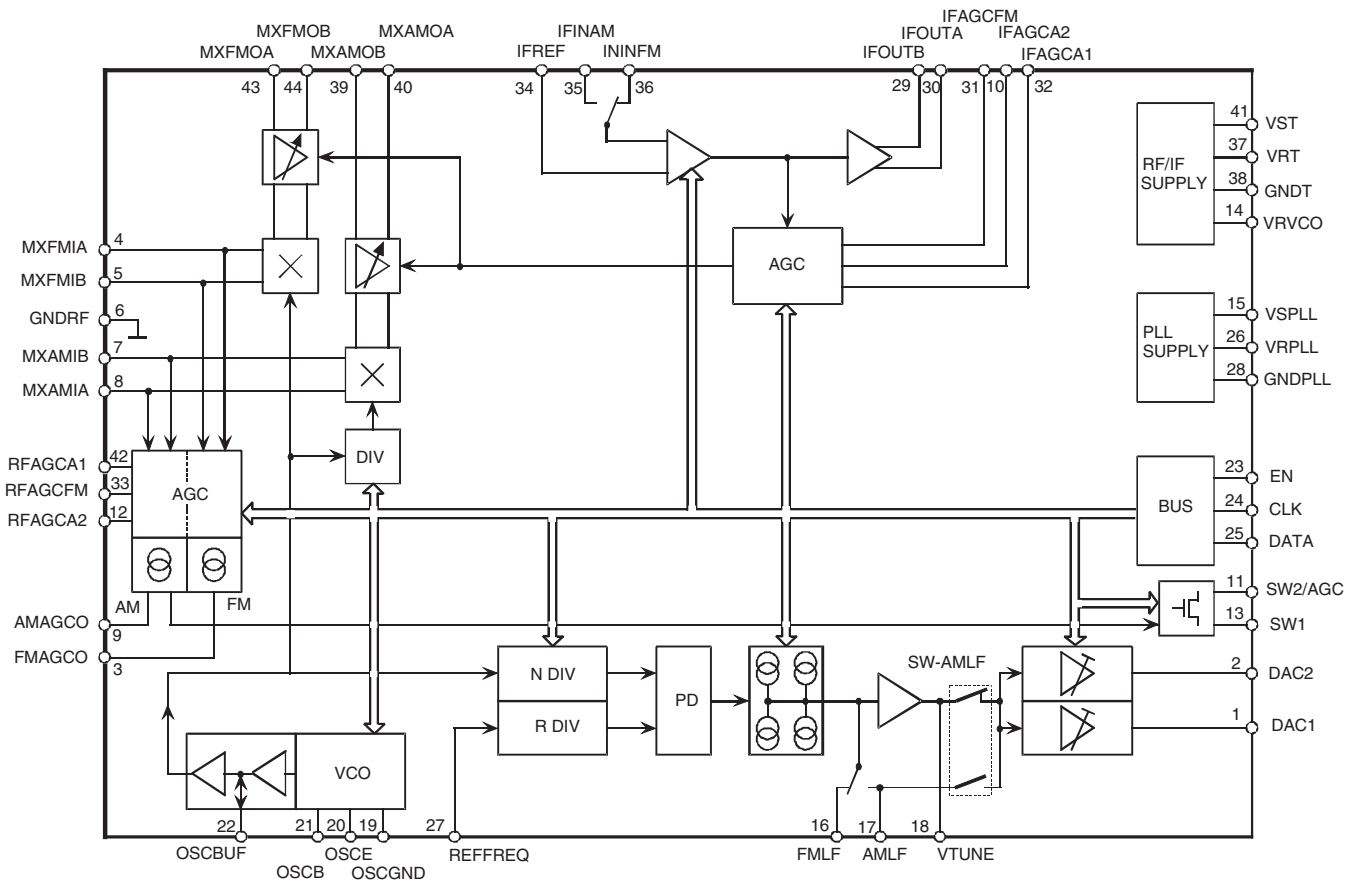


AM/FM Front End IC

T4260



Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SSO44

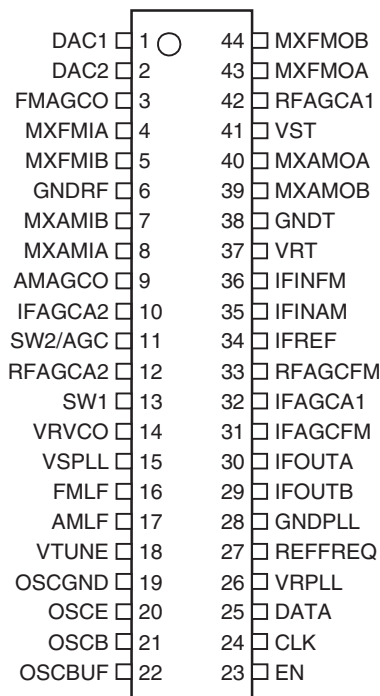


Table 2-1. Pin Description

| Pin | Symbol | Function |
|-----|---------|-------------------------|
| 1 | DAC1 | DAC1 output |
| 2 | DAC2 | DAC2 output |
| 3 | FMAGCO | FM AGC current |
| 4 | MXFMIA | FM mixer input A |
| 5 | MXFMIB | FM mixer input B |
| 6 | GNDRF | RF ground |
| 7 | MXAMIB | AM mixer input B |
| 8 | MXAMIA | AM mixer input A |
| 9 | AMAGCO | AM AGC current |
| 10 | IFAGCA2 | AM IF-AGC filter 2 |
| 11 | SW2/AGC | Switch 2/AM AGC voltage |
| 12 | RFAGCA2 | RF AM-AGC filter 2 |
| 13 | SW1 | Switching output 1 |
| 14 | VRVCO | VCO reference voltage |
| 15 | VSPLL | PLL supply voltage |
| 16 | FMLF | FM loop filter |
| 17 | AMLF | AM loop filter |
| 18 | VTUNE | Tuning voltage |
| 19 | OSCGND | Oscillator ground |
| 20 | OSCE | Oscillator emitter |

Table 2-1. Pin Description (Continued)

| Pin | Symbol | Function |
|-----|---------|--------------------------------|
| 21 | OSCB | Oscillator base |
| 22 | OSCBUF | Oscillator buffer output/input |
| 23 | EN | 3-wire bus Enable |
| 24 | CLK | 3-wire bus Clock |
| 25 | DATA | 3-wire bus Data |
| 26 | VRPLL | PLL reference voltage |
| 27 | REFFREQ | PLL reference frequency |
| 28 | GNDPLL | PLL ground |
| 29 | IFOUTB | IF output B |
| 30 | IFOUTA | IF output A |
| 31 | IFAGCFM | FM IF-AGC filter |
| 32 | IFAGCA1 | AM IF-AGC filter 1 |
| 33 | RFAGCFM | RF FM-AGC filter |
| 34 | IFREF | IF amplifier reference input |
| 35 | IFINAM | IF amplifier AM input |
| 36 | IFINFM | IF amplifier FM input |
| 37 | VRT | Tuner reference voltage |
| 38 | GNDT | Tuner ground |
| 39 | MXAMOB | AM mixer output B |
| 40 | MXAMOA | AM mixer output A |
| 41 | VST | Tuner supply voltage |
| 42 | RFAGCA1 | RF AM-AGC filter 1 |
| 43 | MXFMOA | FM mixer output A |
| 44 | MXFMOB | FM mixer output B |

3. Functional Description

The T4260 implements an AM up-conversion reception path from the RF input signal to the IF output signal. A VCO and an LO prescaler for AM are integrated to generate the LO frequency to the AM mixer. The FM reception path generates the same LO frequency from the RF input signal by a down-conversion to the IF output. The IF A/D output is designed for digital signal processing. The IF can be chosen in the range of 10 MHz to 25 MHz. Automatic gain control (AGC) circuits are implemented to control the preamplifier stages in the AM and FM reception paths.

For improved performance, the PLL has an integrated special 2-bit shift fractional logic with spurious suppression that enables fast frequency changes in AM and FM mode by a low step frequency (f_{PDF}). In addition, two programmable DACs (Digital to Analog Converter) support the alignment via a microcontroller.

For a double-tuner concept, external voltage can be applied at the input of the DACs, the internal PLL can be switched off and the OSC buffer (output) can also be used as input.

Several register bits (bit 0 to bit 145) are used to control the circuit's operation and to adapt certain circuit parameters to the specific application. The control bits are organized in four 8-bit, four 16-bit and three 24-bit registers that can be programmed by the 3-wire bus protocol. The bus protocol and the bit-to-register mapping is described in [Section 8. "3-wire Bus Description" on page 10](#). The meaning of the control bits is mentioned in the following sections.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages are referred to GND

| Parameters | Symbol | Value | Unit |
|---------------------------------------|--------------------|-------------|------|
| Analog supply voltage, pins 15 and 41 | V_{ST}, V_{SPLL} | 10 | V |
| Maximum power consumption | P_{tot} | 1.0 | W |
| Ambient temperature range | T_{amb} | -40 to +85 | °C |
| Storage temperature range | T_{stg} | -40 to +150 | °C |
| Junction temperature | T_j | 150 | °C |

5. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|-----------------------------------|------------|-------|------|
| Junction ambient, soldered to PCB | R_{thJA} | 52 | K/W |

6. Operating Range

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|--|--------------------|------|------|------|------|
| Supply voltage range ⁽¹⁾ , pins 15 and 41 | V_{ST}, V_{SPLL} | 8 | 8.5 | 10 | V |
| Ambient temperature | T_{amb} | -40 | | 85 | °C |
| Oscillator frequency, pin 21 | R_{fi} | 60 | | 175 | MHz |

Note: 1. V_{ST} and V_{SPLL} must have the same voltage.

7. Electrical Characteristics

Test conditions (unless otherwise specified): $V_{ST}/V_{SPLL} = +8.5V$, $T_{amb} = +25°C$

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|--|-----------|--------|------------|-------------|----------------|-------------------|-------|
| 1 | Power Supply | | | | | | | | |
| 1.1 | Supply voltage | | 15, 41 | V_S | 8 | 8.5 | 10 | V | C |
| 1.2 | Supply current | AM and FM mode, $V_S = 10V$ | 15, 41 | I_S | 70 | 85 | 110 | mA | A |
| 2 | PLL Divider | | | | | | | | |
| 2.1 | Programmable R-divider | 14-bit register | | | 3 | | 16383 | | A |
| 2.2 | Programmable (VCO) N-divider (1 kHz step frequency) | 2-bit × 18-bit register switchable via bit 5 | | | 3 | | 262143 | | A |
| 2.3 | Reference oscillator input voltage | $f = 0.1 \text{ MHz to } 3 \text{ MHz}$ | 27 | | 100 | | | mV _{rms} | B |
| 2.4 | Reference frequency | FM AM | | | 120 120 | 150 2850 | 10000 10000 | kHz kHz | |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

7. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_{ST}/V_{SPLL} = +8.5V$, $T_{amb} = +25^{\circ}C$

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------|---|--|-----------|--------------|------|-------|-------------|------------|------------------|
| 2.5 | Settling time in FM mode (switching from 87.5 MHz to 108 MHz or vice versa) | $f_{PD} = 50 \text{ kHz}$ $I_{PD} = 2 \text{ mA}$ | | | | 1 | | ms | B |
| 3 | AMLF/FMLF | | | | | | | | |
| 3.1 | Output current 1 | FMLF, AMLF = 1.8V | 16, 17 | | 40 | 50 | 60 | μA | A ⁽¹⁾ |
| 3.2 | Output current 2 | FMLF, AMLF = 1.8V | 16, 17 | | 80 | 100 | 120 | μA | A ⁽¹⁾ |
| 3.3 | Output current 3 | FMLF, AMLF = 1.8V | 16, 17 | | 850 | 1000 | 1250 | μA | A ⁽¹⁾ |
| 3.4 | Output current 4 | FMLF, AMLF = 1.8V | 16, 17 | | 1650 | 2000 | 2450 | μA | A ⁽¹⁾ |
| 3.5 | Leakage current | FMLF, AMLF = 1.8V | 16, 17 | | | | 10 | nA | A ⁽¹⁾ |
| 4 | VTUNE | | | | | | | | |
| 4.1 | Saturation voltage LOW | $V_{SATL} = V_{TUNEMIN}$ | 18 | V_{SATL} | 100 | 200 | 400 | mV | C |
| 4.2 | Saturation voltage HIGH | $V_{SATH} = V_{SPLL} - V_{TUNEMAX}$ | 18 | V_{SATH} | | | 500 | mV | C |
| 5 | DAC1, DAC2 | | | | | | | | |
| 5.1 | Output current | | 1, 2 | $I_{DAC1,2}$ | | | 1 | mA | D |
| 5.2 | Output voltage | | 1, 2 | $V_{DAC1,2}$ | 0.3 | | $V_S - 0.6$ | V | A |
| 5.3 | Maximum offset range | Offset = 0, gain = 58 | 1, 2 | | 0.9 | 0.98 | 1.1 | V | A ⁽¹⁾ |
| 5.4 | Minimum offset range | Offset = 127, gain = 58 | 1, 2 | | -0.9 | -0.98 | -1.1 | V | A ⁽¹⁾ |
| 5.5 | Maximum gain range | Gain = 255, offset = 64 | 1, 2 | | 2.06 | 2.09 | 2.13 | - | A ⁽¹⁾ |
| 5.6 | Minimum gain range | Gain = 0, offset = 64 | 1, 2 | | 0.63 | 0.67 | 0.73 | - | A ⁽¹⁾ |
| 6 | Oscillator | | | | | | | | |
| 6.1 | Frequency range | | 21 | | 60 | | 170 | MHz | B |
| 6.2 | Fractional frequency range | Fractional mode | 21 | | 60 | | 140 | MHz | A |
| 6.3 | Buffer output | | 22 | | 150 | | | mV_{rms} | C |
| 6.4 | Buffer input | Slave mode | 22 | | 100 | | | mV_{rms} | C |
| 6.5 | Input voltage | | 21 | V_{OSC} | 150 | | | mV_{rms} | A |
| 7 | FM Mixer | | | | | | | | |
| 7.1 | Frequency range | | | | 75 | | 163 | MHz | B |
| 7.2 | Input IP3 | | | | | 133 | | dB μV | C |
| 7.3 | Input impedance | | | | | 3.5 | | k Ω | D |
| 7.4 | Input capacitance | | | | | | 4 | pF | D |
| 7.5 | Noise figure | | | F | | 14 | | dB | C |
| 7.6 | Conversion transconductance | | | | 2.6 | 3.1 | 3.6 | ms | D ⁽¹⁾ |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

7. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_{ST}/V_{SPLL} = +8.5V$, $T_{amb} = +25^{\circ}C$

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------------|---|---|-----|--------|-------------|---------------|------------------|----------------|------------------|
| 8 | AM Mixer (Symmetrical Input) | | | | | | | | |
| 8.1 | Frequency range | | | | 0.075 | | 26 | MHz | B |
| 8.2 | Input IP3 | | | | | 133 | | dB μ V | C |
| 8.3 | Input impedance | | | | | 2.5 | | k Ω | D |
| 8.4 | Noise figure | | | F | | 10 | | dB | C |
| 8.5 | Conversion transconductance | | | | 2.6 | 3.1 | 3.6 | mS | D ⁽¹⁾ |
| 9 | Isolation | | | | | | | | |
| 9.1 | Isolation AM-FM | | | | | 40 | | dB | C |
| 9.2 | IF suppression | | | | | 40 | | dB | C |
| 10 | RF-AGC | | | | | | | | |
| 10.1 | Frequency range | FM AM | | | 75 0.075 | | 163 26 | MHz MHz | A |
| 10.2 | Output current | FM AM | | | | 5 5 | | mA mA | B |
| 10.3 | Output current time constant | FM rising FM falling AM symmetrical | | | | 2 50 40 | | ms ms ms | C |
| 10.4 | RF-AGC AM threshold (programmable with bit 12 - bit 15) | 88 dB μ V | 42 | | 87 | 88 | 90 | dB μ V | A ⁽¹⁾ |
| | | 89 dB μ V | 42 | | 88 | 89 | 91 | dB μ V | A ⁽¹⁾ |
| | | 90 dB μ V | 42 | | 89 | 90 | 92 | dB μ V | A ⁽¹⁾ |
| | | 91 dB μ V | 42 | | 90 | 91 | 93 | dB μ V | A ⁽¹⁾ |
| | | 92 dB μ V | 42 | | 91 | 92 | 94 | dB μ V | A ⁽¹⁾ |
| | | 93 dB μ V | 42 | | 92 | 93 | 95 | dB μ V | A ⁽¹⁾ |
| | | 94 dB μ V | 42 | | 93 | 94 | 96 | dB μ V | A ⁽¹⁾ |
| | | 95 dB μ V | 42 | | 94 | 95 | 97 | dB μ V | A ⁽¹⁾ |
| | | 96 dB μ V | 42 | | 95 | 96 | 98 | dB μ V | A ⁽¹⁾ |
| | | 97 dB μ V | 42 | | 96 | 97 | 99 | dB μ V | A ⁽¹⁾ |
| | | 98 dB μ V | 42 | | 97 | 98 | 100 | dB μ V | A ⁽¹⁾ |
| | | 99 dB μ V | 42 | | 98 | 99 | 101 | dB μ V | A ⁽¹⁾ |
| | | 100 dB μ V | 42 | | 99 | 100 | 102 | dB μ V | A ⁽¹⁾ |
| 101 dB μ V | 42 | | 100 | 101 | 103 | dB μ V | A ⁽¹⁾ | | |
| 102 dB μ V | 42 | | 101 | 102 | 104 | dB μ V | A ⁽¹⁾ | | |
| 103 dB μ V | 42 | | 102 | 103 | 107 | dB μ V | A ⁽¹⁾ | | |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Minimum and maximum limits are characterized for entire temperature range ($-40^{\circ}C$ to $+85^{\circ}C$) but are tested at $+25^{\circ}C$

7. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_{ST}/V_{SPLL} = +8.5V$, $T_{amb} = +25^{\circ}C$

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|----------------|--|--|-----------|--------|------|----------------|------------------|----------------------|------------------|
| 10.5 | RF-AGC FM threshold (programmable with bit 12 - bit 15) | 91 dB μ V | 33 | | 90 | 91 | 93 | dB μ V | A ⁽¹⁾ |
| | | 92 dB μ V | 33 | | 91 | 92 | 95 | dB μ V | A ⁽¹⁾ |
| | | 93 dB μ V | 33 | | 92 | 93 | 96 | dB μ V | A ⁽¹⁾ |
| | | 94 dB μ V | 33 | | 93 | 94 | 96 | dB μ V | A ⁽¹⁾ |
| | | 95 dB μ V | 33 | | 94 | 95 | 98 | dB μ V | A ⁽¹⁾ |
| | | 96 dB μ V | 33 | | 95 | 96 | 99 | dB μ V | A ⁽¹⁾ |
| | | 97 dB μ V | 33 | | 96 | 97 | 102 | dB μ V | A ⁽¹⁾ |
| | | 98 dB μ V | 33 | | 97 | 98 | 101 | dB μ V | A ⁽¹⁾ |
| | | 99 dB μ V | 33 | | 98 | 99 | 102 | dB μ V | A ⁽¹⁾ |
| | | 100 dB μ V | 33 | | 99 | 100 | 104 | dB μ V | A ⁽¹⁾ |
| | | 101 dB μ V | 33 | | 100 | 101 | 104 | dB μ V | A ⁽¹⁾ |
| | | 102 dB μ V | 33 | | 101 | 102 | 105 | dB μ V | A ⁽¹⁾ |
| | | 103 dB μ V | 33 | | 102 | 103 | 106 | dB μ V | A ⁽¹⁾ |
| | | 104 dB μ V | 33 | | 103 | 104 | 107 | dB μ V | A ⁽¹⁾ |
| 105 dB μ V | 33 | | 104 | 105 | 108 | dB μ V | A ⁽¹⁾ | | |
| 106 dB μ V | 33 | | 105 | 106 | 109 | dB μ V | A ⁽¹⁾ | | |
| 11 | IF Amplifier | | | | | | | | |
| 11.1 | Frequency range | | | | 10 | | 25 | MHz | A |
| 11.2 | Output voltage | | | | | 117 | | dB μ V | B |
| 11.3 | Distortion (2-tone IM3) | f1 = 10.7 MHz f2 = 10.75 MHz RL = 2 × 300 Ω | | | | 55 | | dB | A |
| 11.4 | Gain (programmable in 2-dB steps) | Minimum gain Maximum gain | | | | 12 42 | | dB dB | A |
| 11.5 | Input impedance | FM AM | 36, 35 | | | 330 2500 | | Ω Ω | D |
| 12 | IF-AGC | | | | | | | | |
| 12.1 | IF-AGC AM/FM threshold (programmable with bit 0 - bit 2) | 109 dB μ V | 29/30 | | 108 | 109 | 112 | dB μ V | A ⁽¹⁾ |
| | | 111 dB μ V | 29/30 | | 110 | 111 | 114 | dB μ V | A ⁽¹⁾ |
| | | 113 dB μ V | 29/30 | | 111 | 113 | 115 | dB μ V | A ⁽¹⁾ |
| | | 115 dB μ V | 29/30 | | 113 | 115 | 117 | dB μ V | A ⁽¹⁾ |
| | | 117 dB μ V | 29/30 | | 116 | 117 | 121 | dB μ V | A ⁽¹⁾ |
| | | 118 dB μ V | 29/30 | | 117 | 118 | 122 | dB μ V | A ⁽¹⁾ |
| | | 119 dB μ V | 29/30 | | 118 | 119 | 123 | dB μ V | A ⁽¹⁾ |
| 121 dB μ V | 29/30 | | 120 | 121 | 126 | dB μ V | A ⁽¹⁾ | | |
| 12.2 | AGC dynamic range | | | | | 40 | | dB | B |
| 12.3 | AGC time constant (external capacity ≤ 100 nF) | FM rising FM falling AM symmetrical | | | | 16 4 200 | | μ s ms ms | D |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Minimum and maximum limits are characterized for entire temperature range ($-40^{\circ}C$ to $+85^{\circ}C$) but are tested at $+25^{\circ}C$

7. Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_{ST}/V_{SPLL} = +8.5V$, $T_{amb} = +25^{\circ}C$

| No. | Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit | Type* |
|-----------|---|---------------------------------------|-------|--------------------------------------|-------------|------|------------------|----------|------------------|
| 13 | IF Gain | | | | | | | | |
| 13.1 | IF gain (programmable with bit 6 - bit 9) | 12 dB | | | 9 | 12 | 14 | dB | A ⁽¹⁾ |
| | | 14 dB | | | 12 | 14 | 16 | dB | A ⁽¹⁾ |
| | | 16 dB | | | 14 | 16 | 18 | dB | A ⁽¹⁾ |
| | | 18 dB | | | 17 | 18 | 20 | dB | C ⁽¹⁾ |
| | | 20 dB | | | 17 | 20 | 22 | dB | A ⁽¹⁾ |
| | | 22 dB | | | 19 | 22 | 24 | dB | C ⁽¹⁾ |
| | | 24 dB | | | 21 | 24 | 26 | dB | C ⁽¹⁾ |
| | | 26 dB | | | 23 | 26 | 28 | dB | C ⁽¹⁾ |
| | | 28 dB | | | 25 | 28 | 30 | dB | A ⁽¹⁾ |
| | | 30 dB | | | 27 | 30 | 32 | dB | C ⁽¹⁾ |
| | | 32 dB | | | 29 | 32 | 34 | dB | C ⁽¹⁾ |
| | | 34 dB | | | 31 | 34 | 36 | dB | C ⁽¹⁾ |
| | | 36 dB | | | 33 | 36 | 38 | dB | C ⁽¹⁾ |
| | | 38 dB | | | 35 | 38 | 40 | dB | C ⁽¹⁾ |
| 40 dB | | | 37 | 40 | 42 | dB | C ⁽¹⁾ | | |
| 42 dB | | | 39 | 42 | 44 | dB | A ⁽¹⁾ | | |
| 14 | SWO1 (Open Drain) | | | | | | | | |
| 14.1 | Output voltage LOW | I = 1 mA, V _{SWO1} = 8.5V | 13 | V _{SWOL} | 100 | 160 | 200 | mV | A |
| 14.2 | Output leakage current HIGH | | 13 | I _{OHL} | | | 10 | μA | A |
| 14.3 | Maximum output voltage | | 13 | | | 8.5 | | V | C |
| 15 | SW2/AGC (Open Drain in Switch Mode) | | | | | | | | |
| 15.1 | Output voltage LOW | I = 1 mA, V ₁₁ = 6 V | 11 | V _{SWOL} | 100 | 160 | 200 | mV | A |
| 15.2 | Output leakage current HIGH | | 11 | I _{OHL} | | | 10 | μA | A |
| 15.3 | Maximum output voltage | | 11 | | | 6 | | V | C |
| 16 | 3-wire Bus, ENABLE, DATA, CLOCK | | | | | | | | |
| 16.1 | Input voltage | High Low | 23-25 | V _{BUS} V _{BUS} | 2.7 -0.3 | | 5.3 +0.8 | V V | A A |
| 16.2 | Clock frequency | | 24 | | | | 1.0 | MHz | B |
| 16.3 | Period of CLK | | 24 | t _H t _L | 250 250 | | | ns ns | C C |
| 16.4 | Rise time EN, DATA, CLK | | 23-25 | t _R | | | 400 | ns | C |
| 16.5 | Fall time EN, DATA, CLK | | 23-25 | t _F | | | 100 | ns | C |
| 16.6 | Set-up time | | 23-25 | t _S | 100 | | | ns | C |
| 16.7 | Hold time EN | | 23 | t _{HEN} | 250 | | | ns | C |
| 16.8 | Hold time DATA | | 25 | t _{HDA} | 0 | | | ns | C |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Minimum and maximum limits are characterized for entire temperature range (-40°C to +85°C) but are tested at +25°C

8. 3-wire Bus Description

The register settings of the T4260 are programmed by a 3-wire bus protocol. The bus protocol consists of separate commands. A defined number of bits is transmitted sequentially during each command.

One command is used to program all bits of one register. The different registers available (see chapter “3-wire Bus Data Transfer” on page 12) are addressed by the length of the command (number of transmitted bits) and by two address bits that are unique to each register of a given length. 8-bit registers are programmed by 8-bit commands, 16-bit registers are programmed by 16-bit commands and 24-bit registers are programmed by 24-bit commands.

Each bus command starts with a falling edge on the enable line (EN) and ends with a rising edge on EN. EN has to be kept LOW during the bus command.

The sequence of transmitted bits during one command starts with the MSB of the first byte and ends with the LSB of the last byte of the register addressed. To transmit one bit (0/1), DATA has to be set to the appropriate value (LOW/HIGH) and a LOW-to-HIGH transition has to be performed on the clock line (CLK) while DATA is valid. The DATA is evaluated at the rising edges of CLK. The number of LOW-to-HIGH transitions on CLK during the LOW period of EN is used to determine the length of the command.

Figure 8-1. 3-wire Pulse Diagram

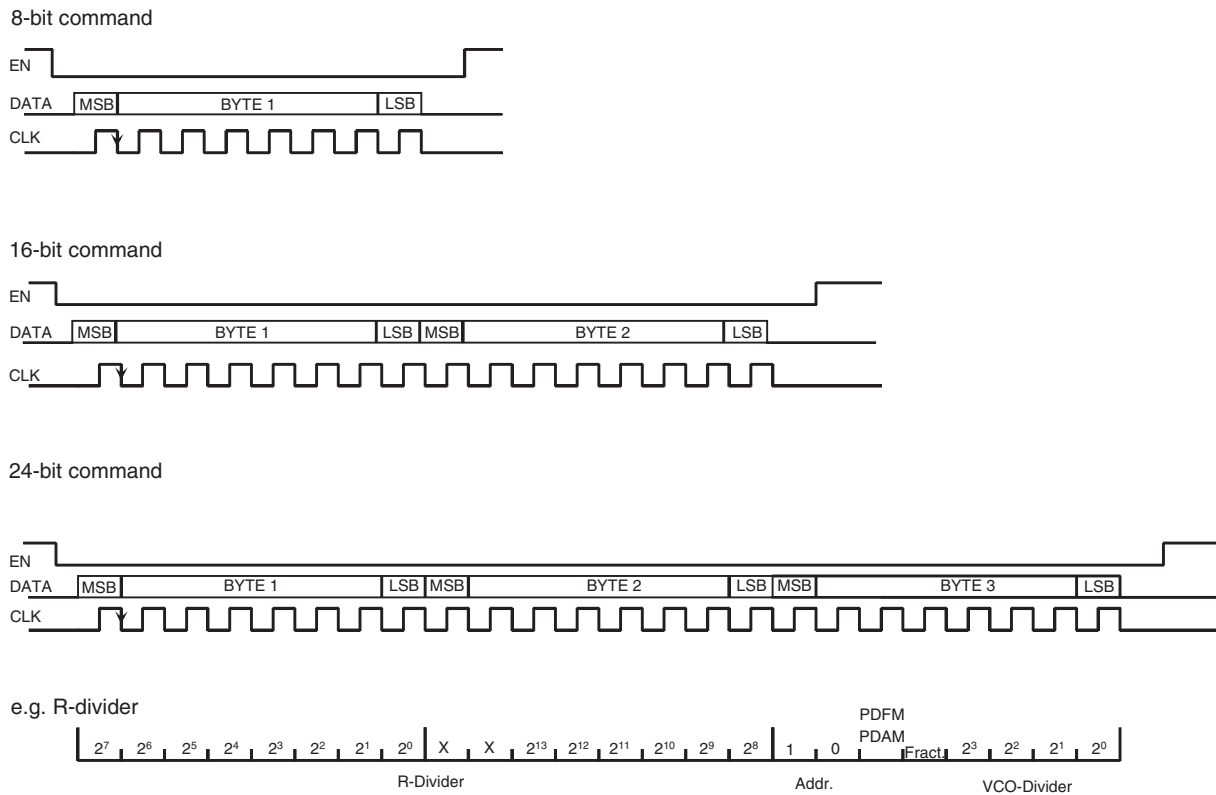
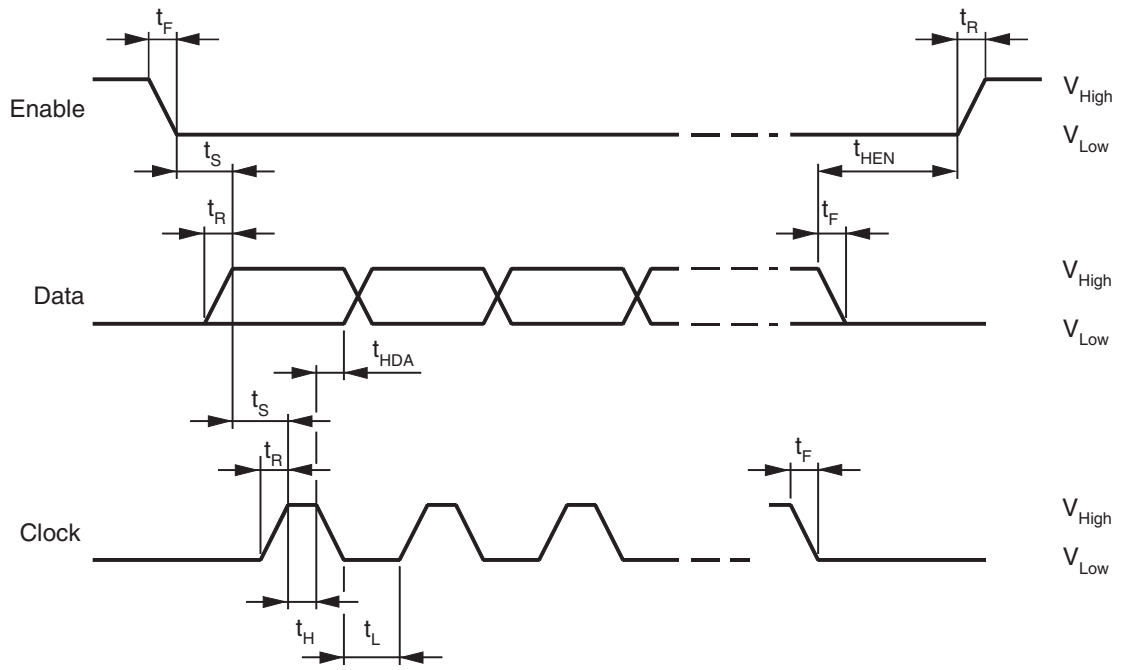


Figure 8-2. 3-wire Bus Timing Diagram



9. 3-wire Bus Data Transfer

Table 9-1. Control Registers

| A24_10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------|-----|-----------------|-----------------|-----------------|-----------------|----------------|----------------|-------|---|-----------|-----|----------------|----------------|----------------|----------------|--|--|--------|--|--|--|--|--|--|--|-----|--|-----|--|--|--|--|--|--|--|--------|--|--|--|--|--|--|--|-----|--|
| MSB | | | | | | | | BYTE 1 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 2 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 3 | | | | | | | | LSB | |
| R-Divider | | | | | | | | R-Divider | | | | | | | | ADDR. | | PDAM/PDFM | | Fractional | | Divider VCO | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | x | x | 2 ¹³ | 2 ¹² | 2 ¹¹ | 2 ¹⁰ | 2 ⁹ | 2 ⁸ | 1 | 0 | 1/0 | 0/1 | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 131 | 130 | 129 | 128 | 127 | 126 | 125 | 124 | 139 | 138 | 137 | 136 | 135 | 134 | 133 | 132 | x | x | 145 | 144 | 143 | 142 | 141 | 140 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| A24_01 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|-------|---|------------------|------------------|------------------|------------------|-----------------|-----------------|---|--|------------|--|--|--|--|--|--|--|-----|--|-----|--|--|--|--|--|--|--|--------|--|--|--|--|--|--|--|-----|--|
| MSB | | | | | | | | BYTE 1 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 2 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 3 | | | | | | | | LSB | |
| N2-Divider | | | | | | | | N2-Divider | | | | | | | | ADDR. | | x | | x | | x | | x | | N2-Divider | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹¹ | 2 ¹⁰ | 2 ⁹ | 2 ⁸ | 0 | 1 | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 2 ¹⁷ | 2 ¹⁶ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 109 | 108 | 107 | 106 | 105 | 104 | 103 | 102 | 117 | 116 | 115 | 114 | 113 | 112 | 111 | 110 | x | x | 123 | 122 | 121 | 120 | 119 | 118 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note: 1. Value has to be 0.

| A24_00 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|-------|---|------------------|------------------|------------------|------------------|-----------------|-----------------|---|--|------------|--|--|--|--|--|--|--|-----|--|-----|--|--|--|--|--|--|--|--------|--|--|--|--|--|--|--|-----|--|
| MSB | | | | | | | | BYTE 1 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 2 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 3 | | | | | | | | LSB | |
| N1-Divider | | | | | | | | N1-Divider | | | | | | | | ADDR. | | x | | x | | x | | x | | N1-Divider | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | 2 ¹⁵ | 2 ¹⁴ | 2 ¹³ | 2 ¹² | 2 ¹¹ | 2 ¹⁰ | 2 ⁹ | 2 ⁸ | 0 | 0 | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 2 ¹⁷ | 2 ¹⁶ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 | 95 | 94 | 93 | 92 | 91 | 90 | 89 | 88 | x | x | 101 | 100 | 99 | 98 | 97 | 96 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Note: 1. Value has to be 0.

| A16_11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------|---|----|----|----|----|----|----|-----|--|-----|--|--|--|--|--|--|--|--------|--|--|--|--|--|--|--|-----|--|
| MSB | | | | | | | | BYTE 1 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 2 | | | | | | | | LSB | |
| DAC2-Gain | | | | | | | | ADDR. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | 1 | 1 | x | x | x | x | x | x | | | | | | | | | | | | | | | | | | | | |
| 73 | 72 | 71 | 70 | 69 | 68 | 67 | 66 | x | x | 79 | 78 | 77 | 76 | 75 | 74 | | | | | | | | | | | | | | | | | | | | |

| A16_10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------|---|--------------|--------|-------------|--------|-----------|--------|------------|--|------------|--|---------|--|--|--|--|--|--------|--|--|--|--|--|--|--|-----|--|
| MSB | | | | | | | | BYTE 1 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 2 | | | | | | | | LSB | |
| DAC2-Offset | | | | | | | | ADDR. | | SW-AMLF | | Osc.-Buffer | | Low c. CP | | High c. CP | | SW-impulse | | SW-wire | | | | | | | | | | | | | | | |
| x | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | 1 | 0 | 1 = standard | ON/OFF | HI/ LO | HI/ LO | ON/OFF | ON/OFF | | | | | | | | | | | | | | | | | | | | |
| 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | x | x | 65 | 64 | 63 | 62 | 61 | 60 | | | | | | | | | | | | | | | | | | | | |

| A16_01 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------|---|--------------------|----|----------------|-----|----------------|-----|-----|--|-----|--|--|--|--|--|--|--|--------|--|--|--|--|--|--|--|-----|--|
| MSB | | | | | | | | BYTE 1 | | | | | | | | LSB | | MSB | | | | | | | | BYTE 2 | | | | | | | | LSB | |
| DAC1-Gain | | | | | | | | ADDR. | | 1 = SW2 0 = AGC | | SW2 1 = low | | SW1 1 = low | | | | | | | | | | | | | | | | | | | | | |
| 2 ⁷ | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | 0 | 1 | x | x | x | 1/0 | 1/0 | 1/0 | | | | | | | | | | | | | | | | | | | | |
| 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | x | x | 51 | 50 | 49 | 48 | 47 | 46 | | | | | | | | | | | | | | | | | | | | |

| A16_00 | | | | | | | | | | | | | | | |
|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------|---|----|----|----|----|------------------|-------|
| MSB | | | | | | | | BYTE 1 | | | | | | | LSB |
| MSB | | | | | | | | BYTE 2 | | | | | | | LSB |
| DAC1-Offset | | | | | | | | ADDR. | | x | x | x | x | x | SHIFT |
| x | 2 ⁶ | 2 ⁵ | 2 ⁴ | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | 0 | 0 | 0 | 0 | 0 | 0 | 0 ⁽¹⁾ | 1/0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | x | x | 37 | 36 | 35 | 34 | 33 | 32 |

Note: 1. Value has to be 0.

| A8_11 | | | | | | | | | | | | | | | |
|-------|---|--------------------------|-------|--------------------------|-------|------------------|-------|--------|--|--|--|--|--|--|-----|
| MSB | | | | | | | | BYTE 1 | | | | | | | LSB |
| ADDR. | | Delay time high cur. CP2 | | Delay time high cur. CP1 | | x | HCDEL | | | | | | | | |
| 1 | 1 | ON/OFF | HI/LO | ON/OFF | HI/LO | 0 ⁽¹⁾ | 1/0 | | | | | | | | |
| x | x | 23 | 22 | 21 | 20 | 19 | 18 | | | | | | | | |

Note: 1. Value has to be 0.

| A8_10 | | | | | | | | | | | | | | | |
|-------|---|-------|--------|----------------|----------------|----------------|----------------|--------|--|--|--|--|--|--|-----|
| MSB | | | | | | | | BYTE 1 | | | | | | | LSB |
| ADDR. | | AM/FM | IF-AGC | RF-AGC | | | | | | | | | | | |
| 1 | 0 | 1/0 | 1/0 | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | | | | | | | | |
| x | x | 17 | 16 | 15 | 14 | 13 | 12 | | | | | | | | |

| A8_01 | | | | | | | | | | | | | | | |
|-------|---|-------|-------|----------------|----------------|----------------|----------------|--------|--|--|--|--|--|--|-----|
| MSB | | | | | | | | BYTE 1 | | | | | | | LSB |
| ADDR. | | IF-IN | VCO | IF-Gain | | | | | | | | | | | |
| 0 | 1 | AM/FM | HI/LO | 2 ³ | 2 ² | 2 ¹ | 2 ⁰ | | | | | | | | |
| x | x | 11 | 10 | 9 | 8 | 7 | 6 | | | | | | | | |

| A8_00 | | | | | | | | | | | | | | | |
|-------|---|-------|------------|------------------|----------------|----------------|----------------|--------|--|--|--|--|--|--|-----|
| MSB | | | | | | | | BYTE 1 | | | | | | | LSB |
| ADDR. | | N2/N1 | PLL ON/OFF | PD TE/PD | IF-AGC | | | | | | | | | | |
| 0 | 0 | 1/0 | 1/0 | 0 ⁽¹⁾ | 2 ² | 2 ¹ | 2 ⁰ | | | | | | | | |
| x | x | 5 | 4 | 3 | 2 | 1 | 0 | | | | | | | | |

Note: 1. Value has to be 0.

10. Bus Control

10.1 IF-AGC

The IF-AGC controls the level of the IF signal that is passed to the external ceramic filter and the IF input (AM pin 35 or FM pin 36 and pin 34). In AM mode the time constant can be selected by the external capacitors at pin 32 (IFAGCA1) and pin 10 (IFAGCA2) and in FM mode by an external capacitor at pin 31 (IFAGCFM). In AM mode, the double pole (by the capacitors at pin 32 and pin 10) allows a better harmonic distortion by a lower time constant.

The IF-AGC threshold can be controlled by setting bits 0 to 2 as given in [Table 10-1](#).

Table 10-1. IF-AGC Threshold

| IF-AGC | B2 | B1 | B0 |
|----------------|----|----|----|
| 109 dB μ V | 0 | 0 | 0 |
| 111 dB μ V | 0 | 0 | 1 |
| 113 dB μ V | 0 | 1 | 0 |
| 115 dB μ V | 0 | 1 | 1 |
| 117 dB μ V | 1 | 0 | 0 |
| 118 dB μ V | 1 | 0 | 1 |
| 119 dB μ V | 1 | 1 | 0 |
| 121 dB μ V | 1 | 1 | 1 |

The IF-AGC ON/OFF can be controlled by bit 16 as given in [Table 10-2](#).

Table 10-2. IF-AGC

| IF-AGC ON/OFF | B16 |
|---------------|-----|
| IF-AGC ON | 0 |
| IF-AGC OFF | 1 |

10.2 PD Test

A special test mode for PD is implemented for final production test only. This mode is activated by setting bit 3 = 1. This mode is not intended to be used by customer application. For normal operation bit 3 has to be set to 0.

Table 10-3. PD-Test Mode

| PD TE/PD | B3 |
|---------------------------------|----|
| Pin 17 = AMLF output (standard) | 0 |
| Pin 17 = PD Test mode | 1 |

10.3 N1/N2

The N2/N1 bit controls the active N-divider. Only one of the two N-Divider can be active. The N1-Divider is activated by setting bit 5 = 0, the N2-Divider by setting bit 5 = 1.

Table 10-4. N-Divider

| N2/N1 | B5 |
|-------------------|----|
| N1-divider active | 0 |
| N2-divider active | 1 |

10.4 IF Amplifier

The IF gain amplifier can be used in AM and FM mode to compensate the loss of the external ceramic bandfilters.

The IF gain can be controlled in 2-dB steps by setting bit 6 to bit 9 as given in [Table 10-5](#).

Table 10-5. IF Gain

| IF Gain | B9 | B8 | B7 | B6 |
|---------|-----|-----|-----|-----|
| 12 dB | 0 | 0 | 0 | 0 |
| 14 dB | 0 | 0 | 0 | 1 |
| 16 dB | 0 | 0 | 1 | 0 |
| 18 dB | 0 | 0 | 1 | 1 |
| 20 dB | 0 | 1 | 0 | 0 |
| ... | ... | ... | ... | ... |
| 40 dB | 1 | 1 | 1 | 0 |
| 42 dB | 1 | 1 | 1 | 1 |

The selection of the IF amplifier input can be controlled by bit 11 as given in [Table 10-6](#).

Table 10-6. IF-IN Operating Mode

| IF-IN AM/FM | B11 |
|-------------|-----|
| IF-IN FM | 0 |
| IF-IN AM | 1 |

The AM input (pin 35) has an input impedance of 2.5 k Ω for matching with a crystal filter. The FM input (pin 36) has an input impedance of 330 Ω for matching with a ceramic filter.

10.5 VCO

The VCO HI/LO function is controlled by means of bit 10.

Table 10-7. VCO Operating Mode

| VCO HI/LO | B10 |
|------------------|-----|
| VCO high current | 0 |
| VCO low current | 1 |

10.6 RF-AGC

The AM and FM RF-AGC controls the current into the AM and FM pin diodes (FM pin 3 and AM pin 9) to limit the level at the AM or FM mixer input. If the level at the AM or FM mixer input exceeds the selected threshold, then the current into the AM or FM pin diodes increases. If this step is not sufficient in AM mode, the source drain voltage of the MOSFET (pin 11) can be decreased. In AM mode, the time constants can be selected by the external capacitors at pin 42 (RFAGCA1) and at pin 12 (RFAGCAM2) and in FM mode by an external capacitor at pin 33 (RFAGCFM). In AM mode, the double pole (by the capacitors at pin 42 and pin 12) allows a better harmonic distortion by a higher time constant.

The RF-AGC can be controlled in 1-dB steps by setting the bits 12 to 15. The values for FM and AM are controlled by bit 17.

Table 10-8. RF-AGC

| RF-AGC AM | RF-AGC FM | B15 | B14 | B13 | B12 |
|----------------|----------------|-----|-----|-----|-----|
| 88 dB μ V | 91 dB μ V | 0 | 0 | 0 | 0 |
| 89 dB μ V | 92 dB μ V | 0 | 0 | 0 | 1 |
| 90 dB μ V | 93 dB μ V | 0 | 0 | 1 | 0 |
| 91 dB μ V | 94 dB μ V | 0 | 0 | 1 | 1 |
| 92 dB μ V | 95 dB μ V | 0 | 1 | 0 | 0 |
| ... | ... | ... | ... | ... | ... |
| 102 dB μ V | 105 dB μ V | 1 | 1 | 1 | 0 |
| 103 dB μ V | 106 dB μ V | 1 | 1 | 1 | 1 |

10.7 Reception Mode

There are two different operation modes, AM and FM, which are selected by means of bit 17 and bit 145 according to [Table 9-1 on page 12](#) and [Table 10-1 on page 14](#). In AM mode (bit 17 = 1), the AM mixer, the AM RF-AGC, the AM divider (prescaler) and the IF AM amplifier (input at pin 35) are activated. In FM mode (bit 17 = 0), the FM mixer, the FM RF-AGC and the IF FM amplifier (input at pin 36) are activated.

In AM or FM reception mode, bit 145 has to be set to the corresponding mode. The buffer amplifier input can be connected to pin 16 (with the external FM loop filter) by bit 145 = 0 and to pin 17 (with the external AM loopfilter) by bit 145 = 1.

The AM/FM function for the tuner part is controlled by bit 17 as given in [Table 10-9](#).

Table 10-9. Tuner Operating Modes

| AM/FM | B17 |
|-------|-----|
| FM | 0 |
| AM | 1 |

10.8 PLL

The PLL can switch off by bit 4 = 0. In this case, the N-Divider input signal is internally connected to ground.

Table 10-10. PLL Mode

| PLL ON/OFF | B4 |
|------------|----|
| PLL OFF | 0 |
| PLL ON | 1 |

10.9 HCDEL

There are two registers, HCDEL 1 (bits 20 and 21) and HCDEL 2 (bits 22 and 23), to control the delay time of the high-current charge pump and to deactivate them. bit 18 (HCDEL) determines whether register HCDEL 1 or 2 is used.

Table 10-11. High-current Charge Pump Delay Time Register

| HCDEL 1/2 Select Mode | HCDEL (B18) |
|-----------------------|-------------|
| HCDEL 1 | 0 |
| HCDEL 2 | 1 |

If bits 20 and 21 (HCDEL 1) or bits 22 and 23 (HCDEL 2) are both set to 0, then the high-current charge pump is deactivated. Otherwise, the delay time can be selected as described in [Table 10-12](#).

Table 10-12. Delay Time of HCDEL Register

| High-current Charge Pump | B21/B23 | B20/B22 |
|--------------------------|---------|---------|
| OFF | 0 | 0 |
| Delay time 5 ns | 0 | 1 |
| Delay time 10 ns | 1 | 0 |
| Delay time 15 ns | 1 | 1 |

10.10 2-bit Shift

A divider 2-bit shift (bit 32 = 0) allows faster frequency changes by using a four times higher step frequency (e.g., $f_{PDF} = 50$ kHz instead of $f_{PDF} = 12.5$ kHz). If the PLL is locked (after the frequency change), the normal step frequency (e.g., $f_{PDF} = 12.5$ kHz) will be active again.

If no 2-bit shift is used (bit 32 = 1), the frequency changes will be done with the normal step frequency (12.5 kHz).

In 2-bit shift mode the N- and R-divider are shifted by two bits to the right (this corresponds by a R- and N-divider division by 4). An important condition for this mode is that the R-divider has to be a multiple of 4.

Table 10-13. Manual and Lock Detect Shift Mode

| 2-bit Shift | B32 |
|----------------------|-----|
| Dividers 2-bit shift | 0 |
| No shift | 1 |

10.11 SW1 (Pin 13)

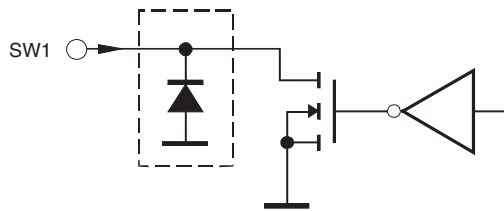
The switching output SW1 (pin 13) is controlled by bit 46 as given in [Table 10-14](#).

Table 10-14. Switching Output

| SW1 | B46 |
|------|-----|
| High | 0 |
| Low | 1 |

Note: SW1 is an open-drain output.

Figure 10-1. Internal Components at SW1



10.12 SW2/AGC (Pin 11)

The pin SW2/AGC works as a switching output (open drain, pin 11) or as an AM AGC-control pin to control the cascade stage of an external AM-preamplifier.

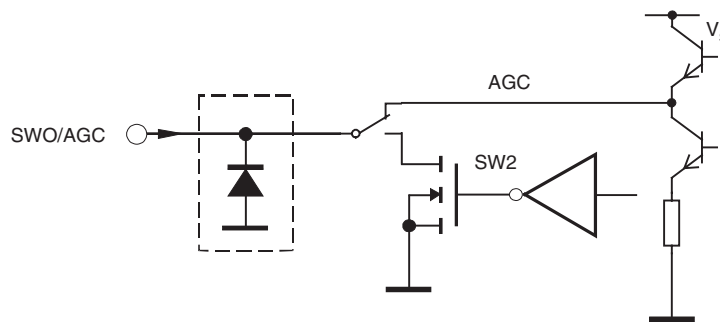
The SW2/AGC is controlled by bits 47 and 48 as given in [Table 10-15](#).

Table 10-15. Switching Output 2/AGC Mode

| SW2/AGC | B48 | B47 |
|--------------|-----|-----|
| AGC function | 0 | X |
| High | 1 | 0 |
| Low | 1 | 1 |

Note: In AGC mode, the output voltage is 6V down to 1V.

Figure 10-2. Internal Components at SW2/AGC



10.13 Test Mode

A special test mode is implemented for final production test only. This mode is activated by setting bit 123 = 1. This mode is not intended to be used by customer application. For normal operation bit 123 has to be set to 0.

Table 10-16. Test Mode

| Test Mode | B123 |
|-----------|------|
| ON | 1 |
| OFF | 0 |

10.14 AM Mixer

The AM mixer is used for up-conversion of the AM reception frequency to the IF frequency. Therefore, an AM prescaler is implemented to generate the necessary LO frequency from the VCO frequency.

The VCO divider can be controlled by the bits 140 to 143 as given in [Table 10-17](#). (The VCO divider is only active in AM mode)

Table 10-17. Divider Factor of the AM Prescaler

| Divider AM Prescaler | B143 | B142 | B141 | B140 |
|----------------------|------|------|------|------|
| Divide by 2 | 0 | 0 | 0 | 0 |
| Divide by 3 | 0 | 0 | 0 | 1 |
| Divide by 4 | 0 | 0 | 1 | 0 |
| Divide by 5 | 0 | 0 | 1 | 1 |
| Divide by 6 | 0 | 1 | 0 | 0 |
| Divide by 7 | 0 | 1 | 0 | 1 |
| Divide by 8 | 0 | 1 | 1 | 0 |
| Divide by 9 | 0 | 1 | 1 | 1 |
| Divide by 10 | 1 | x | x | x |

10.15 FM Mixer

In the FM mixer stage, the FM reception frequency is down-converted to the IF frequency. The VCO frequency is used as LO frequency for the mixer.

10.16 PLL Loop Filter

The PLL loop filter selection for AM and FM mode can be controlled by bit 145 as given in [Table 10-18](#).

Table 10-18. Loop Filter Operating Mode

| PDAM/PDFM | B145 |
|-------------|------|
| PDFM active | 0 |
| PDAM active | 1 |

10.17 Fractional Mode

The activated fractional mode (bit 144 = 0) in connection with the direct shift (bit 32 = 0) allows fast frequency changes (with the help of the 2-bit shift) with a four times higher step frequency. After the frequency change, the normal step frequency is active again.

If the fractional mode is deactivated (bit 144 = 1) and direct shift mode is active, (bit 32 = 0) the VCO frequency is set to the next lower frequency which is many times the amount frequency of 4 times step frequency. This means that the 2 shifted bits of the active N-Divider are not used in this mode. The shift bits are interpreted as logic 0.

The fractional mode with direct shift mode deactivated (bit 32 = 1) allows normal frequency changes with a step frequency of 12.5 kHz.

Table 10-19. Fractional Mode

| Fractional | B144 |
|------------|------|
| ON | 0 |
| OFF | 1 |

10.18 Spurious Suppression

In fractional and direct shift mode the spurious suppression is able by SW wire and SW impulse.

Table 10-20. Spurious Suppression by SW Wire

| SW Wire | B60 |
|---------|-----|
| OFF | 0 |
| ON | 1 |

Table 10-21. Spurious Suppression by Correction Current Charge Pump

| SW Impulse | B61 |
|------------|-----|
| OFF | 0 |
| ON | 1 |

10.19 Charge Pump (AMLF/FMLF)

AMLF/FMLF is the current charge pump output of the PLL. The current can be controlled by setting the bits 62 and 63. The loop filter has to be designed correspondingly to the chosen pump current and the internal reference frequency.

During the frequency change, the high-current charge pump (bit 62) is active to enable fast frequency changes. After the frequency change, the current will be reduced to guarantee a high S/N ratio. The low-current charge pump (bit 63) is then active. The high current charge pump can also be switched off by setting the bits of the active HCDEL register to 0 (bit 20 and bit 21 [HCDEL 1] or bit 22 and bit 23 [HCDEL 2]).

The current of the high-current charge pump is controlled by bit 62 as given in [Table 10-22](#).

Table 10-22. High-current Charge Pump

| High-current Charge Pump | B62 |
|--------------------------|-----|
| 1 mA | 0 |
| 2 mA | 1 |

The current of the low-current charge pump is controlled by bit 63 as given in [Table 10-23](#).

Table 10-23. Low-current Charge Pump

| Low Current Charge Pump | B63 |
|-------------------------|-----|
| 50 μ A | 0 |
| 100 μ A | 1 |

10.20 External Voltage at AMLF (Oscillator)

The oscillator (pin 22) can be switched on/off by bit 65. It is possible to use the oscillator buffer as an input or as an output. At the AMLF (pin 17), an external tuning voltage can be applied (bit 65 = 0). If this is not done, the IC operates in standard mode (bit 65 = 1).

The oscillator, oscillator buffer and the AMLF are controlled by the bits 65 and 64 as given in [Table 10-24 on page 22](#).

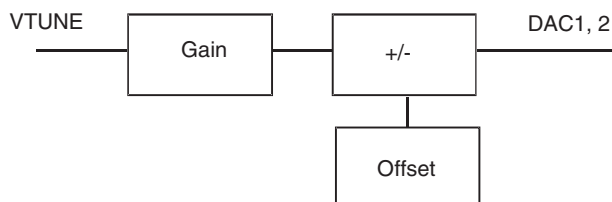
Table 10-24. Oscillator Operating Modes

| Oscillator | Oscillator Buffer | AMLF (Pin 17) | B65 | B64 |
|------------|-------------------|-----------------|-----|-----|
| OFF | INPUT | INPUT f. DAC's | 0 | X |
| ON | OFF | AMLF (standard) | 1 | 0 |
| ON | OUTPUT | AMLF (standard) | 1 | 1 |

10.21 DAC1, 2 (Pins 1, 2)

For automatic tuner alignment, the DAC1 and DAC2 of the IC can be controlled by setting gain and offset values. The principle of the operation is shown in Figure 10-3. The gain is in the range of $0.67 \times V_{TUNE}$ to $2.09 \times V_{TUNE}$. The offset range is +0.98V to -0.98V. For alignment, DAC1 and DAC2 are connected to the varicaps of the preselection filter and the IF filter. For alignment, offset and gain are set for having the best tuner tracking.

Figure 10-3. Block Diagram of DAC1, 2



The gain of DAC1 and DAC2 has a range of approximately $0.67 \times V(TUNE)$ to $2.09 \times V(TUNE)$. This range is divided into 255 steps. One step is approximately $(2.09 - 0.67)/255 = 0.00557 \times V(TUNE)$. The gain of DAC1 can be controlled by the bits 38 to 45 (2^0 to 2^7) and the gain of DAC2 can be controlled by the bits 66 to bit 73 (2^0 to 2^7) as given in Table 10-25.

Table 10-25. Gain of DAC1, 2

| Gain DAC1 Approximately | B45 | B44 | B43 | B42 | B41 | B40 | B39 | B38 | Decimal Gain |
|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|--------------|
| Gain DAC2 Approximately | B73 | B72 | B71 | B70 | B69 | B68 | B67 | B66 | Decimal Gain |
| $0.6728 \times V(TUNE)$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0.6783 \times V(TUNE)$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| $0.6838 \times V(TUNE)$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| $0.6894 \times V(TUNE)$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| $0.9959 \times V(TUNE)$ | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 58 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| $2.0821 \times V(TUNE)$ | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 253 |
| $2.0877 \times V(TUNE)$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 254 |
| $2.0932 \times V(TUNE)$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 255 |

Note: Offset = 64 (intermediate position)

The offset of DAC1 and DAC2 has a range of approximately +0.98 V to -0.99 V. This range is divided into 127 steps. One step is approximately $1.97 \text{ V}/127 = 15.52 \text{ mV}$. The offset of DAC1 can be controlled by the bits 24 to bit 30 (2^0 to 2^6) and the offset gain of DAC2 can be controlled by the bits 52 to bit 58 (2^0 to 2^6) as given in [Table 10-26](#).

Table 10-26. Offset of DAC1, 2

| Offset DAC1 Approximately | B30 | B29 | B28 | B26 | B26 | B25 | B24 | Decimal Offset |
|------------------------------|-----|-----|-----|-----|-----|-----|-----|----------------|
| Offset DAC2 Approximately | B58 | B57 | B56 | B55 | B54 | B53 | B52 | Decimal Offset |
| 0.9815V | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0.9659V | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0.9512V | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0.9353V | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| ... | | ... | ... | ... | ... | ... | ... | ... |
| -0.0120V | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 64 |
| ... | | ... | ... | ... | ... | ... | ... | ... |
| -0.9576V | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 125 |
| -0.9733V | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 126 |
| -0.9890V | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |

Note: Gain = 58 (intermediate position)

10.22 Permitted DAC Conditions

The internal operation amplifier of the DACs should not operate with a too high internal difference voltage at their inputs. This means that a voltage difference higher than 0.5V at the internal OP input should be avoided in operation mode. The respective output OP in the DAC is necessary for the addition and amplification of the tuning voltage (at pin 18) with the desired voltage gain and offset value.

If the tuning voltage reaches a high value e.g. 9V, with a gain setting of 2 times VTUNE and an offset of +1V, then the output OP of the DAC should reach the (calculated) voltage of 19V. The supply voltage of e.g. 10V, however, limits the output voltage (of the DAC) to 10V maximum.

Due to the (limiting) supply voltage and the internal gain resistance ratio of 6, the missing 9V (calculated voltage - V_s) cause a voltage of 1.5V at the OP input. This condition may not remain for a longer period of time.

As long as the calculated DAC output voltage value does not exceed the supply voltage value by more than 3V, no damages should occur during the product's lifetime as the input voltage of the internal OP input voltage does not exceed 0.5V.

$$VTUNE \times \text{DAC gain factor} + \text{DAC offset} < V_s + 3V$$

$$(9V \times 2 + 1V) < 10V + 3V \text{ (condition not allowed)}$$

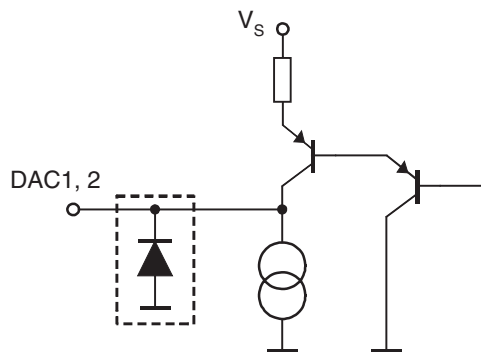
This means when having a gain factor of 2 and an offset value of 1V, the tuning voltage should not exceed 6V.

Maximum tuning voltage < $(V_S + 3\text{ V} - \text{DAC offset})/\text{DAC gain factor}$

e.g.: maximum tuning voltage = $(10\text{V} + 3\text{V} - 1\text{V})/2 = 6\text{V}$

It is also possible to reduce the gain or the offset value instead of (or along with) the tuning voltage.

Figure 10-4. Internal Components of DAC1, 2

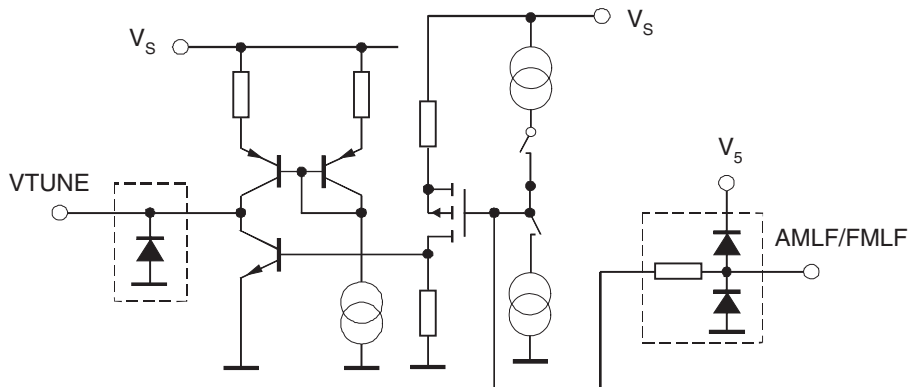


11. Input/Output Interface Circuits

11.1 VTUNE, AMLF and FMLF (Pins 16-18)

VTUNE is the loop amplifier output of the PLL. The bipolar output stage is a rail-to-rail amplifier.

Figure 11-1. Internal Components at VTUNE, AMLF and FMLF



11.2 EN, DATA, CLK (Pins 23-25)

All functions can be controlled via a 3-wire bus consisting of Enable, Data and Clock. The bus is designed for microcontrollers which can operate with 3-V supply voltage. Details of the data transfer protocol can be found in [Section 8. "3-wire Bus Description"](#) on page 10.

Figure 11-2. Internal Components at Enable, Data and Clock

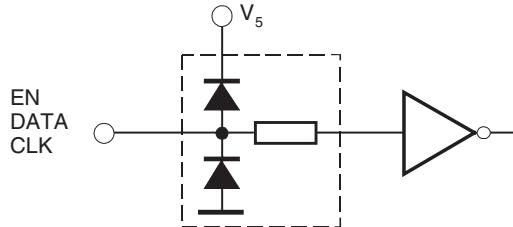
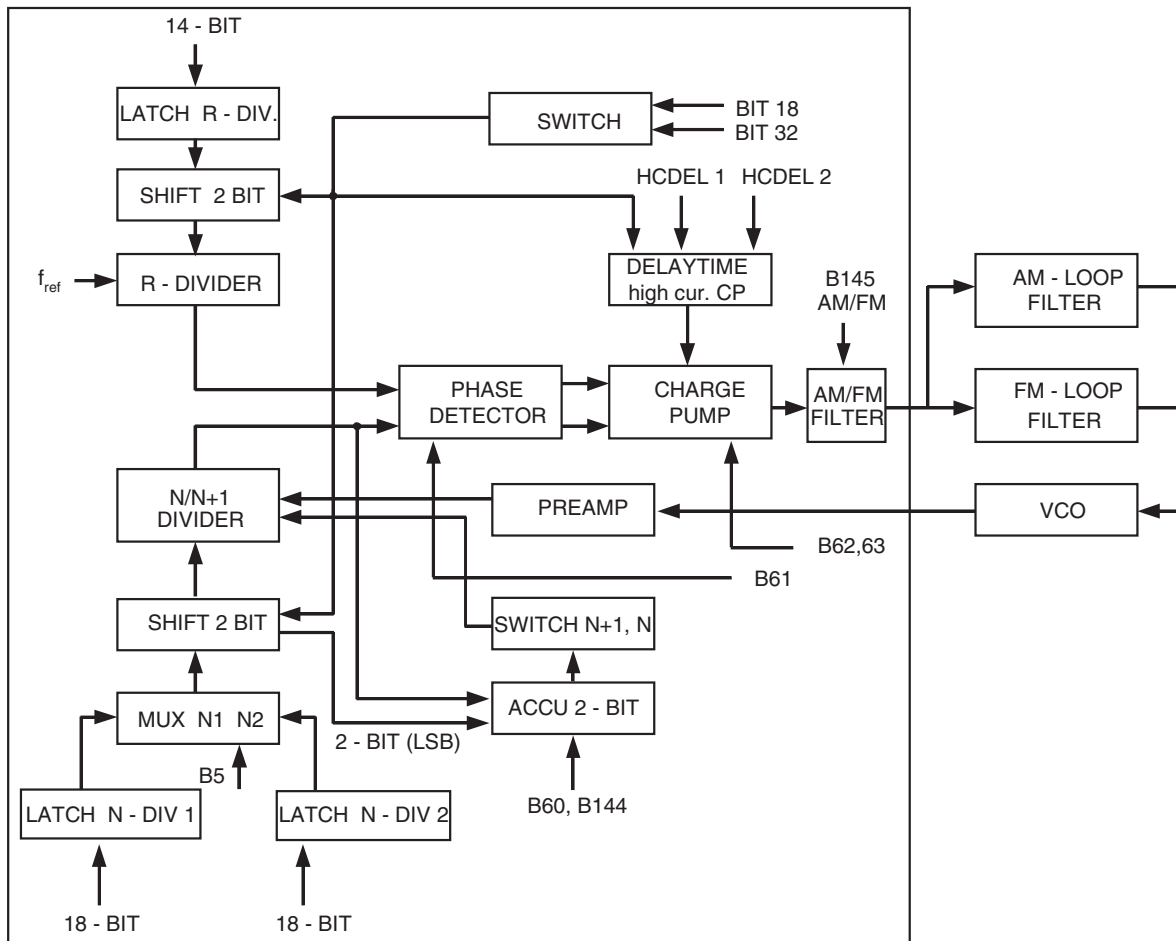


Figure 11-3. Block Diagram of the PLL Core



11.3 PLL Core Block Diagram Description

The two N-dividers are stored in two 18-bit memory register (LATCH N-DIV) and the R-divider in a 14-bit memory register (LATCH R-DIV). One of the two N-dividers (N1 or N2) can be activated by bit 5 as active N-divider (with the 18-bit multiplexer MUX).

The (divider) 2-bit shift mode can be activated with bit 32 = 0. The N- and R-divider are shifted two bits to the right in this shift mode. Because the two lowest R-divider bits (bit 124 and bit 125) are 0 they do not have to be evaluated. In opposite to the R-divider the lowest two N-divider bits (bit 102 and bit 103 or bit 80 and bit 81, depends on the active N-divider) are special evaluated in the ACCU block if fractional mode is active (bit 144 = 0). The two lowest N- and R-divider bits are also called shift bits.

The SWITCH N+1, N block is steering the division through N or N+1 in the N-divider if fractional and 2-bit shift mode are active. There is only a division by N if the fractional mode is deactivated in 2-bit shift mode.

The output signals of the 18-bit N-divider and 14-bit R-divider will be compared in the PHASEDETECTOR which one activates the sink and source currents of the charge pumps (CP).

There are also two HCDEL registers (for the high current CP delay time) but only one of them is active. One of the HCDEL registers can be activated by bit 18. The delay time of the HCDEL register can be selected with bit 20 and bit 21 or bit 22 and bit 23). The current for the high CP (HCCP) can be set by bit 62 and the current for the low current CP (LCCP) by bit 63.

With bit 145 the AM- or FM-Loopfilter (pin) can be activated. It is also possible to use the AM-Loopfilter in FM mode (instead of the FM-Loopfilter) or the FM-Loopfilter in AM mode.

11.4 High-speed Tuning

The fractional mode (bit 144 = 0) in connection with the direct shift mode (bit 32 = 0) allows very fast frequency changes with four times the step frequency ($50 \text{ kHz} = 4 \times f_{\text{PDF}}$) at low frequency steps (e.g., $f_{\text{PDF}} = 12.5 \text{ kHz}$). In direct shift mode, the R- and the N-divider are shifted by 2 bits to the right (this corresponds to a R- and N-divider division by 4 or a step frequency multiplication by 4).

Due to the 2-bit shift, a faster tuning response time of approximately 1 ms instead of 3-4 ms for a tune over the whole FM band from 87.5 MHz to 108 MHz is possible with $f_{\text{PDF}} = 12.5 \text{ kHz}$.

If the FM receiving frequency is 103.2125 MHz (with e.g. $f_{\text{PDF}} = 12.5 \text{ kHz}$ and $f_{\text{IF}} = 10.7 \text{ MHz}$), an N-divider of 9113 and an R-divider of 12 are necessary when using a reference-frequency (f_{ref}) of 150 kHz.

$$f_{\text{VCO}} = f_{\text{IF}} + f_{\text{rec}} = 10.7 \text{ MHz} + 103.2125 \text{ MHz} = 113.9125 \text{ MHz}$$

$$f_{\text{PDF}} = f_{\text{VCO}}/N = f_{\text{ref}}/R = 113.9125 \text{ MHz}/9113 = 150 \text{ kHz}/12 = 12.5 \text{ kHz}$$

An important condition for the use of the fractional mode is an R-divider with an integer value after the division by 4 (R-dividers have to be a multiple of 4).

After a 2-bit shift (divider division by 4), the R-divider is now 3 (instead of 12) and the N-divider is 2278.25 (instead of 9113). The new N-divider of 2278.25 is also called $\frac{1}{4}$ fractional step because the modulo value of the N-divider is $0.25 = \frac{1}{4}$. In total, there are 4 different fractional 2-bit shift steps: full, $\frac{1}{4}$, $\frac{1}{2}$ and $\frac{3}{4}$ step.

If the fractional mode is switched off (bit 144 = 1) during direct shift mode (bit 32 = 0), the modulo value of the N-divider will be ignored (the new N-divider is then 2278 instead of 2278.25). This means that the PLL locks on the next lower multiple frequency of $4 \times f_{PDF}$ (in our case $f_{PDF} = 12.5$ kHz). The new VCO frequency (f_{VCO}) is then 113.9 MHz (instead of 113.9125 MHz in fractional mode).

Also the PLL has additionally a special fractional logic which allows a good spurious suppression in the fractional and direct shift mode. Activating the wire switch (bit 60 = 1) and the correction charge pump (bit 60 = 1) the spurious suppression is active.

11.5 Charge Pump Current Settings

Bit 62 (0 = 1 mA; 1 = 2 mA) allows to adjust the high current, which is active during a frequency change (if the delay time of the active HCDEL register is not switched off). A high charge pump current allows faster frequency changes. After a frequency change, the current reduction is reduced (in locked mode) to the low current which is set by bit 63 (0 = 50 μ A; 1 = 100 μ A). A lower charge pump current guarantees a higher S/N ratio.

The high current charge pump can be switched off by the active HCDEL register bits. In this case, when HCDEL 1 is active and the bits 20 and 21 are 0 (HCDEL 1 delay time = off) or HCDEL 2 is active and the bits 22 and 23 are 0 (HCDEL 2 delay time = off), only the low current charge pump (current) is active in locked and in the frequency change mode.

11.6 AM Prescaler (Divider) Settings

The AM mixer is used for up-conversion of the AM reception frequency to the IF frequency. Therefore, an AM prescaler is implemented to generate the necessary LO from the VCO frequency. For the reception of the AM band, different prescaler (divider) settings are possible.

[Table 11-1 on page 29](#) lists the AM prescaler (divider) settings and the reception frequencies.

$$f_{VCO} = 98.2 \text{ MHz to } 124 \text{ MHz}$$

$$f_{IF} = 10.7 \text{ MHz}$$

$$f_{rec} = f_{VCO} - f_{IF}$$

$$f_{VCO} = \text{AM prescaler} \times (f_{rec} + f_{IF})$$

The following formula can also be useful by AM frequencies higher than 20 MHz:

$$f_{VCO} = \text{AM prescaler} \times (f_{rec} - f_{IF})$$

Table 11-1. AM Prescaler (Divider) Settings and the Reception Frequencies

| Divider (AM Prescaler) | Minimum Reception Frequency [MHz] | Maximum Reception Frequency [MHz] |
|------------------------|-----------------------------------|-----------------------------------|
| No divider | 87.5 | 113.3 |
| Divide by 2 | 38.4 | 51.3 |
| Divide by 3 | 22.033 | 30.633 |
| Divide by 4 | 13.85 | 20.3 |
| Divide by 5 | 8.94 | 14.1 |
| Divide by 6 | 5.667 | 9.967 |
| Divide by 7 | 3.329 | 7.014 |
| Divide by 8 | 1.575 | 4.8 |
| Divide by 9 | 0.211 | 3.078 |
| Divide by 10 | 0 | 1.7 |

Note: The AM Prescaler Divider Settings with f_{VCO} from 98.2 MHz to 124 MHz is only an example. The tuning range depends on the tuning diode and the inductor in the VCO circuit. The tank of the VCO should be designed for a maximum range at pin 18 (VTUNE) of 1.5 V to $V_{SPLL} - 1$ V for a good S/N performance.

The N- and R- divider can be calculated as following:

$$\begin{aligned}
 N &= \text{AM Prescaler} \times (f_{\text{rec}} + f_{\text{IF}})/f_{\text{step}} && \text{(AM mode)} \\
 N &= (f_{\text{rec}} + f_{\text{IF}})/f_{\text{step}} && \text{(FM mode)} \\
 R &= f_{\text{ref}}/f_{\text{step}} && \text{(For all modes)} \\
 f_{VCO} &= N \times f_{\text{step}} \\
 f_{\text{ref}} &= \text{reference oscillator frequency (pin 27)}
 \end{aligned}$$

Example of AM settings:

If the receiving frequency is 0.84 MHz (AM) and the following conditions are:

$f_{\text{ref}} = 4$ MHz; $f_{\text{step}} = 10$ kHz; $f_{\text{IF}} = 10.7$ MHz and an AM-Prescaler of 10 a N-Divider of 11540 and a R-Divider of 400 is necessary.

$$R = f_{\text{ref}}/f_{\text{step}} = 4 \text{ MHz}/10 \text{ KHz} = 400$$

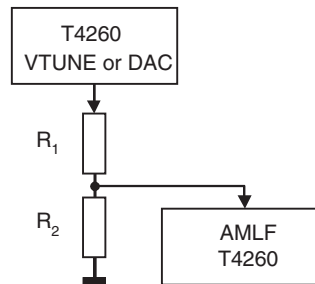
$$N = \text{AM Prescaler} \times (f_{\text{rec}} + f_{\text{IF}})/f_{\text{step}} = 10 \times (0.84 \text{ MHz} + 10.7 \text{ MHz})/10 \text{ KHz} = 11540$$

11.7 External Voltage at AMLF (Pin 17)

By using two ICs, for example, it is possible to operate the AMLF (pin 17) of the second IC either with the tuning voltage (VTUNE [pin 18]), the DAC 1 voltage [pin 1] or the DAC 2 voltage [pin 2] from the first T4260. For voltage reduction at the AMLF [pin 17], a voltage factor ratio of 100/16 (R_1/R_2) is required.

This means that an applied voltage from 0.5 V at pin 17 (AMLF) corresponds to a tuning voltage of 3.625V. It is recommended to use R_1 with 100 k Ω and R_2 with 16 k Ω . The allowed range of R_1 is 10 k Ω to 1 M Ω and 1.6 k Ω to 160 k Ω for R_2 .

Figure 11-4. External Voltage at AMLF (Pin 17)



The maximum input voltage at the AMLF input (pin 17) depends on the applied supply voltage as well as on the gain and offset settings. To avoid any damages during the product's lifetime, the following formulas regarding SWAMLF voltage, gain and offset settings have to be observed (see [Section 10.22 "Permitted DAC Conditions" on page 24](#)).

$$V_{\text{SWAMLF}} \times ([R_1 + R_2]/R_2) \times \text{DAC gain factor} + \text{DAC offset} < V_S + 3V$$

$$(R_1 + R_2)/R_2 = 7.25$$

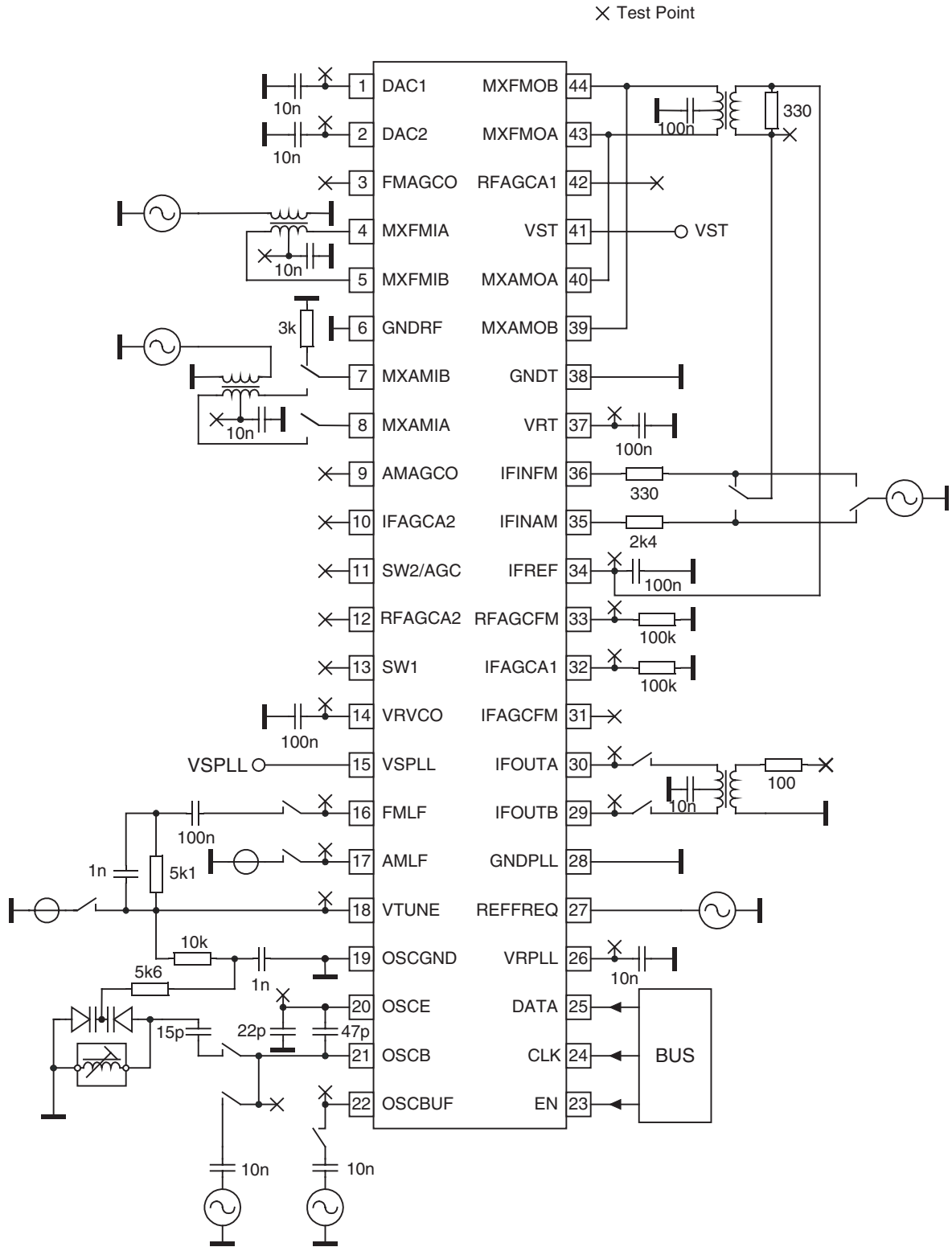
This means when having a gain factor of 2 and an offset value of 1V, the applied SWAMLF voltage should be limited to a voltage lower than 0.83V.

$$\text{SWAMLF voltage} < (V_S + 3V - \text{DAC offset}) / (\text{DAC gain factor} \times 7.25)$$

$$\text{e.g.: maximum SWAMLF voltage} = (10V + 3V - 1V) / (2 \times 7.25) = 0.83V$$

It is also possible to reduce the gain or offset instead (or along with) the SWAMLF voltage.

Figure 11-5. Test Circuit



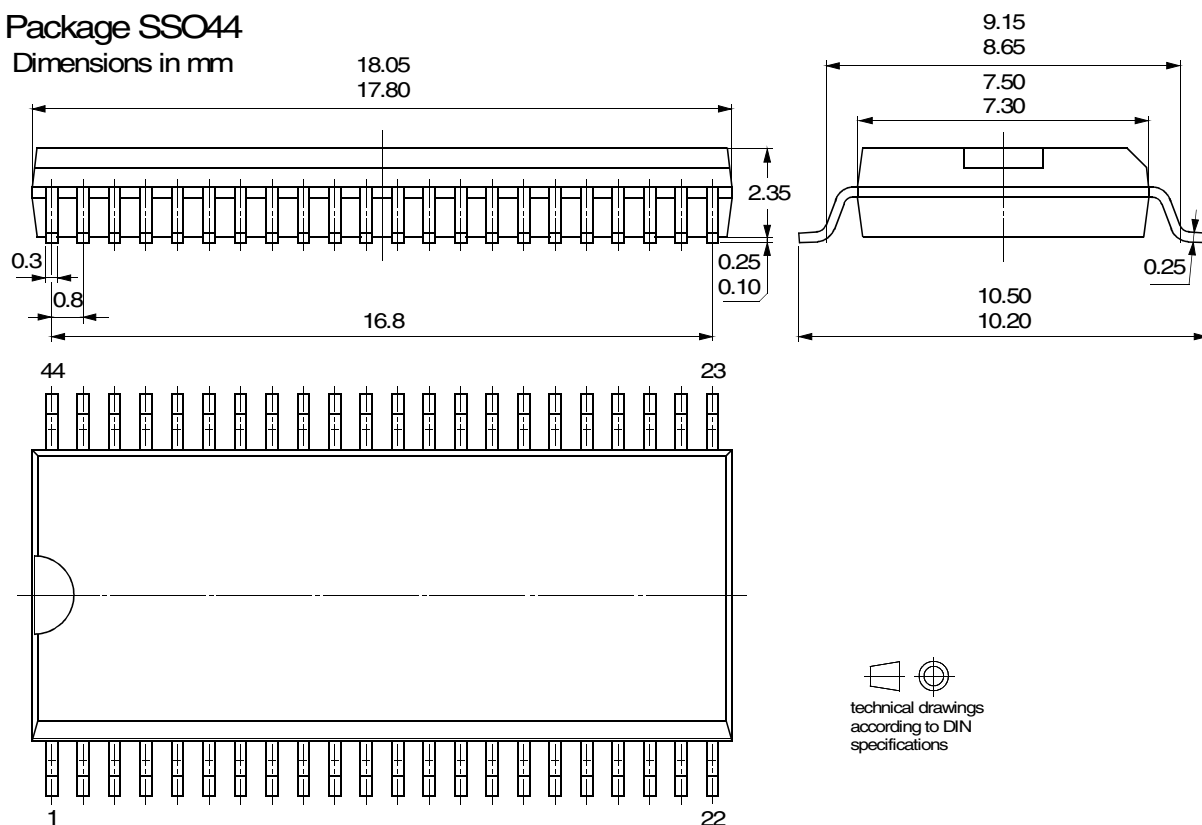
12. Ordering Information

| Extended Type Number | Package | Remarks |
|----------------------|---------------|------------------|
| T4260-ILSH | Pb-free SSO44 | Tube |
| T4260-ILQH | Pb-free SSO44 | Taped and reeled |

13. Package Information

Package SSO44

Dimensions in mm



14. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|------------------|---|
| 4528L-AUDR-05/07 | <ul style="list-style-type: none"> Put datasheet in a new template Number 6.4 in section 7 "Electrical Characteristics" on page 6 added |
| 4528K-AUDR-03/07 | <ul style="list-style-type: none"> Put datasheet in a new template Pb-free logo on page 1 deleted Table 10-8 "RF-AGC" on page 17 changed |



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