

Helping Customers Innovate, Improve & Grow

Features

- Any frequency between 1 MHz and 220 MHz accurate to 6 decimal places
- LVPECL and LVDS output signaling types
- 0.6ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 3.2mm x 2.5mm, 5.0 mm x 3.2 mm and 7.0 mm x 5.0 mm

Applications

- SONET, Synchronous Ethernet, SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express
- Telecom, networking, broadband, instrumentation

Performance Specifications

Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
LVPECL and LVDS, Common AC Characteristics						
Output Frequency Range	f	1	–	220	MHz	
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of Initial tolerance at 25 °C, and variations over operating temperature, aging, supply voltage and load
		-50	–	+50	PPM	
First Year Aging		-2	–	+2	PPM	25°C
10-year Aging		-5	–	+5	PPM	25°C
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Start-up Time	T_start	–	–	10	ms	
Duty Cycle	DC	45	–	55	%	Contact Vectron for tighter duty cycle
LVPECL, DC and AC Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Maximum Output Current	I-driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 1
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 1
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 1
Rise/Fall Time	Tr, Tf	–	300	500	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.6	0.85	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
LVDS, DC and AC Characteristics						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	47	55	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = Low
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Low
Differential Output Voltage	VOD	200	350	500	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	Tr, Tf	–	495	600	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	115	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.6	1.0	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

Typical Phase Noise

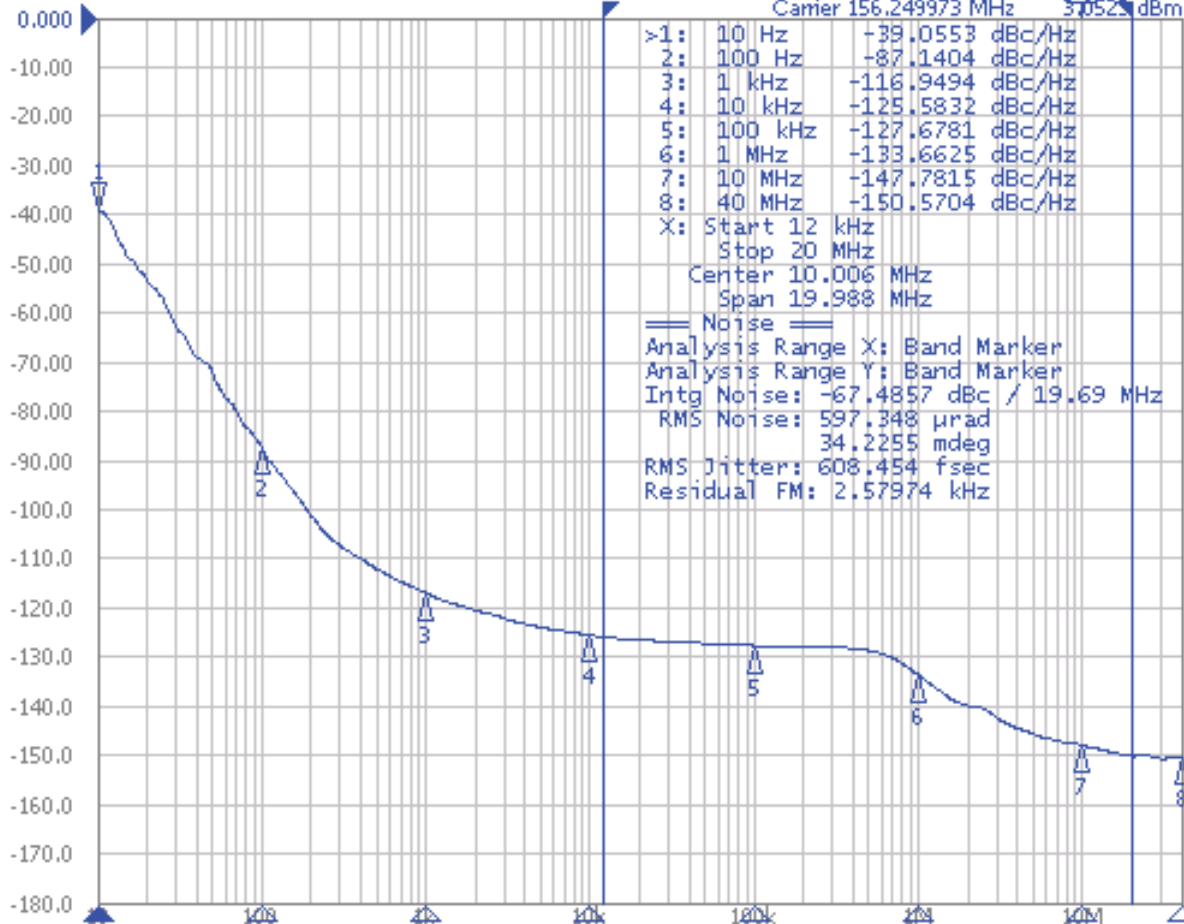
Agilent E5052A Signal Source Analyzer

Phase Noise 10.00dB/ Ref 0.000dBc/Hz [Smo]

Carrier 156.249973 MHz 37.052 dBm

>1:	10 Hz	+39.0553 dBc/Hz
2:	100 Hz	+87.1404 dBc/Hz
3:	1 kHz	-116.9494 dBc/Hz
4:	10 kHz	-125.5832 dBc/Hz
5:	100 kHz	-127.6781 dBc/Hz
6:	1 MHz	-133.6625 dBc/Hz
7:	10 MHz	-147.7815 dBc/Hz
8:	40 MHz	-150.5704 dBc/Hz

X: Start 12 kHz
Stop 20 MHz
Center 10.006 MHz
Span 19.988 MHz
Noise
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -67.4857 dBc / 19.69 MHz
RMS Noise: 597.348 µrad
34.2255 mdeg
RMS Jitter: 608.454 fsec
Residual FM: 2.57974 kHz



IF Gain 20dB Freq Band [99M-1.5GHz] Omit LO Opt [<150kHz] 853pts

Phase Noise Start 10 Hz Stop 40 MHz 8/8

Phase Noise: Hold Cor Ctrl 1.65V Pow 3.3V Attn 0dB ExtRef Stop Svc 2012-12-20 11:04

Save/Recall

Save State

Recall State

Recall by

File Name

Save

Data Trace ...

Save

Memory Trace ...

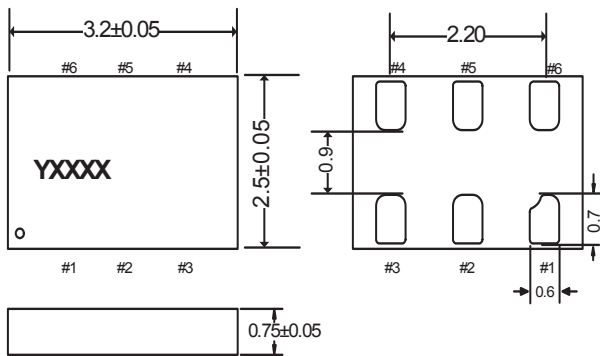
Explorer

Return

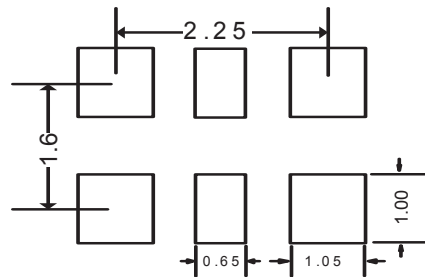
Outline Drawing / Packaging

Package Outline & Dimensions (Unit: mm)

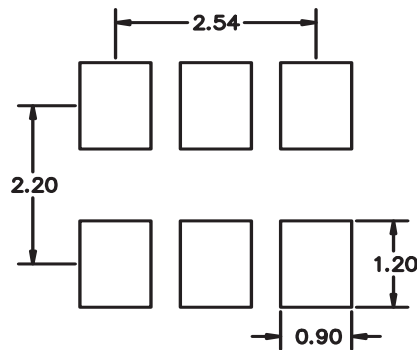
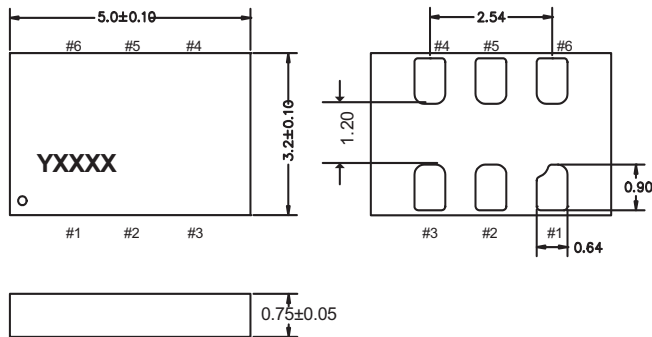
3.2 x 2.5 x 0.75 mm



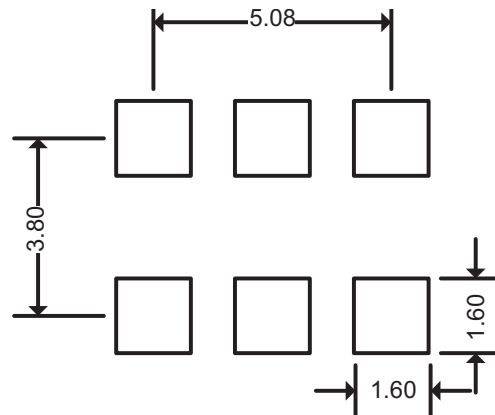
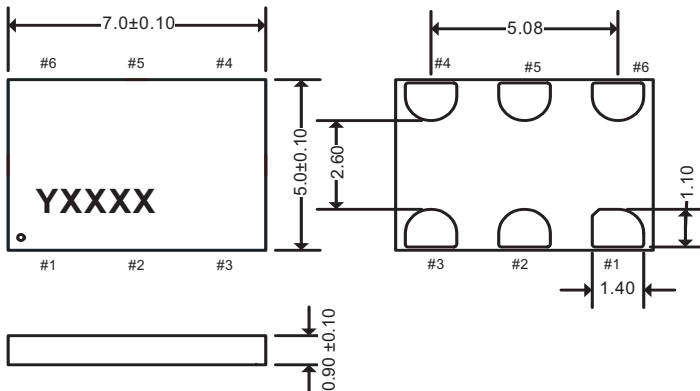
Recommended Land Pattern (Unit: mm)



5.0 x 3.2 x 0.75 mm



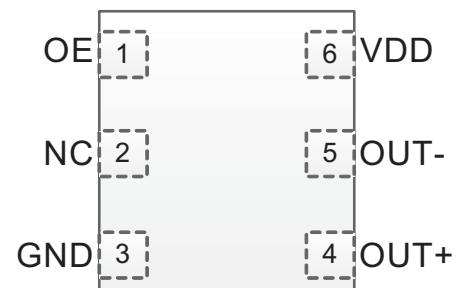
7.0 x 5.0 x 0.90 mm



Pin Connections

Pin	Symbol		Functionality
1	OE	Input	H or Open: specified frequency output L: output is high impedance
2	NC	NA	Do Not Connect; Leave it floating
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage

Top View



Termination Circuit Examples

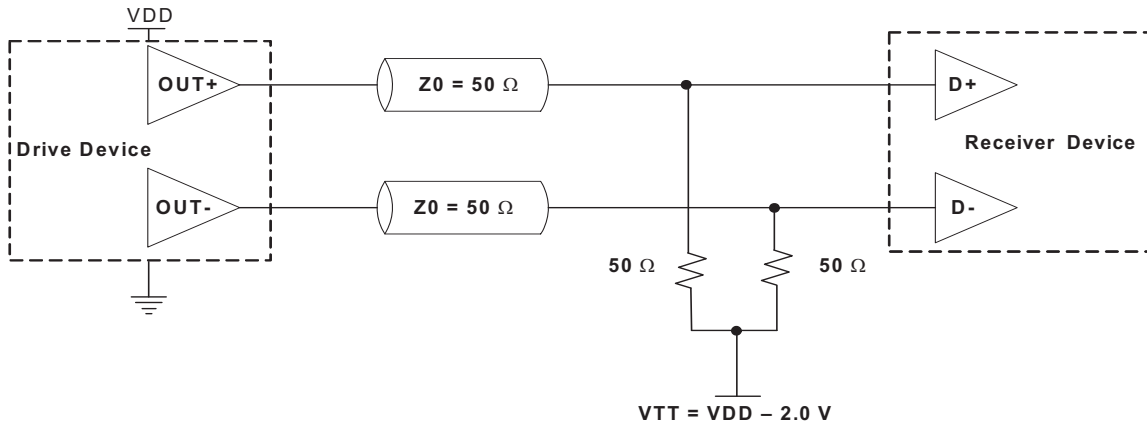


Figure 1. LVPECL Typical Termination

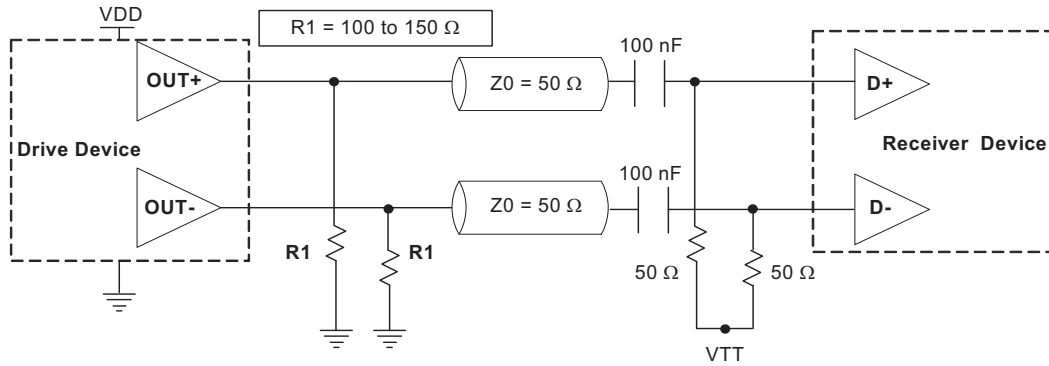


Figure 2. LVPECL AC Coupled Termination

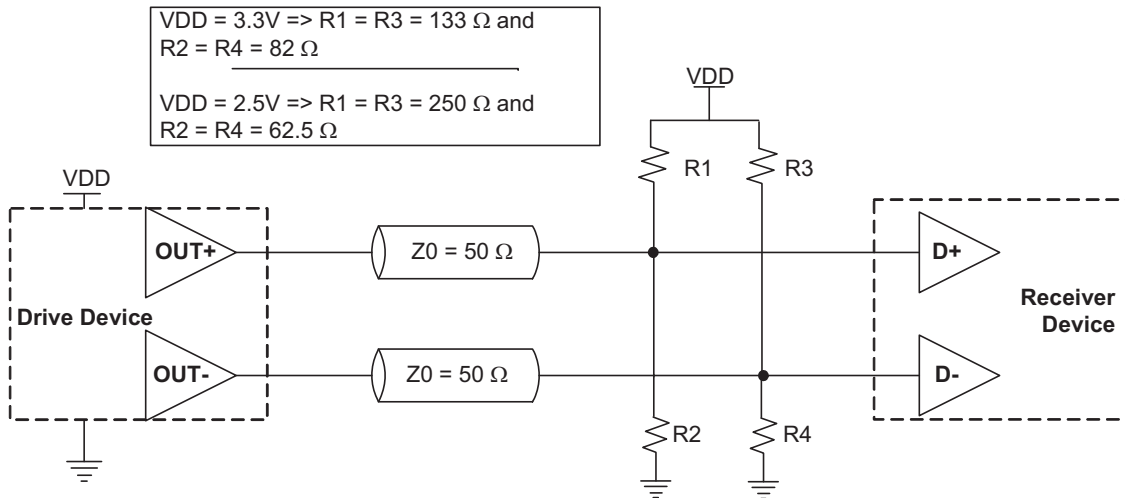


Figure 3. LVPECL with Thevenin Typical Termination

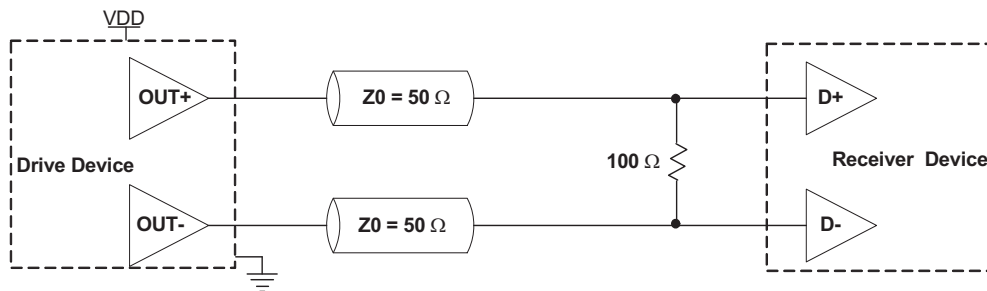


Figure 4. LVDS Single Termination (Load Terminated)

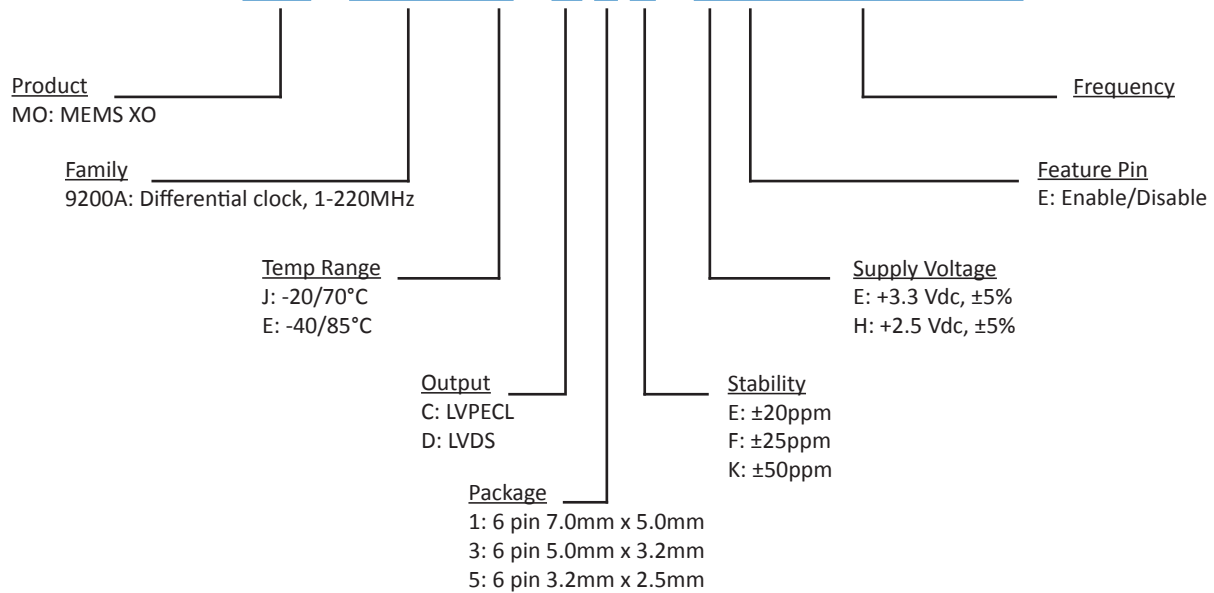
Absolute Maximum Ratings and Test Compliance

Maximum Ratings			
Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Environmental Compliance	
Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Ordering Information

MO - 9200A E - C 3 F - E E 125M000000



Notes:

1. Contact factory for improved stabilities or additional product options. Not all options and codes are available at all frequencies.
2. Unless otherwise stated all values are valid after warm-up time and refer to typical conditions for supply voltage, frequency control voltage, load, temperature (25°C).
3. Subject to technical modification.
4. Contact factory for availability.

Revision History

Revision	Change Summary	Date
1.0	Product Release	June 2013
1.1	Knowles logo and address change	Feb 2014
1.2	Add ± 20 ppm temperature stability	Aug 2014

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