MP4558

1A, 2MHz, 55V Step-Down Converter

The Future of Analog IC Technology®

DESCRIPTION

The MP4558 is a high-frequency, step-down switching regulator with an integrated internal high-side high-voltage power MOSFET. It provides up to a 1A output with current-mode control for fast loop response and easy compensation.

The wide 3.8V-to-55V input range accommodates a variety of step-down applications, including automotive input. A 12µA shutdown-mode supply current makes it suitable for battery-powered applications.

A scaled-down switching frequency in light-load conditions provides high power-conversion efficiency over a wide load range while reducing switching and gate driver losses.

The frequency fold-back prevents inductor current runaway during startup and thermal shutdown provides reliable, fault-tolerant operation.

By switching at 2MHz, the MP4558 can prevent EMI (electromagnetic interference) noise problems, such as those found in AM radio and ADSL applications.

The MP4558 is available in an SOIC8E and a 10-pin 3mm x 3mm QFN package.

FEATURES

- Wide 3.8V-to-55V Operating Input Range
- 250mΩ Internal Power MOSFET
- Up to 2MHz Programmable Switching Frequency
- 140µA Quiescent Current
- Stable with Ceramic Capacitors
- Internal Soft-Start
- Up to 95% Efficiency
- Output Adjustable from 0.8V to 52V
- Available in SOIC8E and 3mm x 3mm QFN10 Packages

APPLICATIONS

- High-Voltage Power Conversion
- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery Powered Systems

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Products, Quality Assurance page.

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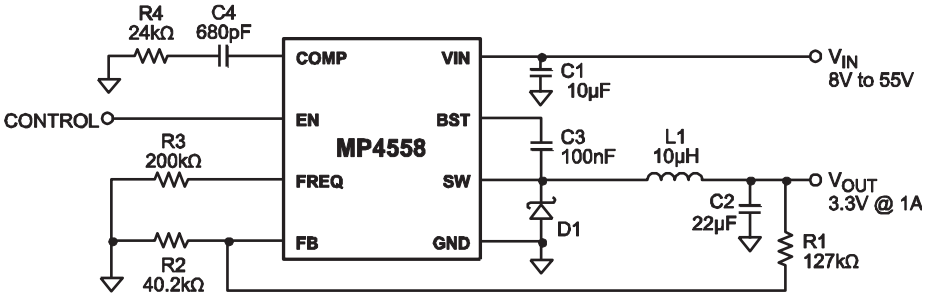
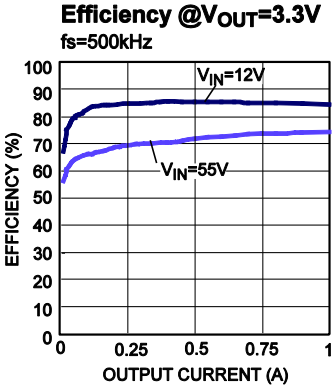
TYPICAL APPLICATION





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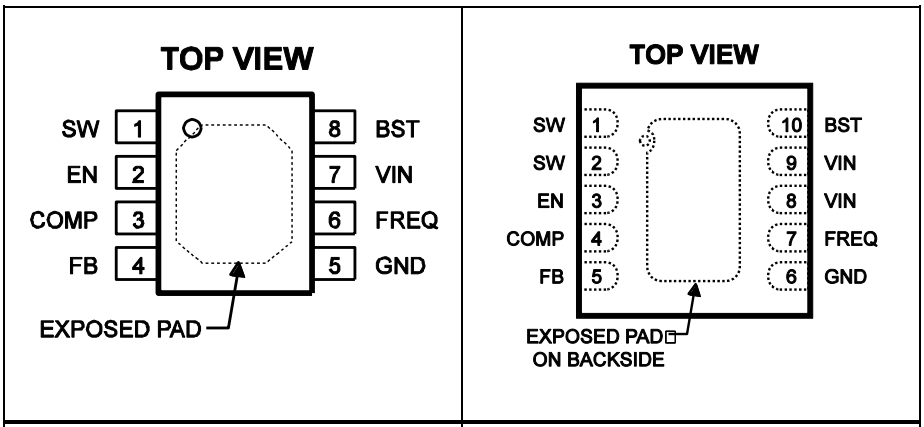
ORDERING INFORMATION

Part Number	Package	Top Marking
MP4558DN*	SOIC8E	MP4558DN LLLLLLLL MPSYWW
MP4558DQ**	QFN10 (3 x 3mm)	ABPY LLL

* For Tape & Reel, add suffix –Z (e.g. MP4558DN–Z)
For RoHS Compliant Packaging, add suffix –LF, (e.g. MP4558DN–LF–Z)
** For Tape & Reel, add suffix –Z (e.g. MP4558DQ–Z)
For RoHS Compliant Packaging, add suffix –LF, (e.g. MP4558DQ–LF–Z)

PACKAGE REFERENCE



SOIC8 (Exposed Pad)	QFN10(3mm x 3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN})..... –0.3V to +60V
Switch Voltage (V_{SW})..... –0.5V to (V_{IN} + 0.5V)
BST to SW..... –0.3V to +5V
All Other Pins..... –0.3V to +5V
Continuous Power Dissipation (T_J = +25°C)(2)
SOIC8E……2.5W
QFN10…… 2.5W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 3.8V to 55V
Output Voltage V_{OUT}..... 0.8V to 52V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8 (Exposed Pad) .....50 ..... 10 ...°C/W
QFN10 (3mm x 3mm).....50 ..... 12 ...°C/W

Notes:
1) Exceeding these ratings may damage the device
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2.5V, V_{COMP} = 1.4V, T_J= –40°C to +85°C. Typical Values are at T_J=25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V < V_{IN} < 55V	T_J=25°C	0.780	0.800	0.820	V
				0.772		0.829	
Feedback Leakage Current	I_{FB}				0.1	1.0	µA
Upper Switch On Resistance (5)	$R_{DS(ON)}$	V_{BST} – V_{SW} = 5V	T_J=25°C	175	250	330	mΩ
				160		400	
Upper Switch Leakage	I_{SW}	V_{EN} = 0V, V_{SW} = 0V			1		µA
Current Limit	I_{LIM}	T_J=25°C	Duty cycle ≤60%	1.3	1.9	3.5	A
				1.1		3.7	
COMP to Current Sense Transconductance	G_{CS}				5.7		A/V
Error Amp Voltage Gain					400		V/V
Error Amp Transconductance		I_{COMP} = ±3µA			120		µA/V
Error Amp Min Source current		V_{FB} = 0.7V			10		µA
Error Amp Min Sink current		V_{FB} = 0.9V			-10		µA
VIN UVLO Threshold		T_J=25°C		2.7	3.0	3.3	V
				2.4		3.6	
VIN UVLO Hysteresis					0.35		V
Soft-Start Time (5)		0V < V_{FB} < 0.8V			0.5		ms
Oscillator Frequency	f_{SW}	R_{FREQ} = 95kΩ	T_J=25°C	0.8	1	1.2	MHz
				0.7		1.3	
Shutdown Supply Current	I_S	V_{EN} < 0.3V			12	20	µA
Quiescent Supply Current	I_Q	No load, V_{FB} = 0.9V (no switching)			140	200	µA
Thermal Shutdown		Hysteresis = 20°C			150		°C
Minimum Off Time	t_{OFF}				100		ns
Minimum On Time (5)	t_{ON}				100		ns
EN Rising Threshold		T_J=25°C		1.4	1.55	1.7	V
				1.3		1.8	
EN Threshold Hysteresis					320		mV

Notes:

5) Derived from bench characterization. Not tested in production..

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PIN FUNCTIONS

SOIC8 Pin #	QFN10 Pin#	Name	Description
1	1, 2	SW	Switch Node. Output of the high-side switch. Requires a low V_F Schottky rectifier to ground. Place the rectifier close to the SW pins to reduce switching spikes.
2	3	EN	Enable Input. Pull this pin below the specified threshold to shut the chip down. Pull it above the specified threshold or leaving it floating to enable the chip.
3	4	COMP	Compensation. GM error amplifier output. Apply control-loop frequency compensation to this pin.
4	5	FB	Feedback. Input to the error amplifier. Connect an external resistive divider between the output and GND: Compare to the internal +0.8V reference to set the regulation voltage.
5	6	GND, Exposed pad	Ground. Connect as close as possible to the output capacitor and avoid high-current switching paths. Connect the exposed pad to GND plane for optimal thermal performance.
6	7	FREQ	Switching Frequency Program Input. Connect a resistor from this pin to ground to set the switching frequency.
7	8, 9	VIN	Input Supply. Supplies power to all the internal control circuitry, both BS regulators, and the high-side switch. Place a decoupling capacitor to ground close to this pin to minimize switching spikes.
8	10	BST	Bootstrap. Positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and the SW pin.

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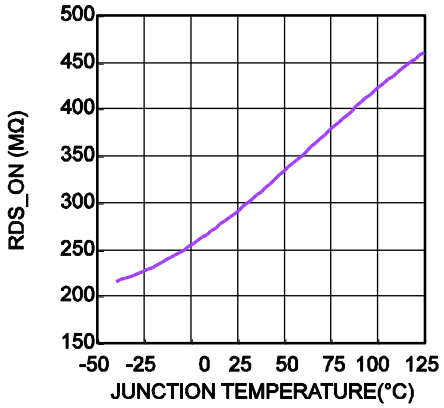
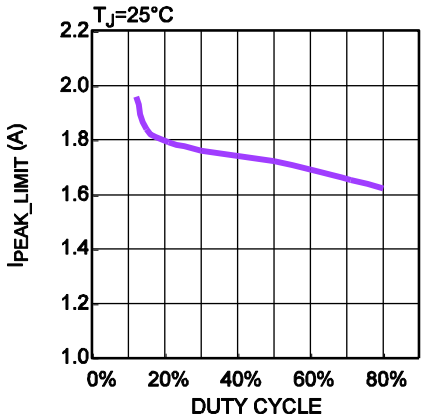
TYPICAL CHARACTERISTICS

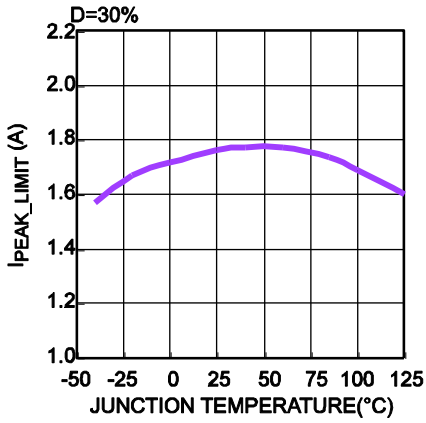
On Resistance vs. Junction Temperature



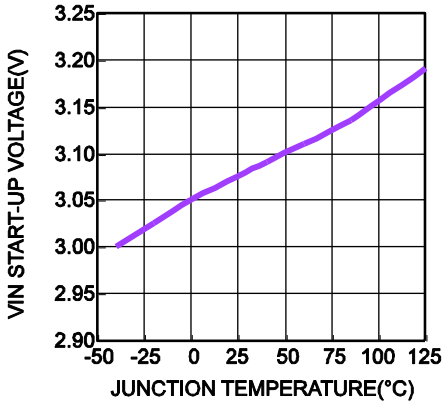
Current Limit vs. Duty Cycle



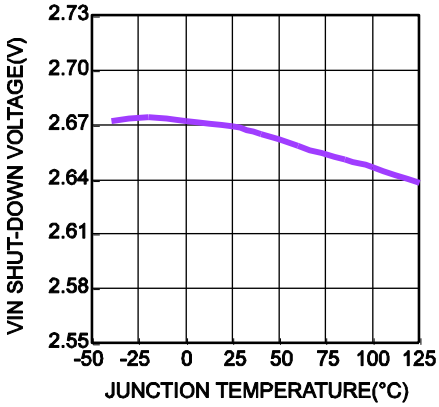
Current Limit vs. Junction Temperature



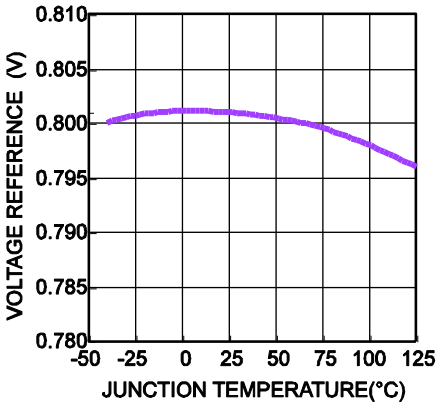
Vin Start-up vs. Junction Temperature



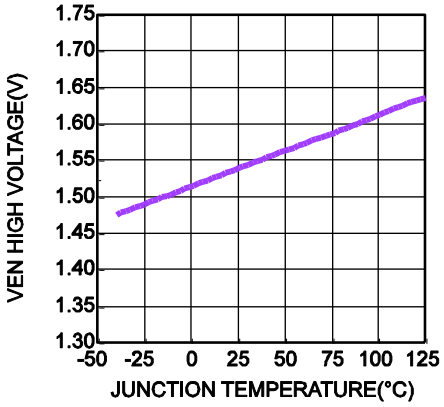
Vin Shut-down vs. Junction Temperature



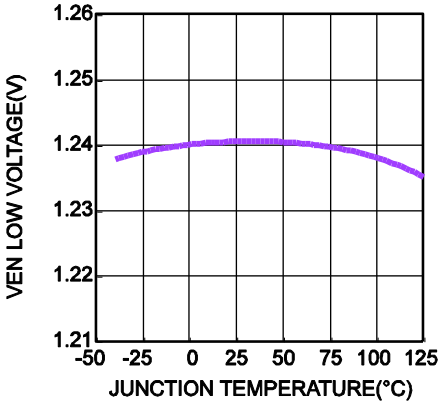
Voltage Reference vs. Junction Temperature



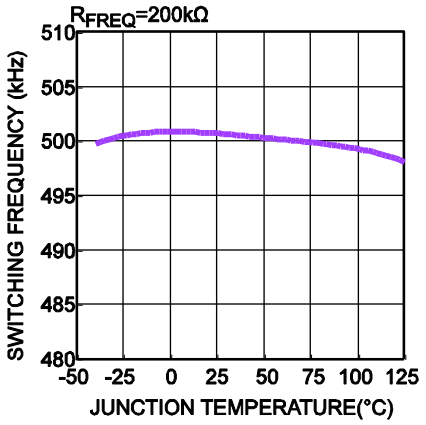
Venable-high vs. Junction Temperature



Venable-low vs. Junction Temperature



Frequency vs. Junction Temperature



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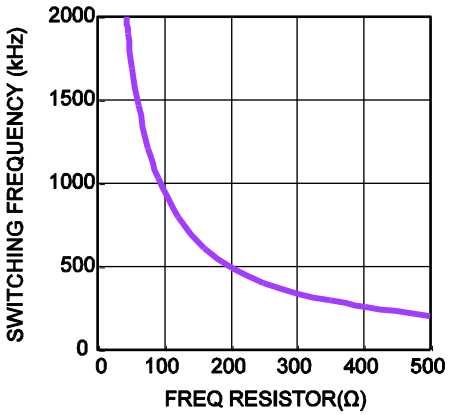
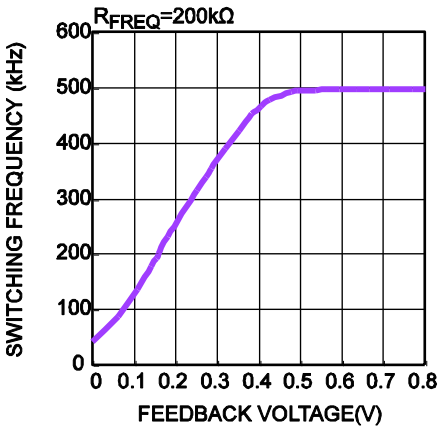
TYPICAL CHARACTERISTICS *(continued)*

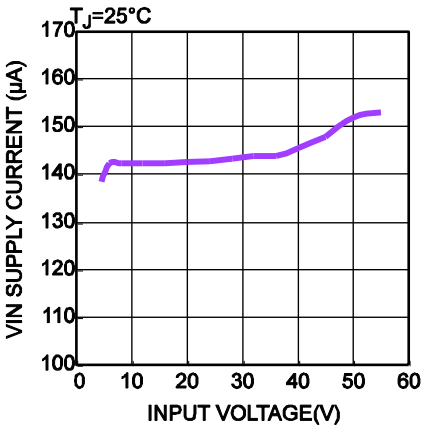
Frequency vs. FREQ Resistor



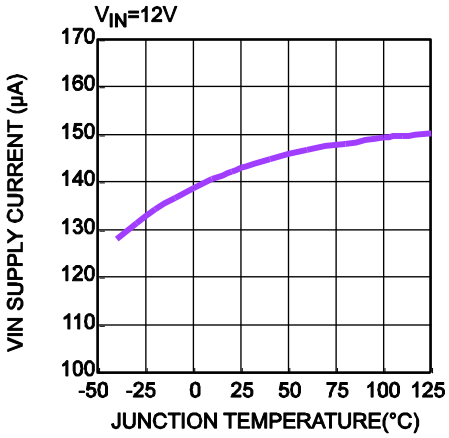
Frequency vs. Feedback Voltage



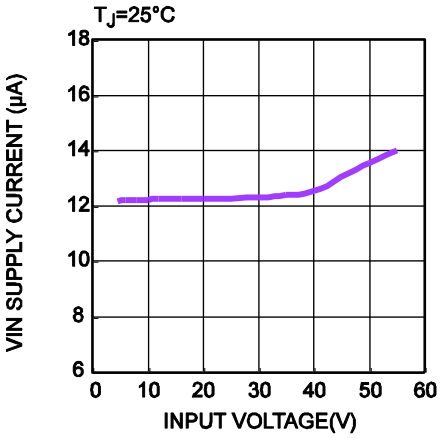
Vin Quiescent Current vs. Input Voltage



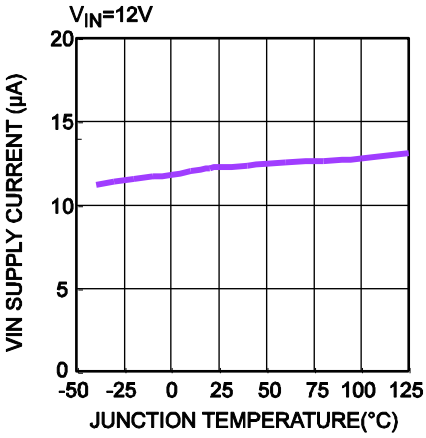
Vin Quiescent Current vs. Junction Temperature



Shutdown Current vs. Input Voltage



Shutdown Current vs. Junction Temperature



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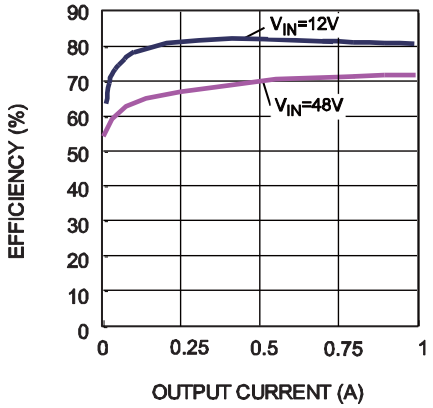
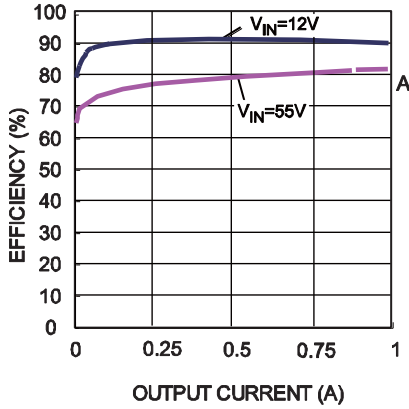
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} =3.3V, C1 = 4.7µF, C2 = 22µF, L1 = 10µH and T_J = 25°C, unless otherwise noted.

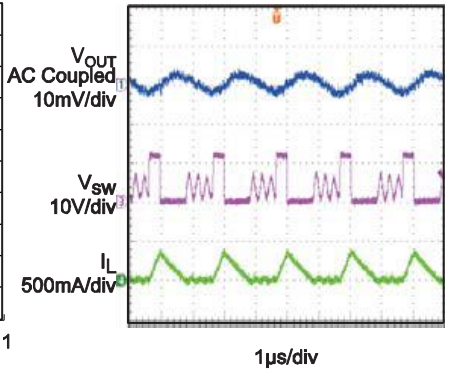
Efficiency @V_{OUT}=2.5V
L1=10µH, fs=500kHz



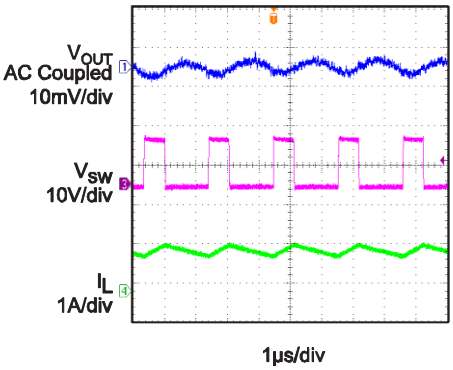
Efficiency @V_{OUT}=5V
L1=15µH, fs=500kHz



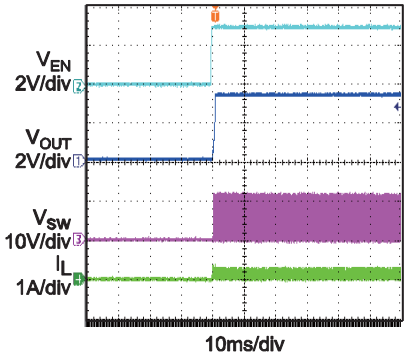
Output Voltage Ripple
I_{OUT}=0.1A



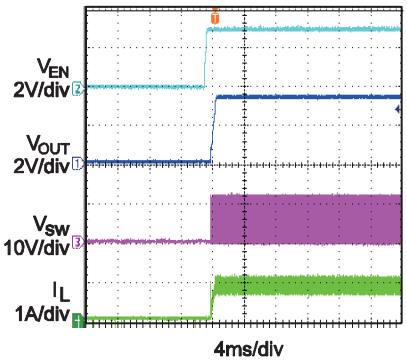
Output Voltage Ripple
I_{OUT}=1A



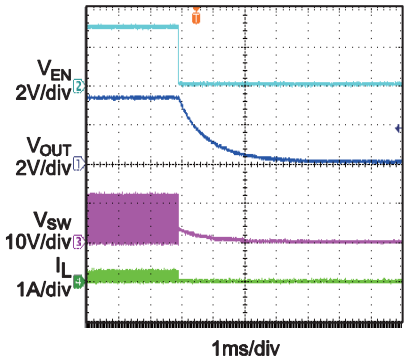
Start up
I_{OUT}=0.1A



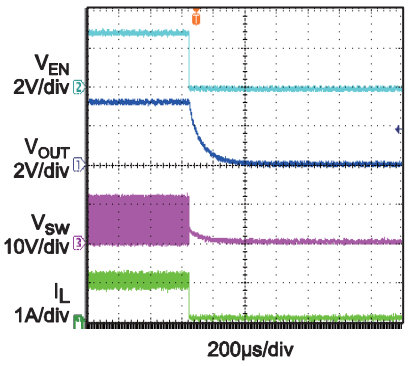
Start up
I_{OUT}=1A



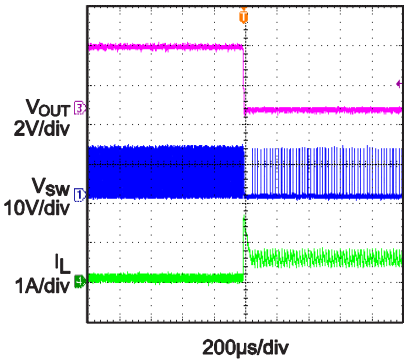
Shut down
I_{OUT}=0.1A



Shut down
I_{OUT}=1A



Short Circuit Entry
I_{OUT}=0.1A to Short



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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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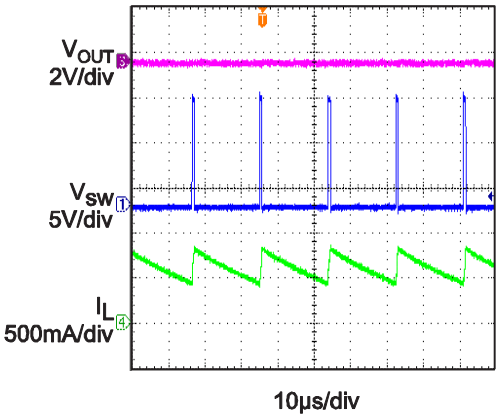
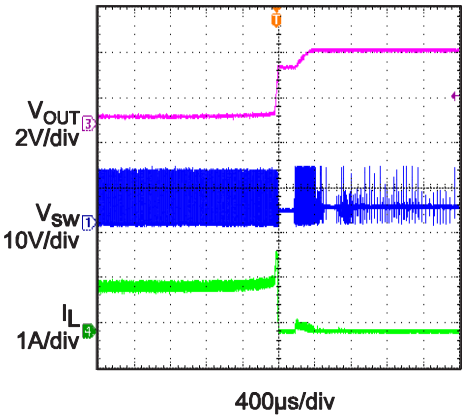
Short Circuit Steady State



Short Circuit Recovery

I_{OUT}=Short to 0A



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BLOCK DIAGRAM

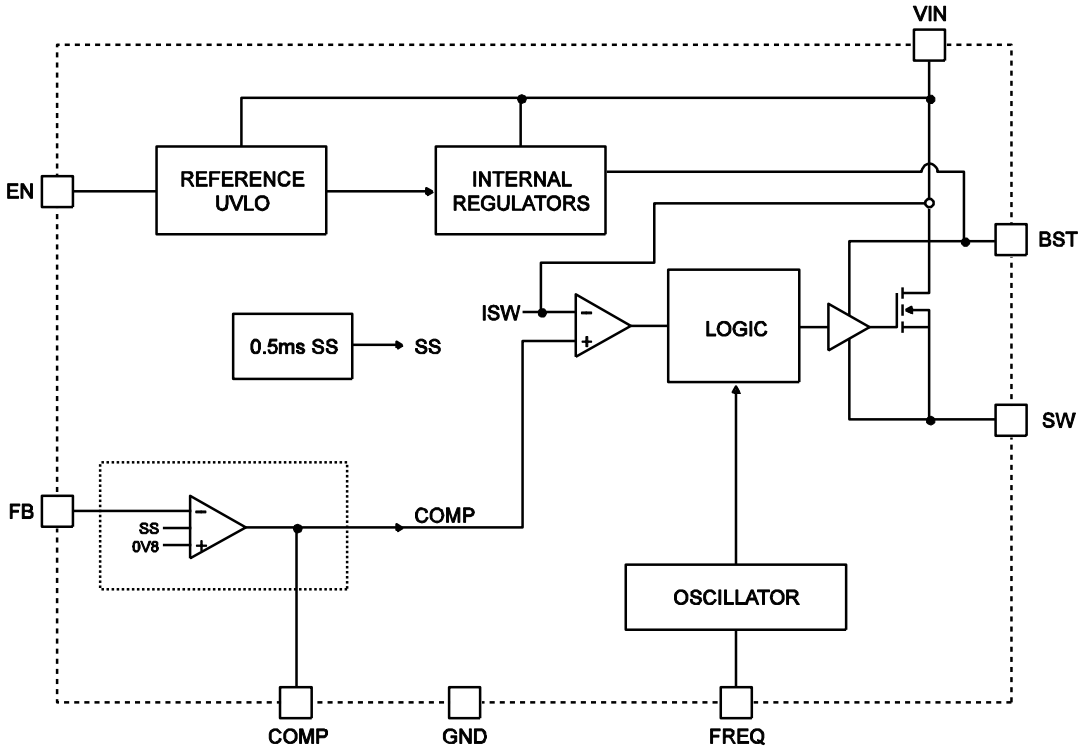

Figure 1: Functional Block Diagram

OPERATION

The MP4558 is a programmable-frequency, non-synchronous, step-down, switching regulator with an integrated high-side, high-voltage power MOSFET. It provides a single, highly efficient solution with current-mode control for fast loop response and easy compensation. It features a wide input voltage range, internal soft-start control, and precision current limiting. Its very low operational quiescent current makes it suitable for battery-powered applications.

PWM Control Mode

At moderate-to-high output current, the MP4558 operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. The internal clock initiates a PWM cycle. The power MOSFET turns on and remains on until its current reaches the value set by the COMP voltage. When the power MOSFET is off, it remains off for at least 100ns before the next cycle starts. If, in one PWM period, the power MOSFET current does not reach the COMP set current value, the power MOSFET remains on to saves on a turn-off operation.

Pulse-Skipping Mode

Under light-load condition, the switching frequency drops to zero to reduce switching and driving losses.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal reference (REF) and outputs a current proportional to the difference between the two. This output current then charges the external compensation network to form the COMP voltage, which controls the power MOSFET current.

While in operation, the minimum COMP voltage is clamped to 0.9V and its maximum is clamped to 2.0V. COMP is internally pulled down to GND in shutdown mode. Avoid pulling COMP up beyond 2.6V.

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Internal Regulator

The 2.6V internal regulator powers most of the internal circuits. This regulator takes the VIN input and operates in the full VIN range. When V_{IN} exceeds 3.0V, the output of the regulator is in full regulation: When V_{IN} is less than 3.0V, the output drops to 0V.

Enable Control

The MP4558 has a dedicated enable control pin (EN): An input voltage that exceeds an upper threshold enables the chip, while a voltage the drops below a lower threshold disables the chip. Its falling threshold is precisely 1.2V, and its rising threshold is 300mV higher, or 1.5V.

When floating, EN is pulled up to about 3.0V by an internal 1µA current source to enable the chip. Pulling it down requires a 1µA current.

When EN drops below 1.2V, the chip enters the lowest shutdown current mode. When EN exceeds 0V but remains below its rising threshold, the chip is still in shutdown mode but with a slightly higher shutdown current.

Under-Voltage Lockout

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO rising threshold is about 3.0V while its falling threshold is a consistent 2.6V.

Internal Soft-Start

Soft-Start prevents the converter output voltage from overshooting during start-up and short-circuit recovery. When the chip starts, the internal circuitry generates a soft-start (SS) voltage that ramps up from 0V to 2.6V. When this voltage is less than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, REF regains control.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds its upper threshold, it shuts down the whole chip. When the temperature falls below its lower threshold, the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. The driver's UVLO is connected to the SS: If the bootstrap voltage hits its UVLO, the soft-start circuit resets. To prevent noise, there is 20µs delay before the reset action. When the device exits the bootstrap UVLO condition, the reset turns off and then soft-start process resumes.

The dedicated internal bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage between the BST and SW nodes falls below regulation, a PMOS pass transistor connected from VIN to BST turns on. The charging current path goes from VIN, to BST and then to SW. The external circuit must provide enough voltage headroom to facilitate charging.

As long as V_{IN} is sufficiently higher than SW, the bootstrap capacitor will charge. When the power MOSFET is ON, V_{IN} is about equal to SW so the bootstrap capacitor cannot charge. When the external diode is on, the difference between VIN and SW is at its largest, thus making it the best period to charge. When there is no current in the inductor, SW equals the output voltage V_{OUT} so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

Under higher duty-cycle operation conditions, the time period available for bootstrap charging is smaller so the bootstrap capacitor may not sufficiently charge.

In case the internal circuit does not have sufficient voltage and the bootstrap capacitor is not charged, extra external circuitry can ensure the bootstrap voltage is in the normal operational region. Refer to the *External Bootstrap Diode* in Application section.

The DC quiescent current of the floating driver is about 20µA. Make sure the bleeding current at the SW node is higher than this value, such that:

$$I_O + \frac{V_O}{(R1+R2)} > 20\mu A$$

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Current Comparator and Current Limit

A current-sense MOSFET accurately senses the current in the power MOSFET. This signal is then fed to the high speed current comparator for current-mode–control purposes, which uses it as one of its inputs with the COMP voltage. When the power MOSFET turns on, the comparator is first blanked until the end of the turn-on transition to avoid noise issues. When the sensed current exceeds the COMP voltage, the comparator output is low and the power MOSFET turns off. The cycle-by-cycle maximum current of the internal power MOSFET is internally limited.

Short-Circuit Protection

When the output is shorted to the ground, the switching frequency folds back and the current limit falls to reduce the short circuit current. When the FB voltage equals 0V, the current limit falls to about 50% of its full current limit. The FB voltage reaches its 100% of its current limit when it exceeds 0.4V

When the short-circuit FB voltage is low, the SS drops by V_{FB} and SS ≈ V_{FB} + 100mV. If the short circuit is removed, the output voltage recovers at the SS rate. When FB is high enough, the frequency and current limit return to normal values.

Startup and Shutdown

If both V_{IN} and V_{EN} exceed their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer blanks the power MOSFET OFF for about 50µs to avoid start-up glitches. When the internal soft-start block is enabled, it first holds its SS output low to ensure the other circuits are ready and then slowly ramps up.

Three events can shut down the chip: EN low, V_{IN} low and thermal shutdown. In shutdown, the power MOSFET turns off first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down.

Programmable Oscillator

An external resistor—R_{FREQ} connected from the FREQ pin to GND—sets the MP4558 oscillating frequency. Calculate the value of R_{FREQ} from:

$$R_{FREQ}(k\Omega) = \frac{100000}{f_S(kHz)} - 5$$

For f_{SW}=500kHz, R_{FREQ}=195kΩ.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

Set the output voltage with a resistor divider between the output voltage and the FB pin. The voltage divider drops the output voltage down to the feedback voltage by the ratio:

$$V_{FB}=V_{OUT}\times\frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2}$$

For example, for R2 = 10kΩ, R1 can be determined by:

$$R1=12.5\times(V_{OUT}-0.8)(k\Omega)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 31.6kΩ.

Inductor

The inductor supplies constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will lower the output ripple voltage. However, a larger-valued inductor is physically larger, has a higher series resistance, or lower saturation current.

Generally, determine an appropriate inductance value by selecting the peak-to-peak inductor ripple current equal to approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. Calculate the inductance value with:

$$L1=\frac{V_{OUT}}{f_s\times\Delta I_L}\times(1-\frac{V_{OUT}}{V_{IN}})$$

Where:

- V_{OUT} is the output voltage,
- V_{IN} is the input voltage,
- f_S is the switching frequency, and
- ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. Calculate the peak inductor current with:

$$I_{LP}=I_{LOAD}+\frac{V_{OUT}}{2\times f_S\times L1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Table 1 lists a number of suitable inductors from various manufacturers. The choice the inductor style mainly depends on the price vs. size requirements and any EMI requirement.

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Table 1: Inductor Selection Guide

Part Number	Inductance (μH)	Max DCR (Ω)	Current Rating (A)	Dimensions L x W x H (mm)
Wurth Electronics				
7447789004	4.7	0.033	2.9	7.3x7.3x3.2
744066100	10	0.035	3.6	10x10x3.8
744771115	15	0.025	3.75	12x12x6
744771122	22	0.031	3.37	12x12x6
TDK				
RLF7030T-4R7	4.7	0.031	3.4	7.3x6.8x3.2
SLF10145T-100	10	0.0364	3	10.1x10.1x4.5
SLF12565T-150M4R2	15	0.0237	4.2	12.5x12.5x6.5
SLF12565T-220M3R5	22	0.0316	3.5	12.5x12.5x6.5
Toko				
FDV0630-4R7M	4.7	0.049	3.3	7.7x7x3
919AS-100M	10	0.0265	4.3	10.3x10.3x4.5
919AS-160M	16	0.0492	3.3	10.3x10.3x4.5
919AS-220M	22	0.0776	3	10.3x10.3x4.5

Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the forward diode voltage and recovery times, use a Schottky diode.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current. Table 2 lists example Schottky diodes and manufacturers.

Table 2: Diode Selection Guide

Diodes	Voltage/ Current Rating	Manufacturer
B290-13-F	90V, 2A	Diodes Inc.
B380-13-F	80V, 3A	Diodes Inc.
CMSH2-100M	100V, 2A	Central Semi
CMSH3-100MA	100V, 3A	Central Semi

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Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use capacitors with low equivalent series resistance (ESR) for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor (C1) can be electrolytic, tantalum or ceramic.

When using electrolytic or tantalum capacitors, include a small, high-quality ceramic capacitor—i.e. 0.1μF—placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors for best results. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP4558 can be optimized for a wide range of capacitances and ESR values.

Compensation Components

MP4558 employs current-mode control for easy compensation and fast transient response. The COMP pin controls the system stability and transient response—the COMP pin is the output of the internal error amplifier. A capacitor-resistor combination in series sets a pole-zero combination to control the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where

- A_{VEA} is the error amplifier voltage gain, 400V/V,
- G_{CS} is the current sense transconductance,5.6A/V, and
- R_{LOAD} is the load resistor value.

The system has two poles of importance: One is caused by the compensation capacitor (C3) and the output resistor of error amplifier; the other is caused by the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where, G_{EA} is the error amplifier transconductance, 120μA/V.

The system has one zero of importance from C3 and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

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The system may have another important zero if the output capacitor has a large capacitance or a high ESR value. The zero, due to the ESR and the output capacitor value, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C5) and R3 compensates for the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C5 \times R3}$$

The compensation network shapes the converter transfer function for a desired loop gain. The feedback-loop unity gain at the system crossover frequency is important: Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies can destabilize the system. Generally, set the crossover frequency to approximately 1/10 of the switching frequency.

Table 3: Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT} (V)	L (μH)	C2 (μF)	R3 (kΩ)	C3 (pF)	C6 (pF)
1.8	4.7	33	32.4	680	None
2.5	4.7 - 6.8	22	26.1	680	None
3.3	6.8 -10	22	68.1	220	None
5	15 - 22	33	47.5	330	None
12	10	22	16	470	2

To optimize the compensation components for conditions not listed in Table 3, use the following procedure.

1. Choose R3 to set the desired crossover frequency. Determine the R3 value from the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency.

2. Choose C3 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero—f_{Z1}—below ¼ the crossover frequency to provide sufficient phase margin. Determine C3 from the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

3. Determine if C5 is required—if the ESR zero of the output capacitor is located at less than 1/2 f_S, or if the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add C5 to set the pole f_{P3} at the location of the ESR zero. Determine the C5 value by the equation:

$$C5 = \frac{C2 \times R_{ESR}}{R3}$$

High-Frequency Operation

The MP4558 switching frequency can be programmed up to 2MHz by an external resistor.

The minimum MP4558 ON-time is typically about 100ns. Pulse-skipping operation can be seen more easily at higher switching frequencies due to the minimum ON-time.

Since the internal bootstrap circuitry has higher impedance that may not be adequate to charge the bootstrap capacitor during each $(1\text{-}D)\times t_S$ charging period, add an external bootstrap charging diode if the switching frequency is about 2MHz (see External Bootstrap Diode section for detailed implementation information).

With higher switching frequencies, the inductive reactance (XL) of the capacitor dominates so that the ESL of the input/output capacitor determines the input/output ripple voltage at higher switching frequencies. Because of this ripple, use high-frequency ceramic capacitors for the input decoupling capacitor and output the filtering capacitor for high-frequency operation.

Layout becomes more important when the device switches at higher frequencies. For best results,

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place the input decoupling capacitor and the catch diode as close to the MP4558 (VIN pin, SW pin and PGND) as close as possible with short and wide traces. This can help to greatly reduce the voltage spikes on the SW node, and lower the EMI noise level.

Route the feedback trace as far from the inductor and noisy power traces as possible. If possible, run the feedback trace on the opposite side of the PCB opposite from the inductor with a ground plane separating the two. Placing the compensation components close to the MP4558. Avoid placing the compensation components close to or under the high-dv/dt SW node, or inside the high-di/dt power loop. If this is not possible, route a ground plane to isolate the circuit. Switching loss is expected to increase at high switching frequencies.

To help to improve the thermal conduction, add grid of thermal vias under the exposed pad. use small vias (15mil barrel diameter) so that the plating process fills the holes, thus aiding conduction to the other side. Excessively large holes can cause solder wicking during the reflow soldering process. The typical pitch (distance between the centers) between thermal vias is typically 40mil.

External Bootstrap Diode

An external bootstrap diode may enhance the regulator efficiency. For the cases described below, add an external BST diode from 5V to the BST pin:

- There is a 5V rail available in the system;
- V_{IN} is no greater than 5V;
- V_{OUT} is between 3.3V and 5V;

This diode is also recommended for high-duty–cycle operation (when V_{OUT}/V_{IN} > 65%) applications.

The bootstrap diode can be a low-cost one such as IN4148 or BAT54.

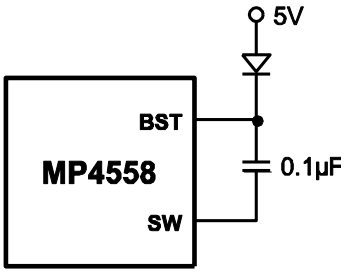

Figure 2: External Bootstrap Diode

At no load or light load, the converter may operate in pulse-skipping mode to maintain the output voltage in regulation: there is less time to refresh the BS voltage. For sufficient gate voltage under such operating conditions, chose V_{IN} – V_{OUT} > 3V. For example, if V_{OUT} = 3.3V, V_{IN} needs to be greater than 3.3V+3V=6.3V for sufficient BST voltage at no load or light load. To meet this requirement, the EN pin can program the input UVLO voltage to V_{OUT}+3V.

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TYPICAL APPLICATION CIRCUITS

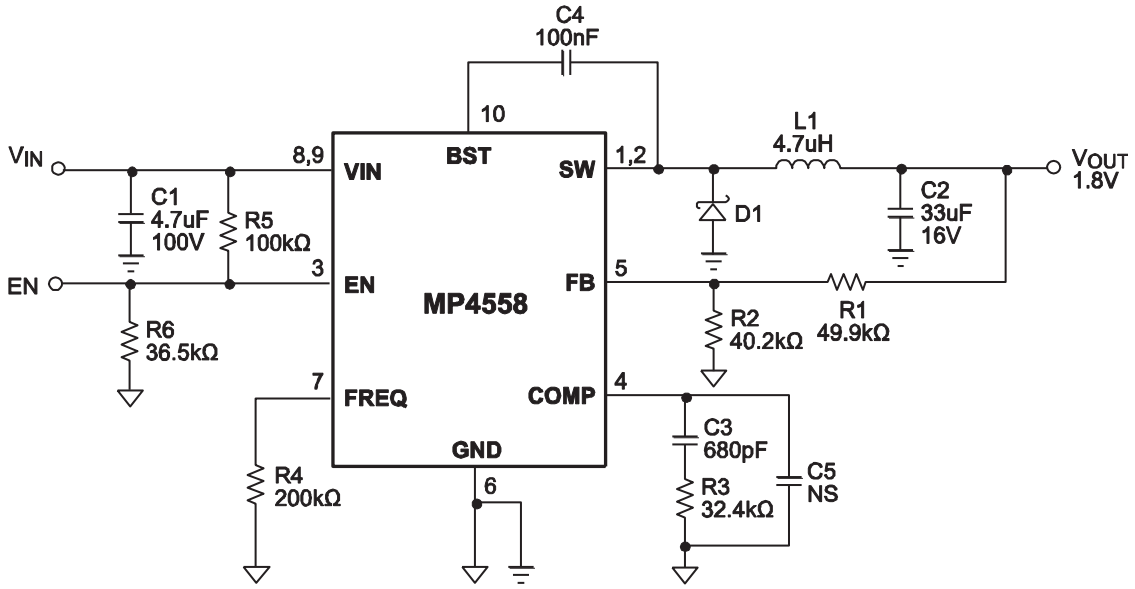

Figure 3—1.8V Output Typical Application Schematic

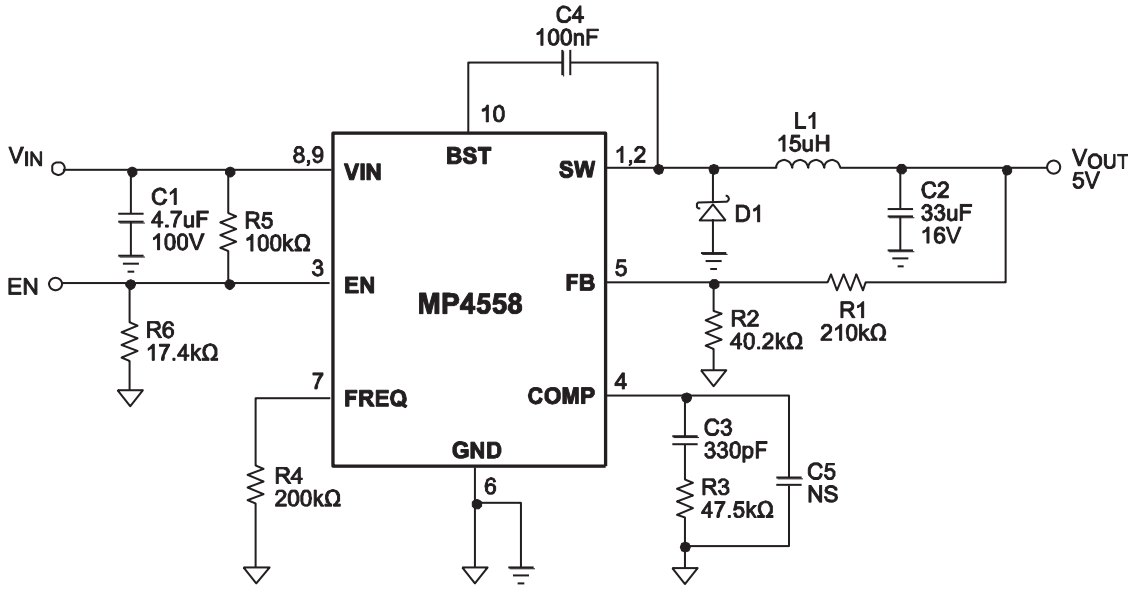

Figure 4—5V Output Typical Application Schematic

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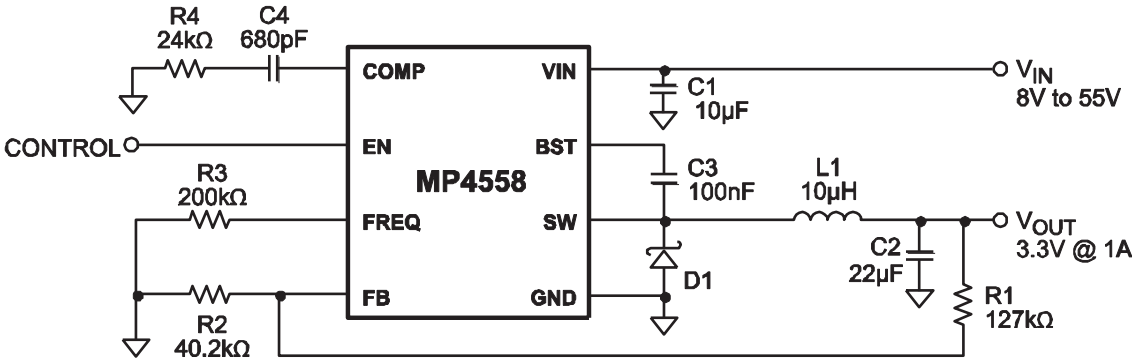
PCB LAYOUT GUIDE

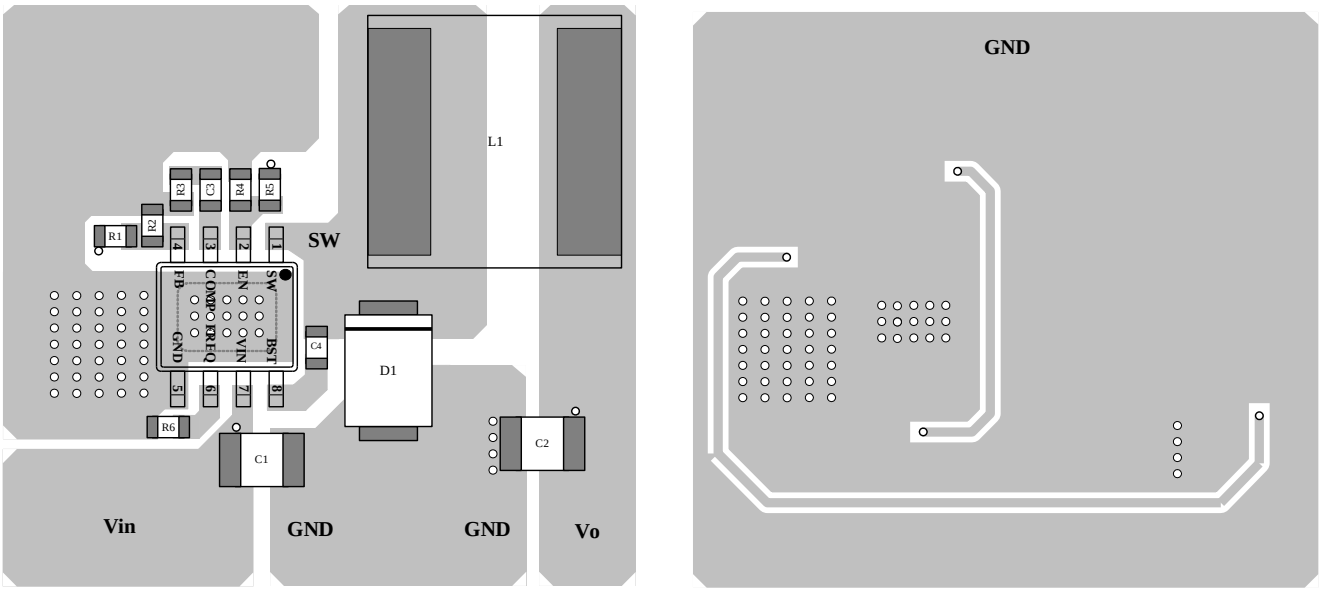
PCB layout is very important to achieve stable operation. Duplicate the EVB layout below for optimal performance.

For changes, please follow these guidelines and use Figure 5 for reference.

1) Keep the switching-current path short and minimize the loop area formed by the input capacitor, high-side MOSFET and external switching diode.
2) Place the bypass ceramic capacitors close to the V_{IN} pin.
3) Use short and direct feedback connections. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route the SW path away from sensitive analog areas such as the FB path.
5) Connect IN, SW, and GND, respectively, to a large copper area to cool the chip to improve thermal performance and long-term reliability.



MP4558 Typical Application Circuit



TOP Layer **Bottom Layer**

MP4558 Layout Guide

Figure 5: MP4558 Typical Application Circuit and PCB Layout Guide

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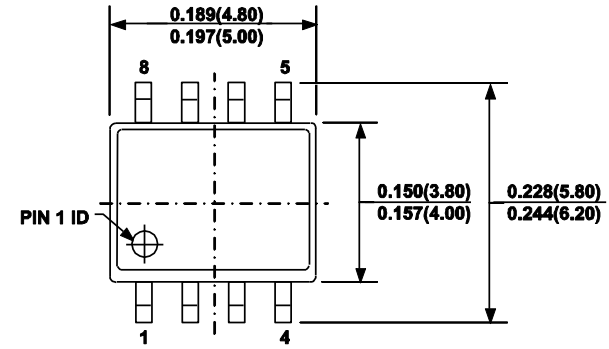
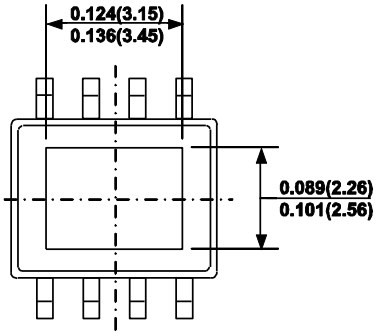
PACKAGE INFORMATION

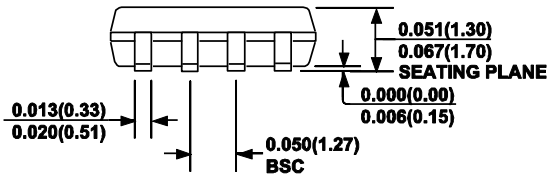
SOIC8 (EXPOSED PAD)



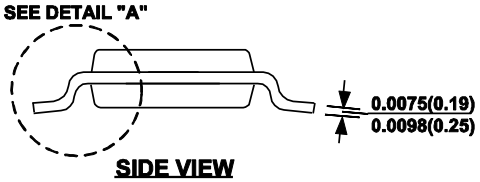
TOP VIEW



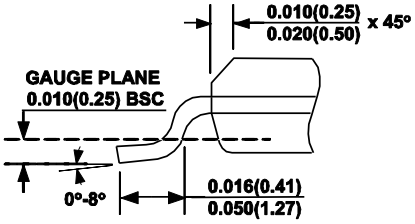
BOTTOM VIEW



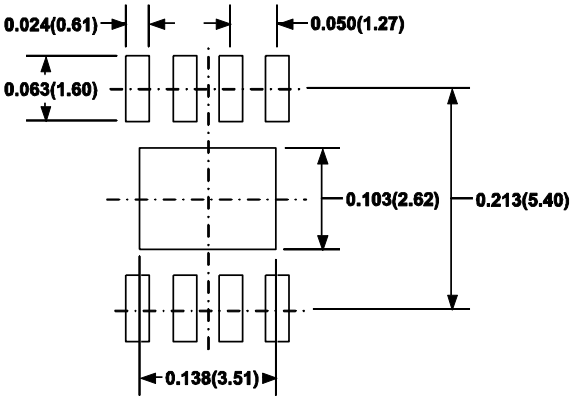
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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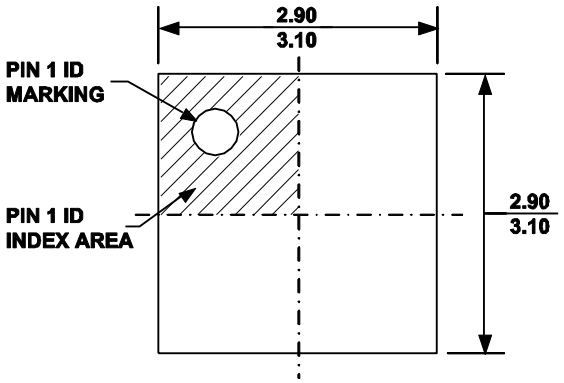
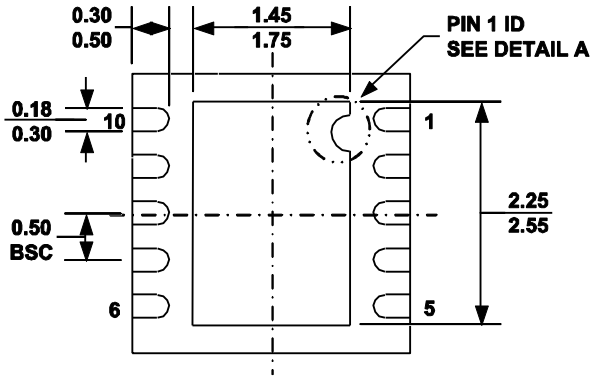
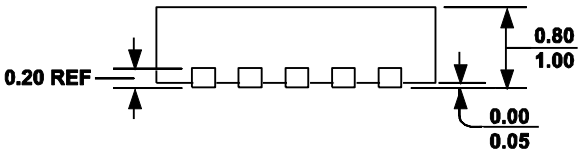
QFN10 (3mm x 3mm)



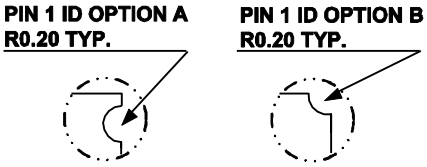
TOP VIEW



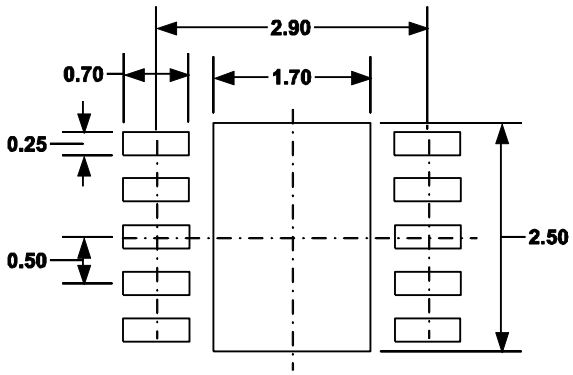
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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