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November 2009



FSA2467 — 0.4Ω Low-Voltage Dual DPDT Analog Switch

FSA2467

0.4Ω Low-Voltage Dual DPDT Analog Switch

Features

- Typical 0.4Ω On Resistance (R_{ON}) for +2.7V supply
- Features Less than 12μA I_{CCT} Current when S_n Input is Lower than V_{CC}
- 0.25Ω Maximum R_{ON} Flatness for +2.7V Supply
- 3 x 3mm 16-Lead Pb-Free MLP Package
- 1.8x2.6mm 16-Lead Pb-Free UMLP Package
- Broad V_{CC} Operating Range
- Low THD (0.02% Typical for 32Ω Load)

Description

The FSA2467 is a dual Double-Pole, Double-Throw (DPDT) analog switch. The FSA2467 operates from a single 1.65V to 4.3V supply. The FSA2467 features an ultra-low on resistance of 0.4Ω at a +2.7V supply and 25°C. This device is fabricated with sub-micron CMOS technology to achieve fast switching speeds and is designed for break-before-make operation.

FSA2467 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature allows mobile handset applications direct interface with baseband processor general-purpose I/Os.

Applications

- Cell Phone
- PDA
- Portable Media Player

Ordering Information

Part Number	Top Mark	Eco Status	Package Description
FSA2467MPX	FSA 2467	Green	16-lead Molded Leadless Package (MLP), JEDEC MO-220, 3 x 3mm Square
FSA2467UMX	GC	Green	16-lead Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6mm

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagram

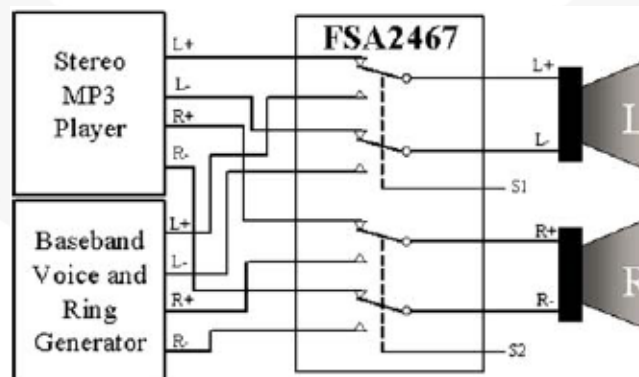


Figure 1. Application Diagram

Pin Assignments

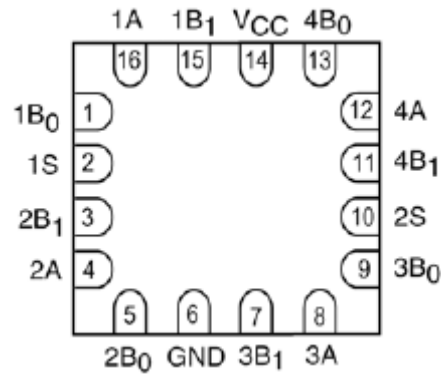


Figure 2. Pin Assignments

Truth Table

Control Inputs	Function
LOW	nB ₀ Connected to nA
HIGH	nB ₁ Connected to nA

Pin Descriptions

Name	Function
nA, nB ₀ , nB ₁	Data Ports
nS	Control Input

Analog Symbol

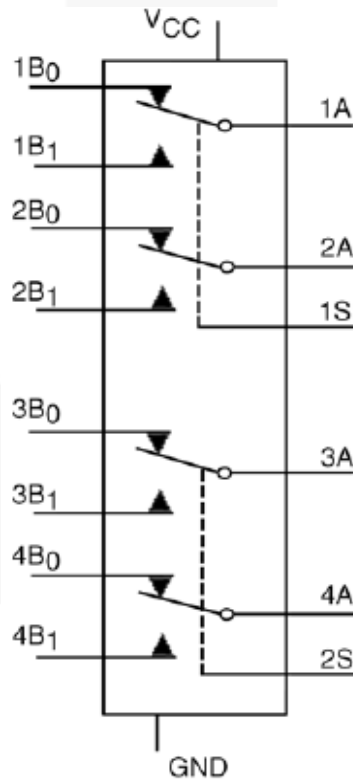


Figure 3. Analog Symbol

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	-0.5	5.0	V
V _S	Switch Voltage	-0.5	V _{CC} +0.3	V
V _{IN}	Input Voltage	-0.5	5.0	V
I _{IK}	Input Diode Current	-50		mA
I _{SW}	Switch Current		350	mA
I _{SWPEAK}	Peak Switch Current (Pulsed at 1ms duration, <10% Duty Cycle)		500	mA
T _{STG}	Storage Temperature Range	-65	+150	°C
T _J	Junction Temperature		+150	°C
T _L	Lead Temperature, Soldering 10 Seconds		+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		5.5 kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	1.65	4.30	V
V _{IN}	Control Input Voltage ⁽¹⁾	0	V _{CC}	V
V _S	Switch Input Voltage	0	V _{CC}	V
T _A	Operating Temperature	-40	+85	°C

Note:

- Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = +25°C			T _A = -40 to +85°C		Units
				Min.	Typ.	Max.	Min	Max.	
V _{IH}	Input Voltage High		4.3				1.4		V
			2.7 to 3.6				1.3		
			2.3 to 2.7				1.1		
			1.65 to 1.95				0.9		
V _{IL}	Input Voltage Low		4.3					0.7	V
			2.7 to 3.6					0.5	
			2.3 to 2.7					0.4	
			1.65 to 1.95					0.4	
I _{IN}	Control Input Leakage	V _{IN} =0V to V _{CC}	1.65 to 4.30				-0.5	0.5	μA
I _{NO(OFF)} I _{NC(OFF)}	Off Leakage Current of Port nB ₀ and nB ₁	nA=0.3V, V _{CC} =0.3V nB ₀ or nB ₁ =0.3V, V _{CC} =0.3V or floating	1.95 to 4.30	-10.0		10.0	-50.0	50.0	nA
I _{A(ON)}	On Leakage Current of Port A	nA=0.3V, V _{CC} =0.3V nB ₀ or nB ₁ =0.3V, V _{CC} =0.3V or floating	1.95 to 4.30	-10.0		10.0	-50.0	50.0	nA
R _{ON}	Switch On Resistance ⁽²⁾	I _{OUT} =100mA	4.3		0.4			0.6	Ω
		nB ₀ or nB ₁ =0V, 0.8V, 1.8V, 2.7V	2.7		0.4			0.6	
		I _{OUT} =100mA, nB ₀ or nB ₁ =0V, 0.7V, 1.2V, 2.3V	2.3	0.55				0.95	
		I _{OUT} =100mA, nB ₀ or nB ₁ =1.0V	1.8	0.8				2.0	
ΔR _{ON}	On Resistance Matching Between Channels ⁽³⁾	I _{OUT} =100mA, nB ₀ or nB ₁ =0.8V	2.7	0.04				0.10	Ω
		I _{OUT} =100mA, nB ₀ or nB ₁ =0.7V	2.3	0.03				0.10	
R _{FLAT(ON)}	On Resistance Flatness ⁽⁴⁾	I _{OUT} =100mA, B ₀ or nB ₁ =0V to V _{CC}	2.7					0.25	Ω
			2.3					0.3	
I _{CC}	Quiescent Supply Current	V _{IN} =0V to V _{CC} I _{OUT} =0V	4.3	-100		100	-500	500	nA
I _{CC(T)}	Increase in I _{CC} Current per Control Voltage	V _{IN} =1.8V	4.3		7.0	12.0		15.0	μA
		V _{IN} =2.6V	4.3		3.0	6.0		7.0	

Notes:

- On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
- Δ R_{ON}=R_{ON max} – R_{ON min} measured at identical V_{CC}, temperature and voltage.
- Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC Electrical Characteristics

Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC}	T _A = +25°C			T _A = -40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t _{ON}	Turn-On Time	nB0 or nB1=1.5V	3.6 to 4.3			50		60	ns	Figure 7
		R _L =50Ω, C _L =35pF	2.7 to 3.6			65		75		
			2.3 to 2.7			80		90		
t _{OFF}	Turn-Off Time	nB0 or nB1=1.5V	3.6 to 4.3			32		40	ns	Figure 7
		R _L =50Ω, C _L =35pF	2.7 to 3.6			42		50		
			2.3 to 2.7			52		60		
t _{BBM}	Break-Before-Make Time	nB0 or nB1=1.5V	3.6 to 4.3		12				ns	Figure 8
		R _L =50Ω, C _L =35pF	2.7 to 3.6		15					
			2.3 to 2.7		20					
Q	Charge Injection	C _L =100pF, V _{GEN} =0V, R _{GEN} =0Ω	3.6 to 4.3		15				pC	Figure 10
		C _L =100pF, V _{GEN} =0V, R _{GEN} =0Ω	2.7 to 3.6		10					
		C _L =100pF, V _{GEN} =0V, R _{GEN} =0Ω	2.3 to 2.7		8					
OIRR	Off Isolation	f=100KHZ, R _L =50Ω, C _L =5pF	3.6 to 4.3		-75				dB	Figure 9
			2.7 to 3.6		-75					
			2.3 to 2.7		-75					
Xtalk	Crosstalk	f=100KHZ, R _L =50Ω, C _L =5pF	3.6 to 4.3		-75				dB	Figure 9
			2.7 to 3.6		-75					
			2.3 to 2.7		-75					
BW	-3dB Bandwidth	R _L =50Ω	2.3 to 4.3		85				MHZ	Figure 12
THD	Total Harmonic Distortion	R _L =32Ω, V _{IN} =2V _{PP} , f=20 to 20kHz	3.6 to 4.3		0.02				%	Figure 13
		R _L =32Ω, V _{IN} =2V _{PP} , f=20 to 20kHz	2.7 to 3.6		0.02					
		R _L =32Ω, V _{IN} =2V _{PP} , f=20 to 20kHz	2.3. to 2.7		0.02					

Capacitance

Symbol	Parameter	Conditions	V _{CC}	T _A = +25°C Typical	Units	Figure
C _{IN}	Control Pin Input Capacitance	f=1MHZ	0	1.5	pF	Figure 7
C _{OFF}	B Port Off Capacitance	f=1MHZ	3.3	32	pF	Figure 7
C _{ON}	A Port On Capacitance	f=1MHZ	3.3	118	pF	Figure 7

Typical Applications

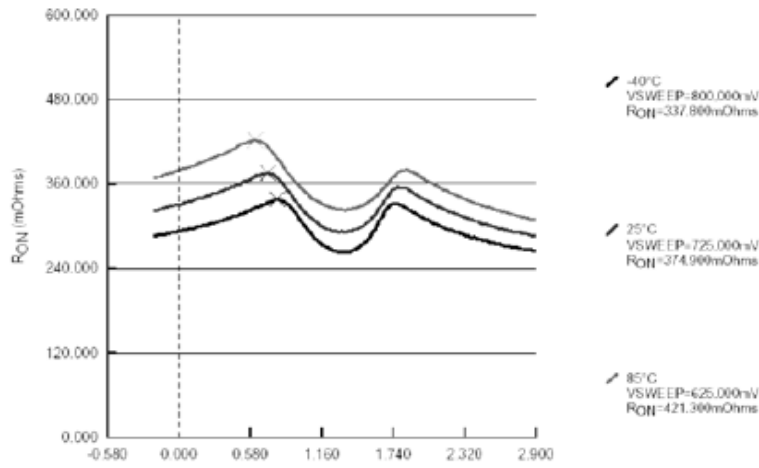


Figure 4. RON at 2.7V VCC

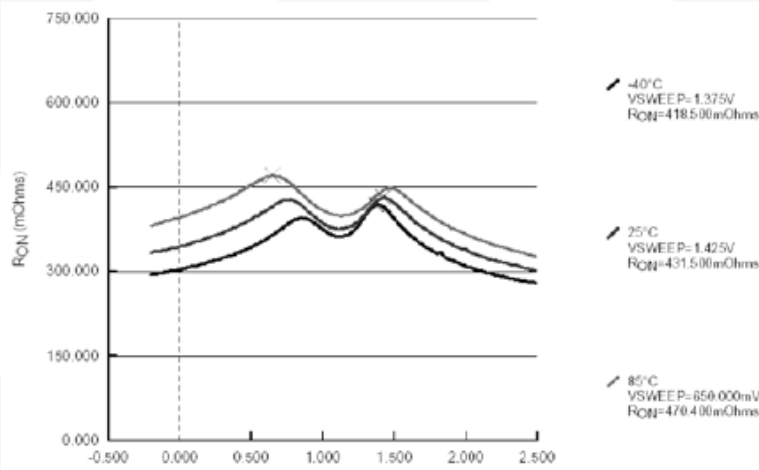


Figure 5. RON at 2.3V VCC

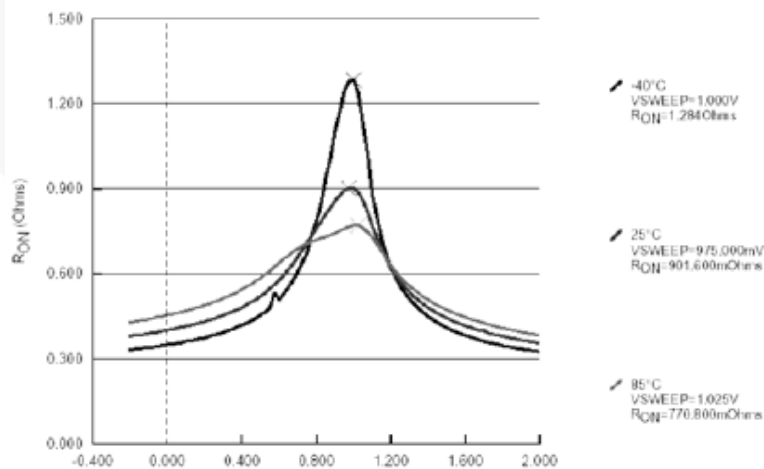
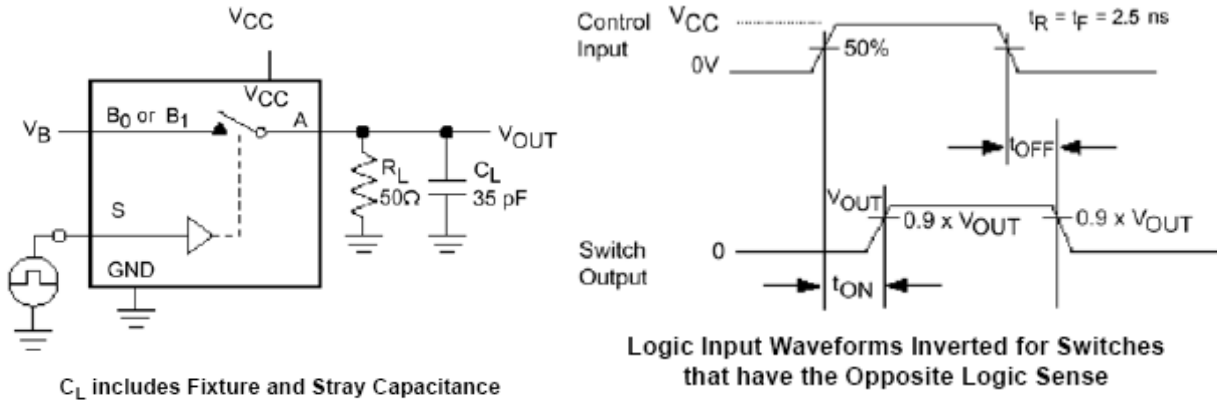


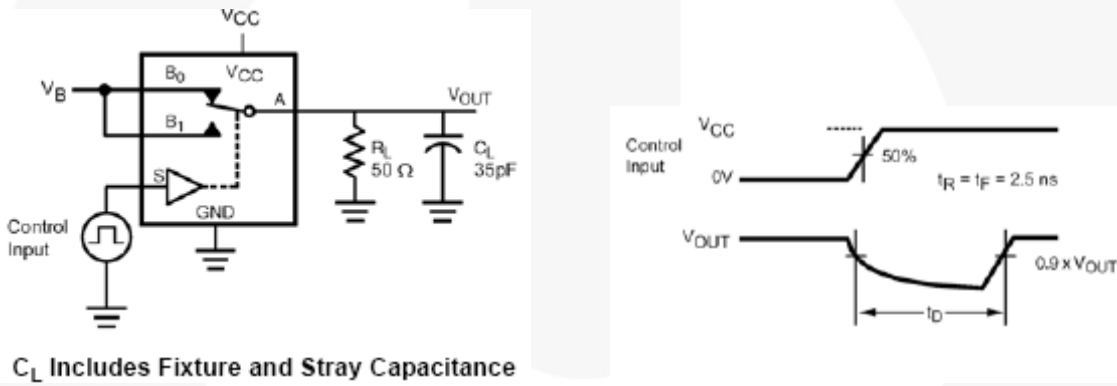
Figure 6. RON at 1.8V VCC

AC Loadings and Waveforms



C_L includes Fixture and Stray Capacitance

Figure 7. Turn-On / Turn-Off Timing



C_L Includes Fixture and Stray Capacitance

Figure 8. Break-Before-Make Timing

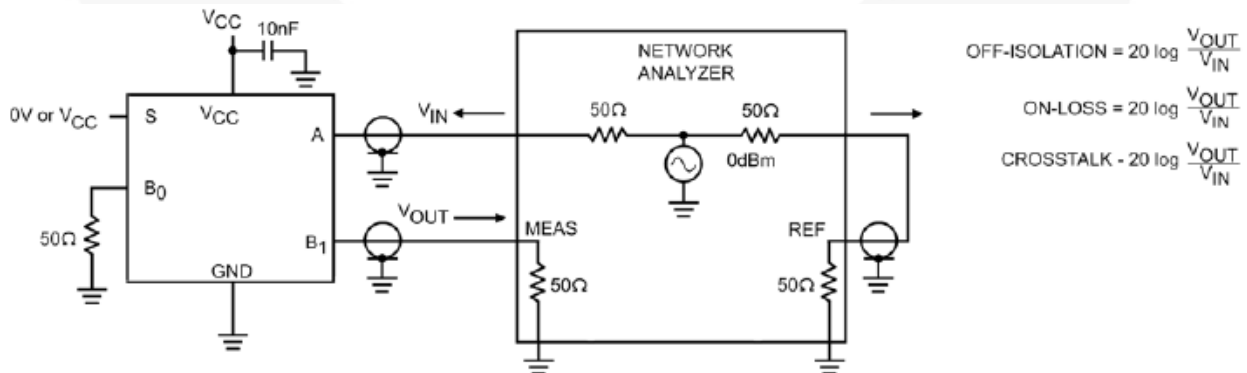


Figure 9. Off Isolation and Crosstalk

AC Loadings and Waveforms (Continued)

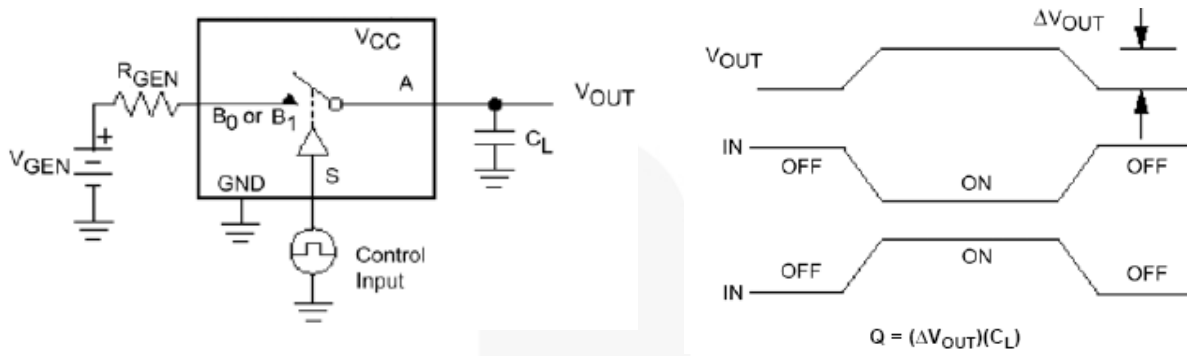


Figure 10. Charge Injection

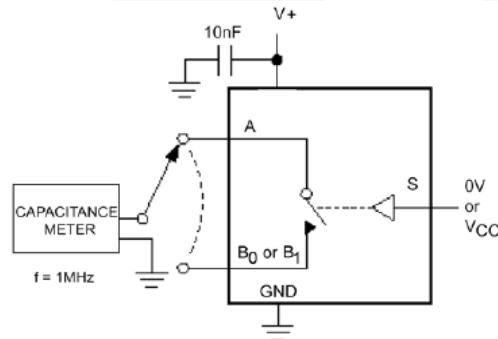


Figure 11. On / Off Capacitance Measurement Setup

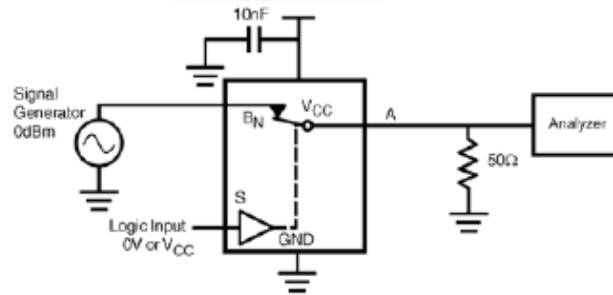


Figure 12. Bandwidth

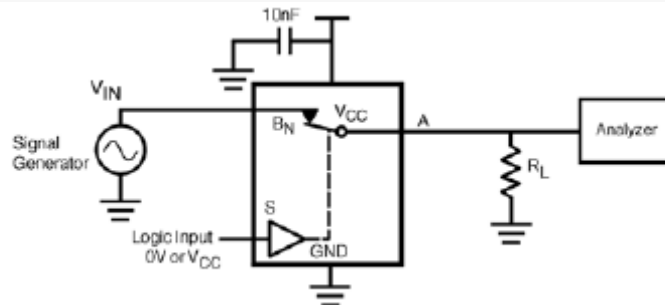
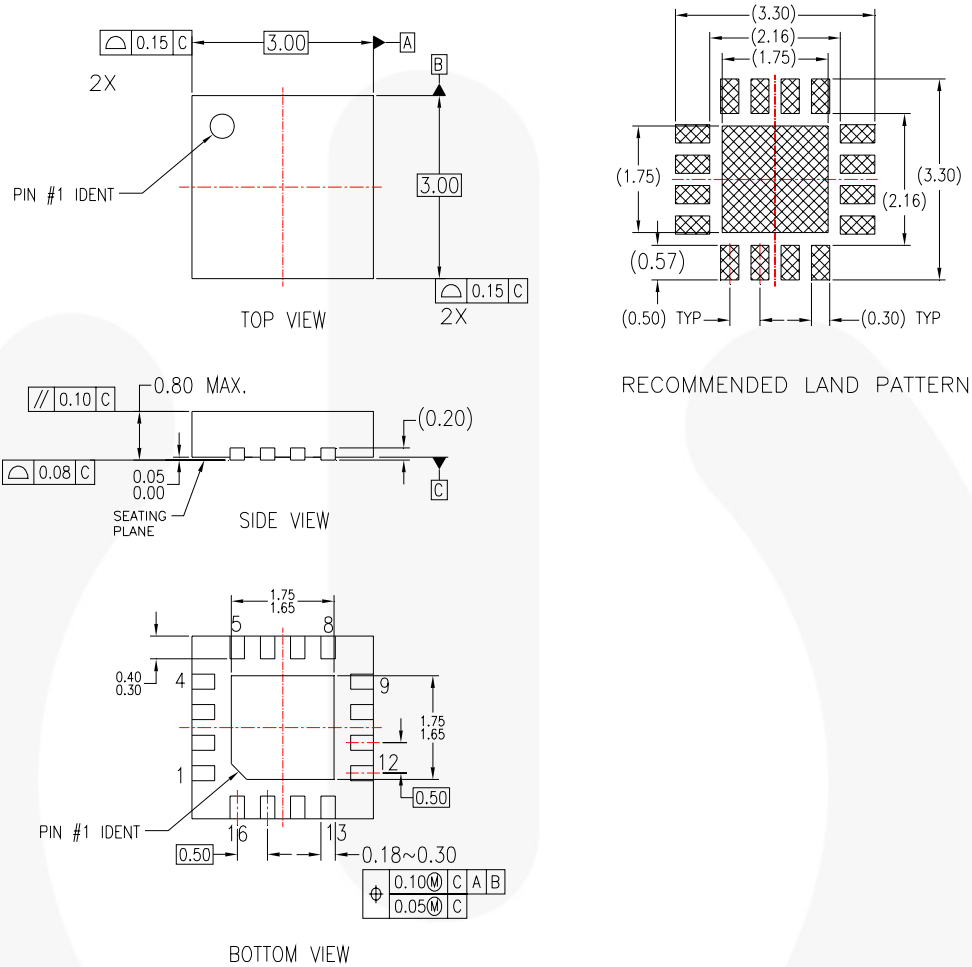


Figure 13. Harmonic Distortion

Package Dimensions



NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WEED-Pending, DATED pending
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MLP16BrevB

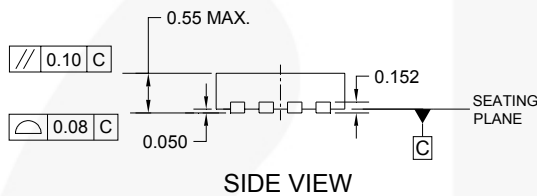
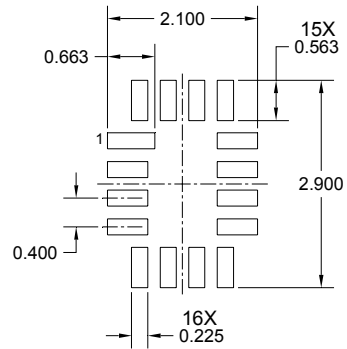
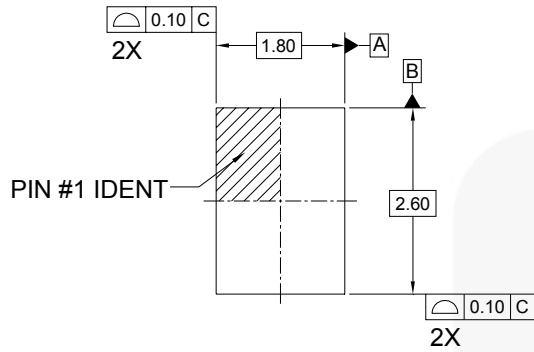
Figure 14. 16-Lead, Molded Leadless Package (MLP), JEDEC MO-220 3x3mm Square

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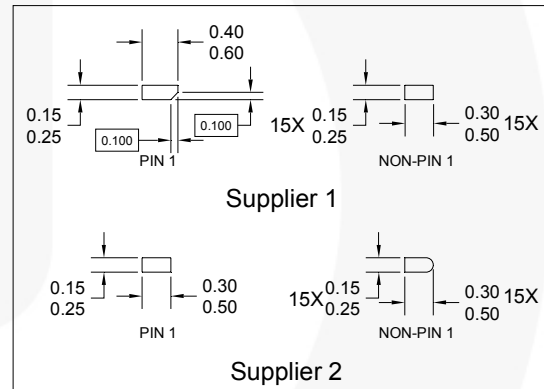
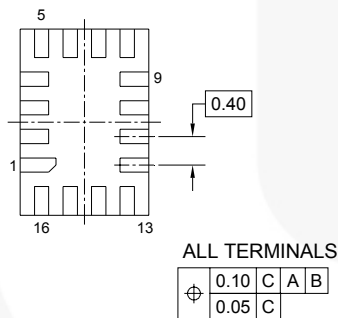
For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:
http://www.fairchildsemi.com/packaging/3x3MLP16_Pack_TNR.pdf.

Package Dimensions



RECOMMENDED LAND PATTERN

TERMINAL SHAPE VARIANTS



ALL TERMINALS

⊕	0.10 C	A	B
	0.05 C		

NOTES:

- A. THIS PACKAGE IS NOT CURRENTLY REGISTERED WITH ANY STANDARDS COMMITTEE
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS
- E. LAND PATTERN IS A MINIMAL TOE DESIGN
- F. DRAWING FILE NAME : UMLP16AREV3

Figure 15. 16-Lead, Ultrathin Molded Leadless Package (UMLP)


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