

NB4N121KMNGEVB

NB4N121KMNGEVB Evaluation Board User's Manual

Board Name: NB4N121KMNGEVB
Device Name: NB4N121KMN



ON Semiconductor®

<http://onsemi.com>

EVAl BOARD USER'S MANUAL

Description

The NB4N121K Evaluation Board was designed to provide a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the device under test NB4N121K.

The NB4N121K is a Clock differential input fanout distribution device with 1 to 21 HCSL level differential outputs, optimized for ultra low propagation delay variation. The NB4N121K is designed with HCSL clock distribution for FBDIMM applications in mind. Inputs can accept differential LVPECL, CML, or LVDS levels. Single-ended LVPECL, CML, LVCMOS or LVTTL levels are accepted with the proper V_{REFAC} supply. Clock input pins incorporate an internal $50\ \Omega$ on die termination resistors. Output drive current at I_{REF} (Pin 1) for 1X load is selected by connecting a $0\ k\Omega$ to $1\ k\Omega$ external resistor to GND. To drive a 2X load, connect the I_{REF} Pin 1 through $20\ k\Omega$ to $50\ k\Omega$ external resistors. The NB4N121K specifically guarantees low output-to-output skews. Optimal design, layout, and processing minimize skew within a device and from device to device. System designers can take advantage of the NB4N121K's performance to distribute low skew clocks across the backplane or the motherboard. The device is packaged in a low profile $8\ x\ 8\ mm$ 52-pin QFN package.

This user's manual provides detailed information on the board's contents, layout and use. The manual should be used in conjunction with the NB4N121K data sheet which contains full technical details on device specifications and operation.

Board Features

- Fully assembled evaluation board with Device-Under-Test (DUT) soldered mounted. The device may be demounted and replaced by a test fixture socket (ANTARES Test Technology, P/N FP0052QN0805C, 3350 Scott Blvd., Bldg 58, Santa Clara, CA 95054, Phone: (408) 988-6800, www.antares-att.com.) for manual insertion of different sample device units.
- Accommodates the electrical characterization of the NB4N121K in the QFN52 package
- Equal length input and output data lines to minimize skew measurement calibration.
- Default 1X output drive ($50\ \Omega$ load) with optional 2X load capability ($25\ \Omega$ load) selectable by installing pulldown resistors and adjusting board R_{REF} setting on I_{REF} (pin1). Adjustable R_{REF} resistor potentiometer for fine tuning output drive current (amplitude) levels.
- Single + 3.3 V Operation for direct LOW Impedance probe connection ($50\ \Omega$ to GND).

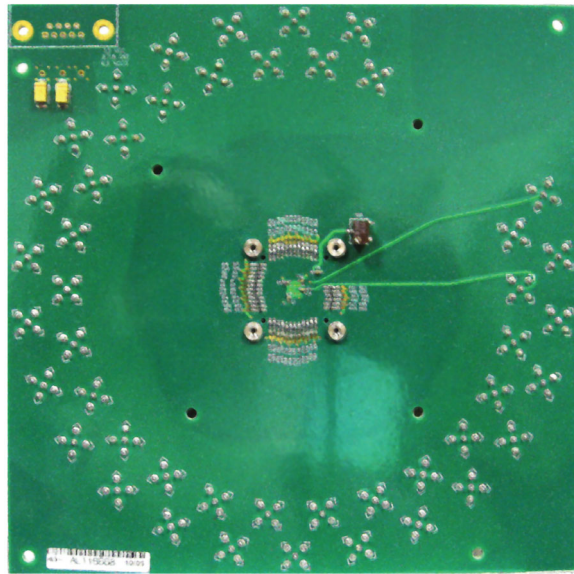
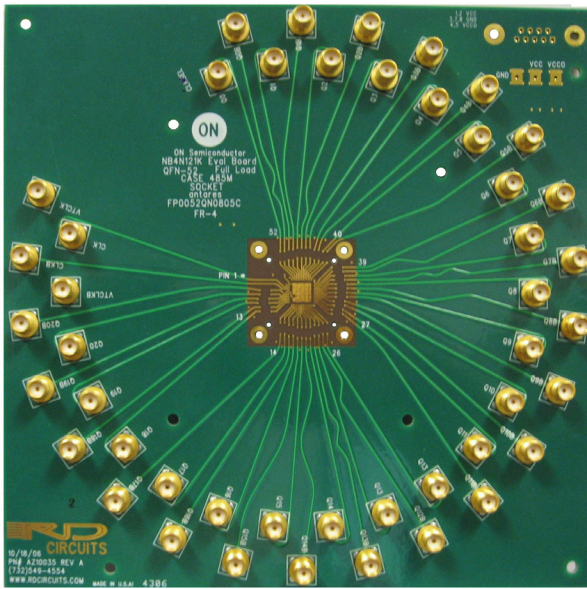
Appendix 1: Device Information

Appendix 2: Schematics

Appendix 3: I_{REF} Pin Load Plot

Appendix 4: Bill of Materials, Board Stackup

NB4N121KMNGEVB



Board Map

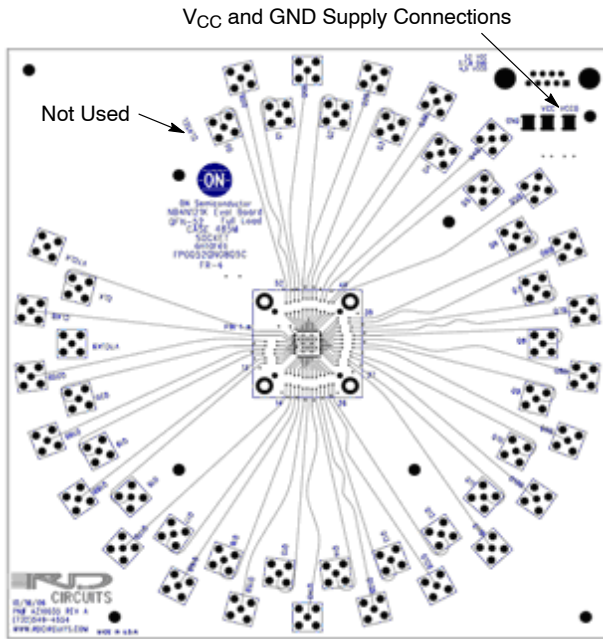


Figure 1. Front

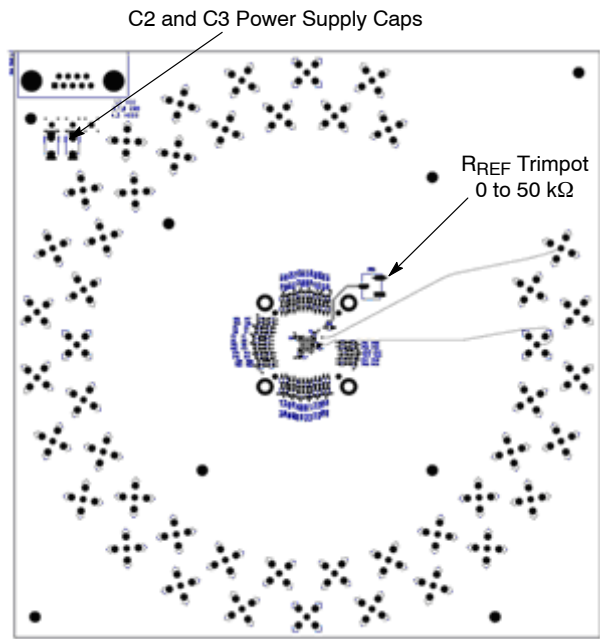


Figure 2. Back

Front Notes:

1. VCCO and VCC contacts must be ganged and connected together to the positive 3.3 V supply.
2. CLKSEL is not used (no SMA).

Back Notes:

1. C2 and C3 are power supply caps
2. RREF trimpot is connected from IREF to GND to select output drive for 1X (0 to 1 kΩ; Short to GND) or 2X loading (20 K to 50 kΩ; Open or Short to VCC). See Appendix 3: Device IREF pin 1 load plot of RREF vs. IREF current

3. Back D.U.T. area detail: (See Figure 3) Odd numbered resistors R17 to R81 are populated for 1X load. Even numbered resistors are not populated. The even numbered resistors may be repopulated with 50 Ω (to GND) components to convert the board to 2X load use with 50 Ω scope input impedance loading (presents a 25 Ω parallel load to the device outputs). Even numbered “series shorting” resistors R17 to R81 are populated zero ohm value. These may be repopulated with a series resistor value to improve signal integrity. Components C1, C4, C5, C6, and C7 are 0.01 μF bypass caps.

NB4N121KMNGEVB

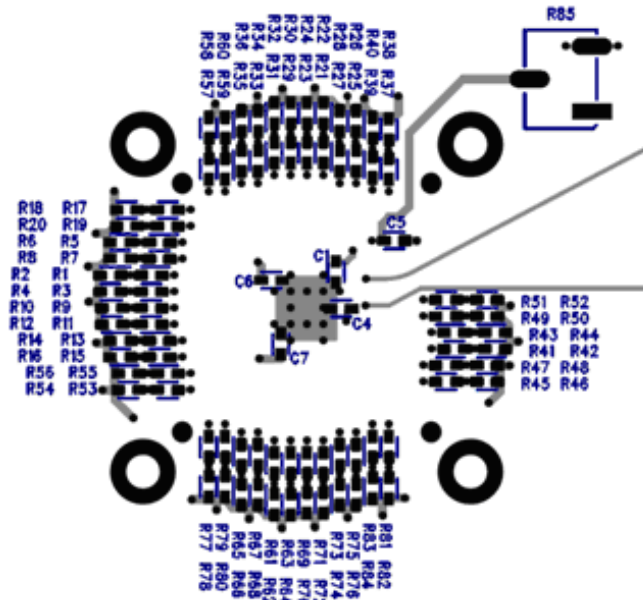


Figure 3. Back D.U.T. Area Detail

Test and Measurements Setup Details:

Step 1: Basic Equipment

- Signal Generator
- Oscilloscope
- Power Supply
- Voltmeter
- Matched High-Speed Coax Cables with SMA Connectors

Step 2: Board Test Connections Setup: (1X Load configuration, I_{REF} pin shorted to GND)

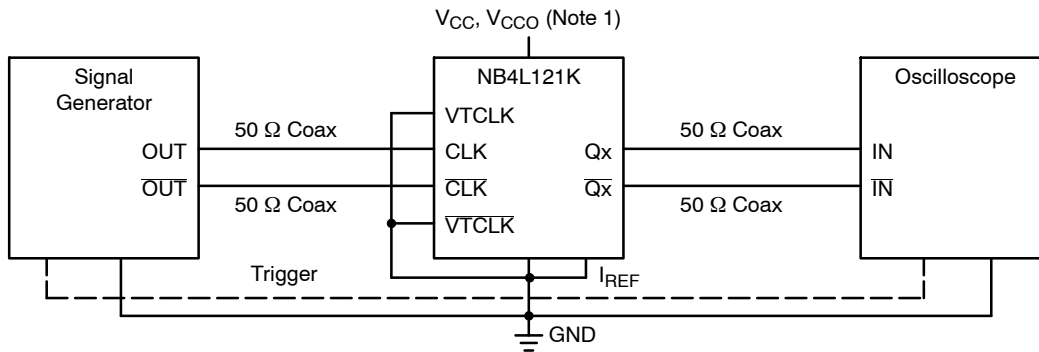


Figure 4. NB4N121KMNGEVB Evaluation Board Connector Configuration

Table 1. Power Supply Connections

Positive and GND supplies must be connected to anvil clips for proper operation. Bridge V_{CC} and V_{CCO} board connection together.

Board Connector Pin	Supply	Value	Device Pin
V_{CC} , V_{CCO} (Note 1)	V_{CC}	3.0 to 3.6 V	7, 26, 39, 52
GND	GND	0 V	2
I_{REF} (Note 2)	R_{REF} to GND	For 1x loading: 0 to 50 k Ω For 2x loading: 20 K to 50 k Ω	1
EXPOSED PAD Vias	GND	Thermal Conduit	Exposed Pad

1. Short together and connect to V_{CC} supply. See **Appendix 4: Board Lamination Stackup**
2. See **Appendix 3: Device I_{REF} pin 1 Load Plot of R_{REF} vs. I_{REF} Current**

NB4N121KMNGEVB

Table 1. Input/Output Board to Device Pin Connections

Board Connector	Device Pin Name	Device Pin
VTCLK	VTCLK	3
CLK	CLK	4
$\overline{\text{CLK}}$	$\overline{\text{CLK}}$	5
$\overline{\text{VTCLK}}$	$\overline{\text{VTCLK}}$	6
$\overline{\text{Q20}}$	$\overline{\text{Q20}}$	8
Q20	Q20	9
$\overline{\text{Q19}}$	$\overline{\text{Q19}}$	10
Q19	Q19	11
$\overline{\text{Q18}}$	$\overline{\text{Q18}}$	12
Q19	Q19	13
$\overline{\text{Q17}}$	$\overline{\text{Q17}}$	14
Q17	Q17	15
$\overline{\text{Q16}}$	$\overline{\text{Q16}}$	16
Q16	Q16	17
$\overline{\text{Q15}}$	$\overline{\text{Q15}}$	18
Q15	Q15	19
$\overline{\text{Q14}}$	$\overline{\text{Q14}}$	20
Q14	Q14	21
$\overline{\text{Q13}}$	$\overline{\text{Q13}}$	22
Q13	Q13	23
$\overline{\text{Q12}}$	$\overline{\text{Q12}}$	24
Q12	Q12	25
$\overline{\text{Q11}}$	$\overline{\text{Q11}}$	27
Q11	Q11	28
$\overline{\text{Q10}}$	$\overline{\text{Q10}}$	29
Q10	Q10	30
$\overline{\text{Q9}}$	$\overline{\text{Q9}}$	31
Q9	Q9	32
$\overline{\text{Q8}}$	$\overline{\text{Q8}}$	33
Q8	Q8	34
$\overline{\text{Q7}}$	$\overline{\text{Q7}}$	35
Q7	Q7	36
$\overline{\text{Q6}}$	$\overline{\text{Q6}}$	37
Q6	Q6	38
$\overline{\text{Q5}}$	$\overline{\text{Q5}}$	40
Q5	Q5	41
$\overline{\text{Q4}}$	$\overline{\text{Q4}}$	42
Q4	Q4	43
$\overline{\text{Q3}}$	$\overline{\text{Q3}}$	44
Q3	Q3	45
$\overline{\text{Q2}}$	$\overline{\text{Q2}}$	46
Q2	Q2	47
$\overline{\text{Q1}}$	$\overline{\text{Q1}}$	48
Q1	Q1	49
$\overline{\text{Q0}}$	$\overline{\text{Q0}}$	50
Q0	Q0	51

Input Pins and Signals

CLK and $\overline{\text{CLK}}$ pins require differential LVPECL levels swinging around an acceptable common mode voltage per datasheet. Internal impedance matching resistor of 50 Ω is provided for driver termination from input pin to the respective VTx pin. Typically the VTx pins are connected to a VTT of $V_{CC}-2.0$ V. The differential inputs can be driven single ended per the datasheet.

Output Pins and Signals

Output pairs in use must always be balance in each pins loading and termination even if only one side of an output pair is delivered to receiver or scope. Do not unbalance an output pair by loading or probing only one line. Unused outputs should be left floating open. The Rs resistors values are zero Ω , but may be changed to value such as 6 to 12 Ω to improve signal integrity.

For 1X loading, set R_{REF} potentiometer between 0 and 1 k Ω to GND for 1X loading (see Appendix 1: Device I_{REF} pin 1 load plot of R_{REF} vs. I_{REF} current).

For 50 Ω (Low Impedance) probes with High Bandwidth (>1 GHz): The odd numbered Serial Resistors R17 to R81 positions are populated with zero Ω resistors. The even numbered Parallel Loading resistors R18 to R82 should not be populated (open). Scope module inputs will provide proper termination 50 Ω to GND. Un-probed outputs will need to be externally loaded with 50 Ω to GND for proper balanced operation.

For High Impedance Probes, low input capacitance probe with High Bandwidth (>1 GHz), odd numbered Series Resistors positions R17 to R81 are populated with 0 Ω value components. The even numbered Parallel Loading resistors R18 to R82 should also all be populated with 50 Ω (to GND) components for proper termination.

For 2X loading, set the R_{REF} between 20 K and 50 k Ω to GND or tie I_{REF} directly to V_{CC} .

For 50 Ω (Low Impedance) probes with High Bandwidth (>1 GHz), the odd numbered Serial Resistors R17 to R81 positions should be populated with zero Ω value components. All even numbered Parallel Loading resistors R18 to R82 should have 50 Ω value components installed. A typical scope (probe) 50 Ω impedance in parallel with the installed even numbered Parallel Loading 50 Ω resistors R18 to R82 will present a 25 Ω (2X) load to the device. Un-probed outputs will need to be externally loaded with 50 Ω to GND to present the proper 25 Ω load to the device.

For High Impedance Probes, low input capacitance probe with High Bandwidth (>1 GHz), odd numbered Series Resistors positions R17 to R81 are populated with 0 Ω value components. The even numbered Parallel Loading resistors R18 to R82 should also all be populated with 25 Ω (to GND) components for proper termination.

Low Impedance Probes:

Use 50 Ω (Low Impedance) probes with High Bandwidth (>1 GHz). The odd numbered Resistors R18 to R82 positions should be populated with 50 Ω value components.

NB4N121KMNGEVB

A typical scope (probe) 50 Ω impedance in parallel with the installed odd numbered 50 Ω Resistor value will present a 25 Ω load to the device. Un-probed outputs will need to be externally loaded with 25 Ω to GND for proper operation.

High Impedance Probes:

Use a high impedance, low input capacitance probe with High Bandwidth (>1 GHz) and repopulate odd numbered Resistors R18 to R82 (25 Ω value).

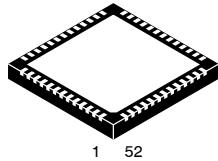
Step 3: Electrical Measurements

Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 l_{fpm}. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

APPENDIXES

Appendix 1: Device Information

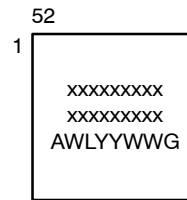
Device Under Test: NB4N121K
 Package Case Identification,
 Device Marking Diagram,
 Device Function Diagram,
 Output Loading Diagram,
 Pinout Diagram,
 Pin Description



**QFN-52
 CASE 485M
 MN SUFFIX**

Figure 5. Package Case Identification

MARKING DIAGRAM



XXXXXXXXXX	= Device Code
A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

Figure 6. Device Marking Diagram

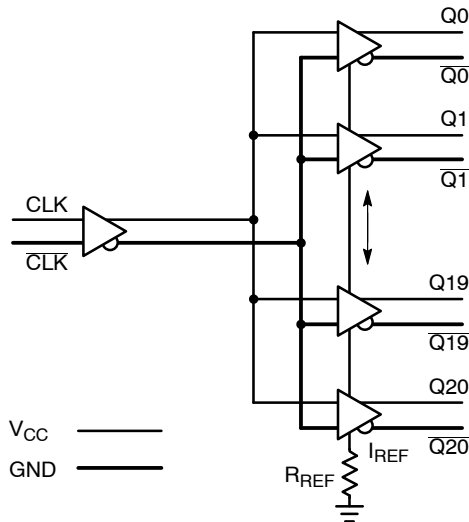


Figure 7. Device Function Diagram

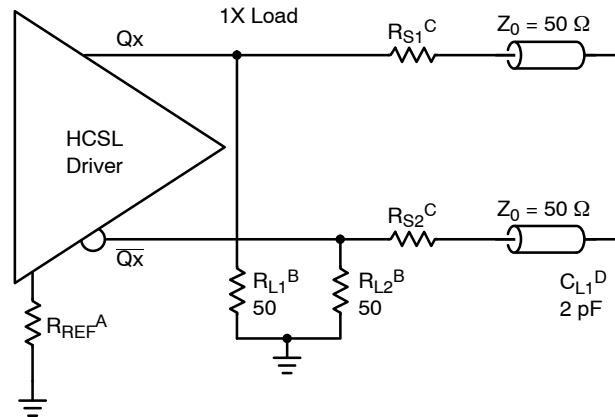


Figure 8. Output Loading Diagram

$RS1^C = 0 \Omega$
 $RREF^A = 0-1 \text{ k}\Omega$ for 1X Load, 20 K-50 K for 2X Load
 RLX^B may be open for 1X load (supplied by scope input module), may be 50 Ω for 2X load to present a 25 Ω load with scope 50 Ω input module impedance.

NB4N121KMNGEVB

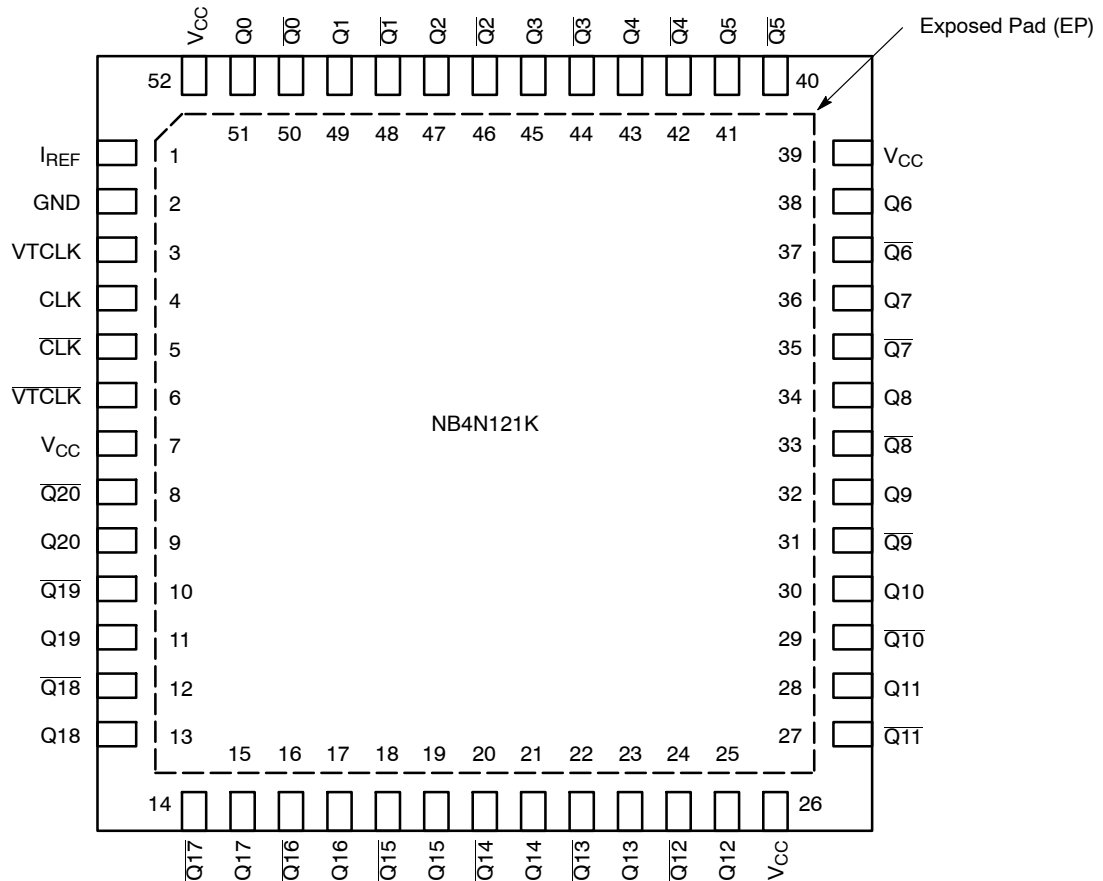


Figure 9. Pinout Diagram

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	I _{REF}	Output	Output current programming pin to select 1X or 2X load. Connect a selected resistor from I _{REF} pin to GND (See Appendix 3: Device I _{REF} pin 1 load plot of R _{REF} vs. I _{REF} current.
2	GND	-	Supply Ground. GND pin must be externally connected to power supply to guarantee proper operation.
3, 6	VTCLK, VTCLK	-	Internal 50 Ω Termination Resistor connection Pins. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device may be susceptible to self-oscillation.
4	CLK	LVPECL Input	CLOCK Input (TRUE)
5	CLK	LVPECL Input	CLOCK Input (INVERT)
7, 26, 39, 52	V _{CC}	-	Positive Supply pins. V _{CC} pins must be externally connected to a power supply to guarantee proper operation.
8, 10, 12, 14, 16, 18, 20, 22, 24, 27, 29, 31, 33, 35, 37, 40, 42, 44, 46, 48, 50	Q[20-0]	HCSL Output	Output (INVERT)
9, 11, 13, 15, 17, 19, 21, 23, 25, 28, 30, 32, 34, 36, 38, 41, 43, 45, 47, 49, 51	Q[20-0]	HCSL Output	Output (TRUE)
Exposed Pad	EP	GND	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a sufficient heat-sinking conduit for proper thermal operation. (Note 1)

Appendix 2: Schematics

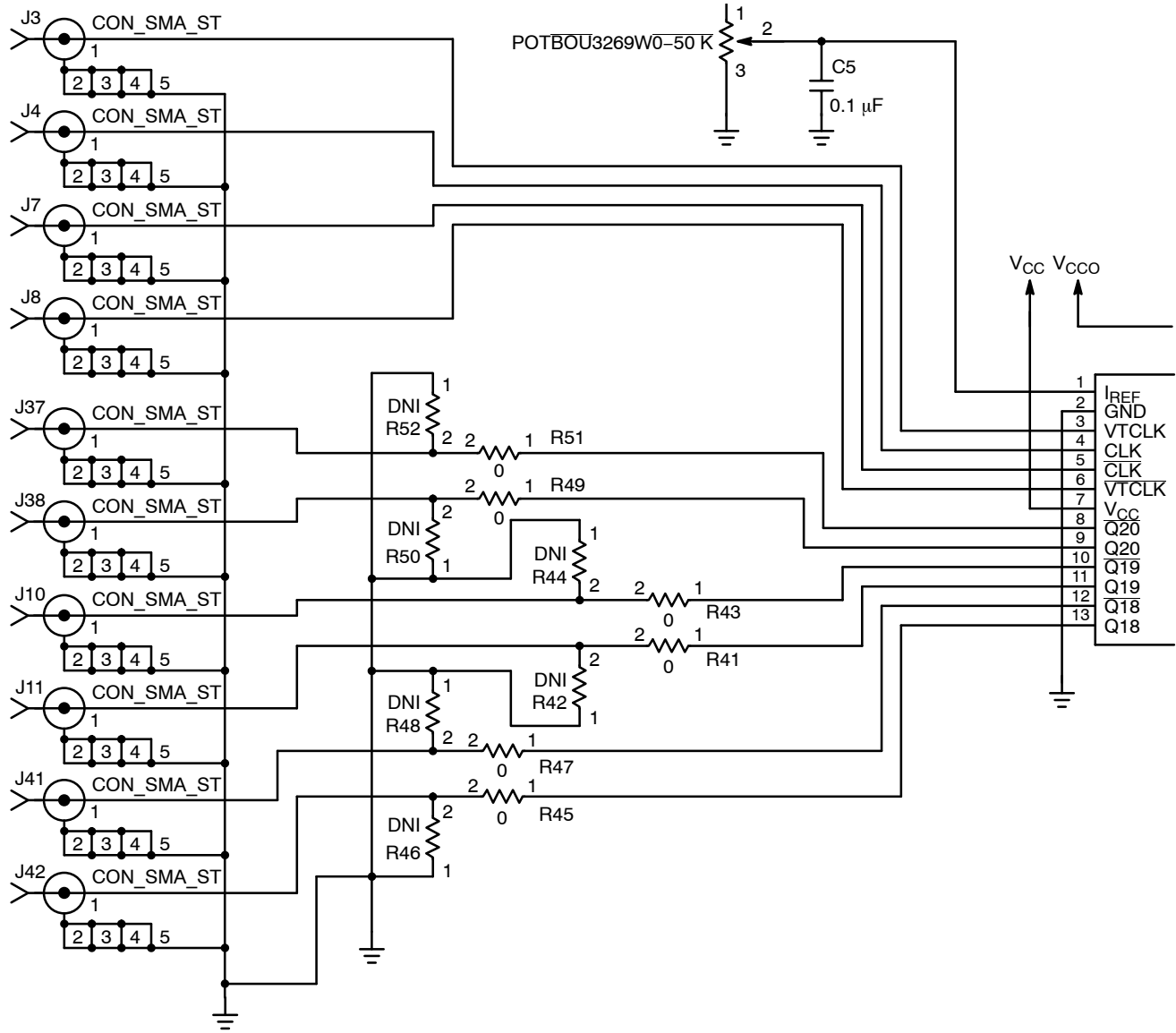


Figure 10. Pins 1 to 13

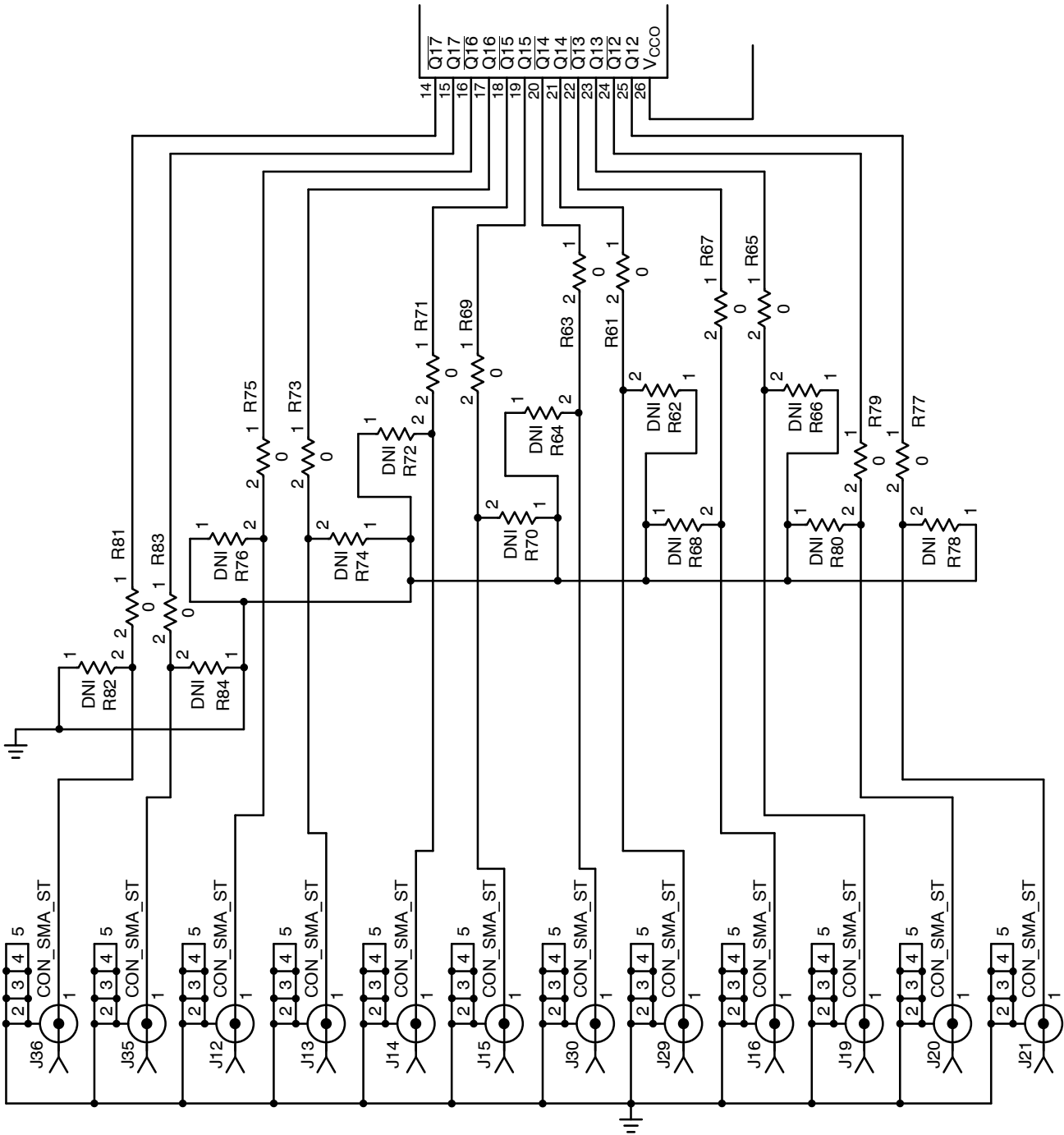


Figure 11. Pins 14 to 26

NB4N121KMNGEVB

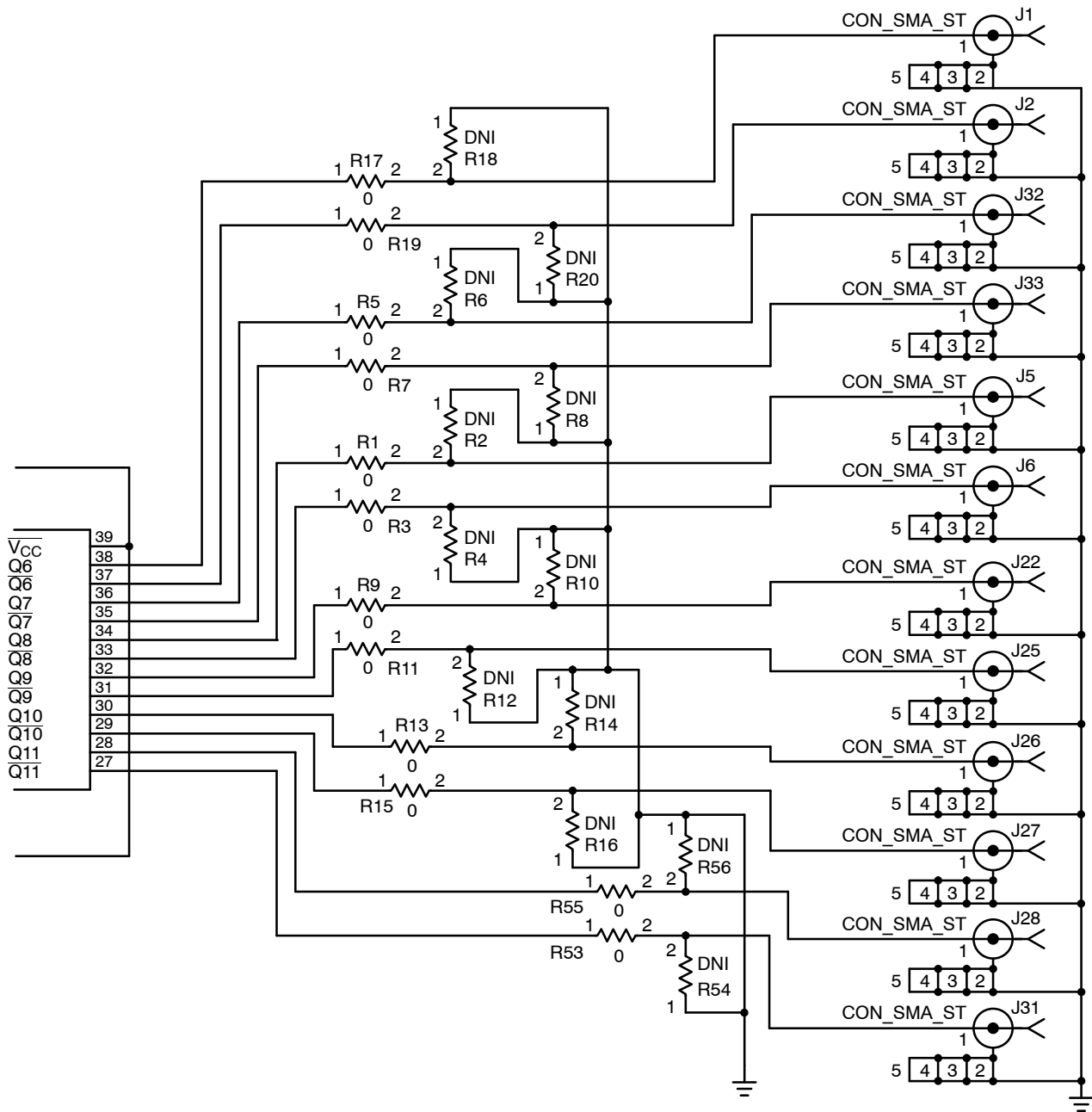


Figure 12. Pins 27 to 39

NB4N121KMNGEVB

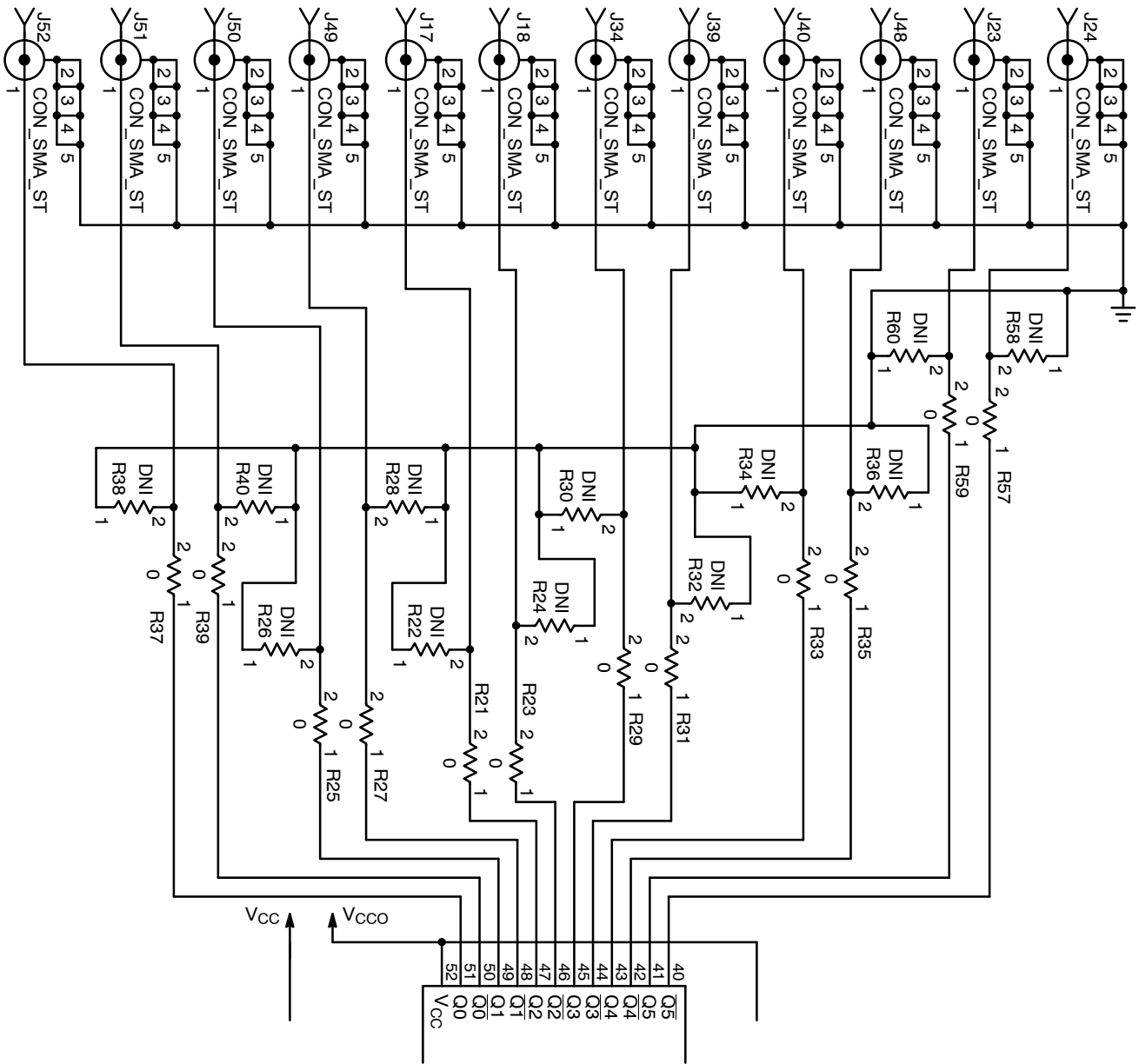


Figure 13. Pins 40 to 52

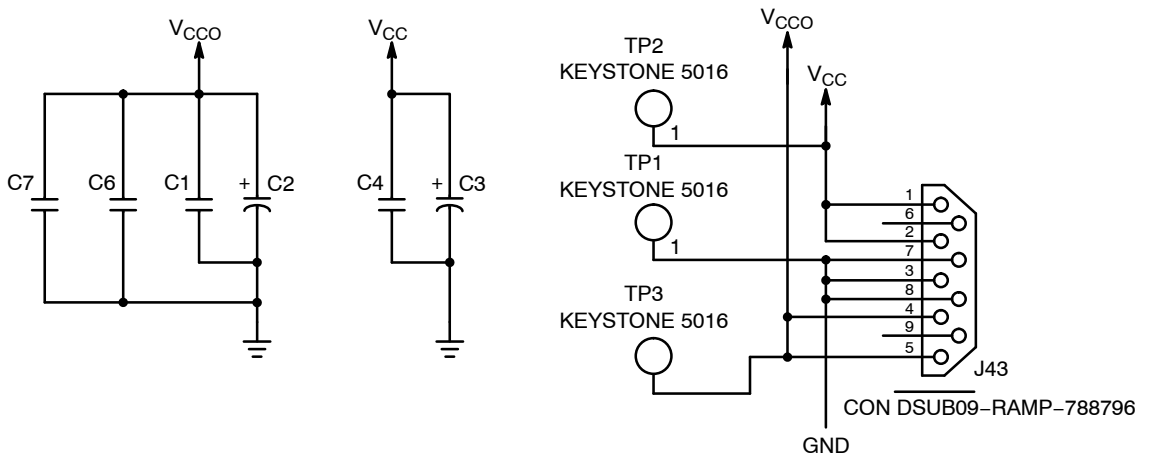


Figure 14. Schematic Bypass and Supply Connector Details

NB4N121KMNGEVB

Appendix 3: Device I_{REF} Pin 1 Load Plot of R_{REF} vs. I_{REF} Current

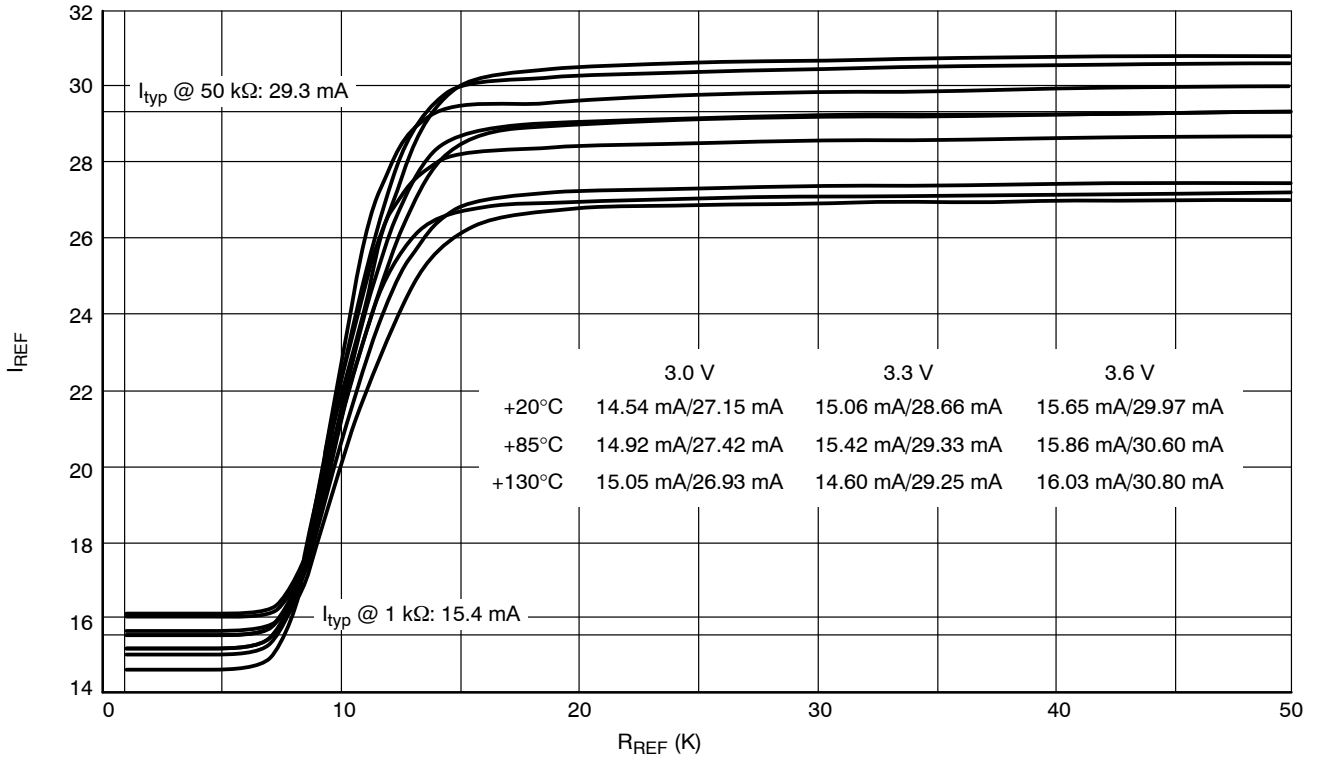


Figure 15. Device I_{REF} pin 1 Load Plot of R_{REF} vs. I_{REF} Current

NB4N121KMNGEVB

Appendix 4: Bill of Materials, Board Lamination Stackup, and Fabrication Notes

Bill of Materials Table

Top	Bot	Description	Value	Source	Source P/N	Reference Designators
0	5	Cap, Chip, 0.1 μ F, 0603, 50 V, 10% X7R	0.1 μ F			C1, C4, C5, C6, C7
0	2	Cap, Chip, 10 μ F, Tant "C", 25 V, 10%	10 μ F			C2, C3
1	0	ANTARES 52 QFN Socket			FP0052QN0805C	Alternative construction option: ANTARES Test Technology 3350 Scott Blvd., Bldg 58, Santa Clara, CA 95054, Phone: (408) 988-6800, www.antares-att.com
	4	2-56 Pem Nuts				DUT1
3		TP1, TP2, TP3				KEYSTONE 5016 (or similar)
46	0	Connector, SMA, Straight		Johnson	142-0701-201	J1, J2, J3, J4, J5, J6, J7, J8, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J48, J49, J50, J51, J52
1		J43			CON DSUB09-RAMP-788796	J43 (Optional - Not Supplied)
0	42	Res, Chip, 0 Ω , 0603, 1/16 W, 5%	0			R1, R3, R5, R7, R9, R11, R13, R15, R17, R19, R21, R23, R25, R27, R29, R31, R33, R35, R37, R39, R41, R43, R45, R47, R49, R51, R53, R55, R57, R59, R61, R63, R65, R67, R69, R71, R73, R75, R77, R79, R81, R83
0	1	0-50 K POTENTIOMETER, TOP ADJUST	0-50 k Ω	BOURNS	3269W-1-503	R85

Board Lamination Stackup:

Dielectric is FR4 (interlayer between 1-2, 2-3, 3-4, 4-5, 5-6).

Layers #1 (Topside) and #6 (Bottomside) are signal path copper (trace width 0.014").

LAMINATION DIAGRAM					
Layer Number	Layer Name	Copper Thickness	Dielectric Thickness	Layer Material	Trace Width
1	TOP	1/2 OZ.			0.014
			0.008	See Note 1	
2	GND	1 OZ.			N/A
			0.005	See Note 1	
3	PWR1	1 OZ.			N/A
			Adjust	See Note 1	
4	PWR2	1 OZ.			N/A
			0.005	See Note 1	
5	GND	1 OZ.			N/A
			0.008	See Note 1	
6	BTN	1/2 OZ.			0.014

FINISHED PCB THICKNESS TO BE:	0.100 \pm 10%
-------------------------------	-----------------

Board Fabrication Notes:

(Unless otherwise specified)

1. **ARTWORK:**
Fabricate using ADC artwork No. AZ10035 Rev A.
Drill locations determined by ADC file
AZ10035NC.DRL
2. **MATERIAL:**
High temp FR4 – 170°C Tg
3. **BOARD THICKNESS:**
Refer to stacking diagram for finished board thickness.
4. **TWIST AND WARP:**
Board twist shall not exceed 0.5% (0.005 in.) per linear inch.
5. **PLATING:**
Copper thickness for internal and external layers is specified in the stacking diagram.
Finished PCB to be electrodeposited hard gold plate, type 1 (99.7% min gold), grade C (knoop hardness 130–200), class X, 3–10 micro inches thick, over entire board surface.
Selective plating is not required.

Hole Plating:

0.011 minimum barrel avg. / 0.009 absolute minimum. Absolute maximum to be determined by PCB vendor based on the required finished hole diameter. Hole diameters are after plating unless otherwise specified.

5.1 – Surface pads in this area to be free from any irregularities or defects that might hinder proper performance of the pad.

6. **ANNULAR RING:**
Annular ring to be 0.005 minimum with top to bottom registration to be within 0.003.

7. **SOLDERMASK:**
Apply soldermask, color: green, type: LP1, per artwork provided. If VIA plugs are required, plug pattern will be supplied with artwork.
8. **SILKSCREEN:**
To be white, non-conductive ink per artwork. No ink is to be on plated thru hole or surface mount pads. Silkscreen lines and text width are to be 0.006 minimum.
9. **SOLDERABILITY:**
Plated holes shall not be rough or irregular so as to prevent proper solder wicking.
10. **DRILL CHART:**
Hole sizes specified are finished hole sizes, unless otherwise specified:
Standard plated hole tolerance is ± 0.003
Standard non-plated hole tolerance is ± 0.002
11. **IMPEDANCE:**
Impedance controlled layers: 1, 6.
12. **APPROVAL:**
100% continuity and isolation test required for each fabricated PCB. Final test data must be cross referenced to the IPC-D-356 file provided. A verification stamp is required on each PCB. A TDR report shall be provided for each impedance controlled layer at the time of shipment. Final acceptance shall be determined by these layers having a characteristic impedance of 50 ohms $\pm 10\%$. Vendor can make line width adjustments on impedance controlled conductor widths of 0.0005. All other artwork deviations must have prior approval from R&D ADC.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

The evaluation board/kit (research and development board/kit) (hereinafter the "board") is not a finished product and is as such not available for sale to consumers. The board is only intended for research, development, demonstration and evaluation purposes and should as such only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. This person assumes full responsibility/liability for proper and safe handling. Any other use, resale or redistribution for any other purpose is strictly prohibited.

The board is delivered "AS IS" and without warranty of any kind including, but not limited to, that the board is production-worthy, that the functions contained in the board will meet your requirements, or that the operation of the board will be uninterrupted or error free. ON Semiconductor expressly disclaims all warranties, express, implied or otherwise, including without limitation, warranties of fitness for a particular purpose and non-infringement of intellectual property rights.

ON Semiconductor reserves the right to make changes without further notice to any board.

You are responsible for determining whether the board will be suitable for your intended use or application or will achieve your intended results. Prior to using or distributing any systems that have been evaluated, designed or tested using the board, you agree to test and validate your design to confirm the functionality for your application. Any technical, applications or design information or advice, quality characterization, reliability data or other services provided by ON Semiconductor shall not constitute any representation or warranty by ON Semiconductor, and no additional obligations or liabilities shall arise from ON Semiconductor having provided such information or services.

The boards are not designed, intended, or authorized for use in life support systems, or any FDA Class 3 medical devices or medical devices with a similar or equivalent classification in a foreign jurisdiction, or any devices intended for implantation in the human body. Should you purchase or use the board for any such unintended or unauthorized application, you shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the board.

This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and may not meet the technical requirements of these or other related directives.

FCC WARNING – This evaluation board/kit is intended for use for engineering development, demonstration, or evaluation purposes only and is not considered by ON Semiconductor to be a finished end product fit for general consumer use. It may generate, use, or radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment may cause interference with radio communications, in which case the user shall be responsible, at its expense, to take whatever measures may be required to correct this interference.

ON Semiconductor does not convey any license under its patent rights nor the rights of others.

LIMITATIONS OF LIABILITY: ON Semiconductor shall not be liable for any special, consequential, incidental, indirect or punitive damages, including, but not limited to the costs of requalification, delay, loss of profits or goodwill, arising out of or in connection with the board, even if ON Semiconductor is advised of the possibility of such damages. In no event shall ON Semiconductor's aggregate liability from any obligation arising out of or in connection with the board, under any theory of liability, exceed the purchase price paid for the board, if any.

For more information and documentation, please visit www.onsemi.com.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative