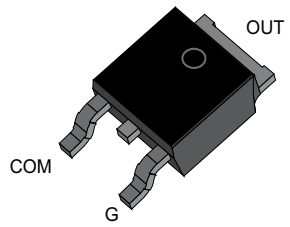
# ACST310-8B

## Overvoltage protected AC switch

**Datasheet – production data**




DPAK

## Features

- AC switch with self over voltage protection
- Microcontroller direct driven (low gate current max. 10 mA)
- Three quadrants (Q1, Q2 and Q3)
- UL94-V0 qualified resin (flammability)
- ECOPACK®2 compliant component

### Benefits

- Enables equipment to meet IEC61000-4-5
- High immunity against fast transients described in IEC61000-4-4 standard
- Needs no external overvoltage protection
- High off-state reliability power device
- Interfaces directly with the microcontroller
- Reduces component count

## Applications

- AC static switching in appliances and industrial control systems
- Driving low power highly inductive loads or resistive AC loads, such as motor control circuits, small home appliances, lighting, fan speed controllers, water valves, pumps, solid state relays, vacuum cleaners, heaters

## Description

The ACST310-8B belongs to the ACS™ / ACST power switch family built with A.S.D.® (application specific discrete) technology. This high performance device is suited to home appliances or industrial systems and drives loads up to 3 A.

This ACST310-8B switch embeds a Triac structure and a high voltage clamping device able to absorb the inductive turn-off energy and withstand line transients such as those described in the IEC 61000-4-5 standard.The component needs a low gate current to be activated ($I_{GT}$ max. 10 mA) and still shows a high electrical noise immunity complying with IEC standards such as IEC 61000-4-4 (fast transient burst test).

**Figure 1. Functional diagram**

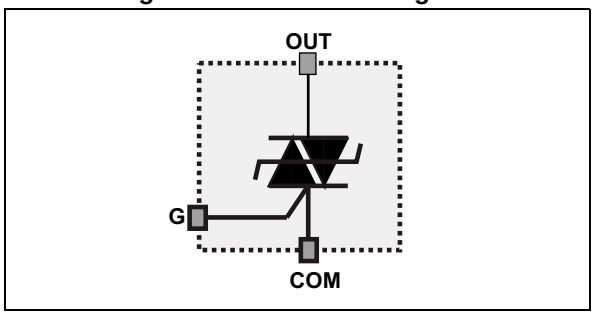



**Table 1. Device summary**

| Symbol | Value | Unit |
|---|---|---|
| $I_{T(RMS)}$ | 3 | A |
| $I_{GT(Q1, Q2, Q3)}$ | 10 | mA |
| $V_{DRM}/V_{RRM}$ | 800 | V |

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# 1 Characteristics

**Table 2. Absolute ratings (limiting values)**

| Symbol | Parameter | Test conditions | | Value | Unit |
|---|---|---|---|---|---|
| $I_{T(RMS)}$ | On-state RMS current (full sine wave) | | $T_c$ = 112 °C | 3 | A |
| $I_{TSM}$ | Non repetitive surge peak on-state current ($T_j$ initial = 25 °C) | f = 50 Hz | tp = 20 ms | 20 | A |
| | | f = 60 Hz | tp = 16.7 ms | 21 | |
| $I^2t$ | $I^2t$ value for fusing | | tp = 10 ms | 2.6 | $A^2s$ |
| dI/dt | Critical rate of rise of on-state current $I_G$ = 2 x $I_{GT,}$ $t_r$ = 100 ns | f = 120 Hz | $T_J$ = 125 °C | 50 | A/µs |
| $V_{PP}$(1) | Non repetitive line peak mains voltage | | $T_J$ = 25 °C | 2 | kV |
| $P_{G(AV)}$ | Average gate power dissipation | | $T_J$ = 125°C | 0.1 | W |
| $P_{GM}$ | Peak gate power | $t_p$ = 20 µs | $T_J$ = 125 °C | 10 | W |
| $I_{GM}$ | Peak gate current | $t_p$ = 20 µs | $T_J$ = 125°C | 1.6 | A |
| $T_{stg}$ | Storage junction temperature range | | | -40 to +150 | °C |
| $T_j$ | Operating junction temperature range | | | -40 to +125 | °C |
| $T_L$ | Maximum lead temperature for soldering during 10 s | | | 260 | °C |

1. according to test described by standard IEC 61000-4-5 standard (see *Figure 16*).

**Table 3. Electrical characteristics**

| Symbol | Test conditions | Quadrant | $T_j$ | Value | | Unit |
|---|---|---|---|---|---|---|
| $I_{GT}$(1) | $V_{OUT}$ = 12 V, $R_L$ = 33 Ω | I - II - III | 25 °C | Max. | 10 | mA |
| $V_{GT}$ | | | | Max. | 1.1 | V |
| $V_{GD}$ | $V_{OUT}$ = $V_{DRM,}$ $R_L$ = 3.3 kΩ | I - II - III | 125 °C | Min. | 0.2 | V |
| $I_H$(2) | $I_{OUT}$ = 100 mA | | 25 °C | Max. | 20 | mA |
| $I_L$ | $I_G$ = 1.2 x $I_{GT}$ | I - III | 25 °C | Max. | 25 | mA |
| | | II | | | 35 | |
| dV/dt(2) | $V_{OUT}$ = 67% $V_{DRM}$, gate open | | 125 °C | Min. | 1000 | V/µs |
| (dI/dt)c(2) | (dV/dt)c = 0.1V/µs | | 125 °C | Min. | 5 | A/ms |
| (dI/dt)c(2) | (dV/dt)c = 10 V/µs | | 125 °C | Min. | 1 | A/ms |
| $V_{CL}$ | $I_{CL}$ = 0.1 mA, tp = 1 ms | | 25 °C | Min. | 850 | V |

1. Minimum $I_{GT}$ is guaranteed at 5% of $I_{GT}$ max.
2. For both polarities of OUT pin referenced to COM pin

**Table 4. Static characteristics**

| Symbol | Test conditions | | Value | | Unit |
|---|---|---|---|---|---|
| $V_{TM}$(1) | $I_{TM}$ = 4.2 A, $t_p$ = 380 µs | $T_j$ = 25 °C | Max. | 1.8 | V |
| $V_{TO}$(1) | Threshold voltage | $T_j$ = 125°C | Max. | 0.9 | V |
| $R_D$(1) | Dynamic resistance | $T_j$ = 125 °C | Max. | 200 | mΩ |
| $I_{DRM}$ $I_{RRM}$ | $V_{OUT}$ = $V_{DRM}$ / $V_{RRM}$ | $T_j$ = 25 °C | Max. | 10 | µA |
| | | $T_j$ = 125 °C | | 500 | |

1. For both polarities of OUT pin referenced to COM pin

**Table 5. Thermal resistances**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(j-c)}$ | Junction to case (AC) | 3 | °C/W |
| $R_{th(j-a)}$ | Junction to ambient | 70 | °C/W |

**Figure 2. Maximum power dissipation versus RMS on-state current (full cycle)**

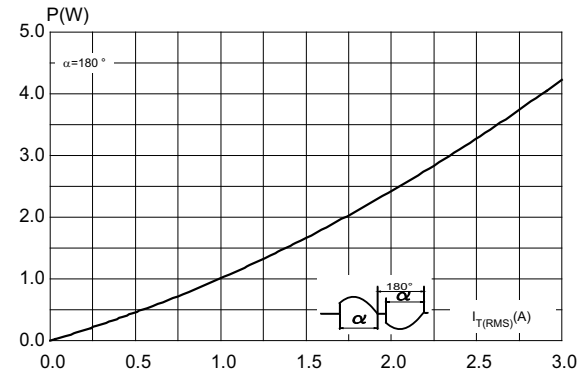



**Figure 3. On-state RMS current versus case temperature**

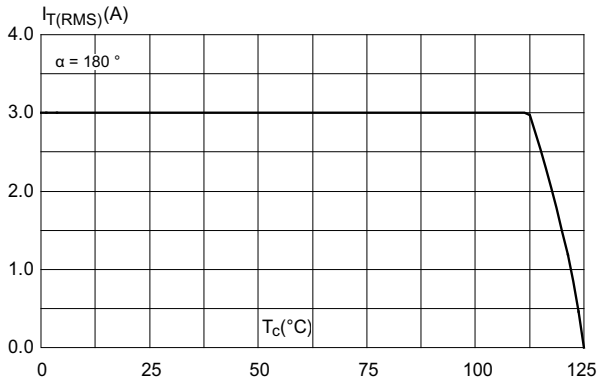


**Figure 4. On-state RMS current versus ambient temperature (free air convection)**

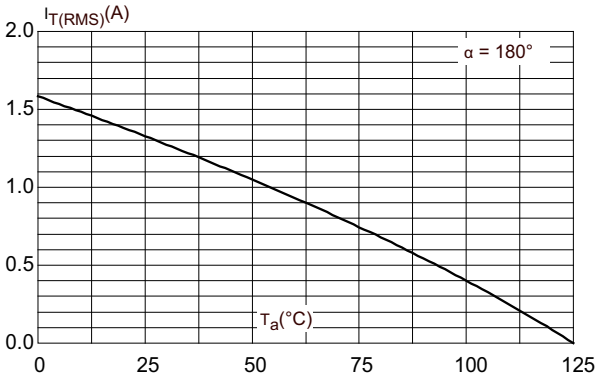



**Figure 5. Relative variation of thermal impedance versus pulse duration**

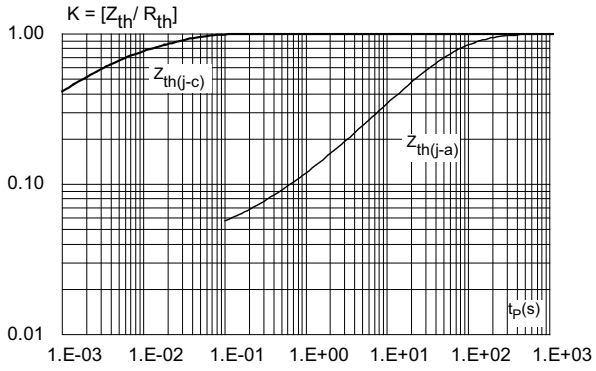



**Figure 6. Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10ms**

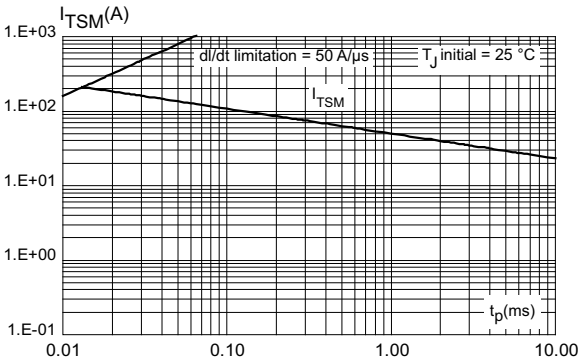



**Figure 7. Surge peak on-state current versus number of cycles**

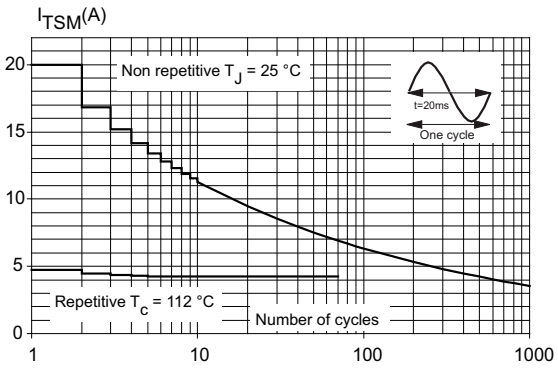


**Figure 8. Relative variation of holding current and latching current versus junction temperature (typical values)**

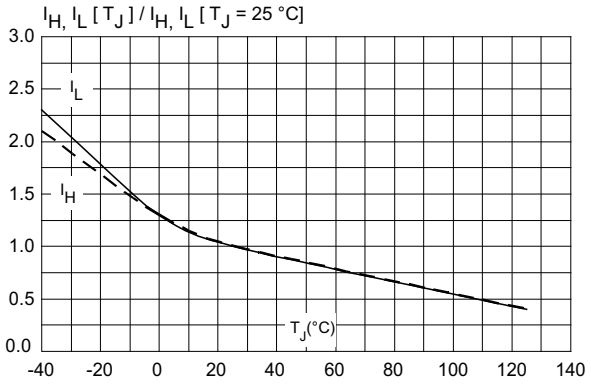



**Figure 9. Relative variation of gate trigger current and gate trigger voltage versus junction temperature (typical values)**

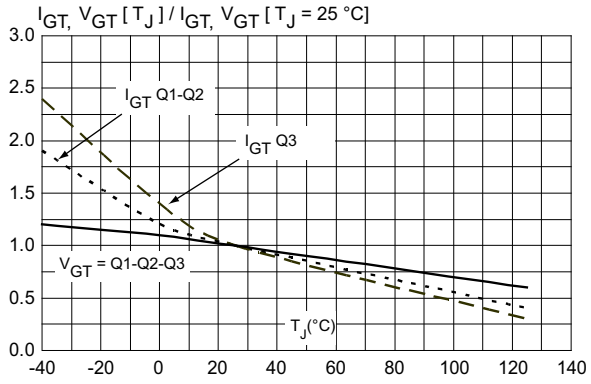



**Figure 10. On-state characteristics (maximum values)**

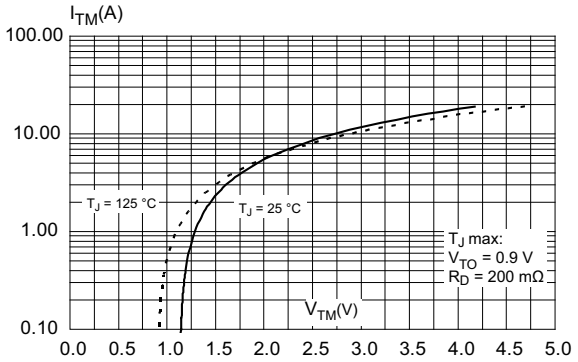



**Figure 11. Relative variation of critical rate of decrease of main current versus junction temperature (typical values)**

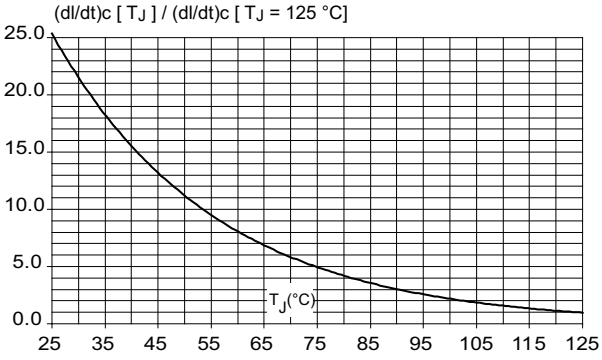


**Figure 12. Relative variation of static dV/dt immunity versus junction temperature**

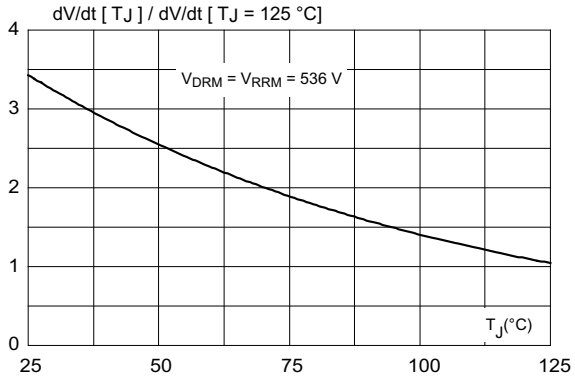



**Figure 13. Relative variation of leakage current versus junction temperature (typical values)**

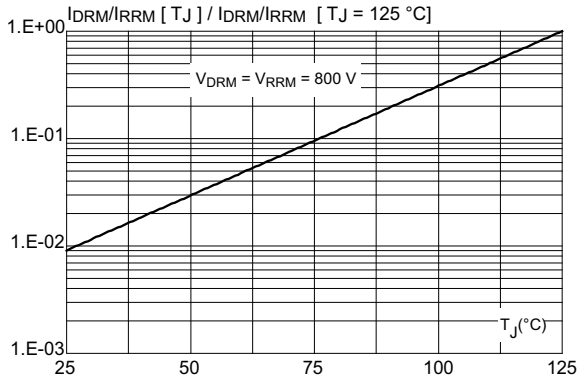
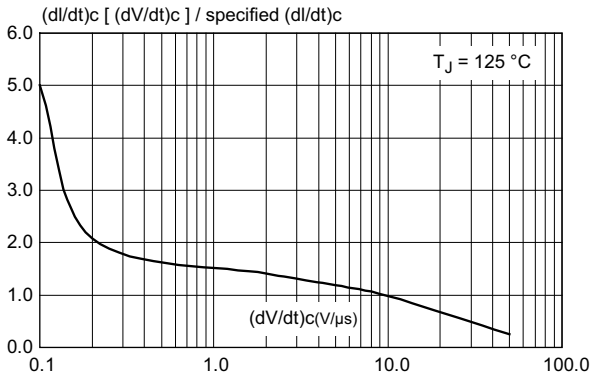



**Figure 14. Relative variation of critical rate of decrease of main current versus reapplied (dV/dt)c**



# 2 Application information

## 2.1 Typical application description

The ACST310 device has been designed to switch on and off, or by phase angle control, highly inductive or resistive loads such as pump, valve, fan, or bulb lamps. Thanks to its high sensitivity ($I_{GT}$ max = 10 mA), the ACST310 can be driven directly by logic level circuits through a resistor as shown on the typical application diagram (*Figure 15*).

**Figure 15. AC induction motor control - typical diagram**

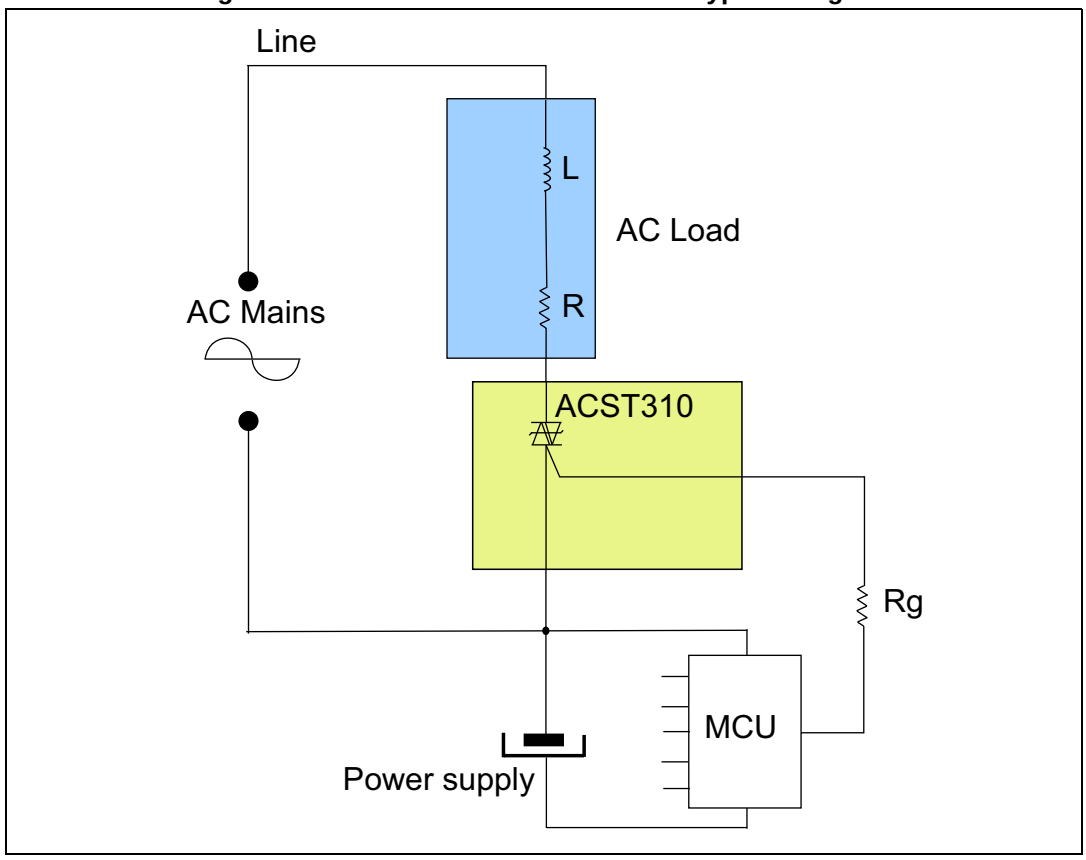
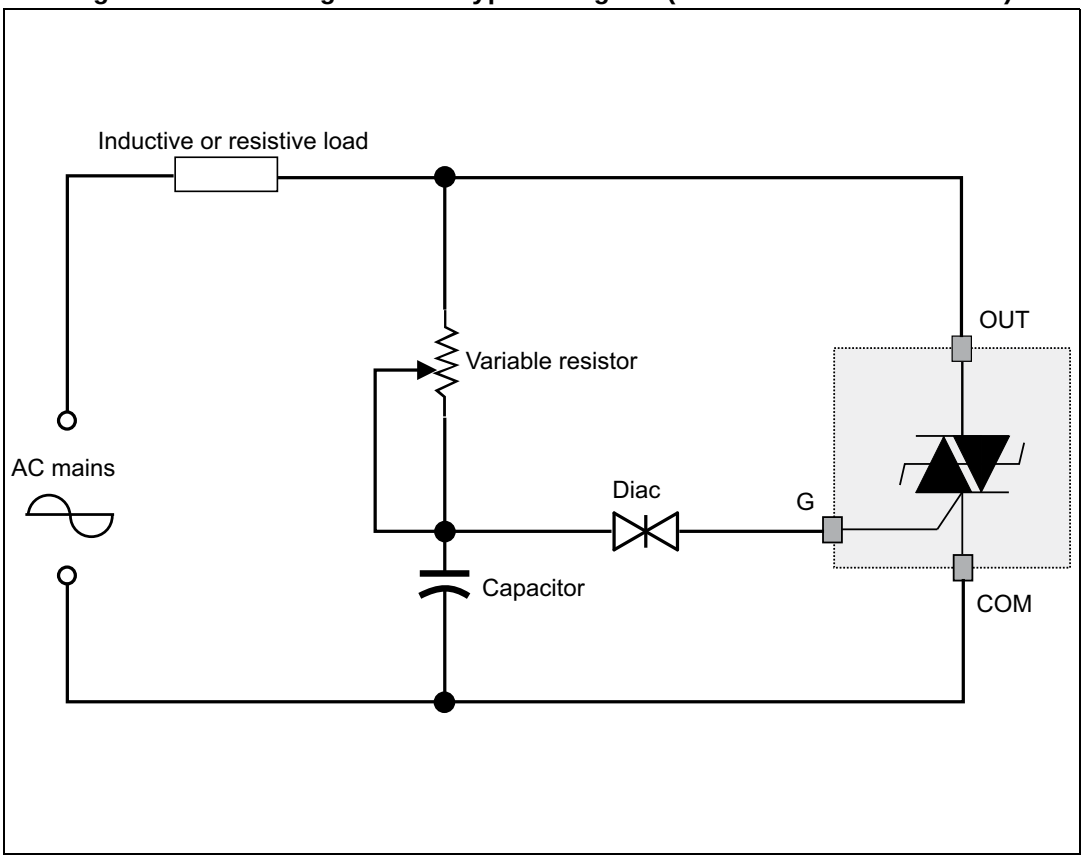


**Figure 16. Phase angle control typical diagram (inductive or resistive load)**



## 2.2 AC line transient voltage ruggedness

In comparison with standard Triacs, which are not robust against surge voltage, the ACST310 is self-protected against over-voltage, specified by the parameter $V_{CL}$. In addition, the ACST310 is a sensitive device ($I_{GT}$ max. 10 mA), but provides a high noise immunity level against fast transients. The ACST310 switch can safely withstand AC line transient voltages either by clamping the low energy spikes, such as inductive spikes at switch off, or by switching to the on state (for less than 10 ms) to dissipate higher energy shocks through the load. This safety feature works even with high turn-on current ramp up.

The test circuit of *Figure 17* represents the ACST310 application, and is used to stress the ACST310 switch according to the IEC 61000-4-5 standard conditions. With the additional effect of the load which is limiting the current, the ACST310 switch withstands the voltage spikes up to 2 kV on top of the peak line voltage. The protection is based on an overvoltage crowbar technology. The ACST310 folds back safely to the on state as shown in *Figure 18*. The ACST310 recovers its blocking voltage capability after the surge and the next zero current crossing. Such a non-repetitive test can be done at least 10 times on each AC line voltage polarity.

**Figure 17. Overvoltage ruggedness test circuit for resistive and inductive loads for IEC 61000-4-5 standards**

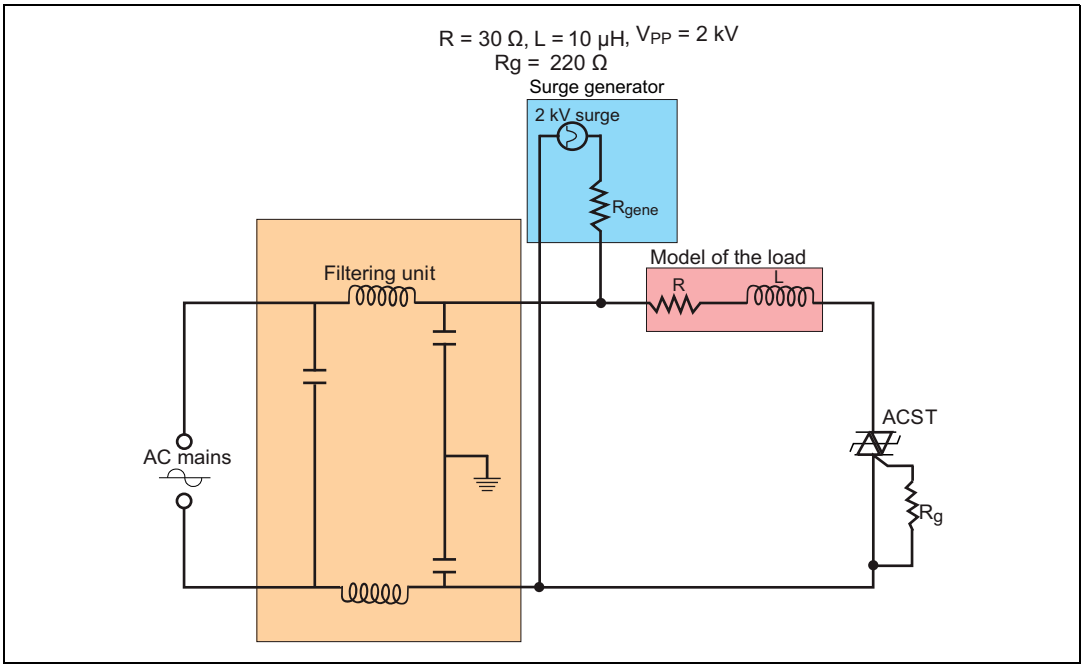
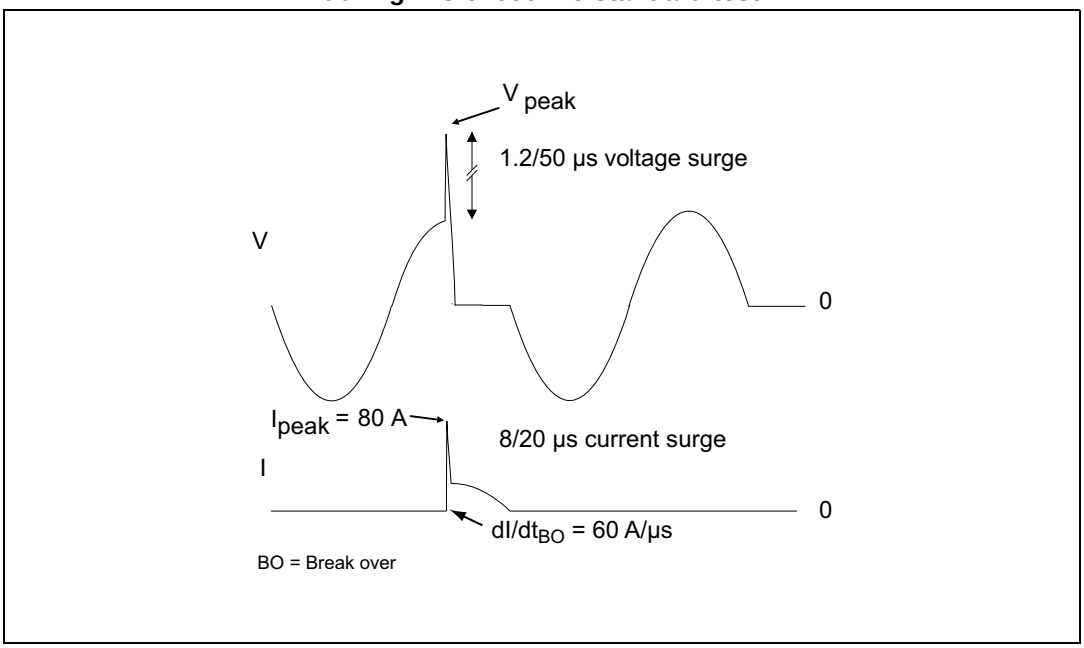


**Figure 18. Typical voltage and current waveforms across the ACST310-8B during IEC 61000-4-5 standard test**




## 2.3 Electrical noise immunity

The ACST310 is a sensitive device ($I_{GT}$ max. 10 mA) and can be controlled directly through a simple resistor by a logic level circuit, and still provides a high electrical noise immunity. The intrinsic immunity of the ACST310 is shown by the specified dV/dt equal to 1000 V/µs at 125 °C. This immunity level is 5 to 10 times higher than the immunity provided by an equivalent standard technology Triac with the same sensitivity. In other words, the ACST310 with $I_{GT}$ = 10 mA has immunity comparable only for higher gate current device ($I_{GT}$ higher than 35 mA).

# 3 Package information

- Epoxy meets UL94-V0
- Lead-free package
- Halogen free molding compound

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

## 3.1 DPAK package information

**Figure 19. DPAK package outline**

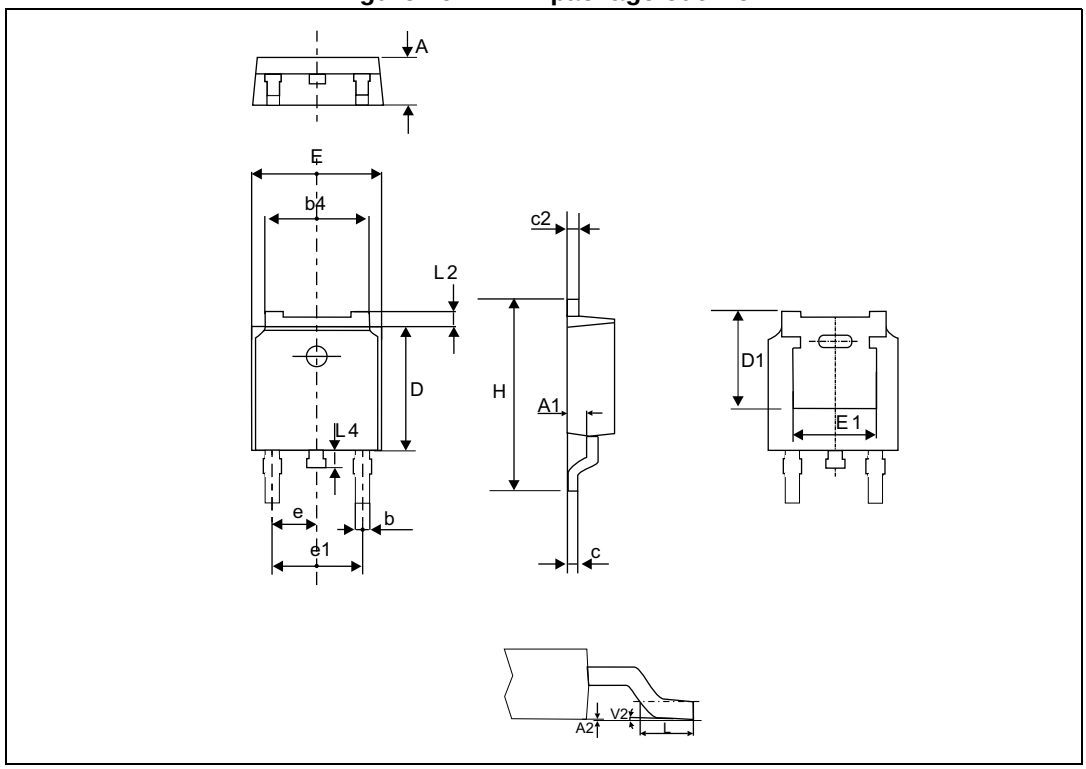
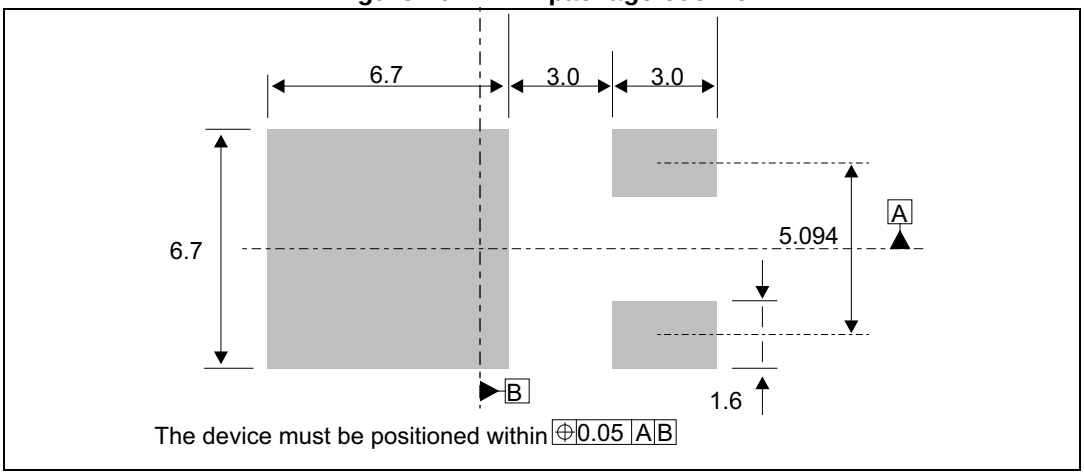


**Table 6. DPAK package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Typ. | Min. | Max. | Typ. | Min. | Max. |
| A | | 2.18 | 2.40 | | 0.0858 | 0.0945 |
| A1 | | 0.9 | 1.10 | | 0.0354 | 0.0433 |
| A2 | | 0.03 | 0.23 | | 0.0012 | 0.0091 |
| b | | 0.64 | 0.90 | | 0.0252 | 0.0354 |
| b4 | | 4.95 | 5.46 | | 0.1949 | 0.2150 |
| c | | 0.46 | 0.61 | | 0.0181 | 0.0240 |
| c2 | | 0.46 | 0.60 | | 0.0181 | 0.0236 |
| D | | 5.97 | 6.22 | | 0.2339 | 0.2449 |
| D1 | | 5.1 | | | 0.2008 | |
| E | | 6.35 | 6.73 | | 0.25 | 0.2650 |
| E1 | | 4.32 | | | 0.1701 | |
| e | 2.286 | | | 0.09 | | |
| e1 | 4.572 | | | 0.18 | | |
| H | | 9.35 | 10.40 | | 0.3681 | 0.4094 |
| L | | 1.0 | 1.78 | | 0.0394 | 0.0701 |
| L2 | | | 1.27 | | | 0.05 |
| L4 | | 0.6 | 1.02 | | 0.0236 | 0.0401 |
| V2 | | 0° | 8° | | 0° | 8° |

**Figure 20. DPAK package outline**



# 4 Ordering information

**Figure 21. Ordering information scheme**

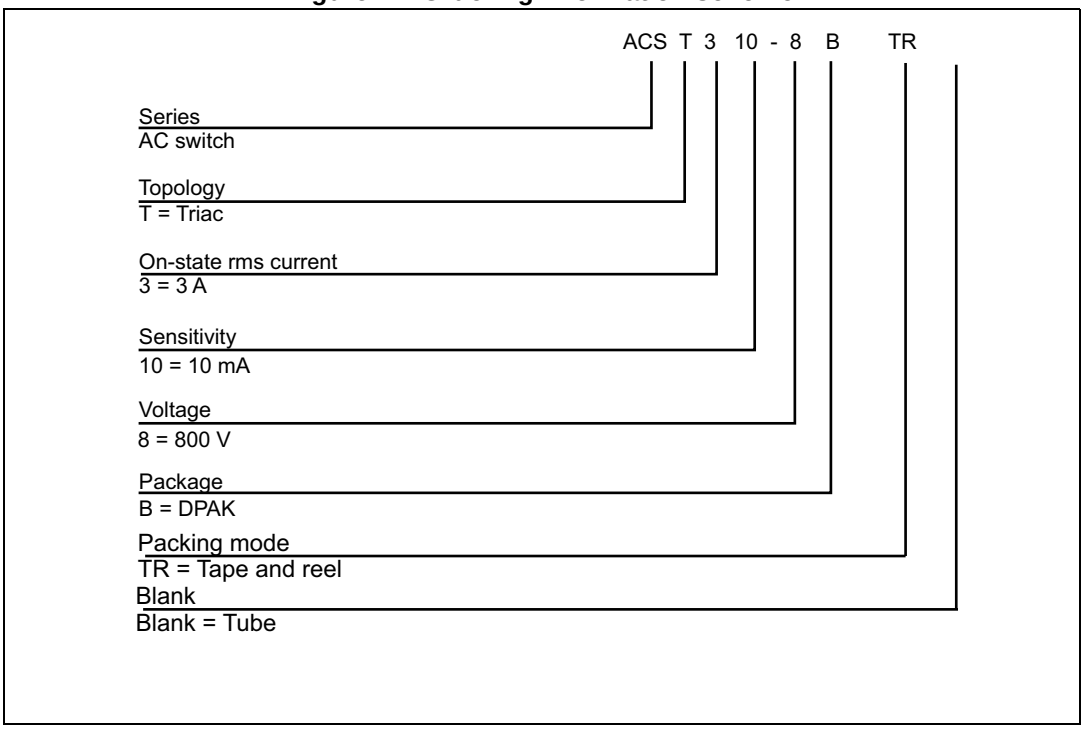



**Table 7. Ordering information**

| Order code | Marking | Package | Weight | Base qty. | Packing mode |
|---|---|---|---|---|---|
| ACST310-8B | ACST 3108 | DPAK | 0.32 g per pc. | 75 | Tube |
| ACST310-8BTR | | | | 2500 | Tape and reel |

# 5 Revision history

**Table 8. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 08-Jul-2015 | 1 | First issue. |