



# EMIF10-1K010F2

IPAD™

## EMI Filter including ESD protection

### Main product characteristics

Where EMI filtering in ESD sensitive equipment is required:

- Mobile Phones
- Computers and printers
- Communication systems
- MCU Boards

### Description

The EMIF10-1K010F2 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

Additionally, this filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

### Benefits

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Lead free package
- Very low PCB space consuming:  
2.42 mm x 2.42 mm
- Very thin package: 0.650 mm
- High efficiency in ESD suppression on both input and output pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging

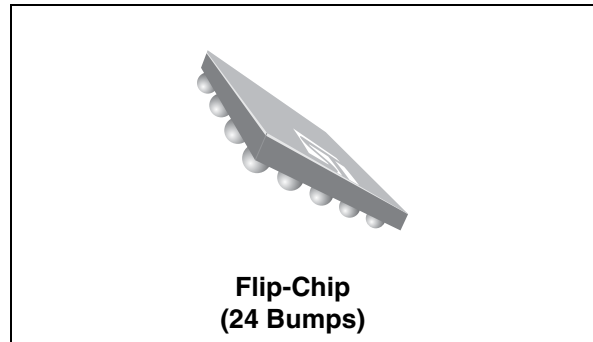
### Complies with the following standards:

#### IEC 61000-4-2 level 4

- 15 kV (air discharge)
- 8 kV (contact discharge)

#### MIL STD 883F - Method 3015.7 Class 3

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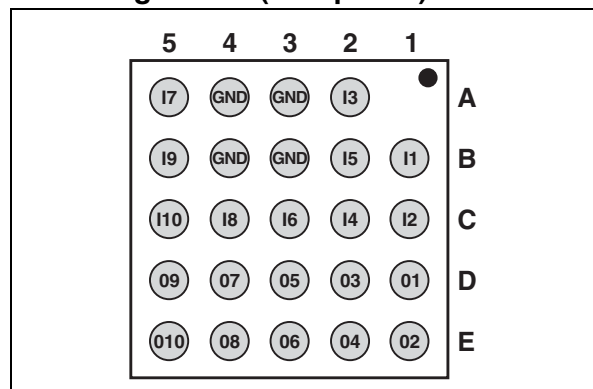


Flip-Chip  
(24 Bumps)

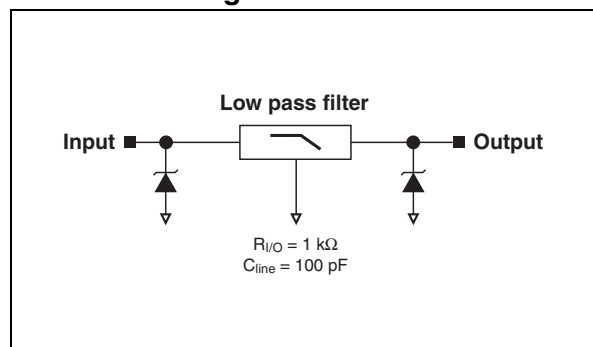
### Order code

Part Number	Marking
EMIF10-1K010F2	FD

### Pin configuration (Bump side)



### Basic cell configuration



# 1 Characteristics

**Table 1. Absolute Ratings ( $T_{amb} = 25^{\circ} C$ )**

Symbol	Parameter and test conditions	Value	Unit
$V_{PP}$	<b>ESD discharge IEC 61000-4-2</b>		
	– Air discharge	15	kV
	– Contact discharge	8	
<b>MIL STD 883F - Method 3015.7 Class 3</b>	25		
$T_j$	Junction temperature	125	$^{\circ}C$
$T_{op}$	Operating temperature range	- 40 to + 85	$^{\circ}C$
$T_{stg}$	Storage temperature range	- 55 to + 150	$^{\circ}C$

**Table 2. Electrical Characteristics ( $T_{amb} = 25^{\circ} C$ )**

Symbol	Parameter
$V_{BR}$	Breakdown voltage
$I_{RM}$	Leakage current @ $V_{RM}$
$V_{RM}$	Stand-off voltage
$V_{CL}$	Clamping voltage
$R_d$	Dynamic impedance
$I_{PP}$	Peak pulse current
$R_{I/O}$	Resistance between Input and Output
$C_{line}$	Input capacitance per line

Symbol	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR}$	$I_R = 1 \text{ mA}$	6	8	10	V
$I_{RM}$	$V_{RM} = 3 \text{ V per line}$			200	nA
$R_d$	$I_{PP} = 10 \text{ A}, t_p = 2.5 \mu\text{s}$		1		$\Omega$
$R_{I/O}$		900	1000	1100	$\Omega$
$C_{line}$	$F = 1 \text{ MHz } V_{OSC} = 30 \text{ mV } V_{line} = 0 \text{ V}$	80	100	120	pF

Figure 1. S21(db) attenuation measurement

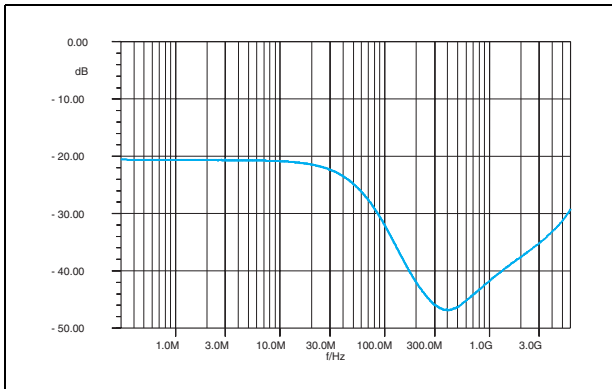


Figure 2. Analog cross talk measurements

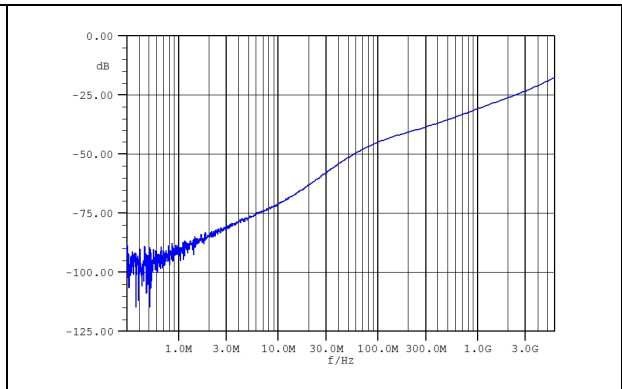


Figure 3. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V<sub>in</sub>) and on one output (V<sub>out</sub>)



Figure 4. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V<sub>in</sub>) and on one output (V<sub>out</sub>)

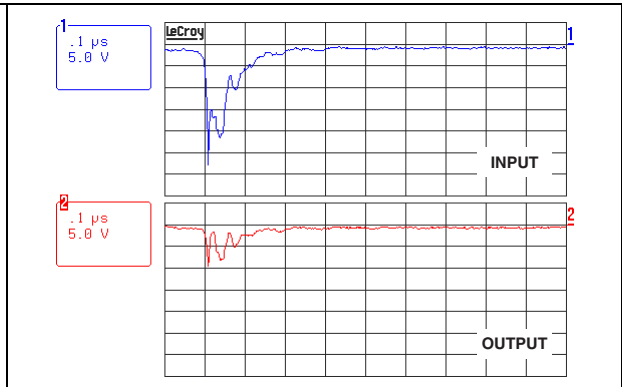


Figure 5. Capacitance versus reverse applied voltage

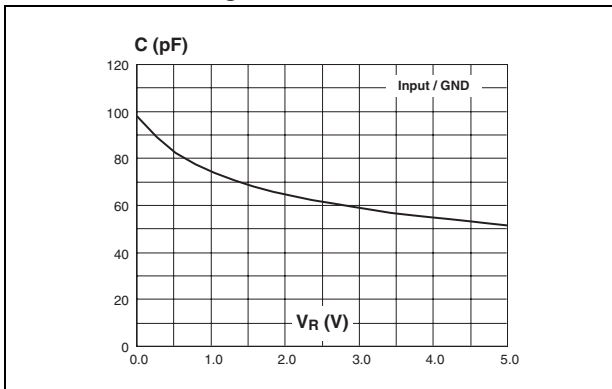


Figure 6. Aplac model

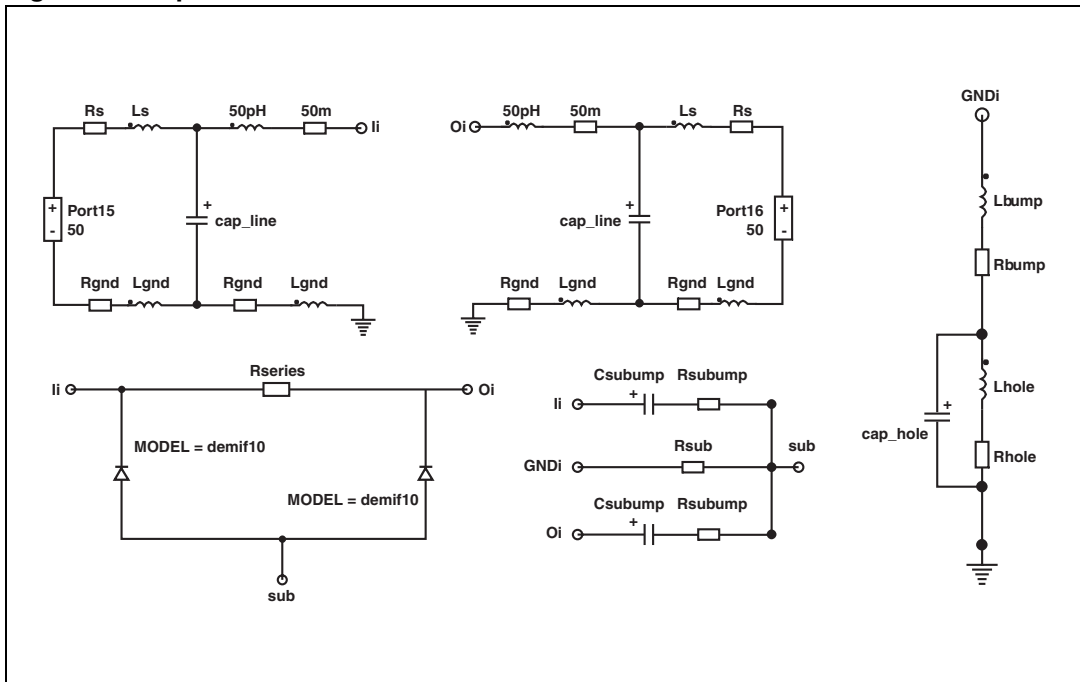
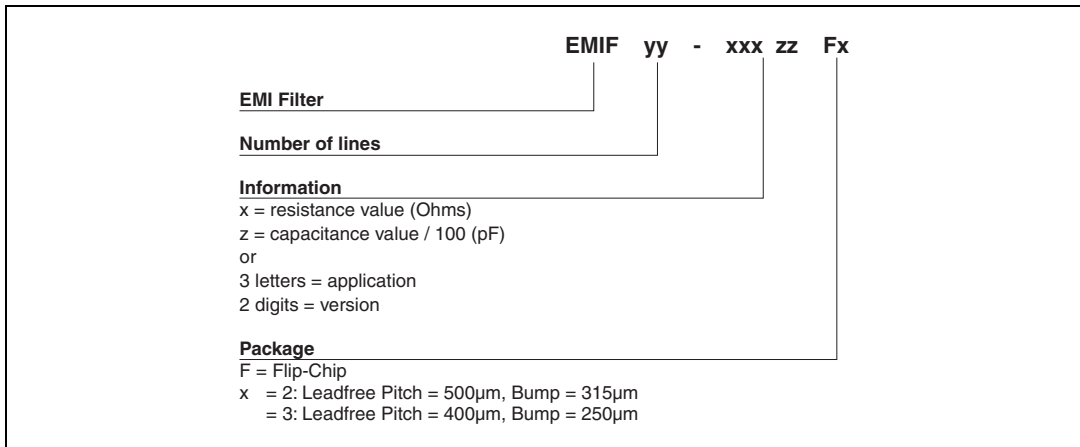


Figure 7. Aplac parameters

$C_z$	57pF	Model demif10
$R_{series}$	960	BV = 7
$cap\_line$	0.8pF	IBV = 1m
$L_s$	0.6nH	CJO = $C_z$
$R_{bump}$	50m	M = 0.3333
$L_{bump}$	50pH	$R_s = 1$
$R_s$	0.15	VJ = 0.6
$C_{subump}$	15pF	TT = 100n
$R_{subump}$	0.15	
$R_{sub}$	0.1	
$l_{hole}$	1.2nH opt	
$R_{hole}$	0.15	
$cap\_hole$	0.15pF	
$R_{gnd}$	0.25	
$l_{gnd}$	0.4nH	

## 2 Ordering Information Scheme



## 3 Package information

Figure 8. Flip-Chip package dimensions

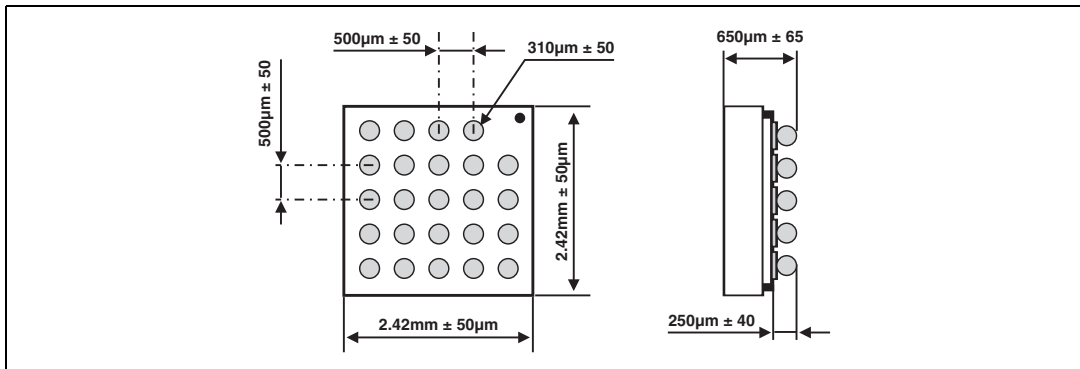
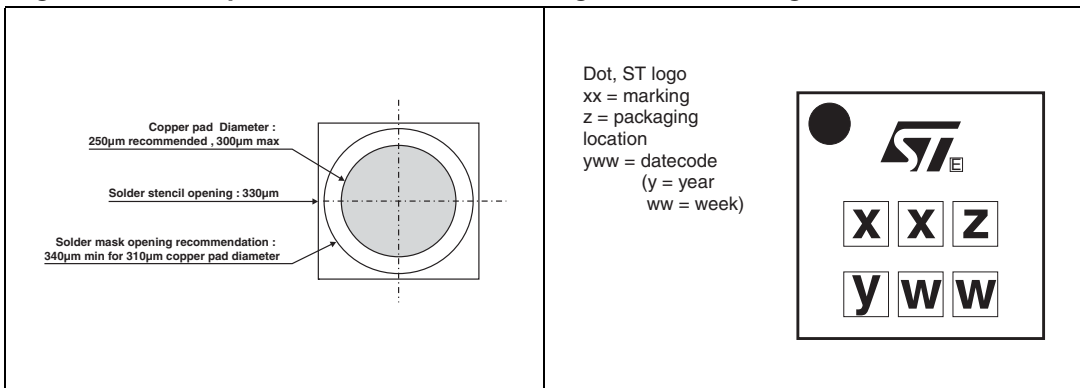


Figure 9. Foot print recommendations      Figure 10. Marking





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