



EMIF10-COM01F2

IPAD™

EMI Filter including ESD protection

Main product characteristics

EMI filtering and ESD protection for:

- Computers and printers
- Communication systems
- Mobile phones

Description

The EMIF10-COM01F2 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

Additionally, this filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

Benefits

- EMI symmetrical (I/O) low-pass filter
- Lead free package
- Very low PCB space consuming: < 6 mm²
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on both input & output pins
- High reliability offered by monolithic integration

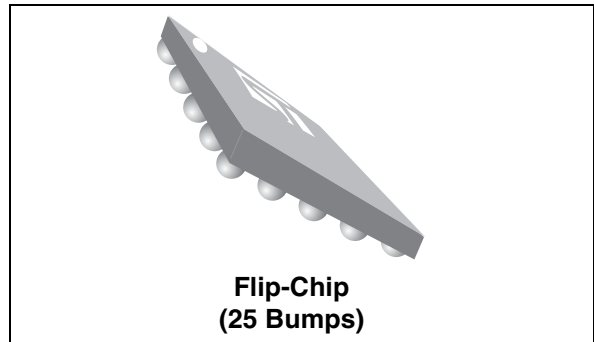
Complies with the following standards:

IEC 61000-4-2 level 4

15 kV (air discharge)

8 kV (contact discharge)

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Flip-Chip
(25 Bumps)

Order code

Part Number	Marking
EMIF10-COM01F2	FE

Figure 1. Pin configuration (Bump side)

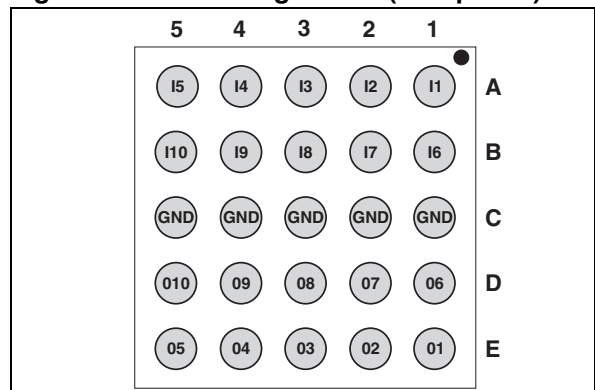
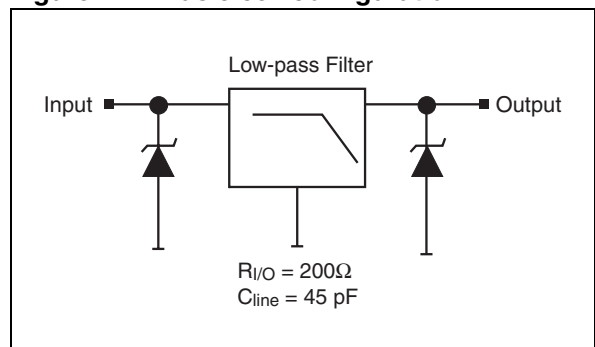


Figure 2. Basic cell configuration



1 Characteristics

Table 1. Absolute Ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2, air discharge	15	kV
	ESD discharge IEC61000-4-2, contact discharge	8	
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{op}	Operating temperature range	- 40 to + 85	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	- 55 to + 150	$^{\circ}\text{C}$

Table 2. Electrical Characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Resistance between Input and Output
C_{line}	Input capacitance per line

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	8	10	V
I_{RM}	$V_{RM} = 3\text{ V per line}$			500	nA
R_d	$I_{PP} = 10\text{ A}, t_p = 2.5\text{ }\mu\text{s}$		1		Ω
$R_{I/O}$		180	200	220	Ω
C_{line}	At 0 V bias		45	50	pF
t_{LH}	$V_{input} = 2.8\text{ V}$ $R_{load} = 100\text{ k}\Omega$			25	ns

Figure 3. S21(db) attenuation measurement⁽¹⁾

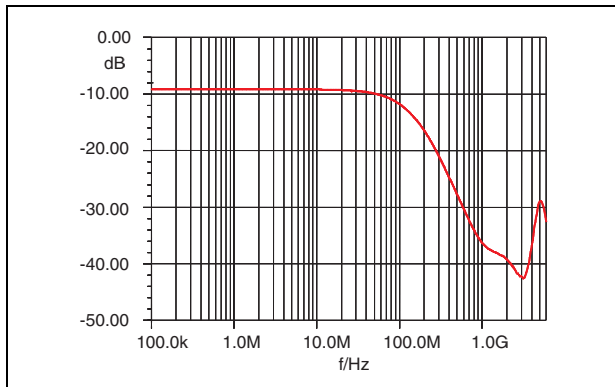
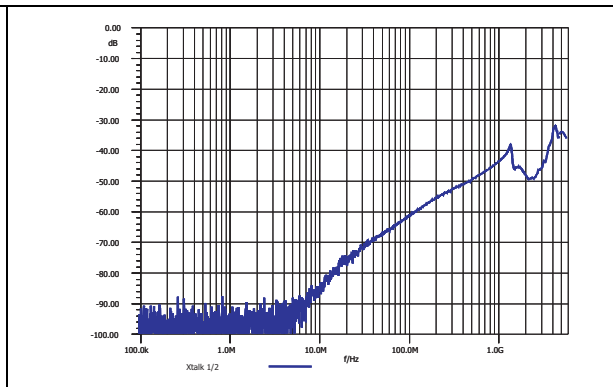


Figure 4. Analog crosstalk



1. Spikes at high frequencies are induced by the PCB layout

Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

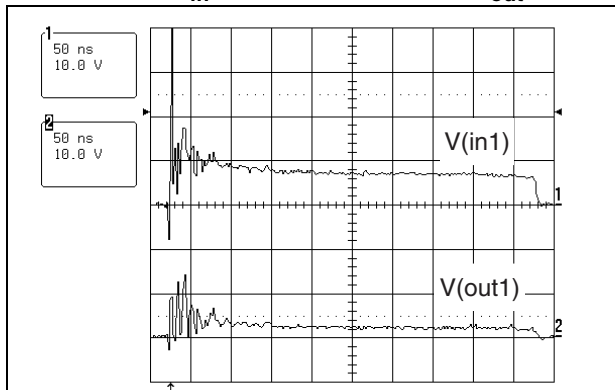


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

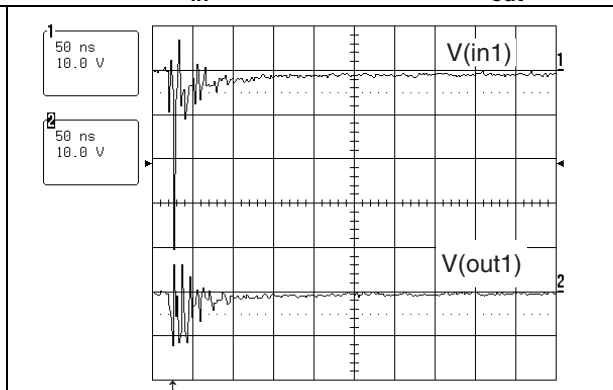


Figure 7. Rise time measurement

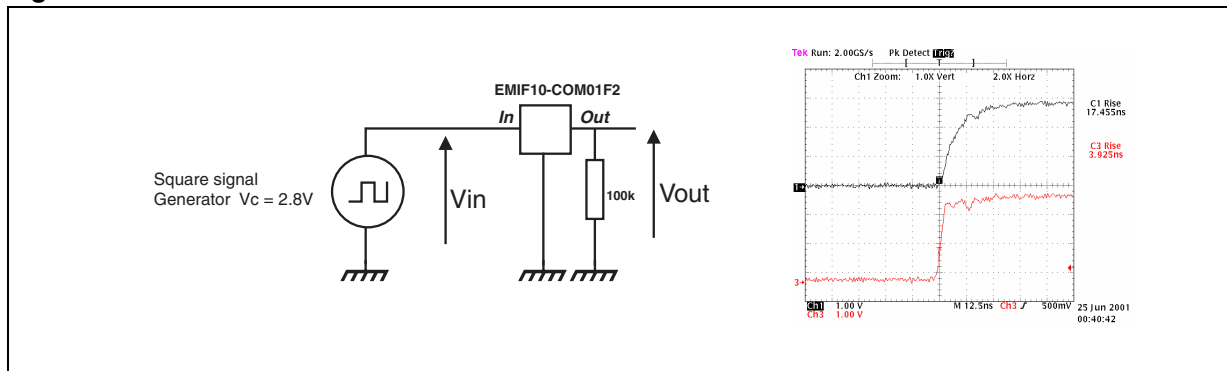


Figure 8. Capacitance versus reverse applied voltage

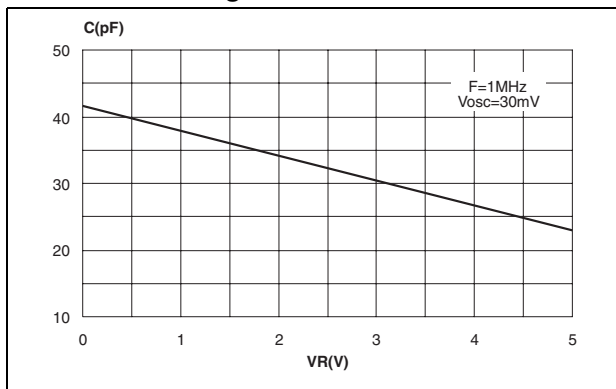
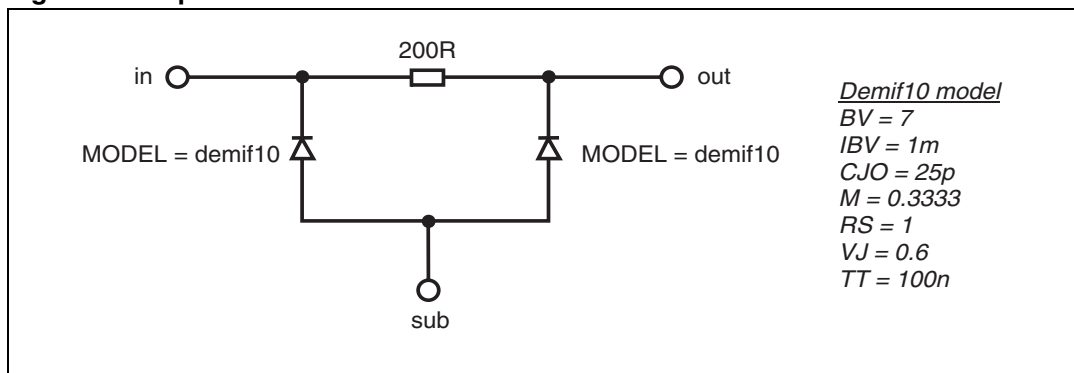


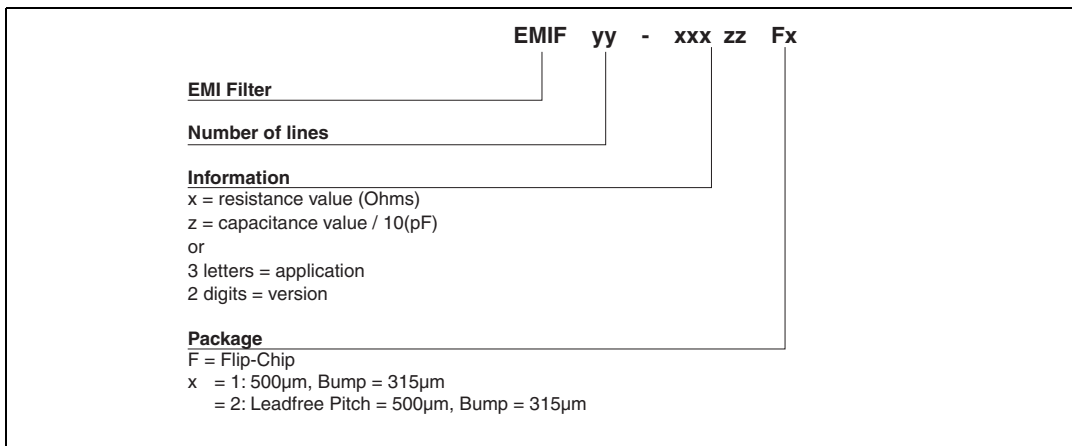
Figure 9. APlac model



1.1 PCB grounding recommendations

In order to ensure a good efficiency in terms of ESD protection and filtering behavior, we recommend to implement microvias (100 µm dia.) between the GND bumps and the GND layer. GND bumps can be connected together in PCB layer 1, and in addition, if possible, use through hole vias (200 µm dia.) in both sides of filter to improve contact to GND (layer). This layout will minimize the distance to the ground and thus parasitic inductances. In addition, we recommend to have GND plane wherever possible.

2 Ordering Information Scheme



3 Package information

Figure 10. Flip-Chip package dimensions

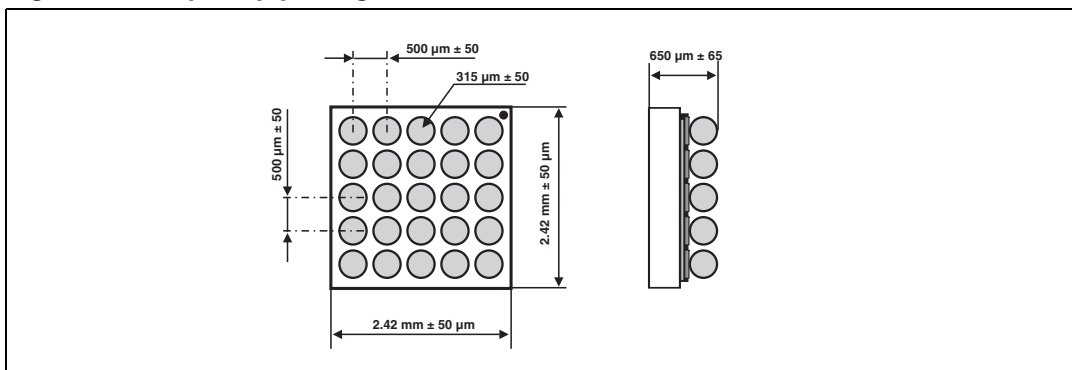
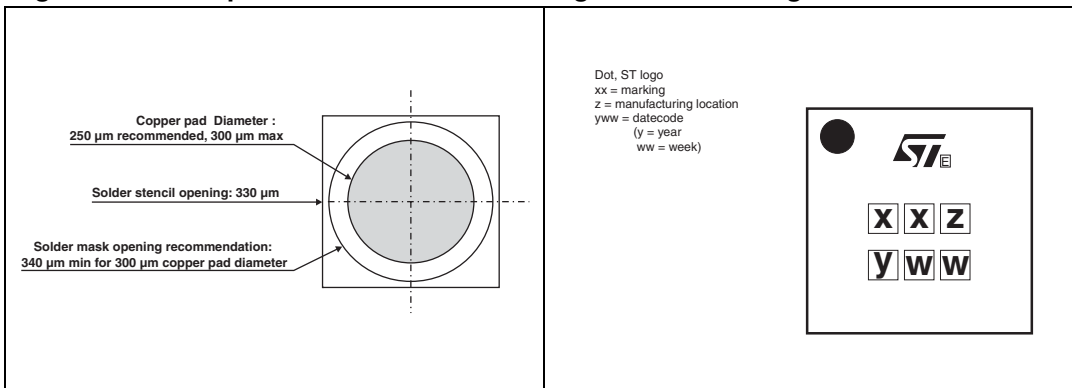


Figure 11. Foot print recommendations Figure 12. Marking



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