AN1762
APPLICATION NOTE

L6205, L6206, L6207 DUAL FULL BRIDGE DRIVERS

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Modern motion control applications need more flexibility that can be addressed only with specialized IC products. The L6205, L6206, L6207 are dual full bridge drivers ICs specifically developed to drive a wide range of motors. These ICs are one-chip cost effective solutions that include several unique circuit design features. These features allow the devices to be used in many applications including DC and stepper motor driving. The principal aim of this development project was to produce easy to use, fully protected power ICs. In addition several key functions such as protection circuit and PWM current control drastically reduce external components count to meet requirements for many different applications.

1 INTRODUCTION

The L6205, L6206, L6207 are highly integrated, mixed-signal power ICs that allow the user to easily design a control system for two-phase bipolar stepper motors, multiple DC motors and a wide range of inductive loads. Figure 1 to Figure 3 show the L6205, L6206, L6207 block diagrams. Each IC integrates eight Power DMOS plus other added features for safe operation and flexibility. The L6207 also features a constant t_{OFF} PWM current control technique (*Synchronous mode*) for each of the two full bridges.

Figure 1. L6205 block diagram.

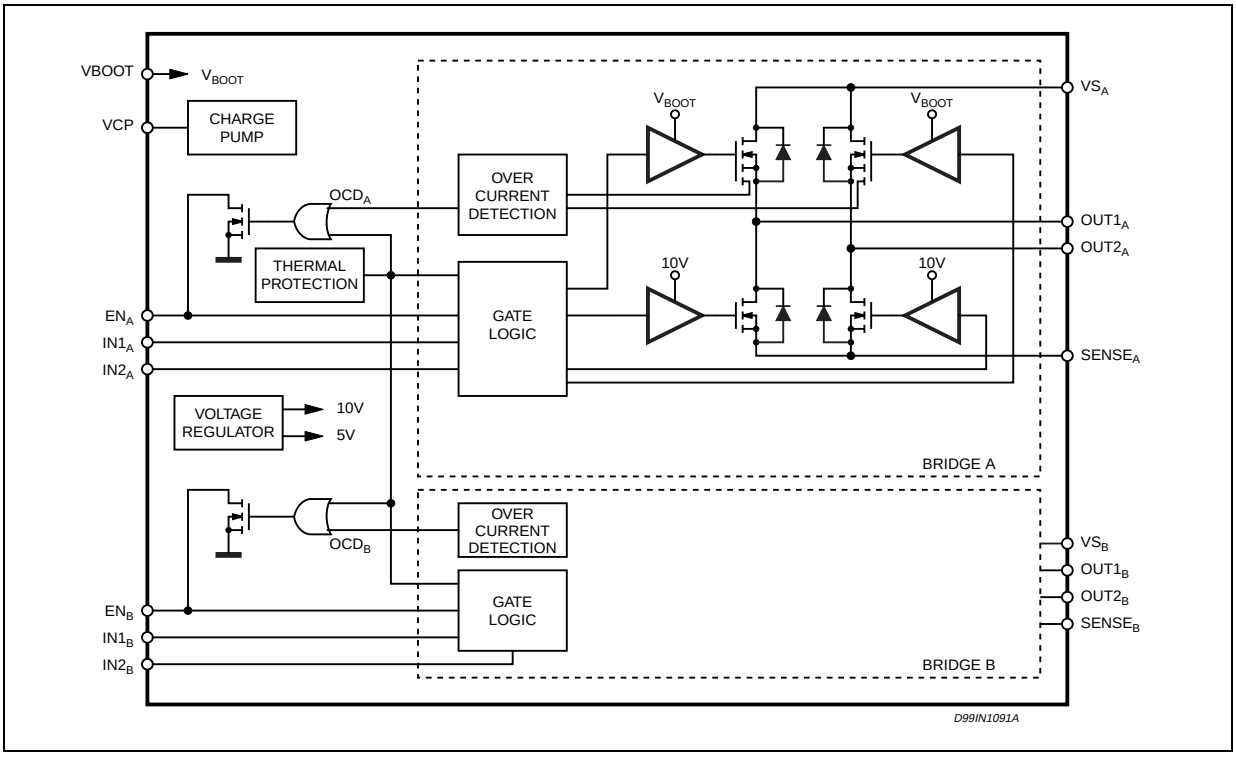


Figure 2. L6206 block diagram.

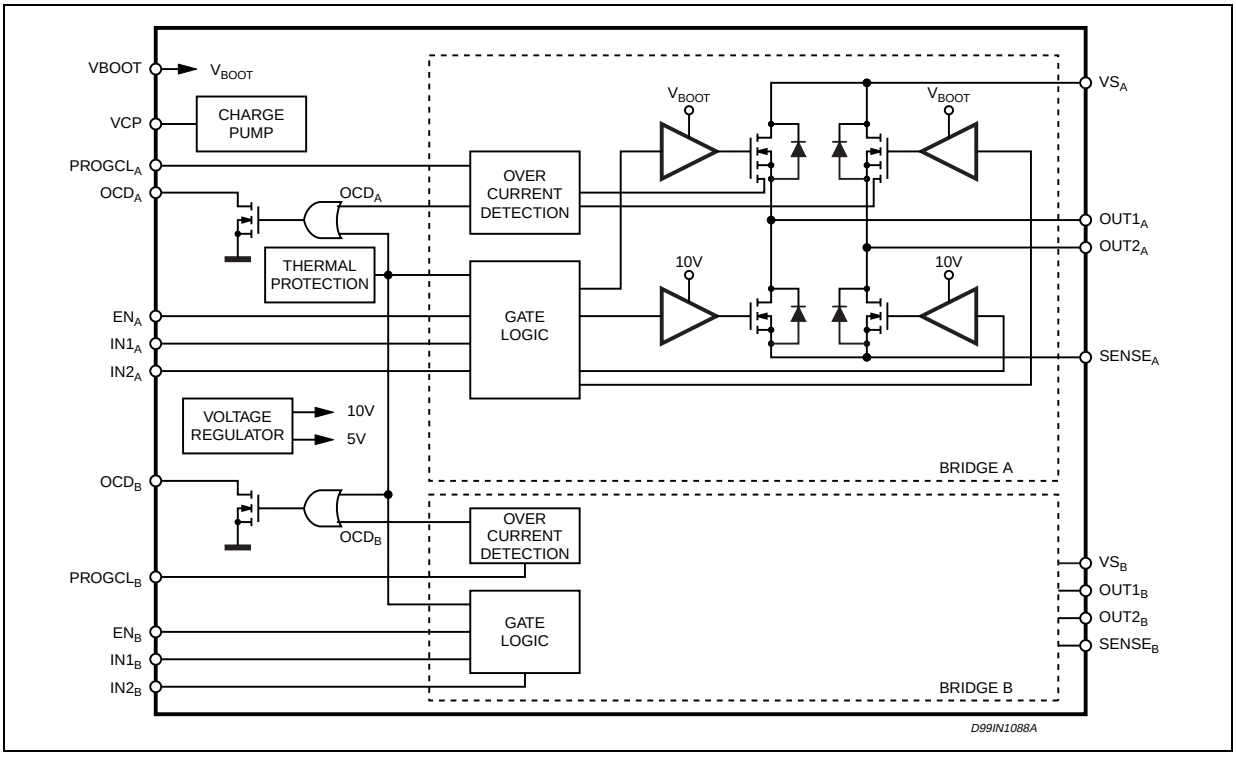
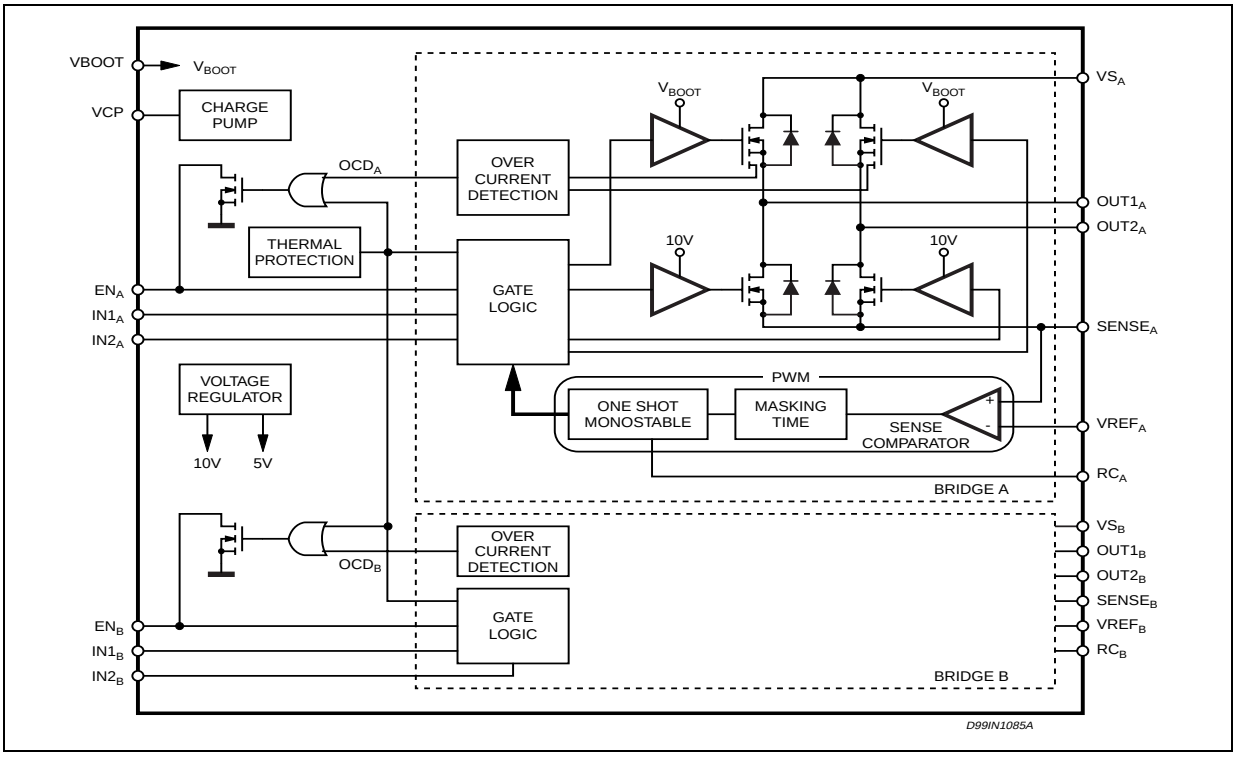


Figure 3. L6207 block diagram.



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2 MAIN DIFFERENCES BETWEEN L6205, L6206, L6207

L6205, L6206 and L6207 are DMOS Dual Full Bridge ICs.

L6205 (see Figure 1) includes logic for CMOS/TTL interface, a charge pump that provide auxiliary voltage to drive the high-side DMOS, non dissipative over current protection circuitry on the high-side DMOS, with fixed trip point set at 5.6 A (see *Over Current Protection* Section), over temperature protection, Under Voltage Lock-Out for reliable start-up.

In addition, L6206 gives the possibility of adjusting the trip point of the over current protection for each of the two full-bridges (through two external resistors), and its internal open-drain mosfets (see *Over Current Protection* Section) are not internally connected to *EN* pins but to separate *OCD* pins, allowing easier external diagnostics and overcurrent management.

L6207 has Over Current protection function with fixed trip point set at 5.6 A and internal open-drain mosfets connected to *EN* pins, as the L6205, but it also integrates two PWM current controller for each of the two full-bridges (see *Programmable off-time Monostable* section).

3 DESIGNING AN APPLICATION WITH L6205, L6206, L6207

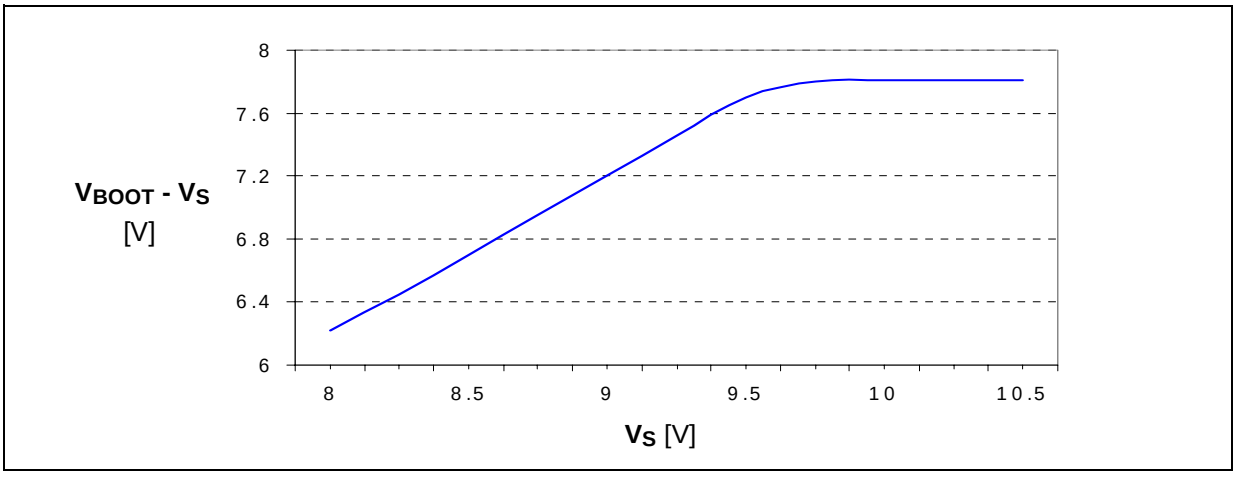
3.1 Current Ratings

With MOSFET (DMOS) devices, unlike bipolar transistors, current under short circuit conditions is, at first approximation, limited by the $R_{DS(ON)}$ of the DMOS themselves and could reach very high values. L6205, L6206, L6207 *Out* pins and the two V_{SA} and V_{SB} pins are rated for a maximum of 2.8A r.m.s. and 5.6A peak (typical values), corresponding to a total (for the whole IC) 5.6A rms (11.2A peak). These values are meant to avoid damaging metal structures, including the metallization on the die and bond wires. In practical applications, though, maximum allowable current is less than these values, due to power dissipation limits (see *Power Management* section). The devices have a built-in Over Current Detection (OCD) that provides protection against short circuits between the outputs and between an output and ground (see *Over Current Protection* section).

3.2 Voltage Ratings and Operating Range

The L6205, L6206, L6207 requires a single supply voltage (V_S), for the motor supply. Internal voltage regulators provide the 5V and 10V required for the internal circuitry. The operating range for V_S is 8 to 52V. To prevent working into undesirable low supply voltage an *Under Voltage Lock Out* (**UVLO**) circuit shuts down the device when supply voltage falls below 6V; to resume normal operating conditions, V_S must then exceed 7V. The hysteresis is provided to avoid false intervention of the UVLO function during fast V_S ringings. It should be noted, however, that DMOS's $R_{DS(ON)}$ is a function of the V_S supply voltage. Actually, when V_S is less than 10V, $R_{DS(ON)}$ is adversely affected, and this is particularly true for the High Side DMOS that are driven from V_{BOOT} supply. This supply is obtained through a charge pump from the internal 10V supply, which will tend to reduce its output voltage when V_S goes below 10V. Figure 4 shows the supply voltage of the high side gate drivers (V_{BOOT} - V_S) versus the supply voltage (V_S).

Figure 4. High side gate drivers supply voltage versus supply voltage.



Note that V_S must be connected to both V_{SA} and V_{SB} since the bootstrap voltage (at V_{BOOT} pin) is the same for the two H-bridges. The integrated DMOS have a rated Drain-Source breakdown voltage of 60V. However V_S should be kept below 52V, since in normal working conditions the DMOS see a V_{ds} voltage that will exceed V_S supply. In particular, during a phase change (when each output of the same H-bridge switches from V_S to GND or vice versa, for example to reverse the current in the load) at the beginning of the dead-time (when all the DMOS are off) the *SENSE* pin sees a negative spike due to a not negligible parasitic inductance of the PCB path from the pin to GND. This spike is followed by a stable negative voltage due to the drop on R_{SENSE}. One of the two *OUT* pins of the bridge sees a similar behavior, but with a slightly larger voltage due to the forward recovery time of the integrated freewheeling diode and the forward voltage drop across it (see Figure 5). Typical duration of this spike is 30ns. At the same time, the other *OUT* pin of the same bridge sees a voltage above V_S, due to the PCB inductance and voltage drop across the high-side (integrated) freewheeling diode, as the current reverses direction and flows into the bulk capacitor. It turns out that the highest differential voltage can be observed between the two *OUT* pins of the same bridge, during the dead-time at a phase change, and this must always be kept below 60V [3].

Figure 5. Currents and voltages during the *dead time* at a phase change.

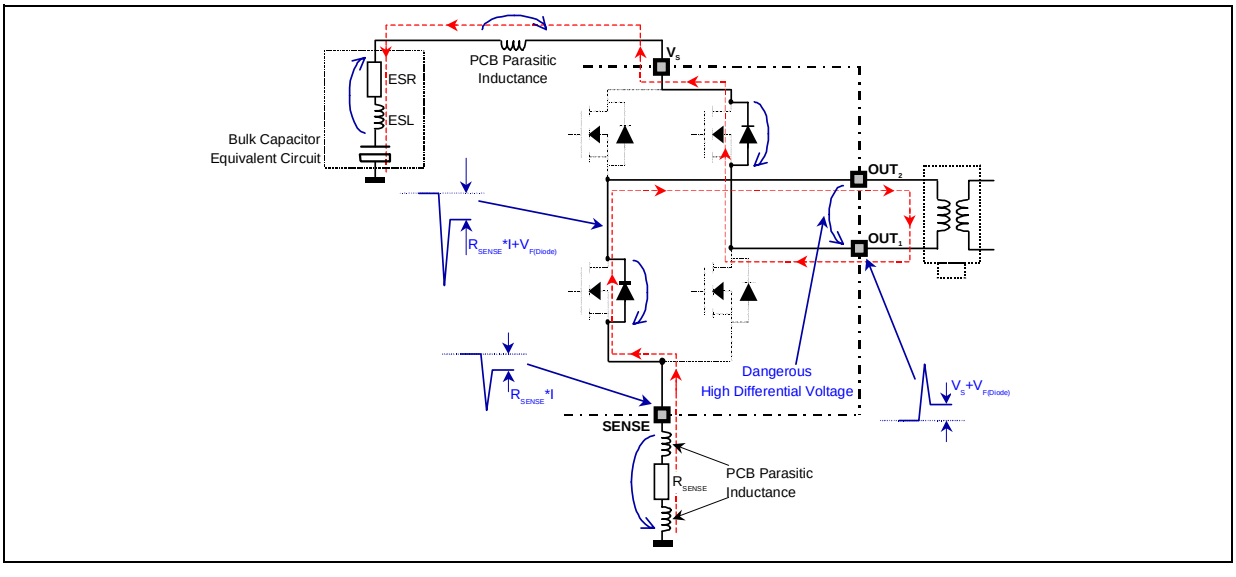
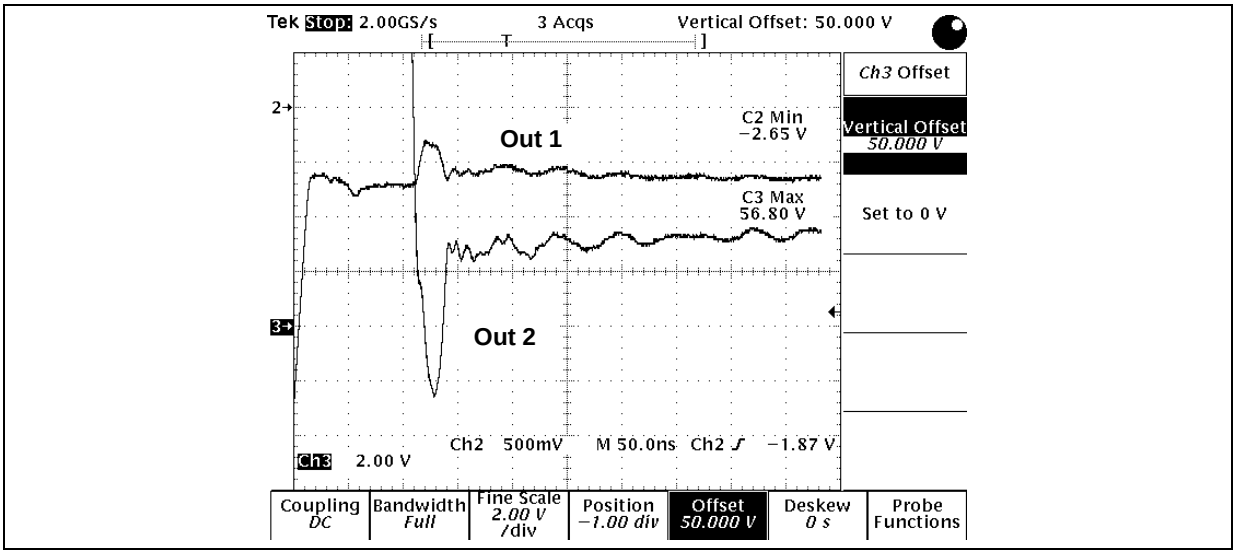


Figure 6 shows the voltage waveforms at the two OUT pins referring to a possible practical situation, with a peak output current of 2.8A, V_S = 52V, R_{SENSE} = 0.33Ω, T_J = 25°C (approximately) and a good PCB layout. Below ground spike amplitude is -2.65V for one output; the other *OUT* pin is at about 57V. In these conditions, total differential voltage reaches almost 60V, which is the absolute maximum rating for the DMOS. Keeping differential voltage between two Output pins belonging to the same Full Bridge within rated values is a must that can be accomplished with proper selection of Bulk capacitor value and equivalent series resistance (ESR), according to current peaks and chopping style and adopting good layout practices to minimize PCB parasitic inductances (see below) [3].

Figure 6. Voltage at the two outputs during the *dead time* at a phase change.



3.3 Choosing the Bulk Capacitor

Since the bulk capacitor, placed between V_S and *GND* pins, is charged and discharged during IC operation, its **AC current capability** must be greater than the r.m.s. value of the charge/discharge current. In the case of a PWM current regulation, the current flows from the capacitor to the IC during the on-time (t_{ON}) and from the IC (implementing a fast decay current recirculation technique) or from the power supply (implementing a slow decay current recirculation technique) to the capacitor during the off-time (t_{OFF}). The r.m.s. value of the current flowing into the bulk capacitor depends on peak output current, output current ripple, switching frequency, duty-cycle and chopping style. It also depends on power supply characteristics. A power supply with poor high frequency performances (or long, inductive connections to the IC) will cause the bulk capacitor to be recharged slowly: the higher the current control switching frequency, the higher the current ripple in the capacitor; r.m.s. current in the capacitor, however, does not exceed the r.m.s. output current. Bulk capacitor value (*C*) and the **ESR** determine the amount of voltage ripple on the capacitor itself and on the IC. In slow decay, neglecting the *dead-time* and output current ripple, and assuming that during the *on-time* the capacitor is not recharged by the power supply, the voltage at the end of the *on-time* is:

$$V_S - I_{OUT} \cdot \left(ESR + \frac{t_{ON}}{C} \right),$$

so the supply voltage ripple is:

$$I_{OUT} \cdot \left(ESR + \frac{t_{ON}}{C} \right),$$

where I_{OUT} is the output current. With fast decay, instead, recirculating current recharges the capacitor, causing the supply voltage to exceed the nominal voltage. This can be very dangerous if the nominal supply voltage is close to the maximum recommended supply voltage (52V). In fast decay the supply voltage ripple is about:

$$I_{OUT} \cdot \left(2 \cdot ESR + \frac{t_{ON} + t_{OFF}}{C}\right),$$

always assuming that the power supply does not recharge the capacitor, and neglecting the output current ripple and the dead-time. Usually (if C > 100 µF) the capacitance role is much less than the ESR, then supply voltage ripple can be estimated as:

$$I_{OUT} \cdot ESR \text{ in slow decay}$$

$$2 \cdot I_{OUT} \cdot ESR \text{ in fast decay}$$

For Example, if a maximum ripple of 500mV is allowed and I_{OUT} = 2A, the capacitor ESR should be lower than:

$$ESR < \frac{0.5V}{2A} = 250m\Omega \text{ in slow decay, and}$$

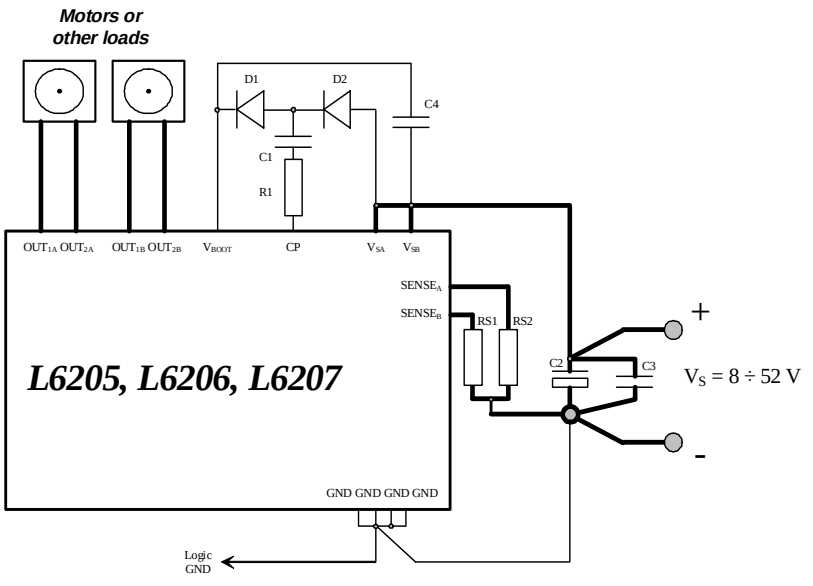
$$ESR < \frac{1}{2} \cdot \frac{0.5V}{2A} = 125m\Omega \text{ in fast decay.}$$

Actually, current sunk by V_{SA} and V_{SB} pins of the device is subject to higher peaks due to reverse recovery charge of internal freewheeling diodes. Duration of these peaks is, tough, very short, and can be filtered using a small value (100÷200 nF), good quality ceramic capacitor, connected as close as possible to the V_{SA}, V_{SB} and GND pins of the IC. Bulk capacitor will be chosen with **maximum operating voltage** 25% greater than the maximum supply voltage, considering also power supply tolerances. For example, with a 48V nominal power supply, with 5% tolerance, maximum voltage is 50.4V, then operating voltage for the capacitor should be at least 63V.

3.4 Layout Considerations

Working with devices that combine high power switches and control logic in the same IC, careful attention has to be paid to the PCB layout. In extreme cases, Power DMOS commutation can induce noises that could cause improper operation in the logic section of the device. Noise can be radiated by high dv/dt nodes or high di/dt paths, or conducted through GND or Supply connections. Logic connections, especially high-impedance nodes (actually all logic inputs, see further), must be kept far from switching nodes and paths. With the L6205, L6206, L6207, in particular, external components for the charge pump circuitry should be connected together through short paths, since these components are subject to voltage and current switching at relatively high frequency (600kHz). Primary mean in minimizing conducted noise is working on a good GND layout (see Figure 7).

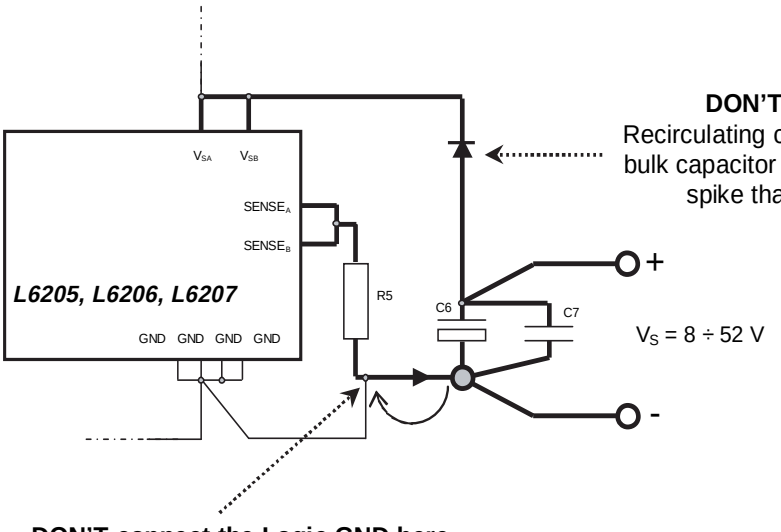
Figure 7. Typical Application and Layout suggestions.



High current GND tracks (i.e. the tracks connected to the sensing resistors) must be connected directly to the negative terminal of the bulk capacitor. A good quality, high-frequency bypass capacitor is also required (typically a 100nF÷200nF ceramic would suffice), since electrolytic capacitors show a poor high frequency performance. Both bulk electrolytic and high frequency bypass capacitors have to be connected with short tracks to V_{SA}, V_{SB} and GND. On the L6205, L6206, L6207 GND pins are the *Logic* GND, since only the quiescent current flows through them. Logic GND and Power GND should be connected together in a *single point*, the bulk capacitor, to keep noise in the Power GND from affecting Logic GND. Specific care should be paid layouting the path from the *SENSE* pins through the sensing resistors to the negative terminal of the bulk capacitor (Power Ground). These tracks must be as short as possible in order to minimize parasitic inductances that can cause dangerous voltage spikes on *SENSE* and *OUT* pins (see the *Voltage Ratings and Operating Range* section); for the same reason the capacitors on V_{SA}, V_{SB} and GND should be very close to the GND and supply pins. Refer to the Sensing Resistors section for information on selecting the sense resistors. Traces that connect to V_{SA}, V_{SB}, $SENSE_A$, $SENSE_B$, and the four *OUT* pins must be designed with adequate width, since high currents are flowing through these traces, and layer changes should be avoided. Should a layer change prove necessary, multiple and large via holes have to be used. A wide GND copper area can be used to improve power dissipation for the device.

Figure 8 shows two typical situations that must be avoided. An important consideration about the location of the bulk capacitors is the ability to absorb the inductive energy from the load, without allowing the supply voltage to exceed the maximum rating. The diode shown in Figure 8 prevents the recirculation current from reaching the capacitors and will result in a high voltage on the IC pins that can destroy the device. Having a switch or a power connection that can disconnect the capacitors from the IC, while there is still current in the motor, will also result in a high voltage transient since there is no capacitance to absorb the recirculation current.

Figure 8. Two situations that must be avoided.



3.5 Sensing Resistors

Each motor winding current is flowing through the corresponding sensing resistor, causing a voltage drop that can be used, by the logic (integrated in the L6207; an external logic can be used with L6205 and L6206), to control the peak value of the load current. Two issues must be taken into account when choosing the R_{SENSE} value:

– The sensing resistor dissipates energy and provides dangerous negative voltages on the *SENSE* pin during the current recirculation. For this reason the resistance of this component should be kept low.

– The voltage drop across R_{SENSE} is compared with a reference voltage (on V_{ref} pin) by the internal comparator (L6207 only). The lower is the R_{SENSE} value, the higher is the peak current error due to noise on Vref pin and to the input offset of the current sense comparator: too small values of R_{SENSE} must be avoided.

A good compromise is calculating the sensing resistor value so that the voltage drop, corresponding to the peak current in the load (I_{peak}), is about 0.5 V: $R_{SENSE} = 0.5\ V / I_{peak}$.

It should be clear that sensing resistor must absolutely be non-inductive type in order to avoid dangerous negative spikes on *SENSE* pins. Wire-wounded resistors cannot be used here, while Metallic film resistors are recommended for their high peak current capability and low inductance. For the same reason the connections between the *SENSE* pins, C6, C7, V_{SA}, V_{SB} and *GND* pins (see Figure 7) must be taken as short as possible (see also the *Layout Considerations* section).

The average power dissipated by the sensing resistor is:

Fast Decay Recirculation: $P_R \approx I_{rms}^2 \cdot R_{SENSE}$

Slow Decay Recirculation: $P_R \approx I_{rms}^2 \cdot R_{SENSE} \cdot D$,

D is the duty-cycle of the PWM current control, I_{rms} is the r.m.s. value of the load current.

Nevertheless, sensing resistor power rating should be chosen taking into account the peak value of the dissipated power:

$$P_R \approx I_{pk}^2 \cdot R_{SENSE} \quad ,$$

where I_{pk} is the peak value of the load current.

Using multiple resistors in parallel will help obtaining the required power rating with standard resistors, and reduce the inductance.

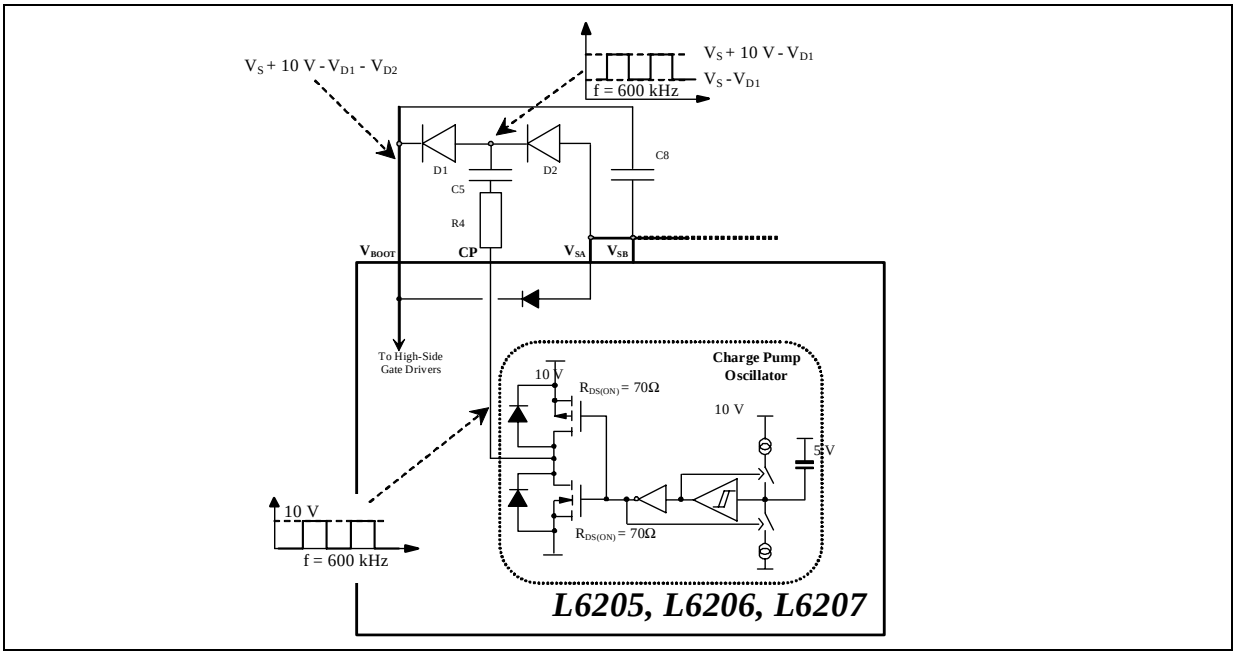
R_{SENSE} tolerance reflects on the peak current error: 1% resistors should be preferred.
The following table shows R_{SENSE} recommended values (to have 0.5V drop on it) and power ratings for typical examples of current peak values.

I_{pk}	R_{SENSE} Value [Ω]	R_{SENSE} Power Rating [W]	Alternatives
0.5	1	0.25	
1	0.5	0.5	2 X 1Ω, 0.25W paralleled
1.5	0.33	0.75	3 X 1Ω, 0.25W paralleled
2	0.25	1	4 X 1Ω, 0.25W paralleled

3.6 Charge pump external components

An internal oscillator, with its output at *CP* pin, switches from GND to 10V with a typical frequency of 600kHz (see Figure 9).

Figure 9. Charge Pump.



When the oscillator output is at ground, C_5 is charged by V_S through D_2. When it rises to 10V, D_2 is reverse biased and the charge flows from C_5 to C_8 through D_1, so the V_{BOOT} pin, after a few cycles, reaches the maximum voltage of V_S + 10V - V_{D1} - V_{D2}, which supplies the high-side gate drivers.

With a differential voltage between V_S and V_{BOOT} of about 9V and both the bridges switching at 50kHz, the typical current drawn by the V_{BOOT} pin is 1.85 mA.

Resistor *R4* is added to reduce the maximum current in the external components and to reduce the slew rate of the rising and falling edges of the voltage at the *CP* pin, in order to minimize interferences with the rest of the circuit. For the same reason care must be taken in realizing the PCB layout of *R4*, *C5*, *D1*, *D2* connections (see also the *Layout Considerations* section). Recommended values for the charge pump circuitry are:

D1, D2 : 1N4148

R4 : 100 Ω (1/8 W)

C5 : 10nF 100V ceramic

C8 : 220nF 25V ceramic

Due to the high charge pump frequency, fast diodes are required. Connecting the cold side of the bulk capacitor (C8) to V_S instead of GND the average current in the external diodes during operation is less than 10 mA (with R4 = 100 Ω); at startup (when V_S is provided to the IC) is less than 200 mA while the reverse voltage is about 10 V in all conditions. 1N4148 diodes withstand about 200 mA DC (1 A peak), and the maximum reverse voltage is 75 V, so they should fit for the majority of applications.

3.7 Sharing the Charge Pump Circuitry

If more than one device is used in the application, it's possible to use the charge pump from one L6205, L6206 or L6207 to supply the V_{BOOT} pins of several ICs. The unused *CP* pins on the slaved devices are left unconnected, as shown in Figure 10. A 100nF capacitor (C8) should be connected to the V_{BOOT} pin of each device. Supply voltage pins (V_S) of the devices sharing the charge pump must be connected together.

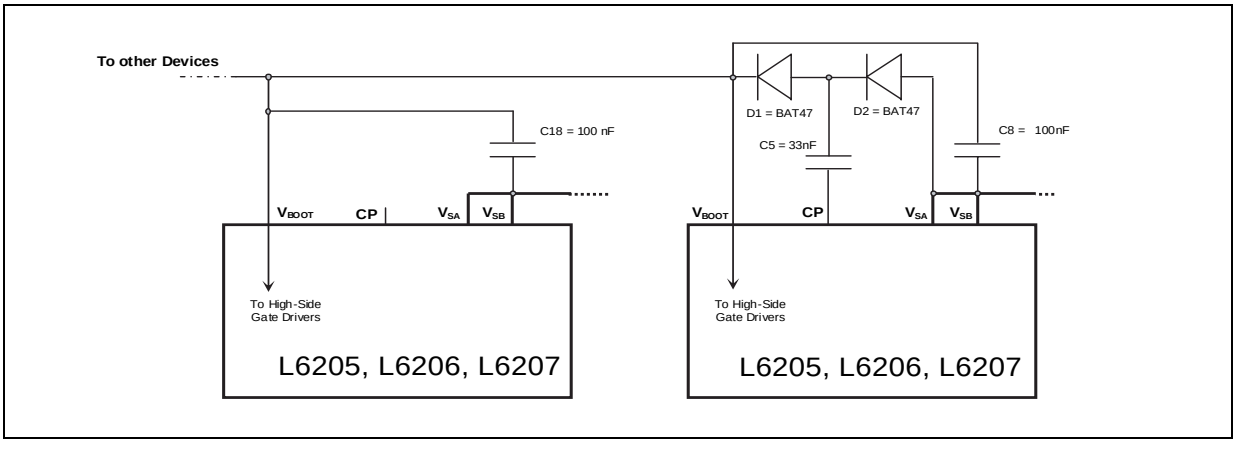
The higher the number of devices sharing the same charge pump, the lower will be the differential voltage available for gate drive (V_{BOOT} - V_S), causing a higher $R_{DS(ON)}$ for the high side DMOS, so higher dissipating power.

In this case it's recommended to omit the resistor on the *CP* pin, obtaining a higher current capability of the charge pump circuitry.

Better performance can also be obtained using a 33nF capacitor for C5 and using schottky diodes (for example BAT47 are recommended).

Sharing the same charge pump circuitry for more than 3÷4 devices is not recommended, since it will reduce the V_{BOOT} voltage increasing the high-side MOS on-resistance and thus power dissipation.

Figure 10. Sharing the charge pump circuitry.



3.8 Reference Voltage for PWM Current Control (L6207 ONLY)

The L6207 has two analog inputs, V_{refA} and V_{refB}, connected to the internal sense comparators, to control the peak value of the motor current through the integrated PWM circuitry. In typical applications these pins are connected together, in order to obtain the same current in the two motor windings. A fixed reference voltage can be easily obtained through a resistive divider from an available 5 V voltage rail (maybe the one supplying the µC or the rest of the application) and GND.

A very simple way to obtain a variable voltage without using a DAC is to low-pass filter a PWM output of a µC (see Figure 11).

Assuming that the PWM output swings from 0 to 5V, the resulting voltage will be:

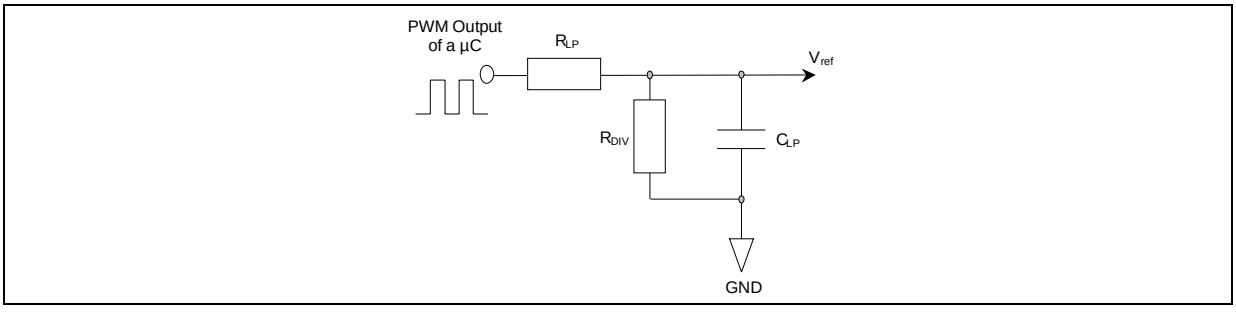
$$V_{ref} = \frac{5V \cdot D_{\mu C} \cdot R_{DIV}}{R_{LP} + R_{DIV}}$$

where $D_{\mu C}$ is the duty-cycle of the PWM output of the µC.

Assuming that the µC output impedance is lower than 1kΩ, with R_{LP} = 56kΩ, R_{DIV} = 15kΩ, C_{LP} = 10nF and a µC PWM switching from 0 to 5V at 100kHz, the low pass filter time constant is about 0.12 ms and the remaining ripple on the V_{ref} voltage will be about 20 mV. Using higher values for R_{LP}, R_{DIV} and C_{LP} will reduce the ripple, but the reference voltage will take more time to vary after changing the duty-cycle of the µC PWM, and too high values of R_{LP} will also increase the impedance of the V_{ref} net at low frequencies, causing a poor noise immunity.

As sensing resistor values are typically kept small, a small noise on V_{ref} input pins might cause a considerable error in the output current. It's then recommended to decouple these pins with ceramic capacitors of some tens of nF, placed very close to V_{ref} and GND pins. Note that V_{ref} pins cannot be left unconnected, while, if connected to GND, zero current is not guaranteed due to voltage offset in the sense comparator. The best way to cut down (IC) power consumption and clear the load current is pulling down the *EN* pins. With very small reference voltage, PWM integrated circuitry can loose control of the current due to the minimum allowed duration of t_{ON} (see the *Programmable off-time Monostable* section).

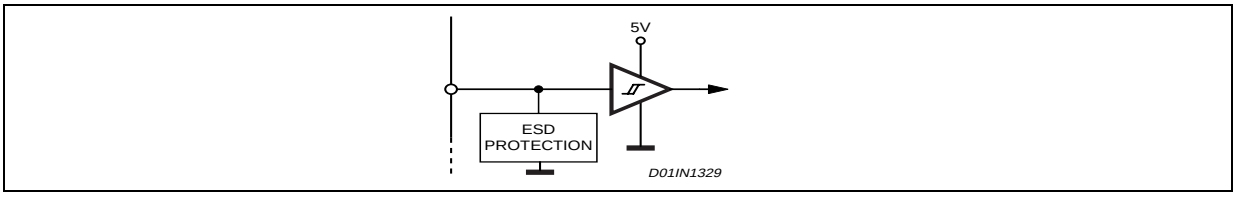
Figure 11. Obtaining a variable voltage through a PWM output of a µC.



3.9 Input Logic pins

IN1$_A$, IN2$_A$, IN1$_B$, IN2$_B$ are CMOS/TTL compatible logic input pins. The input comparator has been realized with hysteresis to ensure the required noise immunity. Typical values for turn-on and turn-off thresholds are $V_{th,ON}$ = 1.8V and $V_{th,OFF}$ = 1.3V. Pins are ESD protected (see Figure 12) (2kV human-body electro-static discharge), and can be directly connected to the logic outputs of a µC; a series resistor is generally not recommended, as it could help inducted noise to disturb the inputs. All logic pins enforce a specific behavior and cannot be left unconnected.

Figure 12. Logic input pins.

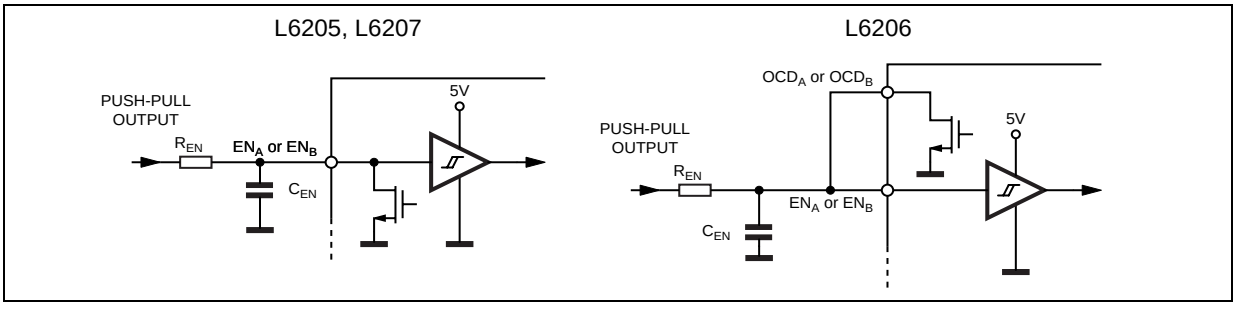


3.10 EN pins

The *EN$_A$, EN$_B$* pins are, actually, bi-directional: as an input, with a comparator similar to the other logic input pins (TTL/CMOS with hysteresis), they control the state of the PowerDMOS. When each of the two pins is at a low logic level, all the PowerDMOS of the corresponding H-bridge (A or B) are turned off. In L6205 and L6207 the EN pins are also connected to the two corresponding open drain outputs of the protection circuits that will pull the pins to GND if over current in the corresponding H-bridge or over temperature conditions exist. In L6206 the open drain outputs are on separate pins, OCD_A and OCD_B, allowing easier external diagnostics and overcurrent management. For this reason, with L6205 and L6207 (and L6206 if EN pins are connected to DIAG pins) EN pins must be driven through a series resistor of 2.2kΩ minimum (for 5V logic), to allow the voltage at the pin to be pulled below the turn-off threshold.

A capacitor (C_{EN} in Figure 13) connected between each EN pin and GND is also recommended, to reduce the r.m.s. value of the output current when overcurrent conditions persist (see *Over Current Protection* section). EN pin must not be left unconnected.

Figure 13. EN_A and EN_B input pins.



3.11 Programmable off-time Monostable (L6207 ONLY)

The L6207 includes a constant off time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOS transistors and ground, as shown in Figure 14. As the current in the load builds up the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$) the sense comparator triggers the monostable switching the low-side MOS off. The low-side MOS remain off for the time set by the monostable and the motor current recirculates in the upper path. When the monostable times out the bridge will again turn on. Since the internal dead time, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective off time is the sum of the monostable time plus the dead time.

Figure 14. PWM Current Control Circuitry (L6207 ONLY).

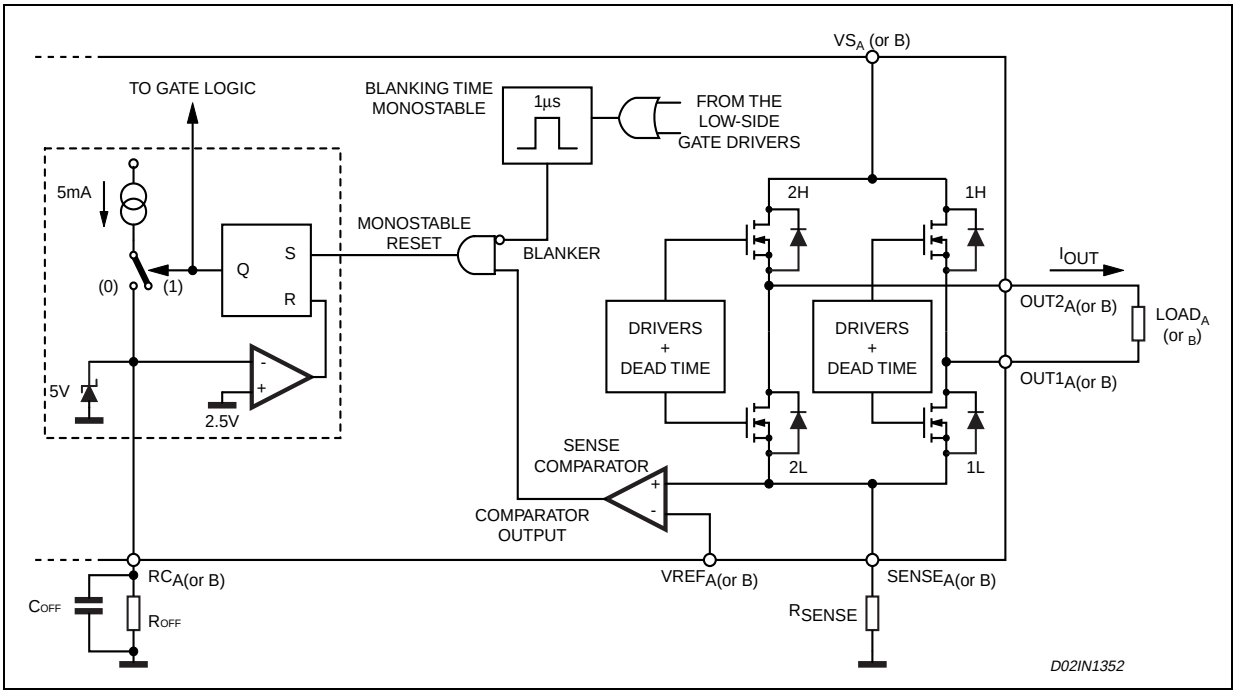


Figure 15 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. Immediately after the low-side Power MOS turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6207 provides a 1µs Blanking Time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely re-trigger the monostable.

Figure 15. PWM Output Current Regulation Waveforms (L6207 ONLY).

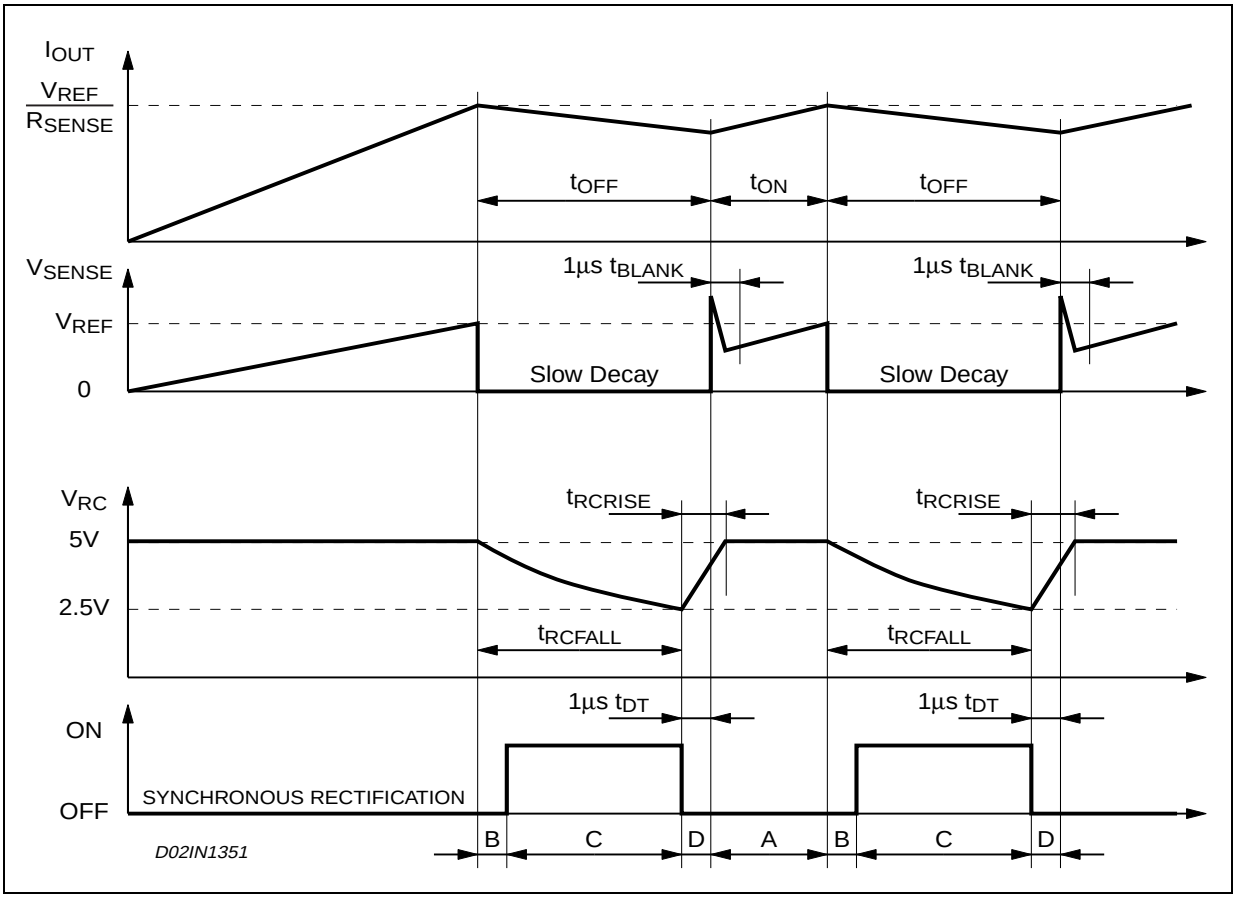


Figure 16 shows the magnitude of the Off Time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$

$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated Dead Time with:

$20K\Omega \leq R_{OFF} \leq 100K\Omega$

$0.47nF \leq C_{OFF} \leq 100nF$

$t_{DT} = 1\mu s$ (typical value)

Therefore:

$t_{OFF(MIN)} = 6.6\mu s$

$t_{OFF(MAX)} = 6ms$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.
The capacitor value chosen for C_{OFF} also affects the Rise Time t_{RCRISE} of the voltage at the pin RC_A (or RC_B). The Rise Time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on time t_{ON}, which depends by motors and supply parameters, has to

be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the on time t_{ON} can not be smaller than the minimum on time $t_{ON(MIN)}$.

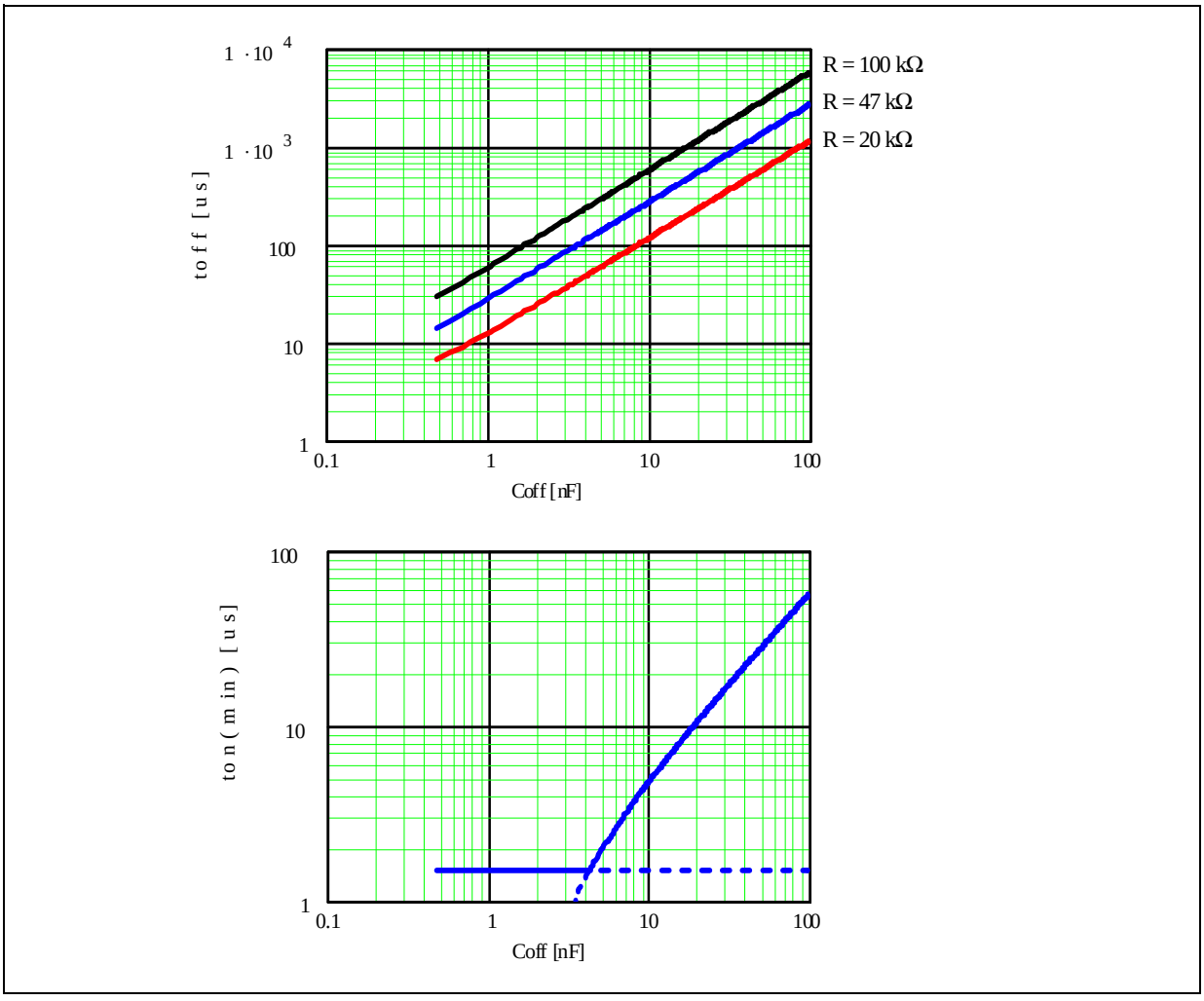
$$\begin{cases} t_{ON} > t_{ON(MIN)} = 1.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

3.11.1 Off-time Selection and minimum on-time (L6207 ONLY)

Figure 16 also shows the lower limit for the on time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the off time t_{OFF} is not more constant.
So, small C_{OFF} value gives more flexibility for the applications (allows smaller on time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

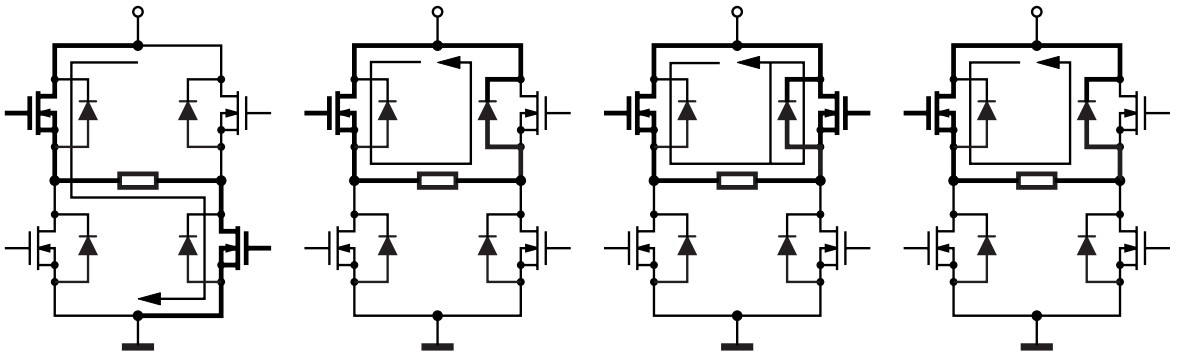
Figure 16. Off-time selection and minimum on-time (L6207 ONLY).



3.11.2 Slow Decay Mode (L6207 ONLY)

Figure 17 shows the operation of the bridge in the Slow Decay mode. At the start of the off time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the dead time the upper power MOS is operated in the synchronous rectification mode. When the monostable times out, the lower power MOS is turned on again after some delay set by the dead time to prevent cross conduction.

Figure 17. Slow Decay Mode Output Stage Configurations



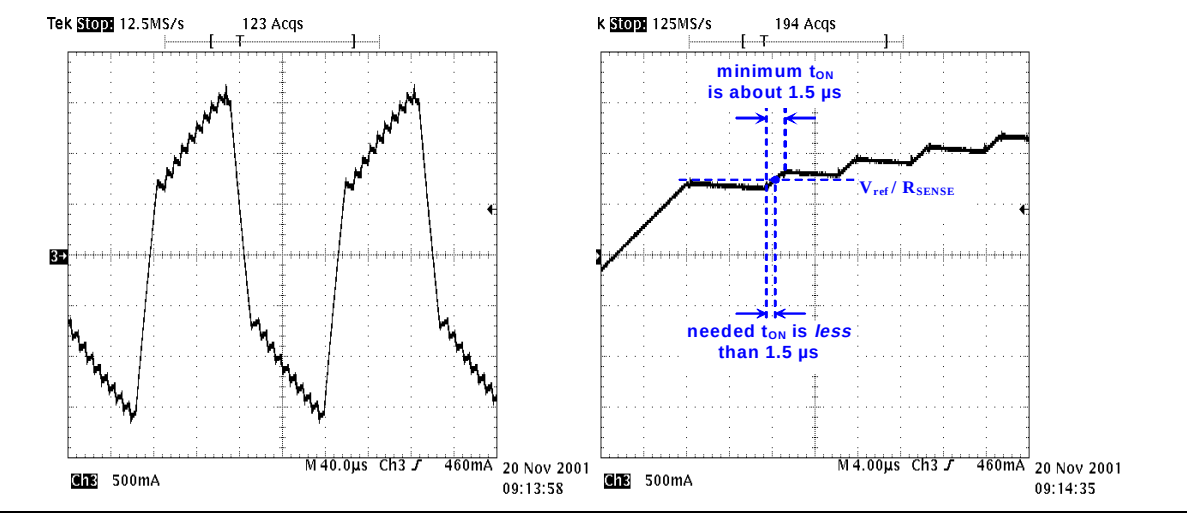
In some conditions (short off-time, very low regulated current, high motor winding L / R) the system may need an on-time shorter than 1.5µs. In these cases the PWM current controller can loose the regulation.

Figure 18 shows the operation of the circuit in this condition. When the current first reaches the threshold, the bridge is turned off for a fixed time and the current decays. During the following on-time current increases above the threshold, but the bridge cannot be turned off until the minimum 1.5µs on-time expires. Since current increases more in each on-time than it decays during the off-time, it keeps growing during each cycle, with steady state asymptotic value set by duty-cycle and load DC resistance: the resulting peak current will be

$I_{pk} = V_S \cdot D / R_{LOAD}$,

where $D = t_{ON} / (t_{ON} + t_{OFF})$ is the duty-cycle and R_{LOAD} is the load DC resistance.

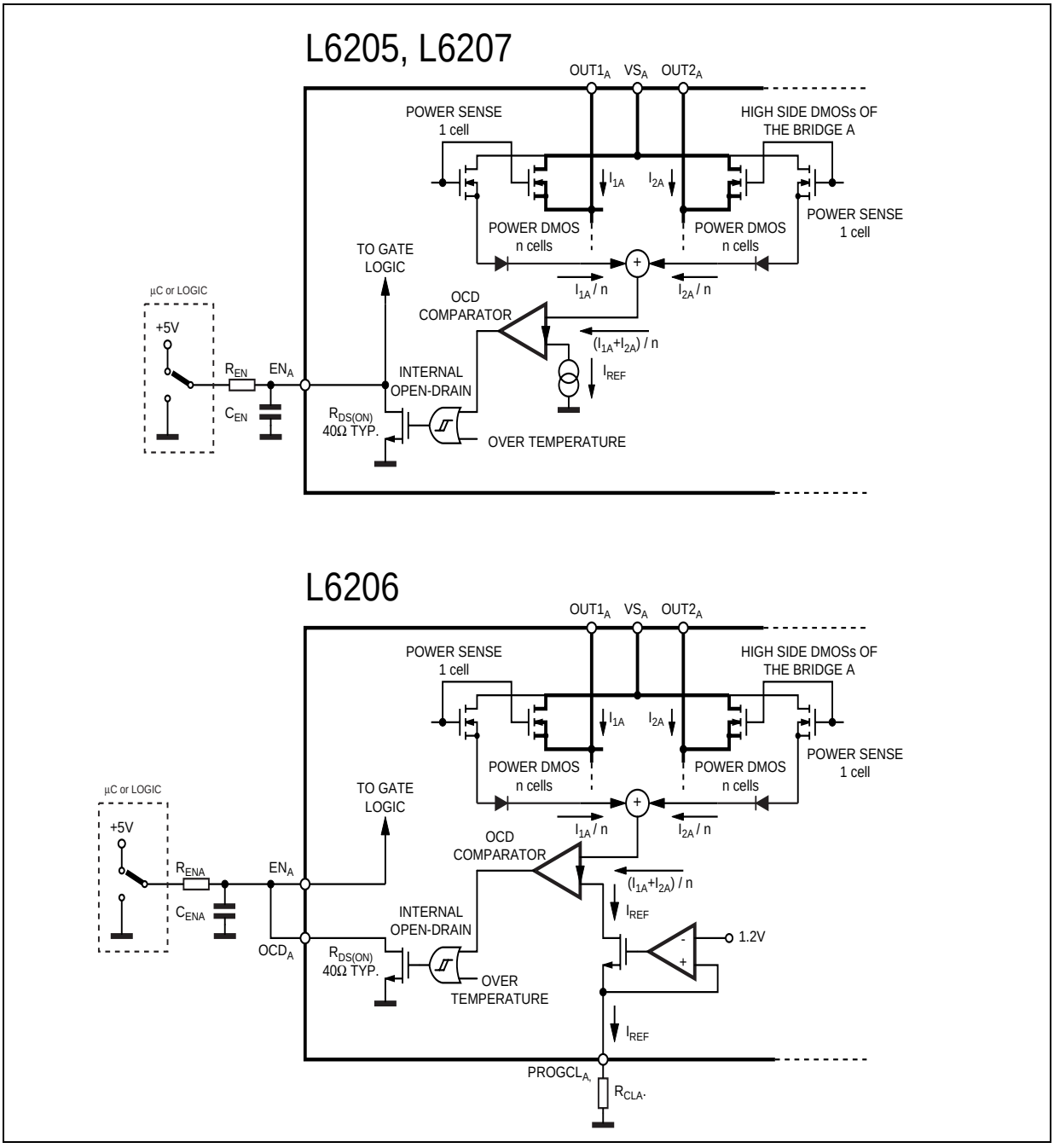
Figure 18. Minimum on-time can cause the PWM controller to loose the regulation (L6207 ONLY).



3.12 Over Current Protection

To implement an Over Current (i.e. short circuit) Protection, a dedicated Over Current Detection (OCD) circuitry (see Figure 19 for a simplified schematic) senses the current in each high side. Power DMOS are actually made up with thousands of individual identical cells, each carrying a fraction of the total current flowing. The current sensing element, connected in parallel to the Power DMOS, is made only with few such cells, having a 1:N ratio compared to the power DMOS. The total drain current is split between the output and the sense element according to the cell ratio. Sensed current is, then, a small fraction of the output current and will not contribute significantly to power dissipation.

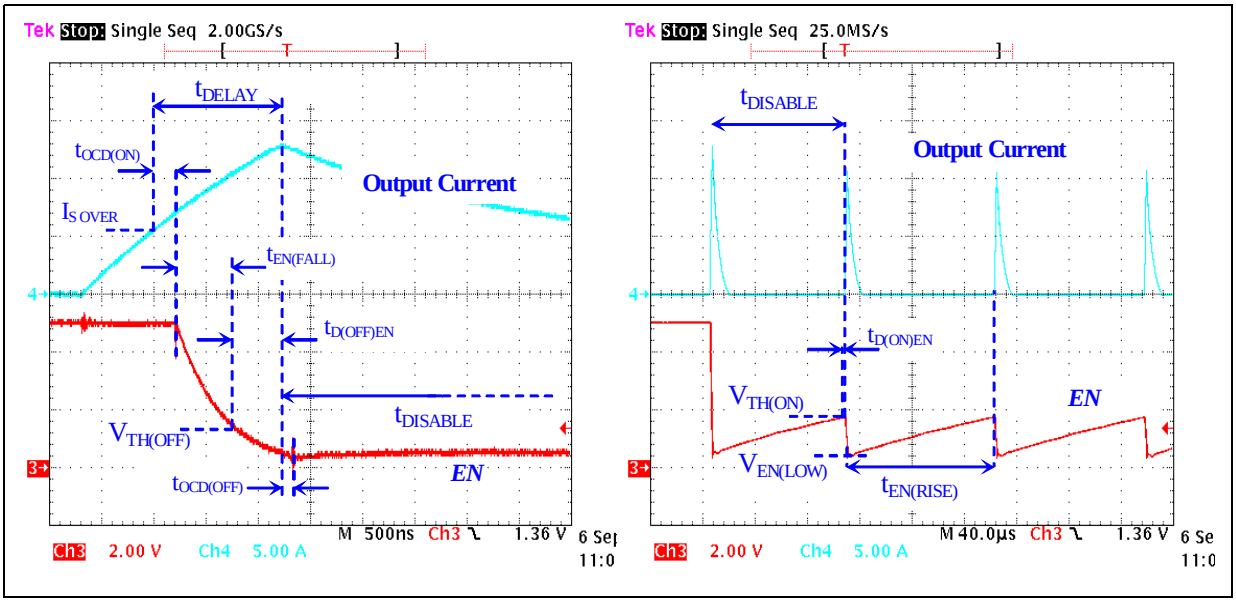
Figure 19. Over Current Detection simplified circuitry.



This sensed current is compared to an internally generated reference (adjustable through the external resistors R_{CLA} and R_{CLB} for L6206) to detect an over current condition. An internal open drain mosfet turns on when the sum of the currents in the bridges 1A and 2A or 1B and 2B reaches the threshold (5.6A typical value for L6205 and L6207; adjustable through the external resistors R_{CLA} and R_{CLB} for L6206); in L6205 and L6207 the open drain are internally connected to the *EN* pins; with L6206 *OCD* pins should be connected to *EN* pins to allow the protection working. To ensure an over current protection, connect these pins to an external RC network (see Figure 19).

Figure 20 shows the device operating in overcurrent condition (short to ground). When an over current is detected the internal open drain mosfet pull the *EN* pin to GND switching off all 4 power DMOS of the interested bridge and allowing the current to decay. Under a persistent over current condition, like a short to ground or a short between two output pins, the external RC network on the *EN* pin (see Figure 19) reduces the r.m.s. value of the output current by imposing a fixed disable-time after each over current occurrence. The values of R_{EN} and C_{EN} are selected to ensure proper operation of the device under a short circuit condition. When the current flowing through the high side DMOS reaches the OCD threshold (5.6 A typ. for L6205 and L6207, adjustable for L6206), after an internal propagation delay ($t_{OCD(ON)}$) the open drain starts discharging C_{EN}. When the *EN* pin voltage falls below the turn-off threshold ($V_{TH(OFF)}$) all the Power DMOS turn off after the internal propagation delay ($t_{D(OFF)EN}$). The current begins to decay as it circulates through the freewheeling diodes. Since the DMOS are *off*, there is no current flowing through them and no current to sense so the OCD circuit, after a short delay ($t_{OCD(OFF)}$), switches the internal open drain device off, and R_{EN} can charge C_{EN}. When the voltage at *EN* pin reaches the turn-on threshold ($V_{TH(ON)}$), after the $t_{D(ON)EN}$ delay, the DMOS turn on and the current restarts. Even if the maximum output current can be very high, the external RC network provides a disable time ($t_{DISABLE}$) to ensure a safe r.m.s. value (see Figure 20).

Figure 20. Over Current Operation.



The maximum value reached by the current depends on its slew-rate, so on the short circuit nature and supply voltage, and on the total intervention delay (t_{DELAY}). It can be noticed that after the first current peak, the maximum value reached by the output current becomes lower, because the capacitor on *EN* pins is discharged starting from a lower voltage, resulting in a shorter t_{DELAY}.

The following approximate relations estimate the disable time and the first OCD intervention delay after the short circuit (worst case).

The time the device remains disabled is:

$$t_{DISABLE} = t_{OCD(OFF)} + t_{EN(RISE)} + t_{D(ON)EN}$$

where

$$t_{EN(RISE)} = R_{EN} \cdot C_{EN} \cdot \ln \frac{V_{DD} - V_{EN(LOW)}}{V_{DD} - V_{TH(ON)}}$$

$V_{EN(LOW)}$ is the minimum voltage reached by the *EN* pin, and can be estimated with the relation:

$$V_{EN(LOW)} = V_{TH(OFF)} \cdot e^{-\frac{t_{D(OFF)EN} + t_{OCD(OFF)}}{R_{OPDR} \cdot C_{EN}}}$$

The total intervention time is

$$t_{DELAY} = t_{OCD(ON)} + t_{EN(FALL)} + t_{D(OFF)EN}$$

where

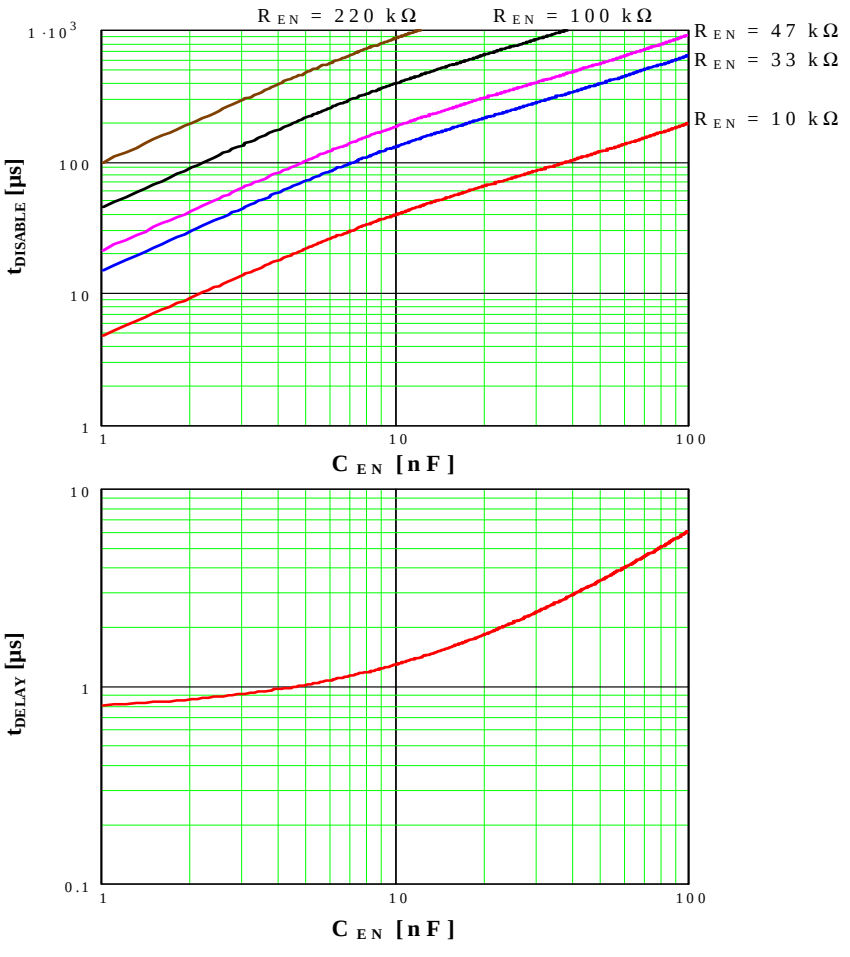
$$t_{EN(FALL)} = R_{OPDR} \cdot C_{EN} \cdot \ln \frac{V_{DD}}{V_{TH(OFF)}}$$

$t_{OCD(OFF)}$, $t_{OCD(ON)}$, $t_{D(ON)EN}$, $t_{D(OFF)EN}$, and R_{OPDR} are device intrinsic parameters, V_{DD} is the pull-up voltage applied to R_{EN}.

The external RC network, C_{EN} in particular, must be chosen obtaining a reasonable fast OCD intervention (short t_{DELAY}) and a safe disable time (long $t_{DISABLE}$). Figure 21 shows both $t_{DISABLE}$ and t_{DELAY} as a function of C_{EN}: at least 100µs for $t_{DISABLE}$ are recommended, keeping the delay time below 1÷2µs at the same time.

The internal open drain can also be turned on if the device experiences an **over temperature** (OVT) condition. The OVT will cause the device to shut down when the die temperature exceeds the OVT threshold (T_J>165 °C typ.). Since the OVT is also connected directly to the gate drive circuits (see Figure 1 to Figure 3), all the Power DMOS will shut down, even if *EN* pin voltage is still over $V_{th(OFF)}$. When the junction temperature falls below the OVT turn-off threshold (150 °C typ.), the open drain turn off, C_{EN} is recharged up to $V_{TH(ON)}$ and then the PowerDMOS are turned on back.

Figure 21. Typical disable and delay time as a function of C_{EN}, for several values of R_{EN}.



3.13 Adjusting the Over Current Detection trip point (L6206 ONLY)

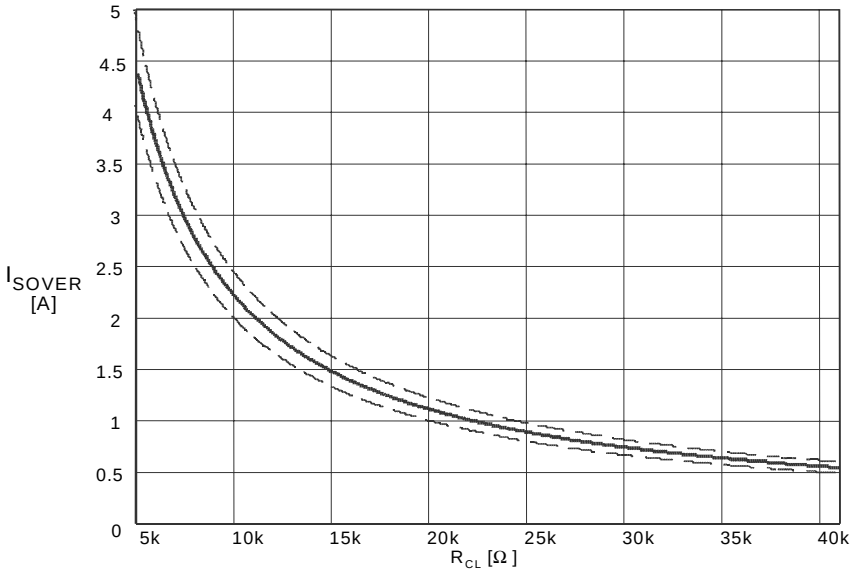
The L6206 allows the user to set the Over Current Detection threshold separately for the two full bridges connecting two resistors (R_{CL}) to pins *PROGCL$_A$* and *PROGCL$_B$*. The OCD threshold (I_{SOVER}) follows the equations:

– I_{SOVER} = 5.6A ±30% at -25 °C < T_j < 125 °C if R_{CL} = 0 Ω (*PROGCL* connected to GND)

– $I_{SOVER} = \frac{22100}{R_{CL}}$ ±10% at -25 °C < T_j < 125 °C if 5K Ω < R_{CL} < 40k Ω

Figure 22 shows the OCD threshold versus R_{CL} value in the range from 5kΩ to 40kΩ.

Figure 22. Output Current Detection Threshold versus R_{CL} Value (L6206 ONLY)

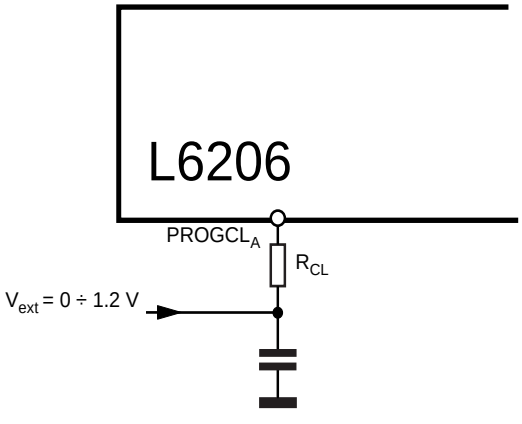


The Over Current Detection threshold can also be adjusted through an external reference voltage, as shown in Figure 23. The external reference voltage source should be able to sink current (about 300 µA maximum). Moreover, if supply voltage is provided to the L6206 before V_{EXT}, and its *EN* pins are at a high logic level, the device starts working with minimum OCD threshold (actually the capacitor placed at the bottom of R_{CL} allows a short start-up time with higher OCD threshold). V_{EXT} can also be obtained through a PWM output of a µC, adding a series resistor to obtain a low-pass filter.

The OCD threshold (I_{SOVER}) follows the equation:

$$I_{SOVER} = \frac{18416.7(1.2V - Vext)}{R_{CL}} \pm 10\%, \qquad \text{at } -25\,^{\circ}C < T_j < 125\,^{\circ}C \qquad \text{if } 0.5\,A < I_{SOVER} < 4.5\,A$$

Figure 23. Adjusting the OCD Threshold through an external reference voltage (L6206 ONLY)

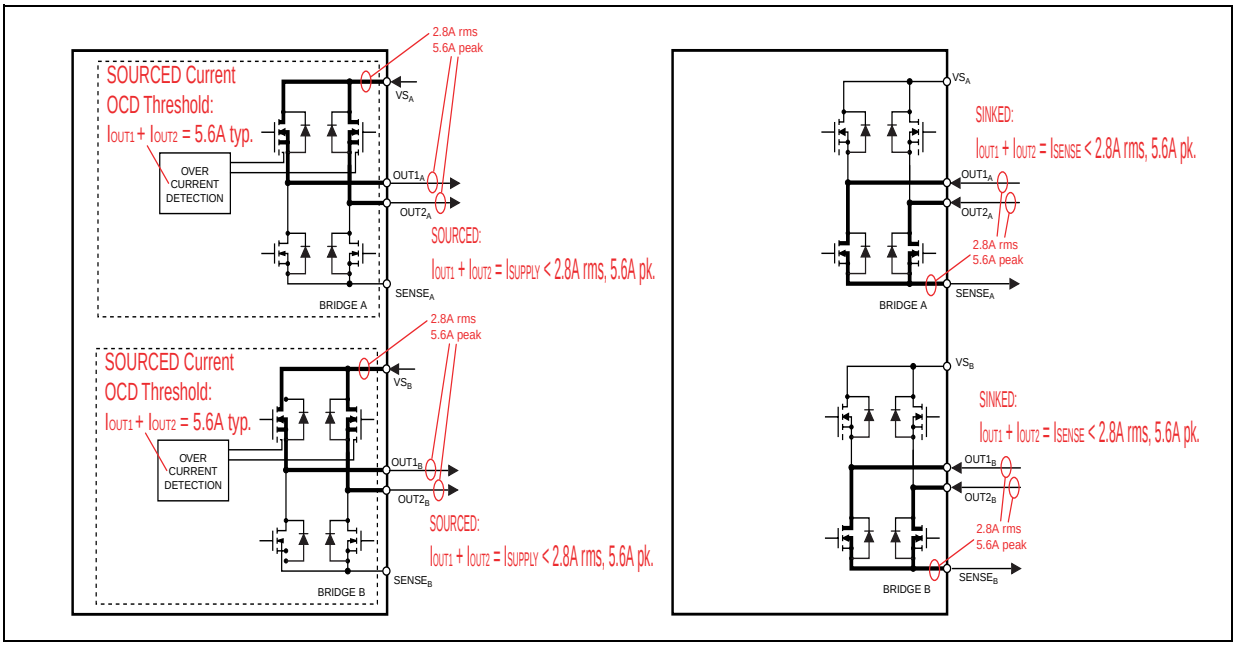


3.14 Paralleling two Full Bridges

3.14.1 Paralleling two Full Bridges to get a single Full Bridge

The outputs of L6205, L6206, L6207 can be paralleled to increase the output current capability or reduce the power dissipation in the device at a given current level. It must be noted, however, that the internal wire bond connections from the die to the power or sense pins of the package must carry current in both of the associated half bridges (see Figure 24). When the two halves of one full bridge (for example $OUT1_A$ and $OUT2_A$) are connected in parallel, the peak current rating is not increased since the total current must still flow through one bond wire on the power supply or sense pin. In addition, the over current detection senses the sum of the current in the upper devices of each bridge (A or B) so connecting the two halves of one bridge in parallel does not increase the over current detection threshold.

Figure 24. V_S and SENSE pins maximum current handling



This configuration has to be used when two separate loads are driven, since the ICs has only two ENABLE inputs, one for the full bridge A and the other for the bridge B. In this case pulling to GND one of the two ENABLE pins will disable only one load (see Figure 25).

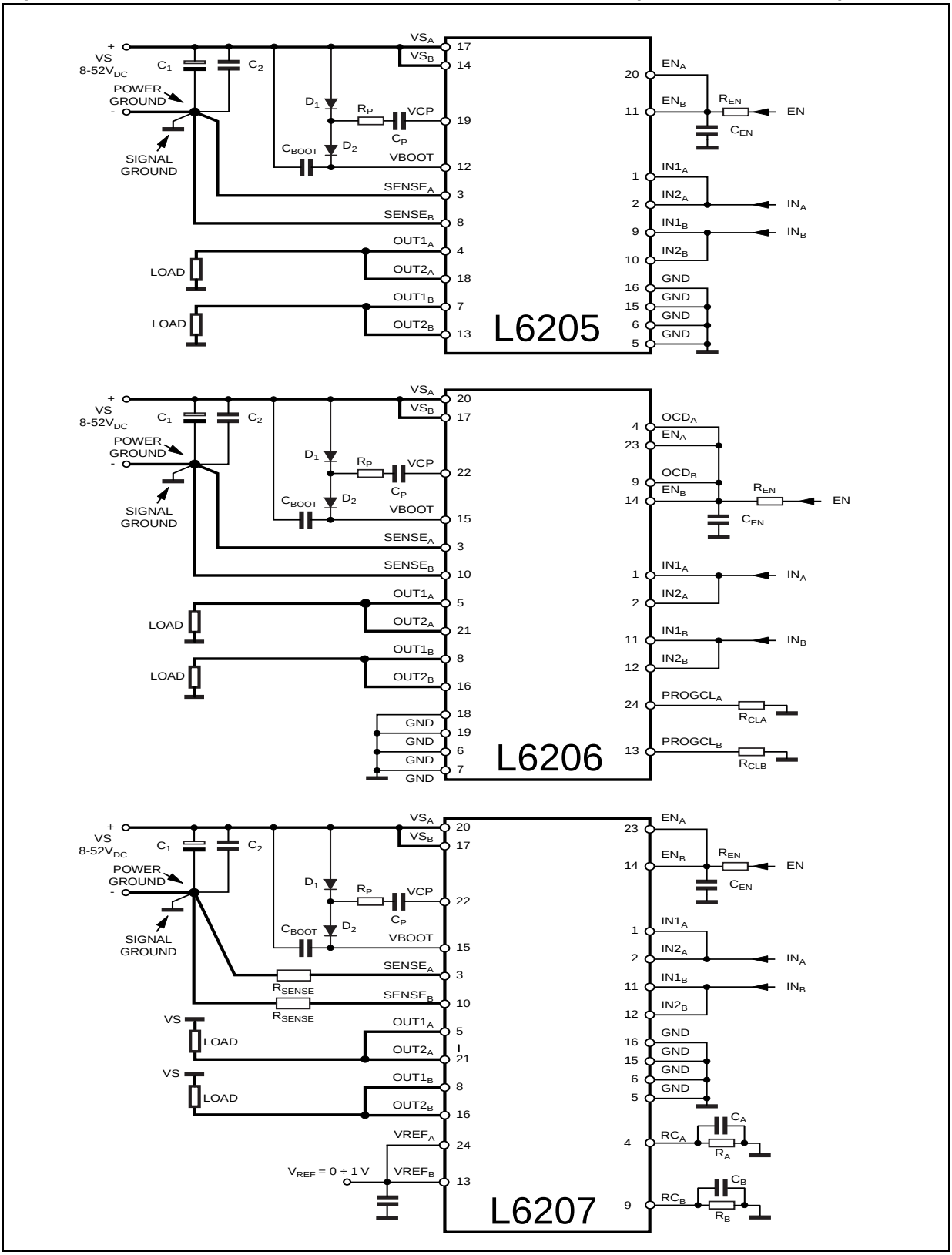
This configuration can also be used if a 5.6A OCD threshold is desired (instead of 11.2A).

Half Bridge 1 and the Half Bridge 2 of the Bridge A are connected in parallel and the same done for the Bridge B as shown in Figure 25. In this configuration, the peak current for each half bridge is still limited by the bond wires for the supply and sense pins so the dissipation in the device will be reduced, but the peak current rating is not increased. Using this configuration with L6206, two separate resistors connected to pins $PROGCL_A$ and $PROGCL_B$ must be used. With L6207, two separate RC network should be used on *RC* pins. When two different loads are driven (see Figure 25) by the two equivalent half bridges, two separate sensing resistors are needed, while if the two equivalent half bridges drive two separate loads, they must be connected from the *OUT* pins to V_S (see Figure 25) to make the PWM current control working properly.

In this configuration, the resulting bridge has the following characteristics (typical values).

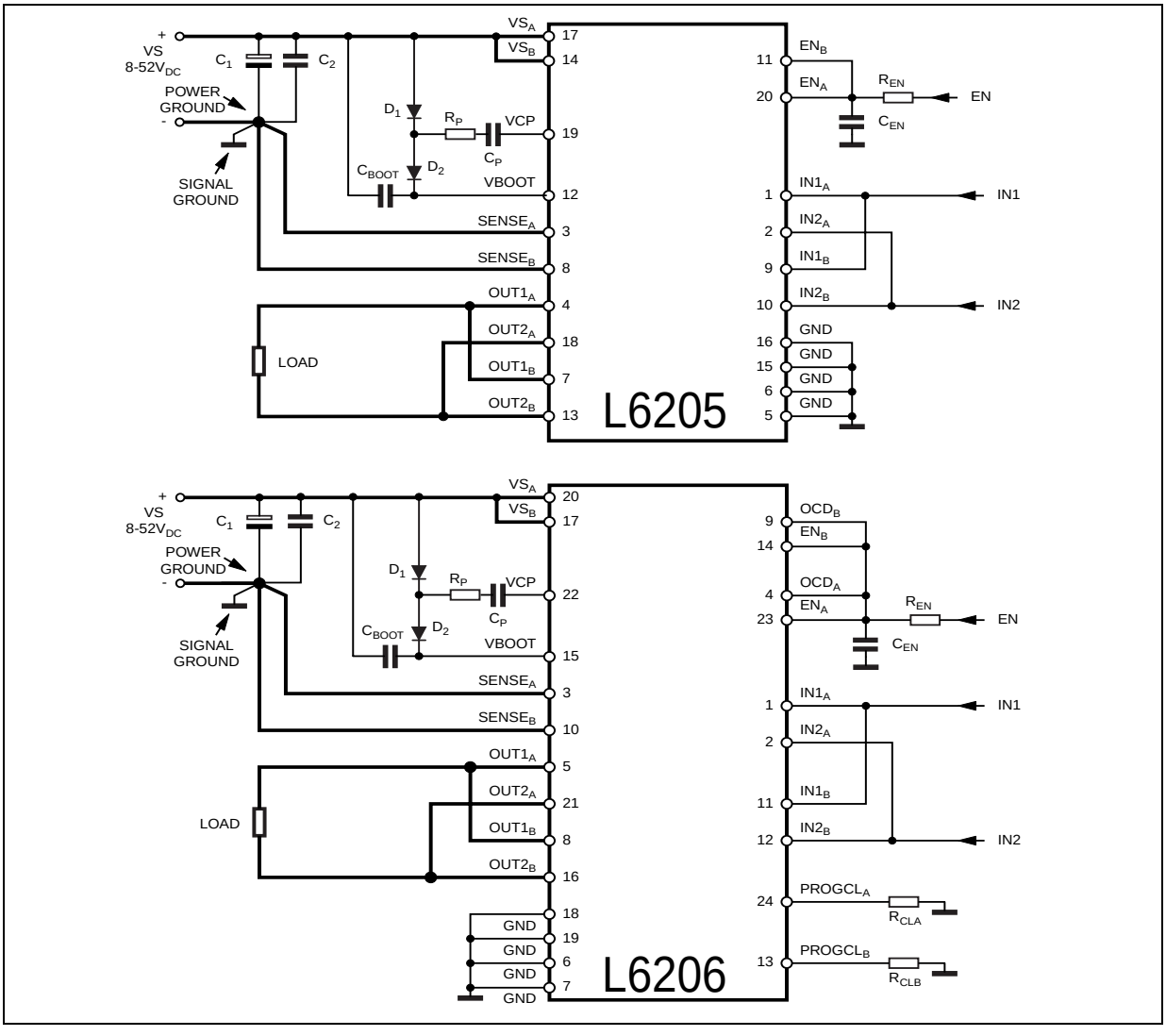
- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$ 0.15Ω Typ. Value @ T_J = 25°C
- 2.8A max RMS Load Current
- 5.6A OCD Threshold

Figure 25. Parallel connection with lower Overcurrent Threshold (L6205, L6206, L6207)



For some applications the recommended configuration is Half Bridge 1 of Bridge A paralleled with the Half Bridge 1 of the Bridge B, and the same for the Half Bridges 2 as shown in Figure 26.

Figure 26. Parallel connection for higher current (L6205 and L6206 ONLY)



This configuration cannot be used with L6207, because of its internal PWM current controllers that work separately for bridge A and bridge B. Using this configuration with the L6207 may damage the device.

In this configuration the resulting Bridge has the following characteristics (typical values).

- Equivalent Device: FULL BRIDGE
- $R_{DS(ON)}$ 0.15Ω Typ. Value @ T_J = 25°C
- 5.6A max RMS Load Current
- 11.2A OCD Threshold

It should be noted that using two separate loads for the two equivalent half bridges the maximum current cannot be sourced or sinked simultaneously by the two equivalent half bridges (for example to drive two separate loads), due to the 5.6 A maximum current limit for *V_S* and *SENSE* pins (see Figure 24). When a single load is driven (see Figure 26) R_{CLA} and R_{CLB} resistors connected to PROGCL pins of L6206 should have the same value.

3.14.2 Paralleling the four Half Bridges to get a single Half Bridge

It is also possible to parallel the four Half Bridges to obtain a simple Half Bridge as shown in Figure 27.

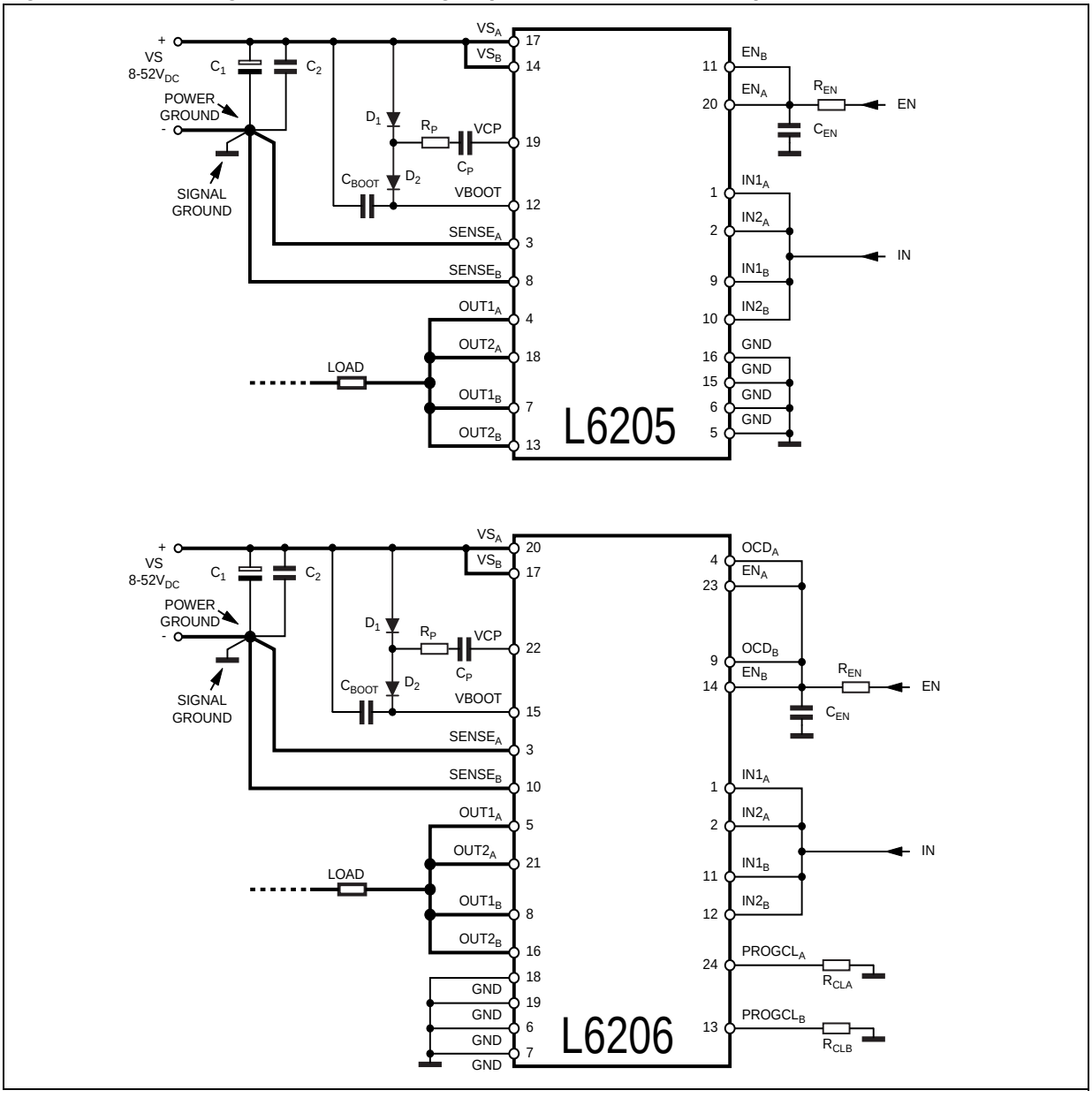
This configuration cannot be used with L6207, because of its internal PWM current controllers that work separately for bridge A and bridge B. Using this configuration with the L6207 may damage the device.

The resulting half bridge has the following characteristics (typical values).

- Equivalent Device: HALF BRIDGE
- $R_{DS(ON)}$ 0.075Ω Typ. Value @ T_J = 25°C
- 5.6A max RMS Load Current
- 11.2A OCD Threshold

With L6206 R_{CLA} and R_{CLB} resistors connected to PROGCL pins must have the same value.

Figure 27. Paralleling the four Half Bridges (L6205 and L6206 ONLY)

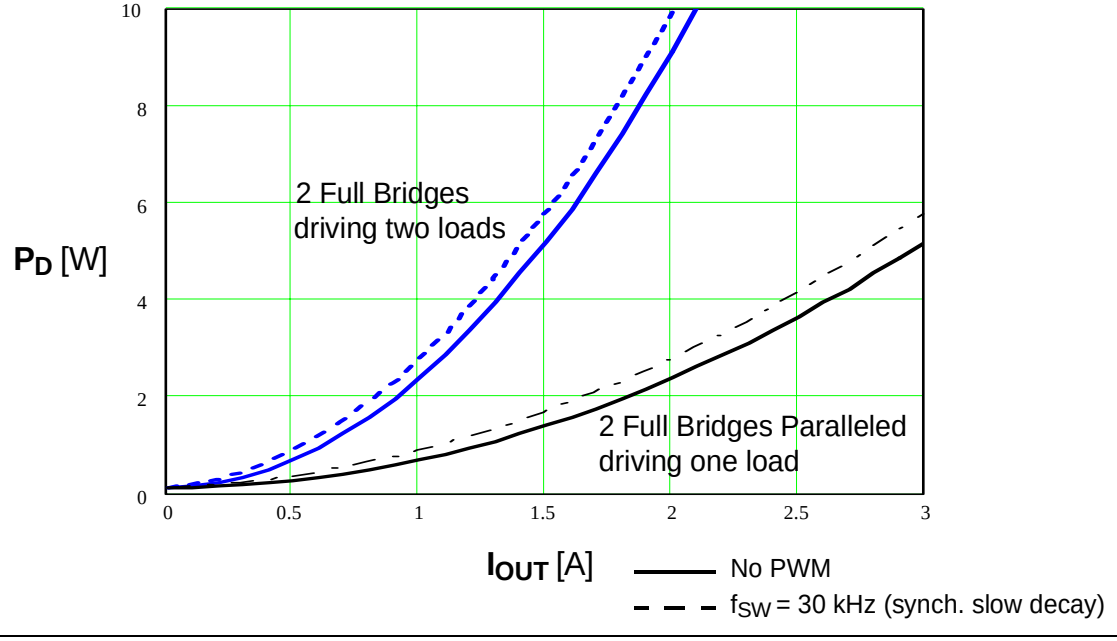


3.15 Power Management

Even when operating at current levels well below the maximum ratings of the device, the operating junction temperature must be kept below 125 °C.

Figure 28 shows the IC dissipated power versus the r.m.s. load current, in the case of a single IC driving two loads (for instance 2 DC motors or a two-phase stepper motor) or a single IC, with two full bridges paralleled (see *Paralleling two Full Bridges* section) driving one load (for instance 1 DC motor or one phase of a two-phase stepper motor) and assuming the supply voltage is 24V.

Figure 28. IC Dissipated Power versus Output Current.

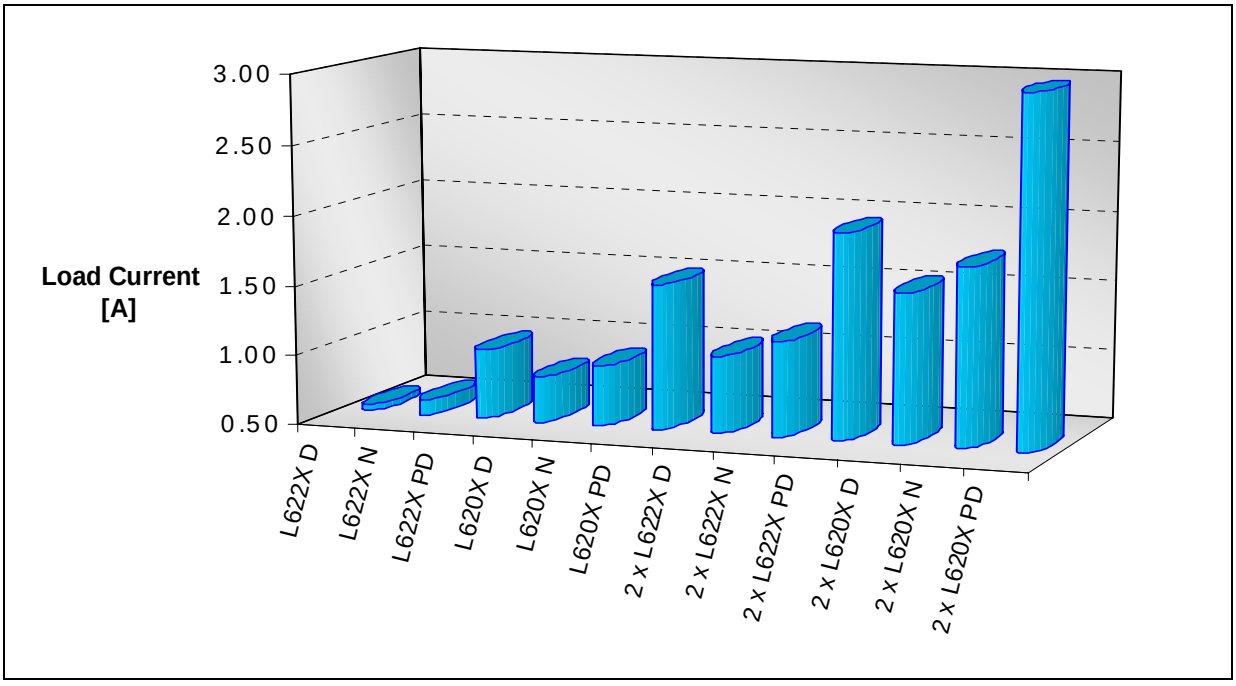


3.15.1 Maximum output current vs. selectable devices

Figure 29 reports a performance comparison between different devices of the PowerSPIN family, for different packages and in paralleled configuration, with the following assumptions:

- Each equivalent full bridge drives a load.
- Supply voltage: 24 V; Switching frequency: 30 kHz.
- T_{amb} = 25 °C, T_J = 125 °C.
- Maximum $R_{DS(ON)}$ (taking into account process spread) has been considered, @ 125 °C.
- Maximum quiescent current I_Q (taking into account process spread) has been considered.
- PCB is a FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm) for SO and PowerDIP packages (D, N suffixes).
- PCB is a FR4 with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer for the PowerSO package (PD suffix).
- For each device configuration (on the x axis) y axis reports the maximum output (load) current.
- 2 x 'device' means that the two loads are driven by two equivalent full bridges obtained paralleling two full bridges for each of the two IC used. The current reported in Figure 29 is the maximum output current an equivalent full bridge (a paralleled IC).

Figure 29. Maximum output current vs. selectable devices.



3.15.2 Power Dissipation Formulae for different sequences

Figure 30 to Figure 33 are screenshots of a spreadsheet that helps calculating power dissipation in specified conditions (application and motor data), and estimates the resulting junction temperature for a given package and copper area available on the PCB [4].

The model assumes that the device is driving a two-phase bipolar stepper motor and that a PWM current control with slow decay recirculation technique is implemented (L6207 integrates the PWM controller); it considers power dissipation during the on-time and the off-time, rise and fall time (when a phase change occurs) considering the operating sequence (Normal, Wave or Half Step Mode), the switching losses and the quiescent current power dissipation.

Figure 30. Definition of parameters for the three different sequences. The current in only one phase is shown.

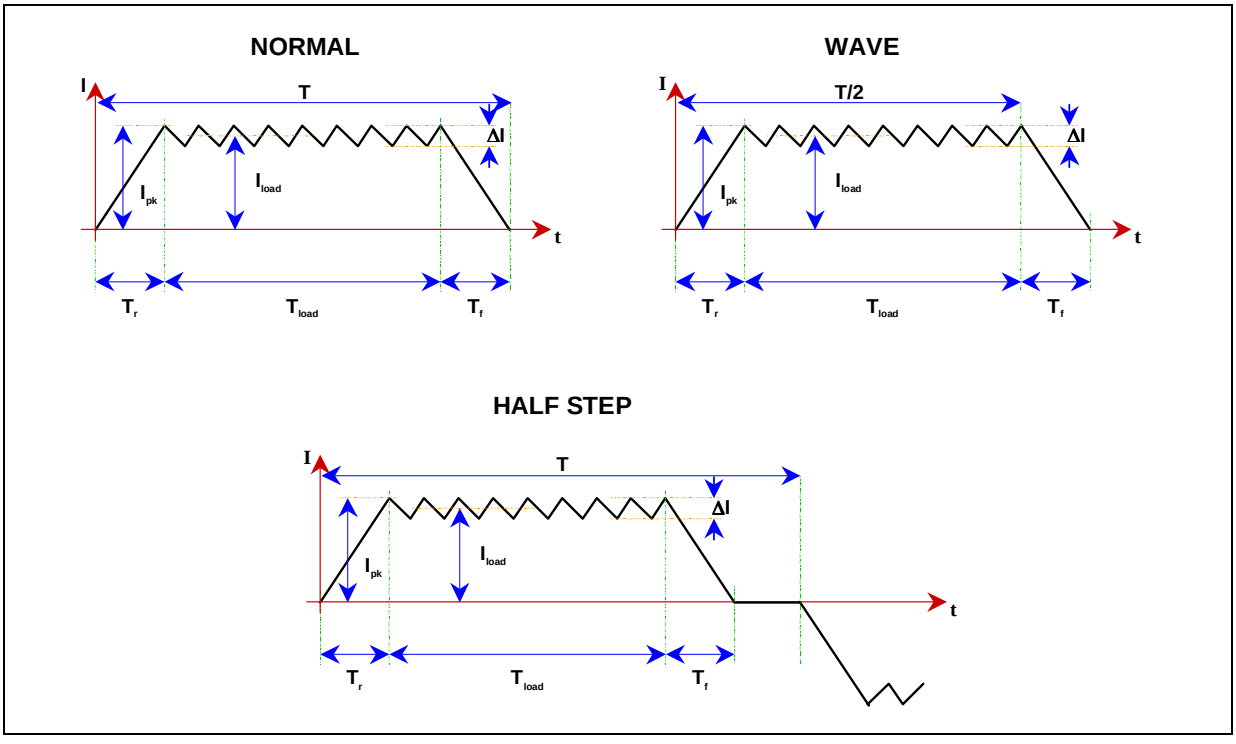


Figure 31. Input Data.

Input Data

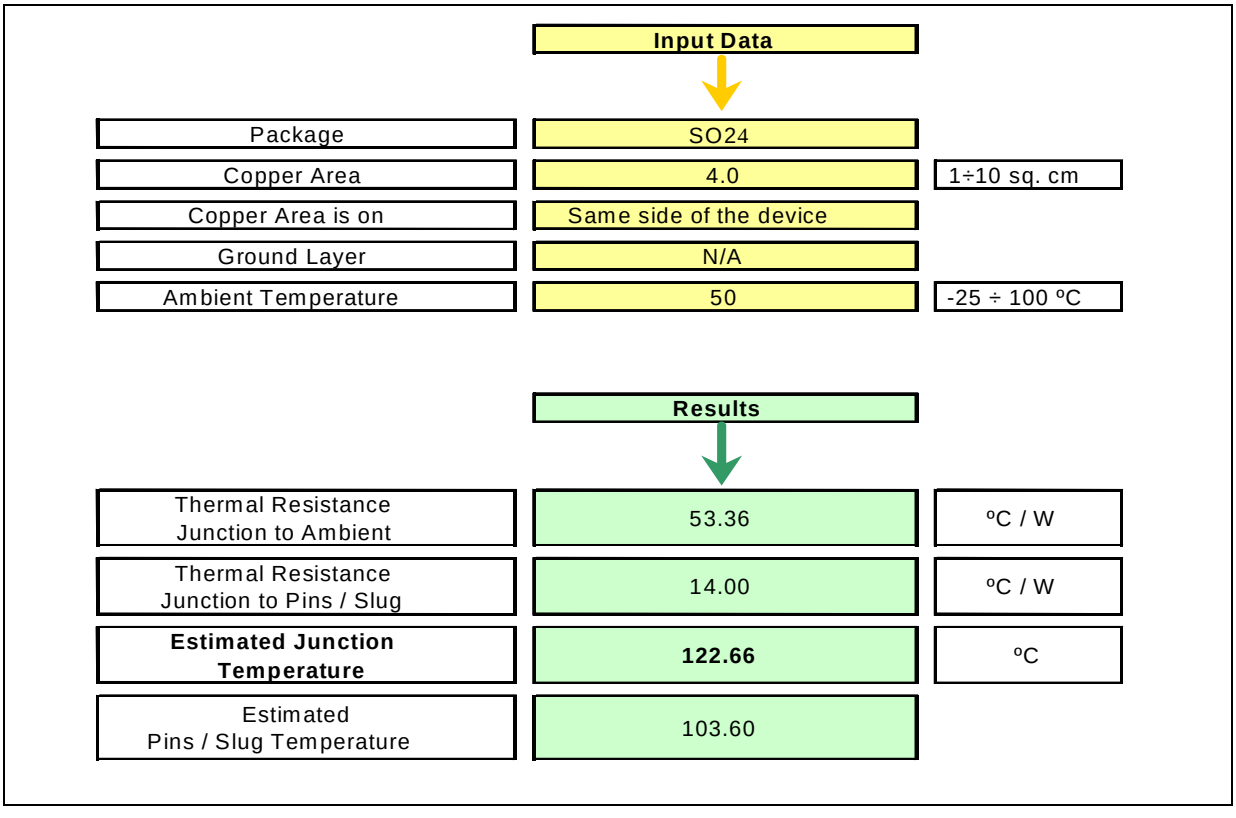
Device Input Values				
Maximum Drain-Source ON Resistance	Ron	= 5.60E-01	[Ohm]	Average Value between High-Side and Low-Side
Maximum diode voltage	Vd	= 1.20E+00	[V]	
Quiescent Current	Iq	= 5.50E-03	[mA]	
Motor Input Values				
Maximum BEMF Voltage	Vb	= 1.50E+01	[V]	
Motor Inductance	Lm	= 7.90E-03	[H]	
Motor Resistance	Rm	= 6.60E+00	[Ohm]	
Application Input Values				
Supply Voltage	Vs	= 2.40E+01	[V]	
Peak Current	Ipk	= 1.00E+00	[A]	
Off-Time	tOFF	= 1.50E-05	[s]	
Step Frequency	fCK	= 1.00E+03	[Hz]	
Sensing Resistance	Rs	= 5.00E-01	[Ohm]	
Decay Type	SLOW		-	"SLOW" = Synchronous Slow Decay "FAST" = Quasi-Synchronous Fast decay
Stepping sequence	WAVE		-	"NORMAL", "HALF" or "WAVE"

Figure 32. Power Dissipation formulae and results.

		Result			
PowerDMOS Commutation Time	Tcom =	9.60E-08	[s]	Vs / (250V/µs)	
Rise Time	Trise =	4.03E-04	[s]	$-\ln\left[\frac{(-Ipk \cdot Rm - 2 \cdot Ipk \cdot Ron - Ipk \cdot Rs + Vs)}{Vs}\right] \cdot \frac{Lm}{Rm + Rs + 2Ron}$	
Fall Time	Tfall =	3.16E-04	[s]	$-\ln\left[\frac{Vs}{(Ipk \cdot Rm + 2 \cdot Ipk \cdot Ron + Ipk \cdot Rs + Vs)}\right] \cdot \frac{Lm}{(Rm + 2 \cdot Ron + Rs)}$ $-\ln\left[\frac{(Vs - 2 \cdot Vd)}{(Ipk \cdot Rm + Ipk \cdot Rs + Vs - 2 \cdot Vd)}\right] \cdot \frac{Lm}{(Rm + Rs)}$	NORMAL Mode HALF or WAVE Mode
Duty Cycle	D =	6.25E-01	-	Vb / Vs	Sync. Slow Decay
Switching Frequency	fSW =	2.50E+04	[Hz]	(1-D) / tOFF	
Current Ripple	ΔI =	2.85E-02	[A]	(Vs - Vb)*D / (Lm* fSW)	
Period	T =	2.00E-03	[s]	2 / fCK 4 / fCK 2 / fCK	NORMAL Mode HALF Mode WAVE Mode
Load Time	Tload =	5.97E-04	[s]	T-Trise-Tfall (3/4)T-rise (T/2)-Trise	NORMAL Mode HALF Mode WAVE Mode
Average Current during Load Time	I =	9.86E-01	[A]	$Ipk - \frac{\Delta I}{2}$	
r.m.s. Current during Load Time	Irms =	9.86E-01	[A]	$\sqrt{Ipk \cdot (Ipk - \Delta I) + \frac{\Delta I^2}{3}}$	
Rise Time Dissipating Energy	Erise =	1.50E-04	[J]	$2Ron \cdot Ipk^2 \cdot \frac{Trise}{3}$	
Fall Time Dissipating Energy	Efall =	3.62E-04	[J]	$2Ron \cdot Ipk^2 \cdot \frac{Tfall}{3}$ $2 \cdot Vd\left[Tfall \cdot \frac{(-Vs + 2 \cdot Vd)}{(Rm + Rs)} + \right.$ $\left. \cdot (Ipk \cdot Rm + Ipk \cdot Rs + Vs - 2 \cdot Vd) \cdot \frac{\left[1 - \exp\left[\frac{-Tfall}{Lm} \cdot (Rm + Rs)\right]\right]}{(Rm + Rs)^2}\right]$	MORMAL Mode HALF or WAVE Mode
Load Time Diss. Energy	Eload =	6.50E-05	[J]	$2Ron \cdot Irms^2 \cdot Tload$	Sync. Slow Decay

Commutatiion Time Dissipating Pw	Ecom =	6.78E-05	[J]	2Vs · I · Tcom · Tload · fSW
Quiescent Dissipating Pw	Pq =	1.32E-01	[W]	Vs · Iq
Total Dissi-pating Power	**P =**	**1.36E+00**	**[W]**	$\frac{2}{T}$ ·(Erise + Efall + Eload + Ecom) + Pq

Figure 33. Thermal Data inputs and results.



4 APPLICATION EXAMPLE (L6207)

Application Data		Motor Data	
Rotation Speed:	300 rpm (f_{CK} = 1kHz)	Winding Resistance:	6.6Ω
Winding peak Current:	1A	Winding Inductance:	7.9mH
Maximum Ripple:	50mA	Step Angle:	1.8°/step
Supply Voltage:	24V ±5%	Maximum BEMF at 300rpm:	15V
Sequence:	Wave Mode		

4.1 Decay mode, sensing resistors and reference voltage.

Referring to approximated formulae in Figure 32, it's possible to calculate the Duty-Cycle (D), the Switching Frequency (f_{SW}), the Current Ripple (ΔI). With a 15 µs off-time, we will have:

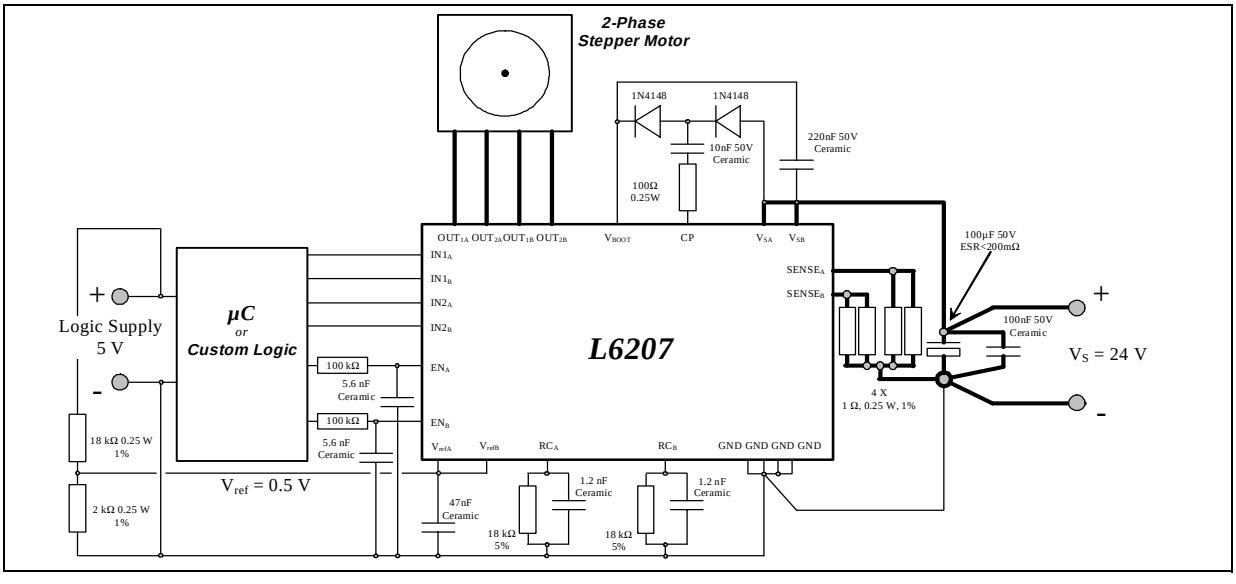
D ≅ 63%, f_{SW} ≅ 25kHz, ΔI ≅ 29mA. The on-time is t_{ON} = D / f_{SW} ≅ 25µs, which is far from the minimum allowed (1.5µs), so slow decay can be used.

The bulk capacitor need to withstand at least 24V + 5% + 25% ≅ 32V. A 50V capacitor will be used. Allowing a voltage ripple of 200mV, the capacitor ESR should be lower than 200mV / 1A = 200mΩ; the AC current capability should be about 1A.

Providing a reference voltage of 0.5V, 0.5Ω sensing resistor are needed. The resistors power rating is about P_R ≅ $I_{rms}^2 \cdot R_{SENSE} \cdot D$ ≅ 0.32W. Two 1Ω - 0.25W - 1% resistors in parallel are used. The charge pump uses recommended components (1N4148 diodes, ceramic capacitors and a 100Ω resistor to reduce EMI).

R = 18kΩ, C = 1.2 nF are connected to the RC pins, obtaining t_{OFF} ≅ 16µs. On the EN pins 5.6nF capacitors have been placed, and the pins are driven by the µC through 100kΩ resistors. With these values, in case of short circuit between two OUT pins or an OUT pin and GND, the PowerDMOS turns off after about 1µs, and $t_{DISABLE}$ ≅ 240µs.

Figure 34. Application Example.



With Wave Drive selected, referring to Figure 31 to Figure 33, the dissipating power is about 1.36 W. If the ambient temperature is lower than 50°C, with 4cm^2 of copper area on the PCB and a SO24 package, the estimated junction temperature is about 123°C. Using more copper area or a PowerDIP package will reduce the junction temperature.

5 APPENDIX - EVALUATION BOARDS

5.1 PractiSPIN

PractiSPIN is an evaluation and demonstration system that can be used with the PowerSPIN family (L62XX) of devices. A Graphical User Interface (GUI) (see Figure 35) program runs on an IBM-PC under windows and communicates with a common ST7 based interface board (see Figure 36) through the RS232 serial port. The ST7 interface board connects to a device specific evaluation board (target board) via a standard 34 pin ribbon cable interface.

Depending on the target device the PractiSPIN can drive a stepper motor, 1 or 2 DC motors or a brushless DC (BLDC) motor, operating significant parameters such as SPEED, CURRENT, VOLTAGE, DIRECTION, ACCELERATION and DECELERATION RATES from a user friendly graphic interface, and programming a sequence of movements.

The software also allows evaluating the power dissipated by the selected device and, for a given package and dissipating copper area on the PCB, estimates the device's junction temperature.

Figure 35. PractiSPIN PC Software

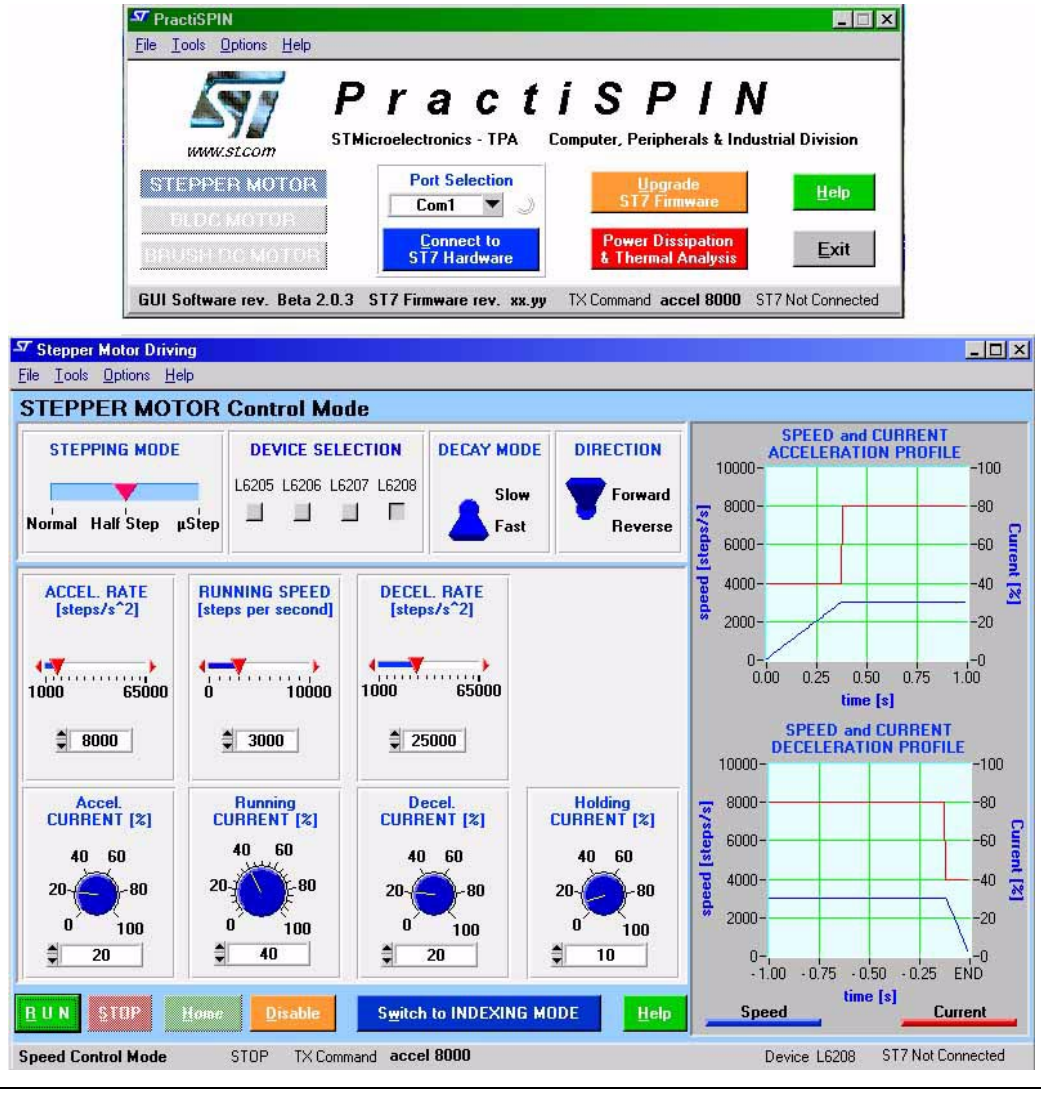
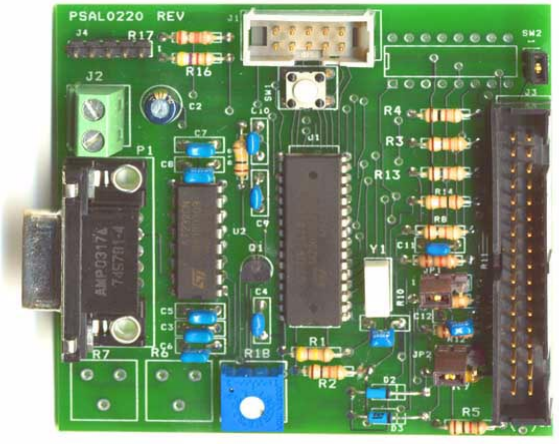


Figure 36. PractiSPIN ST7 Evaluation Board



5.2 EVAL6205N

An evaluation board has been produced to help the evaluation of the device in PowerDIP package. It implements a typical application with several added components. Figure 38 shows the electrical schematic of the board; in the table below the part list is reported.

CN1, CN2, CN3, CN4	2-poles connector	R1	100Ω resistor
CN5	34-poles connector	R2	700Ω 0.6W resistor
C1	220nF/100V Ceramic or Polyester capacitor	R3, R4, R13	10kΩ resistor
C2	220nF/100V Ceramic or Polyester capacitor	R5, R6	4.7kΩ resistor
C3	100µF/63V capacitor	R7, R8, R9, R10, R11, R12	1Ω 0.4W resistor
C4	10nF/100V Ceramic capacitor	R18, R14	1kΩ resistor
C5	10µF/16V Capacitor	R15, R19	20kΩ resistor
C6, C7, C11	100nF Capacitor	R16, R20	2.2kΩ resistor
C8, C10	470pF Capacitor	R21, R17	5kΩ trimmer
C9, C12	68nF Capacitor	R22	12kΩ resistor
C13	2.2nF Capacitor	R23	50kΩ trimmer
D1, D2	1N4148 Diode	U1	L6205N
D3	BZX79C5V1 5.1V Zener Diode	U2	L6506
JP1	3-pin jumper	JP2, JP3, JP4, JP5	2-pin jumper

The Evaluation Board provides external connectors for the supply voltage, an external 5V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN tool. The board also accommodates the L6506 PWM current controller. R23 sets the PWM operating frequency. If the L6506 does not need to be used, simply connect the two V_{REF} inputs to a voltage high enough to keep current control inactive.

The PractiSPIN tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains an upgradeable firmware. This tool allows a fast and easy evaluation of the PowerSPIN family devices, giving the ability of driving DC, BLDC and Stepper motors, depending on the target device. The PractiSPIN connected to the EVAL6205N can drive DC motors and inductive loads, allowing output voltage and current settings

The PC-software also provides a Power Dissipation and Thermal Analysis section, intended to help a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point designing an application (from the power dissipation and thermal point of view).

Running the evaluation board in stand-alone mode, instead, R17 and R21 set the reference voltage separately for the two bridges, while R16, C9 and R20, C12 are low-pass filters to provide an external reference voltage by a PWM output of a µC (see also the Microstepping section). Using external V_{REF} inputs R15, R17, R19, R21 can be disconnected through JP4 and JP5, unless the PractiSPIN ST7 evaluation board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN documentation).

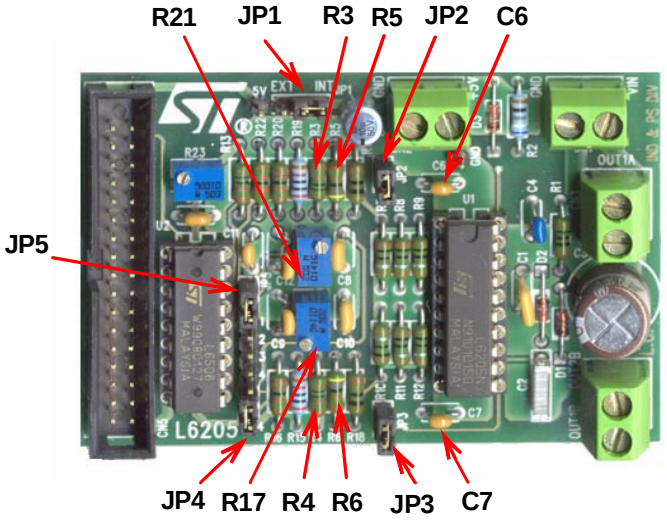
Closing JP2 and JP3 is recommended for safe Over Current Protection.

The 5V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R2, D3. Depending on the supply voltage, the value of resistor R2 should be changed in order to ensure a correct biasing of D3.

The jumper JP1 allows choosing the 5V voltage from the internal zener diode network or pin 11 of CN5 (for example an external µC board can provide 5V to the evaluation board). Also CN2 connector can be used to provide an external 5V voltage to the board (in that case R2, D3 should be disconnected). CN2, or pin 1 of CN5, can also be used to provide a 5V voltage to external circuits (as, for example, the PractiSPIN ST7 board). In this case the current that can be drawn form the board depends on the supply voltage and on R2 value.

Figure 39 to Figure 41 show the component placement and the two layers layout of the L6205N Evaluation Board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 37. EVAL6205N.



5.2.1 Important Notes

JP1 : close in INT position for use with PractiSPIN ST7 board

C6, C7 : recommended change to 5.6 nF for safe Overcurrent protection

R3, R4 : recommended change to 100 k for safe Overcurrent protection

R5, R6 : recommended change to 100 k if EN pins are driven from the CN5 connector (for example with PractiSPIN ST7 board) for safe Overcurrent protection

R17, R21 : set the maximum current obtainable through PractiSPIN (see PractiSPIN documentation)

R2 : recommended change to adequate value (depending on supply voltage) to obtain 5V across D3

JP2, JP3 : close for safe Overcurrent protection

JP4, JP5 : close for use with PractiSPIN ST7 board

Figure 38. EVAL6205N Electrical schematic.

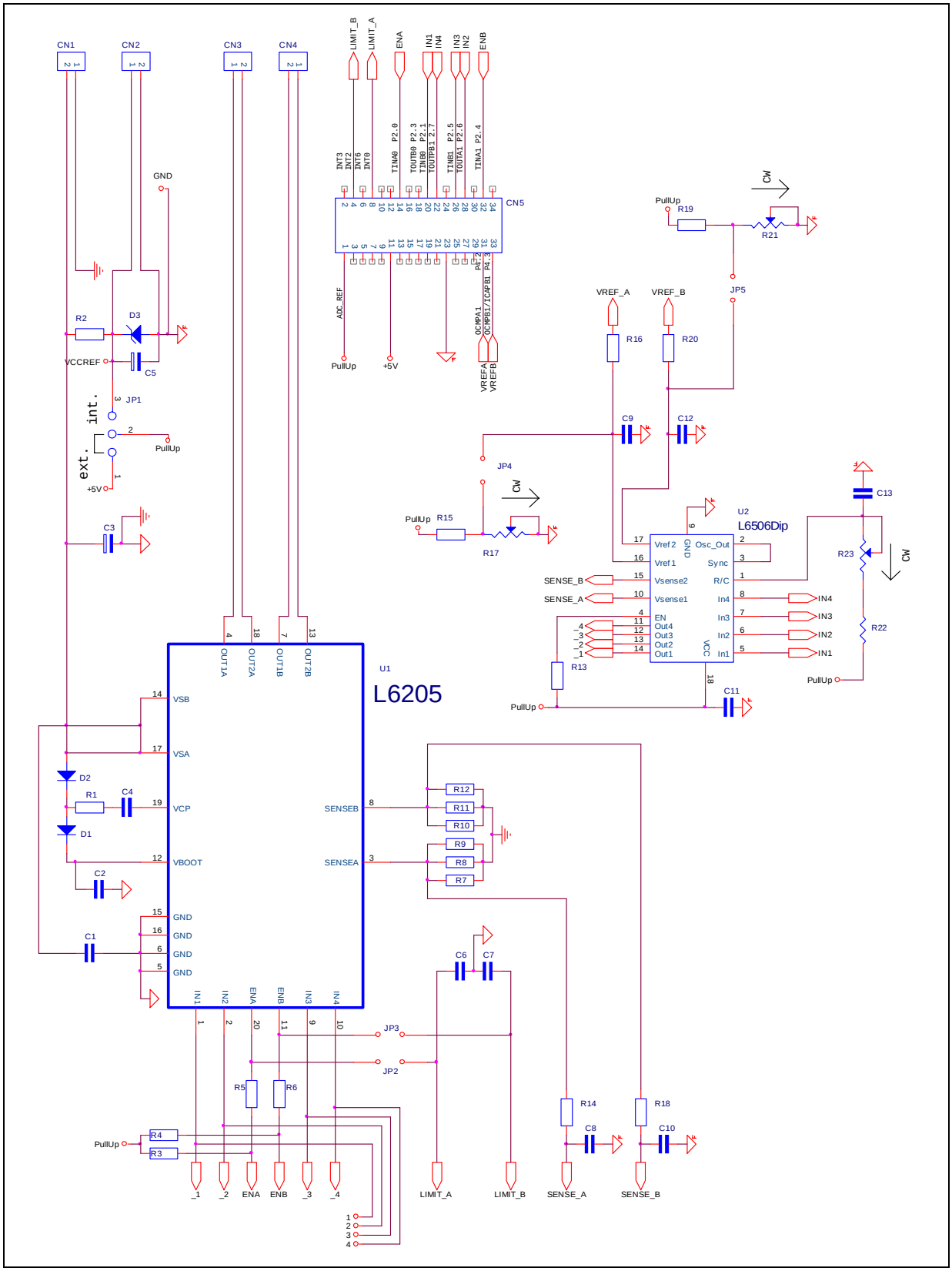


Figure 39. EVAL6205N Component placement.

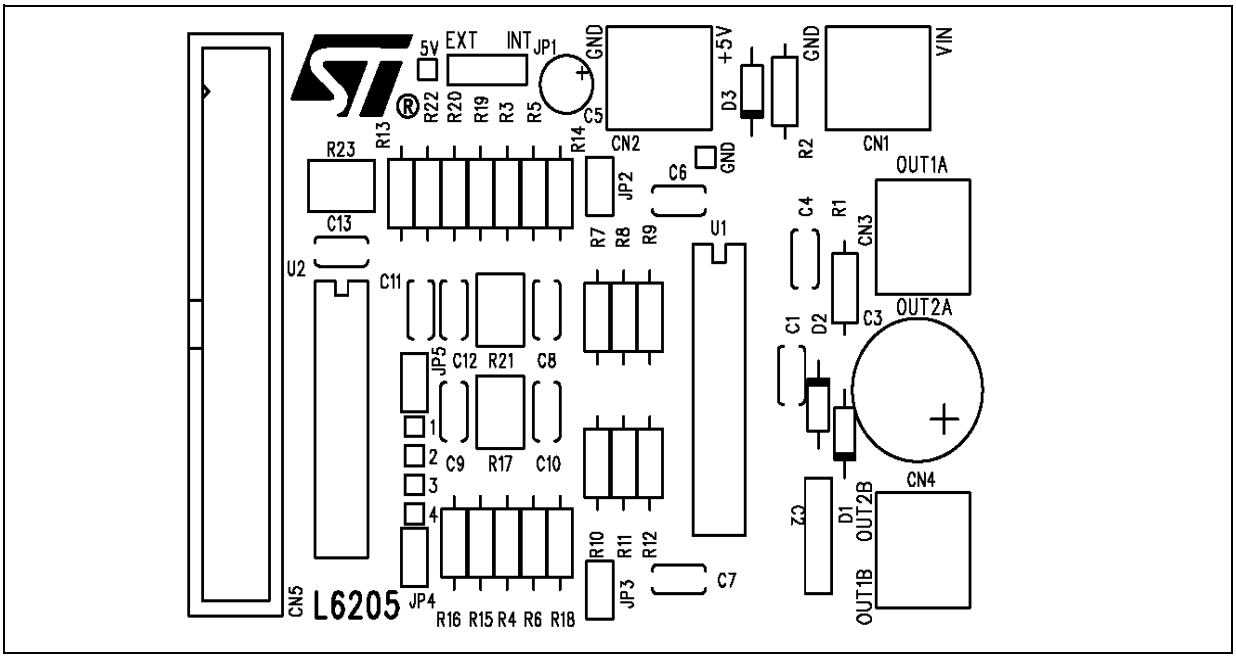


Figure 40. EVAL6205N Top Layer Layout.

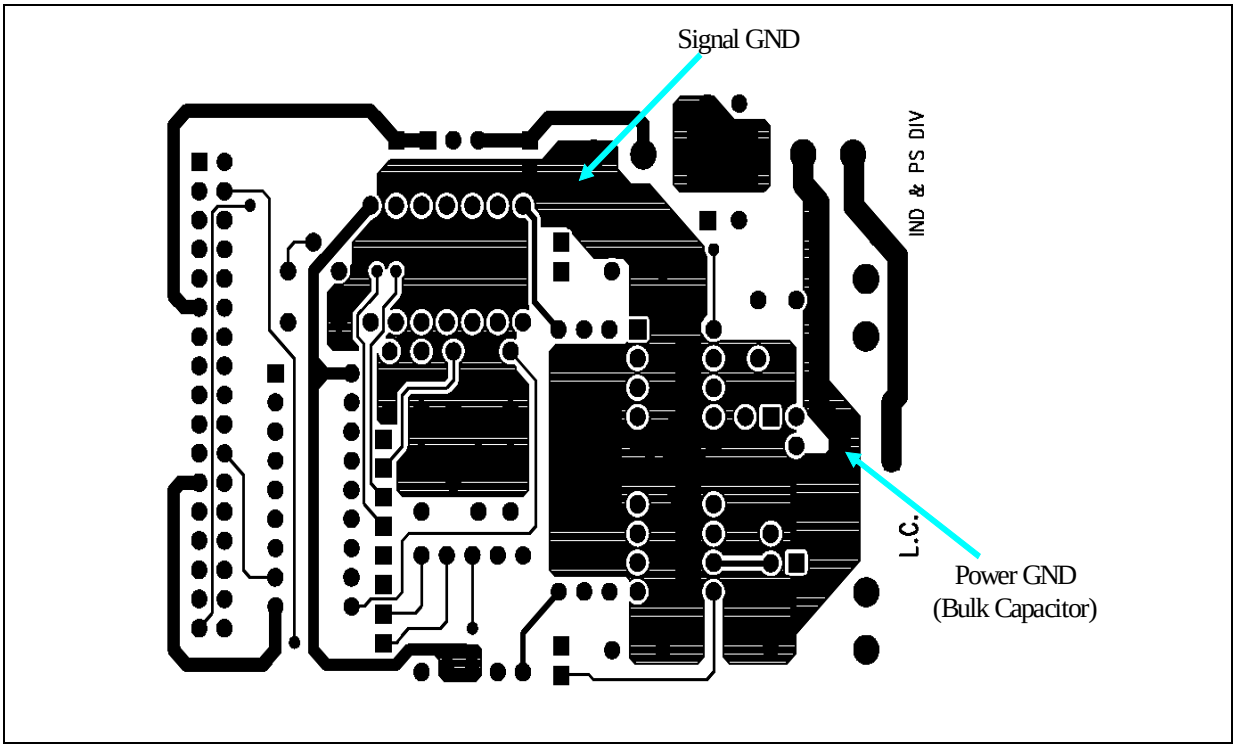
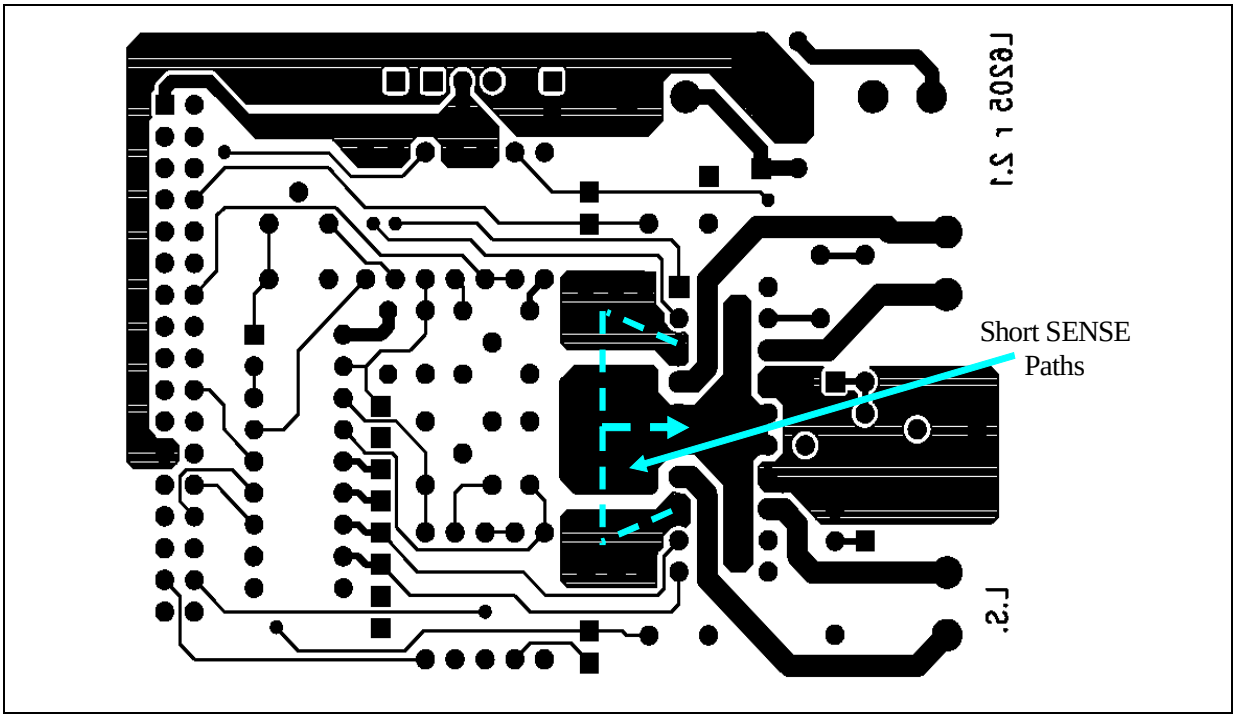


Figure 41. EVAL6205N Bottom Layer Layout.



5.3 EVAL6206N

An evaluation board has been produced to help the evaluation of the device in PowerDIP package. It implements a typical application with several added components. Figure 43 shows the electrical schematic of the board; in the table below the part list is reported.

CN1, CN2, CN3, CN4	2-poles connector	R1	100Ω resistor
CN5	34-poles connector	R2	700Ω 0.6W resistor
C1	220nF/100V Ceramic or Polyester capacitor	R3, R4, R16	10kΩ resistor
C2	220nF/100V Ceramic or Polyester capacitor	R5, R6	4.7kΩ resistor
C3	100µF/63V capacitor	R7, R8	50kΩ trimmer
C4	10nF/100V Ceramic capacitor	R9, R10, R11, R12, R13, R14	1Ω 0.4W resistor
C5, C8, C10	10µF/16V Capacitor	R15, R21	2.2kΩ resistor
C6, C7	47nF Capacitor	R17, R23	20kΩ resistor
C9, C13	68nF Capacitor	R18, R22	750Ω resistor
C11	100nF Capacitor	R19, R25	2.2kΩ resistor
C12, C14	470pF Capacitor	R20, R26	5kΩ trimmer
C15	2.2nF Capacitor	R27, R24	1kΩ resistor
D1, D2	1N4148 Diode	R28	12kΩ resistor
D3	BZX79C5V1 5.1V Zener Diode	R29	50kΩ trimmer
JP1	3-pin jumper	U1	L6205N
JP2 to JP7	2-pin jumper	U2	L6506

The Evaluation Board provides external connectors for the supply voltage, an external 5V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN tool. The board also accomodate the L6506 PWM current controller. R29 sets the PWM operating frequency. If the L6506 does not need to be used, simply connect the two V_{REF} inputs to a voltage high enough to keep current control inactive.

The PractiSPIN tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains an upgradeable firmware. This tool allows a fast and easy evaluation of the PowerSPIN family devices, giving the ability of driving DC, BLDC and Stepper motors, depending on the target device. The PractiSPIN connected to the EVAL6206N can drive DC motors and inductive loads, allowing output voltage and current settings

The PC-software also provides a Power Dissipation and Thermal Analysis section, intended to help a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point designing an application (from the power dissipation and thermal point of view).

Running the evaluation board in stand-alone mode, instead, R20 and R26 set the reference voltage separately for the two bridges, while R19, C9 and R25, C13 are low-pass filters to provide an external reference voltage by a PWM output of a µC (see also the Microstepping section). Using external V_{REF} inputs R17, R20, R23, R26 can be disconnected through JP6 and JP7, unless the PractiSPIN ST7 evaluation board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN documentation).

Closing JP4 and JP5, R7 and R8 allow adjusting the Over Current Detection threshold separately for the two full bridges. Leaving JP4 and JP5 opened, the OCD threshold can be programmed providing reference voltages at the bottom of R7 and R8, through pins 27 and 29 of CN5. R15, R18, C8, R21, R22, C10 provide low-pass filtering to obtain these reference voltages from an external PWM output of a µC.

Closing JP2 and JP3 allows Over Current Protection to work, connecting each *EN* pin to the corresponding *OCD* pin.

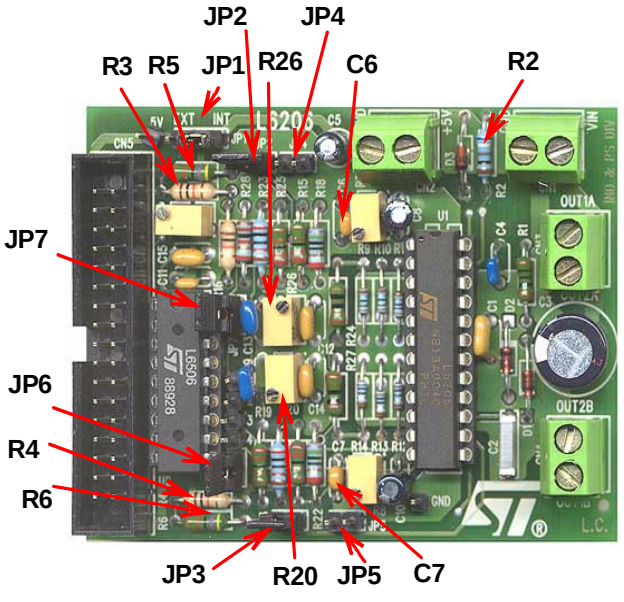
The 5V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R2, D3. Depending on the supply voltage, the value of resistor R2 should be changed in order to ensure a correct biasing of D3.

The jumper JP1 allows choosing the 5V voltage from the internal zener diode network or pin 11 of CN5 (for example an external µC board can provide 5V to the evaluation board). Also CN2 connector can be used to provide an external 5V voltage to the board (in that case R2, D3 should be disconnected). CN2, or pin 1 of CN5,

can also be used to provide a 5V voltage to external circuits (as, for example, the PractiSPIN ST7 board). In this case the current that can be drawn form the board depends on the supply voltage and on R2 value.

Figure 44 to Figure 46 show the component placement and the two layers layout of the L6206N Evaluation Board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 42. EVAL6206N.



5.3.1 Important Notes

JP1 : close in INT position for use with PractiSPIN ST7 board

C6, C7 : recommended change to 5.6 nF for safe Overcurrent protection

R3, R4 : recommended change to 100 k for safe Overcurrent protection

R5, R6 : recommended change to 100 k if EN pins are driven from the CN5 connector (for example with PractiSPIN ST7 board), for safe Overcurrent protection

R20, R26 : set the maximum current obtainable through PractiSPIN (see PractiSPIN documentation)

R2 : recommended change to adequate value (depending on supply voltage) to obtain 5V across D3

JP2, JP3 : close to allow Overcurrent protection

JP4, JP5 : close for on-board OCD threshold adjusting through R7, R8

JP6, JP7 : close for use with PractiSPIN ST7 board

Figure 43. EVAL6206N Electrical schematic.

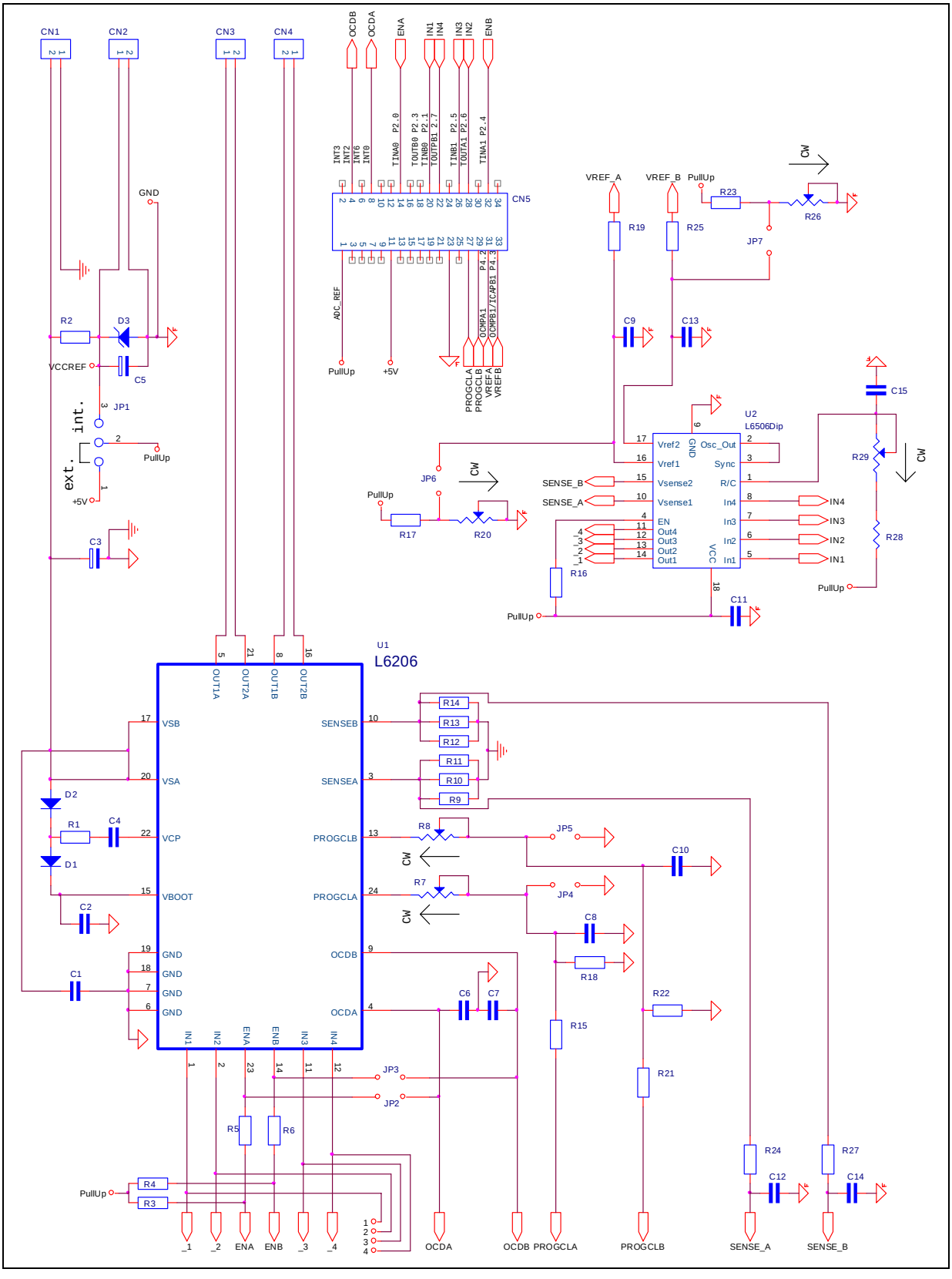


Figure 44. EVAL6206N Component placement.

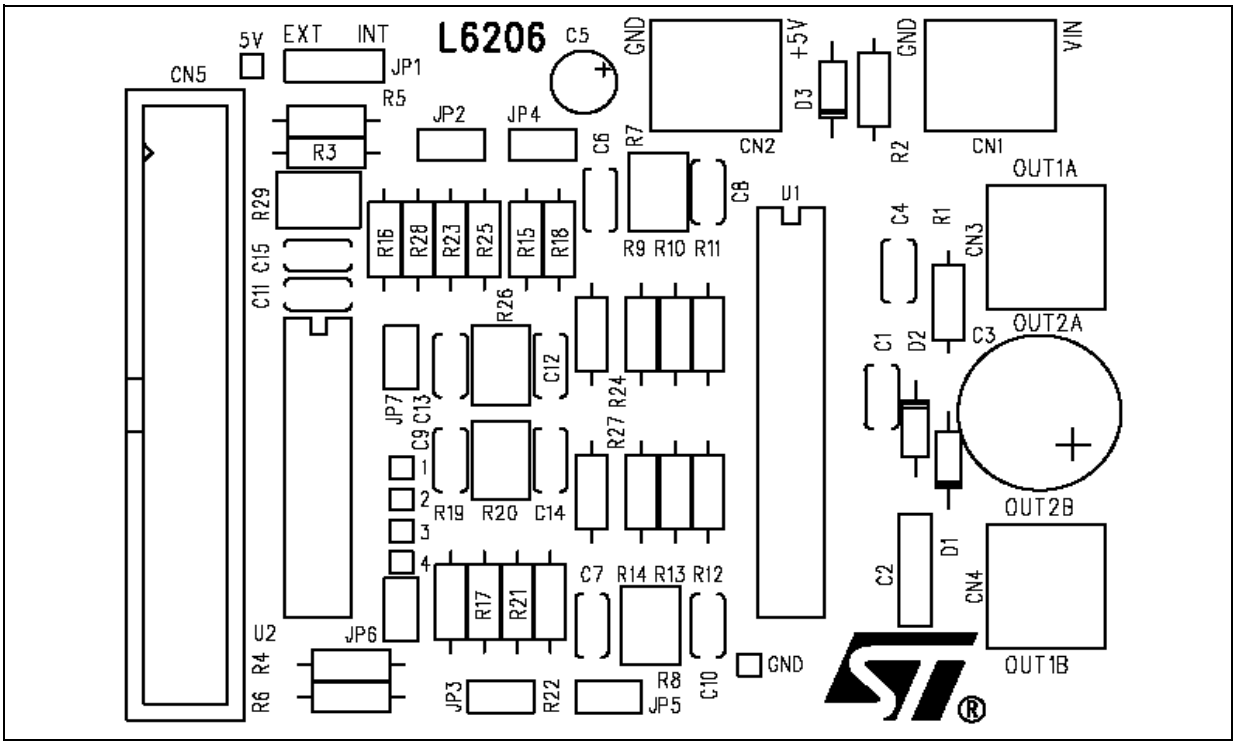


Figure 45. EVAL6206N Top Layer Layout.

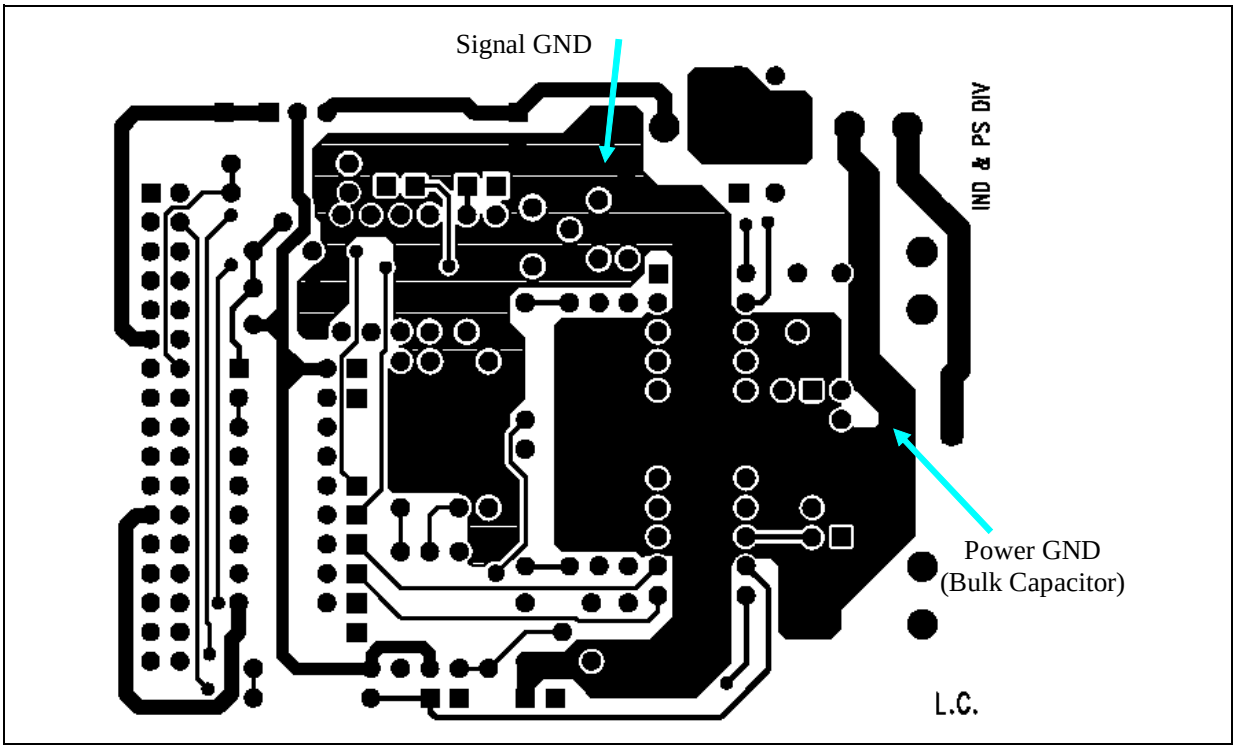
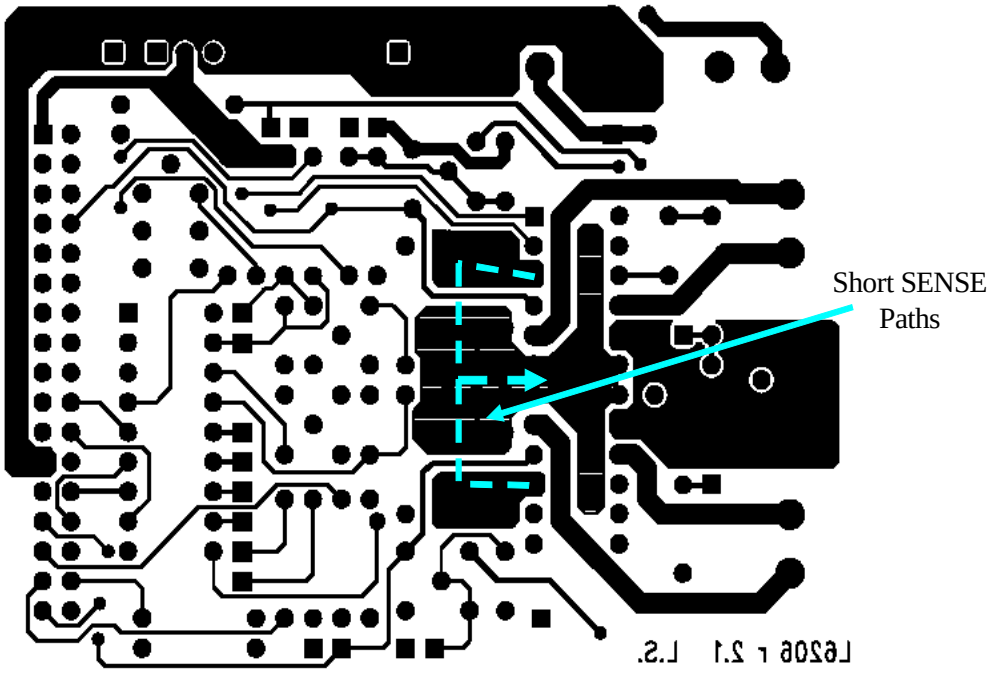


Figure 46. EVAL6206N Bottom Layer Layout.



5.4 EVAL6206PD

An evaluation board has been produced to help the evaluation of the device in PowerSO package. It implements a typical application with several added components. Figure 48 shows the electrical schematic of the board; in the table below the part list is reported.

CN1, CN2, CN3, CN4	2-poles connector	JP2 to JP5	2-pin jumper
CN5	34-poles connector	R1	750Ω 0.6W resistor
C1	220nF/100V Ceramic or Polyester capacitor	R2, R3, R26	10kΩ resistor
C2	220nF/100V Ceramic or Polyester capacitor	R4, R5	4.7kΩ resistor
C3	100µF/63V capacitor	R6, R7	50kΩ trimmer
C4	10nF/100V Ceramic capacitor	R8, R9, R10, R11	0.4Ω 1W resistor
C5, C8, C10	10µF/16V Capacitor	R12, R19	20kΩ resistor
C6, C7	100nF Capacitor	R13, R14, R17, R20	2.2kΩ resistor
C9, C13	68nF Capacitor	R15, R18	750Ω resistor
C11	100nF Capacitor	R16, R22	5kΩ trimmer
C12, C15	470pF Capacitor	R23, R21	1kΩ resistor
C14	2.2nF Capacitor	R24	12kΩ resistor
D1	Bat46SW Diodes	R25	50kΩ trimmer
D2	BZX79C5V1 5.1V Zener Diode	U1	L6205N
JP1	3-pin jumper	U2	L6506

The Evaluation Board provides external connectors for the supply voltage, an external 5V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN tool. The board also accomodate the L6506 PWM current controller. R25 sets the PWM operating frequency. If the L6506 does not need to be used, simply connect the two V_{REF} inputs to a voltage high enough to keep current control inactive.

The PractiSPIN tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains an upgradeable firmware. This tool allows a fast and easy evaluation of the PowerSPIN family devices, giving the ability of driving DC, BLDC and Stepper motors, depending on the target device. The PractiSPIN connected to the EVAL6206PD can drive DC motors and inductive loads, allowing output voltage and current settings

The PC-software also provides a Power Dissipation and Thermal Analysis section, intended to help a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point designing an application (from the power dissipation and thermal point of view).

Running the evaluation board in stand-alone mode, instead, R16 and R22 set the reference voltage separately for the two bridges, while R14, C9 and R20, C13 are low-pass filters to provide an external reference voltage by a PWM output of a µC (see also the Microstepping section). Using external V_{REF} inputs R12, R16, R19, R22 should be disconnected, unless the PractiSPIN ST7 evaluation board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN documentation).

Closing JP4 and JP5, R6 and R7 allow adjusting the Over Current Detection threshold separately for the two full bridges. Leaving JP4 and JP5 opened, the OCD threshold can be programmed providing reference voltages at the bottom of R6 and R7, through pins 27 and 29 of CN5. R13, R15, C8, R17, R18, C10 provide low-pass filtering to obtain these reference voltages from an external PWM output of a µC.

Closing JP2 and JP3 allows Over Current Protection to work, connecting each *EN* pin to the corresponding *OCD* pin.

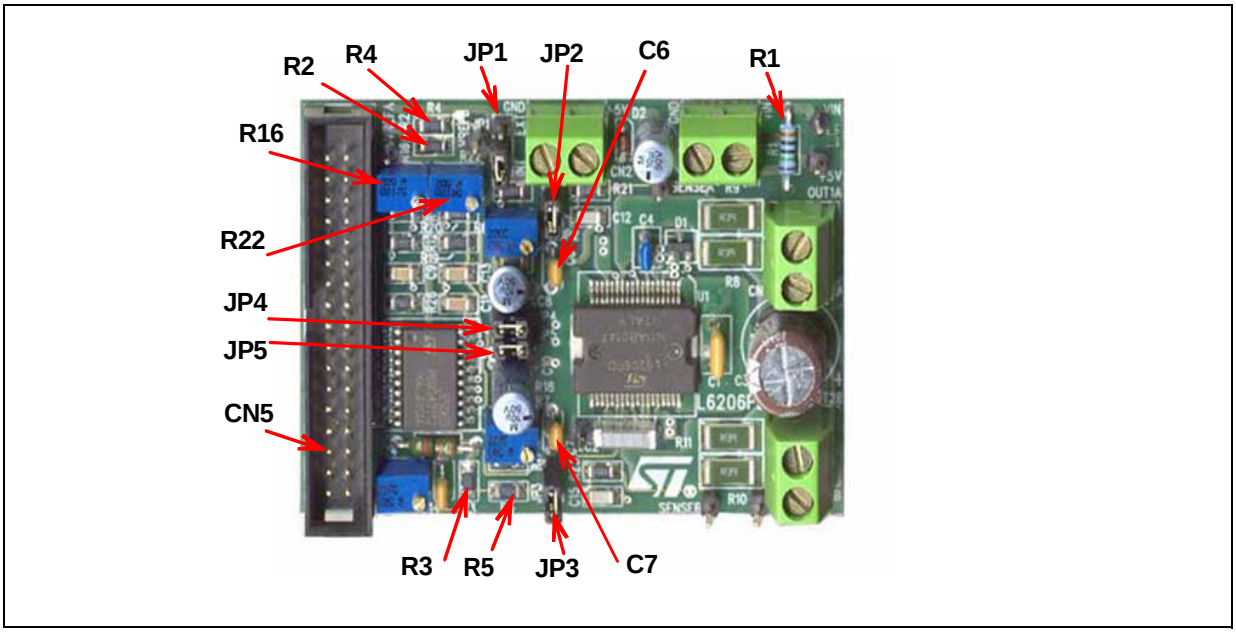
The 5V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R1, D2. Depending on the supply voltage, the value of resistor R1 should be changed in order to ensure a correct biasing of D2.

The jumper JP1 allows choosing the 5V voltage from the internal zener diode network or pin 11 of CN5 (for example an external µC board can provide 5V to the evaluation board). Also CN2 connector can be used to provide an external 5V voltage to the board (in that case R1, D2 should be disconnected). CN2, or pin 1 of CN5, can also be used to provide a 5V voltage to external circuits (as, for example, the PractiSPIN ST7 board). In this

case the current that can be drawn form the board depends on the supply voltage and on R1 value.

Figure 49 to Figure 51 show the component placement and the two layers layout of the L6206PD Evaluation Board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 47. EVAL6206PD.



5.4.1 Important Notes

JP1 : close in INT position for use with PractiSPIN ST7 board

C6, C7 : recommended change to 5.6 nF for safe Overcurrent protection

R2, R3 : recommended change to 100 k for safe Overcurrent protection

R4, R5 : recommended change to 100 k if EN pins are driven from the CN5 connector (for example with PractiSPIN ST7 board) for safe Overcurrent protection

R16, R22 : set the maximum current obtainable through PractiSPIN (see PractiSPIN documentation)

R1 : recommended change to adequate value (depending on supply voltage) to obtain 5V across D2

JP2, JP3 : close to allow Overcurrent protection

JP4, JP5 : close for on-board OCD threshold adjusting through R6, R7

CN5 : VrefA and VrefB positions are inverted if compared to other EVAL62XX boards.

Figure 48. EVAL6206PD Electrical schematic.

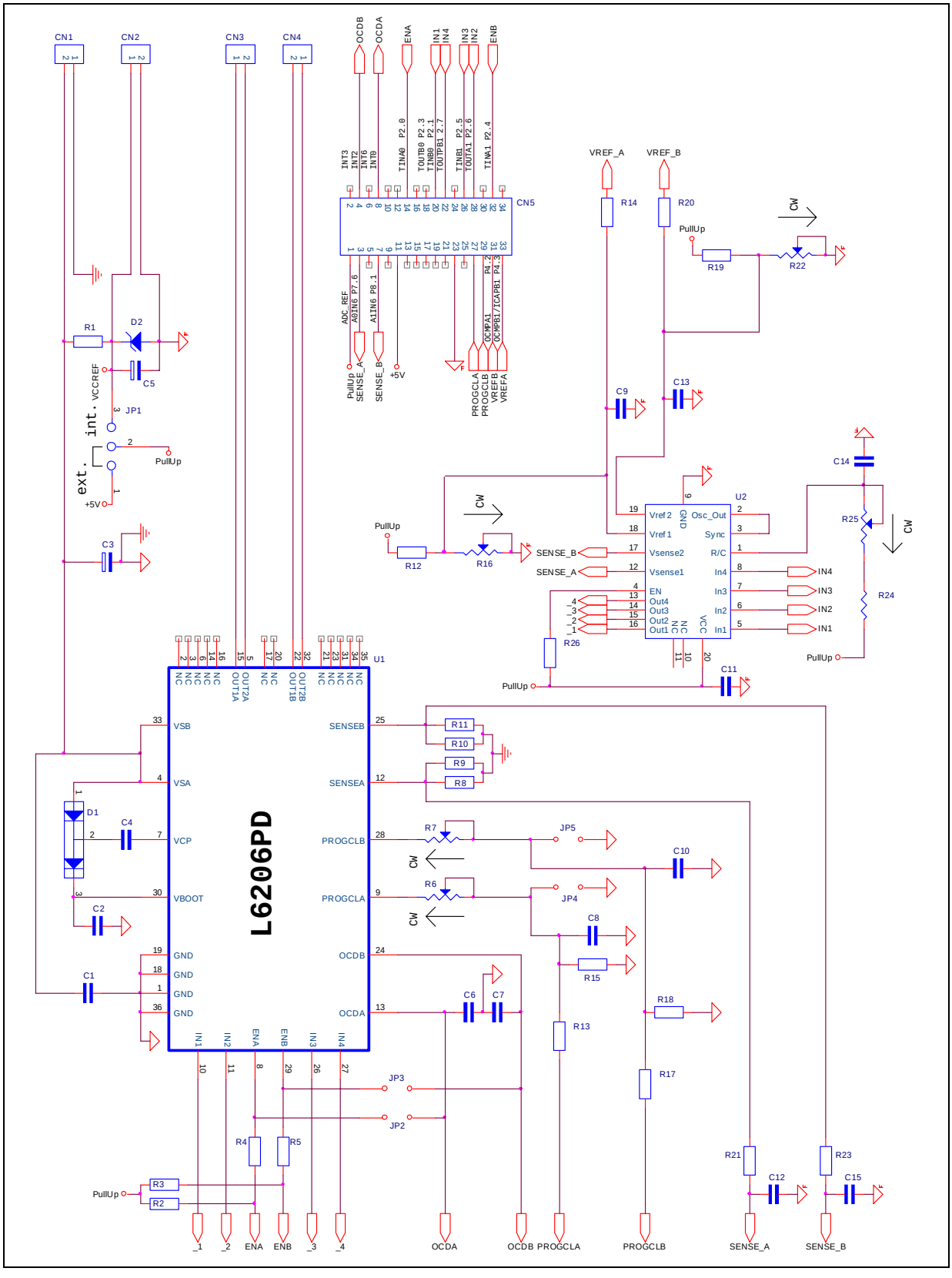


Figure 49. EVAL6206PD Component placement.

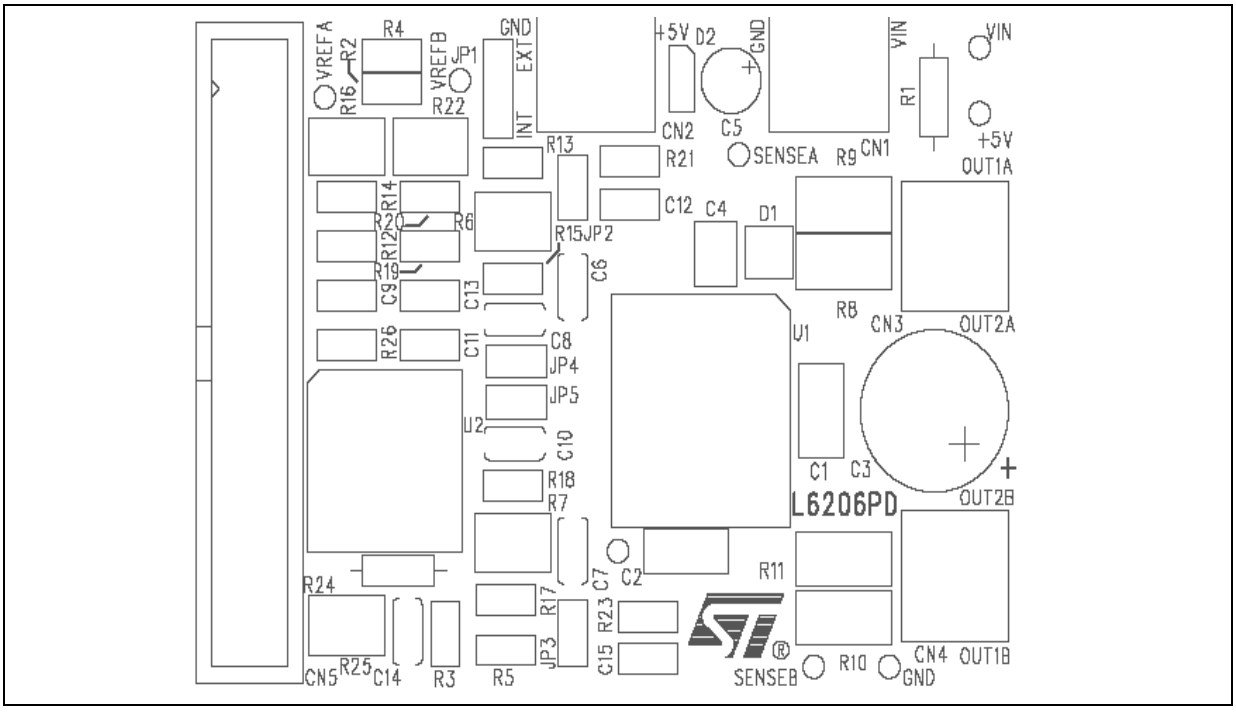


Figure 50. EVAL6206PD Top Layer Layout.

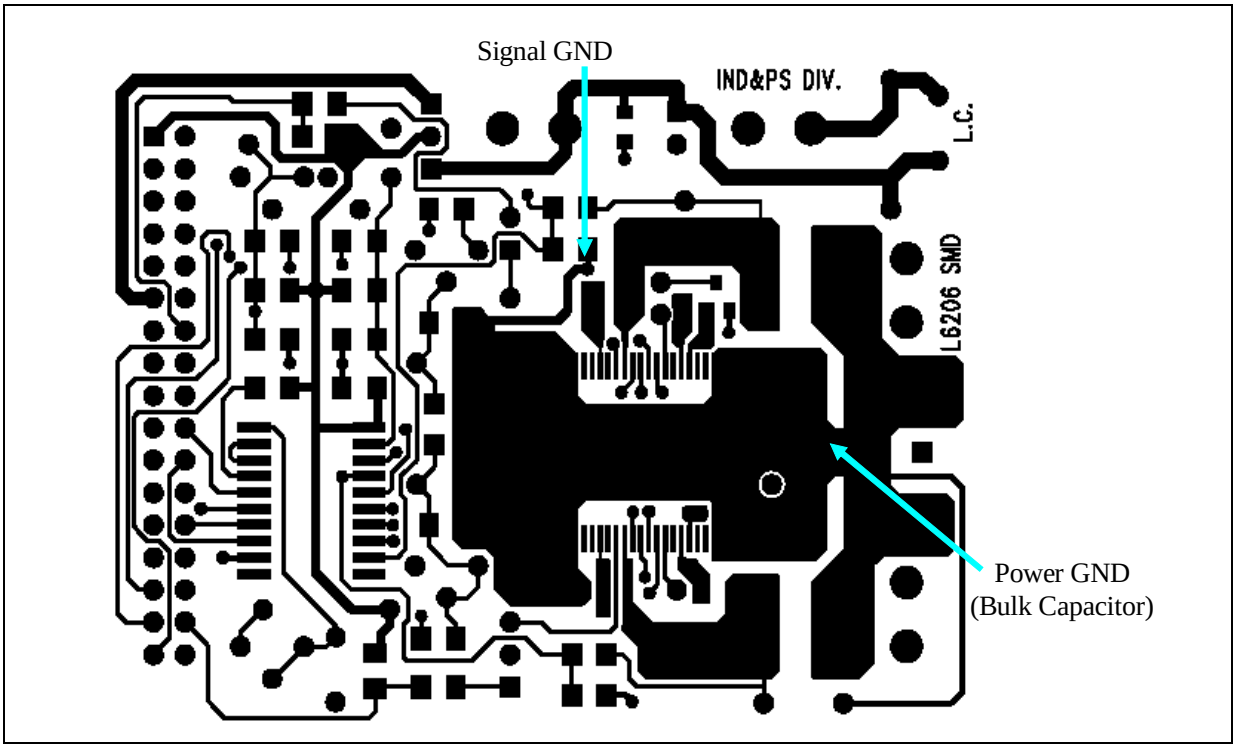
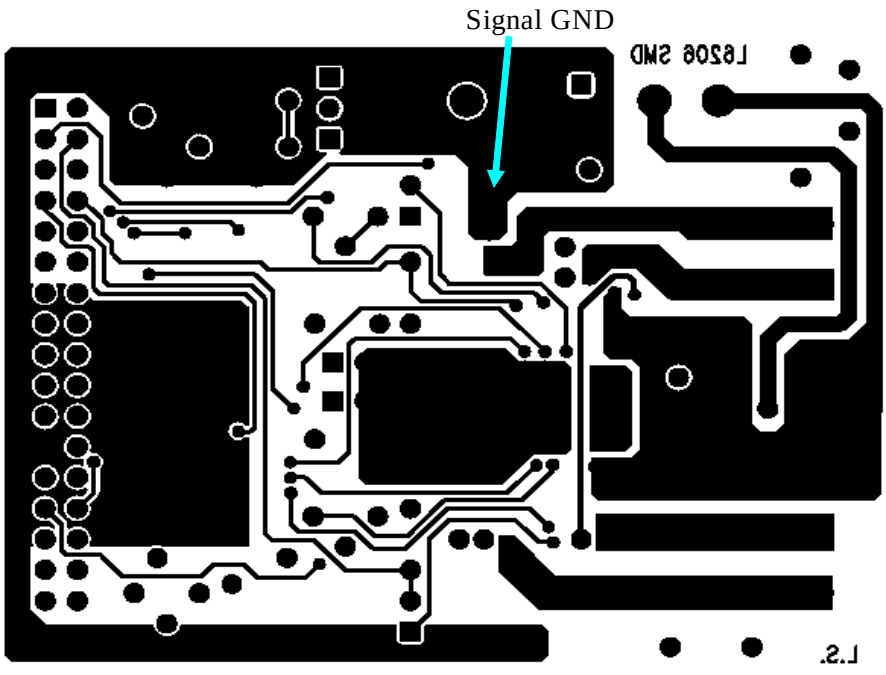


Figure 51. EVAL6206PD Bottom Layer Layout.



5.5 EVAL6207N

An evaluation board has been produced to help the evaluation of the device in PowerDIP package. It implements a typical application with several added components. Figure 53 shows the electrical schematic of the board; in the table below the part list is reported.

CN1, CN2, CN3, CN4	2-poles connector	JP1	3-pin jumper
CN5	34-poles connector	JP2, JP3	2-pin jumper
C1	220nF/100V Ceramic or Polyester capacitor	R1	100Ω resistor
C2	220nF/100V Ceramic or Polyester capacitor	R2	3.17kΩ 0.6W resistor
C3	100µF/63V capacitor	R3, R4	4.7kΩ resistor
C4	10nF/100V Ceramic capacitor	R5, R16	20kΩ resistor
C5	10µF/16V Capacitor	R6, R7	100kΩ trimmer
C6, C7	100nF Capacitor	R8, R17	2.2kΩ 0.4W resistor
C8, C9	68nF Capacitor	R9 to R14	1Ω 0.4Ω resistor
C10, C11	820pF Capacitor	R18, R15	5kΩ trimmer
D1, D2	1N4148 Diode	U1	L6205N
D3	BZX79C5V1 5.1V Zener Diode	U2	L6506

The Evaluation Board provides external connectors for the supply voltage, an external 5V reference for the logic inputs, four outputs for the motor and a 34-pin connector to control the main functions of the board through an external µC board or the PractiSPIN tool.

The PractiSPIN tool is composed of a graphic interface software running on a PC that connects with the hardware based on the ST7 µC, which contains an upgradeable firmware. This tool allows a fast and easy evaluation of the PowerSPIN family devices, giving the ability of driving DC, BLDC and Stepper motors, depending on the target device. The PractiSPIN connected to the EVAL6207N can drive DC motors and inductive loads, allowing output voltage and current settings

The PC-software also provides a Power Dissipation and Thermal Analysis section, intended to help a fast evaluation of the device, package and dissipating copper area required by the user's application, and to be a good starting point designing an application (from the power dissipation and thermal point of view).

Running the evaluation board in stand-alone mode, instead, R15 and R18 set the reference voltage separately for the two bridges, while R8, C8 and R17, C9 are low-pass filters to provide an external reference voltage by a PWM output of a µC (see also the Microstepping section). Using external V_{REF} inputs R5, R15, R16, R18 should be disconnected, unless the PractiSPIN ST7 evaluation board is used. This board, in fact, is provided with an offset cancellation circuitry trimmable through a potentiometer (see PractiSPIN documentation).

R6, C10 and R7, C11 are used to set the off-time of the two channels of the IC.

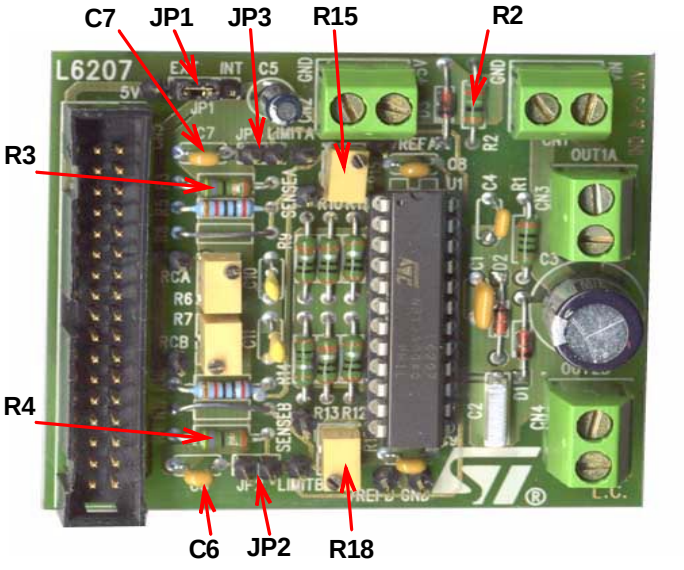
Closing JP2 and JP3 is recommended for safe Over Current Protection.

The 5V voltage for logic inputs and for references (V_{refA} and V_{refB}) is obtained from R2, D3. Depending on the supply voltage, the value of resistor R2 should be changed in order to ensure a correct biasing of D3.

The jumper JP1 allows choosing the 5V voltage from the internal zener diode network or pin 11 of CN5 (for example an external µC board can provide 5V to the evaluation board). Also CN2 connector can be used to provide an external 5V voltage to the board (in that case R2, D3 should be disconnected). CN2, or pin 1 of CN5, can also be used to provide a 5V voltage to external circuits (as, for example, the PractiSPIN ST7 board). In this case the current that can be drawn form the board depends on the supply voltage and on R2 value.

Figure 54 to Figure 56 show the component placement and the two layers layout of the L6207N Evaluation Board. A large GND area has been used, to guarantee minimal noise and good power dissipation for the device.

Figure 52. EVAL6207N.



5.5.1 Important Notes

JP1 : close in INT position for use with PractiSPIN ST7 board

C6, C7 : recommended change to 5.6 nF for safe Overcurrent protection

R3, R4 : recommended change to 100 k for safe Overcurrent protection

R15, R18 : set the maximum current obtainable through PractiSPIN (see PractiSPIN documentation)

R2 : recommended change to adequate value (depending on supply voltage) to obtain 5V across D3

JP2, JP3 : close for safe Overcurrent protection

Figure 53. EVAL6207N Electrical schematic.

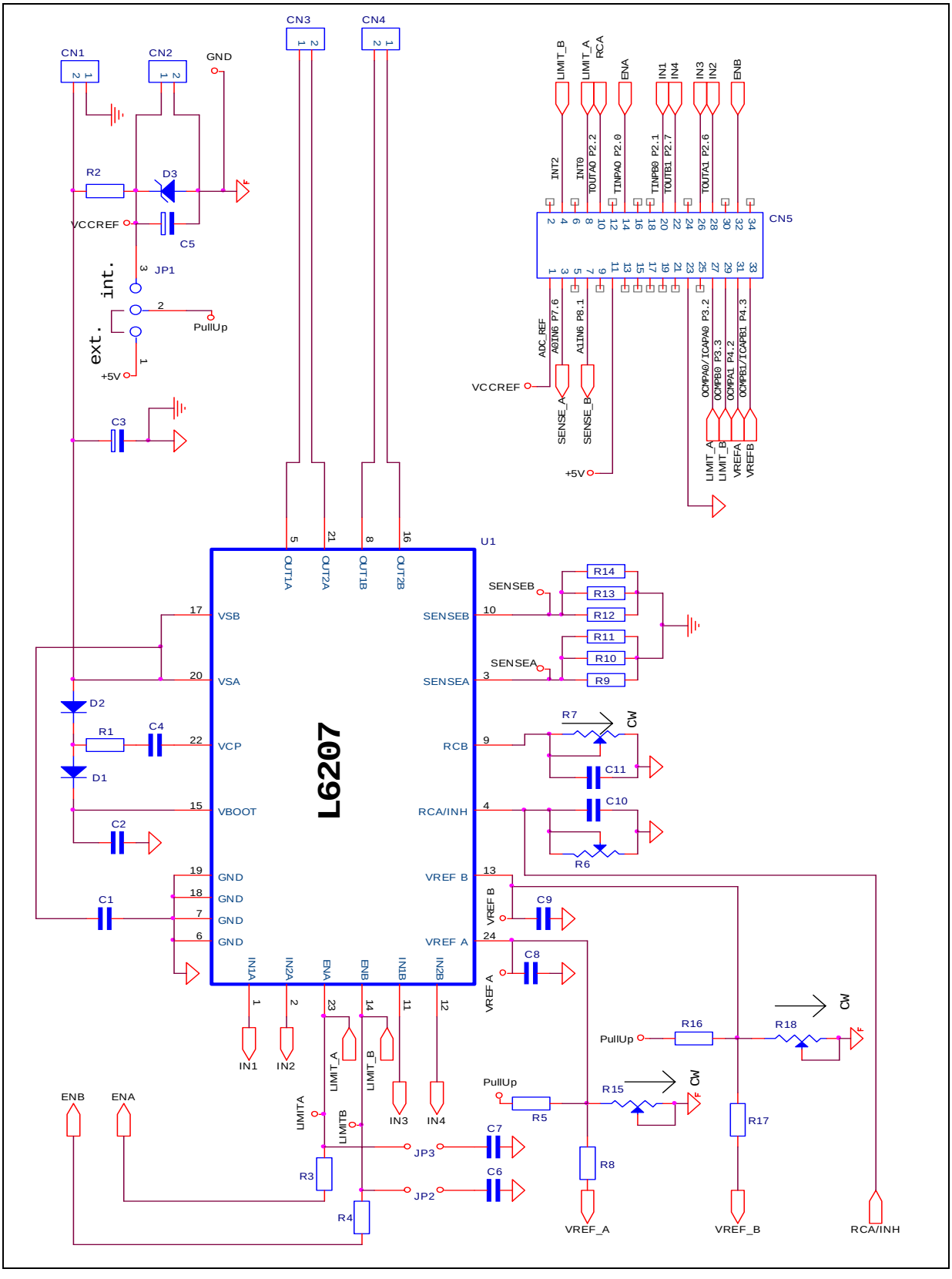


Figure 54. EVAL6207N Component placement.

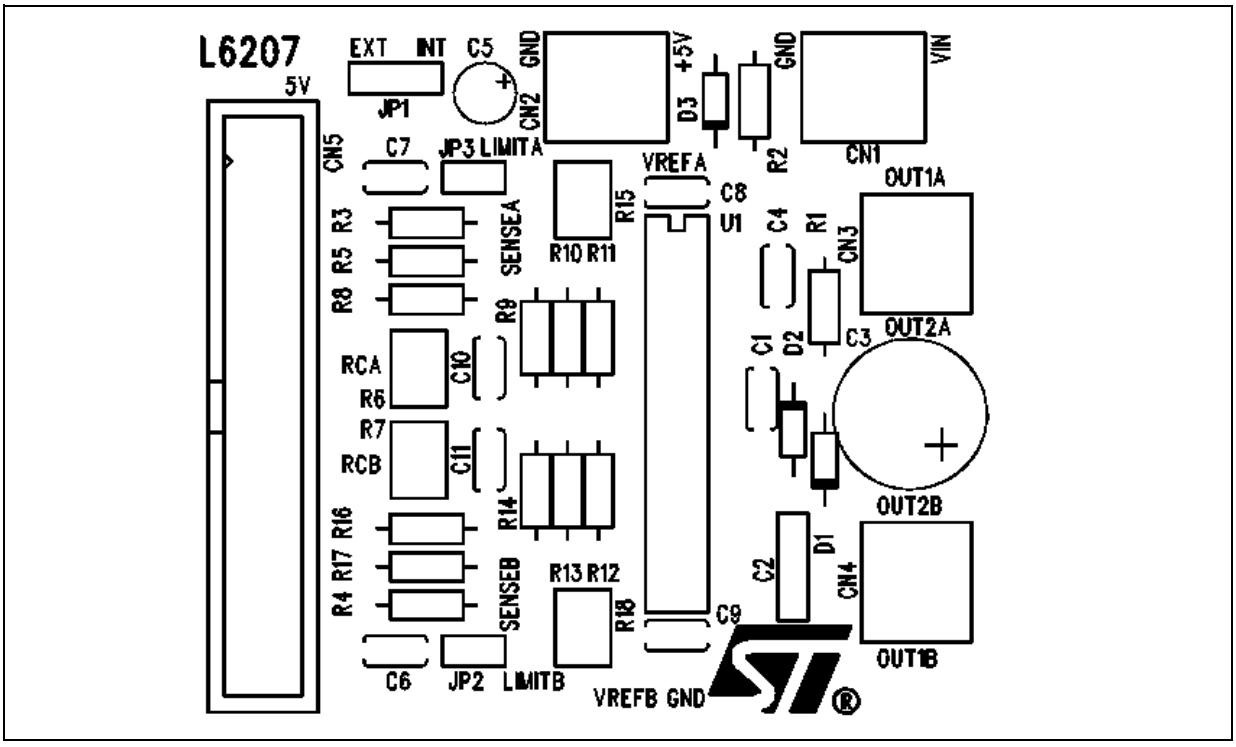


Figure 55. EVAL6207N Top Layer Layout.

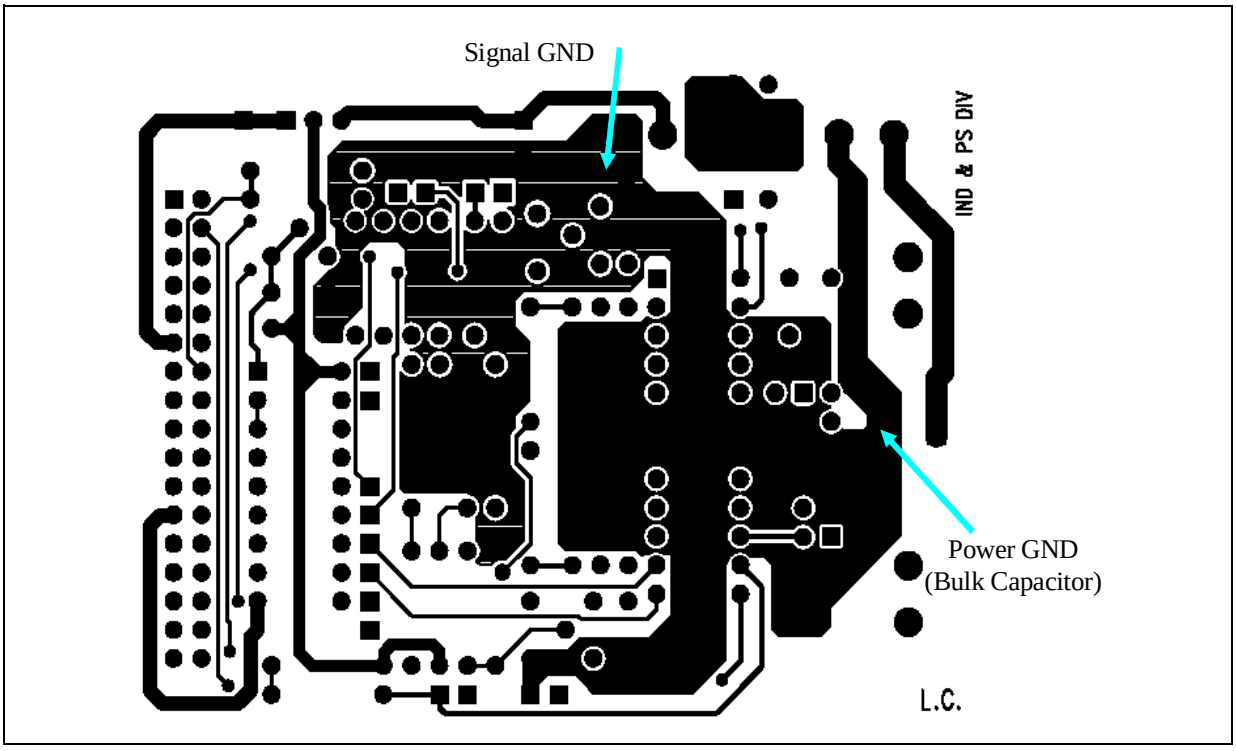
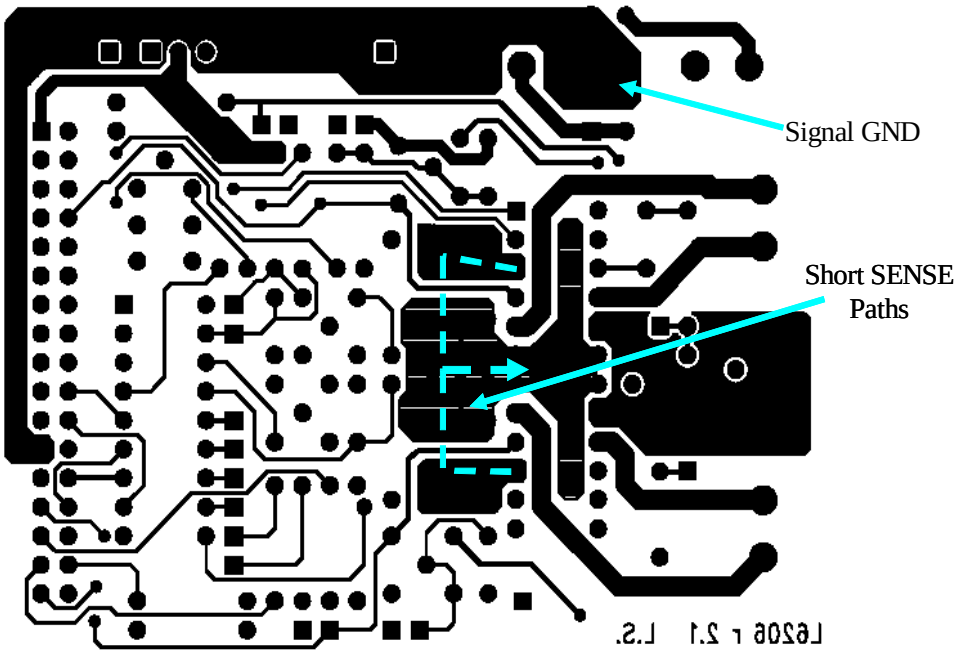


Figure 56. EVAL6207N Bottom Layer Layout.



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