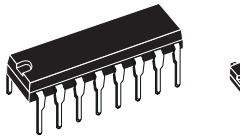
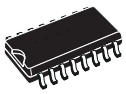
M74HC4520

DUAL 4 BIT BINARY COUNTER

- HIGH SPEED :
  f_{MAX} = 60 MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} =4μA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 4520



DIP



SOP

TSSOP

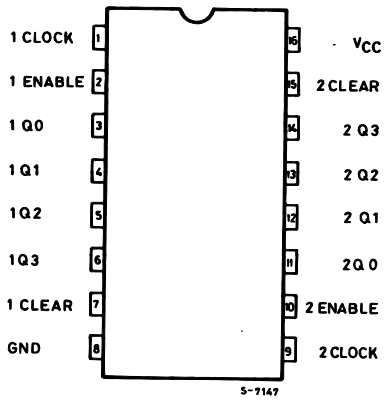
ORDER CODES

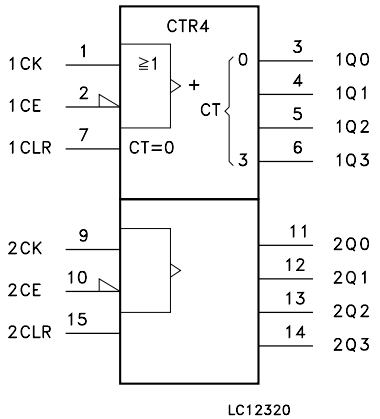
PACKAGE	TUBE	T & R
DIP	M74HC4520B1R	
SOP	M74HC4520M1R	M74HC4520RM13TR
TSSOP		M74HC4520TTR

DESCRIPTION

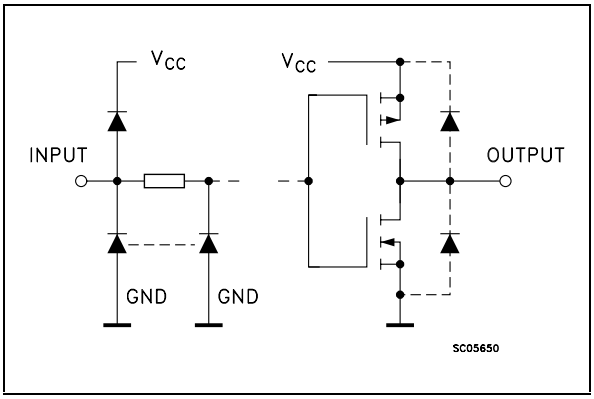
The M74HC4520 is an high speed CMOS DUAL BINARY COUNTER fabricated with silicon gate C^2MOS technology.
It consists of two identical internally synchronous 4-stage counters. The counter stages are D-TYPE flip-flops having interchangeable CLOCK and ENABLE inputs for incrementing on either the positive-going or negative-going transition.
For single-unit operation the ENABLE input is maintained "high" and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their clear lines.
The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held permanently low.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

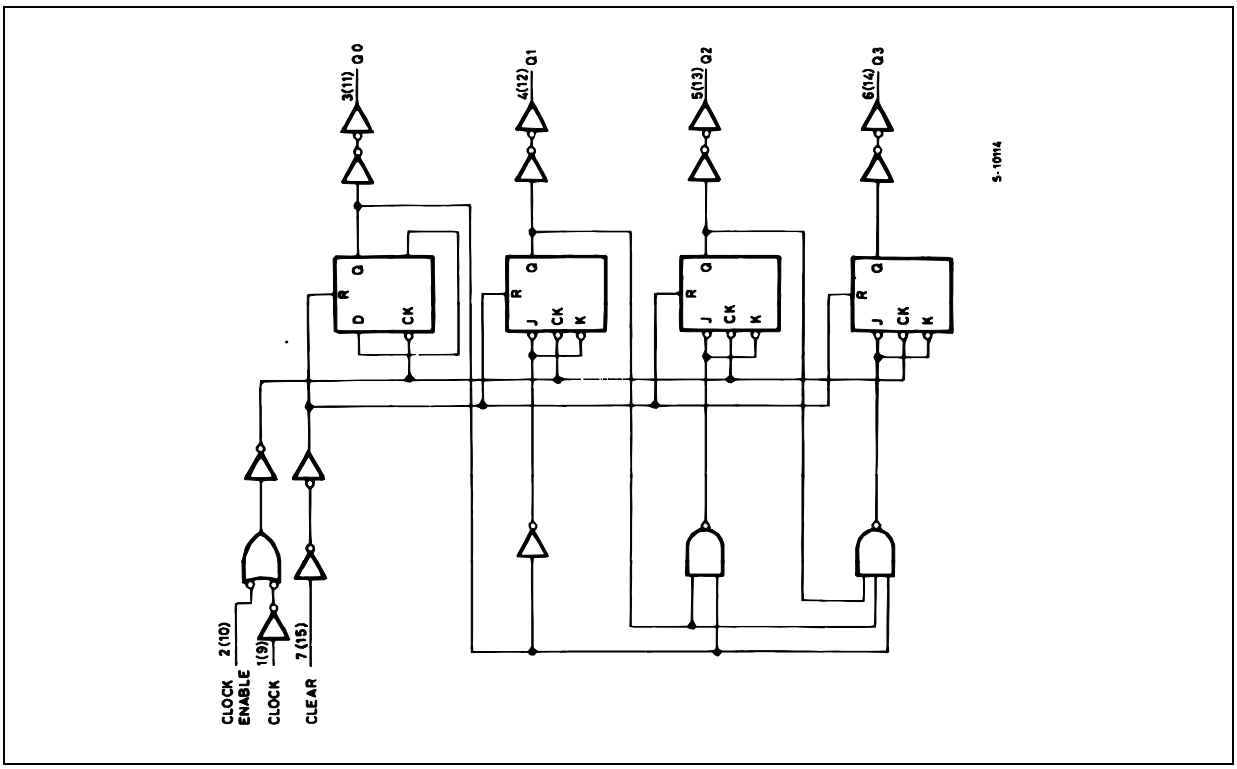
PIN No	SYMBOL	NAME AND FUNCTION
1, 9	1CLOCK, 2CLOCK	Clock Inputs (LOW to HIGH, Edge-Triggered)
2, 10	1CE, 2CE	Clock Enable Inputs
3, 4, 5, 6	1Q0 to 1Q3	Data Outputs
7, 15	1CLEAR, 2CLEAR	Asynchronous Reset Inputs (Active LOW)
11, 12, 13, 14	2Q0 tO 2Q3	Data Outputs
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

INPUTS			FUNCTION
CLOCK	CLOCK ENABLE	CLEAR	
⎍	H	L	INCREMENT COUNTER
L	⎎	L	INCREMENT COUNTER
⎎	X	L	NO CHANGE
X	⎍	L	NO CHANGE
⎍	L	L	NO CHANGE
H	⎎	L	NO CHANGE
X	X	H	Q0 THRU Q3=L

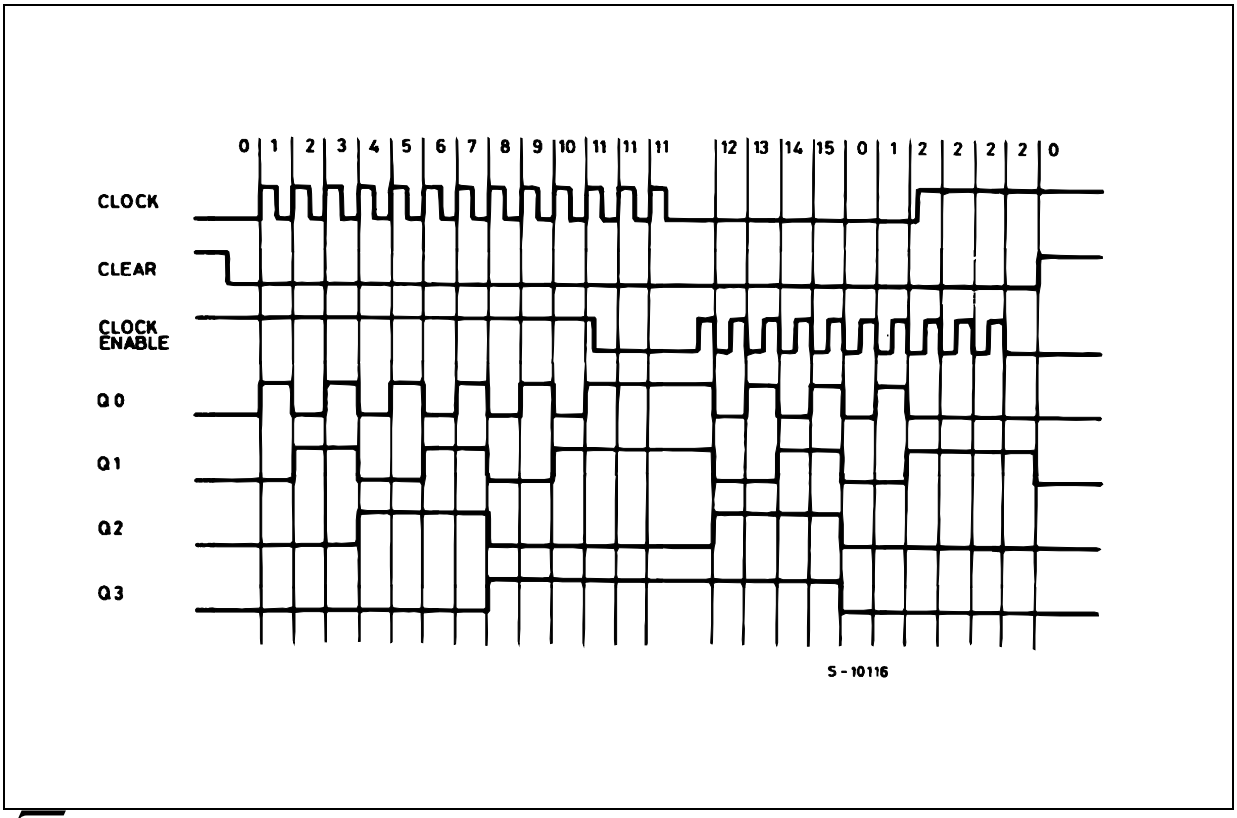
X : Don't Care
Z : High Impedance

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns