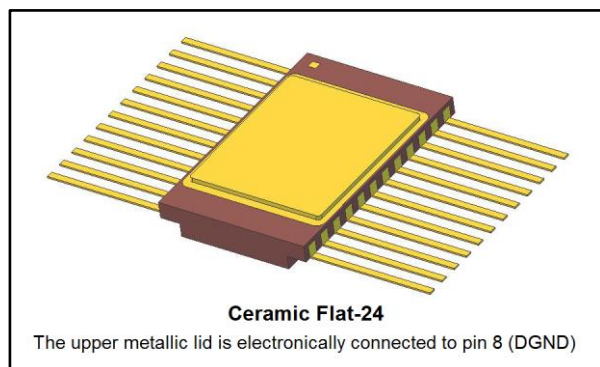


Rad-hard high resolution DAC

Datasheet - production data



Features

- $\Sigma\Delta$ DAC
- 16-bit resolution at 3 kHz bandwidth
- External master clock: 2.4 to 3.6 MHz
- Internal master clock: 3 MHz
- Sampling frequency: 12 ksp/s at 3 MHz master clock
- Serial peripheral interface (SPI)
- Selectable input format: straight binary or two's complement
- Internally filtered, single-ended output voltage
- Output feedback pin dedicated for high precision sensing
- 1.8 V/3.3 V digital interfaces
- 3 V to 3.6 V analog supply
- Compatible with the RHF100 1.2 V Vref
- Power-down mode
- 100 krad MIL-STD-883 1019.7
- SEL immune (up to 120 MeV.cm²/mg)
- SEU characterized

Applications

- Space applications
- Telemetry
- Interferometry
- High-accuracy instrumentation

Description

The RHRDAC1612 is a very low-noise, low-frequency, radiation hardened DAC optimized to operate in a bandwidth up to 3 kHz. This DAC has a sigma-delta architecture which provides superior linearity performance and features a very good signal-to-noise ratio of 96 dB@3 kHz.

The DAC operates with a standard SPI input data which it converts into single-ended, internally-filtered voltage outputs. The SPI interface allows write and read mode implementations.

Specifically designed to optimize precision over power consumption, the RHRDAC1612 only dissipates 15 mW at 12 ksp/s clocking.

Table 1: Device summary

Parameter	RH-DAC1612K1	RHRDAC1612K01V
SMD ⁽¹⁾	—	5962R16211
Quality level	Engineering model	QML-V Flight model
Package	Flat-24	
Mass	1.25 g	
Temperature range	-55 °C to 125 °C	

Notes:

⁽¹⁾SMD = standard microcircuit drawing

Contents

1	Functional description	6
2	Pin description	7
3	Radiations	9
	3.1 Total ionizing dose (TID)	9
	3.2 Heavy ions	9
4	DAC operation	11
	4.1 SPI interface.....	11
	4.1.1 SPI frame format	11
	4.1.2 SPI write sequence.....	12
	4.1.3 SPI read sequence	12
	4.2 DAC configuration registers	13
	4.3 DAC register data update options	15
	4.4 DAC transfer function.....	16
	4.5 External Vref power-up sequence	17
	4.6 DAC operation flow charts	19
	4.7 ARSTN and PDN digital pin functions	21
	4.8 Power-on-reset (POR) feature	21
	4.9 Power supply sequencing	21
	4.10 Setting the RHRDAC1612.....	22
	4.11 SYNC OUT pin.....	23
	4.12 Output feedback pin	23
	4.13 Pull-up and pull-down on digital inputs.....	24
	4.14 Anti-aliasing output filter design	24
	4.15 Auto-calibration feature	25
	4.16 VREFIN input	27
	4.17 VREFOUT output.....	28
	4.18 TESTA and TESTD pins	28
5	Absolute maximum ratings and operating conditions	29
6	Electrical characteristics	31
7	Electrical characteristic curves	38
8	Package information	43
	8.1 Ceramic Flat-24 package information	44

9	Ordering information.....	45
10	Revision history	46

List of tables

Table 1: Device summary	1
Table 2: External filter components	6
Table 3: Pin descriptions	7
Table 4: Radiation performance of the RHRDAC1612.....	9
Table 5: DAC configuration bits and function	13
Table 6: Transfer function.....	16
Table 7: Truth table of ARSTN and PDN.....	21
Table 8: Control bit possibilities	22
Table 9: Pull-up and pull-down pin assignments	24
Table 10: VREFOUT behavior vs. PDN and ARSTN	28
Table 11: Absolute maximum ratings	29
Table 12: Operating conditions (Tamb from -55 °C to 125 °C)	29
Table 13: Electrical characteristics	31
Table 14: Timing characteristics	33
Table 15: Ceramic Flat-24 mechanical data	44
Table 16: Order codes	45
Table 17: Document revision history	46

List of figures

Figure 1: Block diagram	6
Figure 2: Typical application schematic	6
Figure 3: Pin locations	7
Figure 4: SPI interface connections for stand-alone operations	11
Figure 5: SPI frame format	11
Figure 6: Address 01h in binary	11
Figure 7: SPI write sequence	12
Figure 8: SPI read sequence	12
Figure 9: Data and control frame format	13
Figure 10: Connections between the DAC and the master	15
Figure 11: Asynchronous DAC data update	15
Figure 12: Synchronous DAC data update	16
Figure 13: Data frame input	16
Figure 14: Internal switches for boost sequence	17
Figure 15: Boost sequence	18
Figure 16: DAC operation flow chart (main)	19
Figure 17: DAC operation flow chart (continued)	20
Figure 18: Another connection for C2	24
Figure 19: Simplified RHRDAC1612 output stage	25
Figure 20: Simplified schematic of output stage with auto-calibration feature	26
Figure 21: Output voltage behavior during calibration	27
Figure 22: DAC timing diagram 1	35
Figure 23: DAC timing diagram 2	36
Figure 24: DAC timing diagram 3	37
Figure 25: INL vs. input code, internal master clock, AVCC = 3.3 V	38
Figure 26: DNL vs. input code, internal master clock, AVCC = 3.3 V	38
Figure 27: INL vs. input code, external master clock, AVCC = 3.3 V	38
Figure 28: DNL vs. input code, external master clock, AVCC = 3.3 V	38
Figure 29: INL vs. input code, internal master clock, AVCC = 3 V	39
Figure 30: DNL vs. input code, internal master clock, AVCC = 3 V	39
Figure 31: INL vs. input code, internal master clock, AVCC = 3.6 V	39
Figure 32: DNL vs. input code, internal master clock, AVCC = 3.6 V	39
Figure 33: INL vs. input code vs. temperature, internal master clock, AVCC = 3 V	39
Figure 34: INL vs. input code vs. temperature, internal master clock, AVCC = 3.3 V	39
Figure 35: INL vs. input code vs. temperature, internal master clock, AVCC = 3.6 V	40
Figure 36: INL vs. input code vs. temperature, external master clock, AVCC = 3 V	40
Figure 37: INL vs. input code vs. temperature, external master clock, AVCC = 3.3 V	40
Figure 38: INL vs. input code vs. temperature, external master clock, AVCC = 3.6 V	40
Figure 39: Gain error vs. AVCC vs. temperature, internal master clock	40
Figure 40: Gain error vs. AVCC vs. temperature, external master clock	40
Figure 41: Spectral noise density vs. temperature	41
Figure 42: Signal to noise ratio vs. temperature	41
Figure 43: Distortion vs. AVCC vs. temperature, internal master clock	41
Figure 44: Distortion vs. AVCC vs. temperature, external master clock	41
Figure 45: Voltage spectrum vs. frequency, external master clock	41
Figure 46: Load regulation vs. input code	41
Figure 47: PSRR vs. frequency vs. temperature, lower code input	42
Figure 48: PSRR vs. frequency vs. temperature, middle code input	42
Figure 49: PSRR vs. frequency vs. temperature, higher code input	42
Figure 50: Ceramic Flat-24 package outline	44

1 Functional description

Figure 1: Block diagram

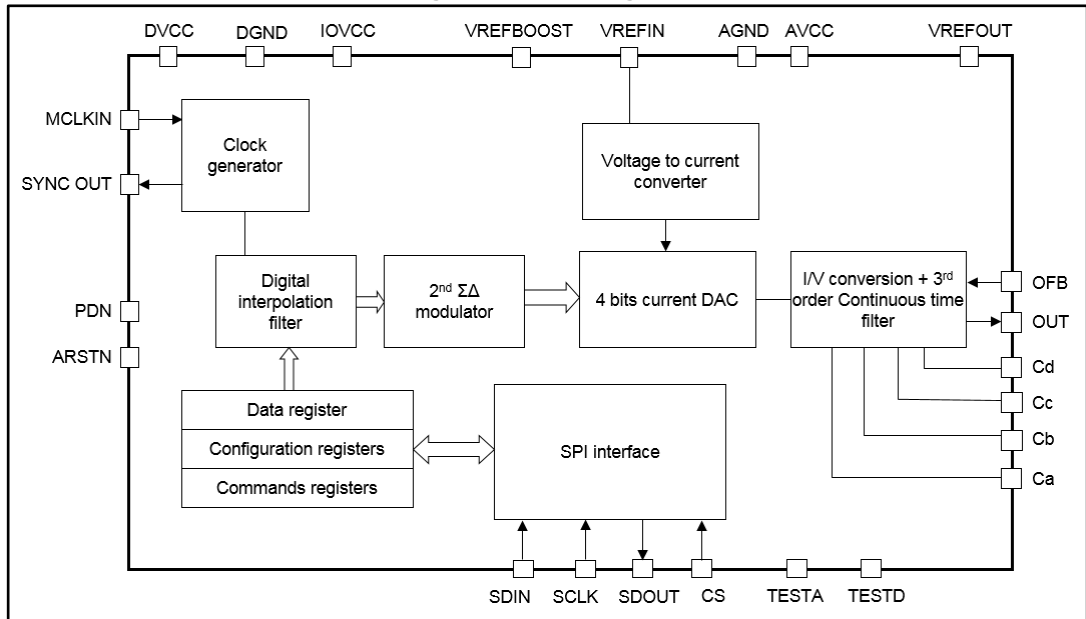


Figure 2: Typical application schematic

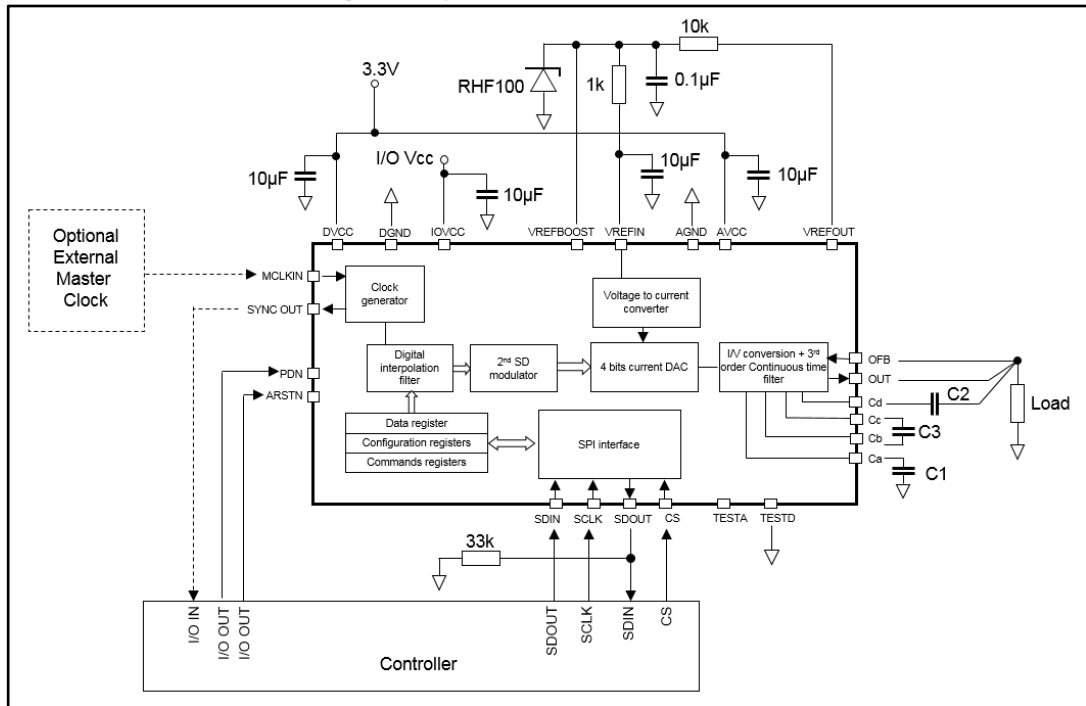


Table 2: External filter components

C1	C2	C3	Bw
10 nF	2.2 nF	4.7 nF	3 kHz

2 Pin description

Figure 3: Pin locations

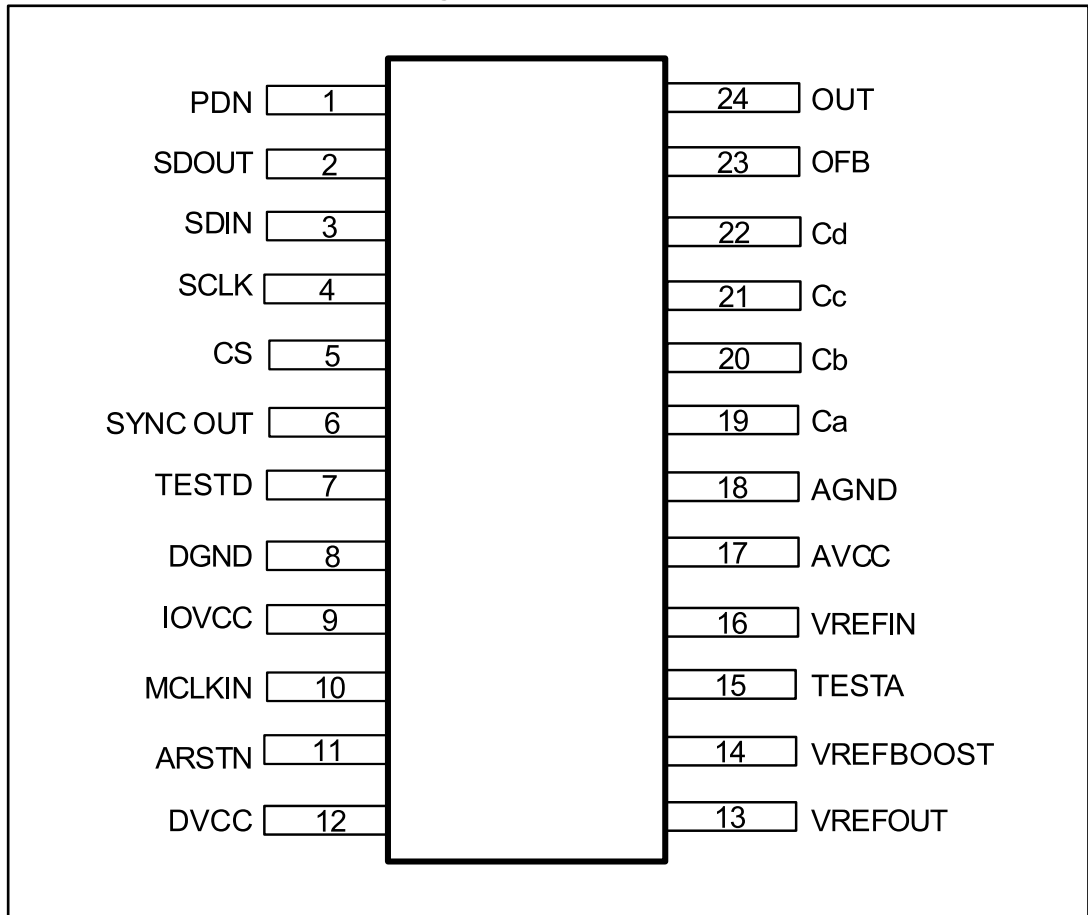


Table 3: Pin descriptions

Pin	Pin name	Description	Type
1	PDN	Power-down (active low) + internal pull-down current source	Digital
2	SDOUT	SPI data output + external pull-down resistor of 33 kΩ	
3	SDIN	SPI data input + internal pull-down current source	
4	SCLK	SPI clock input + internal pull-down current source	
5	CS	Chip select and SPI synchronization + Internal pull-up current source	
6	SYNC OUT	Master clock divided by OSR, low level during TWU	
7	TESTD	Digital test input, must be connected to DGND	
8	DGND	Digital ground	Power
9	IOVCC	IO power supply	
10	MCLKIN	Master clock input, when not used, this input must be connected to DGND	Digital
11	ASRTN	Asynchronous reset (active low) + internal pull-up current source	

Pin	Pin name	Description	Type
12	DVCC	Digital power supply	Power
13	VREFOUT	External voltage reference output power supply	Analog
14	VREFBOOST	External voltage reference boost current	
15	TESTA	Analog test pin, must be left floating	
16	VREFIN	External voltage reference input	
17	AVCC	Analog power supply	Power
18	AGND	Analog ground	Analog
19	Ca	Filter I/O	
20	Cb		
21	Cc		
22	Cd		
23	OFB	Output feedback	
24	OUT	Analog buffered/filtered single-ended output	

3 Radiations

Table 4: Radiation performance of the RHRDAC1612

Type	Features	Value	Unit
TID	Dose rate = 60 mrad/s up to	100	krad
Heavy Ions	SEL immune up to: (with a particle angle of 60° at 125°C)	125	MeV.cm ² /mg
	SEL immune up to: (with a particle angle of 0° at 125°C)	60	
	Analog SEFI immune up to:	> 3.3	
	Digital SEFI	< 1.83	
	SET at 25°C immune up to:	> 1.83	
Protons	SEL at 125°C immune up to:	184	MeV
	Analog SEFI immune up to:	184	
	Digital SEFI	< 10	
	SET at 25°C	< 10	

3.1 Total ionizing dose (TID)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHRDAC1612 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification condition C, (dose rate = 60 mrad/s, full CMOS technology).

All parameters provided in [Section 6: "Electrical characteristics"](#) apply to both pre- and post-irradiation, as follows:

- All test are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- The initial characterization is performed in qualification only on both biased and unbiased parts.

- Each wafer lot is tested at 60 mrad/s only, in the worst bias case condition, based on the results obtained during the initial qualification.

3.2 Heavy ions

The behavior of the RHRDAC1612 when submitted to heavy ions and protons is not tested in production. Heavy ions and protons trials are performed on qualification lots only.

During these trials, Analog and Digital SEFI have been observed. The occurrence of an Analog SEFI is very low, approximately an event over 70 years on GEO (worst case between LEO, SPOT and GEO comparison), but this event is not easily detectable in an application.

In the other hand, the occurrence of a digital SEFI is a little bit more important, approximately an event over 25 years on GEO (worst case between LEO, SPOT and GEO), but it is easily detectable in the application.

Analog SEFI

An analog erroneous output by a SEFI is not possible to detect in an application without using a dedicated circuitry to measure the analog output of the DAC (additional ADC and a dedicated data processing for example).

Then, to prevent analog SEFI, we recommend to perform a global reset of the circuit periodically^a.

Digital SET and SEFI

The following process describes how to detect a digital SET and a digital SEFI on SPI, and how to correct them:

- After reset and startup phase (DAC fully configured by the user and ready to use), store the values of the registers at the addresses 01h and 02h.
- Update these values whenever a voluntary action of the type “change of mode”, “modification of the data”, “autocal” etc is performed.
- Periodically (1) read the registers at addresses 01h and 02h
- Register 01h:
 - If configuration (n) = configuration (n-1): the circuit behaves properly, no specific action required.
 - If configuration (n) modified, then rewrite configuration (n-1), taking care to put in standby for some bits if necessary, and read the configuration.

Then:

If configuration (n + 1) = configuration (n-1): the circuit behaves properly, no specific action required.

If configuration (n + 1) different from configuration (n-1): proceed to a global reset of the circuit.

If offset (n) changed (without new autocal): proceed to a global reset of the circuit.

- Register 02h:

If data (n) = data (n-1): the circuit behaves properly, no specific action required.

If data (n) is modified, then rewrite data (n-1) and read the data.

Then:

If data (n + 1) = data (n-1) : the circuit behaves properly, no specific action required.

if data (n + 1) different from data (n-1): proceed to a global reset of the circuit.

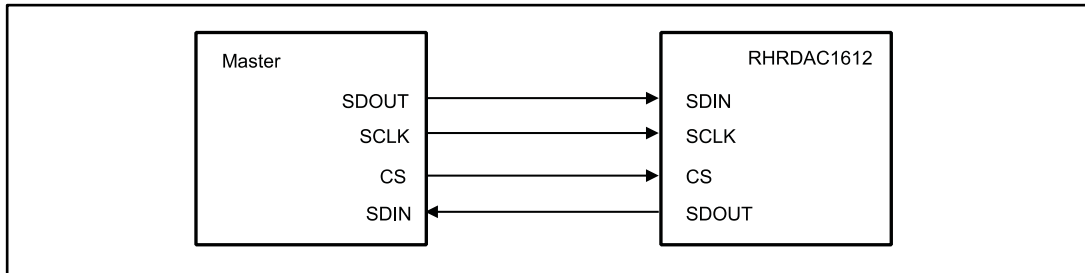
^a The period is linked to the mission profile (“SEE rates orbit” report available upon request), and it should be defined by the user.

4 DAC operation

4.1 SPI interface

The SPI interface consists of an internal 32 bit input shift register which is connected to the SDIN input. When the chip select signal, CS, is set to low level, the data on SDIN is shifted into the internal shift register on the rising edge of the clock SPI SCLK. Exactly 32 edges of SCLK must be applied to correctly update the shift register. If less than 32 edges is applied and CS goes high, the SPI transaction is aborted.

Figure 4: SPI interface connections for stand-alone operations

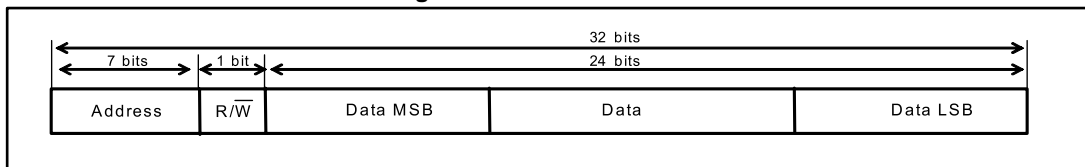


The SPI interface is designed for stand-alone operations only. A daisy chain is not possible.

4.1.1 SPI frame format

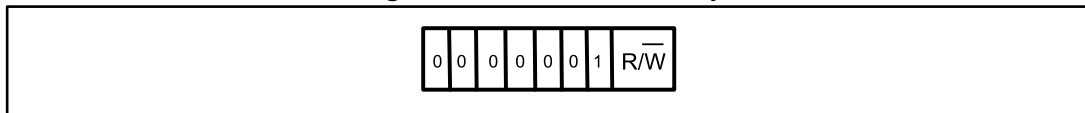
The expected SPI frame format is shown in *Figure 5: "SPI frame format"* below. The 32 bits are divided into 7 bits, 1 bit, and 24 bits of data. The 7 and 1 bits can be used to address the register bank i.e. a R/W bit which determines if it is a read or write command. If the R/W bit is set to 1, the SPI register bank is read. If the R/W bit is set to 0, the SPI register bank is written with the data bits.

Figure 5: SPI frame format



The data are written in the SDIN input with the MSB first. The first bit that enters in the SDIN after the falling edge of the CS is bit 7 of the address that corresponds to the MSB of the first byte. By convention, the address is coded on 7 bits. *Figure 6: "Address 01h in binary"* shows address 01h in binary for the first byte that enters in the SPI interface.

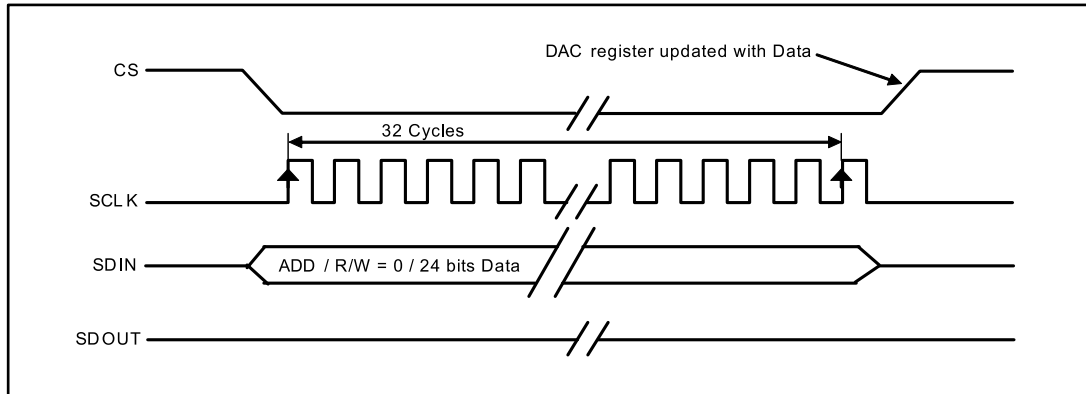
Figure 6: Address 01h in binary



4.1.2 SPI write sequence

Figure 7: "SPI write sequence" describes how the SPI interface works for a write operation. The chip select signal, CS, is pulled low to indicate the start of the transaction. After the falling edge of CS, 32 cycles of SCLK are applied to shift the data on the SDIN into the shift register. The first 7 bits sent by the master on the SDIN indicate which register is to be written, and the next bit sent by the master indicates that a write access of the DAC registers is required (R/W = 0). The last 24 bits sent on the SDIN contain the data to be written to the DAC register. The DAC register specified by the address field is loaded with the data input on the rising edge of the CS.

Figure 7: SPI write sequence

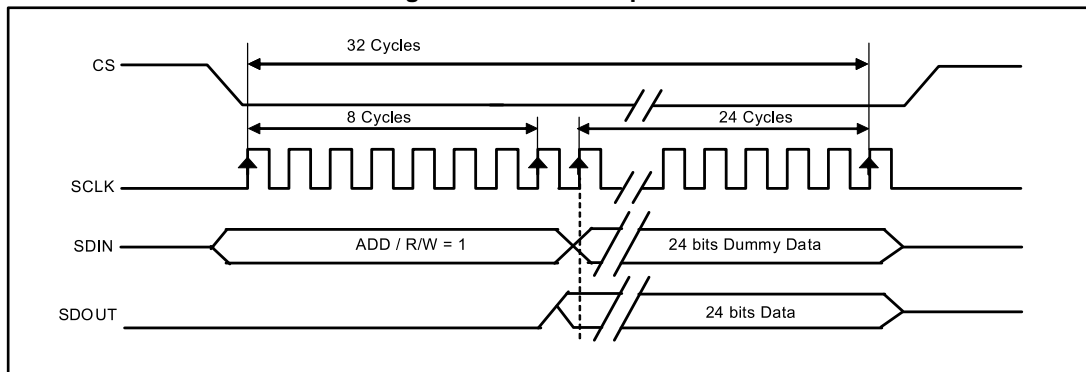


During a write sequence, the output data, SDOOUT, remains at a low level.

4.1.3 SPI read sequence

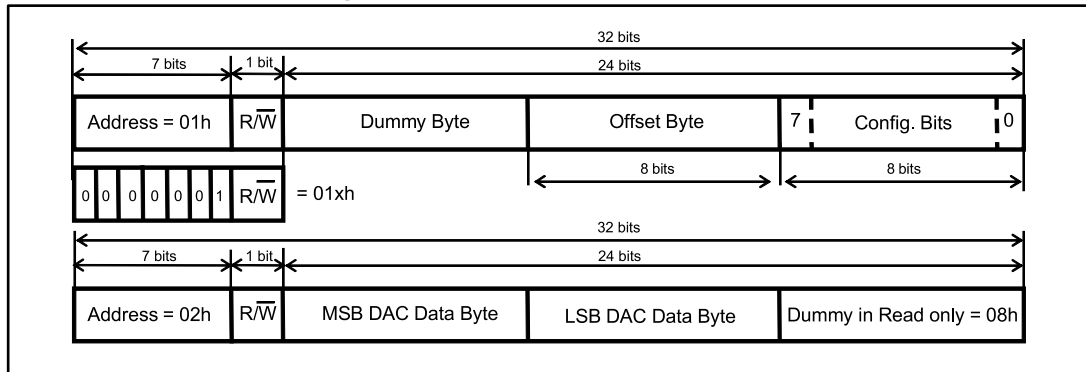
The CS signal is pulled low to indicate the start of a transmission. With CS low, 32 cycles of SCLK are applied to shift the data on the SDIN into the shift register. The first 7 bits sent by the master on the SDIN, indicate to the slave the address of the register to be read. The next bit (R/W = 1) indicates that a read operation is to be performed. The final 24 bits on the SDIN are dummy data. At the eighth rising edge of the SCLK, the contents of the register addressed are loaded into the internal shift register. This requires the shift register to be synchronously preset with the data to be shifted out. Then, the data required to be read are shifted out to the MSB first, with the last 24 cycles of the SCLK on the SDOOUT output.

Figure 8: SPI read sequence



4.2 DAC configuration registers

Figure 9: Data and control frame format



- Address = 01h
 - Configuration bit register: this 8-bit register is used to configure and control the DAC.
 - Offset byte register: this 8-bit register is used to read the result of the offset calibration of the DAC. The result is in two's complement format. If the value is in the range of 01h to FEh, the auto-calibration has gone well. If the value is 00h or FFh, the device cannot compensate the offset and there is an internal problem. If the result is 80h, the device has no offset error to compensate.
- Address = 02h
 - DAC data byte: this 16-bit register is used to set the output voltage of the DAC.

Table 5: "DAC configuration bits and function" shows the name and the function of each bit.

Table 5: DAC configuration bits and function

Address	Config. bit/data	Name	POR or ASRSTN value	Read/Write possibilities	Description
01h	0 = LSB	CAL	0	Read	This bit gives the calibration status. If set to 0, it indicates calibration is ongoing. If set to 1, it indicates calibration is complete. This bit is cleared to 0 after reading the configuration bit register.

Address	Config. bit/data	Name	POR or ASRSTN value	Read/Write possibilities	Description
	1	LC	1	Read/Write	<p>Launch calibration bit: unlike other configuration bits, it performs its function only on transition from 1 to 0, or 0 to 1.</p> <ul style="list-style-type: none"> The DAC always performs an automatic calibration on wakeup from reset or standby (reference voltage active or not) before going to the operating state. If this bit transitions from 1 to 0 in the calibration state, the calibration cycle is terminated, and the DAC returns to the operating state. If this bit transitions from 0 to 1 in the operating state, a new calibration cycle is started, and the DAC moves to the calibration state. <p>Calibration proceeds using the internal or external master clock. It depends on the RC EN bit value. Before launching an auto-calibration, the output voltage must be set to VREFIN (DAC DATA = 8000).</p>
	2	Vseries	0	Read/Write	<p>If this bit is set to 1, it modifies the boost sequence for the Vref. This bit must be set to 1 when using an external series Vref instead of a shunt Vref. This bit is useless if the VREFOUT and VREFBOOST pins are not used. It can only be written in standby mode.</p>
	3	Unused	0	Read	
	4	Unused	1	Read	
	5	RC EN	1	Read/Write	<p>Enable internal RC oscillator. This bit is set to 0 to enable the external master clock input MCLKIN. It can only be written in standby mode.</p>
	6	Unused	1	Read	
01h	7	Two's complement/straight binary	0	Read/Write	<p>When set to 0, the data format is in straight binary mode and when set to 1, the data format is in two's complement mode.</p>
	8-15	Offset byte register	xxh	Read	<p>This byte contains the results of the offset calibration which are in two's complement format.</p>

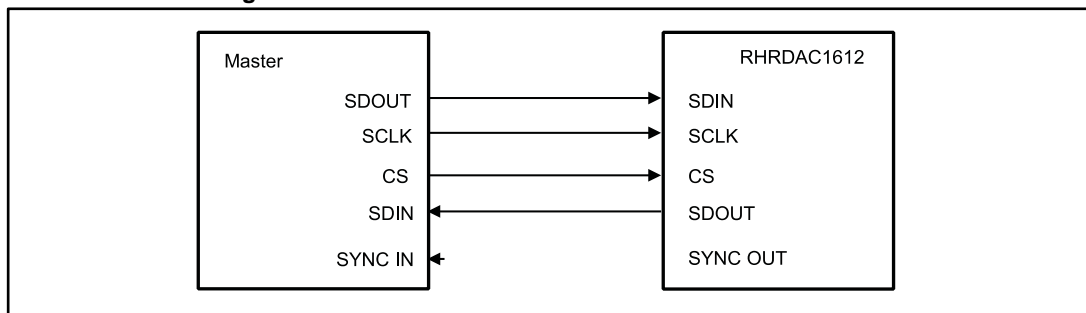
Address	Config. bit/data	Name	POR or ASRSTN value	Read/Write possibilities	Description
02h	0-23	DAC data	800008h	Read/Write	These 16 bits of data set the output DAC voltage. The last bits (16 to 23) are in read-only mode and their reset value is 08h.

4.3 DAC register data update options

DAC register data can be updated in two ways.

Figure 10: "Connections between the DAC and the master" shows the connections between the master and the DAC.

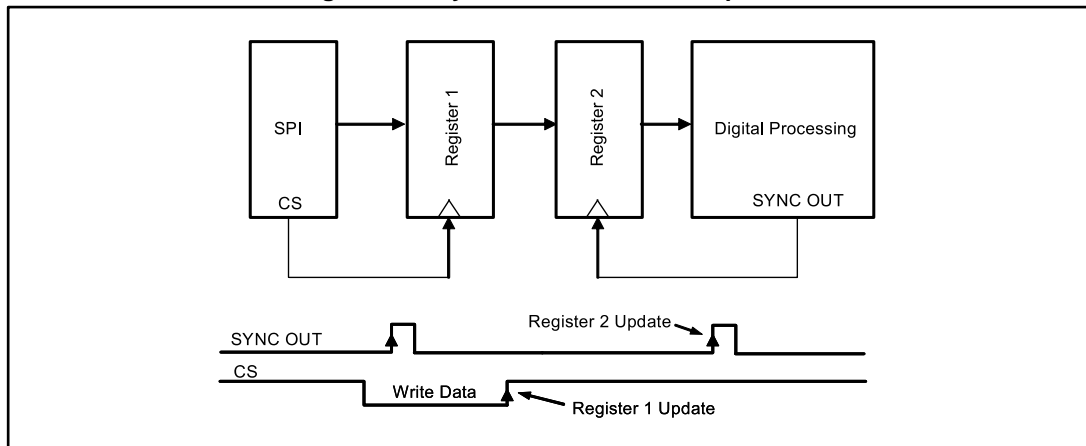
Figure 10: Connections between the DAC and the master



1. SYNC OUT, signal not used by the master

In this configuration, data entered through the SPI interface are not synchronized with the internal sample rate. Register 2 (register used by the digital processing) is updated with the content of register 1 at the rising edge of SYNC OUT. Register 1 is updated at the rising edge of CS with the condition that 32 cycles of SCLK have been achieved. Figure 11: "Asynchronous DAC data update" shows this option.

Figure 11: Asynchronous DAC data update

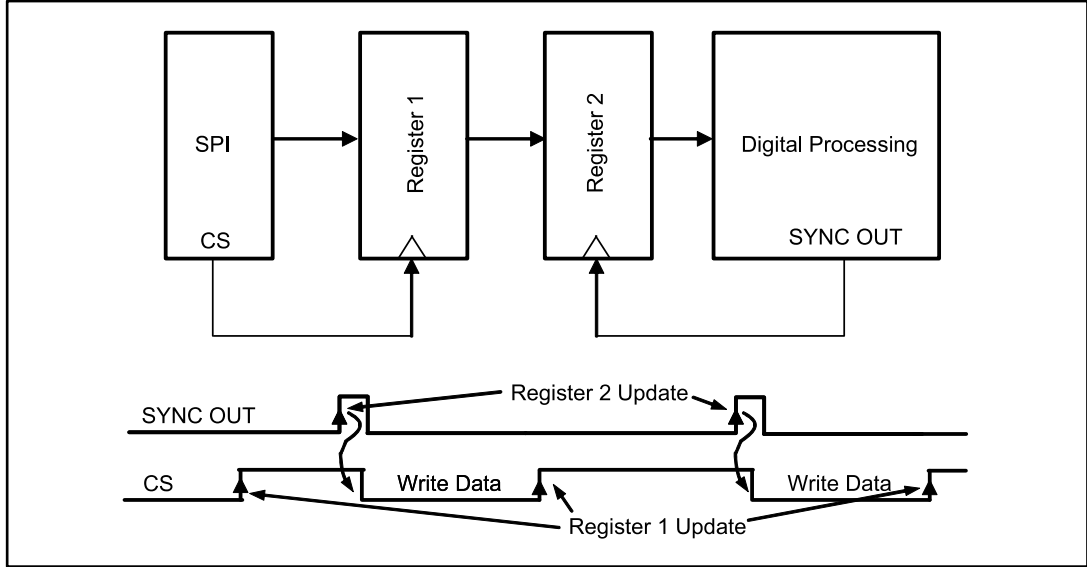


1. SYNC OUT, signal used by the master

In this configuration, data entered through the SPI interface are synchronized with the internal sample rate at the condition that after a rising edge of SYNC OUT, an SPI write

transaction starts and finishes before the next rising edge of SYNC OUT. Register 2 (register used by the digital processing) is updated with the content of register 1 at the rising edge of SYNC OUT. Register 1 is updated at the rising edge of CS with the condition that 32 cycles of SCLK have been achieved. *Figure 12: "Synchronous DAC data update"* shows this option.

Figure 12: Synchronous DAC data update



4.4 DAC transfer function

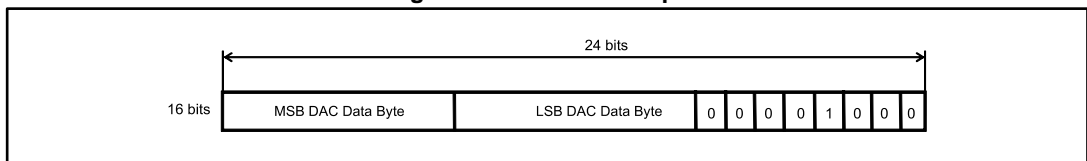
Thanks to the two's complement/straight binary bit configuration, the RHRDAC1612 can accept data in two formats: two's complement and straight binary.

Table 6: "Transfer function" shows the formulas used to calculate the transfer function ($V_{out} = f(\text{digital code})$) of the RHRDAC1612.

Table 6: Transfer function

Data format	16-bit data
Two's complement	$V_{out} = 2 \times V_{ref} \times \frac{\text{Data} + 2^{15}}{2^{16}}$
Straight binary	$V_{out} = 2 \times V_{ref} \times \frac{\text{Data}}{2^{16}}$

Figure 13: Data frame input



4.5 External Vref power-up sequence

The RHRDAC1612 has an internal boost sequence to speed-up the charge of necessary external filtering capacitors used by the reference voltage. The boost sequence can take into consideration both shunt and series Vref thanks to the bit Vseries in the configuration register.

This boost sequence is necessary for the DAC because the auto-calibration is based on the VREFIN input voltage and this voltage must be as accurate as possible (error < LSB).

Figure 14: "Internal switches for boost sequence" shows the internal switches specifically used for the boost sequence.

Figure 14: Internal switches for boost sequence

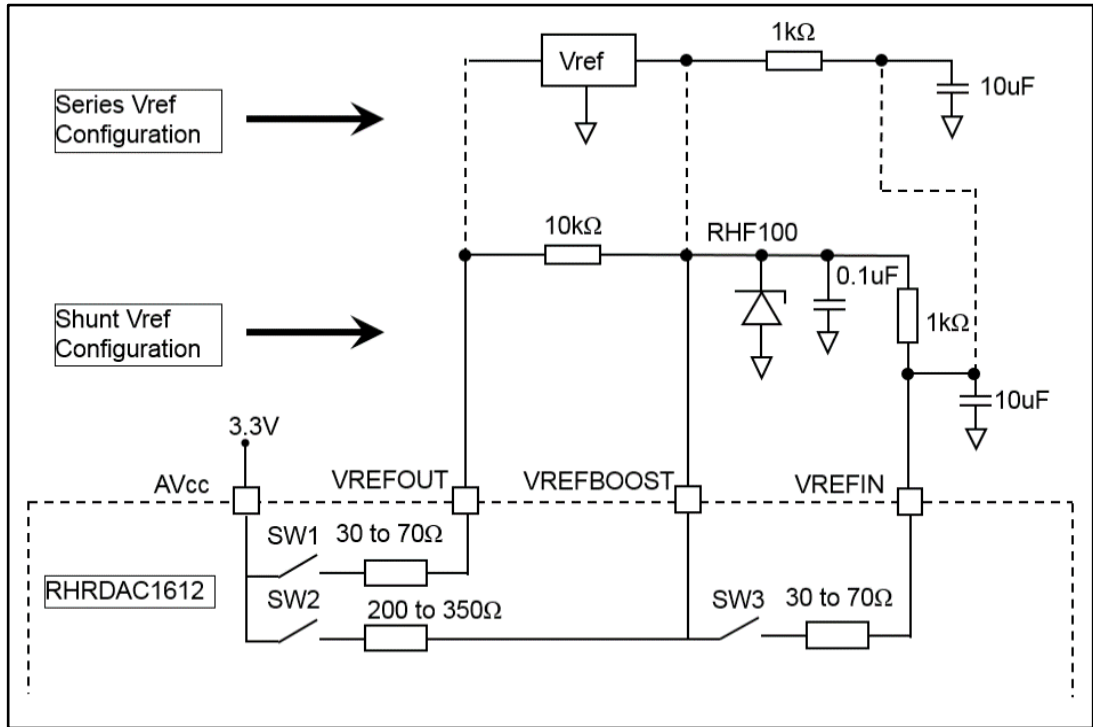
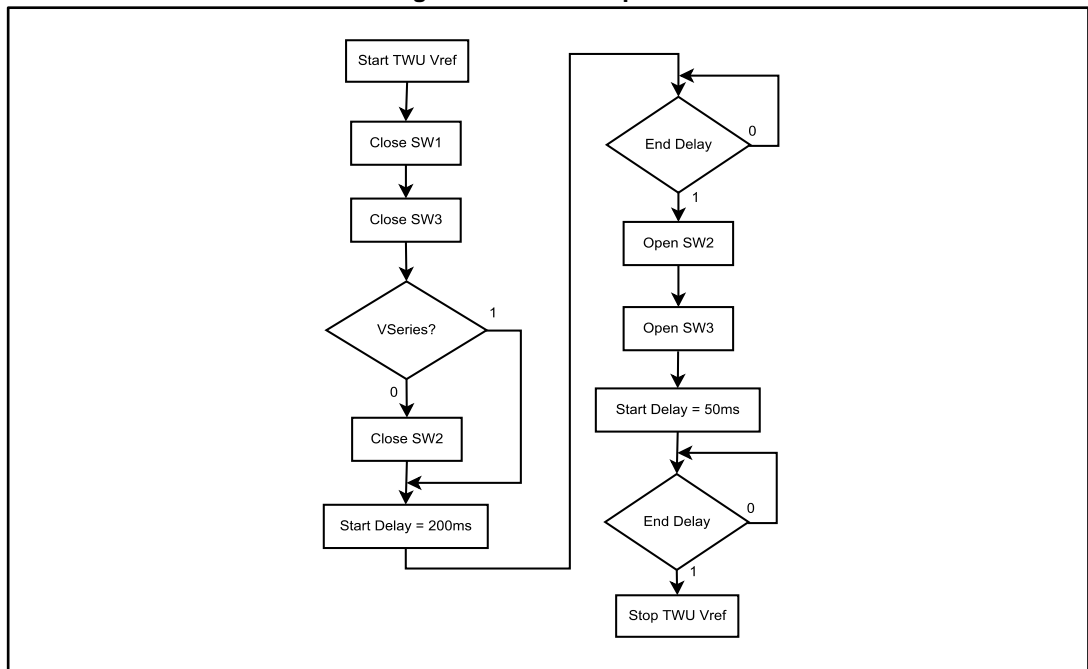


Figure 15: "Boost sequence" shows different steps of the boost sequence.

Figure 15: Boost sequence



4.6 DAC operation flow charts

Figure 16: "DAC operation flow chart (main)" shows how the DAC manages different situations.

Figure 16: DAC operation flow chart (main)

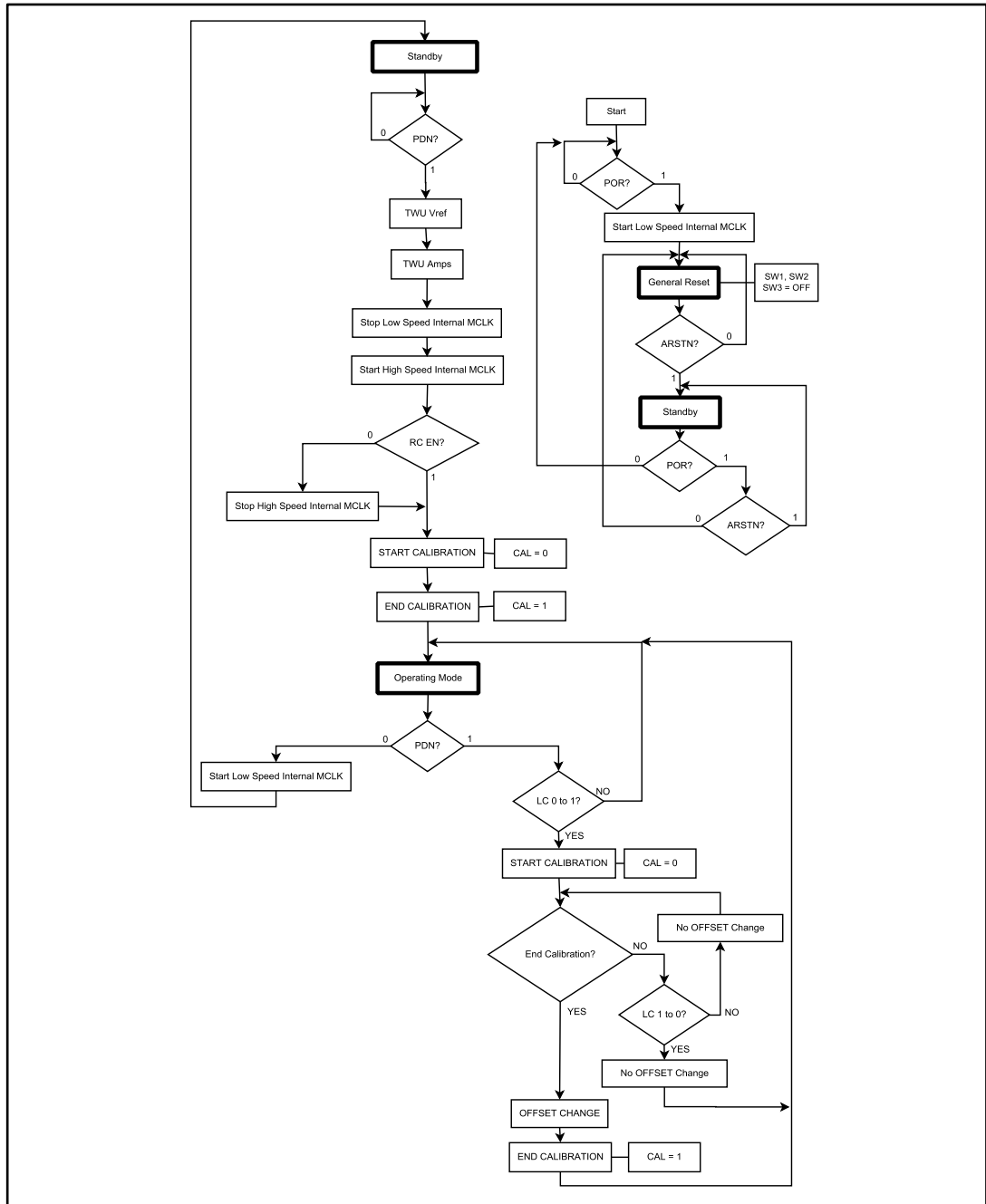
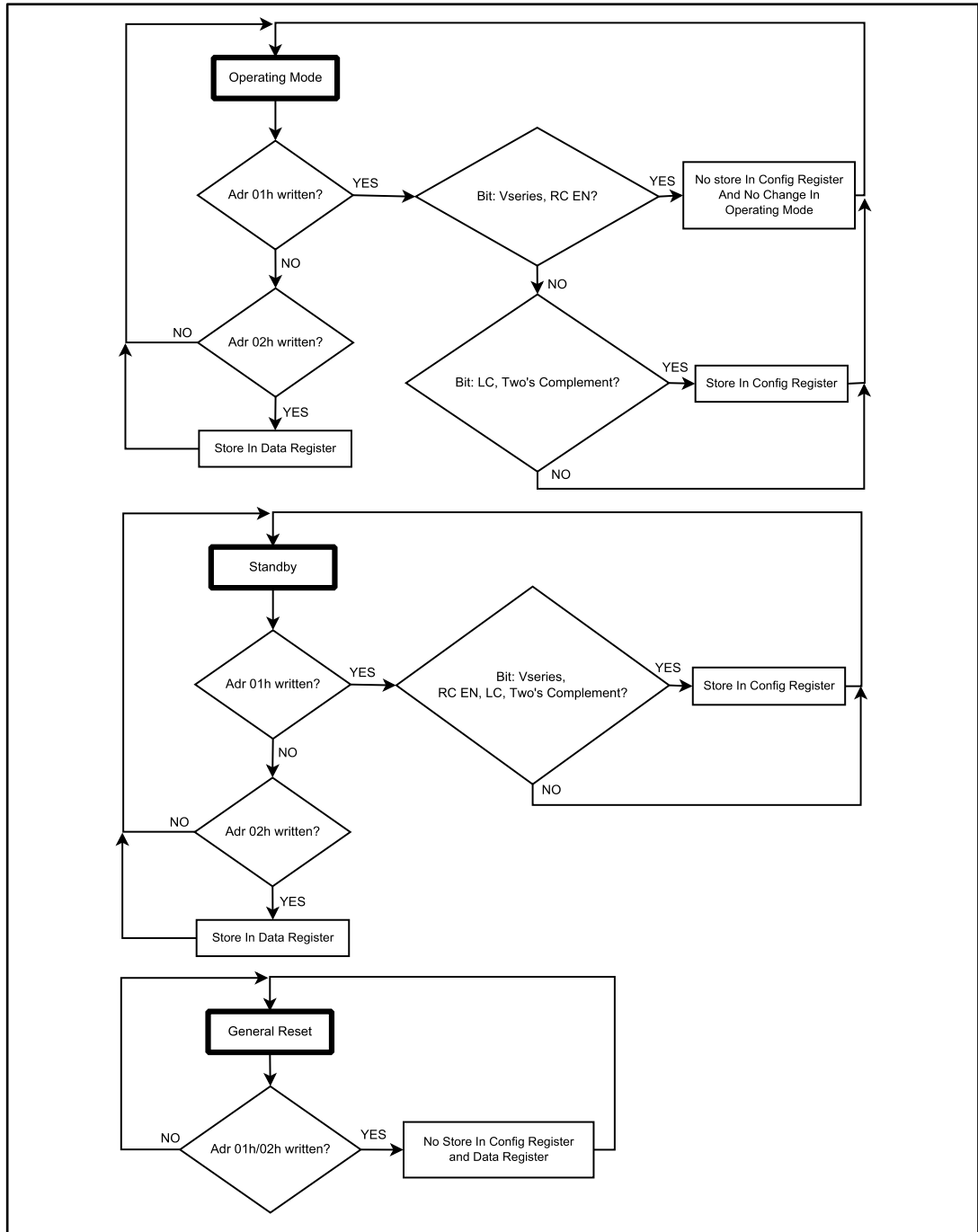


Figure 17: DAC operation flow chart (continued)



1. POR = internal power-on-reset
2. Internal MCLK = internal master clock at 3 MHz typical
3. Low-power INT CLK = internal low-power clock at 10 kHz
4. TWU Vref = wakeup and boost sequence of external Vref
5. TWU amps = wakeup of output amplifiers + analog filter
6. TWU Vref + TWU amps = TWU in *Table 12: "Operating conditions (Tamb from -55 °C to 125 °C)"*
7. Reset = reset mode of DAC

8. Standby = standby mode of DAC
9. Operating = normal operation of DAC.
10. CAL = flag that indicates the start/end of the calibration
11. Offset change = function that changes the offset register value
12. Calibration = function that calibrates the offset error. When the function starts, CAL = 0 and when the function ends, CAL = 1.

4.7 ARSTN and PDN digital pin functions

ARSTN

ARSTN is an input that allows the RHRDAC1612 to be reset asynchronously. This input is active at low level ("0" logic) and has total priority vs. the PDN input and SPI control.

While ARSTN = "0" logic, the registers of the RHRDAC1612 cannot be set. A read of these registers gives 00h.

When ARSTN changes from "0" to "1" logic, all values in the register are set to default as indicated in [Table 6](#) (see POR or ARSTN column).

PDN

PDN is an input that allows the RHRDAC1612 to be set asynchronously in standby. This input is active at low level ("0" logic). Despite the standby feature, this input **must be used** to set/reset the bits Vseries and RC EN at address 01h as shown in [Figure 17: "DAC operation flow chart \(continued\)"](#).

[Table 6](#) below shows the truth table of ARSTN and PDN.

Table 7: Truth table of ARSTN and PDN

ARSTN	PDN	Icc	Vout
0	0	Standby	HiZ state
1	0		
0	1	≈ 2.2 mA	LowZ, equal to ≈ VREFIN (it is not recommended to use this combination)
1	1	Operating	LowZ operating, Vout = f (code in Adr 02h)

4.8 Power-on-reset (POR) feature

The RHRDAC1612 integrates an internal POR connected to AVCC. POR levels are given in [Table 13: "Electrical characteristics"](#). If AVCC does not reach 2 V to 2.3 V when AVCC increases, the internal POR forces a reset equivalent to ARSTN = 0. If AVCC does not reach 2 V to 1.7 V when AVCC decreases, the internal POR is not active.

4.9 Power supply sequencing

The RHRDAC1612 has three different power supplies (AVCC, DVCC, and IOVCC). These power supplies must be set and reset as described in [Figure 23: "DAC timing diagram 2"](#) and the amplitude must respect values in [Table 12: "Operating conditions \(Tamb from -55 °C to 125 °C\)"](#).

To avoid unwanted behavior on the output during power supply sequencing, it is also advised to keep the ARSTN and PDN inputs at low levels (GND).

4.10 Setting the RHRDAC1612

The RHRDAC1612 can only be programmed through the SPI bus. A specific byte, at address 01h, is dedicated for this purpose (see [Table 5: "DAC configuration bits and function"](#)). Depending on the ARSTN and PDN pin levels, the following table shows what can be written or read in this specific byte. Refer also to [Figure 17: "DAC operation flow chart \(continued\)"](#).

Table 8: Control bit possibilities

	WRITE sequence				READ sequence			
	ARSTN = 0		ARSTN = 1		ARSTN = 0		ARSTN = 1	
	PDN = 0	PDN = 1	PDN = 0	PDN = 1	PDN = 0	PDN = 1	PDN = 0	PDN = 1
CAL	X ⁽¹⁾	X	NA ⁽²⁾	NA	X	X	OK	OK
LC				OK				
Vseries			OK ⁽³⁾	NA				
RC EN				OK				
Two's complement								

Notes:

- ⁽¹⁾X = action impossible, result is always 0
- ⁽²⁾NA = not applicable
- ⁽³⁾OK = action possible

Vseries, RC EN, and LC

- Vseries indicates if a shunt or series reference voltage is connected to the VREFIN pin and is supplied by the VREFOUT pin. The Vseries bit is only used when the RHRDAC1612 is woken up by the PDN pin ("0" to "1"). So, the write of this bit is only possible when PDN = 0.
- RC EN indicates if the DAC uses the internal or the external master clock. As it is not advised to switch clocks during operation, this bit can be written only when PDN = 0.
- LC is used to launch the output offset auto-calibration. Offset calibration is useful only when the DAC is in operating mode. Consequently, calibration is performed only when PDN = 1.

Output voltage at startup

When the PDN goes from 0 to 1, RHRDAC1612 enters wakeup mode for a maximum period of 440 ms (TWU + CALT). During this time, Vout is set to VREFIN with a lowZ output impedance, whatever the DAC data code written at address 02h. At the end of 440 ms, the output voltage is set to the code present at this time in the DAC data (address 02h).

Examples of RHRDAC1612 settings

1. External Vref = shunt, internal master clock used
 - a. Power-up the DAC and during this sequence, keep ARSTN and PDN at GND
 - b. Set ARSTN to 1
 - c. Set the two's complement bit and DAC data word if necessary



- d. There is no need to set Vseries and RC EN because, by default, they are on the Vref shunt and internal master clock
- e. Set PDN to 1
- f. Wait a maximum period of 440 ms (the wakeup time)
- g. After 440 ms, launch an auto-calibration cycle with the LC bit
- h. After a maximum period of 40 ms, the DAC is ready to use
2. External Vref = shunt, external master clock used
 - a. Power-up the DAC and during this sequence, keep ARSTN and PDN at GND
 - b. Set ARSTN to 1
 - c. Set the two's complement bit and DAC data word if necessary
 - d. There is no need to set Vseries
 - e. Set the RC EN bit for the external master clock
 - f. Set PDN to 1
 - g. Wait a maximum period of 440 ms (the wakeup time)
 - h. After 440 ms, launch an auto-calibration cycle with the LC bit
 - i. After a maximum period of 40 ms, the DAC is ready to use

4.11 SYNC OUT pin

SYNC OUT is an output that mirrors the internal clocking of the RHRDAC1612.

This pin can be used to synchronize a master when an accurate timing is requested (see [Section 4.3: "DAC register data update options"](#)). However, depending on the state of the RHRDAC1612, five scenarios below can be described for the SYNC OUT pin.

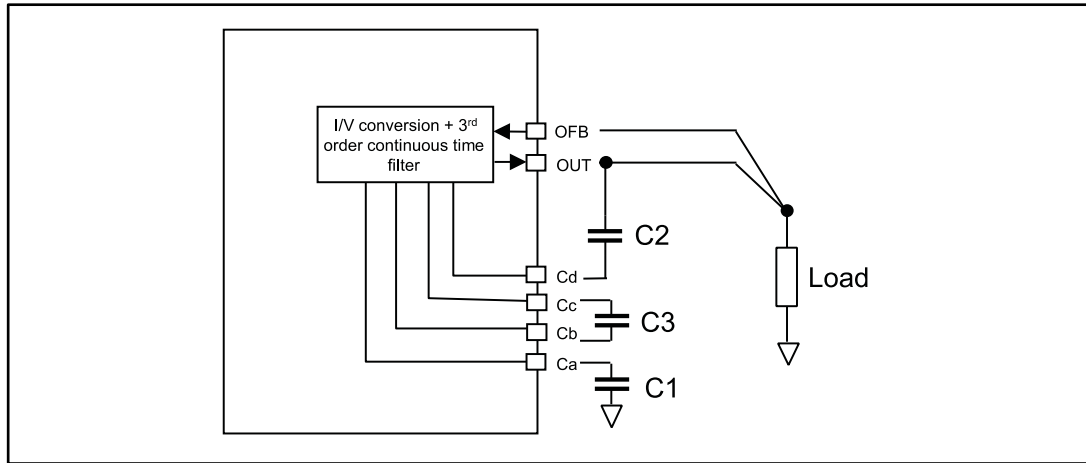
- During operation and when the internal master clock is chosen, SYNC OUT frequency = internal master clock/256 = 9.6 kHz to 14.4 kHz.
- During operation and when the external master clock is chosen, SYNC OUT frequency = external master clock/256 = 12 kHz for ExtMCLK = 3 MHz.
- When PDN goes from 0 to 1, during t8 time (see [Table 14: "Timing characteristics"](#)), SYNC OUT frequency = low-speed internal clock/256 \approx 32 kHz/256 = 125 Hz.
- When PDN goes from 1 to 0, during t9 time (see [Table 14: "Timing characteristics"](#)), SYNC OUT frequency = low-speed internal clock/256 \approx 32 kHz/256 = 125 Hz.
- When PDN = 0, SYNC OUT output is disabled.

4.12 Output feedback pin

A dedicated output feedback pin is available to sense the output voltage as close as possible to the load to avoid errors due to parasitic resistance. [Figure 2: "Typical application schematic"](#) shows how the connection must be made.

Note that the C2 capacitor can be organized as presented in [Figure 2: "Typical application schematic"](#) but, it can also be directly connected to OUT as presented in the following figure.

Figure 18: Another connection for C2



4.13 Pull-up and pull-down on digital inputs

To prevent floating digital inputs, the RHRDAC1612 integrates dedicated pull-ups or pull-downs vs. the IOVCC and/or DGND pins (see table below). These pull-ups or pull-downs are current source and their values are given in [Table 12: "Operating conditions \(Tamb from -55 °C to 125 °C\)"](#).

Table 9: Pull-up and pull-down pin assignments

Pin	Pin assignment
ARSTN	Pull-up
PDN	Pull-down
MCLKIN	
SDIN	
SCLK	
CS	Pull-up

These pull-ups or pull-downs mean that if all the digital inputs are left floating, the RHRDAC1612 is reset and consequently put into standby mode.

SDOUT

SDOUT does not have an internal pull-up or pull-down functionality. Consequently and to avoid standby current fluctuating in standby mode, it is mandatory to place an external pull-down resistor vs. DGND as represented in [Figure 2: "Typical application schematic"](#). A good choice of resistor is 33 kΩ.

4.14 Anti-aliasing output filter design

The RHRDAC1612 integrates roughly all the necessary components to make a third-order low pass output filter. The only external components needed are three capacitors as represented in [Figure 2: "Typical application schematic"](#).

The following figure shows a simplified view of what is inside the RHRDAC1612 output stage.

Auto-calibration acts on the output offset voltage in the range ± 4 mV and a resolution step of 31 μ V.

Auto-calibration results are given for information. They can be found in bit 8 to 15 of the register at address 01h (see [Table 5: "DAC configuration bits and function"](#)). The number in this byte is signed with the following characteristics:

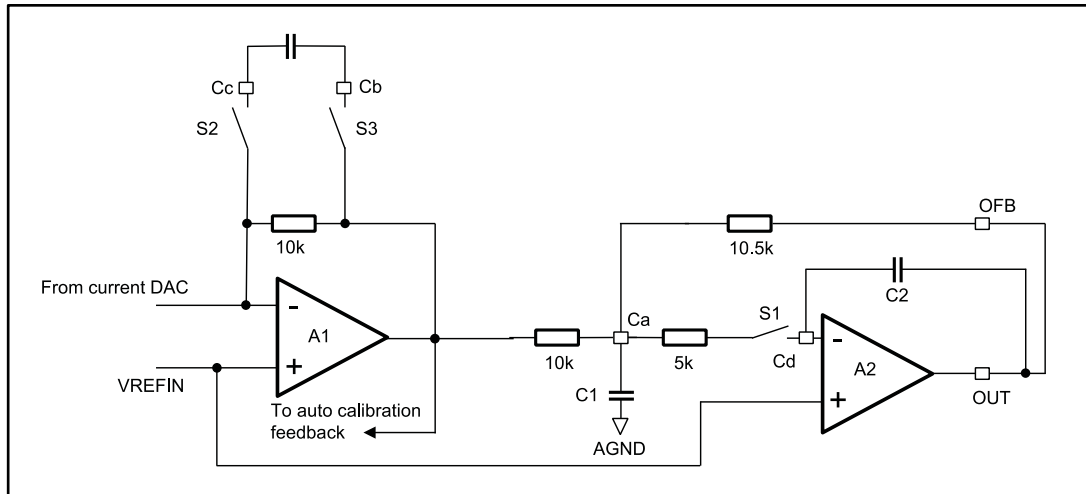
- 128 is the offset correction which is 0
- Between 1 to 127 is the negative internal correction
- Between 129 to 254 is the positive internal correction
- 0 or 255 is "auto-calibration failed" which means the offset is out of the calibration range.



Due to the discrete nature of the auto-calibration feature (31 μ V), a repeating auto-calibration sequence with an output voltage, output current, input voltage reference, and temperature unchanged, can give a different number each time.

The following figure shows a simplified schematic of the output stage with the auto-calibration feature.

Figure 20: Simplified schematic of output stage with auto-calibration feature

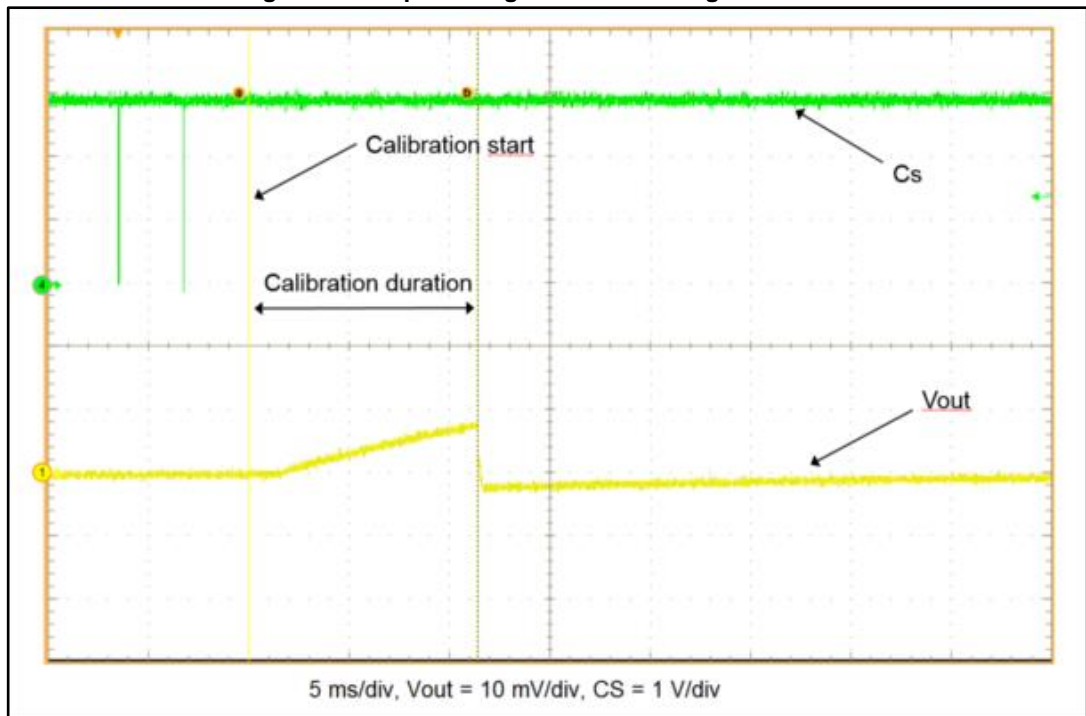


During normal operation, S1 to S3 are closed and the auto-calibration feedback is disabled. When auto-calibration is requested, S1 to S3 are open. During calibration, OUT voltage stays roughly at the value settled before the calibration request thanks to C1, C2, and the auto-calibration time. At the end of calibration, S1 to S3 are closed and OUT behavior can be as follows:

- No offset change and DAC data unchanged in address 02h during calibration i.e. OUT remains constant.
- Offset changes and DAC data unchanged in address 02h during calibration i.e. OUT has a step corresponding to offset correction value.
- No offset change and DAC data changed in address 02h during calibration i.e. OUT has a step corresponding to DAC data change value.
- Offset changes and DAC data changed in address 02h during calibration i.e. OUT has a step corresponding to DAC data change value \pm the offset correction.

The following figure shows the output behavior during an auto-calibration. The output voltage has been set to VREFIN.

Figure 21: Output voltage behavior during calibration

**Note on the CAL bit**

The CAL bit is a read-only bit that gives the calibration status.

1. "0" indicates:
 - a. The idle state if the calibration was not requested with the LC bit before "0" was read.
 - b. Calibration is ongoing if the calibration was requested with the LC bit before "0" was read.
2. "1" indicates that the calibration has ended. **"1" is automatically reset to "0" when this bit is read.**



After a wakeup with PDN from "0" to "1" (see [Section 4.10: "Setting the RHRDAC1612"](#)), an auto-calibration is automatically made. Consequently, the first read of CAL after this wakeup is "1".

4.16 VREFIN input

The RHRDAC1612 output voltage is directly proportional to the VREFIN input voltage. Any variation on VREFIN (e.g. noise, absolute precision, temperature) is proportionally copied on the output voltage.

RHF100 is an STMicroelectronics 1.2 V precision shunt reference voltage. The RHRDAC1612 has been designed to work optimally with the RHF100.

In [Figure 2: "Typical application schematic"](#), the low-pass filter created by the 1 k Ω /10 μ F eliminates most of the noise produced by the RHF100. On the RHF100, the 0.1 μ F in parallel ensures stability while the 10 k Ω resistor biases the RHF100 through the VREFOUT pin power supply.

4.17 VREFOUT output

This pin is used to provide a power supply through AVCC to the external reference connected to VREFIN (see [Figure 14: "Internal switches for boost sequence"](#)). This output is directly driven by the PDN pin and when the RHRDAC1612 is set in standby, VREFOUT is disconnected from AVCC thereby putting the reference voltage in standby. The internal switch can handle up to 12 mA allowing connection to a wide range of external references.

Table 10: VREFOUT behavior vs. PDN and ARSTN

PDN	ARSTN	VREFOUT
0	0	HiZ
0	1	
1	0	
1	1	AVCC

4.18 TESTA and TESTD pins

TESTA and TESTD pins are used for making industrial tests on the ATE. **These pins are not used in normal operation. TESTA must be left floating and TESTD must be connected to DGND.**

5 Absolute maximum ratings and operating conditions

Table 11: Absolute maximum ratings

Symbol	Parameter	Values	Unit
AVCC	Analog supply voltage	4.5	V
DVCC	Digital supply voltage	4.5	
IOVCC	Digital buffer supply voltage	4.5	
V _{IN_Ana}	Analog inputs: bottom limit \geq top limit	-0.3 to AVCC+ 0.3	
V _{IN_Dig}	Digital inputs: bottom limit \geq top limit	-0.3 to IOVCC + 0.3	
I _{Dout}	Digital output current	-10 to 10	mA
T _{stg}	Storage temperature	-65 to 150	°C
R _{thjc}	Thermal resistance junction-to-case	22	°C/W
R _{thja}	Thermal resistance junction-to-ambient	60	
ESD	HBM (human body model) ⁽¹⁾	2	kV
I _{ESD diode}	Continuous current in ESD diode	10	mA

Notes:

⁽¹⁾Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 k Ω resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 12: Operating conditions (T_{amb} from -55 °C to 125 °C)

Symbol	Parameter	Min	Typ	Max	Unit
AVCC	Analog supply voltage	3	3.3	3.6	V
DVCC	Digital supply voltage	3	3.3	3.6	
AVCC - DVCC	Differential voltage	-0.2	0	0.2	
IOVCC	I/O supply voltage	1.6		DVCC	
DVCC - IOVCC	Differential voltage	0		2	
V _{ref}	External reference voltage	1	1.2	1.4	
V _{IL}	Digital input voltage low level	0		0.4	
V _{IH}	Digital input voltage high level	0.8 x IOVCC		IOVCC	
V _{OLD}	Digital output voltage low level with 1 mA sink current	0		0.4	
V _{OHD}	Digital output voltage high level with 1 mA source current	IOVCC - 0.4 V		IOVCC	
I _{IHD}	Digital internal pull-down current source (Vs. DGND), pins PDN, SCLK, SDIN, and MCLK1 = IOVCC	100		300	μ A
I _{ILD}	Digital internal pull-up current source (Vs. IOVCC), pins CS and ARSTN = DGND	-300		-100	

Symbol	Parameter	Min	Typ	Max	Unit
Bw	Bandwidth, C1 = 10 nF, C2 = 2.2 nF, C3 = 4.7 nF		3		kHz
MCLKI	Internal master clock	2.4	3	3.6	MHz
MCLKE	External master clock	2.4	3	3.6	
dt	External master clock duty cycle	40	50	60	%
jt	External master clock jitter, bench evaluation			100	ps
CL	Capa-load guaranteed by design, stability, noise	100		200	pF

6 Electrical characteristics

Unless otherwise specified, the test conditions in [Table 13: "Electrical characteristics"](#) are: AVCC = DVCC = 3 V to 3.6 V, IOVCC = 1.6 V to 3.6 V, Ext MCLKIN = 3.072 MHz, external $V_{ref} = 1.2$ V, $C_{load} = 100$ pF, $T_{amb} = -55$ °C to 125 °C.

Table 13: Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I _{ccA}	Current consumption on AVCC	PDN = ARSTN = IOVCC		4	4.7	mA
I _{ccD}	Current consumption on DVCC internal clock ⁽¹⁾	PDN = ARSTN = IOVCC		640	750	μA
I _{ccIO}	Current consumption on IOVCC internal clock ⁽²⁾⁽³⁾	PDN = ARSTN = CS = IOVCC		5	10	
I _{ccStdbY}	Total current consumption in standby mode	PDN = 0.4 V, ARSTN = CS = IOVCC, Ext MCLK = OFF		100	200	
POR level	Internal power-on-reset, threshold levels	VCC increasing	2.02		2.3	
		VCC decreasing	1.7		2	
RON1	Between AVCC and VREFOUT		30		70	Ω
RON2	Between AVCC and VREFBOOST		200		350	
RON3	Between VREFBOOST and VREFIN		30		70	
LSB	Lowest significant bit	V _{ref} = 1.2 V		36.6		μV
V _{max}	High output rail			2 x V _{ref}		V
V _{min}	Low output rail on 10 kΩ load connected to GND				12	mV
LR _{sink}	Output load regulation with 100 μA output sink current	V _{out} = 1.2 V (middle code)		20	150	μV
				0.54	4.1	LSB
LR _{source}	Output load regulation with 1 mA output source current			20	150	μV
				0.54	4.1	LSB
Ge	Gain error	V _{ref} = 1.2 V	-0.35	-0.55	-0.75	%
dGe/dT	Gain error drift vs. temperature	V _{ref} = 1.2 V, average value		2.4		ppm/°C
		V _{ref} = 1.2 V, standard deviation		1.3		
O _e	Offset error (after a calibration sequence) ⁽⁴⁾	V _{ref} = 1.2 V	-150		150	μV
			-4.1		4.1	LSB

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
dOe/dT	Offset error drift vs. temperature, calibration at -55 °C and 125 °C	Vref = 1.2 V, average value		0.9		$\mu\text{V}/^\circ\text{C}$
		Vref = 1.2 V, standard deviation		0.3		
INL	Integral non-linearity (guaranteed by distortion measurement)	Vref = 1.2 V, LSB = 36.6 μV	-4.5	± 2.5	+4.5	LSB
dINL/dT	Linearity error drift vs. temperature	Vref = 1.2 V, average value		5.4		mLSB/ $^\circ\text{C}$
		Vref = 1.2 V, standard deviation		0.8		
DNL	Differential non-linearity	Vref = 1.2 V, Ta = 25 °C		± 0.3		LSB
N	Noise level for Vref = 1.2 V and BW = 0.1 Hz - 10 Hz	Ta = -55 °C		21		μVrms
		Ta = 25 °C		15		
		Ta = 125 °C		13		
	Noise level for Vref = 1.2 V and BW = 10 Hz - 3 kHz	Ta = -55 °C		12		
		Ta = 25 °C		16	19	
		Ta = 125 °C		24		
en	Spectral noise density at 1 kHz and Vref = 1.2 V	Ta = -55 °C		215		nV/V/Hz
		Ta = 25 °C		260	345	
		Ta = 125 °C		370		
SNR	Output signal to noise ratio		93	96		dB
SFDR	Spurious free dynamic range	Vref = 1.2 V, BW = 10 Hz - 3 kHz, sine at 64 Hz and -1 dBFS, Ta = 25 °C	89.5		-89.5	dBc
THD						
	H3				-100	
St	Settling time at 0.1 % on 100 pF load	BW = 3 kHz, Ta = 25 °C		0.8		ms
SYNC OUT freq.	Master clock divided by OSR (OSR = 256)	Internal MCLK	9.6	12	14.4	kHz
		External MCLK	9.6	12	14.4	
SYNC OUT pulse ⁽⁵⁾⁽⁶⁾	SYNC OUT pulse duration, tpulse = 8/MCLKx	Internal MCLK	2.2	2.66	3.32	μs
		External MCLK	2.2	2.66	3.32	
Sample rate	DAC sample rate (MCLK/256)	Internal MCLK	9.6	12	14.4	ksps
		External MCLK	9.6	12	14.5	
Iref	Input reference current	Vref = 1 V to 1.4 V			1	μA
PSRR	Power supply rejection ratio	100 Hz/200 mVpp ripple		80		dB
TWU ⁽⁷⁾⁽⁶⁾	Wakeup time (during TWU, the DAC cannot be used) ⁽⁸⁾		230	310	440	ms

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
CALT ⁽⁶⁾	Calibration time (during CALT, the DAC cannot be used) ⁽⁹⁾			20	40	
Vwu	Wakeup output voltage	During TWU		Vref		

Notes:

- (1) In case of external master clock, IccD is divided by 2.
(2) In case of external master clock, add 20 μ A to 30 μ A to IccIO.
(3) If PDN connected to IOVCC pin, add I_{IH} current.
(4) Due to internal ADC LSB value calibration sequencer, after each calibration a difference of about 20 to 30 μ V can be observed.
(5) Guaranteed by design
(6) Post irradiation test measurement is not performed, however this parametric limits are guaranteed by characterization
(7) Settling time of analog output filter is not taken into account
(8) Add calibration time (CALT) for the total wake-up time (TWU)
(9) Tested during offset error test by applying a calibration time lower than the maximum time specified.

Unless otherwise specified, the test conditions in [Table 14: "Timing characteristics"](#) are: AVCC = DVCC = 3 V to 3.6 V, IOVCC = 1.6 V to 3.6 V, T_{amb} = -55 °C to 125 °C. Conditions are guaranteed by design, correlation, and pattern tests.

Table 14: Timing characteristics

Symbol	Parameter	Min	Max	Unit
t1 ⁽¹⁾	Internal POR high level to ARSTN high level threshold	100		μ s
t2 ⁽¹⁾	ARTN high level threshold to PDN high level threshold	50		ns
t3 ⁽¹⁾	PDN high level threshold to CS low level threshold	1		ms
t4 ⁽¹⁾	PDN high level threshold to stable output voltage without any SPI commands	230	480	ms
t5 ⁽¹⁾	CS high level threshold to effective output voltage change		5500/MCLK	s
t6 ⁽¹⁾	PDN low level threshold to effective HiZ output		5	ms
t7 ⁽¹⁾	Internal POR low level to effective HiZ output (to do with PDN falling before)		5	
t8 ⁽¹⁾⁽²⁾	PDN high level threshold to effective SYNC OUT signal ON		490	
t9 ⁽¹⁾⁽²⁾	PDN low level threshold to effective SYNC OUT signal OFF		10	
t10 ⁽¹⁾	ARSTN low level threshold to SYNC OUT signal OFF		100	μ s
t11 ⁽¹⁾	PDN high level threshold to first calibration sequence	t4 max + 100 μ s		ms
t12 ⁽¹⁾	MCLK OFF before PDN high level threshold		500	μ s
t13 ⁽¹⁾	MCLK ON after PDN low level threshold	500		
t14 ⁽¹⁾	PDN pulse width low	20		ms
t15 ⁽¹⁾	ARSTN pulse width low	1		

Symbol	Parameter	Min	Max	Unit
t16 ⁽¹⁾	CS low level threshold to rising edge of SCLK	1		ns
t17 ⁽¹⁾	Data setup time	25		ns
t18 ⁽¹⁾	Data hold time	25		
t19 ⁽¹⁾	SCLK period	125		
t20 ⁽¹⁾	SCLK low time	50		
t21 ⁽¹⁾	SCLK high time	50		
t22 ⁽¹⁾	SCLK rising edge to CS high level threshold	1		
t23 ⁽¹⁾	Minimum CS time at high level	5		
t24 ⁽¹⁾	SDOUT setup time	25		ns
t25 ⁽¹⁾	SDOUT hold time	25		
t26 ⁽¹⁾	VCCA, DVCC, IOVCC positive slew rate	300	0.003	V/ms
t27 ⁽¹⁾	Delay between POR high level to AVCC min. value		100	ms
t28 ⁽¹⁾	Delay between AVCC min., value to IOVCC min. value		100	
t29 ⁽¹⁾	VCCA, DVCC, IOVCC negative slew rate	300	0.003	V/ms
t30 ⁽¹⁾	Delay between POR low level to DVCC = 0.5 V		100	ms
t31 ⁽¹⁾	Delay between POR low level to IOVCC = 0.5 V		100	

Notes:

⁽¹⁾Post irradiation test measurement is not performed, however this parametric limits are guaranteed by characterization.

⁽²⁾See [Section 4.1.1: "SPI frame format"](#).

Figure 22: DAC timing diagram 1

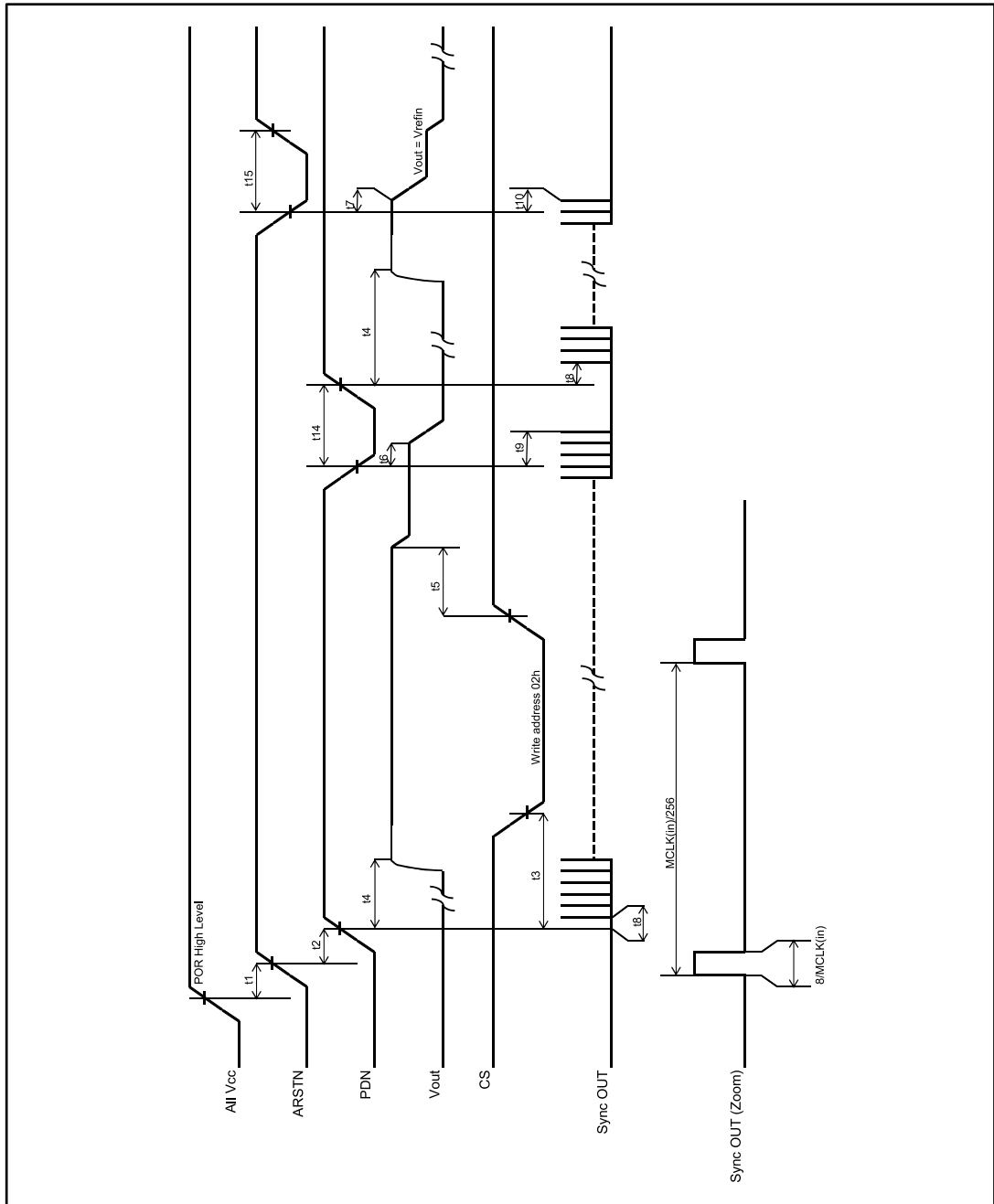


Figure 23: DAC timing diagram 2

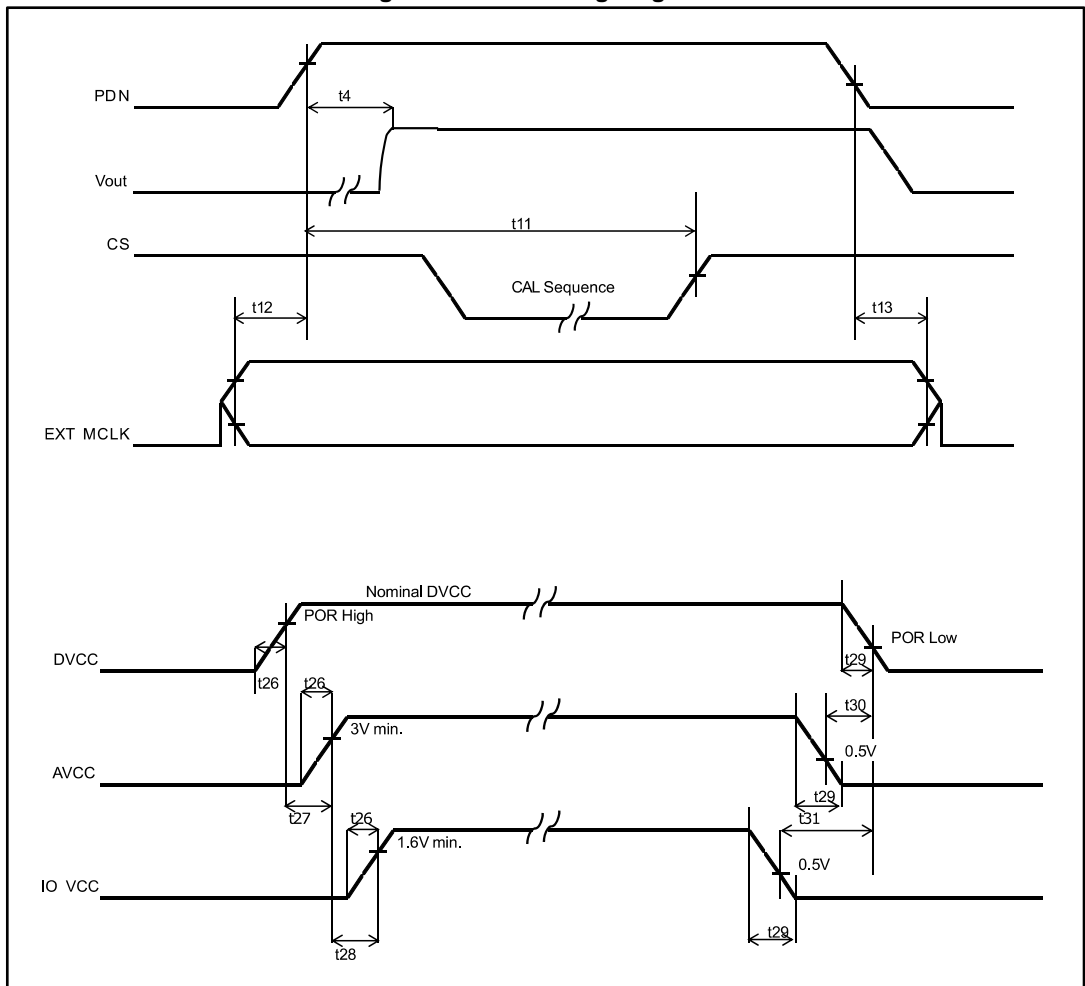
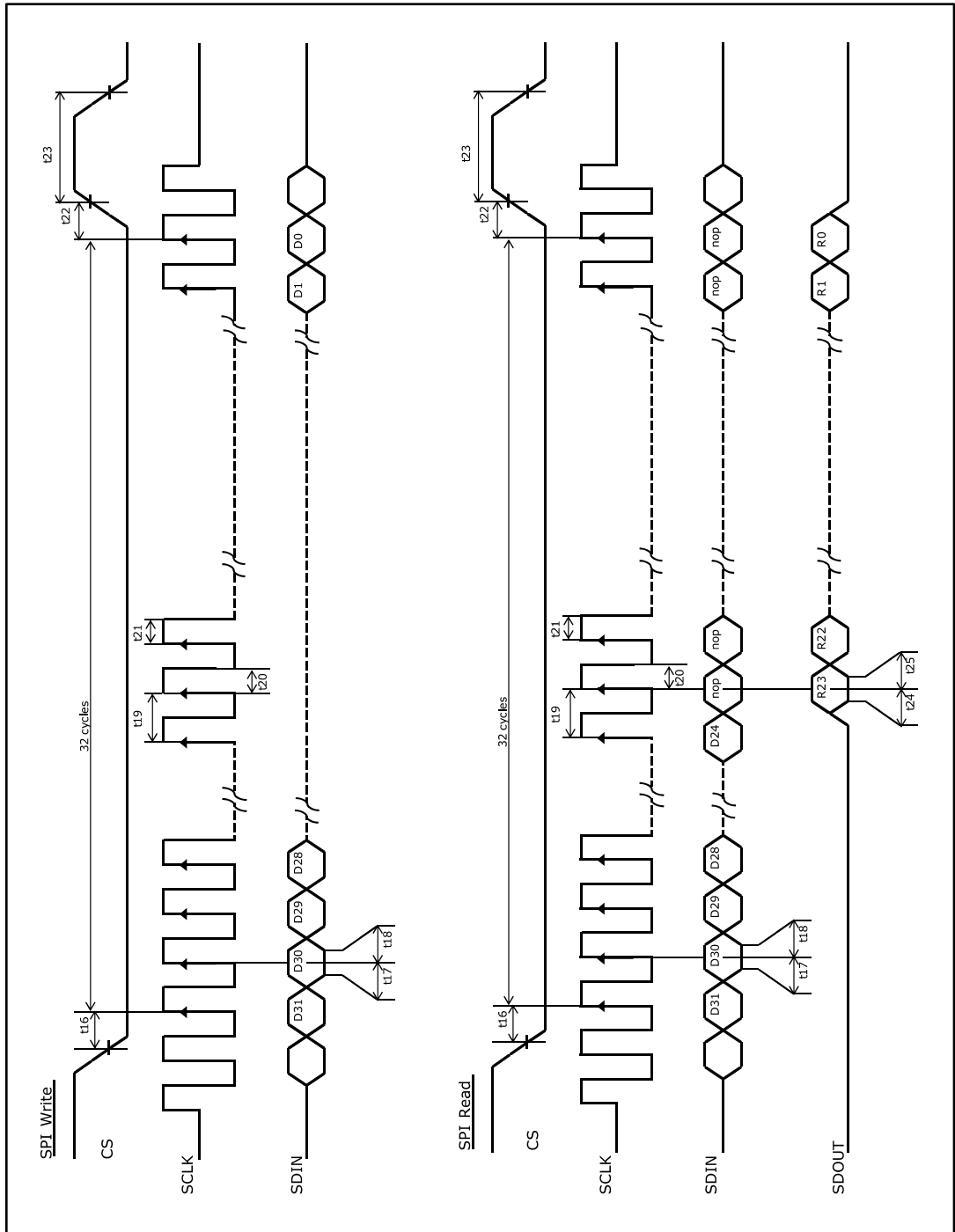


Figure 24: DAC timing diagram 3



7 Electrical characteristic curves

Figure 25: INL vs. input code, internal master clock, AVCC = 3.3 V

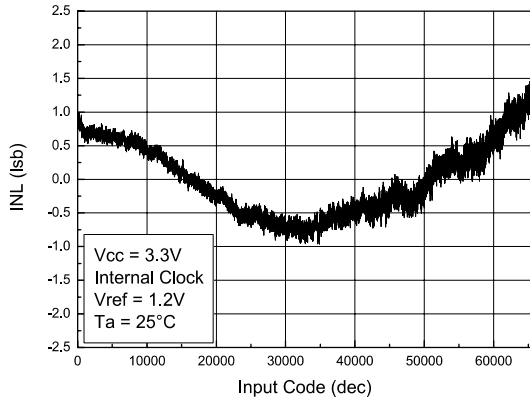


Figure 26: DNL vs. input code, internal master clock, AVCC = 3.3 V

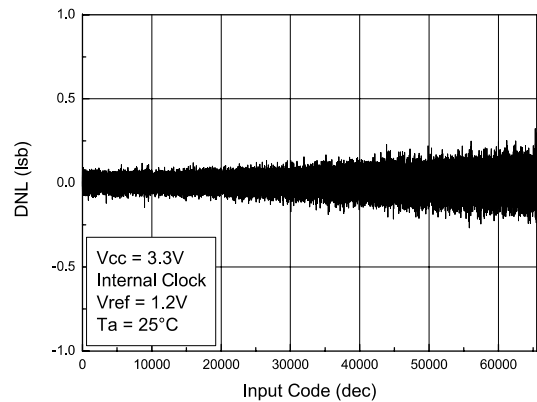


Figure 27: INL vs. input code, external master clock, AVCC = 3.3 V

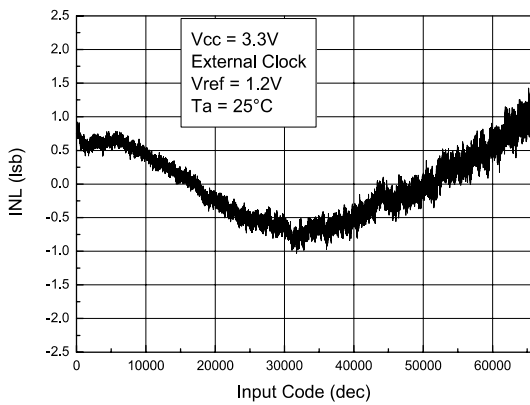


Figure 28: DNL vs. input code, external master clock, AVCC = 3.3 V

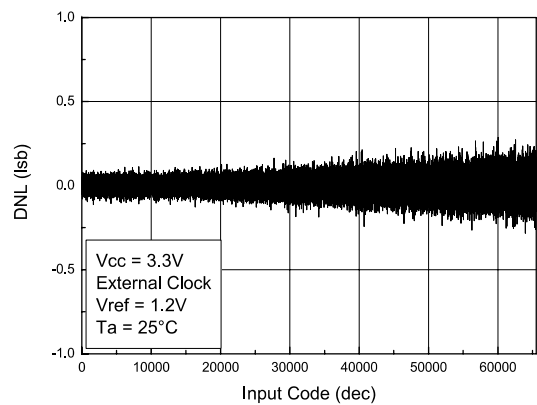


Figure 29: INL vs. input code, internal master clock, AVCC = 3 V

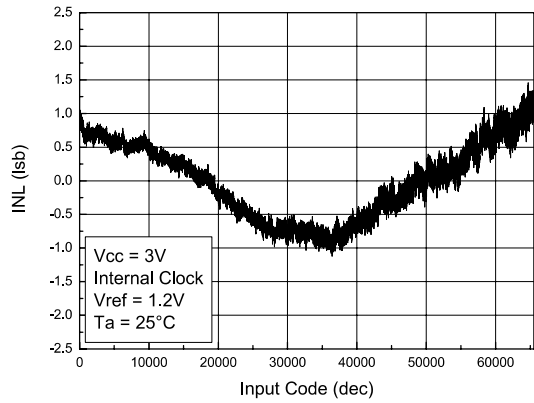


Figure 30: DNL vs. input code, internal master clock, AVCC = 3 V

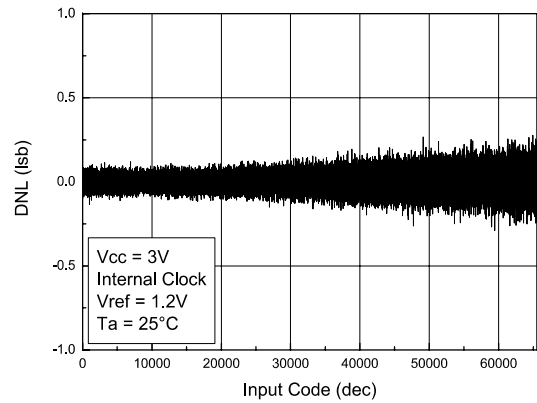


Figure 31: INL vs. input code, internal master clock, AVCC = 3.6 V

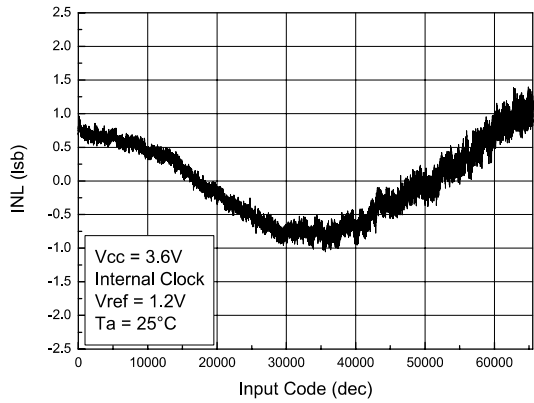


Figure 32: DNL vs. input code, internal master clock, AVCC = 3.6 V

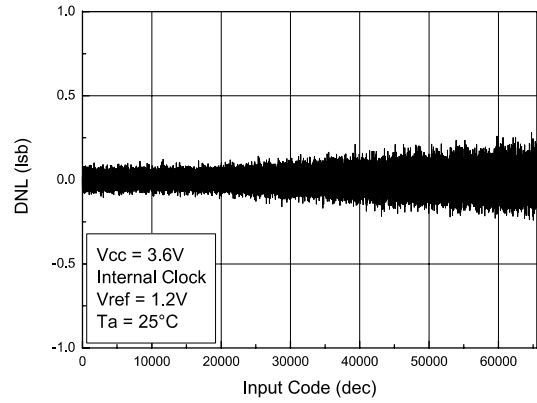


Figure 33: INL vs. input code vs. temperature, internal master clock, AVCC = 3 V

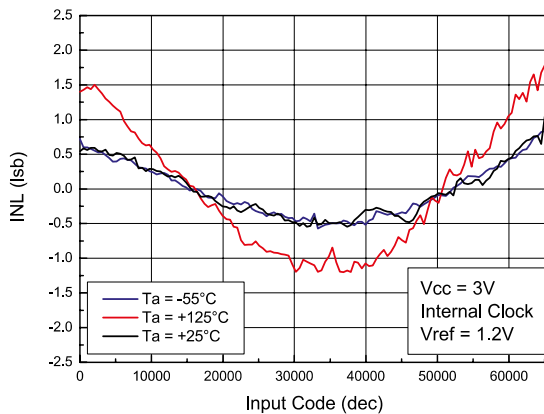
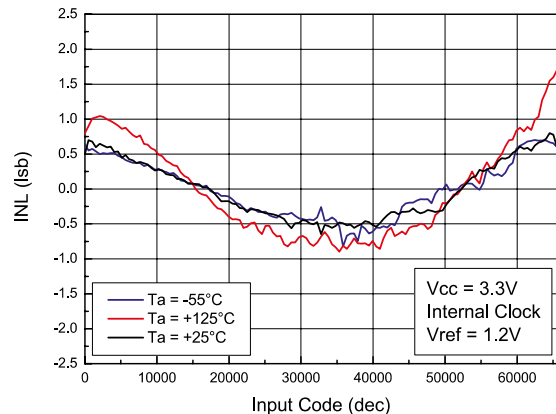
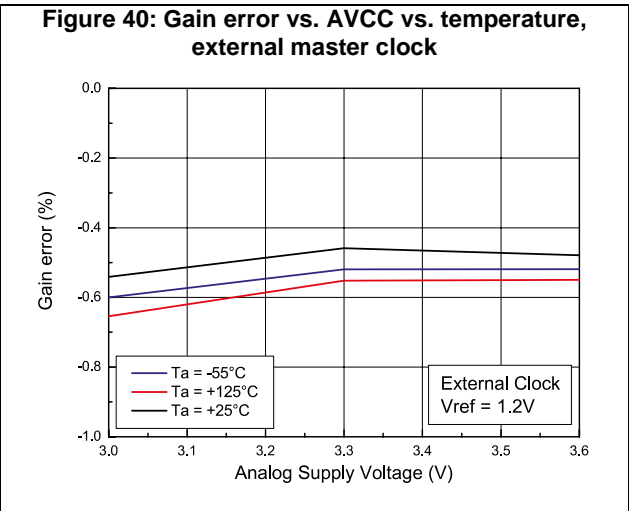
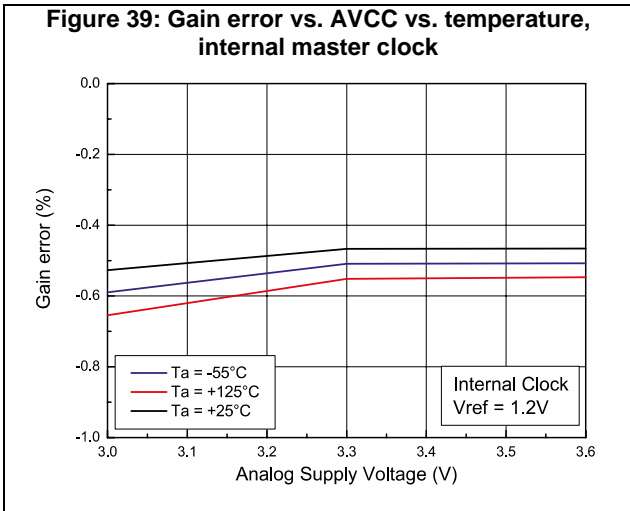
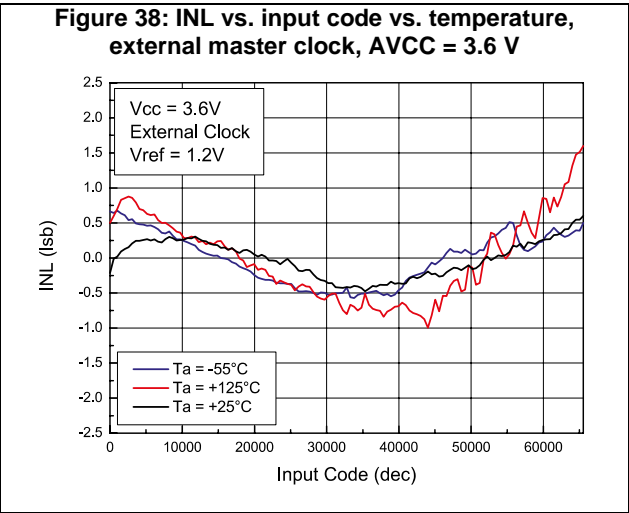
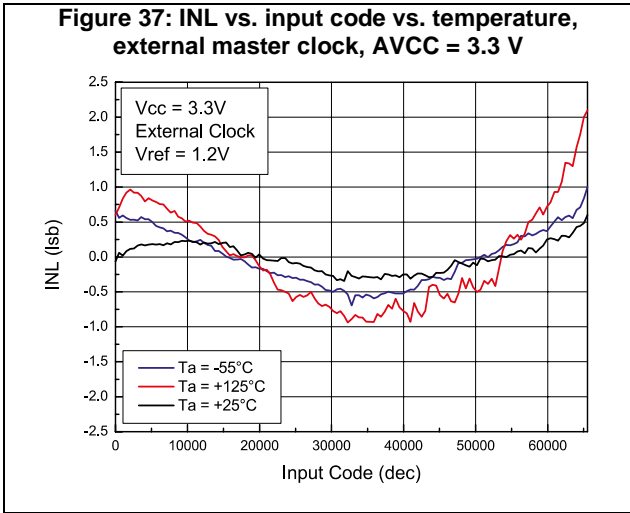
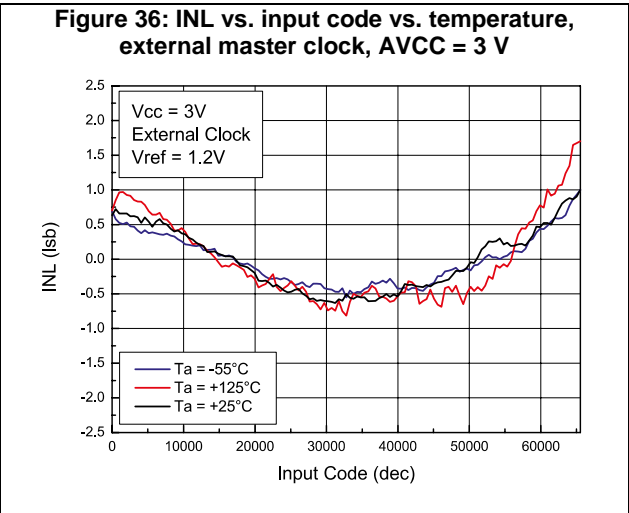
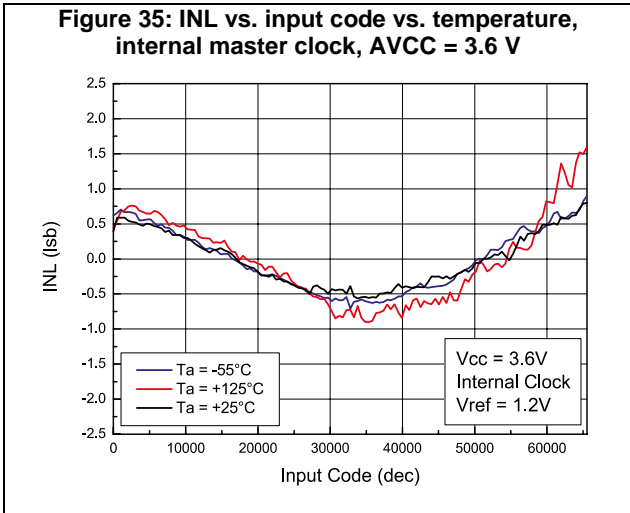


Figure 34: INL vs. input code vs. temperature, internal master clock, AVCC = 3.3 V





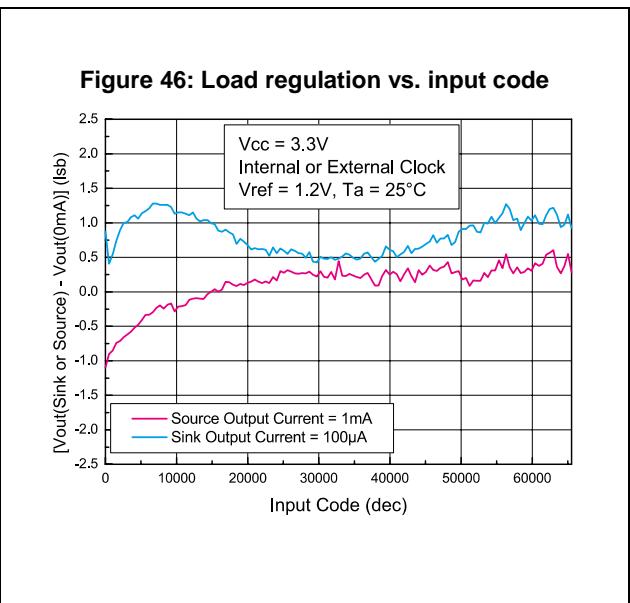
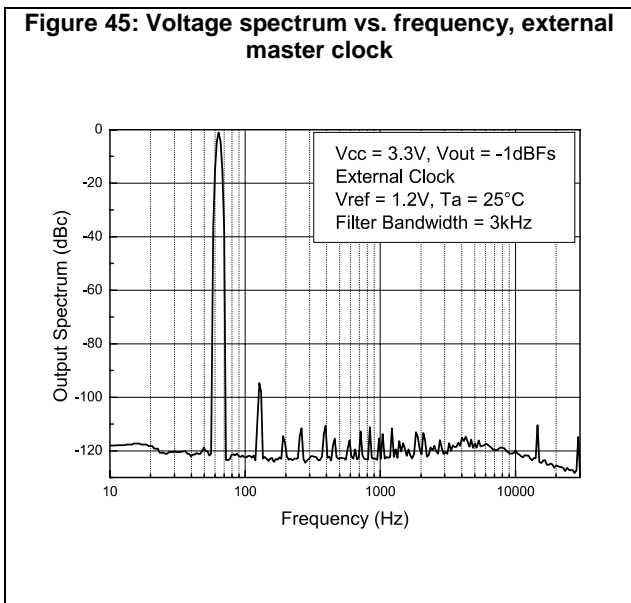
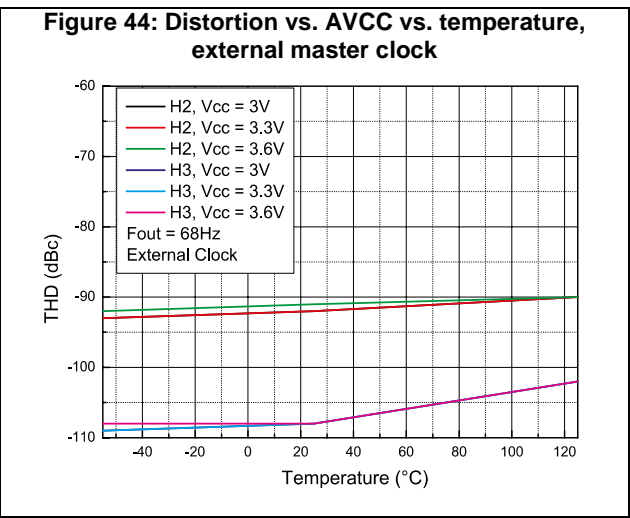
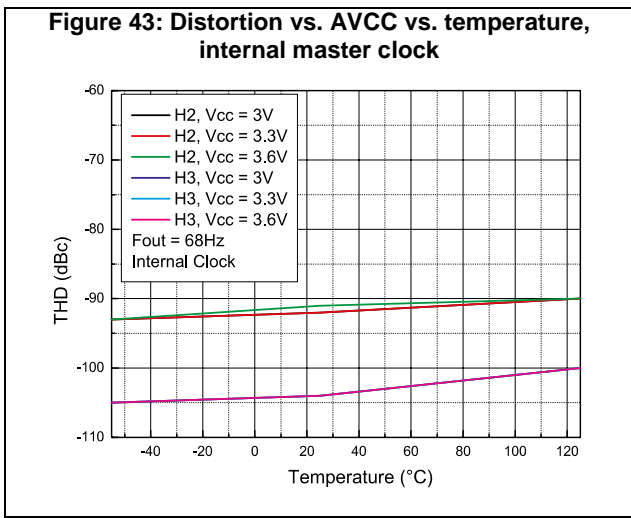
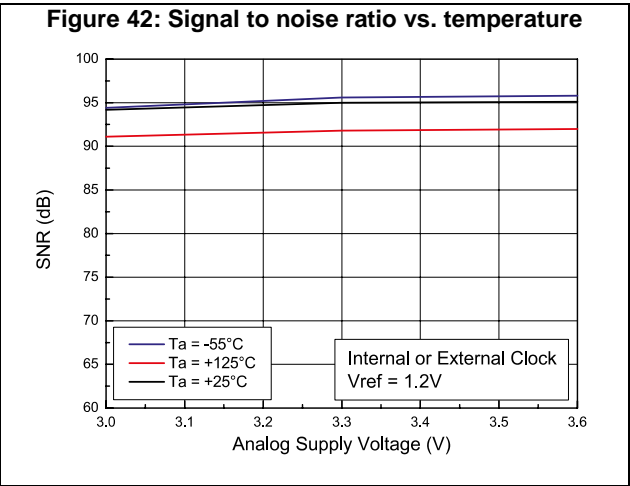
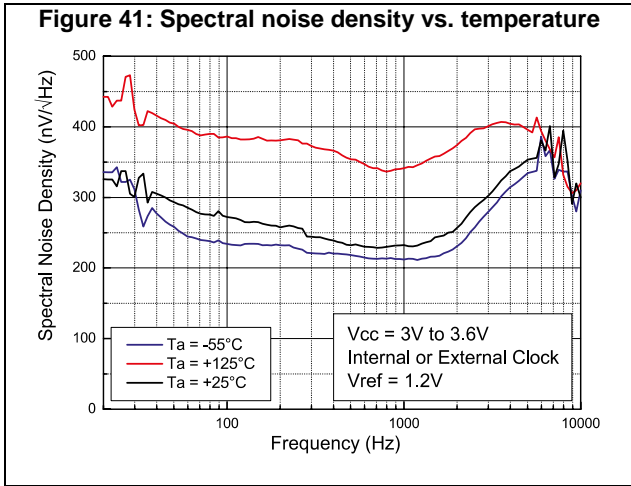


Figure 47: PSRR vs. frequency vs. temperature, lower code input

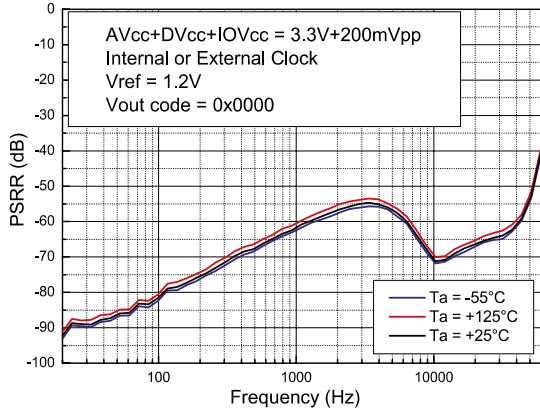


Figure 48: PSRR vs. frequency vs. temperature, middle code input

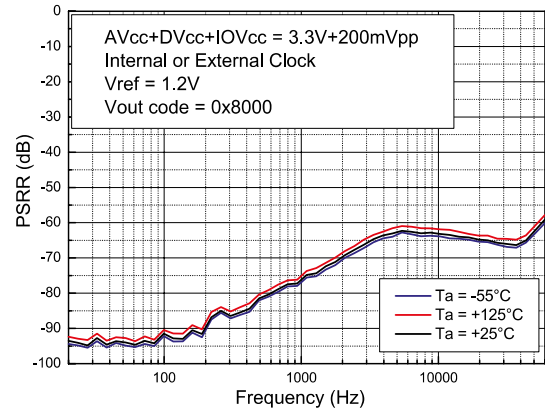
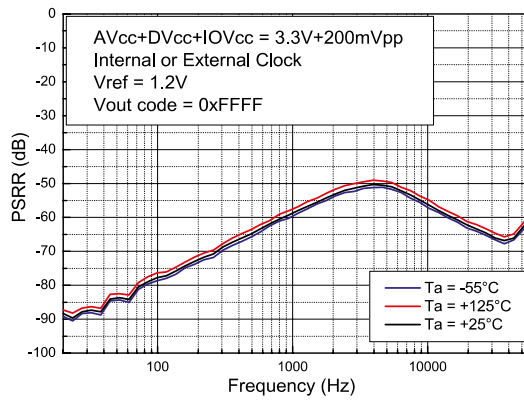


Figure 49: PSRR vs. frequency vs. temperature, higher code input

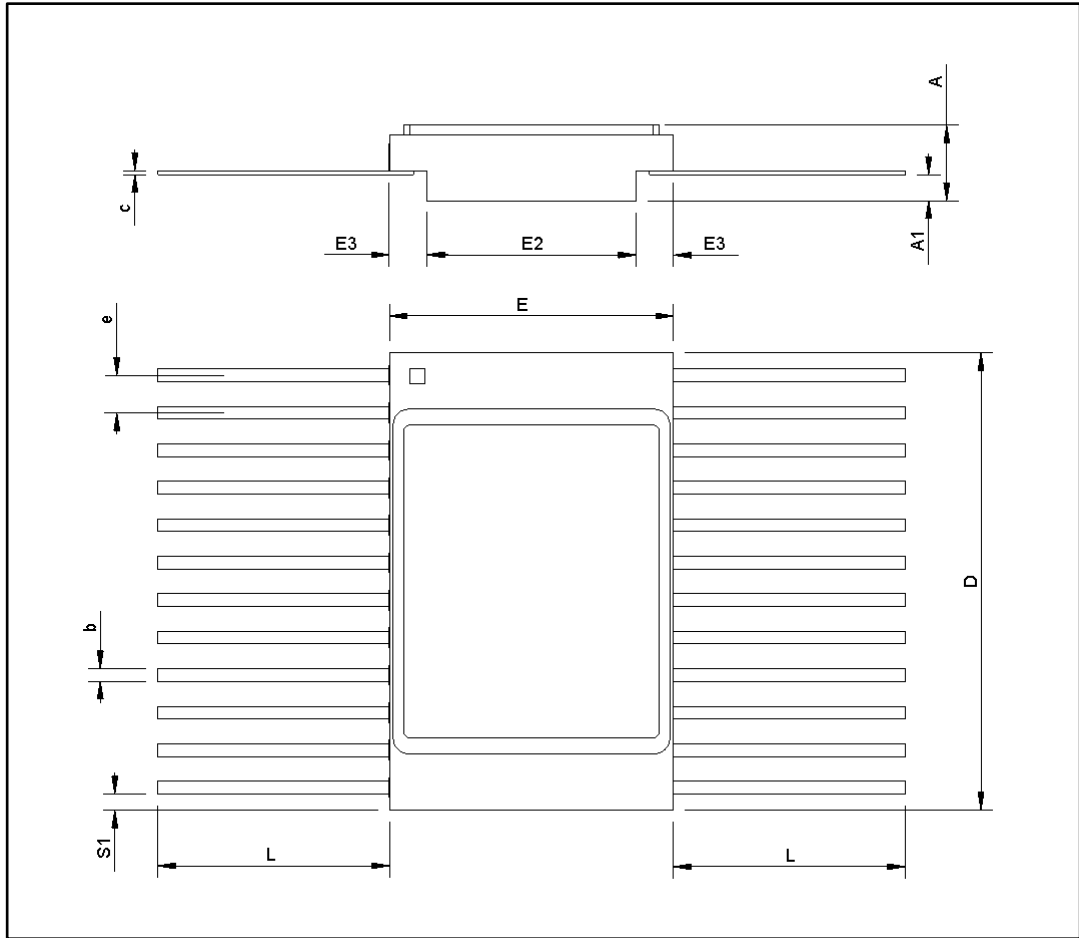


8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 Ceramic Flat-24 package information

Figure 50: Ceramic Flat-24 package outline



1. The upper metallic lid is electronically connected to pin number 8 (DGND)

Table 15: Ceramic Flat-24 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.31	2.54	2.77	0.091	0.100	0.109
A1	0.66		1.14	0.026		0.045
b	0.38	0.33	0.48	0.015	0.013	0.019
c	0.1	0.125	0.15	0.004	0.005	0.006
D	15.34	15.49	15.64	0.604	0.610	0.616
E	9.52		9.78	0.375		0.385
E2	6.96		7.26	0.274		0.286
E3		1.27			0.050	
e		1.27			0.050	
L	6.35		9.4	0.25		0.37
S1		0.13			0.005	

9 Ordering information

Table 16: Order codes

Order code	Description	Temp. range	Package	Marking ⁽¹⁾	Packing
RH-DAC1612K1	Engineering model	-55 °C to 125 °C	Flat-24	RH-DAC1612K1	Conductive strip pack
RHRDAC1612K01V	QML-V Flight model			5962R1621101VXC	

Notes:

⁽¹⁾Specific marking only. Complete marking includes the following: - ST logo - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week) - Country of origin (FR = France).



Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

Date code

The date code is structured as follows: EM (engineering model) = xyywwz

Where:

- x (EM only): 3, assembly location Rennes (France)
- yy: last two digits year
- ww: week digits
- z: lot index in the week

10 Revision history

Table 17: Document revision history

Date	Revision	Changes
07-Mar-2017	1	Initial release
06-Nov-2017	2	Added QML-V Flight Model references. Minor changes throughout the document.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved