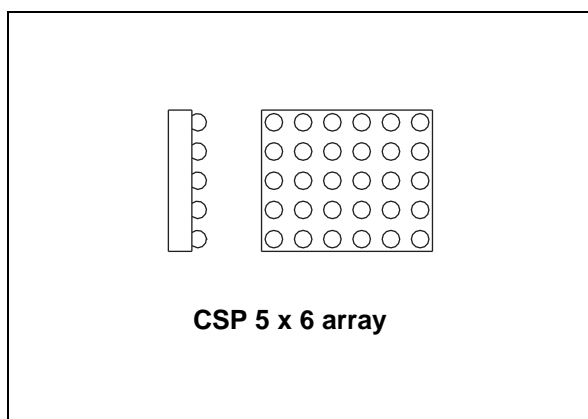


2-channel microless high-efficiency digital audio system Sound Terminal®

Datasheet - production data



Features

- Wide-range supply voltage (4.5 V - 18 V)
- 2 channels of ternary PWM (stereo mode)
- 2 channels of 24-bit FFX™
- 100 dB SNR and dynamic range
- Digital gain +24dB
- Sample rates (fs) from 32 to 48 kHz
- Fixed MCLK at 256 x fs
- Automatic zero-detect mute
- Automatic invalid input detect mute
- Short-circuit detection at startup (Out-V_{CC}, Out-Gnd, Out 1b-Out 2a)
- 2-channel I²S input data interface
- 2 Hz DC cut filter (input)
- 96 kHz internal processing sample rate, 24-bit precision
- Embedded thermal-overload and short-circuit protection

Applications

- LCDs
- DVDs
- Cradles
- Digital speakers
- Wireless-speaker cradles

Description

The STA333SML is an integrated circuit comprising digital audio processing, digital amplifier control and an FFX power output stage to create a high-power, single-chip FFX solution for all-digital amplification with high quality and high efficiency.

The STA333SML power section consists of four independent half-bridge stages. Two channels can be provided by two full bridges, providing up to 10 W + 10 W of power.

Also featured in the STA333SML are new advanced modes for AM radio interference reduction. The serial audio data input interface accepts the popular I²S format. Two channels of FFX™ processing are provided.

The STA333SML is part of the Sound Terminal® family that provides full digital audio streaming to the speaker, offering cost effectiveness, low-power dissipation and sound enrichment.

Table 1. Device summary

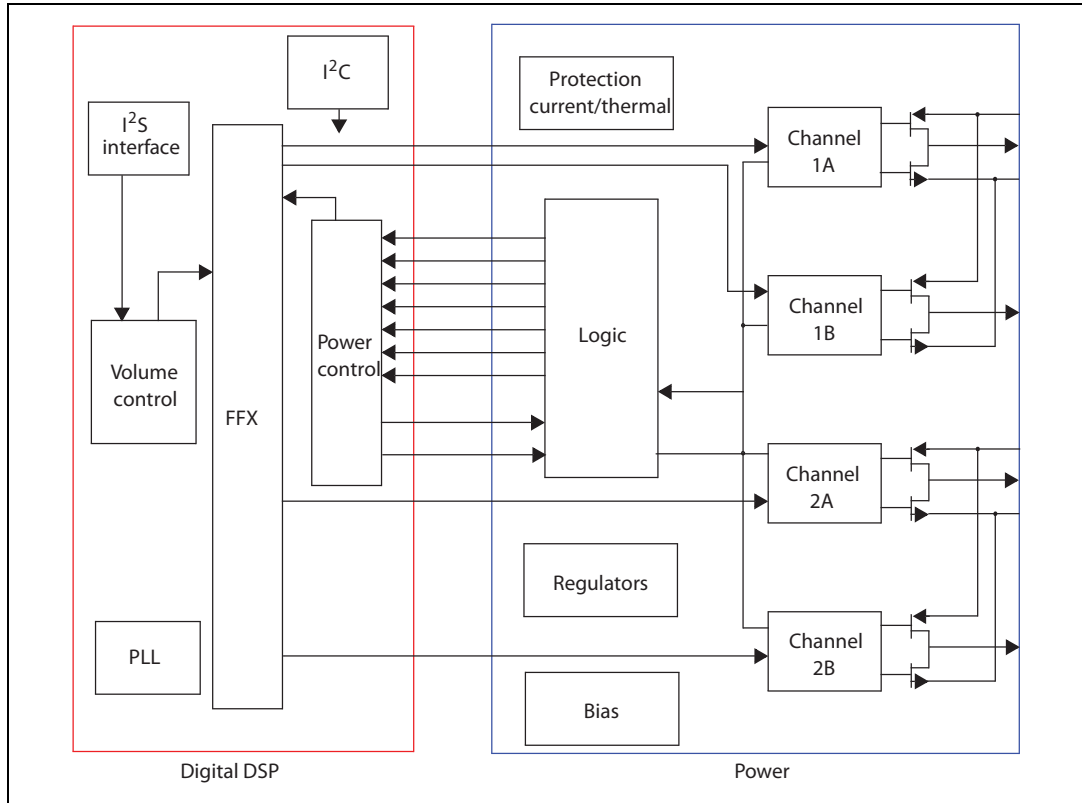
Order code	Package	Packaging
STA333SML	CSP 5x6 array	Tube
STA333SMLTR	CSP 5x6 array	Tape and reel

Contents

- 1 Block diagram 3**
- 2 Pin description 4**
 - 2.1 Pinout 4
 - 2.2 Pin list 5
- 3 Electrical specifications 6**
 - 3.1 Absolute maximum ratings 6
 - 3.2 Thermal data 6
 - 3.3 Recommended operating conditions 7
 - 3.4 Electrical specifications - digital section 7
 - 3.5 Electrical specifications - power section 8
 - 3.6 Power-off sequence 10
 - 3.7 Testing 10
 - 3.8 Serial audio interface description 11
 - 3.8.1 Serial audio interface protocols 11
 - 3.9 Application information 12
- 4 Package mechanical data 13**
 - 4.1 Soldering information 15
- 5 Revision history 16**

1 Block diagram

Figure 1. Block diagram



2 Pin description

2.1 Pinout

Figure 2. Pin connections (package top view)

	1	2	3	4	5
A	GND1	OUT1A	NC	VDDREG	SDI
B	GND1	VCC1	NC	LRCKI	VDD_DIG
C	OUT1B	VCC1	GNDREG	BICKI	GND_DIG
D	OUT2A	VCC2	VCCREG	SDA	XTI
E	GND2	VCC2	NC	SCL	VDD_PLL
F	GND2	OUT2B	NC	VSS	GND_PLL

2.2 Pin list

Table 2. Pin description

Pin n°	Name	Description	Pad information
I/O pins			
B4	LRCKI	I ² S Left/Right clock	
C4	BICKI	I ² S serial clock	
A5	SDI	I ² S serial data channels 1 & 2	
D5	XTI	Master clock input	
E4	PWDN	'0' = power-down; '1'=normal operation	
D4	INTLINE	'0' = power bridge in fault; '1'=normal operation	
Power output pins			
A2	OUT1A	Positive output 1	
C1	OUT1B	Negative output 1	
D1	OUT2A	Positive output 2	
F2	OUT2B	Negative output 2	
Power supplies (preliminary)			
B2/C2	VCC1	Positive supply (upper MOSFET) to left H-bridge P output	
E2/D2	VCC2	Positive supply (upper MOSFET) to right H-bridge P output	
A1/B1	GND1	Negative supply (lower MOSFET) to left H-bridge P output	
E1/F1	GND2	Negative supply (lower MOSFET) to right H-bridge P output	
D3	VCCREG	Reference voltage to V _{CC}	These pins are output pins that must be externally filtered. Do not connect these pins to external supply voltage.
C3	GNDREG	Reference voltage to ground	
A4	VDDREG	Reference voltage to 3.3 V	
F4	VSS	Reference voltage to V _{CC} - 3.3 V	
B5	VDD_DIG	Digital supply	
C5	GND_DIG	Digital ground	
E5	VDD_PLL	PLL supply	
F5	GND_PLL	PLL ground	
A3, B3, E3, F3	NC	Not connected	

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Analog supply voltage (pins VCCx)	-0.3	-	20	V
V_{DD}	Digital supply voltage (pins VDD_DIG)	-0.3	-	4.0	V
I_L	Logic input interface	-0.3	-	4.0	V
T_{op}	Operating junction temperature	0	-	150	°C
T_{stg}	Storage temperature	-40	-	150	°C

Warning: Stresses beyond those listed in [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Table 5: Recommended operating conditions](#) are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. In the real application, a power supply with nominal value rated within the limits of the recommended operating conditions may rise beyond the maximum operating conditions for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{Th(j-case)}$	Thermal resistance junction to ambient	-	51.5		°C/W
T_{sd}	Thermal-shutdown junction temperature	140	150	160	°C
T_w	Thermal-warning temperature	-	130	-	°C
T_{hsd}	Thermal-shutdown hysteresis	18	20	22	°C

3.3 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Analog supply voltage (VCCx)	4.5	-	18	V
V_{DD}	Digital supply voltage (VDD_DIG)	3.0	3.3	3.6	V
I_L	Logic input interface	3.0	3.3	3.6	V
T_{amb}	Ambient temperature	0	-	70	°C

3.4 Electrical specifications - digital section

Table 6. Electrical characteristics for digital section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{il}	Input current, no pull-up or pull-down resistor	$V_i = 0\text{ V}$	-	-	± 10	μA
I_{ih}		$V_i = V_{DD} = 3.6\text{ V}$	-	-	± 10	μA
V_{il}	Low-level input voltage	-	-	-	$0.2^* V_{DD}$	V
V_{ih}	High-level input voltage	-	$0.8^* V_{DD}$	-	-	V
V_{ol}	Low-level output voltage	$I_{ol} = 2\text{ mA}$	-	-	$0.4^* V_{DD}$	V
V_{oh}	High-level output voltage	$I_{oh} = 2\text{ mA}$	$0.8^* V_{DD}$	-	-	V
I_{pu}	Pull-up current	-	25	66	125	μA
R_{pu}	Equivalent pull-up resistance	-	-	50	-	$\text{k}\Omega$

3.5 Electrical specifications - power section

The specifications in [Table 7](#) below are given for the conditions $V_{CC} = 13\text{ V}$, $V_{DD} = 3.3\text{ V}$, $f_{SW} = 384\text{ kHz}$, $T_{amb} = 25\text{ °C}$ and $R_L = 8\ \Omega$, unless otherwise specified.

Table 7. Electrical specifications for power section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	THD = 1%	-	8	-	W
		THD = 10%	-	10	-	
R _{dsON}	Power P-channel/N-channel MOSFET (total bridge)	I _d = 1 A	-	106		mΩ
I _{dss}	Power P-channel/N-channel leakage	V _{CC} = 18 V	-	-	10	μA
gP	Power P-channel R _{dsON} matching	I _d = 1 A	95	-	-	%
gN	Power N-channel R _{dsON} matching	I _d = 1 A	95	-	-	%
I _{LDT}	Low-current dead time (static)	Resistive load, refer to Figure 4	-	5	10	ns
I _{HDT}	High-current dead time (dynamic)	Refer to Figure 5	-	10	20	ns
t _r	Rise time	Resistive load, refer to Figure 4	-	8	10	ns
t _f	Fall time	Resistive load, refer to Figure 4	-	8	10	ns
V _{CC}	Supply voltage	-	4.5	-	18	V
I _{VCC}	Supply current from V _{CC} in power down	PWRDN = 0	30	60	200	μA
	Supply current from V _{CC} in operation	PCM input signal = -60 dBFS Switching frequency = 384 kHz No LC filters	-	30	50	mA
I _{VDD_DIG}	Supply current for FFX processing (reference only)	Internal clock = 49.152 MHz	10	30	50	mA
	Supply current in standby	-	8	11	25	mA
Av_DIG	Digital Gain			24		dBFS
I _{SCP}	Short-circuit protection	High-impedance output ⁽¹⁾	2.7	3.8	5.0	A
V _{OVP}	Overvoltage protection threshold			22.9		V
V _{UVP}	Undervoltage protection threshold	-	-	3.5	4.3	V
t _{min}	Output minimum pulse width	No load	20	30	60	ns

Table 7. Electrical specifications for power section (continued)

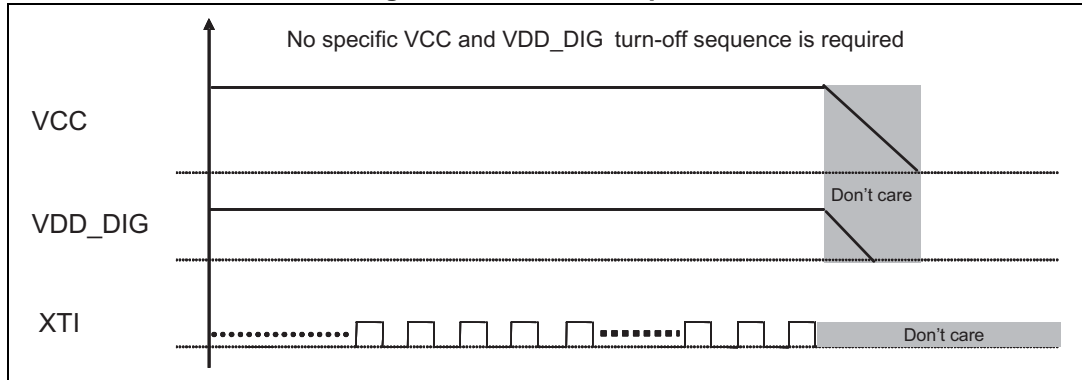
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD+N	Total harmonic distortion and noise	FFX stereo mode, $P_o = 1\text{ W}$, $f = 1\text{ kHz}$	-	0.05	0.2	%
DR	Dynamic range	-	-	100	-	dB
SNR	Signal to noise ratio in ternary mode	A-weighted	-	100	-	dB
	Signal to noise ratio in binary mode	A-weighted	-	90	-	
PSRR	Power supply rejection ratio	FFX stereo mode, $< 5\text{ kHz}$, $V_{\text{RIPPLE}} = 1\text{ V RMS}$ audio input = dither only	-	80	-	dB
X_{TALK}	Crosstalk	FFX stereo mode, $< 5\text{ kHz}$, One channel driven at 1 W the other channel measured	-	80	-	dB
η	Peak efficiency in FFX mode	$P_o = 2 \times 10\text{ W}$ into $8\ \Omega$	-	90	-	%

1. The I_{SCP} current limit data is for 1 channel of BTL configuration, thus, $2 * I_{\text{SCP}}$ drives the 2-channel BTL configuration.

3.6 Power-off sequence

The power-off sequence shown in *Figure 3* below ensures a pop-free turn-off.

Figure 3. Power-off sequence



3.7 Testing

Figure 4. Test circuit

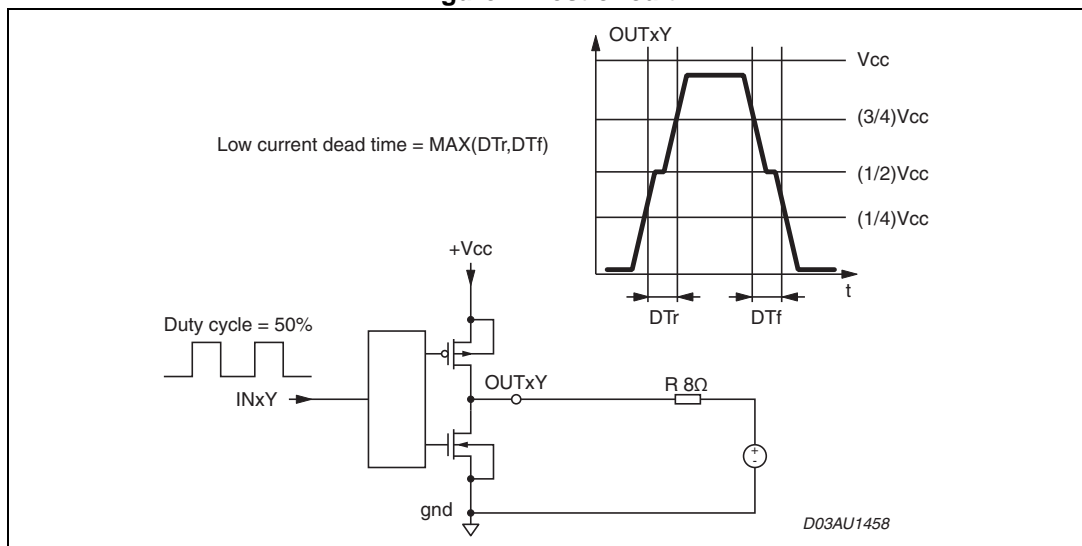
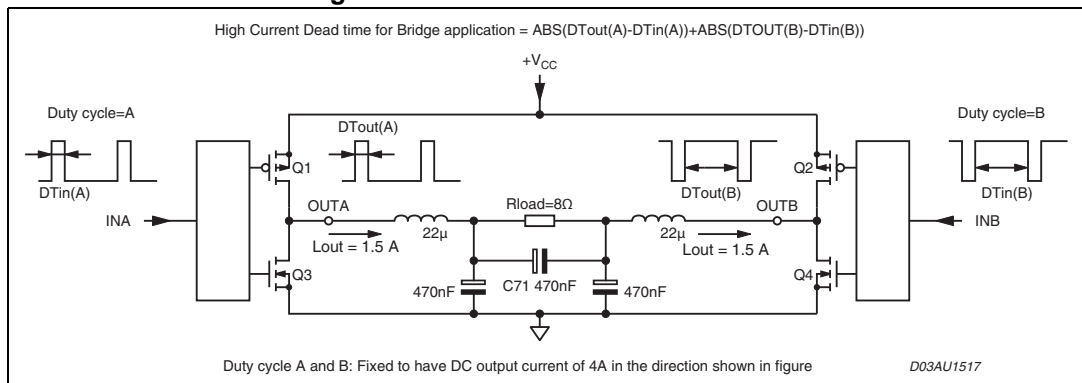


Figure 5. Current deadtime test circuit



3.8 Serial audio interface description

3.8.1 Serial audio interface protocols

The STA333SML serial audio input was designed to interface with standard digital audio components and to accept I²S formats. The STA333SML always acts as a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 input pins: left/right clock LRCKI (pin B4), serial clock BICKI (pin C4), and serial data SDI (pin A5).

The available formats are shown in *Figure 6*, *Figure 7* and *Figure 8*.

Figure 6. I²S - 16 fs

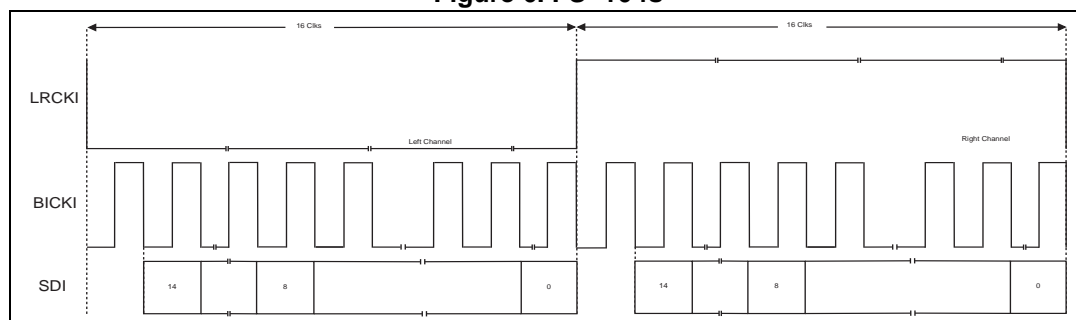


Figure 7. I²S - 24fs

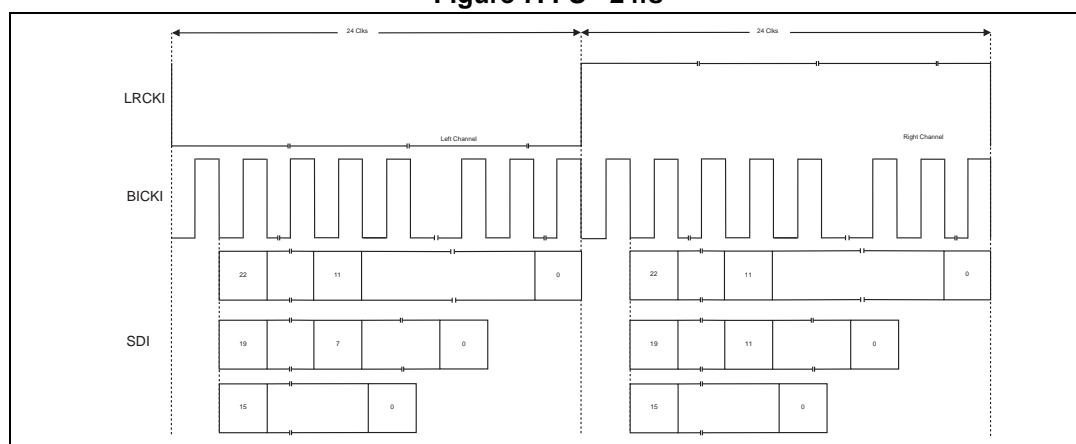
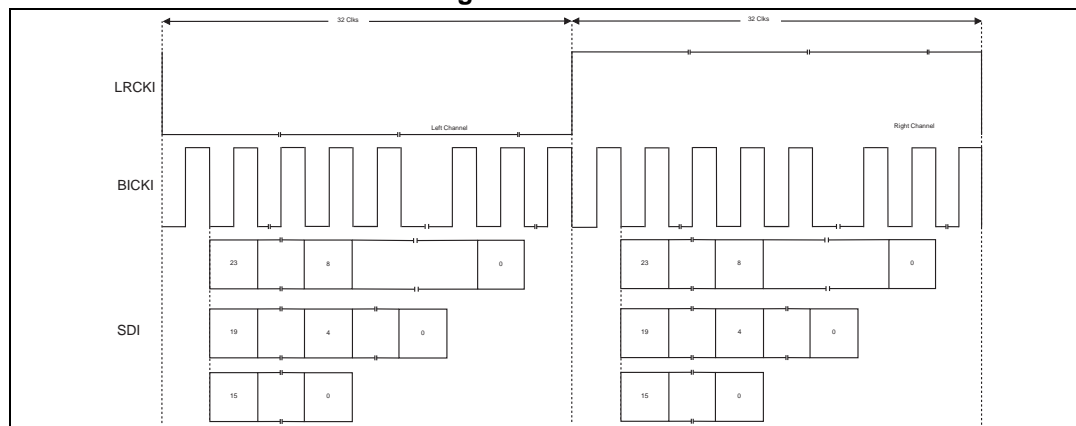
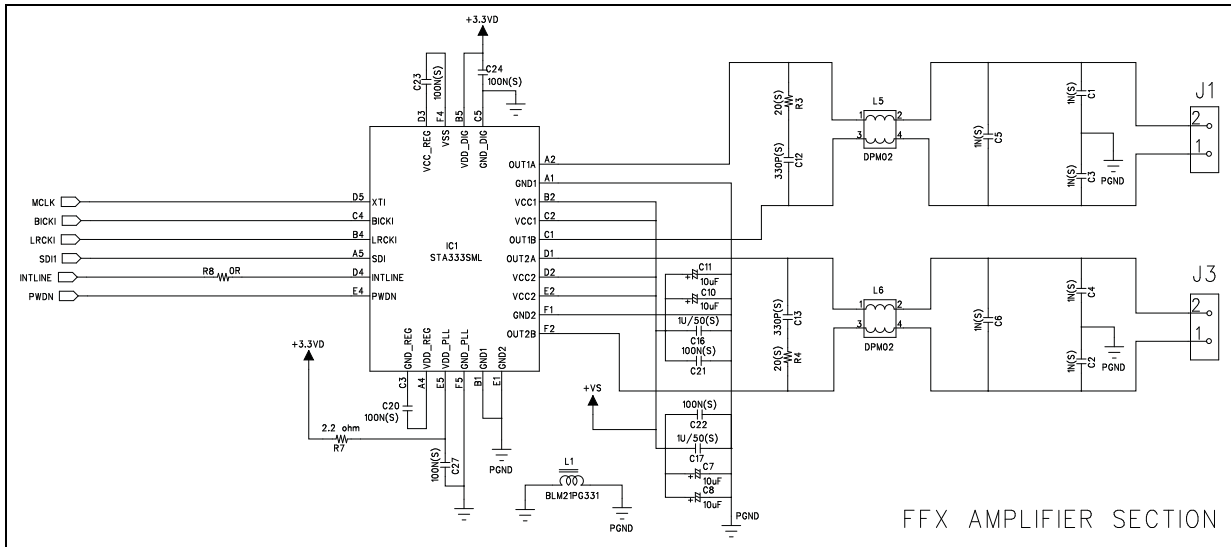


Figure 8. I²S - 32fs



3.9 Application information

Figure 9. Application diagram



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

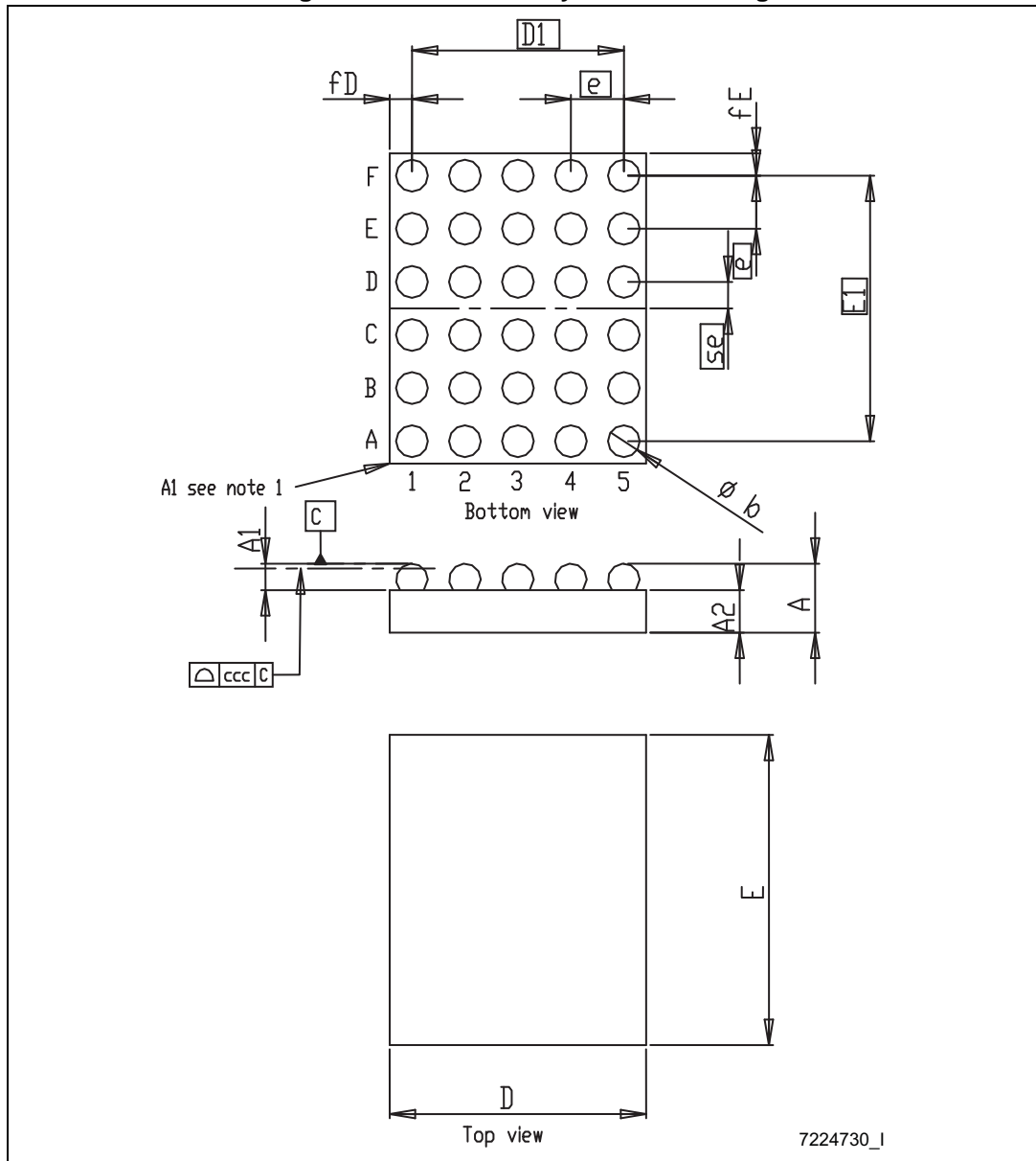
The STA333SML comes in a CSP 5x6 array package.

Figure 10 below shows the package outline and gives the dimensions.

Table 8. CSP 5x6 array package dimensions

Symbol	mm		
	Min	Typ	Max
A	0.585	0.65	0.715
A1	0.210	0.25	0.29
A2	0.38	0.4	0.42
b	0.265	0.315	0.365
D	2.52	2.57	2.62
D1		2	
E	3.19	3.24	3.29
E1		2.5	
e	0.45	0.5	0.55
se	0.2	0.25	0.3
fD	0.277	0.285	0.293
fE	0.362	0.370	0.378
ccc			0.08

Figure 10. CSP 5x6 array outline drawing



4.1 Soldering information

Figure 11. Recommended soldering reflow profile for mounting on PCB

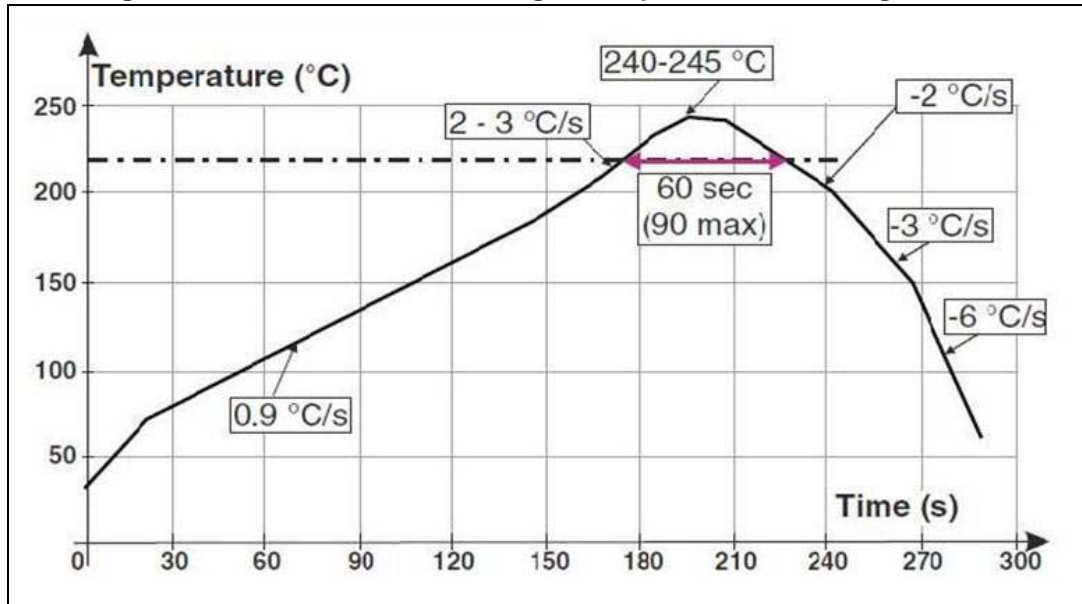


Table 9. Recommended soldering reflow values for mounting on PCB

Profile	Typ	Max
Temp. gradient in preheat (T=70-180°C)	0.9 °C/s	3 °C/s
Temp.gradient (T=200-225 °C)	2 °C/s	3 °C/s
Peak temp. in reflow	240-245 °C	260 °C
Time above 220 °C	60 s	90 s
Temp. gradient in cooling	-2 to -3 °C	-6 °C
Time from 50 to 220 °C	160 to 220 s	

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Oct-2013	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2013 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

