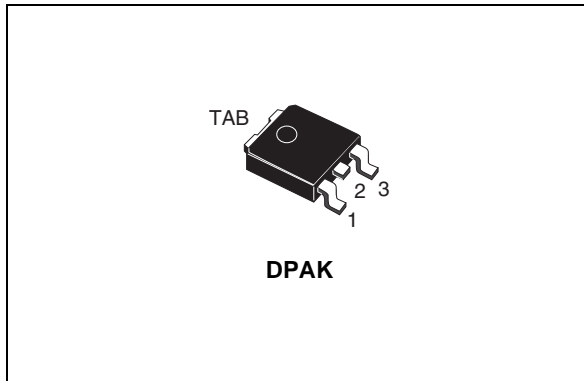


## P-channel 40 V, 0.013 $\Omega$ typ., 46 A, STripFET™ VI DeepGATE™ Power MOSFET in a DPAK package

Datasheet - preliminary data



### Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD46P4LLF6	40 V	0.017 $\Omega$	46 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate input resistance

### Applications

- Switching applications
- LCC converters, resonant converters

### Description

This device is a P-channel Power MOSFET developed using the 6<sup>th</sup> generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages

Figure 1. Internal schematic diagram

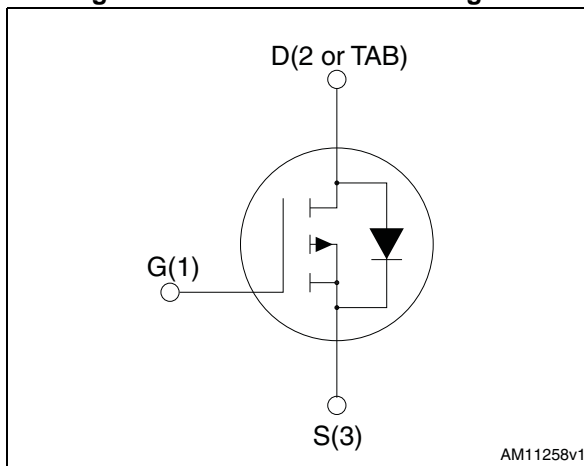


Table 1. Device summary

Order code	Marking	Package	Packaging
STD46P4LLF6	46P4LLF6	DPAK	Tape and reel

**Note:** For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	46	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	32.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	184	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	70	W
$T_{stg}$	Storage temperature	-55 to 175	°C
$T_j$	Max. operating junction temperature	175	°C

1. Pulse width limited by safe operating area.

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.14	°C/W

*Note:* For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 40\ \text{V}$ , ( $V_{GS} = 0$ )			1	$\mu\text{A}$
		$V_{DS} = 40\ \text{V}$ , $T_c = 125\text{ °C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{GS} = \pm 20\ \text{V}$ , ( $V_{DS} = 0$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 23\ \text{A}$		0.013	0.017	$\Omega$
		$V_{GS} = 4.5\ \text{V}$ , $I_D = 23\ \text{A}$		0.018	0.0235	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 32\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0$	-	2900	-	pF
$C_{oss}$	Output capacitance		-	400	-	pF
$C_{riss}$	Reverse transfer capacitance		-	150	-	pF
$Q_g$	Total gate charge	$V_{DD} = 24\ \text{V}$ , $I_D = 46\ \text{A}$ $V_{GS} = 4.5\ \text{V}$ (see <a href="#">Figure 3</a> )	-	30	-	nC
$Q_{gs}$	Gate-source charge		-	TBD	-	nC
$Q_{gd}$	Gate-drain charge		-	TBD	-	nC

*Note:* For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 32\text{ V}$ , $I_D = 23\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 2</a> )	-	TBD	-	ns
$t_r$	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
$t_f$	Fall time		-	TBD	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		46	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		184	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 23\text{ A}$ , $V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 23\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 16\text{ V}$ (see <a href="#">Figure 4</a> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge		-	TBD		nC
$I_{RRM}$	Reverse recovery current		-	TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

### 3 Test circuits

Figure 2. Switching times test circuit for resistive load

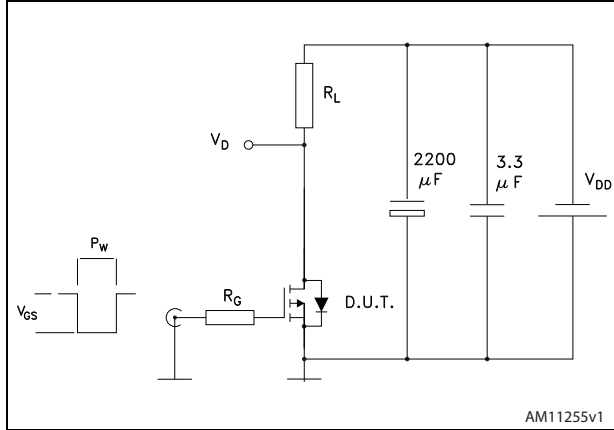


Figure 3. Gate charge test circuit

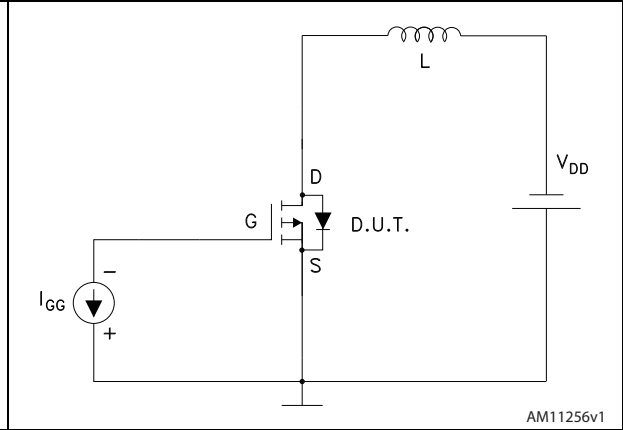
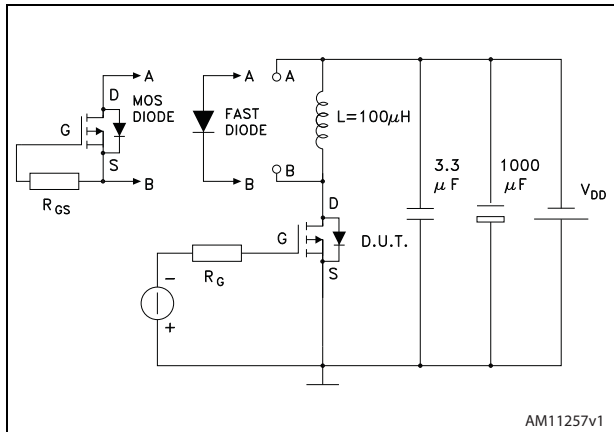


Figure 4. Test circuit for diode recovery behavior



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 5. DPAK (TO-252) type A drawing

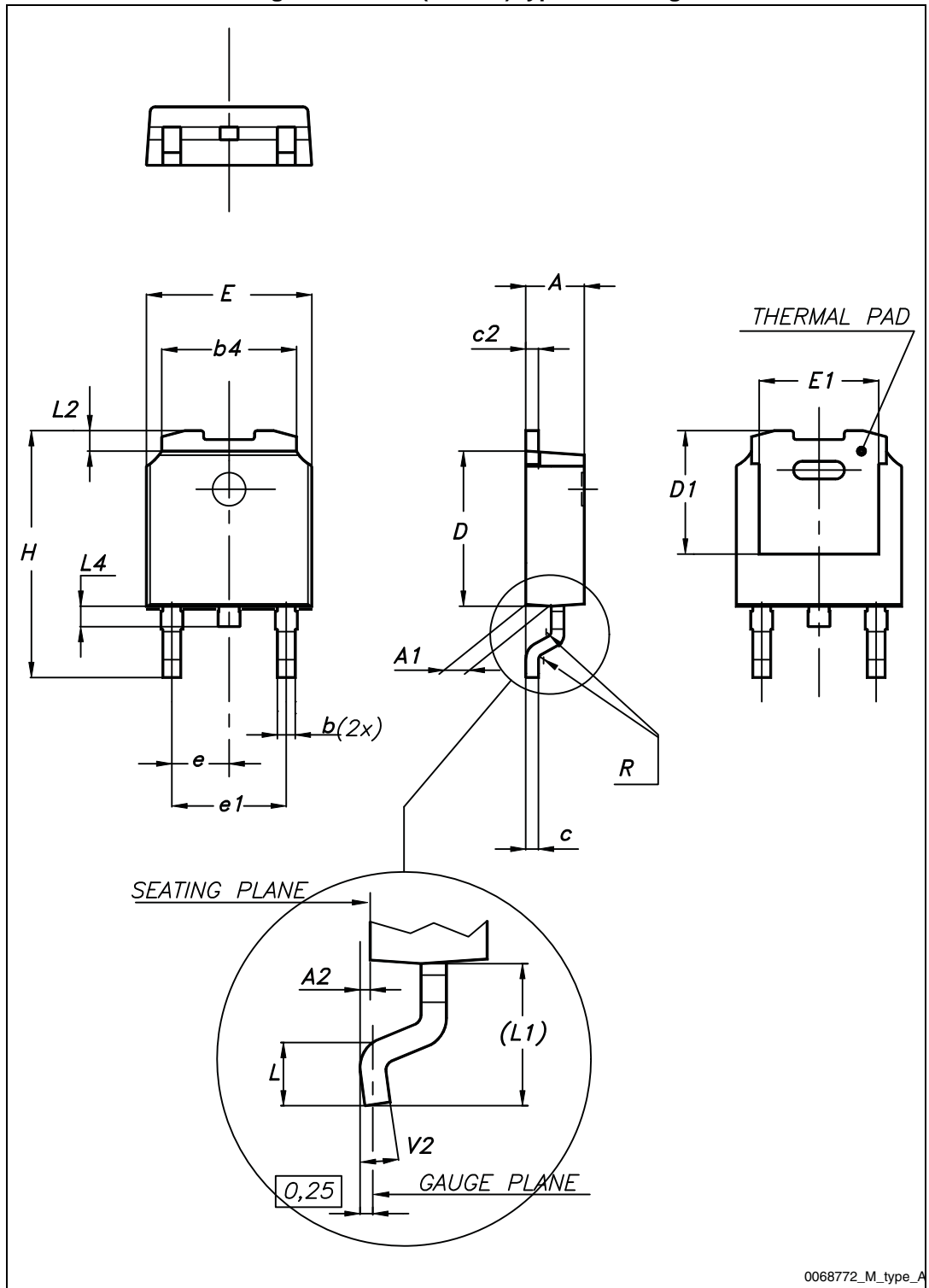
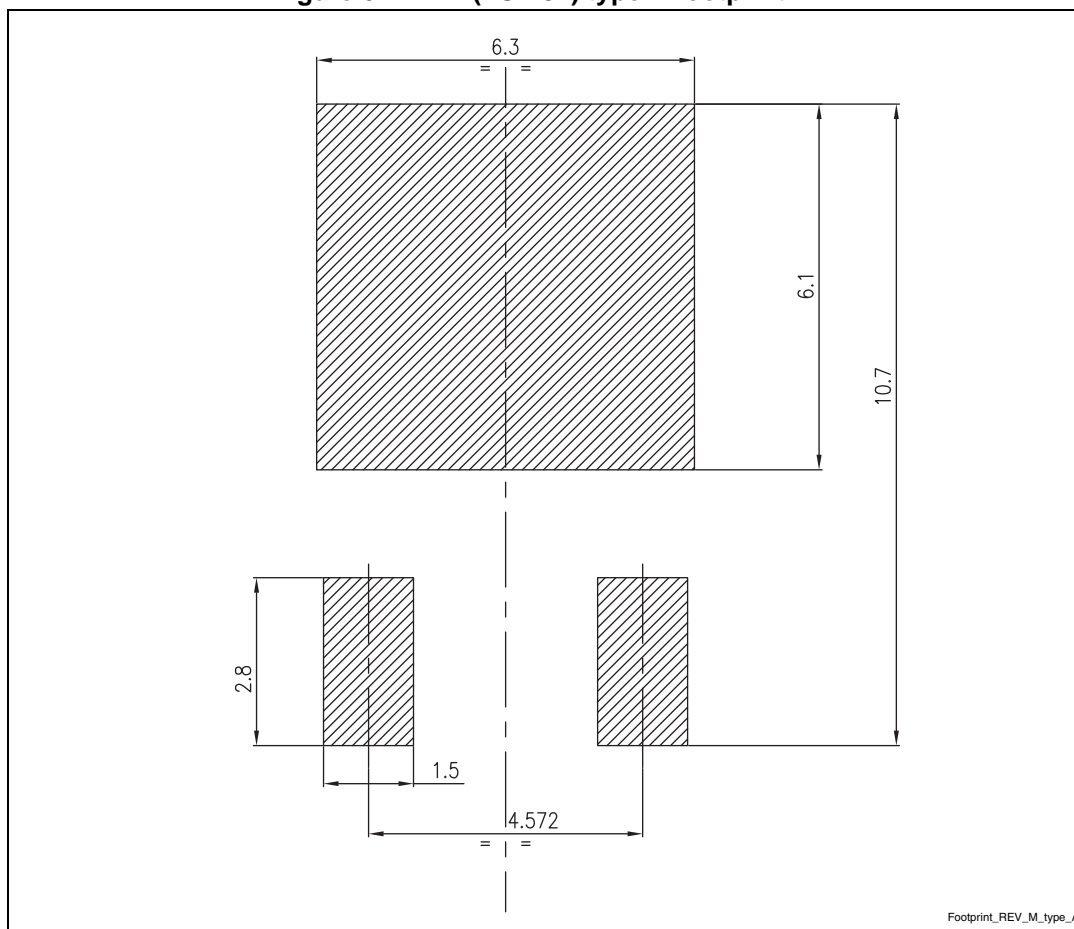


Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 6. DPAK (TO-252) type A footprint (a)



a. All dimensions are in millimeters

# 5 Packaging mechanical data

Figure 7. Tape for DPAK (TO-252)

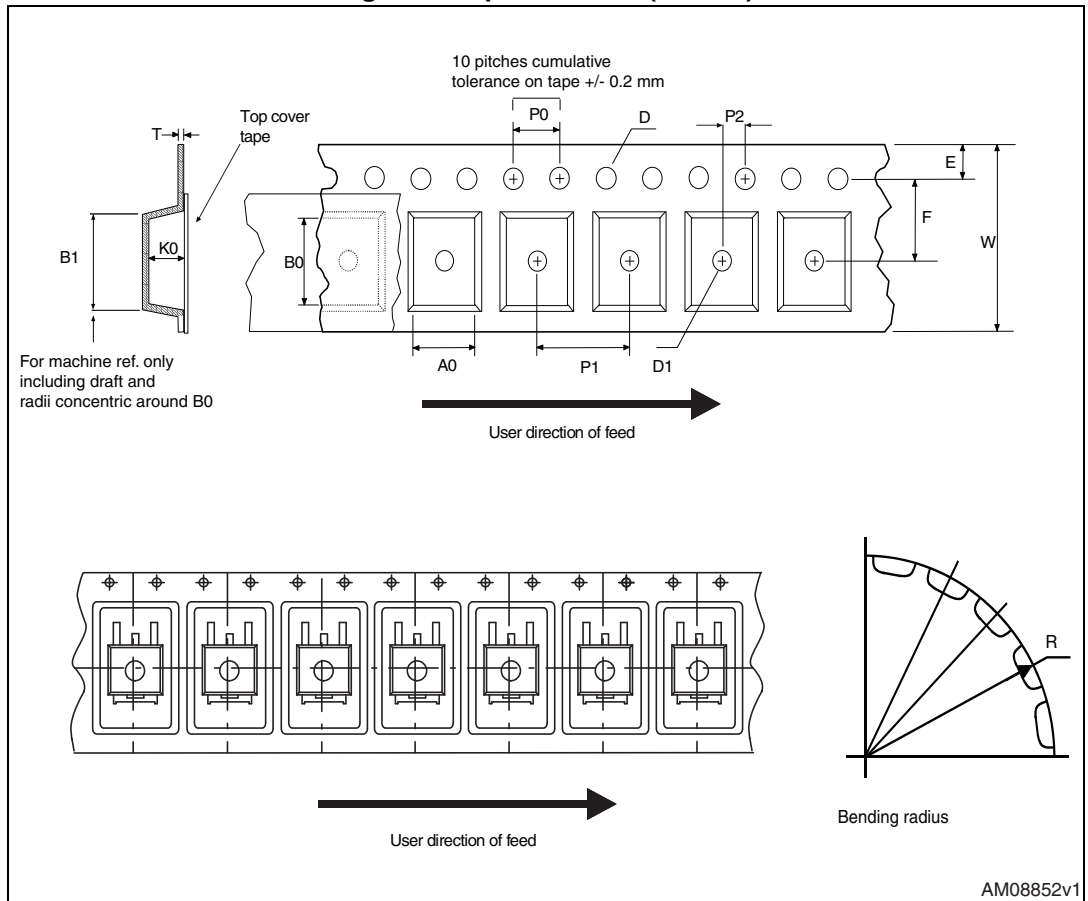


Figure 8. Reel for DPAK (TO-252)

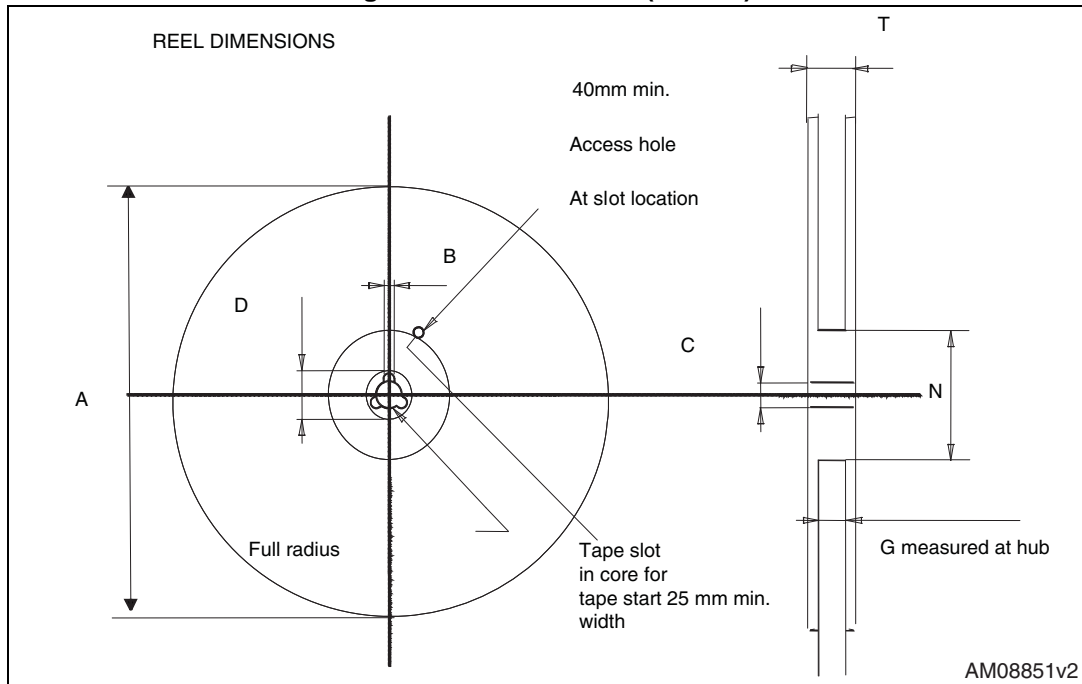


Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
17-Jan-2014	1	First release

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