



# STL120NH02V

N-channel 20 V - 0.0025  $\Omega$  - 120 A - PowerFLAT™ (6x5)  
STripFET™ III Power MOSFET

Preliminary Data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STL120NH02V	20 V	< 0.003 $\Omega$	28 A <sup>(1)</sup>

1. Value limited by wire bonding

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Conduction losses reduced
- 2.5V gate drive
- Switching losses reduced
- Very low threshold device

## Application

- Switching applications

## Description

The STL120NH02V utilizes the latest advanced design rules of ST's proprietary STripFET™ Technology. Thanks to a very low threshold, it is ideal for Synchronous Buck Converter in point of load brick module. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

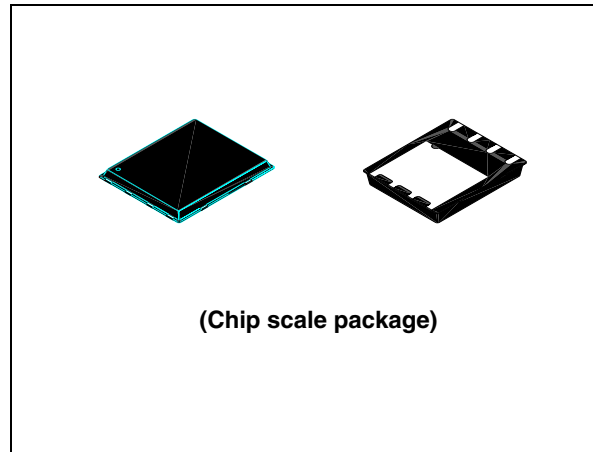


Figure 1. Internal schematic diagram

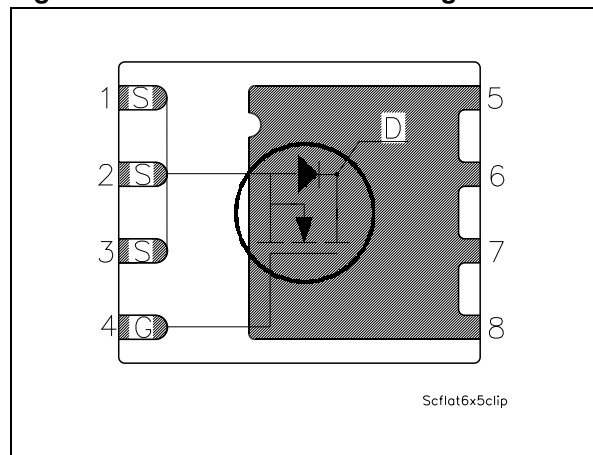


Table 1. Device summary

Order code	Marking	Package	Packaging
STL120NH02V	L120NH02V	PowerFLAT™ (6x5)	Tape & reel

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	20	V
$V_{GS}$	Gate-source voltage	$\pm 8$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	120	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	75	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	28	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	4	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	80	W
	Derating factor <sup>(3)</sup>	0.03	W/ $^\circ\text{C}$
$T_j$ $T_{stg}$	Operating junction temperature storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according to Rthj-case
2. Pulse width limited by safe operating area
3. When mounted on FR-4 board of 1in<sup>2</sup>, 2oz Cu. t < 10 sec

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case (drain) (steady state)	1.56	$^\circ\text{C}/\text{W}$
Rthj-pcb <sup>(1)</sup>	Thermal resistance junction-pcb max	31.2	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1in<sup>2</sup>, 2oz Cu. t < 10 sec

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	10	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	2.8	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	20			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating},$ $T_C = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 8 \text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.60			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5 \text{ V}, I_D = 14 \text{ A}$ $V_{GS} = 2.5 \text{ V}, I_D = 14 \text{ A}$		0.0025 0.003	0.003 0.004	$\Omega$ $\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$		6400		pF
$C_{oss}$	Output capacitance			1203		pF
$C_{rss}$	Reverse transfer capacitance			85		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10 \text{ V}, I_D = 28 \text{ A}$ $R_G = 4.7 \Omega, V_{GS} = 2.3 \text{ V}$ (see <a href="#">Figure 2</a> )		44		ns
$t_r$	Rise time			140		ns
$t_{d(off)}$	Turn-off delay time			62		ns
$t_f$	Fall time			23		ns
$Q_g$	Total gate charge	$V_{DD} = 10 \text{ V}, I_D = 28 \text{ A},$ $V_{GS} = 2.5 \text{ V}$ (see <a href="#">Figure 3</a> )		26.5	44	nC
$Q_{gs}$	Gate-source charge			11.6		nC
$Q_{gd}$	Gate-drain charge			11.8		nC

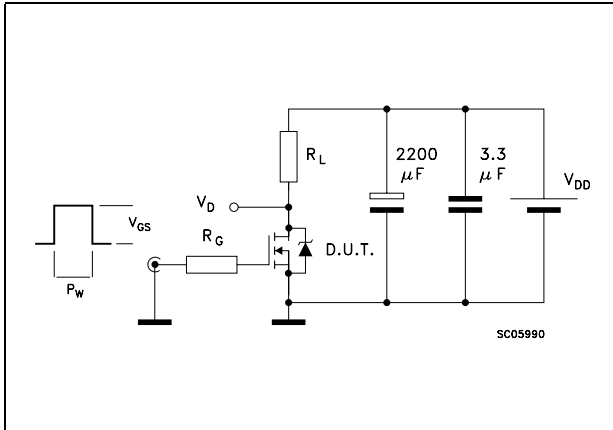
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				28 112	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 28 \text{ A}$ , $V_{GS} = 0$			1.1	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 28 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 13 \text{ V}$ (see <a href="#">Figure 4</a> )		47 61 2.6		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 28 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 13 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 4</a> )		48.3 65 2.7		ns nC A

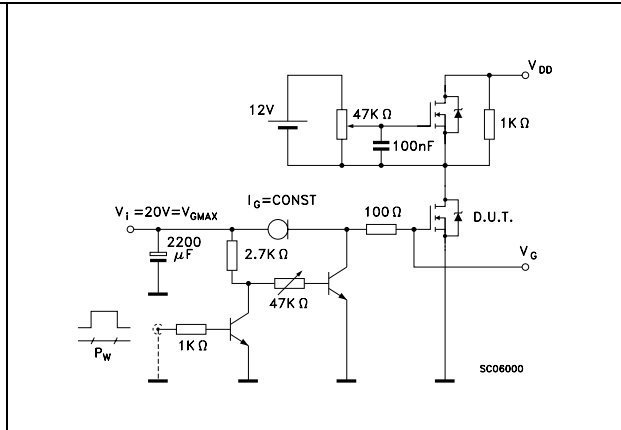
1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuit

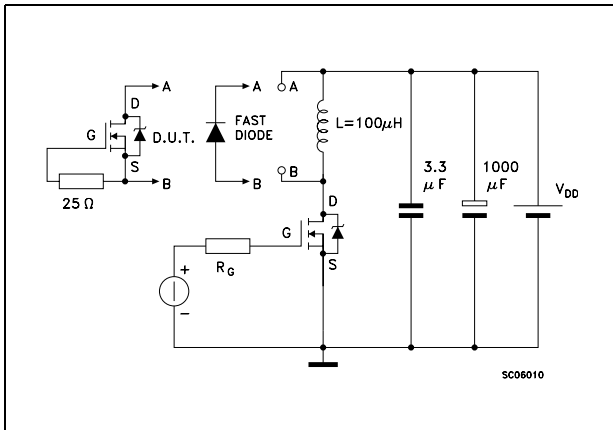
**Figure 2. Switching times test circuit for resistive load**



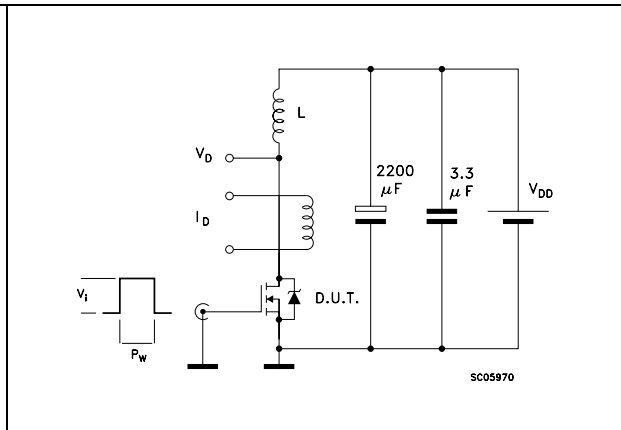
**Figure 3. Gate charge test circuit**



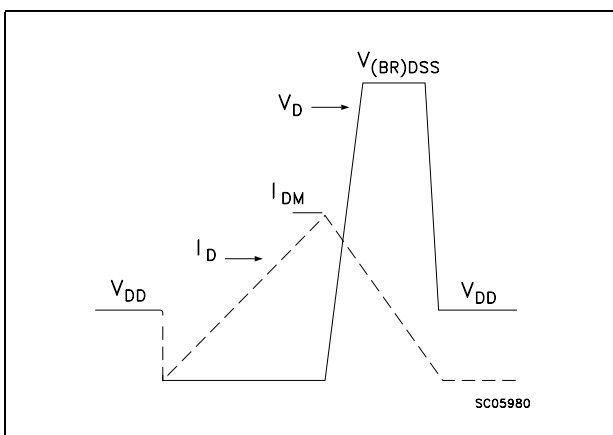
**Figure 4. Test circuit for inductive load switching and diode recovery times**



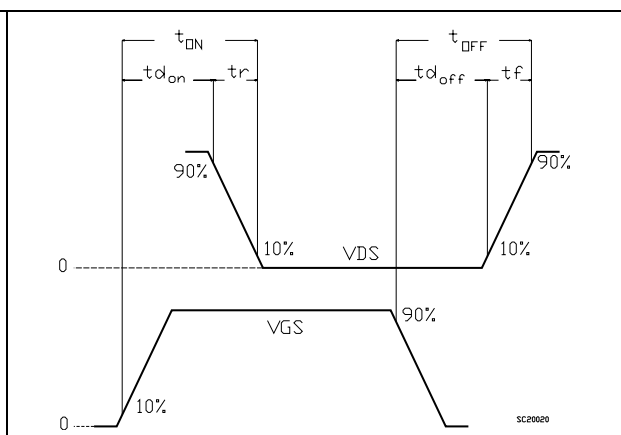
**Figure 5. Unclamped Inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**

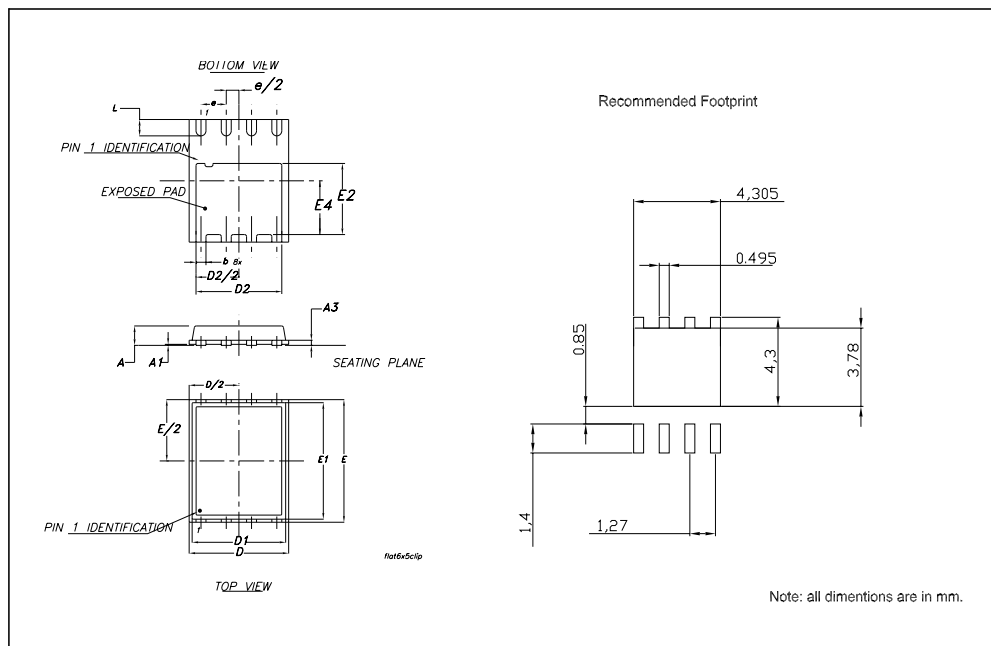


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**PowerFLAT™ (6x5) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



## 5 Revision history

**Table 8. Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
24-Jun-2005	1	New document
04-Sep-2006	2	Document reformatted, no content change
14-Dec-2007	3	Document status promoted from target specification to preliminary data.

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