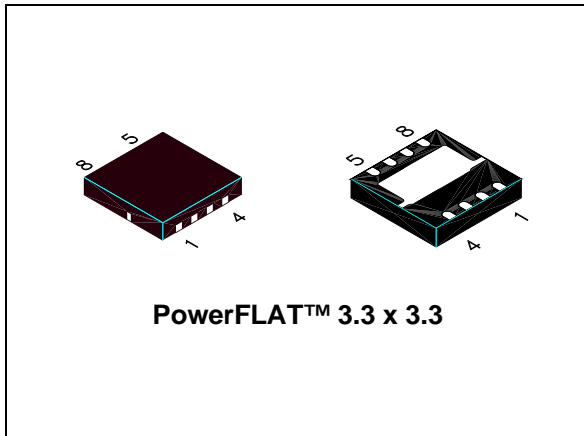


N-channel 100 V, 0.0017 Ω typ., 8 A, STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 3.3 x 3.3 package

Datasheet - preliminary data



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STL8N10F7	100 V	0.020 Ω	8 A	3.5 W

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device utilizes the 7th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Figure 1. Internal schematic diagram

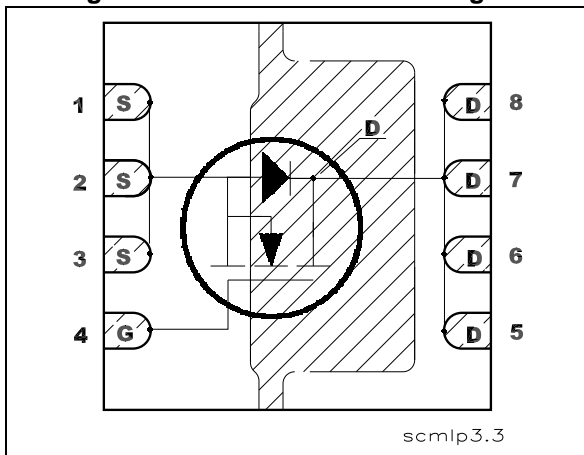


Table 1. Device summary

Order code	Marking	Package	Packaging
STL8N10F7	8N10F7	PowerFLAT™ 3.3 x 3.3	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous)	8	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	32	A
$P_{TOT}^{(2)}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(1)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	3.5	W
T_J	Operating junction temperature	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

1. This value is rated according to $R_{thj-pcb}$.
2. This value is rated according to R_{thj-c} .
3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case	2.5	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ sec}$

2 Electrical characteristics

($T_{CASE}=25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS}=0$)	$I_D = 250\ \mu\text{A}$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS}=0$)	$V_{DS} = 100\text{ V}$ $V_{DS} = 100\text{ V}; T_C=125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS}=0$)	$V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D = 250\ \mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS}= 10\text{ V}, I_D= 4\text{ A}$		0.0017	0.0020	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}, f=1\text{ MHz},$ $V_{GS}=0$	-	2000	-	pF
C_{oss}	Output capacitance		-	350	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
Q_g	Total gate charge	$V_{DD}=50\text{ V}, I_D = 8\text{ A}$ $V_{GS}=10\text{ V}$ <i>Figure 3</i>	-	22	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=50\text{ V}, I_D= 4\text{ A},$ $R_G=4.7\ \Omega, V_{GS}= 10\text{ V}$ <i>Figure 2</i>	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-	-	8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8 \text{ A}$, $V_{GS} = 0$	-	-	1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 8 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 80 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	-		ns
Q_{rr}	Reverse recovery charge		-	-		nC
I_{RRM}	Reverse recovery current		-	-		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

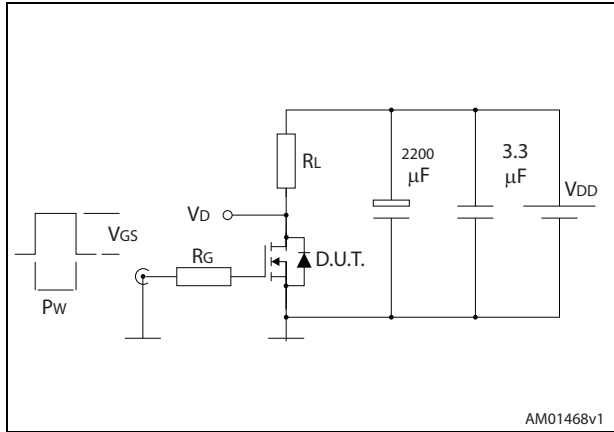


Figure 3. Gate charge test circuit

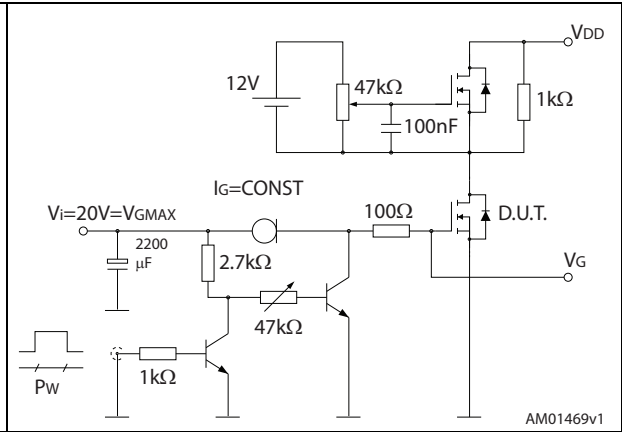


Figure 4. Test circuit for inductive load switching and diode recovery times

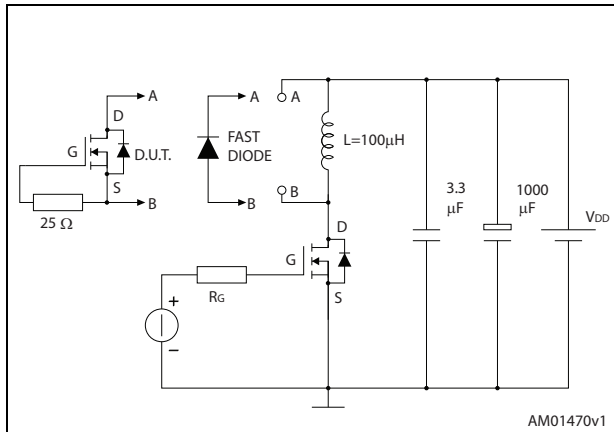


Figure 5. Unclamped inductive load test circuit

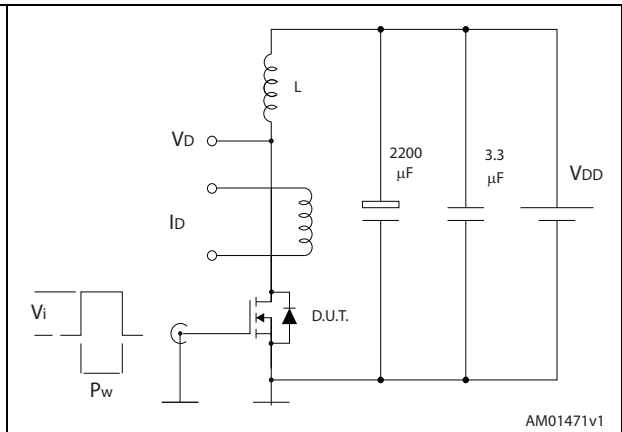


Figure 6. Unclamped inductive waveform

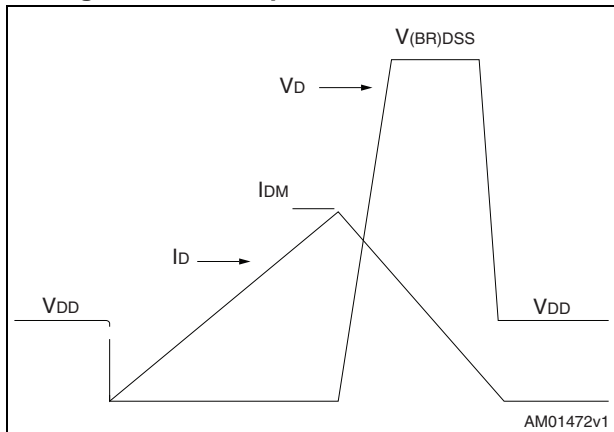
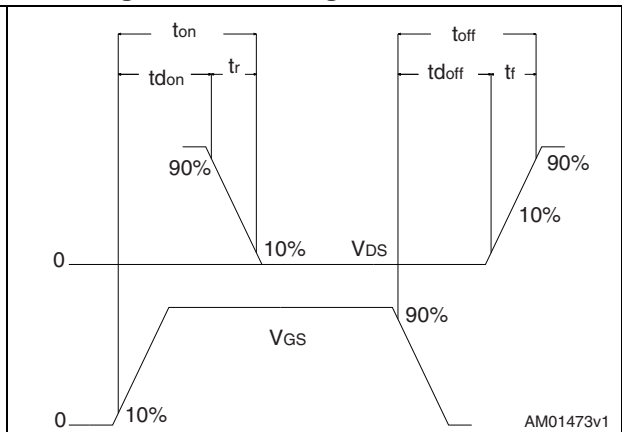


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. PowerFLAT™ 3.3 x 3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
A3		0.20	
b	0.23		0.38
D	3.20	3.30	3.40
D2	2.50		2.75
E	3.20	3.30	3.40
E2	1.25		1.50
e		0.65	
L	0.30		0.50

Figure 8. PowerFLAT™ 3.3 x 3.3 drawing

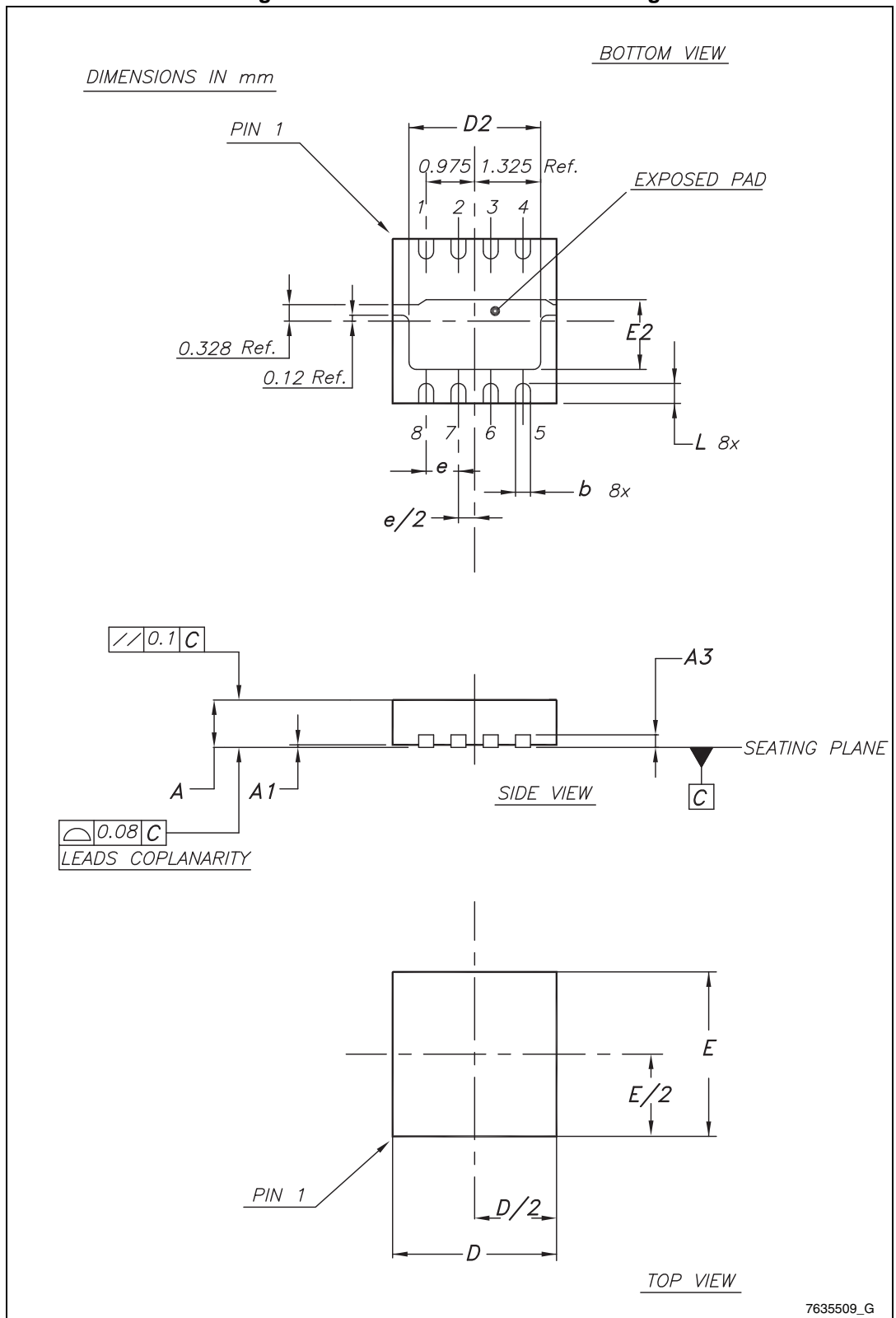
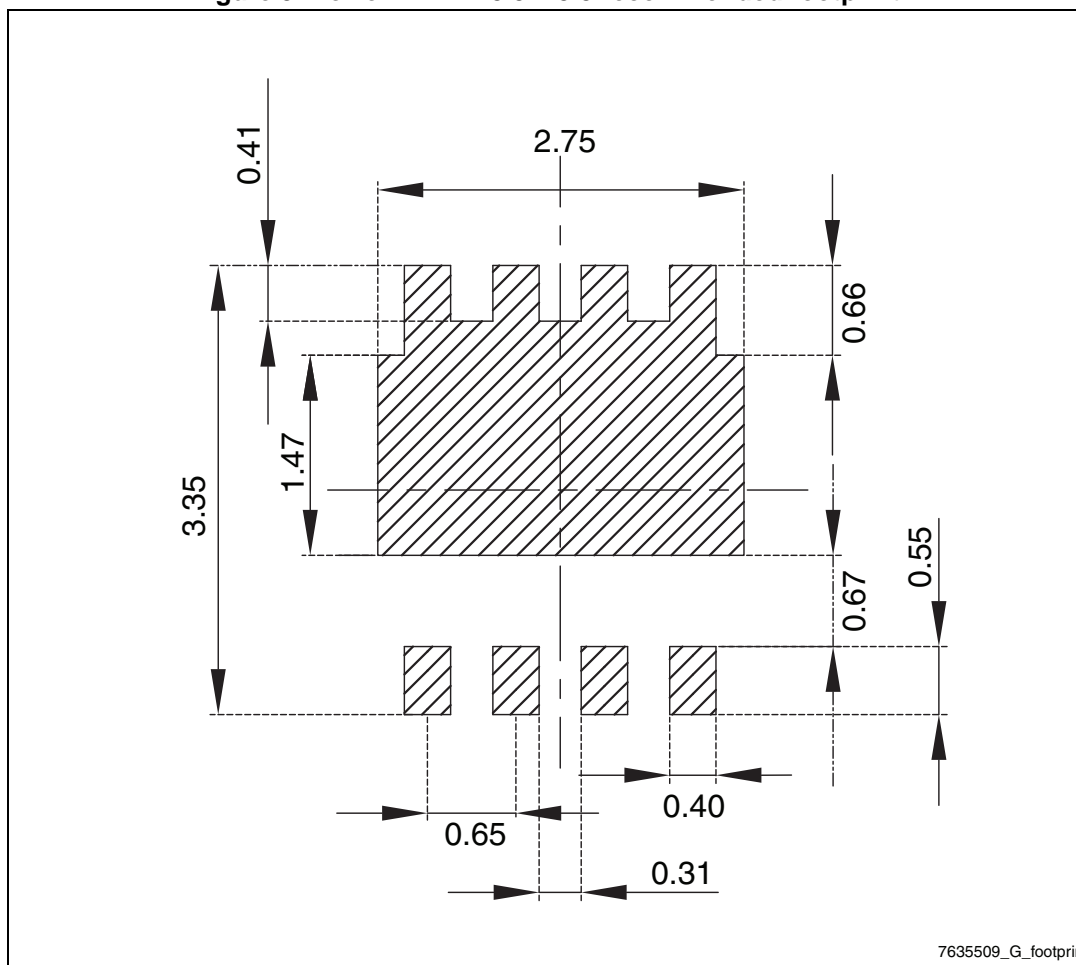


Figure 9. PowerFLAT™ 3.3 x 3.3 recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
31-Jul-2013	1	First release.

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