

P-channel 30 V, 0.015 Ω typ., 9 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 3.3 x 3.3 package

Datasheet – preliminary data

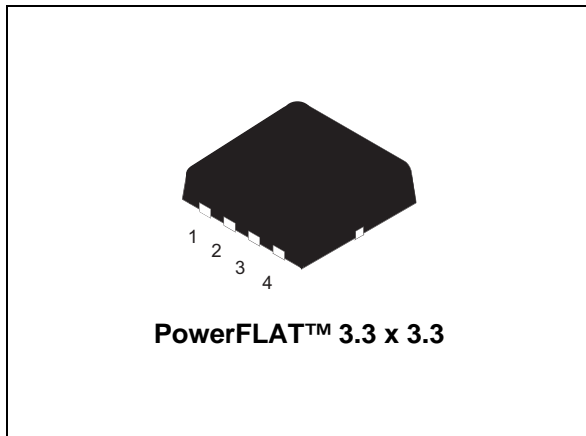
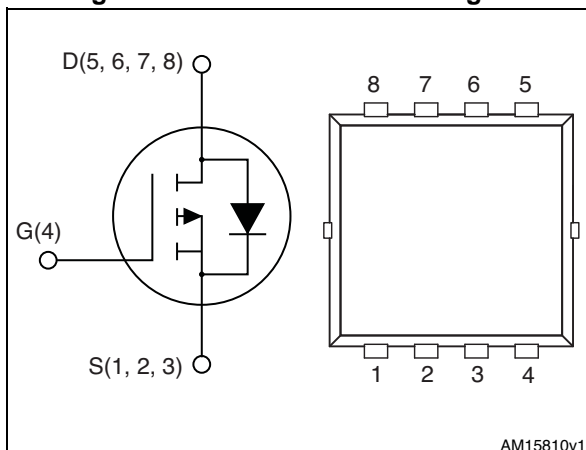


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STL9P3LLH6	30 V	0.018 Ω	9A

- $R_{DS(on)} * Q_g$ industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL9P3LLH6	9P3L	PowerFLAT™ 3.3 x 3.3	Tape and reel

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5.9	A
$I_{DM}^{(1), (2)}$	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at $T_C = T_j\text{-pcb}$	2.9	W
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Value related to $R_{thj\text{-pcb}}$.
2. Pulse width limited by safe operating area.

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}^{(2)}$	Thermal resistance junction-case	2.5	$^\circ\text{C/W}$
$R_{thj\text{-pcb}}^{(1)}$	Thermal resistance junction-pcb	42.8	$^\circ\text{C/W}$
$R_{thj\text{-pcb}}^{(2)}$	Thermal resistance junction-pcb	63.5	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10$ sec.
2. Steady state.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu A$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 30\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, T_C = 125\text{ °C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$		0.015	0.018	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 4.5\text{ A}$		0.02	0.025	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	2550	-	pF
C_{oss}	Output capacitance		-	380	-	pF
C_{riss}	Reverse transfer capacitance		-	220	-	pF
Q_g	Total gate charge	$V_{DD} = 24\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 4.5\text{ V}$ (see Figure 2)	-	12	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 24\text{ V}, I_D = 4.5\text{ A},$ $R_G = 4.7\ \Omega, V_{GS} = 10\text{ V}$	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 9\text{ A}, V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 16\text{ V}, T_j = 150\text{ }^\circ\text{C}$	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		nC
I_{RRM}	Reverse recovery current		-	TBD		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

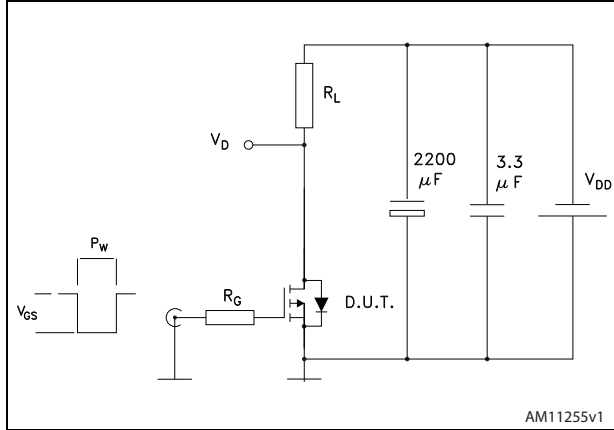


Figure 3. Gate charge test circuit

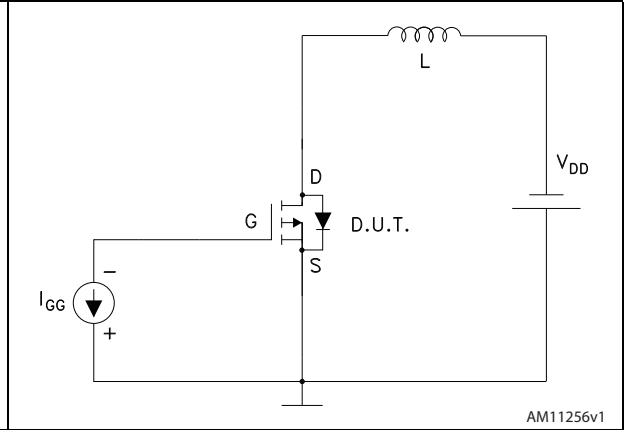
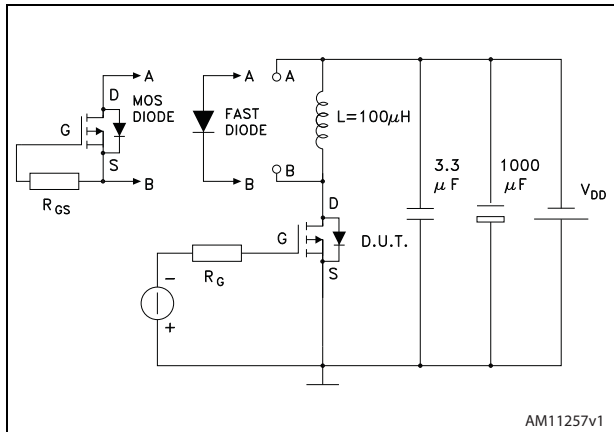


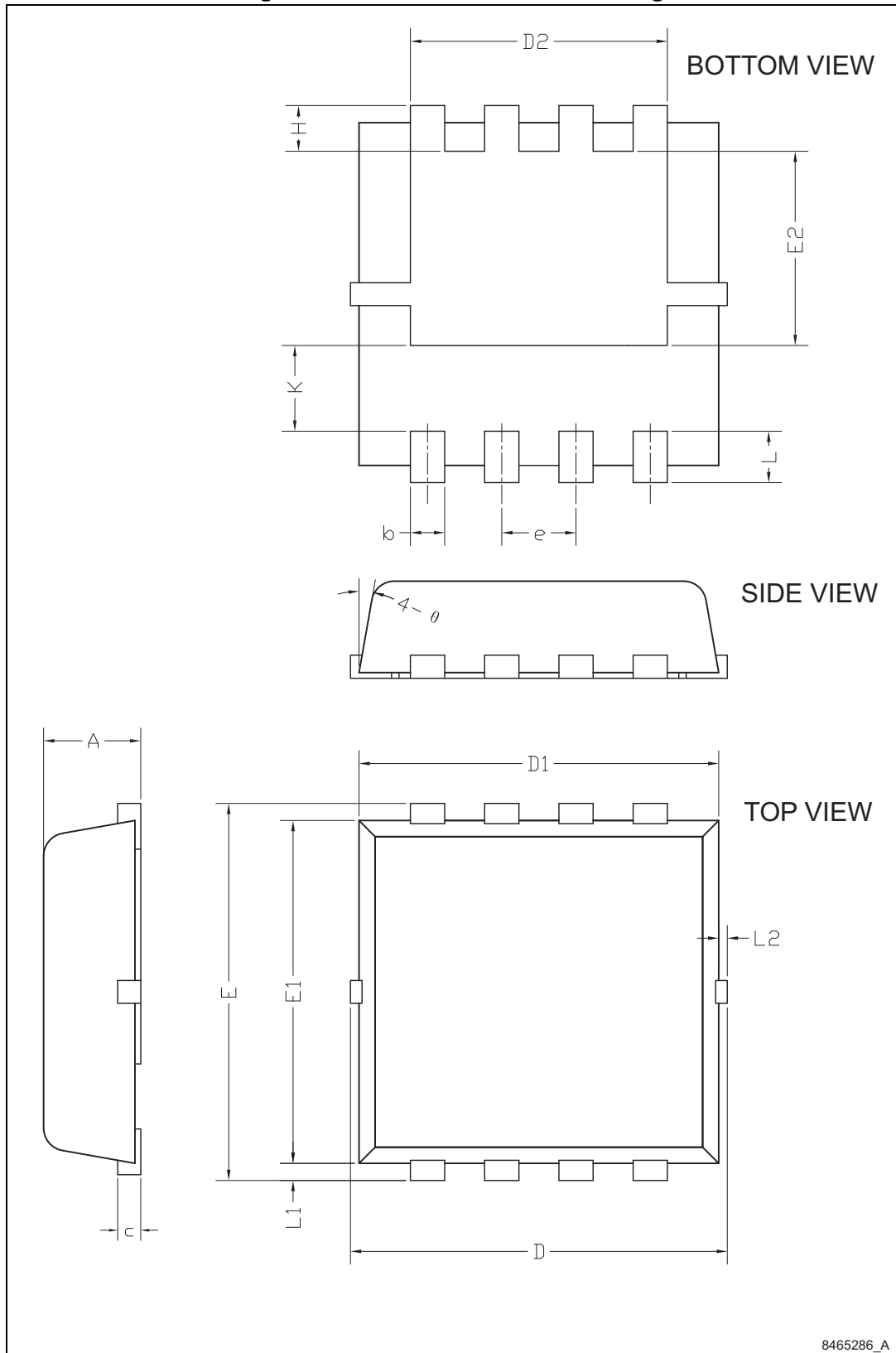
Figure 4. Test circuit for diode recovery behavior



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 5. PowerFLAT™ 3.3 x 3.3 drawing

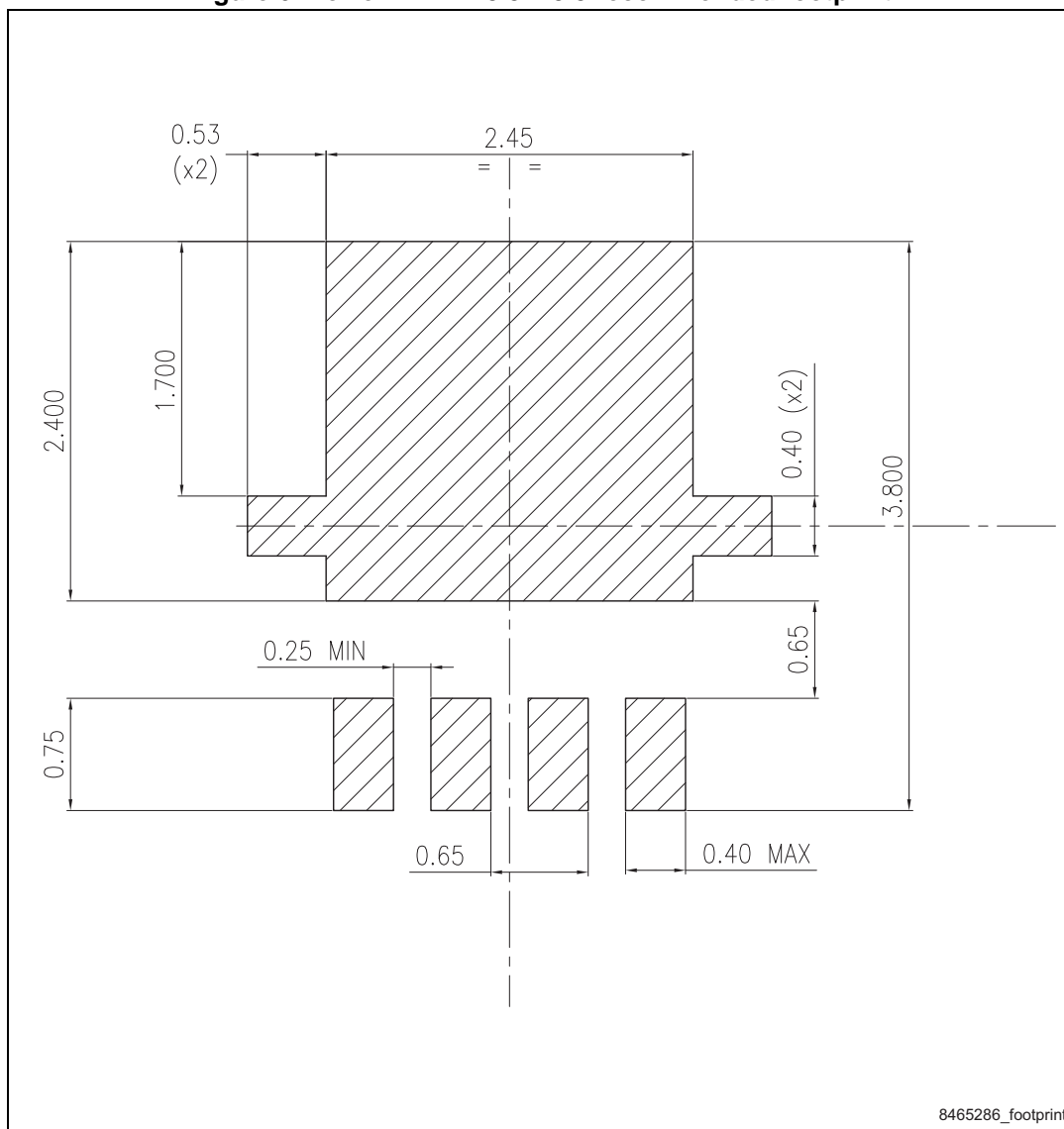


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Table 8. PowerFLAT™ 3.3 x 3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
∅	8°	10°	12°

Figure 6. PowerFLAT™ 3.3 x 3.3 recommended footprint



8465286_footprint

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
23-Jan-2014	1	First release.

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