

3W filter-free class D audio power amplifier

Features

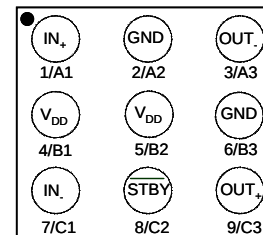
- Operating from $V_{CC} = 2.4V$ to $5.5V$
- Standby mode active low
- Output power: 3W into 4Ω and 1.75W into 8Ω with 10% THD+N max and 5V power supply.
- Output power: 2.3W @5V or 0.75W @ 3.0V into 4Ω with 1% THD+N max.
- Output power: 1.4W @5V or 0.45W @ 3.0V into 8Ω with 1% THD+N max.
- Adjustable gain via external resistors
- Low current consumption 2mA @ 3V
- Efficiency: 88% typ.
- Signal to noise ratio: 85dB typ.
- PSRR: 63dB typ. @217Hz with 6dB gain
- PWM base frequency: 250kHz
- Low pop & click noise
- Thermal shutdown protection
- Available in flip-chip 9 x 300 μ m (Pb-free)

Description

The TS4962M is a differential Class-D BTL power amplifier. It is able to drive up to 2.3W into a 4Ω load and 1.4W into a 8Ω load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical Class-AB audio amps.

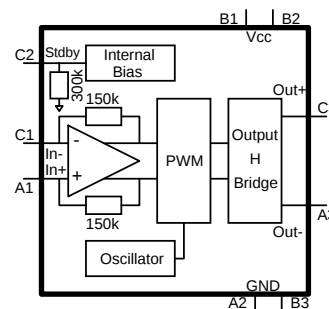
The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

Pin connections



IN+: positive differential input
 IN-: negative differential input
 VDD: analog power supply
 GND: power supply ground
 STBY: standby pin (active low)
 OUT+: positive differential output
 OUT-: negative differential output

Block diagram



Applications

- Cellular phone
- PDA
- Notebook PC

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1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ^{(1), (2)}	6	V
V_{in}	Input voltage ⁽³⁾	GND to V_{CC}	V
T_{oper}	Operating free-air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient ⁽⁴⁾	200	°C/W
P_{diss}	Power dissipation	Internally Limited ⁽⁵⁾	
ESD	Human body model	2	kV
ESD	Machine model	200	V
Latch-up	Latch-up immunity	200	mA
V_{STBY}	Standby pin voltage maximum voltage ⁽⁶⁾	GND to V_{CC}	V
	Lead temperature (soldering, 10sec)	260	°C

1. Caution: This device is not protected in the event of abnormal operating conditions, such as for example, short-circuiting between any one output pin and ground, between any one output pin and V_{CC} , and between individual output pins.
2. All voltage values are measured with respect to the ground pin.
3. The magnitude of the input signal must never exceed $V_{CC} + 0.3V$ / GND - 0.3V.
4. The device is protected in case of over temperature by a thermal shutdown active @ 150°C.
5. Exceeding the power derating curves during a long period causes abnormal operation.
6. The magnitude of the standby signal must never exceed $V_{CC} + 0.3V$ / GND - 0.3V.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	2.4 to 5.5	V
V_{IC}	Common mode input voltage range ⁽²⁾	0.5 to $V_{CC} - 0.8$	V
V_{STBY}	Standby voltage input: ⁽³⁾ Device ON Device OFF	$1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ ⁽⁴⁾	V
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient ⁽⁵⁾	90	°C/W

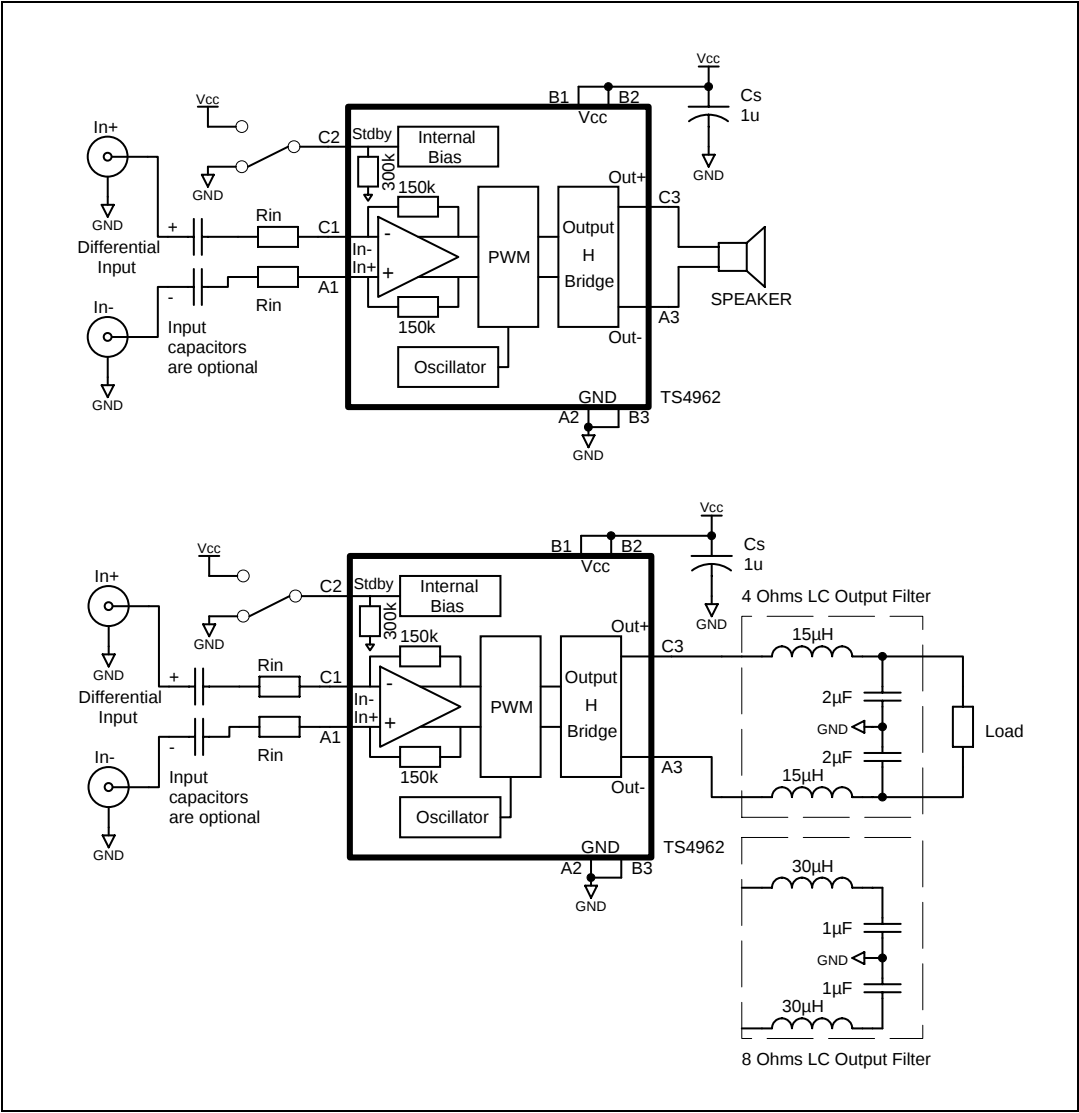
1. For V_{CC} from 2.4V to 2.5V, the operating temperature range is reduced to $0^\circ\text{C} \leq T_{amb} \leq 70^\circ\text{C}$.
2. For V_{CC} from 2.4V to 2.5V, the common mode input range must be set at $V_{CC}/2$.
3. Without any signal on V_{STBY} , the device will be in standby.
4. Minimum current consumption is obtained when $V_{STBY} = GND$.
5. With heat sink surface = 125mm².

2 Application component information

Table 3. Component information

Component	Functional description
C_s	Bypass supply capacitor. Install as close as possible to the TS4962M to minimize high-frequency ripple. A 100nF ceramic capacitor should be added to enhance the power supply filtering at high frequency.
R_{in}	Input resistor to program the TS4962M differential gain (gain = $300k\Omega/R_{in}$ with R_{in} in $k\Omega$).
Input capacitor	Due to common mode feedback, these input capacitors are optional. However, they can be added to form with R_{in} a 1st order high pass filter with -3dB cut-off frequency = $1/(2*\pi*R_{in}*C_{in})$.

Figure 1. Typical application schematics



3 Electrical characteristics

Table 4. $V_{CC} = +5V$, $GND = 0V$, $V_{IC} = 2.5V$, $t_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		2.3	3.3	mA
I_{STBY}	Standby current ⁽¹⁾	No input signal, $V_{STBY} = GND$		10	1000	nA
V_{OO}	Output offset voltage	No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max, F = 1kHz, $R_L = 4\Omega$ THD = 10% max, F = 1kHz, $R_L = 4\Omega$ THD = 1% max, F = 1kHz, $R_L = 8\Omega$ THD = 10% max, F = 1kHz, $R_L = 8\Omega$		2.3 3 1.4 1.75		W
THD + N	Total harmonic distortion + noise	$P_{out} = 900mW_{RMS}$, G = 6dB, 20Hz < F < 20kHz $R_L = 8\Omega + 15\mu H$, BW < 30kHz $P_{out} = 1W_{RMS}$, G = 6dB, F = 1kHz, $R_L = 8\Omega + 15\mu H$, BW < 30kHz		1 0.4		%
Efficiency	Efficiency	$P_{out} = 2W_{RMS}$, $R_L = 4\Omega + \geq 15\mu H$ $P_{out} = 1.2W_{RMS}$, $R_L = 8\Omega + \geq 15\mu H$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽²⁾	F = 217Hz, $R_L = 8\Omega$, G=6dB, $V_{ripple} = 200mV_{pp}$		63		dB
CMRR	Common mode rejection ratio	F = 217Hz, $R_L = 8\Omega$, G = 6dB, $\Delta V_{icm} = 200mV_{pp}$		57		dB
Gain	Gain value	R_{in} in k Ω	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	k Ω
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, $P_{out} = 1.2W$, $R_L = 8\Omega$		85		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 4. $V_{CC} = +5V$, $GND = 0V$, $V_{IC} = 2.5V$, $t_{amb} = 25^{\circ}C$ (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise	$F = 20Hz$ to $20kHz$, $G = 6dB$ Unweighted $R_L = 4\Omega$ A-weighted $R_L = 4\Omega$		85 60		μV_{RMS}
		Unweighted $R_L = 8\Omega$ A-weighted $R_L = 8\Omega$		86 62		
		Unweighted $R_L = 4\Omega + 15\mu H$ A-weighted $R_L = 4\Omega + 15\mu H$		83 60		
		Unweighted $R_L = 4\Omega + 30\mu H$ A-weighted $R_L = 4\Omega + 30\mu H$		88 64		
		Unweighted $R_L = 8\Omega + 30\mu H$ A-weighted $R_L = 8\Omega + 30\mu H$		78 57		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		87 65		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		82 59		

- Standby mode is active when V_{STBY} is tied to GND.
- Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ $F = 217Hz$.

Table 5. $V_{CC} = +4.2V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		2.1	3	mA
I_{STBY}	Standby current ⁽²⁾	No input signal, $V_{STBY} = GND$		10	1000	nA
V_{OO}	Output offset voltage	No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max, F = 1kHz, $R_L = 4\Omega$ THD = 10% max, F = 1kHz, $R_L = 4\Omega$ THD = 1% max, F = 1kHz, $R_L = 8\Omega$ THD = 10% max, F = 1kHz, $R_L = 8\Omega$		1.6 2 0.95 1.2		W
THD + N	Total harmonic distortion + noise	$P_{out} = 600mW_{RMS}$, G = 6dB, 20Hz < F < 20kHz $R_L = 8\Omega + 15\mu H$, BW < 30kHz $P_{out} = 700mW_{RMS}$, G = 6dB, F = 1kHz, $R_L = 8\Omega + 15\mu H$, BW < 30kHz		1 0.35		%
Efficiency	Efficiency	$P_{out} = 1.45W_{RMS}$, $R_L = 4\Omega + \geq 15\mu H$ $P_{out} = 0.9W_{RMS}$, $R_L = 8\Omega + \geq 15\mu H$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽³⁾	F = 217Hz, $R_L = 8\Omega$, G=6dB, $V_{ripple} = 200mV_{pp}$		63		dB
CMRR	Common mode rejection ratio	F = 217Hz, $R_L = 8\Omega$, G = 6dB, $\Delta V_{icm} = 200mV_{pp}$		57		dB
Gain	Gain value	R_{in} in k Ω	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	k Ω
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, $P_{out} = 0.9W$, $R_L = 8\Omega$		85		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 5. $V_{CC} = +4.2V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise	F = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A-weighted $R_L = 4\Omega$		85 60		μV_{RMS}
		Unweighted $R_L = 8\Omega$ A-weighted $R_L = 8\Omega$		86 62		
		Unweighted $R_L = 4\Omega + 15\mu H$ A-weighted $R_L = 4\Omega + 15\mu H$		83 60		
		Unweighted $R_L = 4\Omega + 30\mu H$ A-weighted $R_L = 4\Omega + 30\mu H$		88 64		
		Unweighted $R_L = 8\Omega + 30\mu H$ A-weighted $R_L = 8\Omega + 30\mu H$		78 57		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		87 65		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		82 59		

1. All electrical values are guaranteed with correlation measurements at 2.5V and 5V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ $F = 217Hz$.

Table 6. $V_{CC} = +3.6V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		2	2.8	mA
I_{STBY}	Standby current ⁽²⁾	No input signal, $V_{STBY} = GND$		10	1000	nA
V_{OO}	Output offset voltage	No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max, F = 1kHz, $R_L = 4\Omega$ THD = 10% max, F = 1kHz, $R_L = 4\Omega$ THD = 1% max, F = 1kHz, $R_L = 8\Omega$ THD = 10% max, F = 1kHz, $R_L = 8\Omega$		1.15 1.51 0.7 0.9		W
THD + N	Total harmonic distortion + noise	$P_{out} = 500mW_{RMS}$, G = 6dB, 20Hz < F < 20kHz $R_L = 8\Omega + 15\mu H$, BW < 30kHz $P_{out} = 500mW_{RMS}$, G = 6dB, F = 1kHz, $R_L = 8\Omega + 15\mu H$, BW < 30kHz		1 0.27		%
Efficiency	Efficiency	$P_{out} = 1W_{RMS}$, $R_L = 4\Omega + \geq 15\mu H$ $P_{out} = 0.65W_{RMS}$, $R_L = 8\Omega + \geq 15\mu H$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽³⁾	F = 217Hz, $R_L = 8\Omega$, G=6dB, $V_{ripple} = 200mV_{pp}$		62		dB
CMRR	Common mode rejection ratio	F = 217Hz, $R_L = 8\Omega$, G = 6dB, $\Delta V_{icm} = 200mV_{pp}$		56		dB
Gain	Gain value	R_{in} in k Ω	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	k Ω
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, $P_{out} = 0.6W$, $R_L = 8\Omega$		83		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 6. $V_{CC} = +3.6V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise	F = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A-weighted $R_L = 4\Omega$		83 57		μV_{RMS}
		Unweighted $R_L = 8\Omega$ A-weighted $R_L = 8\Omega$		83 61		
		Unweighted $R_L = 4\Omega + 15\mu H$ A-weighted $R_L = 4\Omega + 15\mu H$		81 58		
		Unweighted $R_L = 4\Omega + 30\mu H$ A-weighted $R_L = 4\Omega + 30\mu H$		87 62		
		Unweighted $R_L = 8\Omega + 30\mu H$ A-weighted $R_L = 8\Omega + 30\mu H$		77 56		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		85 63		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		80 57		

1. All electrical values are guaranteed with correlation measurements at 2.5V and 5V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ $F = 217Hz$.

Table 7. $V_{CC} = +3V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.9	2.7	mA
I_{STBY}	Standby current ⁽²⁾	No input signal, $V_{STBY} = GND$		10	1000	nA
V_{OO}	Output offset voltage	No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max, F = 1kHz, $R_L = 4\Omega$ THD = 10% max, F = 1kHz, $R_L = 4\Omega$ THD = 1% max, F = 1kHz, $R_L = 8\Omega$ THD = 10% max, F = 1kHz, $R_L = 8\Omega$		0.75 1 0.5 0.6		W
THD + N	Total harmonic distortion + noise	$P_{out} = 350mW_{RMS}$, G = 6dB, 20Hz < F < 20kHz $R_L = 8\Omega + 15\mu H$, BW < 30kHz $P_{out} = 350mW_{RMS}$, G = 6dB, F = 1kHz, $R_L = 8\Omega + 15\mu H$, BW < 30kHz		1 0.21		%
Efficiency	Efficiency	$P_{out} = 0.7W_{RMS}$, $R_L = 4\Omega + \geq 15\mu H$ $P_{out} = 0.45W_{RMS}$, $R_L = 8\Omega + \geq 15\mu H$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽³⁾	F = 217Hz, $R_L = 8\Omega$, G=6dB, $V_{ripple} = 200mV_{pp}$		60		dB
CMRR	Common mode rejection ratio	F = 217Hz, $R_L = 8\Omega$, G = 6dB, $\Delta V_{icm} = 200mV_{pp}$		54		dB
Gain	Gain value	R_{in} in k Ω	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	k Ω
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, $P_{out} = 0.4W$, $R_L = 8\Omega$		82		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 7. $V_{CC} = +3V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output Voltage Noise	$f = 20Hz$ to $20kHz$, $G = 6dB$ Unweighted $R_L = 4\Omega$ A-weighted $R_L = 4\Omega$		83 57		μV_{RMS}
		Unweighted $R_L = 8\Omega$ A-weighted $R_L = 8\Omega$		83 61		
		Unweighted $R_L = 4\Omega + 15\mu H$ A-weighted $R_L = 4\Omega + 15\mu H$		81 58		
		Unweighted $R_L = 4\Omega + 30\mu H$ A-weighted $R_L = 4\Omega + 30\mu H$		87 62		
		Unweighted $R_L = 8\Omega + 30\mu H$ A-weighted $R_L = 8\Omega + 30\mu H$		77 56		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		85 63		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		80 57		

1. All electrical values are guaranteed with correlation measurements at 2.5V and 5V.
2. Standby mode is active when V_{STBY} is tied to GND.
3. Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ $F = 217Hz$.

Table 8. $V_{CC} = +2.5V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.7	2.4	mA
I_{STBY}	Standby current ⁽¹⁾	No input signal, $V_{STBY} = GND$		10	1000	nA
V_{OO}	Output offset voltage	No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power	G=6dB THD = 1% max, F = 1kHz, $R_L = 4\Omega$ THD = 10% max, F = 1kHz, $R_L = 4\Omega$ THD = 1% max, F = 1kHz, $R_L = 8\Omega$ THD = 10% max, F = 1kHz, $R_L = 8\Omega$		0.52 0.71 0.33 0.42		W
THD + N	Total harmonic distortion + noise	$P_{out} = 200mW_{RMS}$, G = 6dB, 20Hz < F < 20kHz $R_L = 8\Omega + 15\mu H$, BW < 30kHz $P_{out} = 200mW_{RMS}$, G = 6dB, F = 1kHz, $R_L = 8\Omega + 15\mu H$, BW < 30kHz		1 0.19		%
Efficiency	Efficiency	$P_{out} = 0.47W_{RMS}$, $R_L = 4\Omega + \geq 15\mu H$ $P_{out} = 0.3W_{RMS}$, $R_L = 8\Omega + \geq 15\mu H$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽²⁾	F = 217Hz, $R_L = 8\Omega$, G=6dB, $V_{ripple} = 200mV_{pp}$		60		dB
CMRR	Common mode rejection ratio	F = 217Hz, $R_L = 8\Omega$, G = 6dB, $\Delta V_{icm} = 200mV_{pp}$		54		dB
Gain	Gain value	R_{in} in k Ω	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	k Ω
F_{PWM}	Pulse width modulator base frequency		180	250	320	kHz
SNR	Signal to noise ratio	A-weighting, $P_{out} = 1.2W$, $R_L = 8\Omega$		80		dB
t_{WU}	Wake-up time			5	10	ms
t_{STBY}	Standby time			5	10	ms

Table 8. $V_{CC} = +2.5V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_N	Output Voltage Noise	F = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A-weighted $R_L = 4\Omega$		85 60		μV_{RMS}
		Unweighted $R_L = 8\Omega$ A-weighted $R_L = 8\Omega$		86 62		
		Unweighted $R_L = 4\Omega + 15\mu H$ A-weighted $R_L = 4\Omega + 15\mu H$		76 56		
		Unweighted $R_L = 4\Omega + 30\mu H$ A-weighted $R_L = 4\Omega + 30\mu H$		82 60		
		Unweighted $R_L = 8\Omega + 30\mu H$ A-weighted $R_L = 8\Omega + 30\mu H$		67 53		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		78 57		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		74 54		

- Standby mode is active when V_{STBY} is tied to GND.
- Dynamic measurements - $20 \cdot \log(rms(V_{out})/rms(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} @ $F = 217Hz$.

Table 9. $V_{CC} = +2.4V$, $GND = 0V$, $V_{IC} = 2.5V$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		1.7		mA
I_{STBY}	Standby current ⁽¹⁾	No input signal, $V_{STBY} = GND$		10		nA
V_{OO}	Output offset voltage	No input signal, $R_L = 8\Omega$		3		mV
P_{out}	Output power	G=6dB THD = 1% max, F = 1kHz, $R_L = 4\Omega$ THD = 10% max, F = 1kHz, $R_L = 4\Omega$ THD = 1% max, F = 1kHz, $R_L = 8\Omega$ THD = 10% max, F = 1kHz, $R_L = 8\Omega$		0.48 0.65 0.3 0.38		W
THD + N	Total harmonic distortion + noise	$P_{out} = 200mW_{RMS}$, G = 6dB, 20Hz < F < 20kHz $R_L = 8\Omega + 15\mu H$, BW < 30kHz		1		%
Efficiency	Efficiency	$P_{out} = 0.38W_{RMS}$, $R_L = 4\Omega + \geq 15\mu H$ $P_{out} = 0.25W_{RMS}$, $R_L = 8\Omega + \geq 15\mu H$		77 86		%
CMRR	Common mode rejection ratio	F = 217Hz, $R_L = 8\Omega$, G = 6dB, $\Delta V_{icm} = 200mV_{pp}$		54		dB
Gain	Gain value	R_{in} in k Ω	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from Standby to GND		273	300	327	k Ω
F_{PWM}	Pulse width modulator base frequency			250		kHz
SNR	Signal to noise ratio	A Weighting, $P_{out} = 1.2W$, $R_L = 8\Omega$		80		dB
t_{WU}	Wake-up time			5		ms
t_{STBY}	Standby time			5		ms
V_N	Output voltage noise	F = 20Hz to 20kHz, G = 6dB Unweighted $R_L = 4\Omega$ A-weighted $R_L = 4\Omega$		85 60		μV_{RMS}
		Unweighted $R_L = 8\Omega$ A-weighted $R_L = 8\Omega$		86 62		
		Unweighted $R_L = 4\Omega + 15\mu H$ A-weighted $R_L = 4\Omega + 15\mu H$		76 56		
		Unweighted $R_L = 4\Omega + 30\mu H$ A-weighted $R_L = 4\Omega + 30\mu H$		82 60		
		Unweighted $R_L = 8\Omega + 30\mu H$ A-weighted $R_L = 8\Omega + 30\mu H$		67 53		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		78 57		
		Unweighted $R_L = 4\Omega + \text{Filter}$ A-weighted $R_L = 4\Omega + \text{Filter}$		74 54		

1. Standby mode is active when V_{STBY} is tied to GND.

4 Electrical characteristic curves

The graphs included in this section use the following abbreviations:

- $R_L + 15\mu\text{H}$ or $30\mu\text{H}$ = pure resistor + very low series resistance inductor
- Filter = LC output filter ($1\mu\text{F} + 30\mu\text{H}$ for 4Ω and $0.5\mu\text{F} + 60\mu\text{H}$ for 8Ω)
- All measurements done with $C_{S1}=1\mu\text{F}$ and $C_{S2}=100\text{nF}$ except for PSRR where C_{S1} is removed.

Figure 2. Test diagram for measurements

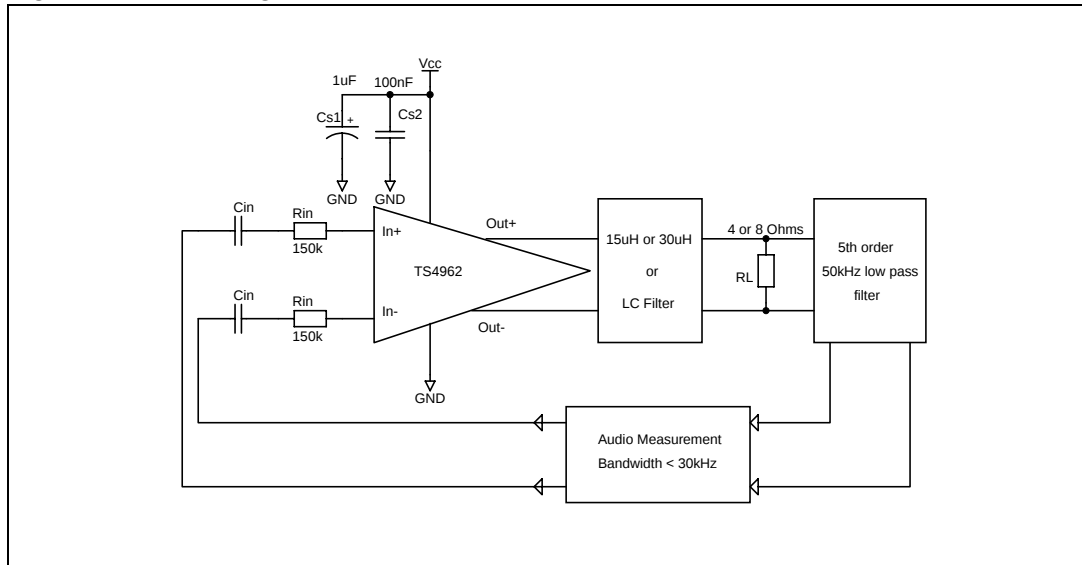


Figure 3. Test diagram for PSRR measurements

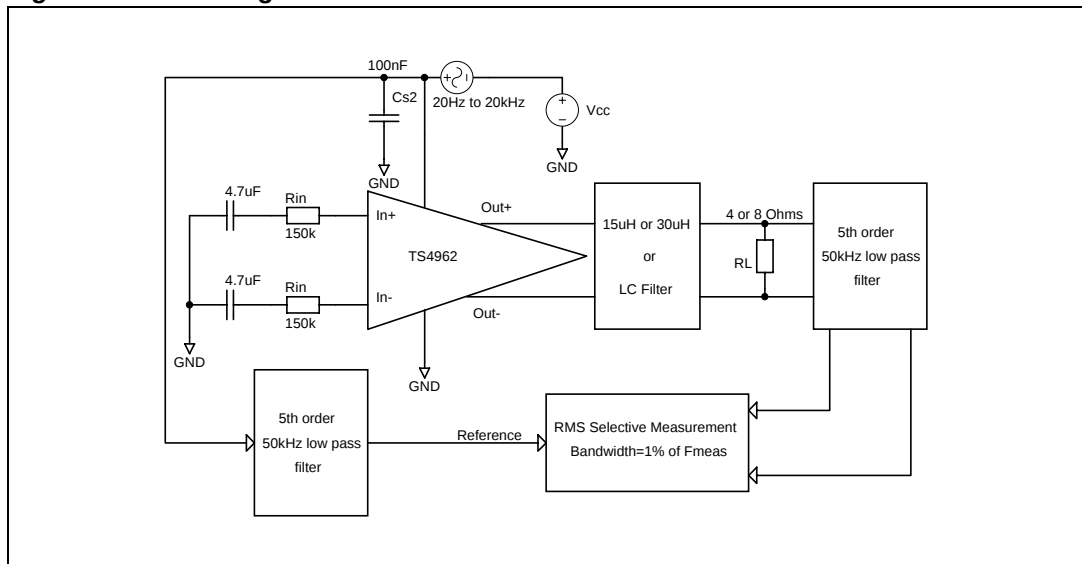


Figure 4. Current consumption vs. power supply voltage

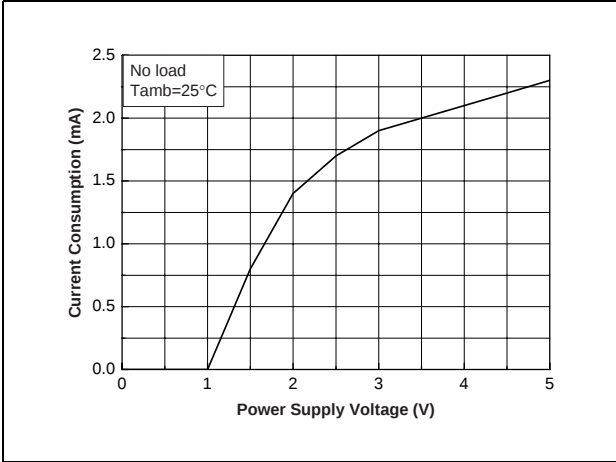


Figure 5. Current consumption vs. standby voltage

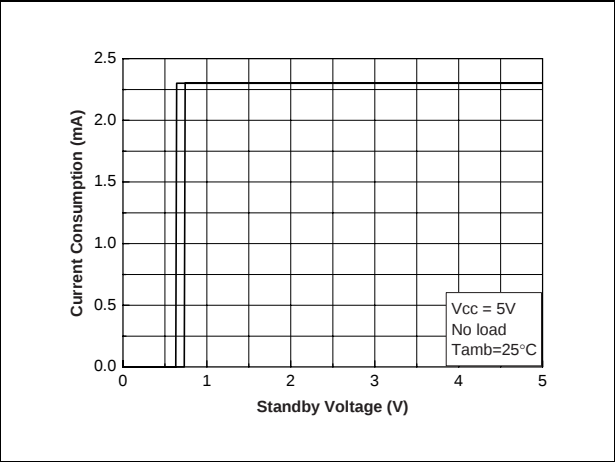


Figure 6. Current consumption vs. standby voltage

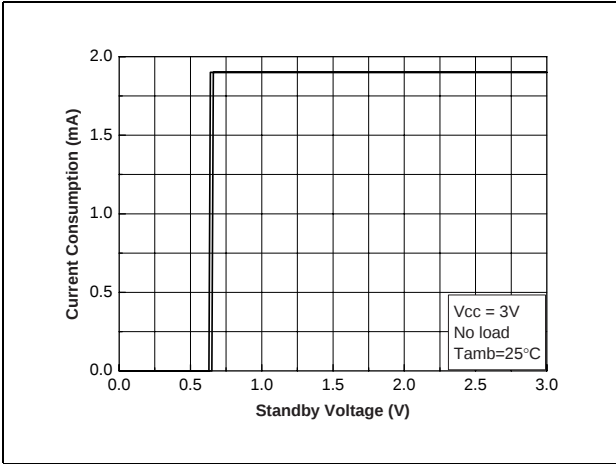


Figure 7. Output offset voltage vs. common mode input voltage

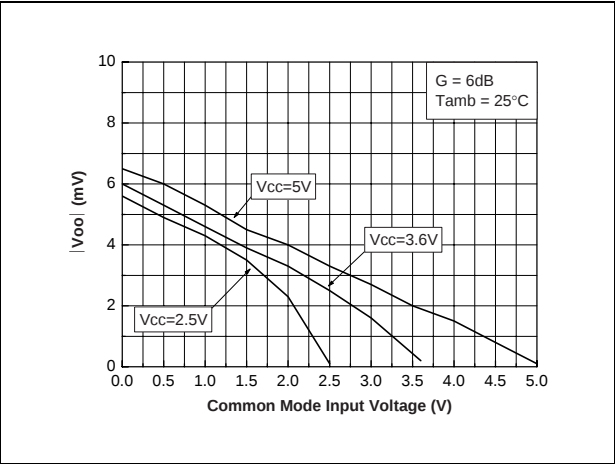


Figure 8. Efficiency vs. output power

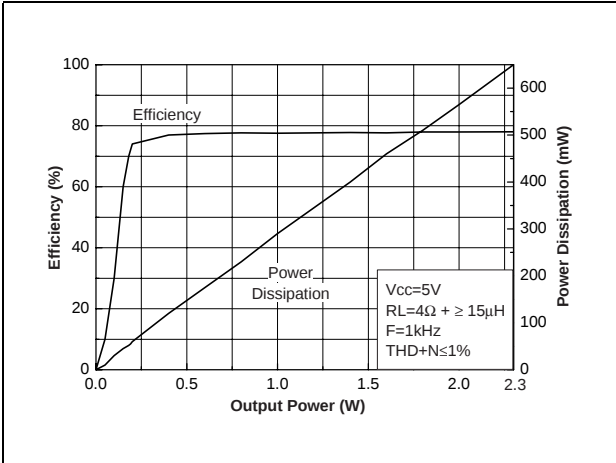


Figure 9. Efficiency vs. output power

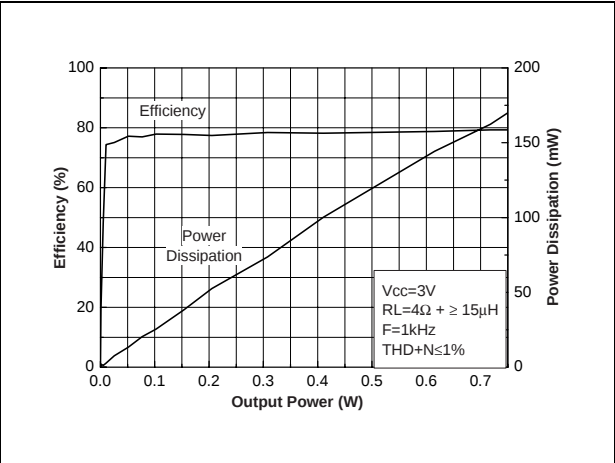


Figure 10. Efficiency vs. output power

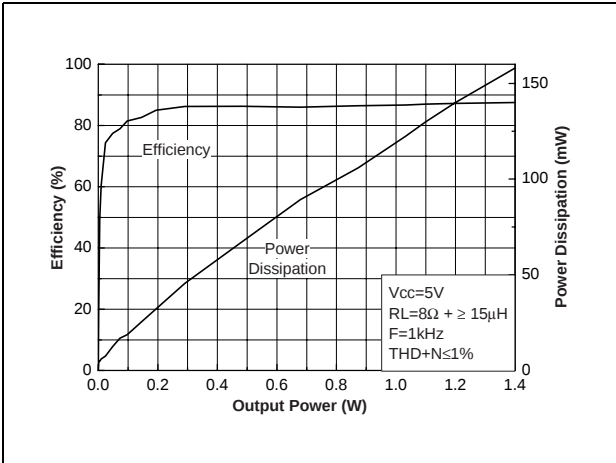


Figure 11. Efficiency vs. output power

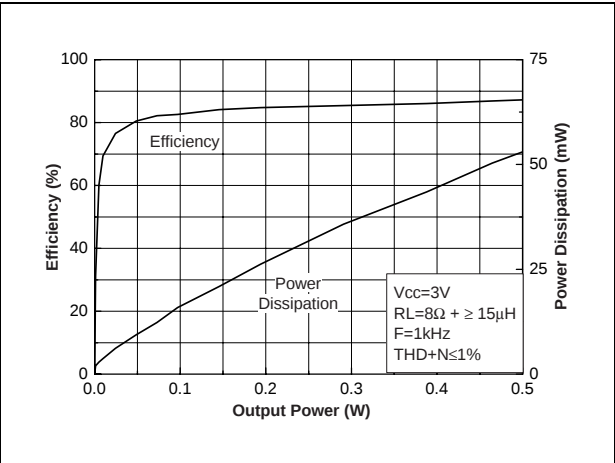


Figure 12. Output power vs. power supply voltage

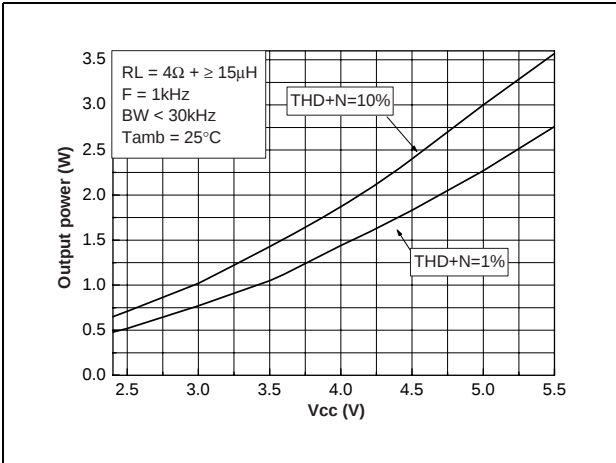


Figure 13. Output power vs. power supply voltage

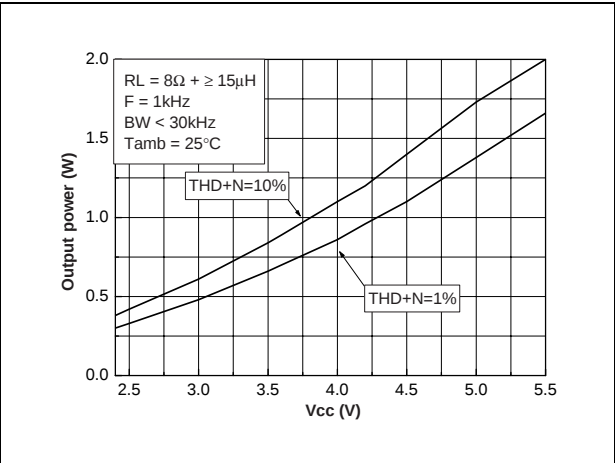


Figure 14. PSRR vs. frequency

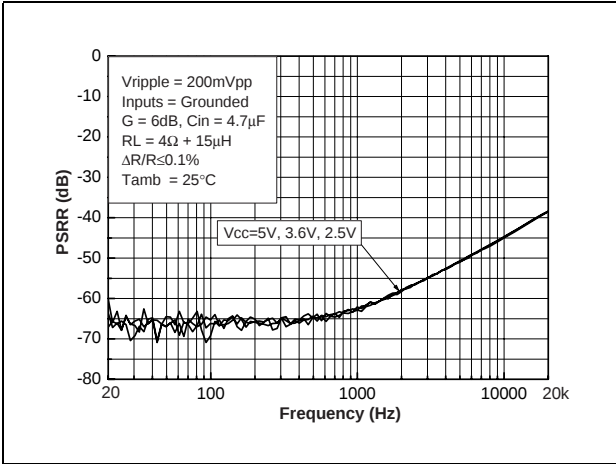


Figure 15. PSRR vs. frequency

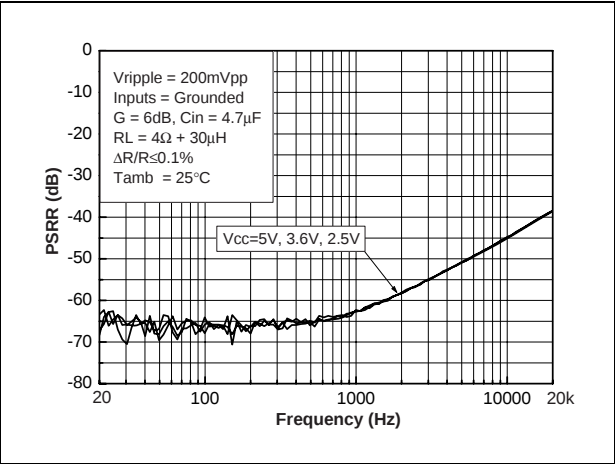


Figure 16. PSRR vs. frequency

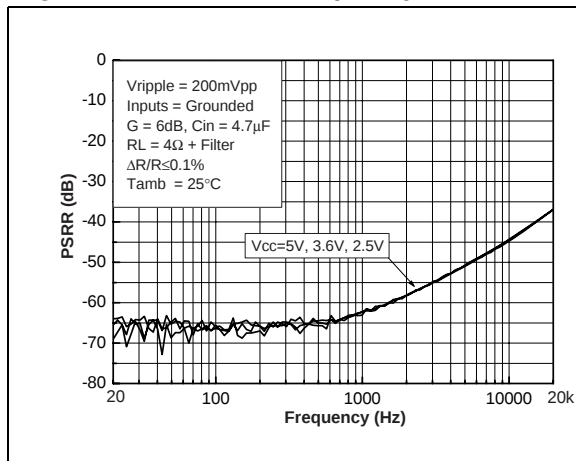


Figure 17. PSRR vs. frequency

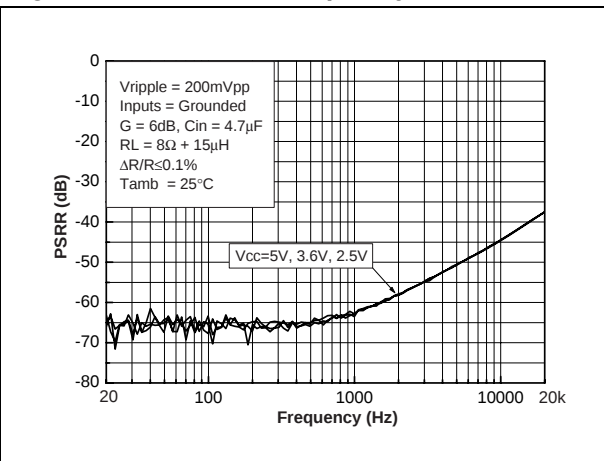


Figure 18. PSRR vs. frequency

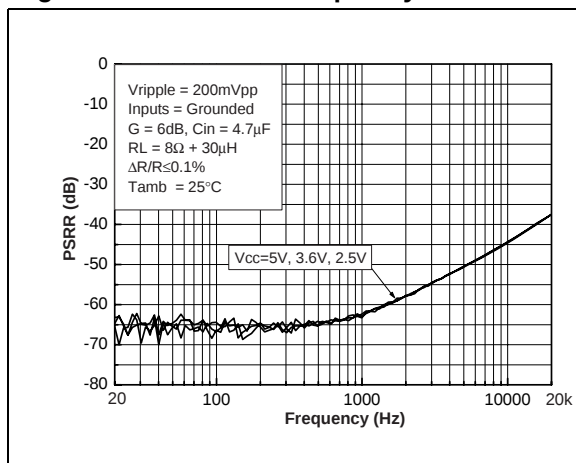


Figure 19. PSRR vs. frequency

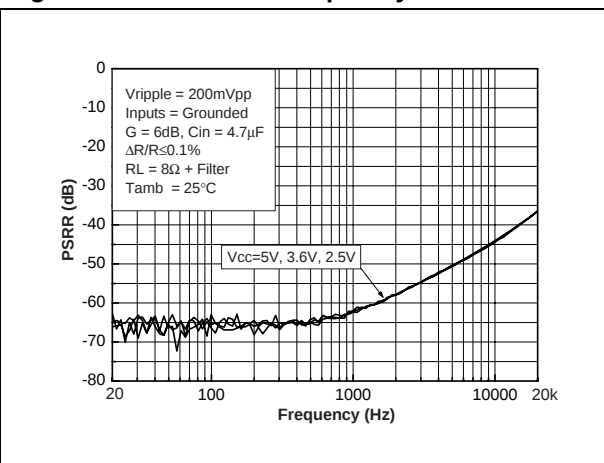


Figure 20. PSRR vs. common mode input voltage

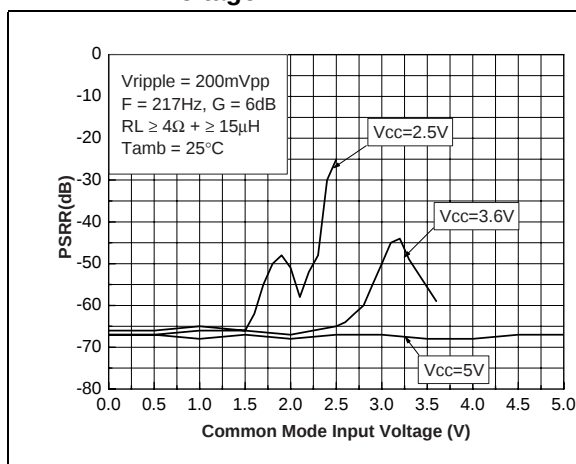


Figure 21. CMRR vs. frequency

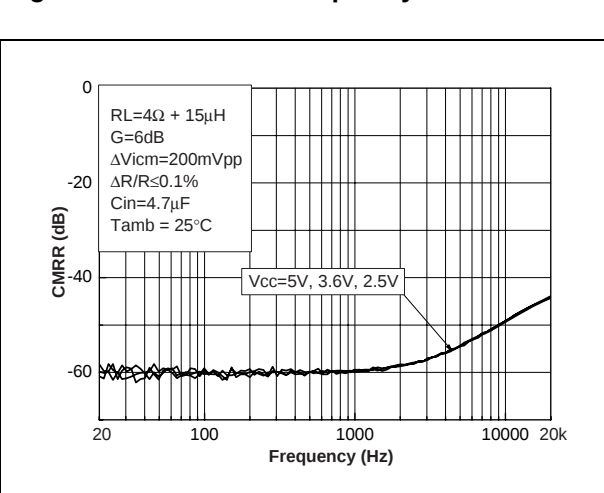


Figure 22. CMRR vs. frequency

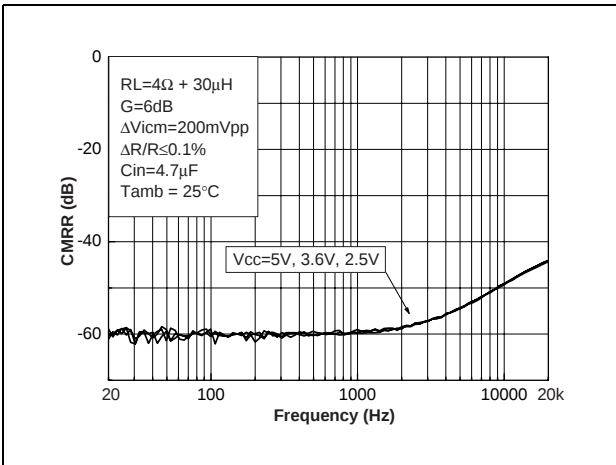


Figure 23. CMRR vs. frequency

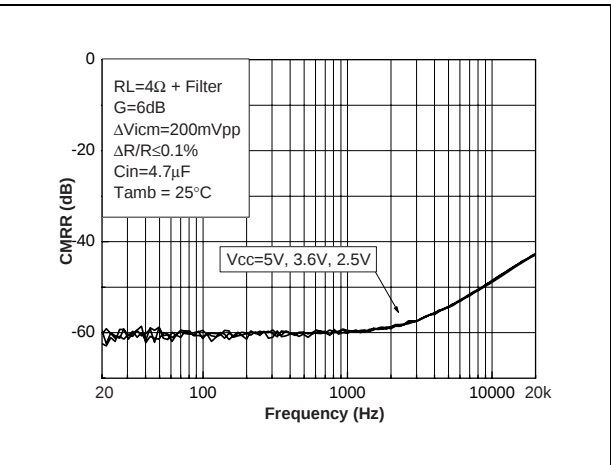


Figure 24. CMRR vs. frequency

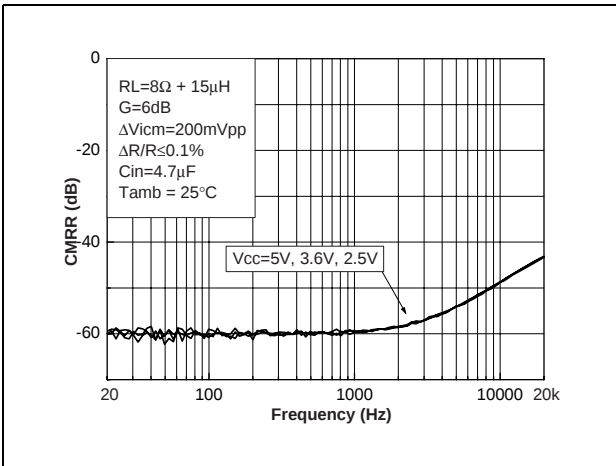


Figure 25. CMRR vs. frequency

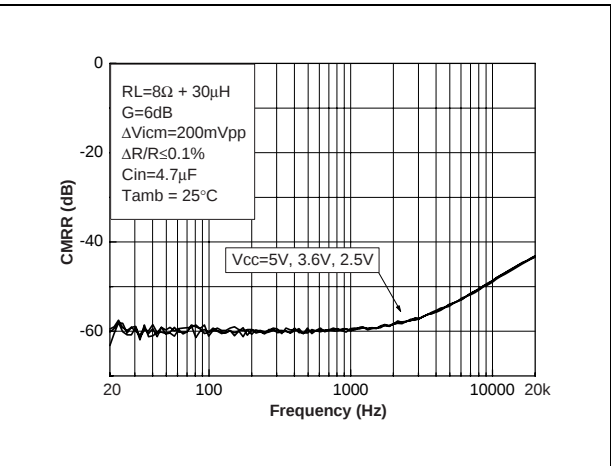


Figure 26. CMRR vs. frequency

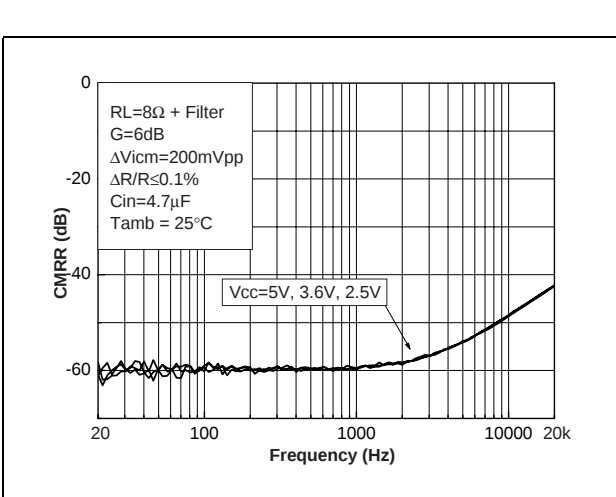


Figure 27. CMRR vs. common mode input voltage

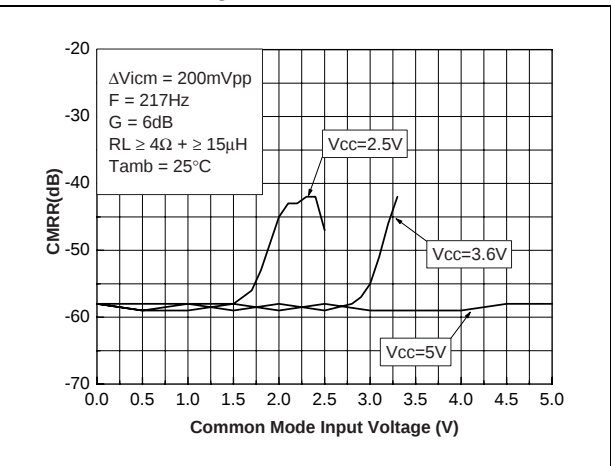


Figure 28. THD+N vs. output power

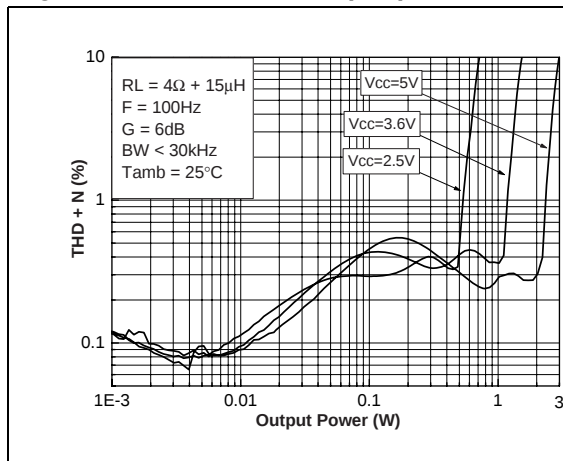


Figure 29. THD+N vs. output power

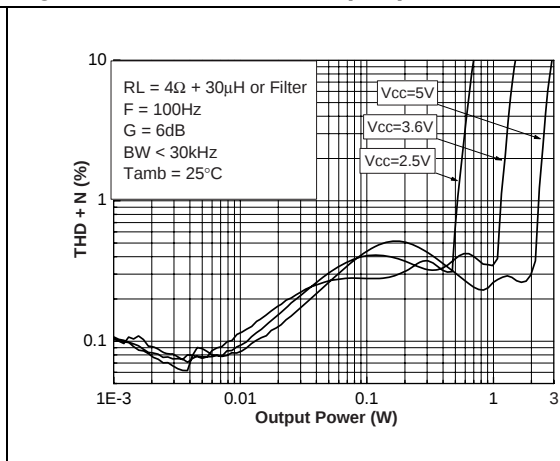


Figure 30. THD+N vs. output power

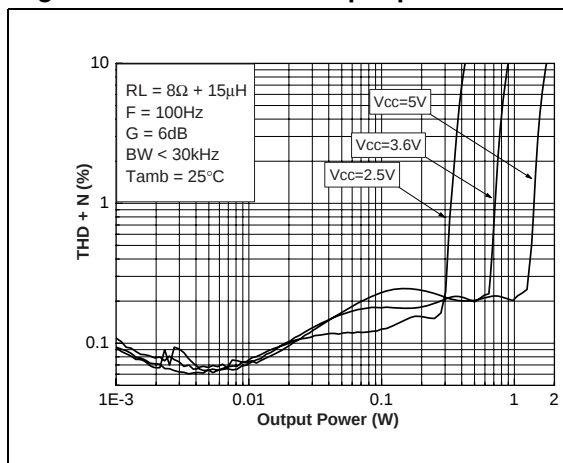


Figure 31. THD+N vs. output power

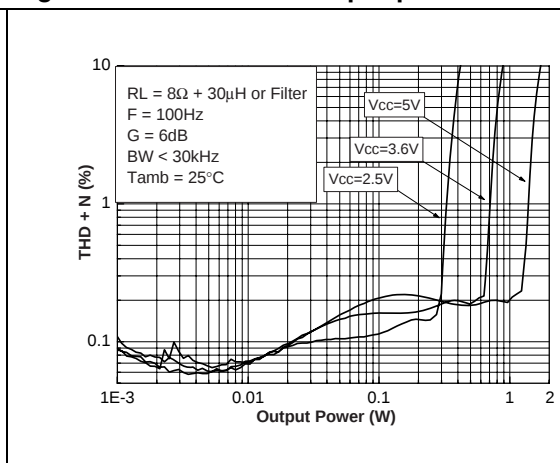


Figure 32. THD+N vs. output power

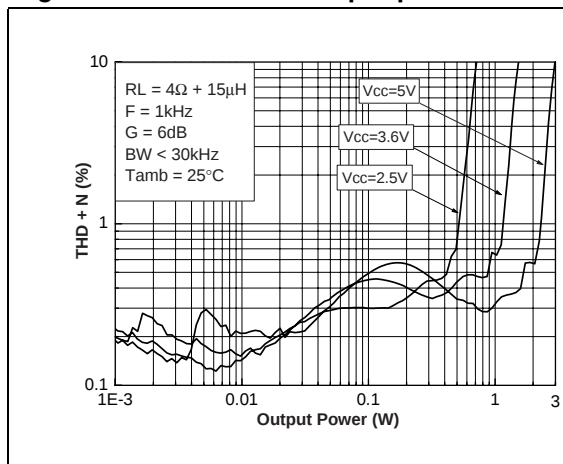


Figure 33. THD+N vs. output power

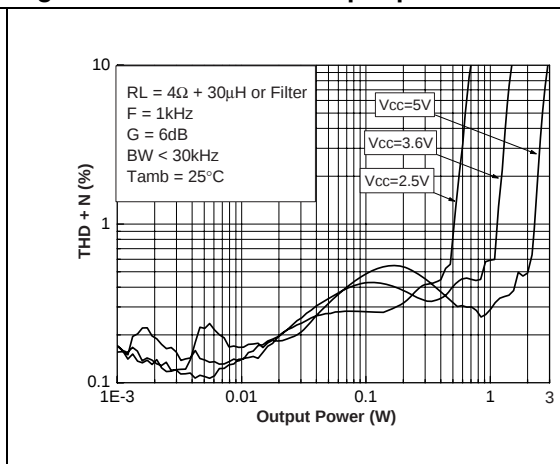


Figure 34. THD+N vs. output power

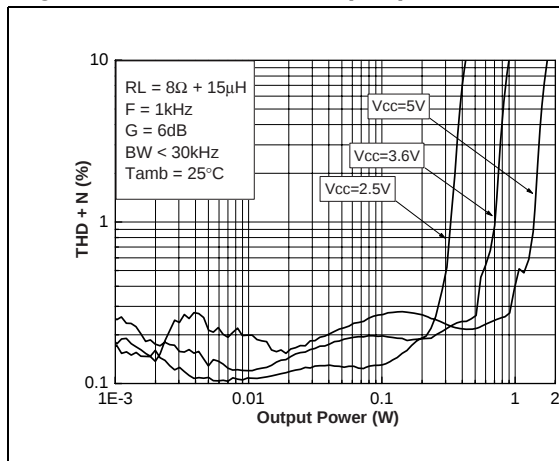


Figure 35. THD+N vs. output power

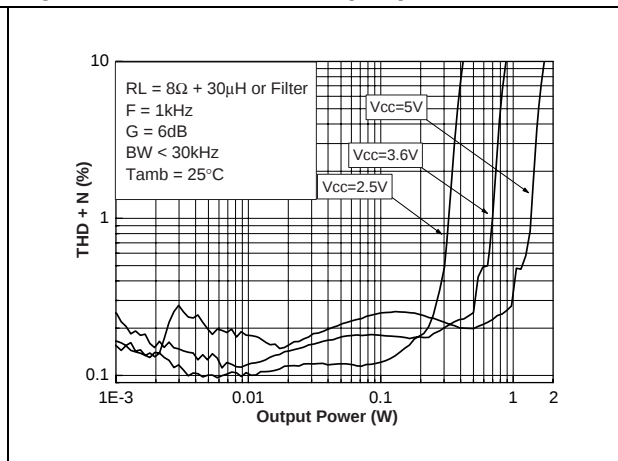


Figure 36. THD+N vs. frequency

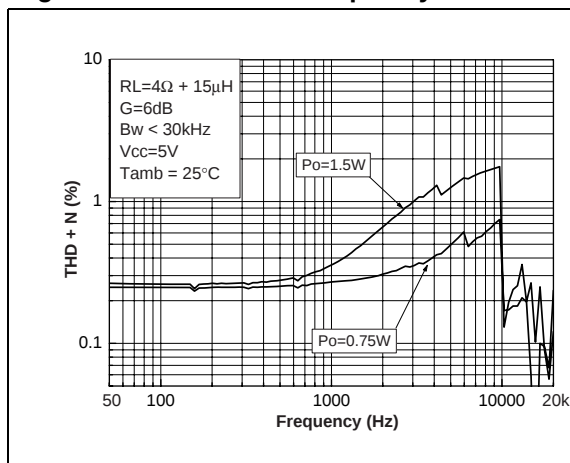


Figure 37. THD+N vs. frequency

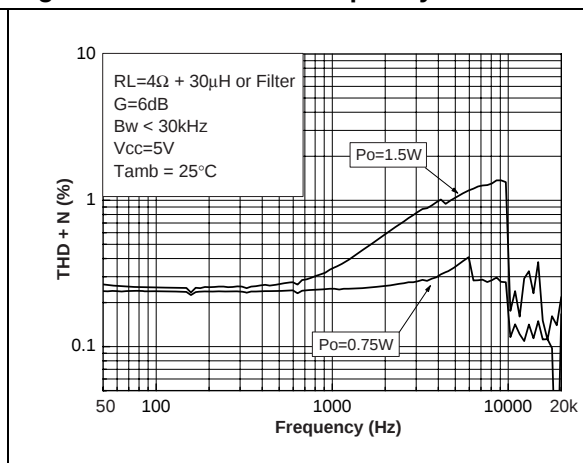


Figure 38. THD+N vs. frequency

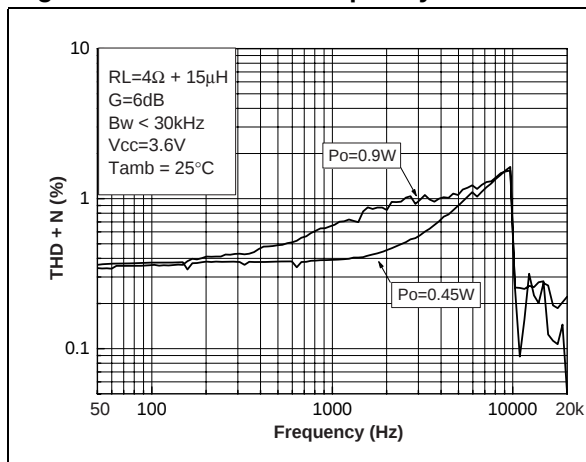


Figure 39. THD+N vs. frequency

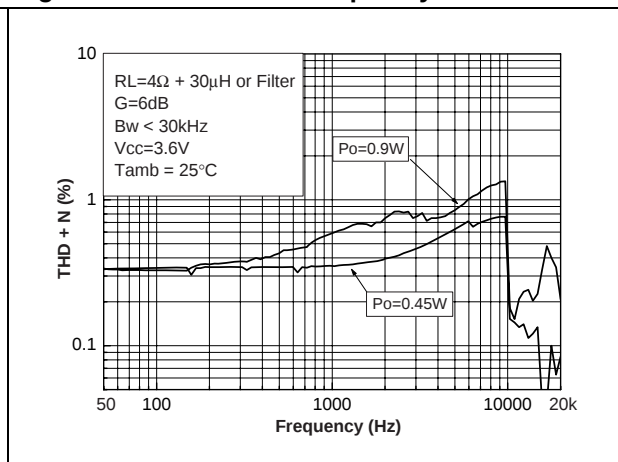


Figure 40. THD+N vs. frequency

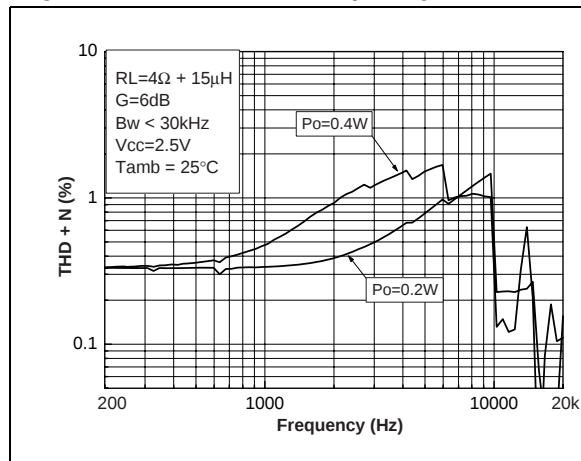


Figure 41. THD+N vs. frequency

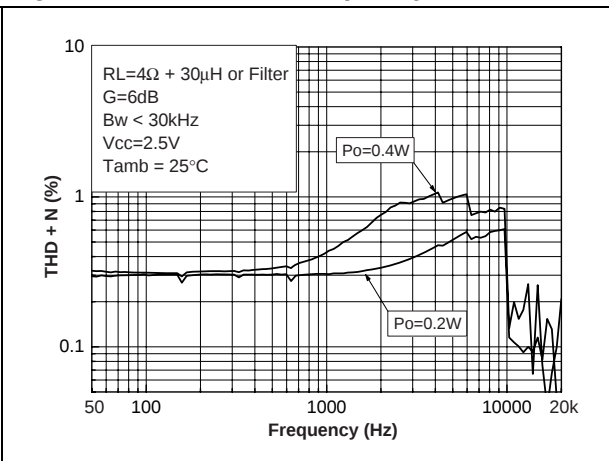


Figure 42. THD+N vs. frequency

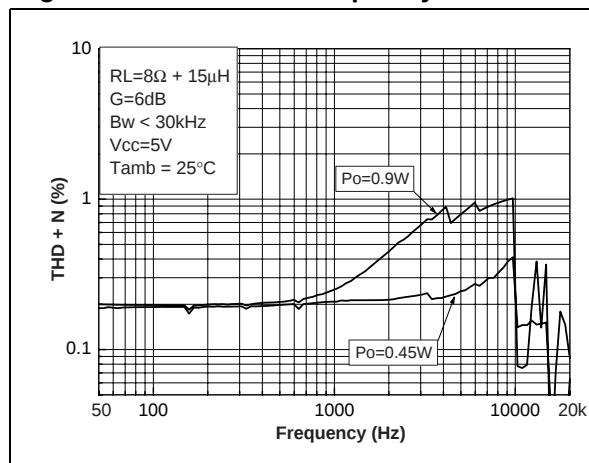


Figure 43. THD+N vs. frequency

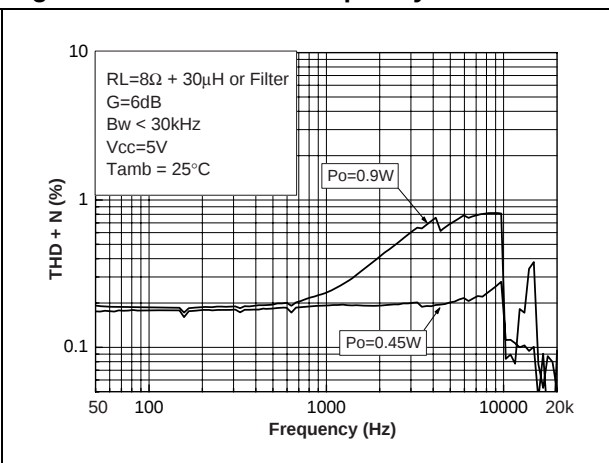


Figure 44. THD+N vs. frequency

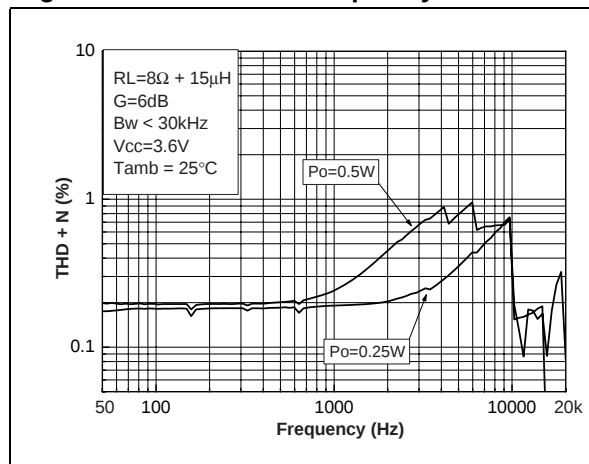


Figure 45. THD+N vs. frequency

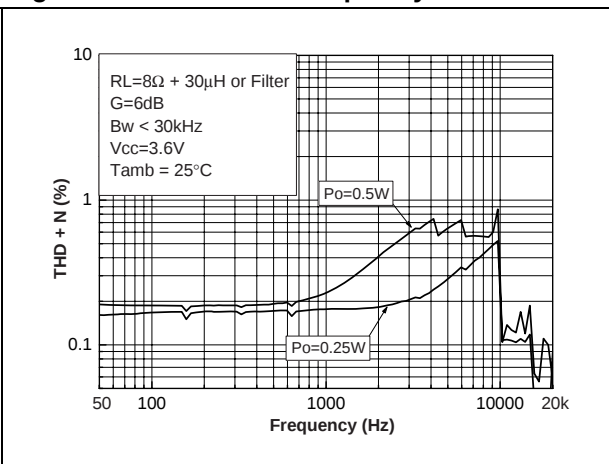


Figure 46. THD+N vs. frequency

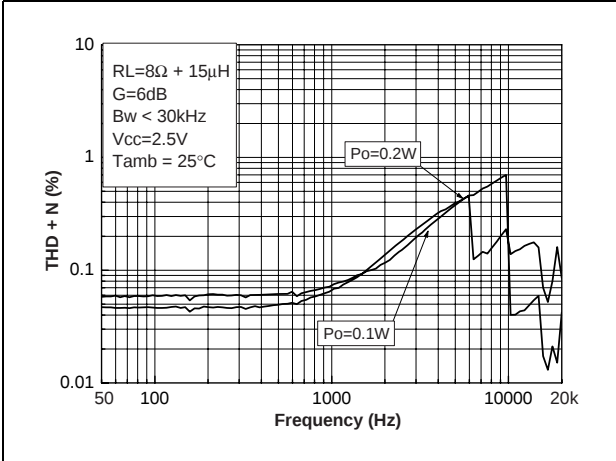


Figure 47. THD+N vs. frequency

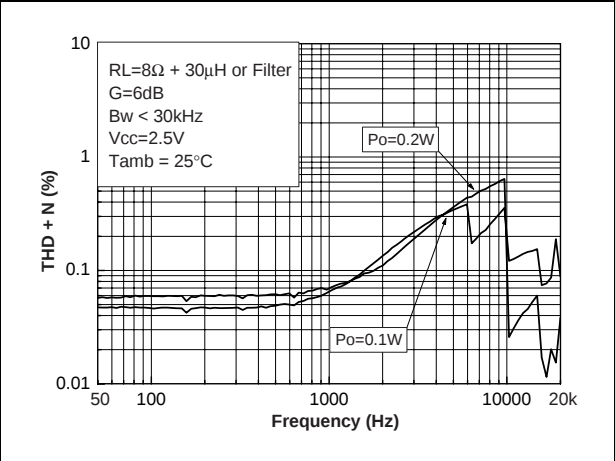


Figure 48. Gain vs. frequency

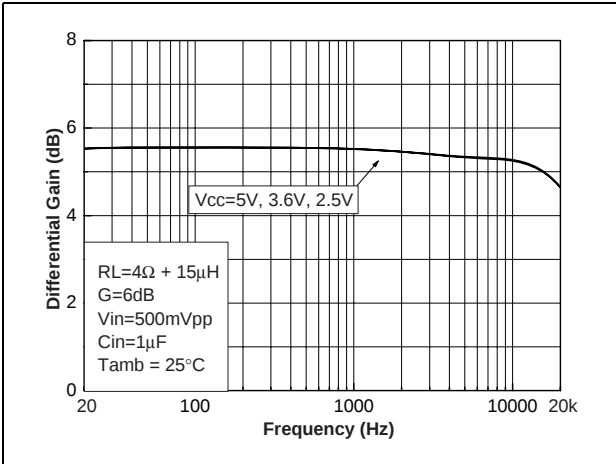


Figure 49. Gain vs. frequency

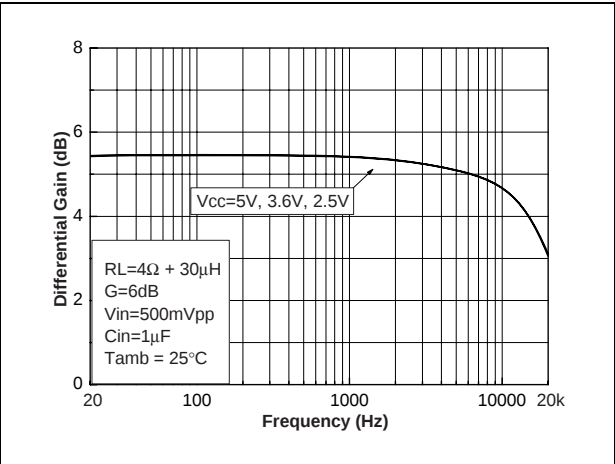


Figure 50. Gain vs. frequency

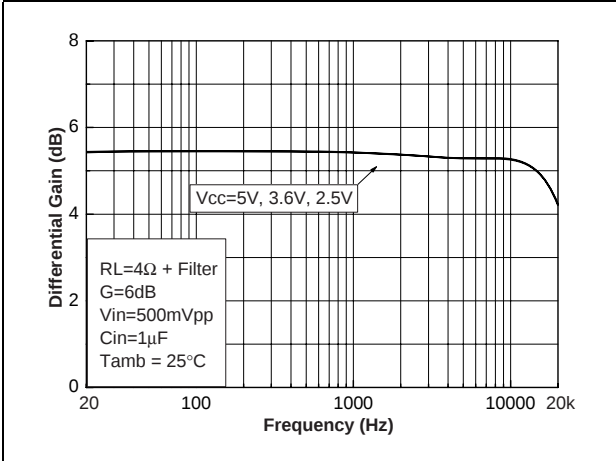


Figure 51. Gain vs. frequency

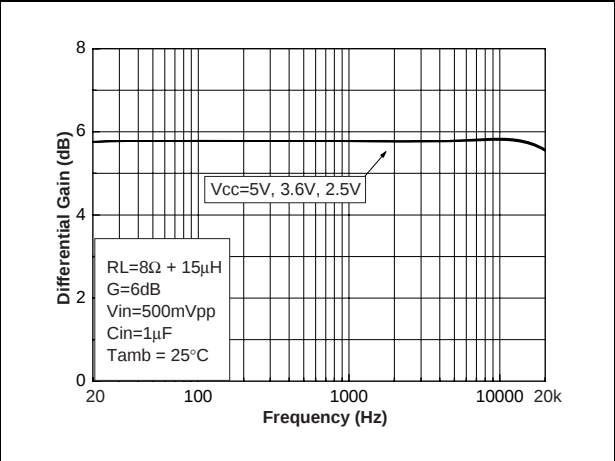


Figure 52. Gain vs. frequency

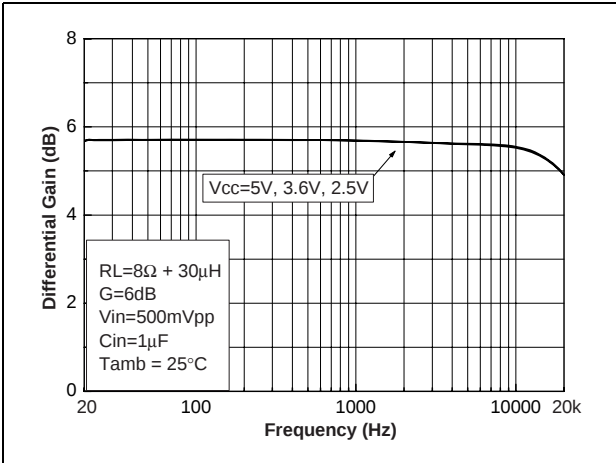


Figure 53. Gain vs. frequency

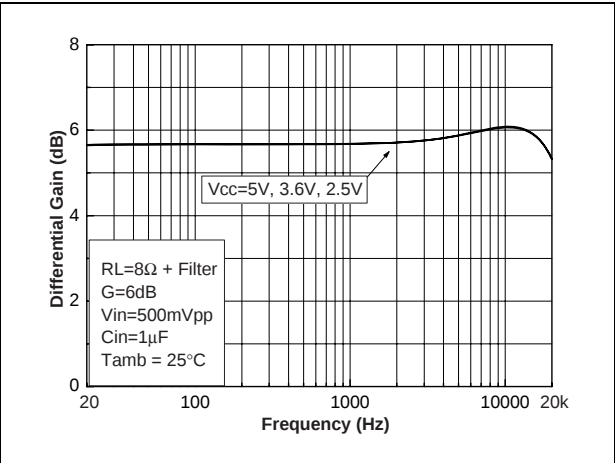


Figure 54. Gain vs. frequency

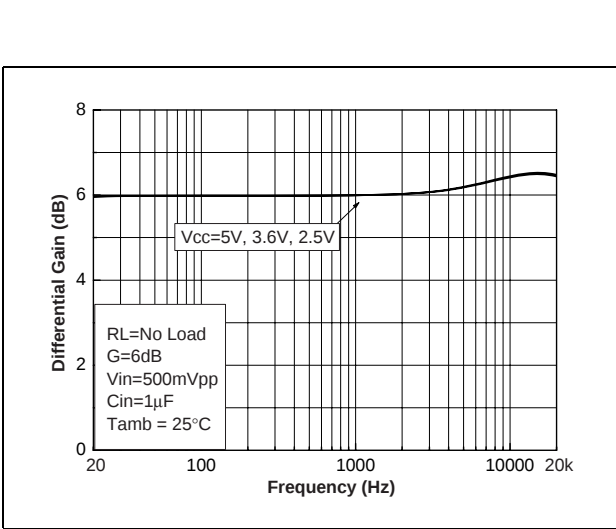


Figure 55. Startup & shutdown time
 $V_{CC} = 5V, G = 6dB, C_{in} = 1\mu F$
(5ms/div)

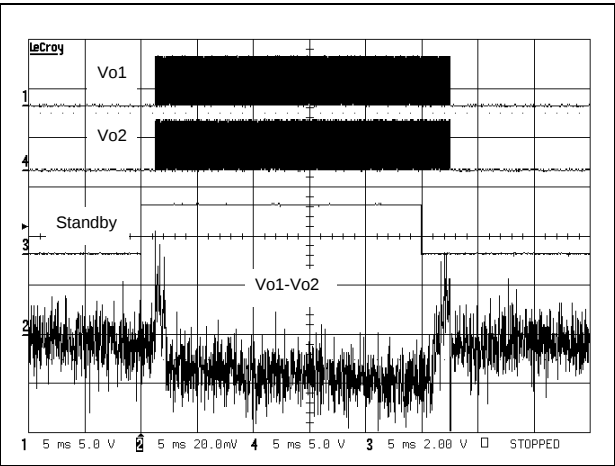


Figure 56. Startup & shutdown time
 $V_{CC} = 3V$, $G = 6dB$, $C_{in} = 1\mu F$
(5ms/div)

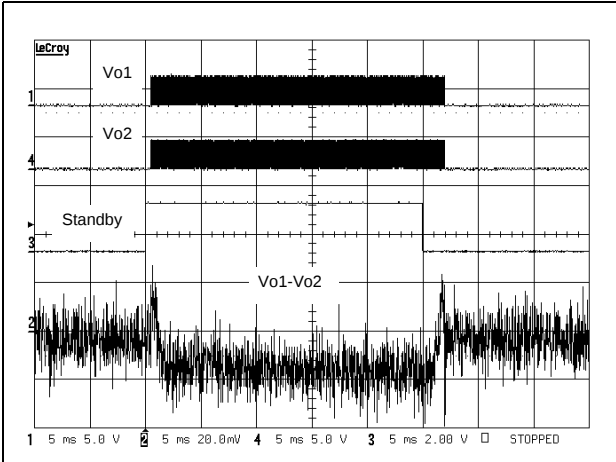


Figure 57. Startup & shutdown time
 $V_{CC} = 5V$, $G = 6dB$, $C_{in} = 100nF$
(5ms/div)

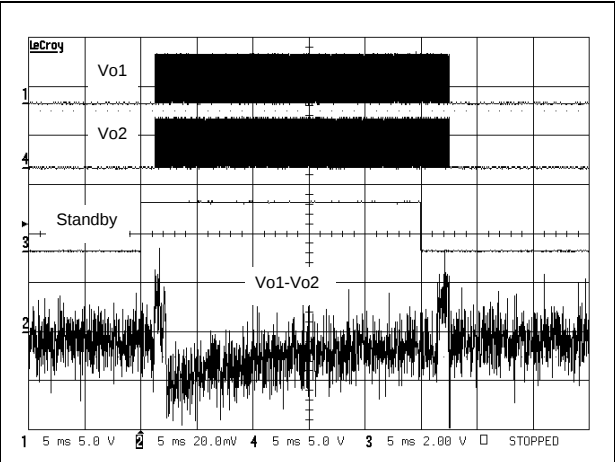


Figure 58. Startup & shutdown time
 $V_{CC} = 3V$, $G = 6dB$, $C_{in} = 100nF$
(5ms/div)

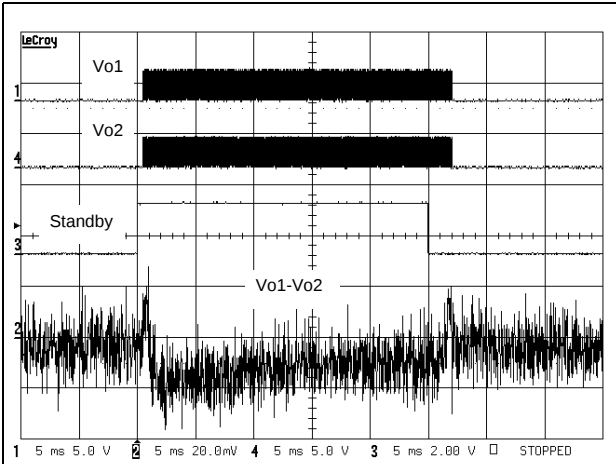


Figure 59. Startup & shutdown time
 $V_{CC} = 5V$, $G = 6dB$, No C_{in} (5ms/div)

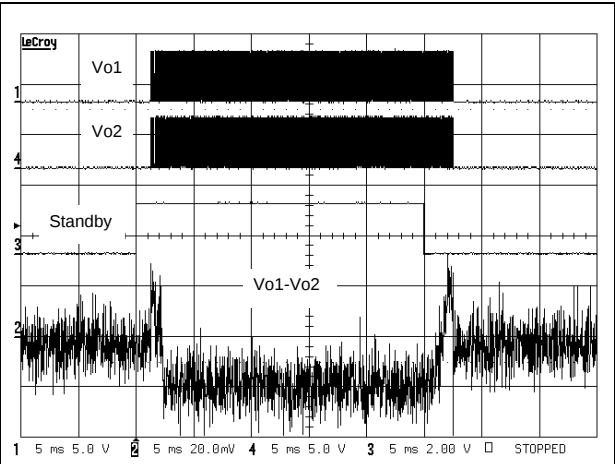
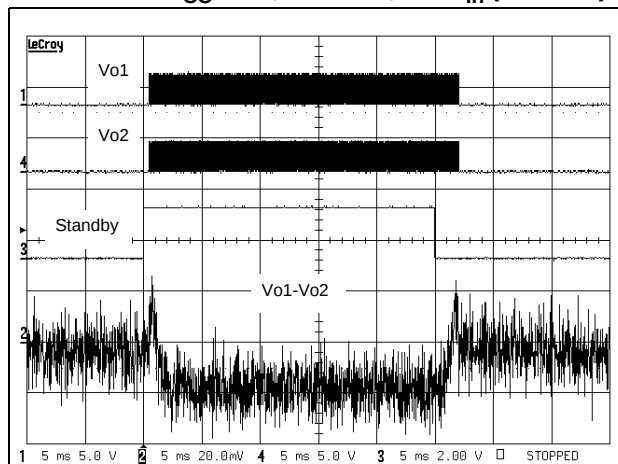


Figure 60. Startup & shutdown time
 $V_{CC} = 3V$, $G = 6dB$, No C_{in} (5ms/div)



5 Application information

5.1 Differential configuration principle

The TS4962M is a monolithic fully-differential input/output class D power amplifier. The TS4962M also includes a common-mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximizes the output power. Moreover, as the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

The advantages of a full-differential amplifier are:

- High PSRR (power supply rejection ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers.
- Easier interfacing with differential output audio DAC.
- No input coupling capacitors required due to common mode feedback loop.

The main disadvantage is:

- As the differential function is directly linked to external resistor mismatching, paying particular attention to this mismatching is mandatory in order to obtain the best performance from the amplifier.

5.2 Gain in typical application schematic

Typical differential applications are shown in [Figure 1 on page 4](#).

In the flat region of the frequency-response curve (no input coupling capacitor effect), the differential gain is expressed by the relation:

$$A_{V_{diff}} = \frac{Out^+ - Out^-}{In^+ - In^-} = \frac{300}{R_{in}}$$

with R_{in} expressed in $k\Omega$

Due to the tolerance of the internal $150k\Omega$ feedback resistor, the differential gain will be in the range (no tolerance on R_{in}):

$$\frac{273}{R_{in}} \leq A_{V_{diff}} \leq \frac{327}{R_{in}}$$

5.3 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

However, due to V_{icm} limitation in the input stage (see [Table 2: Operating conditions on page 3](#)), the common mode feedback loop can ensure its role only within a defined range. This range depends upon the values of V_{CC} and R_{in} (A_{Vdiff}). To have a good estimation of the V_{icm} value, we can apply this formula (no tolerance on R_{in}):

$$V_{icm} = \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 150k\Omega}{2 \times (R_{in} + 150k\Omega)} \quad (V)$$

with

$$V_{IC} = \frac{In^+ + In^-}{2} \quad (V)$$

and the result of the calculation must be in the range:

$$0.5V \leq V_{icm} \leq V_{CC} - 0.8V$$

Due to the +/-9% tolerance on the 150kΩ resistor, it's also important to check V_{icm} in these conditions:

$$\frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 136.5k\Omega}{2 \times (R_{in} + 136.5k\Omega)} \leq V_{icm} \leq \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 163.5k\Omega}{2 \times (R_{in} + 163.5k\Omega)}$$

If the result of V_{icm} calculation is not in the previous range, input coupling capacitors must be used (with V_{CC} from 2.4V to 2.5V, input coupling capacitors are mandatory).

For example:

With $V_{CC} = 3V$, $R_{in} = 150k$ and $V_{IC} = 2.5V$, we typically find $V_{icm} = 2V$ and this is lower than $3V - 0.8V = 2.2V$. With 136.5kΩ we find 1.97V, and with 163.5kΩ we have 2.02V. So, no input coupling capacitors are required.

5.4 Low frequency response

If a low frequency bandwidth limitation is requested, it is possible to use input coupling capacitors.

In the low frequency region, C_{in} (input coupling capacitor) starts to have an effect. C_{in} forms, with R_{in} , a first order high-pass filter with a -3dB cut-off frequency:

$$F_{CL} = \frac{1}{2\pi \times R_{in} \times C_{in}} \quad (Hz)$$

So, for a desired cut-off frequency we can calculate C_{in} ,

$$C_{in} = \frac{1}{2\pi \times R_{in} \times F_{CL}} \quad (F)$$

with R_{in} in Ω and F_{CL} in Hz.

5.5 Decoupling of the circuit

A power supply capacitor, referred to as C_S , is needed to correctly bypass the TS4962M.

The TS4962M has a typical switching frequency at 250kHz and output fall and rise time about 5ns. Due to these very fast transients, careful decoupling is mandatory.

A 1 μ F ceramic capacitor is enough, but it must be located very close to the TS4962M in order to avoid any extra parasitic inductance created an overly long track wire. In relation with dI/dt , this parasitic inductance introduces an overvoltage that decreases the global efficiency and, if it is too high, may cause a breakdown of the device.

In addition, even if a ceramic capacitor has an adequate high frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4 Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1 μ F/6.3V capacitor used at 5V, loses about 50% of its value. In fact, with a 5V power supply voltage, the decoupling value is about 0.5 μ F instead of 1 μ F. As C_S has particular influence on the THD+N in the medium-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots, which can be problematic if they reach the power supply AMR value (6V).

5.6 Wake-up time (t_{WU})

When the standby is released to set the device ON, there is a wait of about 5ms. The TS4962M has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

5.7 Shutdown time (t_{STBY})

When the standby command is set, the time required to put the two output stages into high impedance and to put the internal circuitry in shutdown mode, is about 5ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

5.8 Consumption in shutdown mode

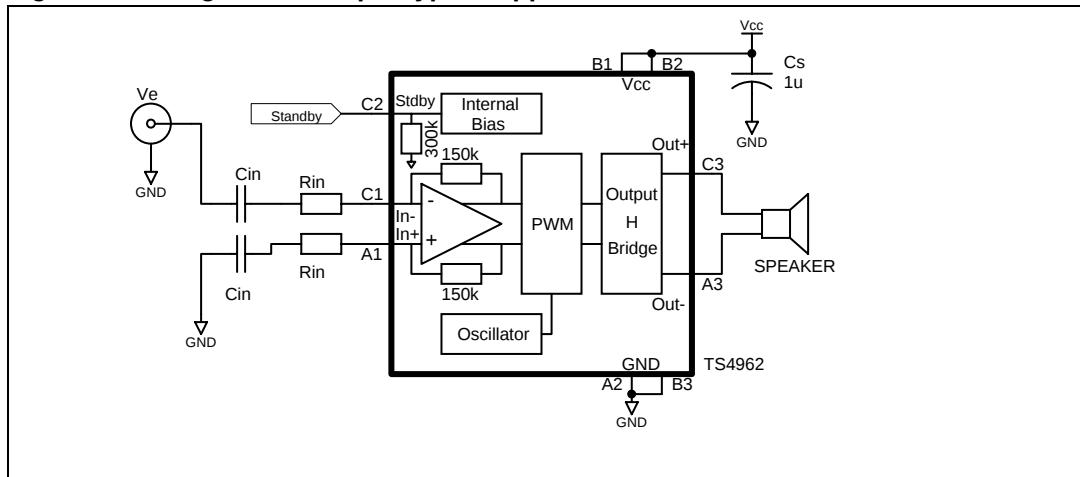
Between the shutdown pin and GND there is an internal 300k Ω resistor. This resistor forces the TS4962M to be in standby mode when the standby input pin is left floating.

However, this resistor also introduces additional power consumption if the shutdown pin voltage is not 0V.

For example, with a 0.4V standby voltage pin, [Table 2: Operating conditions on page 3](#), shows that you must add $0.4V/300k\Omega = 1.3\mu A$ in typical ($0.4V/273k\Omega = 1.46\mu A$ in maximum) to the shutdown current specified in [Table 4 on page 5](#).

5.9 Single-ended input configuration

It is possible to use the TS4962M in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The schematic in [Figure 61](#) shows a single-ended input typical application.

Figure 61. Single-ended input typical application

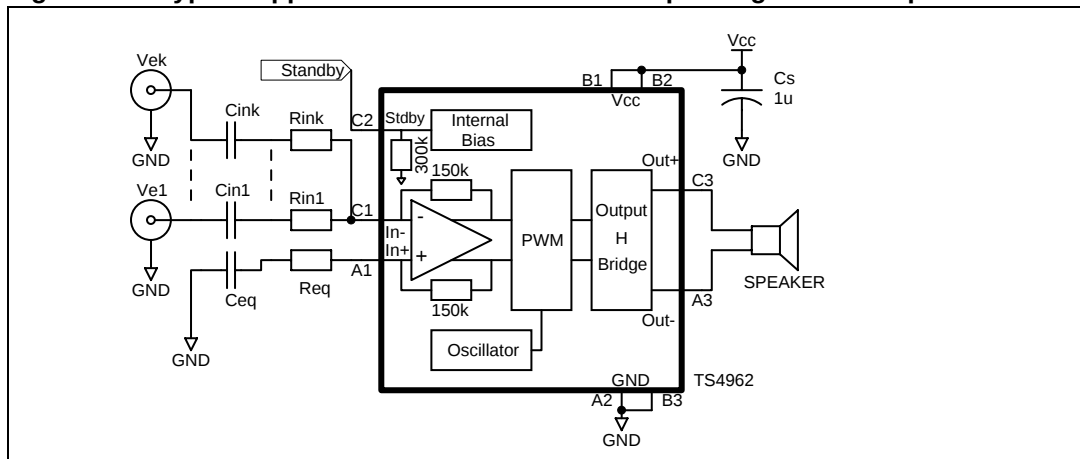
All formulas are identical except for the gain (with R_{in} in $k\Omega$) :

$$A_{V_{single}} = \frac{V_e}{Out^+ - Out^-} = \frac{300}{R_{in}}$$

And, due to the internal resistor tolerance we have:

$$\frac{273}{R_{in}} \leq A_{V_{single}} \leq \frac{327}{R_{in}}$$

In the event that multiple single-ended inputs are summed, it is important that the impedance on both TS4962M inputs (In^- and In^+) are equal.

Figure 62. Typical application schematic with multiple single-ended inputs

We have the following equations:

$$\text{Out}^+ - \text{Out}^- = V_{e1} \times \frac{300}{R_{in1}} + \dots + V_{ek} \times \frac{300}{R_{ink}} \quad (V)$$

$$C_{eq} = \sum_{j=1}^k C_{inj}$$

$$C_{inj} = \frac{1}{2 \times \pi \times R_{inj} \times F_{CLj}} \quad (F)$$

$$R_{eq} = \frac{1}{\sum_{j=1}^k \frac{1}{R_{inj}}}$$

In general, for mixed situations (single-ended and differential inputs), it is best to use the same rule, that is, to equalize impedance on both TS4962M inputs.

5.10 Output filter considerations

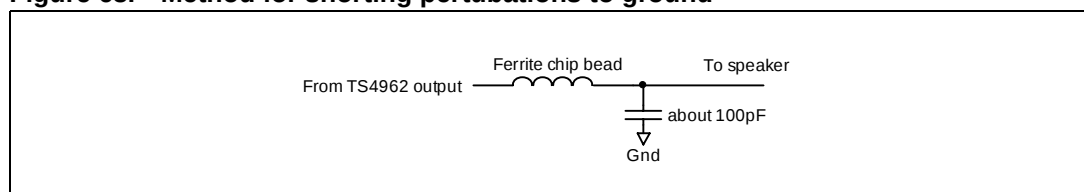
The TS4962M is designed to operate without an output filter. However, due to very sharp transients on the TS4962M output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS4962M outputs and loudspeaker terminal is long (typically more than 50mm, or 100mm in both directions, to the speaker terminals). As the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow:

- Reduce, as much as possible, the distance between the TS4962M output pins and the speaker terminals.
- Use ground planes for “shielding” sensitive wires.
- Place, as close as possible to the TS4962M and in series with each output, a ferrite bead with a rated current at minimum 2A and impedance greater than 50Ω at frequencies above 30MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit. Murata BLM18EG221SN1 or BLM18EG121SN1 are possible examples of devices you can use.
- Allow enough footprint to place, if necessary, a capacitor to short perturbations to ground (see the schematics in [Figure 63](#)).

Figure 63. Method for shorting perturbations to ground

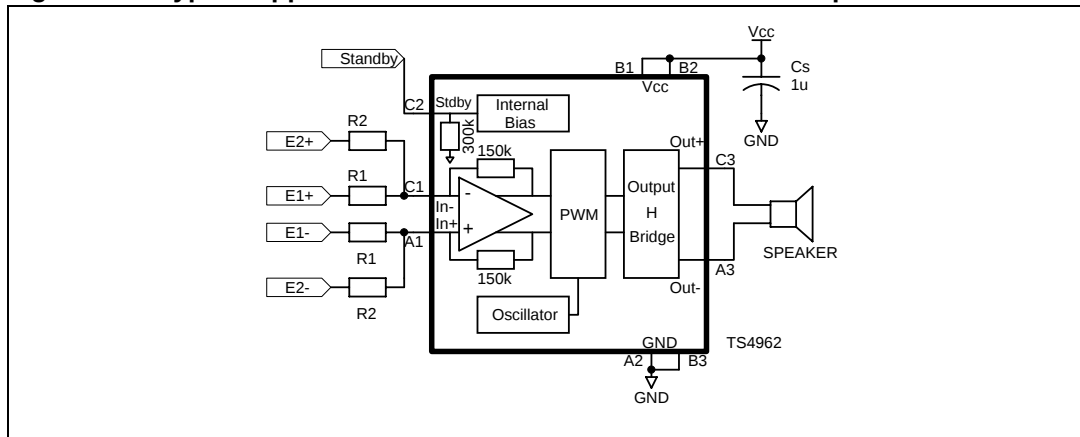


In the case where the distance between the TS4962M outputs and speaker terminals is high, it is possible to have low frequency EMI issues due to the fact that the typical operating frequency is 250kHz. In this configuration, we recommend using an output filter (as shown in [Figure 1: Typical application schematics on page 4](#)). It should be placed as close as possible to the device.

5.11 Different examples with summed inputs

Example 1: Dual differential inputs

Figure 64. Typical application schematic with dual differential inputs



With (R_i in $k\Omega$):

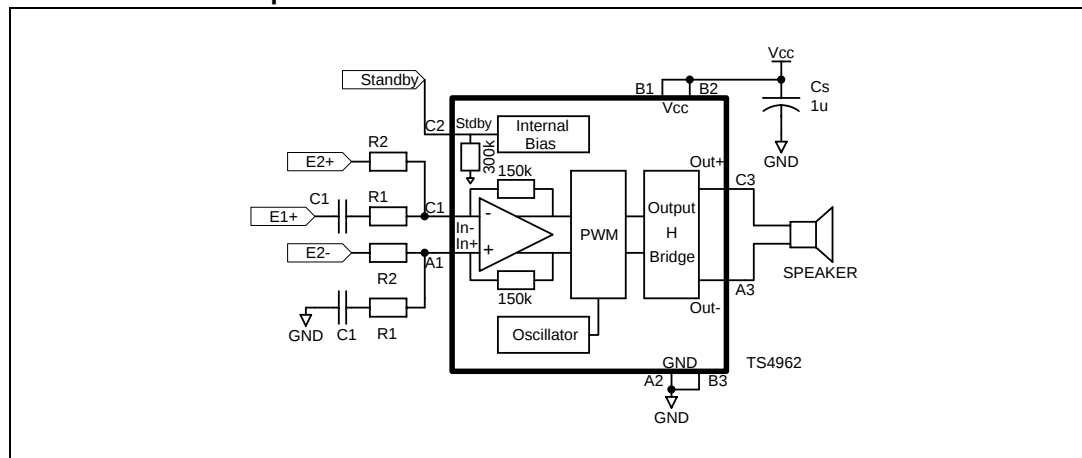
$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^+ - E_1^-} = \frac{300}{R_1}$$

$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^+ - E_2^-} = \frac{300}{R_2}$$

$$0.5V \leq \frac{V_{CC} \times R_1 \times R_2 + 300 \times (V_{IC1} \times R_2 + V_{IC2} \times R_1)}{300 \times (R_1 + R_2) + 2 \times R_1 \times R_2} \leq V_{CC} - 0.8V$$

$$V_{IC1} = \frac{E_1^+ + E_1^-}{2} \quad \text{and} \quad V_{IC2} = \frac{E_2^+ + E_2^-}{2}$$

Figure 65. Typical application schematic with one differential input plus one single-ended input


$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^+} = \frac{300}{R_1}$$

$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^+ - E_2^-} = \frac{300}{R_2}$$

$$C_1 = \frac{1}{2\pi \times R_1 \times F_{CL}} \quad (F)$$

6 Demoboard

A demoboard for the TS4962M is available with a flip-chip to DIP adapter. For more information about this demoboard, refer to **Application Note AN2134**.

Figure 66. Schematic diagram of mono class D demoboard for TS4962M

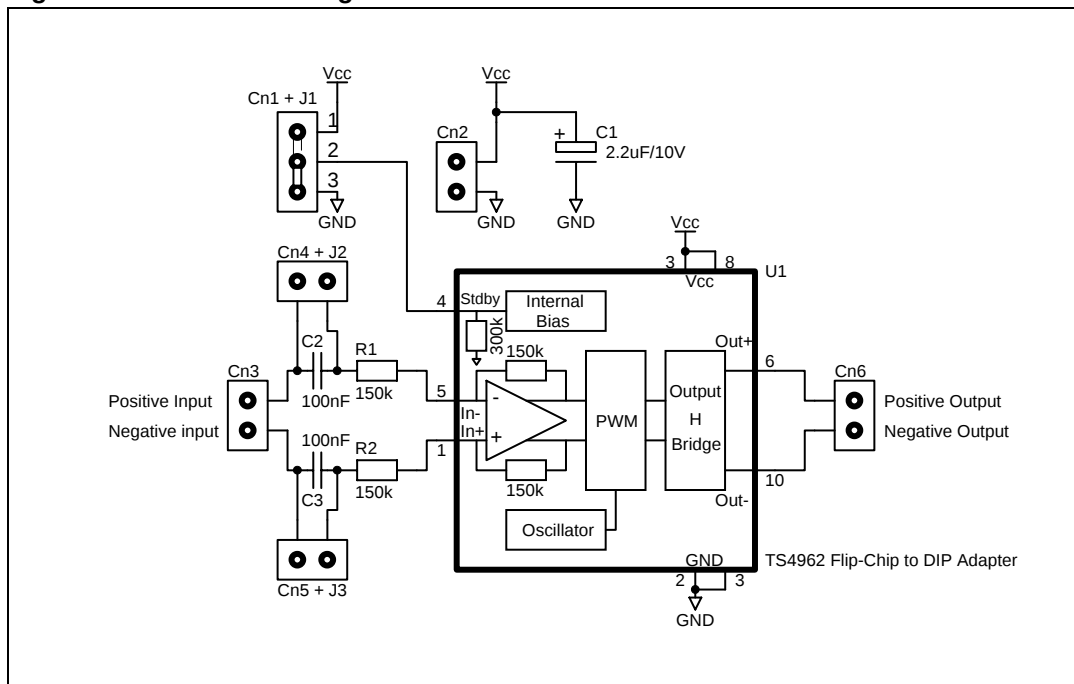


Figure 67. Diagram for flip-chip-to-DIP adapter

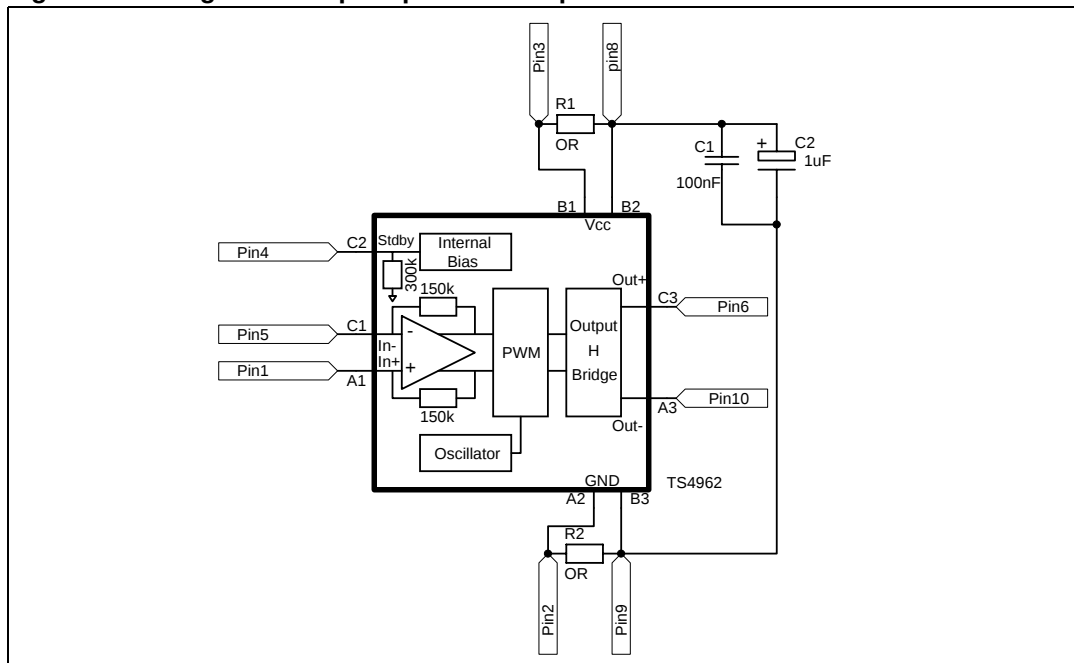


Figure 68. Top view

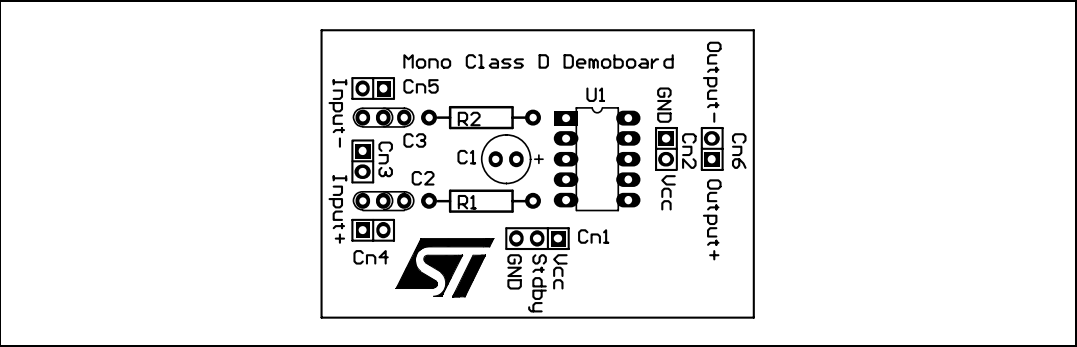


Figure 69. Bottom layer

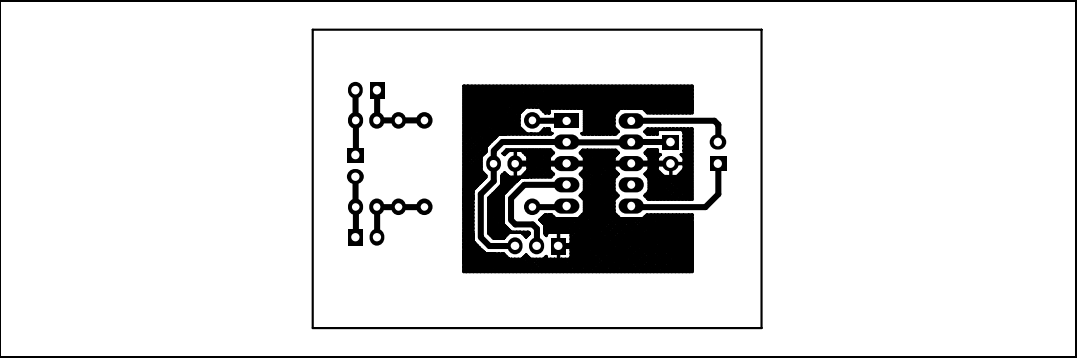
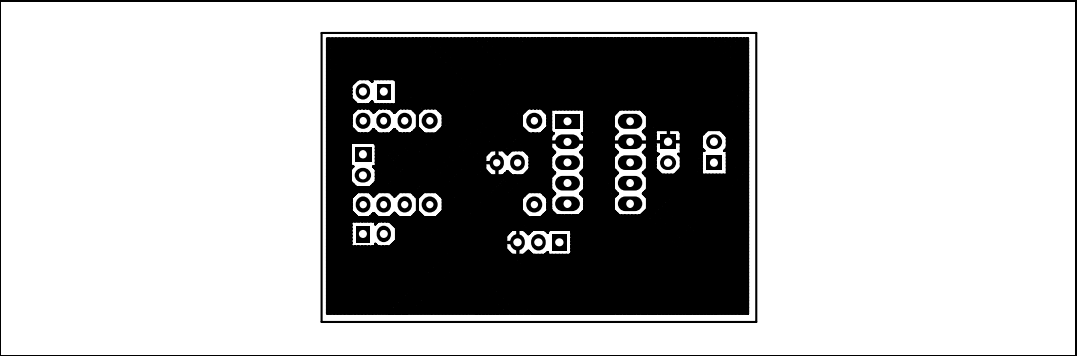
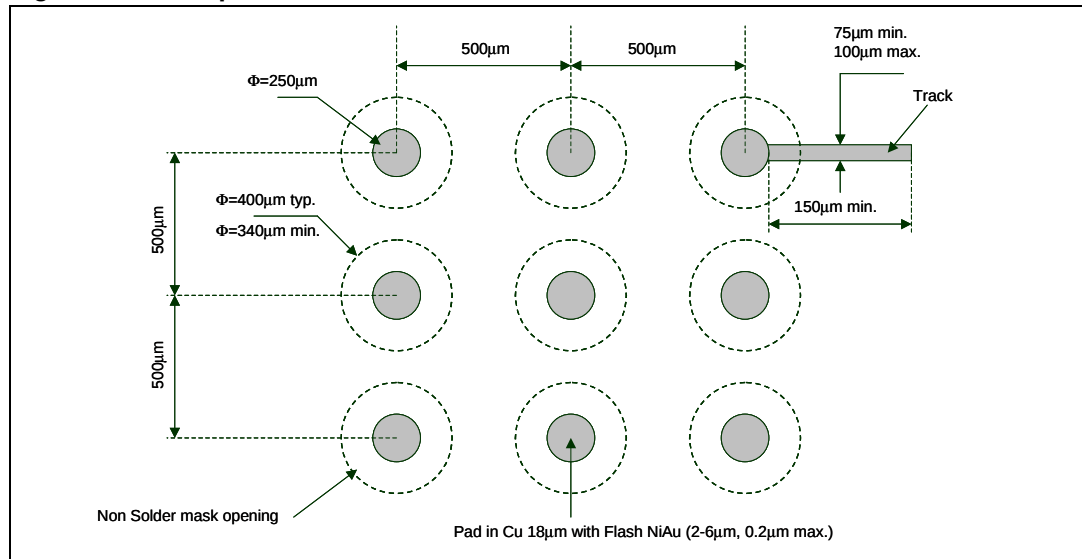


Figure 70. Top layer



7 Footprint recommendations

Figure 71. Footprint recommendations



8 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 72. Pin-out for 9-bump flip-chip (top view)

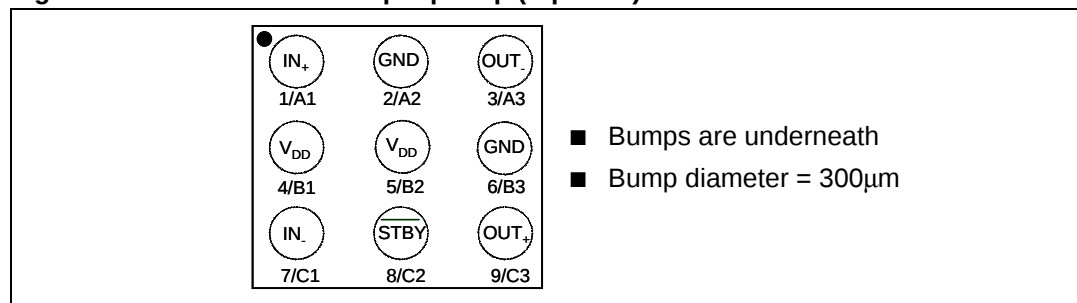


Figure 73. Marking for 9-bump flip-chip (top view)

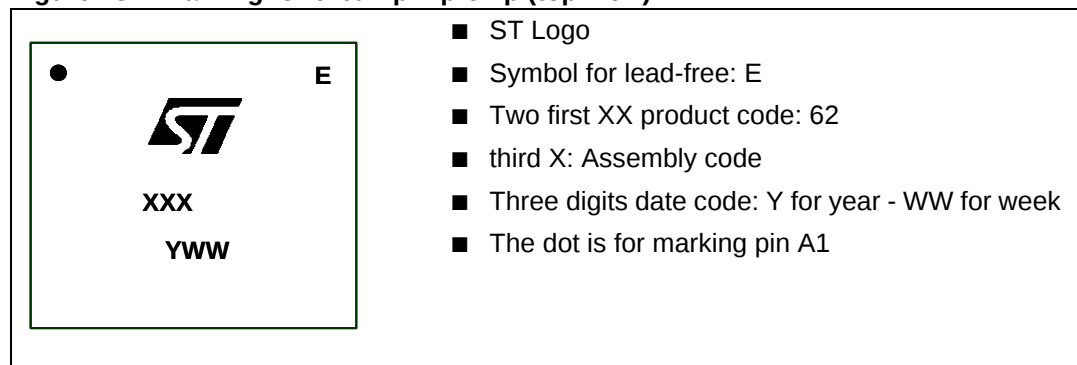
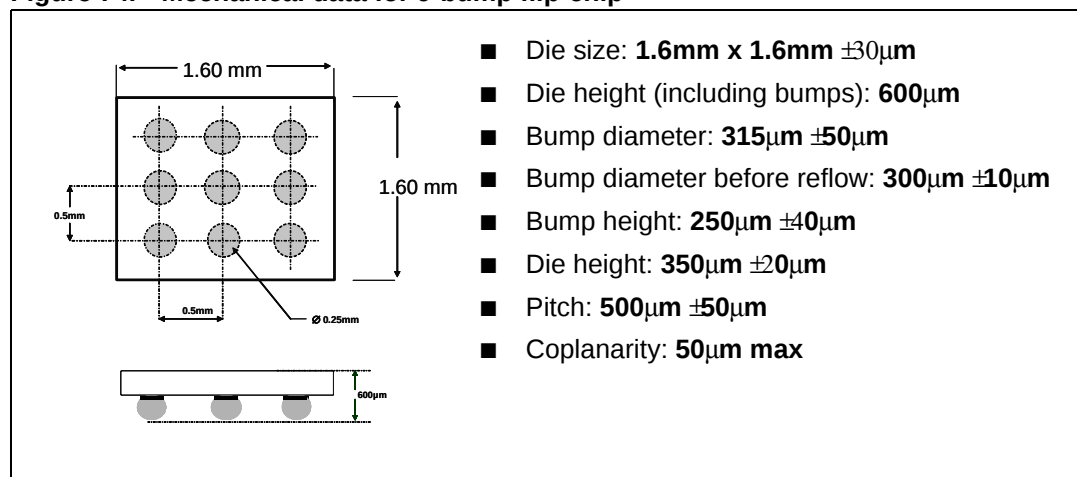


Figure 74. Mechanical data for 9-bump flip-chip



9 Ordering information

Table 10. Order codes

Part number	Temperature range	Package	Packing	Marking
TS4962MEIJT	-40°C to +85°C	Lead-free flip-chip	Tape & reel	62

10 Revision history

Date	Revision	Changes
Oct. 2005	1	First release corresponding to the product preview version.
Nov. 2005	2	Electrical data updated for output voltage noise, see Table 4 , Table 5 , Table 6 , Table 7 , Table 8 and Table 9 Formatting changes throughout.
Dec. 2005	3	Product in full production.
10-Jan-2007	4	Template update, no technical changes.

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