VND920-E

DOUBLE CHANNEL HIGH SIDE SOLID STATE RELAY

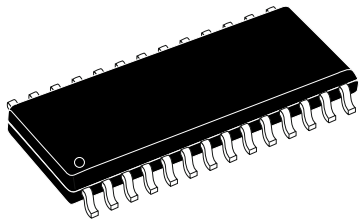
Table 1. General Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VND920-E	16mΩ	35 A (*)	36 V

(*) Per channel with all the output pins connected to the PCB.

- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V_{CC}
- VERY LOW STAND-BY POWER DISSIPATION
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



SO-28 (DOUBLE ISLAND)

DESCRIPTION

The VND920-E is a double chip device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. Built-in analog current sense output delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSO-10™	VND920-E	VND920TR-E

Note: (**) See application schematic at page 9.

Figure 2. Block Diagram

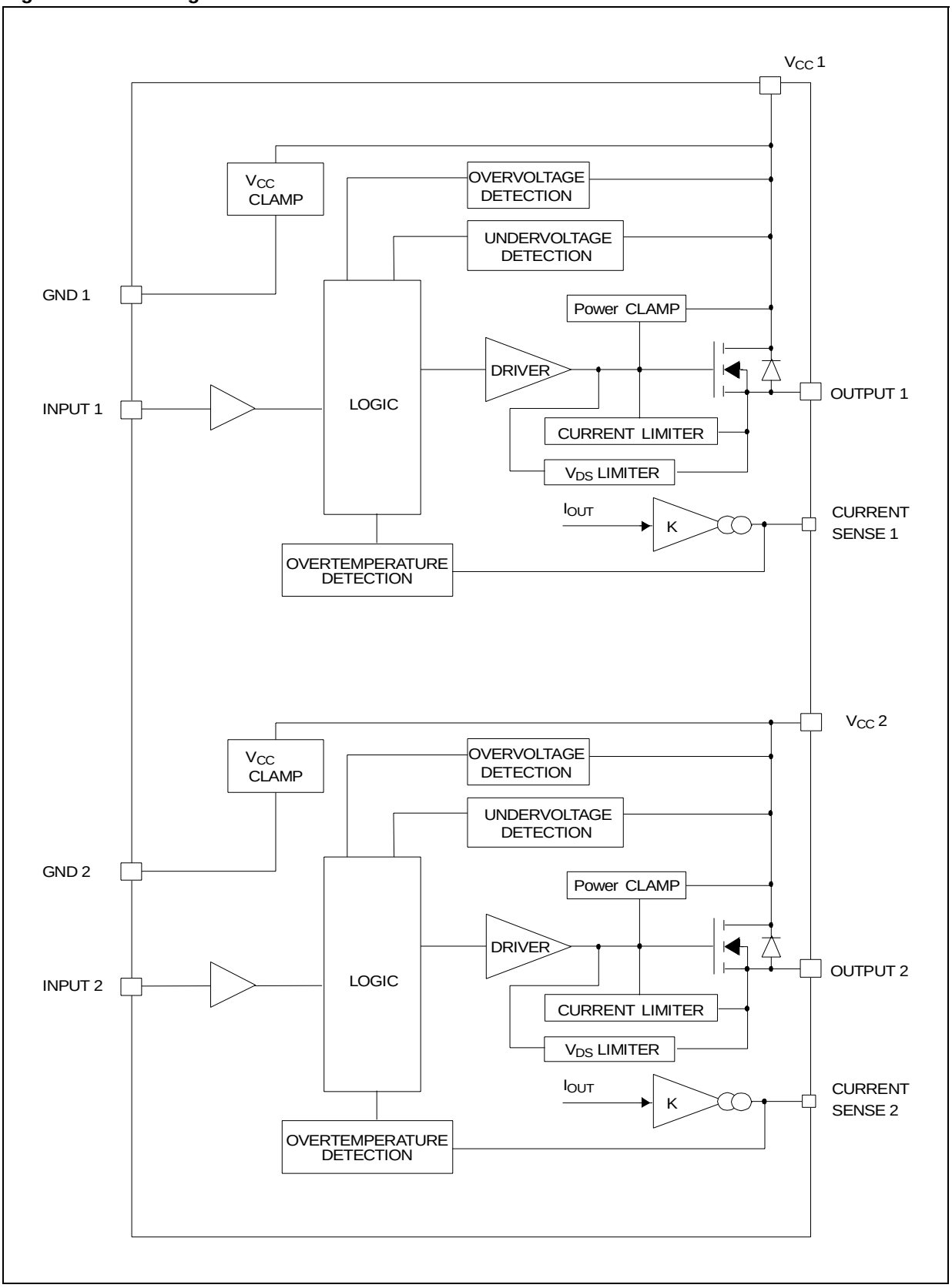
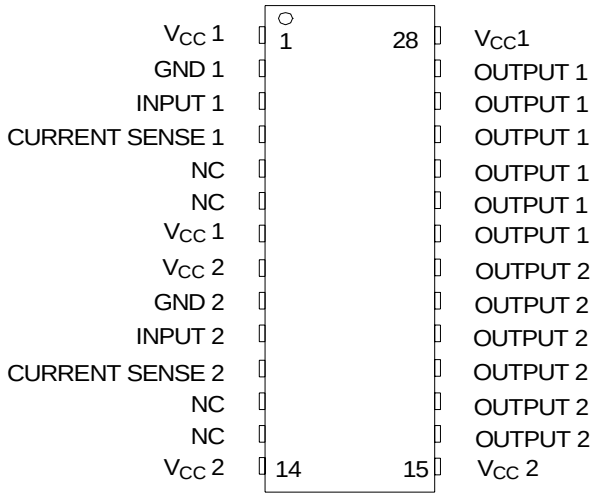


Table 3. Absolute Maximum Ratings (Per each channel)

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
- V_{CC}	Reverse DC Supply Voltage	- 0.3	V
- I_{GND}	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
- I_{OUT}	Reverse DC Output Current	- 21	A
I_{IN}	DC Input Current	+/- 10	mA
V_{CSENSE}	Current Sense Maximum Voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - OUTPUT - V_{CC}	 4000 2000 5000 5000	 V V V V
E_{MAX}	Maximum Switching Energy (L=0.25mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=45A)	355	mJ
P_{tot}	Power Dissipation T_l≤25°C	6.25 (See note 1)	W
T_j	Junction Operating Temperature	Internally limited	°C
T_c	Case Operating Temperature	- 40 to 150	°C
T_{STG}	Storage Temperature	- 55 to 150	°C

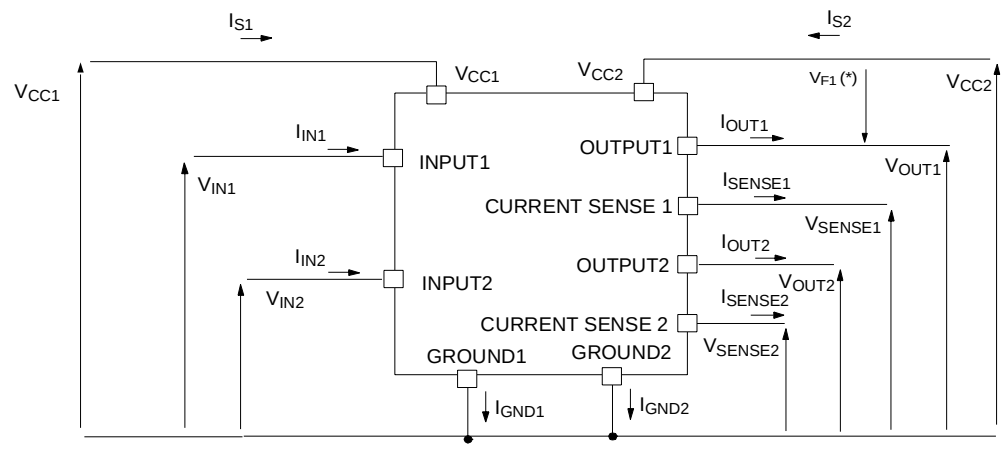
Note: 1. Per island

Table 4. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins



Connection / Pin	Current Sense	N.C.	Output	Input
Floating		X	X	X
To Ground	Through 1KΩ resistor	X		Through 10KΩ resistor

Figure 3. Current and Voltage Conventions



(*) $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

Table 5. Thermal Data

Symbol	Parameter	Value		Unit
$R_{thj\text{-}lead}$	Thermal Resistance Junction-lead	20		°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (one chip ON)	60 (1)	45 (2)	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient (two chips ON)	46 (1)	32 (2)	°C/W

Note: (1) When mounted on a standard single-sided FR-4 board with 1cm^2 of Cu (at least 35µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

Note: (2) When mounted on a standard single-sided FR-4 board with 6cm^2 of Cu (at least 35µm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)

(Per island)

Table 6. Power

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating Supply Voltage		5.5	13	36	V
V_{USD}	Undervoltage Shut-down		3	4	5.5	V
V_{OV}	Overvoltage Shut-down		36			V
R_{ON}	On State Resistance	I_{OUT}=10A; T_j =25°C I_{OUT}=10A I_{OUT}=3A; V_{CC}=6V			15 30 50	mΩ mΩ mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20mA (See note 2)	41	48	55	V
I_S	Supply Current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V Off State; V_{CC}=13V; T_j=25°C; V_{IN}=V_{OUT}=0V On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0; R_{SENSE}=3.9KΩ		10 10	25 20 5	µA µA mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =25°C			3	µA

Note: 2. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

ELECTRICAL CHARACTERISTICS (continued)

Table 7. Switching (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	R_L=1.3Ω (see figure 2)		50		µs
$t_{d(off)}$	Turn-off Delay Time	R_L=1.3Ω (see figure 2)		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	R_L=1.3Ω (see figure 2)		See relative diagram		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	R_L=1.3Ω (see figure 2)		See relative diagram		V/µs

Table 8. Logic Input

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	V_{IN}=1.25V	1			µA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V

Table 9. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward on Voltage	$-I_{OUT}$=5A; T_j=150°C			0.6	V

Table 10. Protections (see note 3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
I_{lim}	DC Short Circuit Current	V_{CC}=13V 5V<V_{CC}<36V	30	45	75 75	A A
V_{demag}	Turn-off Output Clamp Voltage	I_{OUT}=2A; V_{IN}=0V; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output Voltage Drop Limitation	I_{OUT}=1A; T_j=-40°C....+150°C		50		mV

Note: 3. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

ELECTRICAL CHARACTERISTICS (continued)

Table 11. Current Sense ($9V \le V_{CC} \le 16V$) (See Fig. 4)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=1A; V_{SENSE}=0.5V; T_j= -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT}=1A; V_{SENSE}=0.5V; T_j= -40°C...+150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=10A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT}=10A; V_{SENSE}=4V; T_j=-40°C...+150°C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=30A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT}=30A; V_{SENSE}=4V; T_j=-40°C...+150°C	-6		+6	%
I_{SENSEO}	Analog Sense Leakage Current	V_{CC}=6...16V; I_{OUT}=0A;V_{SENSE}=0V; T_j=-40°C...+150°C	0		10	µA
V_{SENSE}	Max Analog Sense Output Voltage	V_{CC}=5.5V; I_{OUT}=5A; R_{SENSE}=10KΩ V_{CC}>8V; I_{OUT}=10A; R_{SENSE}=10KΩ	2 4			V V
V_{SENSEH}	Sense Voltage in Overtemperature conditions	V_{CC}=13V; R_{SENSE}=3.9KΩ		5.5		V
$R_{VSENSEH}$	Analog Sense Output Impedance in Overtemperature Condition	V_{CC}=13V; T_j>T_{TSD}; All channels open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 4)			500	µs

Note: 4. Current sense signal delay after positive input slope

Figure 4. I_{OUT}/I_{SENSE} **Vs.** I_{OUT}

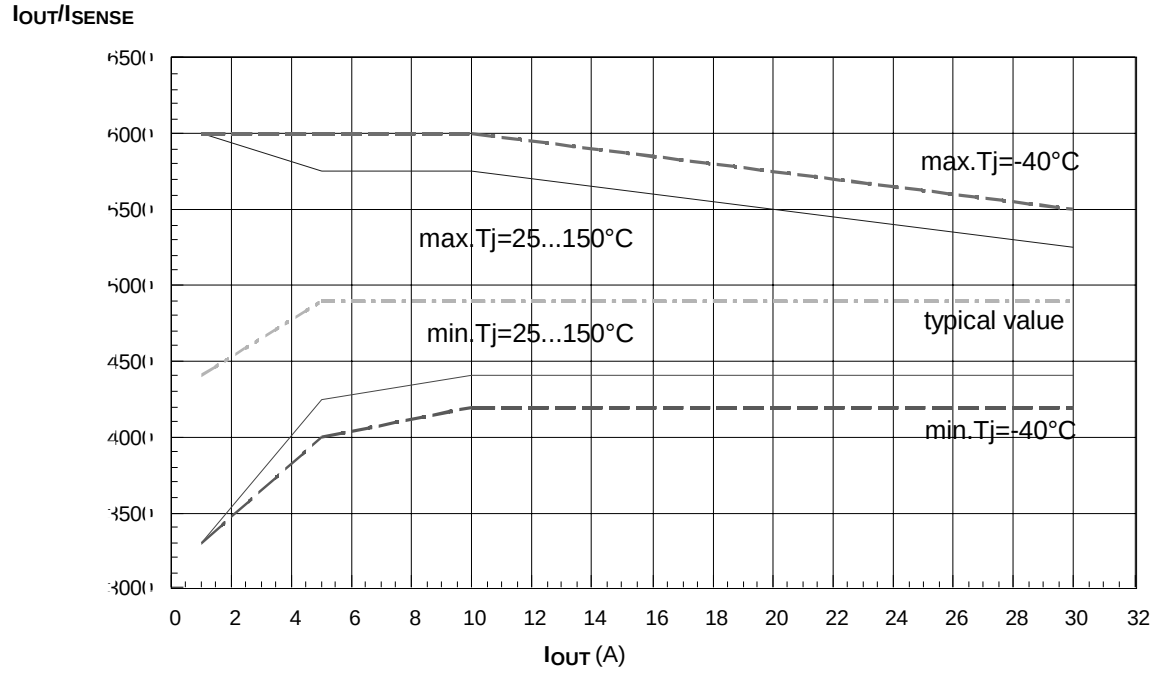


Figure 5. Switching Characteristics (Resistive load R_L=1.3Ω)

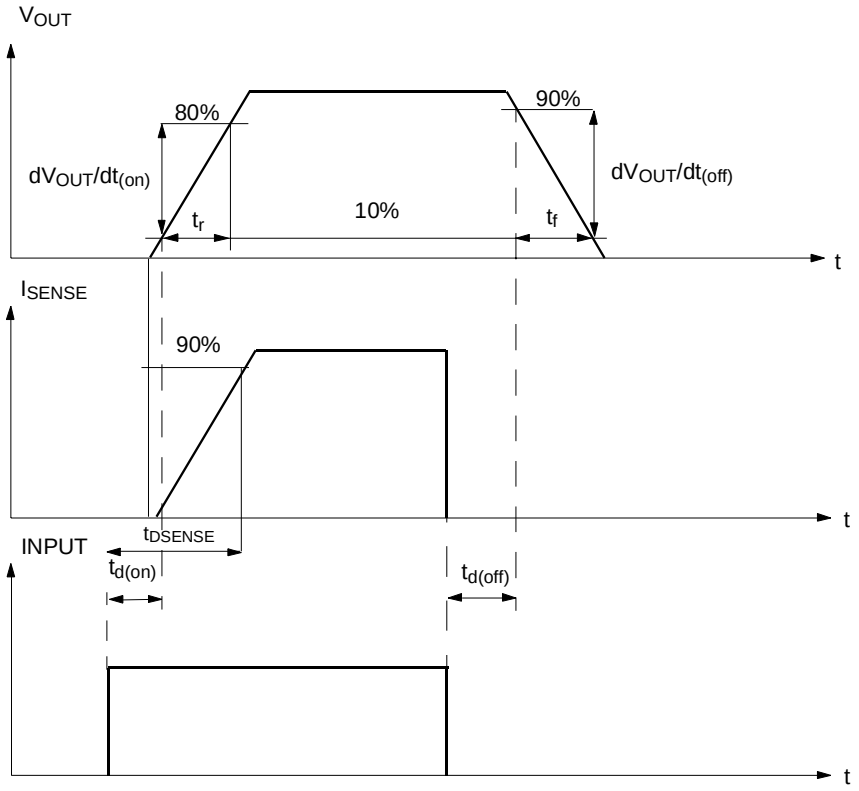


Table 12. Truth Table (per each channel)

CONDITIONS	INPUT	OUTPUT	CURRENT SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 13. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms

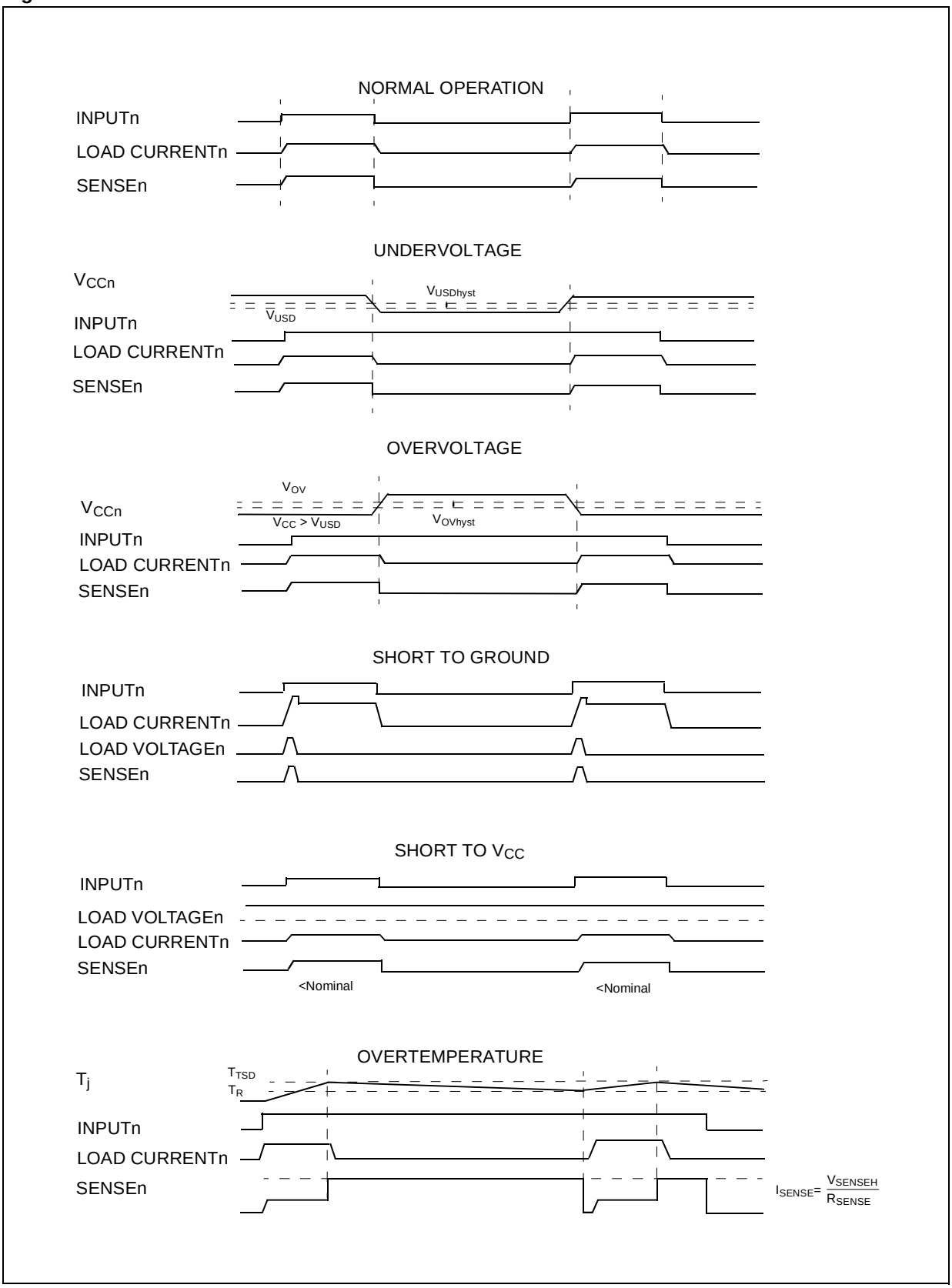
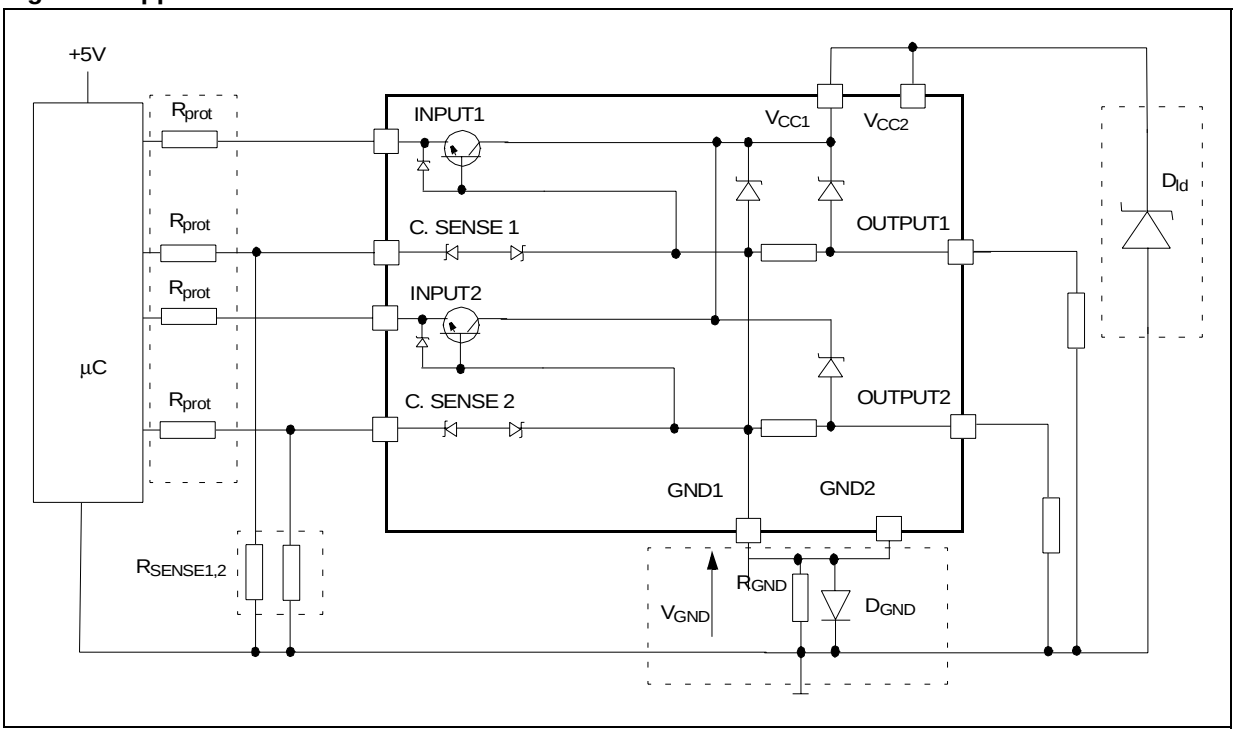


Figure 7. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.
2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D = (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$5k\Omega \leq R_{prot} \leq 65k\Omega$.

Recommended R_{prot} value is 10kΩ.

Figure 8. Off State Output Current

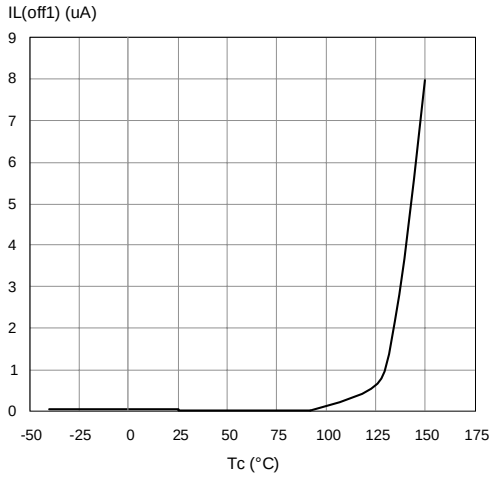


Figure 9. High Level Input Current

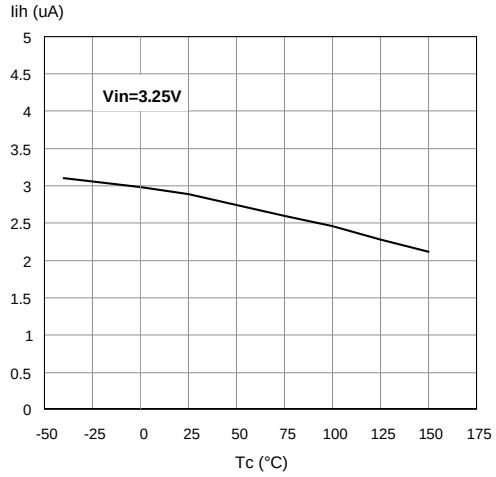


Figure 10. Input Clamp Voltage

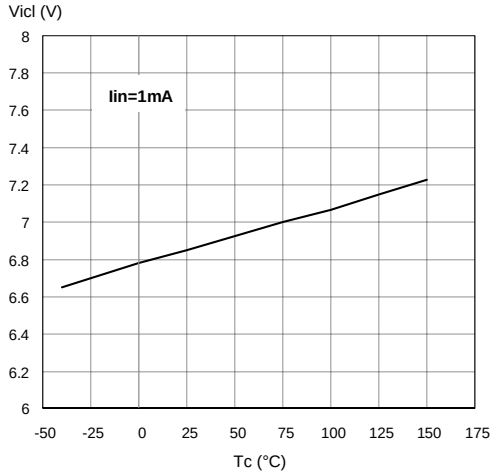


Figure 12. On State Resistance Vs V_{CC}

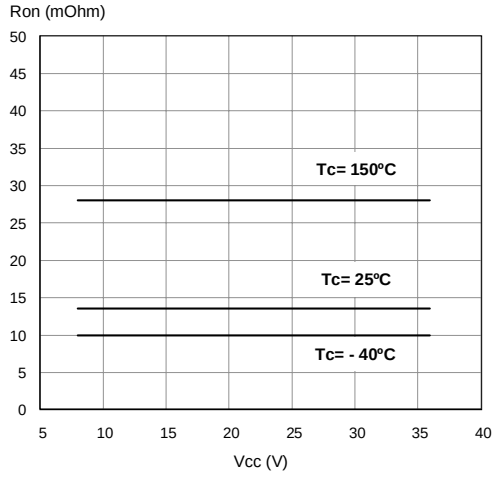


Figure 11. On State Resistance Vs T_{case}

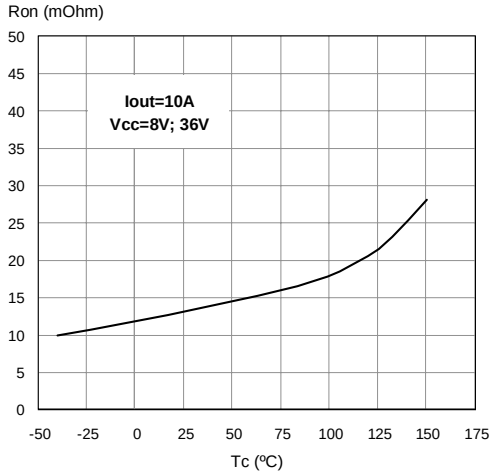


Figure 13. Input High Level

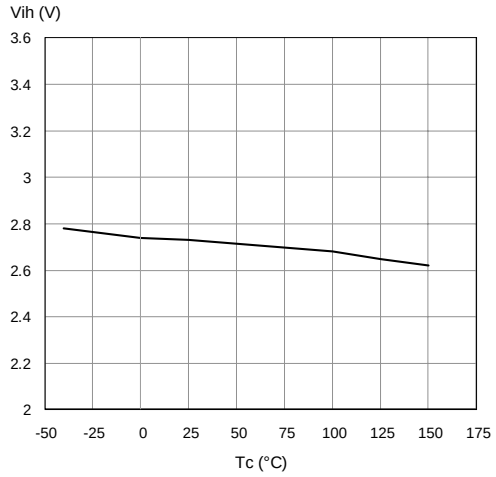


Figure 14. Input Low Level

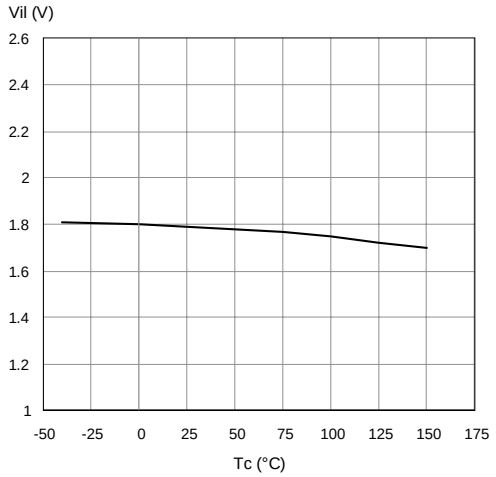


Figure 15. Turn-on Voltage Slope

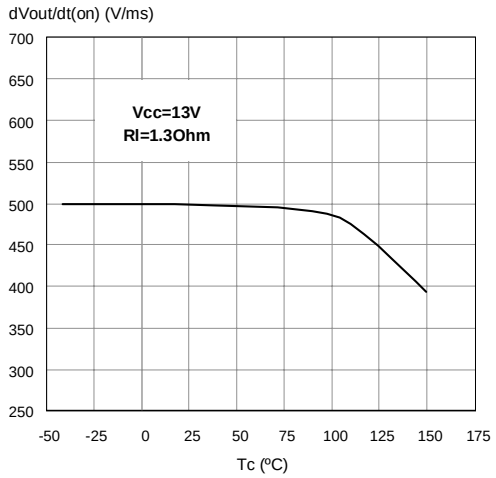


Figure 16. Overvoltage Shutdown

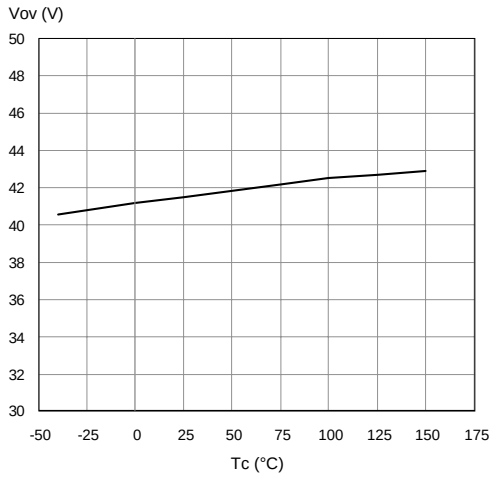


Figure 17. Input Hysteresis Voltage

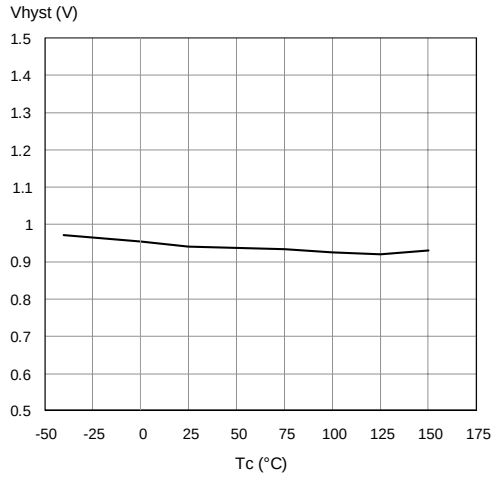


Figure 18. Turn-off Voltage Slope

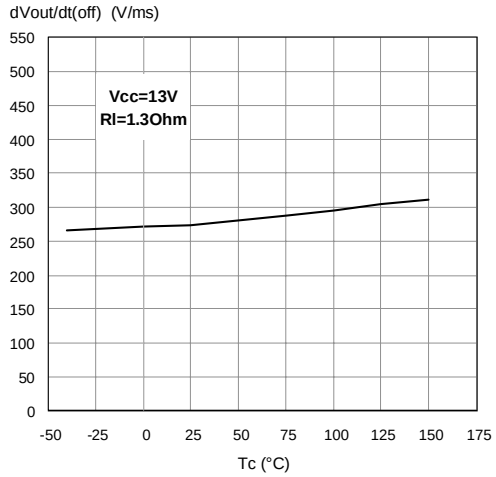


Figure 19. I_{LIM} Vs T_{case}

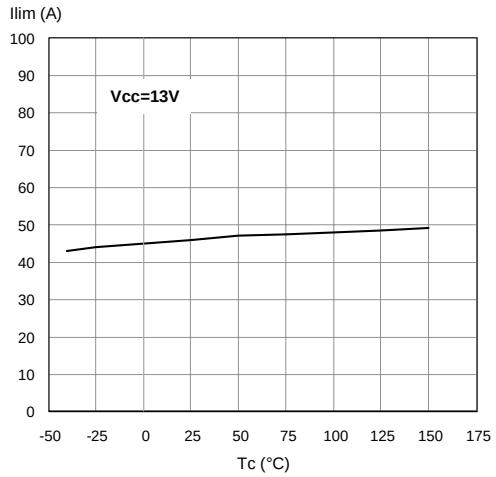
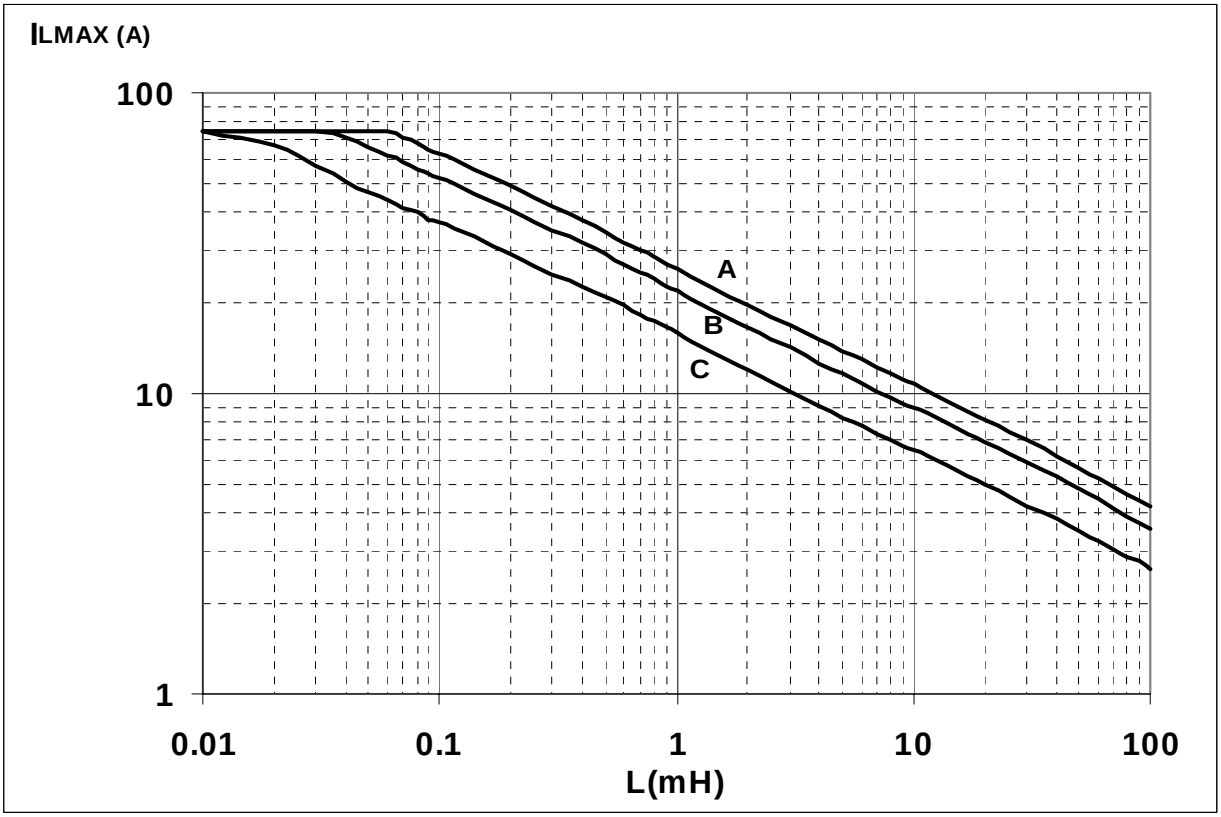


Figure 20. Maximum turn off current versus load inductance



A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

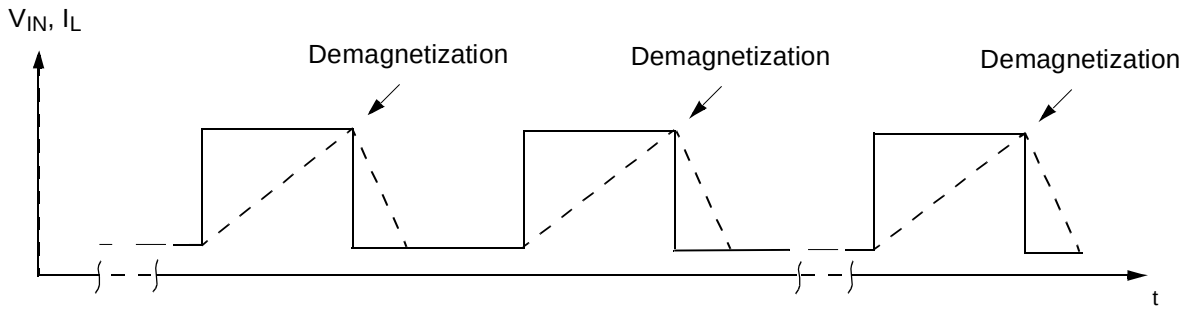
C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

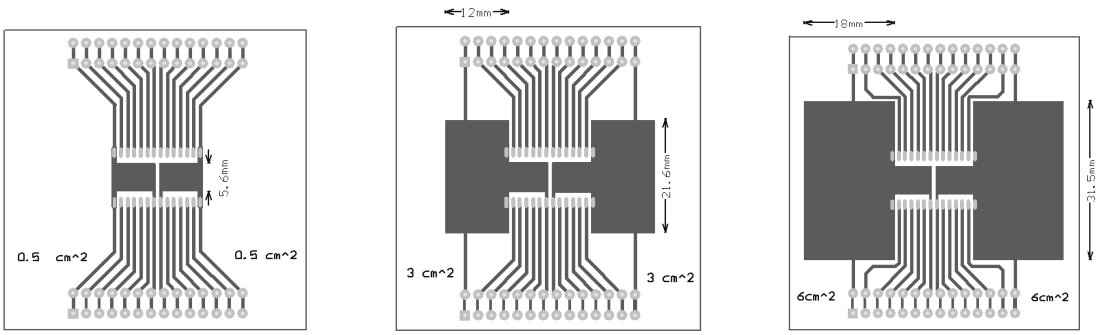
Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



SO-28 Double Island Thermal Data

Figure 21. Double Island PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: 0.5cm^2, 3cm^2, 6cm^2).

Table 14. Thermal Calculation According To The Pcb Heatsink Area

Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	R_{thA} x P_{dchip1} + T_{amb}	R_{thC} x P_{dchip1} + T_{amb}	
OFF	ON	R_{thC} x P_{dchip2} + T_{amb}	R_{thA} x P_{dchip2} + T_{amb}	
ON	ON	R_{thB} x (P_{dchip1} + P_{dchip2}) + T_{amb}	R_{thB} x (P_{dchip1} + P_{dchip2}) + T_{amb}	P_{dchip1}=P_{dchip2}
ON	ON	(R_{thA} x P_{dchip1}) + R_{thC} x P_{dchip2} + T_{amb}	(R_{thA} x P_{dchip2}) + R_{thC} x P_{dchip1} + T_{amb}	P_{dchip1}≠P_{dchip2}

R_{thA} = Thermal resistance Junction to Ambient with one chip ON

R_{thB} = Thermal resistance Junction to Ambient with both chips ON and P_{dchip1}=P_{dchip2}

R_{thC} = Mutual thermal resistance

Figure 22. $R_{thj-amb}$ Vs. PCB Copper Area In Open Box Free Air Condition

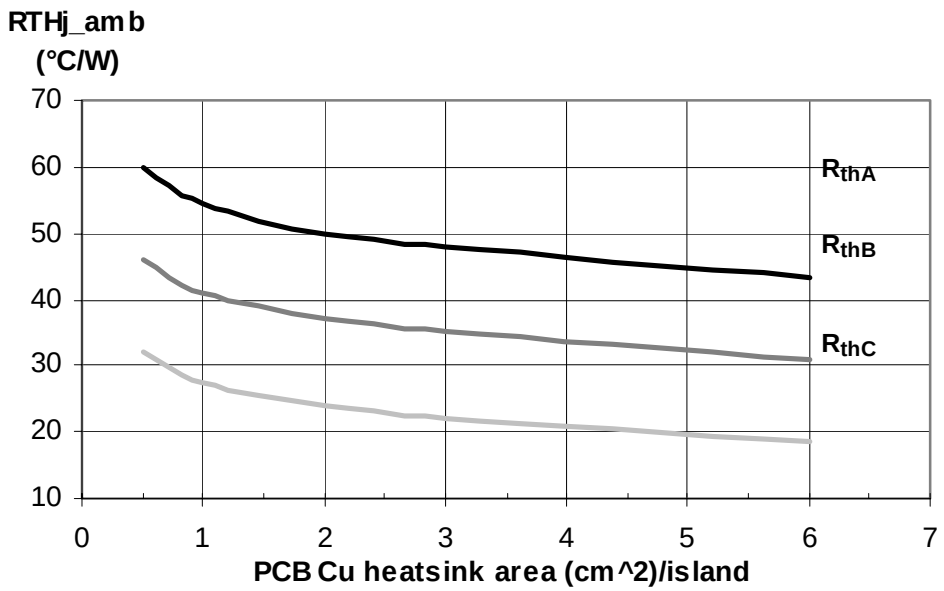


Figure 23. SO-28 Thermal Impedance Junction Ambient Single Pulse

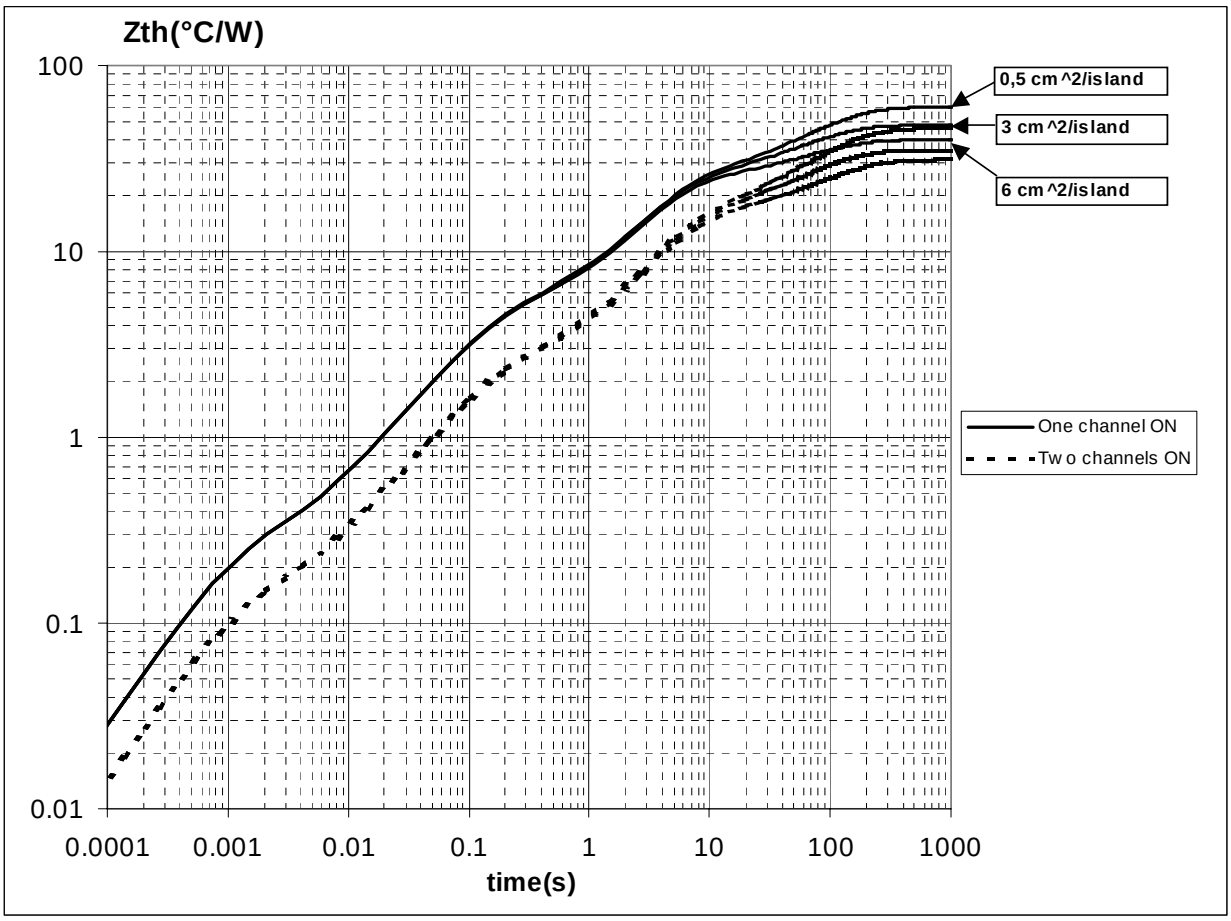
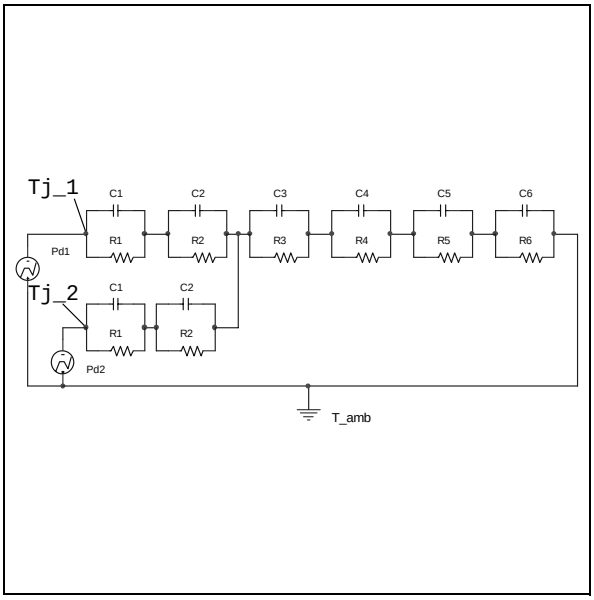


Figure 24. Thermal fitting model of a two channels HSD in SO-28



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Table 15. Thermal Parameter

Area/island (cm^2)	0.5	6
R1= (°C/W)	0.02	
R2= (°C/W)	0.1	
R3= (°C/W)	2.2	
R4= (°C/W)	11	
R5= (°C/W)	15	
R6= (°C/W)	30	13
C1= (W.s/°C)	0.0015	
C2= (W.s/°C)	7.00E-03	
C3= (W.s/°C)	1.50E-02	
C4= (W.s/°C)	0.2	
C5= (W.s/°C)	1.5	
C6= (W.s/°C)	5	8

PACKAGE MECHANICAL

Table 16. SO-28 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A			2.65
a1	0.10		0.30
b	0.35		0.49
b1	0.23		0.32
C		0.50	
c1	45° (typ.)		
D	17.7		18.1
E	10.00		10.65
e		1.27	
e3		16.51	
F	7.40		7.60
L	0.40		1.27
S	8° (max.)		

Figure 25. SO-28 Package Dimensions

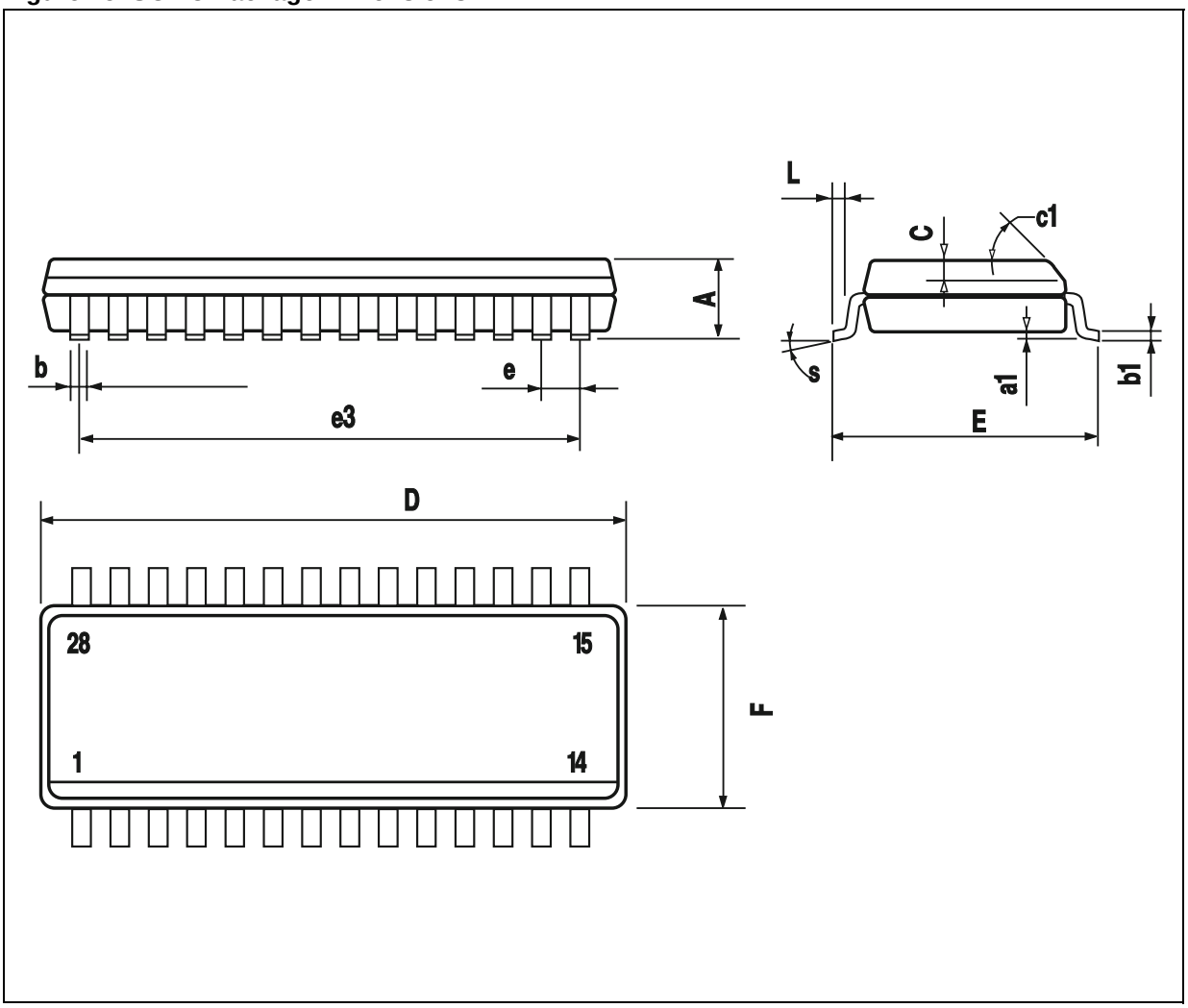
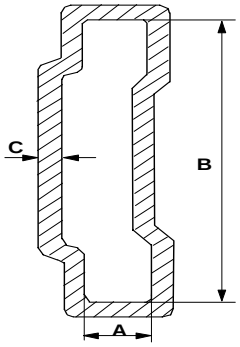


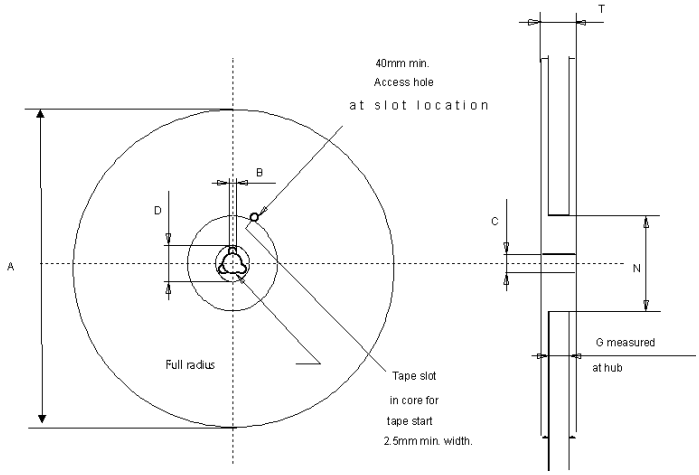
Figure 26. SO-28 Tube Shipment (No Suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 27. Tape And Reel Shipment (Suffix "TR")



REEL DIMENSIONS

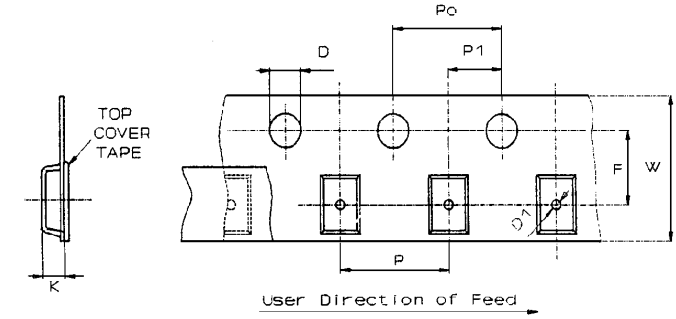
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

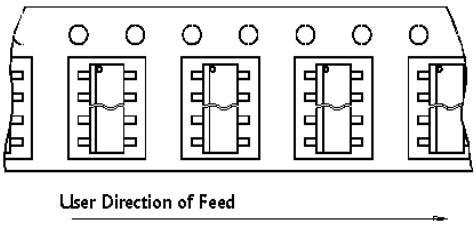
TAPE DIMENSIONS

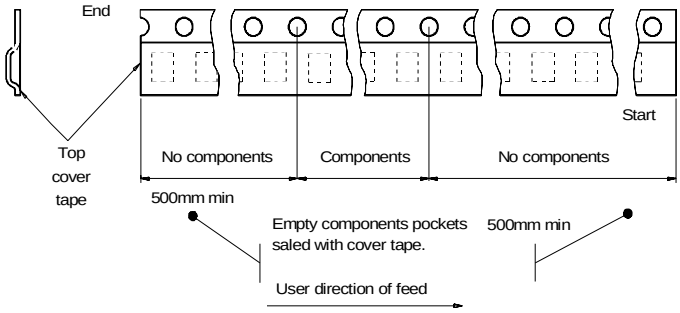
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







REVISION HISTORY

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.

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