

# ADC1005

## 10-Bit $\mu$ P Compatible A/D Converter

### General Description

The ADC1005 is a CMOS 10-bit successive approximation A/D converter. The 20-pin ADC1005 outputs 10-bit data in a two-byte format for interface with 8-bit microprocessors.

The ADC1005 has differential inputs to permit rejection of common-mode signals, allow the analog input range to be offset, and also to permit the conversion of signals not referred to ground. In addition, the reference voltage can be adjusted, allowing smaller voltage spans to be measured with 10-bit resolution.

### Features

- Easy interface to all microprocessors
- Differential analog voltage inputs

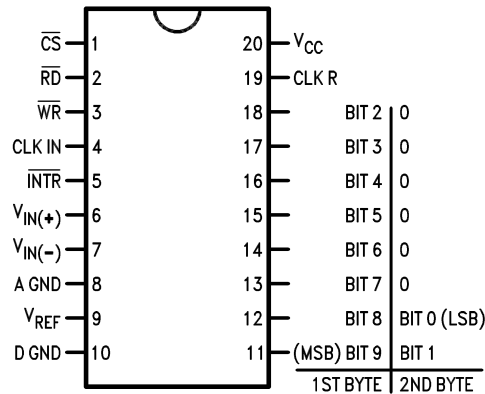
- Operates ratiometrically or with 5  $V_{DC}$  voltage reference or analog span adjusted voltage reference
- 0V to 5V analog input voltage range with single 5V supply
- On-chip clock generator
- TLL/MOS input/output compatible
- 0.3" standard width 20-pin DIP

### Key Specifications

- Resolution 10 bits
- Linearity Error  $\pm 1/2$  LSB and  $\pm 1$  LSB
- Conversion Time 50  $\mu$ s

### Connection Diagram

ADC 1005 (for an 8-bit data bus)  
Dual-In-Line Package



Top View

00526101

### Ordering Information

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005BCJ-1	J20A	0°C to +70°C	$\pm 1/2$ LSB
ADC1005BCJ	J20A	-40°C to +85°C	
ADC1005CCJ-1	J20A	0°C to +70°C	$\pm 1$ LSB

**Absolute Maximum Ratings** (Notes 1,

2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	6.5V
Logic Control Inputs	-0.3V to +15V
Voltage at Other Inputs and Outputs	-0.3V to $V_{CC}$ +0.3V
Input Current Per Pin	±5 mA
Input Current Per Package	±20 mA
Storage Temperature Range	-65°C to +150°C

Package Dissipation at $T_A=25^\circ\text{C}$	875 mW
Lead Temperature (Soldering, 10 seconds)	
Dual-In-Line Package (Ceramic)	300°C
ESD Susceptibility (Note 8)	800V

**Operating Ratings** (Notes 1, 2)

Supply Voltage ( $V_{CC}$ )	4.5V to 6.0V
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$ -40°C ≤ $T_A$ ≤ +85°C
ADC1005BCJ	
ADC1005BCJ-1, ADC1005CCJ-1	

**Electrical Characteristics**

The following specifications apply for  $V_{CC} = 5V$ ,  $V_{REF} = 5V$ ,  $f_{CLK} = 1.8$  MHz unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; All other limits  $T_A = T_j = 25^\circ\text{C}$ .

Parameter	Conditions	ADC1005BCJ			ADC1005BCJ-1, ADC1005CCJ-1			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
<b>Converter Characteristics</b>								
Linearity Error (Note 3)			<b>±0.5</b>					
ADC1005BCJ								LSB
ADC1005BCJ-1						±0.5	<b>±0.5</b>	LSB
ADC1005CCJ-1						±1	<b>±1</b>	LSB
Zero Error			<b>±0.5</b>					
ADC1005BCJ								LSB
ADC1005BCJ-1						±0.5	<b>±0.5</b>	LSB
ADC1005CCJ-1						±1	<b>±1</b>	LSB
Fullscale Error			<b>±0.5</b>					
ADC1005BCJ								LSB
ADC1005BCJ-1						±0.5	<b>±0.5</b>	LSB
ADC1005CCJ-1						±1	<b>±1</b>	LSB
Reference Input Resistance	MIN	4.8	<b>2.2</b>		4.8	2.4	<b>2.2</b>	kΩ
	MAX	4.8	<b>8.3</b>		4.8	7.6	<b>8.3</b>	kΩ
Common-Mode Input (Note 4)	MIN MAX		<b><math>V_{CC}+0.05</math> <math>GND-0.05</math></b>			$V_{CC}+0.05$ $GND-0.05$	<b><math>V_{CC}+0.05</math> <math>GND-0.05</math></b>	V V
DC Common-Mode Error	Over Common-Mode Input Range	±1/8	<b>±1/4</b>		±1/8	±1/4	<b>±1/4</b>	LSB
Power Supply Sensitivity	$V_{CC}=5 V_{DC} \pm 5\%$ $V_{REF} = 4.75V$	±1/8	<b>±1/4</b>		±1/8	±1/4	<b>±1/4</b>	LSB

## Electrical Characteristics (Continued)

The following specifications apply for  $V_{CC} = 5V$ ,  $V_{REF} = 5V$ ,  $f_{CLK} = 1.8$  MHz unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; All other limits  $T_A = T_J = 25^\circ C$ .

Parameter	Conditions	ADC1005BCJ			ADC1005BCJ-1, ADC1005CCJ-1			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
<b>DC Characteristics</b>								
$V_{IN(1)}$ Logical "1" Input Voltage MIN	$V_{CC}=5.25V$ (except $CLK_{IN}$ )		<b>2.0</b>			2.0	<b>2.0</b>	V
$V_{IN(0)}$ Logical "0" Input Voltage MAX	$V_{CC}=4.75V$ (Except $CLK_{IN}$ )		<b>0.8</b>			0.8	<b>0.8</b>	V
$I_{IN}$ Logical "1" Input Current MAX	$V_{IN}=5.0V$	0.005	<b>1</b>		0.005	1	<b>1</b>	$\mu A$
$I_{IN}$ Logical "0" Input Current MAX	$V_{IN}=0V$	-0.005	<b>-1</b>		-0.005	-1	<b>-1</b>	$\mu A$
$V_{T+(MIN)}$ Minimum $CLK_{IN}$ Positive going Threshold Voltage		3.1	<b>2.7</b>		3.1	2.7	<b>2.7</b>	V
$V_{T(MAX)}$ Maximum $CLK_{IN}$ Positive going Threshold Voltage		3.1	<b>3.5</b>		3.1	3.5	<b>3.5</b>	V
$V_{T-(MIN)}$ Minimum $CLK_{IN}$ Negative going Threshold Voltage		1.8	<b>1.5</b>		1.8	1.5	<b>1.5</b>	V
$V_{T-(MAX)}$ Maximum $CLK_{IN}$ Negative going Threshold Voltage		1.8	<b>2.1</b>		1.8	2.1	<b>2.1</b>	V
$V_{H(MIN)}$ Minimum $CLK_{IN}$ Hysteresis ( $V_{T+}-V_{T-}$ )		1.3	<b>0.6</b>		1.3	0.6	<b>0.6</b>	V
$V_{H(MAX)}$ Maximum $CLK_{IN}$ Hysteresis ( $V_{T+}-V_{T-}$ )		1.3	<b>2.0</b>		1.3	2.0	<b>2.0</b>	V
$V_{OUT(1)}$ Logical "1" Output Voltage MIN	$V_{CC}=4.75V$ $I_{OUT}=-360 \mu A$ $I_{OUT}=-10 \mu A$		<b>2.4</b>			2.8	<b>2.4</b>	V
			<b>4.5</b>			4.6	<b>4.5</b>	V
$V_{OUT(0)}$ Logical "0" Output Voltage MAX	$V_{CC}=4.75V$ $I_{OUT}=1.6$ mA		<b>0.4</b>			0.34	<b>0.4</b>	V
$I_{OUT}$ TRI-STATE® Output Current MAX	$V_{OUT} = 0V$ $V_{OUT} = 5V$	-0.01	<b>-3</b>		-0.01	-0.3	<b>-3</b>	$\mu A$
		0.01	<b>3</b>		0.01	0.3	<b>3</b>	$\mu A$
$I_{SOURCE}$ Output Source Current MIN	$V_{OUT}=0V$	-14	<b>-6.5</b>		-14	-7.5	<b>-6.5</b>	mA
$I_{SINK}$ Output Sink Current MIN	$V_{OUT}=5V$	16	<b>8.0</b>		16	9.0	<b>8.0</b>	mA
$I_{CC}$ Supply Current MAX	$f_{CLK}=1.8$ MHz $CS = "1"$	1.5	<b>3</b>		1.5	2.5	<b>3</b>	mA

## AC Electrical Characteristics

The following specifications apply for  $V_{CC} = 5V$ ,  $V_{REF} = 5V$ ,  $V_{REF} = 5V$ ,  $t_r = t_f = 20$  ns unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; All other limits  $T_A = T_j = 25^\circ C$ .

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Limit Units
$f_{CLK}$ , Clock Frequency	MIN		0.2	0.2	MHz
	MAX		2.6	2.6	MHz
Clock Duty Cycle	MIN		40	40	%
	MAX		60	60	%
$t_C$ , Conversion Time	MIN		80	80	$1/f_{CLK}$
	MAX		90	90	$1/f_{CLK}$
	MIN	$f_{CLK}=1.8$ MHz	45	45	$\mu s$
	MAX	$f_{CLK}=1.8$ MHz	50	50	$\mu s$
$t_{W(WR)L}$ , Minimum $\overline{WR}$ Pulse Width	$\overline{CS} = 0$	100	150	150	ns
$t_{ACC}$ , Access Time (Delay from falling edge of $\overline{RD}$ to Output Data Valid)	$\overline{CS} = 0$ $C_L = 100$ pF, $R_L = 2k$	170	300	300	ns
$t_{1H}$ , $t_{0H}$ , TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 10k$ , $C_L = 10$ pF	125		200	ns
	$R_L = 2k$ , $C_L = 100$ pF	145	230	230	ns
$t_{WI}$ , $t_{RI}$ , Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$		300	450	450	ns
$t_{IRS}$ , $\overline{INTR}$ to 1st Read Set-up Time		400	550	550	ns
$C_{IN}$ , Capacitance of Logic Inputs		5		7.5	pF
$C_{OUT}$ , Capacitance of Logic Outputs		5		7.5	pF

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to ground.

**Note 3:** Linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line which passes through the end points of the transfer characteristic.

**Note 4:** For  $V_{IN(-)} \geq V_{IN(+)}$  the digital output code will be 00 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than  $V_{CC}$  supply. Be careful, during testing at low  $V_{CC}$  levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog  $V_{IN}$  does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0  $V_{DC}$  to 5  $V_{DC}$  input voltage range will therefore require a minimum supply voltage of 4.950  $V_{DC}$  over temperature variations, initial tolerance and loading.

**Note 5:** Typicals are at 25°C and represent most likely parametric norm.

**Note 6:** Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 7:** Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

**Note 8:** Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.