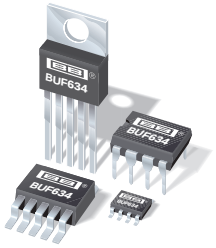
BURR - BROWN®



BUF634

250mA HIGH-SPEED BUFFER

FEATURES

- HIGH OUTPUT CURRENT: 250mA
- SLEW RATE: 2000V/µs
- PIN-SELECTED BANDWIDTH: 30MHz to 180MHz
- LOW QUIESCENT CURRENT: 1.5mA (30MHz BW)
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- INTERNAL CURRENT LIMIT
- THERMAL SHUTDOWN PROTECTION
- 8-PIN DIP, SO-8, 5-LEAD TO-220, 5-LEAD DDPAK SURFACE-MOUNT

APPLICATIONS

- VALVE DRIVER
- SOLENOID DRIVER
- OP AMP CURRENT BOOSTER
- LINE DRIVER
- HEADPHONE DRIVER
- VIDEO DRIVER
- MOTOR DRIVER
- TEST EQUIPMENT
- ATE PIN DRIVER

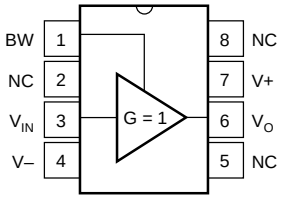
DESCRIPTION

The BUF634 is a high speed unity-gain open-loop buffer recommended for a wide range of applications. It can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback and improve capacitive load drive.

For low power applications, the BUF634 operates on 1.5mA quiescent current with 250mA output, 2000V/µs slew rate and 30MHz bandwidth. Bandwidth can be adjusted from 30MHz to 180MHz by connecting a resistor between V– and the BW Pin.

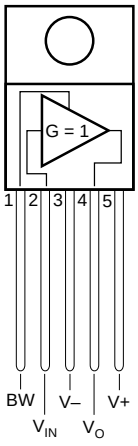
Output circuitry is fully protected by internal current limit and thermal shut-down making it rugged and easy to use.

8-Pin DIP Package
SO-8 Surface-Mount Package

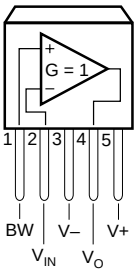


The BUF634 is available in a variety of packages to suit mechanical and power dissipation requirements. Types include 8-pin DIP, SO-8 surface-mount, 5-lead TO-220, and a 5-lead DDPAK surface-mount plastic power package.

5-Lead TO-220



5-Lead DDPAK Surface Mount



NOTE: Tabs are connected to V– supply.

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
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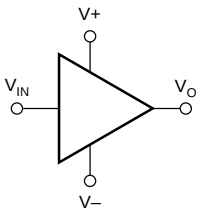
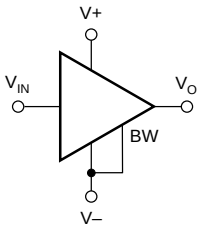
SBOS030

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C[1], V_S = ±15V, unless otherwise noted.

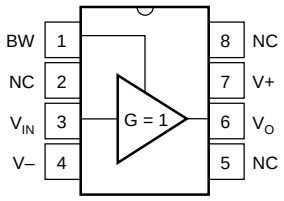
PARAMETER	CONDITION	BUF634P, U, T, F						UNITS
		LOW QUIESCENT CURRENT MODE			WIDE BANDWIDTH MODE			
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage			±30	±100		*	*	mV
vs Temperature	Specified Temperature Range		±100			*		µV/°C
vs Power Supply	V_S = ±2.25V[2] to ±18V		0.1	1		*	*	mV/V
Input Bias Current	V_{IN} = 0V		±0.5	±2		±5	±20	µA
Input Impedance	R_L = 100Ω		80 || 8			8 || 8		MΩ || pF
Noise Voltage	f = 10kHz		4			*		nV/√Hz
GAIN	R_L = 1kΩ, V_O = ±10V	0.95	0.99		*	*		V/V
	R_L = 100Ω, V_O = ±10V	0.85	0.93		*	*		V/V
	R_L = 67Ω, V_O = ±10V	0.8	0.9		*	*		V/V
OUTPUT								
Current Output, Continuous			±250			*		mA
Voltage Output, Positive	I_O = 10mA	(V+) –2.1	(V+) –1.7		*	*		V
Negative	I_O = –10mA	(V–) +2.1	(V–) +1.8		*	*		V
Positive	I_O = 100mA	(V+) –3	(V+) –2.4		*	*		V
Negative	I_O = –100mA	(V–) +4	(V–) +3.5		*	*		V
Positive	I_O = 150mA	(V+) –4	(V+) –2.8		*	*		V
Negative	I_O = –150mA	(V–) +5	(V–) +4		*	*		V
Short-Circuit Current			±350	±550		±400	*	mA
DYNAMIC RESPONSE								
Bandwidth, –3dB	R_L = 1kΩ		30			180		MHz
	R_L = 100Ω		20			160		MHz
Slew Rate	20Vp-p, R_L = 100Ω		2000			*		V/µs
Settling Time, 0.1%	20V Step, R_L = 100Ω		200			*		ns
1%	20V Step, R_L = 100Ω		50			*		ns
Differential Gain	3.58MHz, V_O = 0.7V, R_L = 150Ω		4			0.4		%
Differential Phase	3.58MHz, V_O = 0.7V, R_L = 150Ω		2.5			0.1		°
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±2.25[2]		±18	*		*	V
Quiescent Current, I_Q	I_O = 0		±1.5	±2		±15	±20	mA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operating		–40		+125	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Shutdown Temperature, T_J			175			*		°C
Thermal Resistance, θ_{JA}	"P" Package[3]		100			*		°C/W
θ_{JA}	"U" Package[3]		150			*		°C/W
θ_{JA}	"T" Package[3]		65			*		°C/W
θ_{JC}	"T" Package		6			*		°C/W
θ_{JA}	"F" Package[3]		65			*		°C/W
θ_{JC}	"F" Package		6			*		°C/W
								

* Specifications the same as Low Quiescent Mode.

NOTES: (1) Tests are performed on high speed automatic test equipment, at approximately 25°C junction temperature. The power dissipation of this product will cause some parameters to shift when warmed up. See typical performance curves for over-temperature performance. (2) Limited output swing available at low supply voltage. See Output voltage specifications. (3) Typical when all leads are soldered to a circuit board. See text for recommendations.

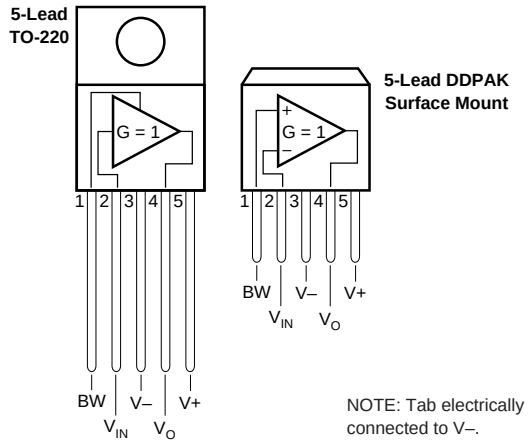
PIN CONFIGURATION

Top View **8-Pin Dip Package**
SO-8 Surface-Mount Package



NC = No Connection

Top View



NOTE: Tab electrically connected to V–.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering,10s)	+300°C

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
BUF634P	8-Pin Plastic DIP	006	–40°C to +85°C
BUF634U	SO-8 Surface-Mount	182	–40°C to +85°C
BUF634T	5-Lead TO-220	315	–40°C to +85°C
BUF634F	5-Lead DDPAK	325	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

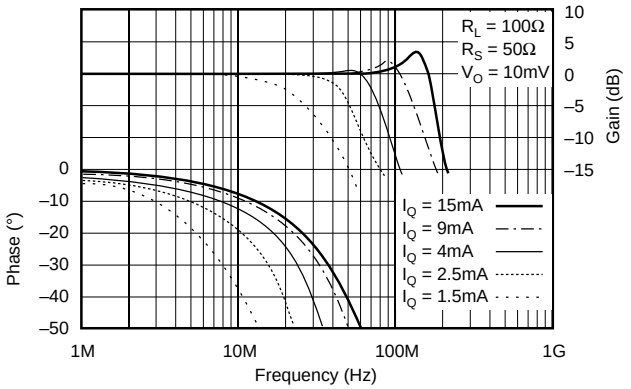
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

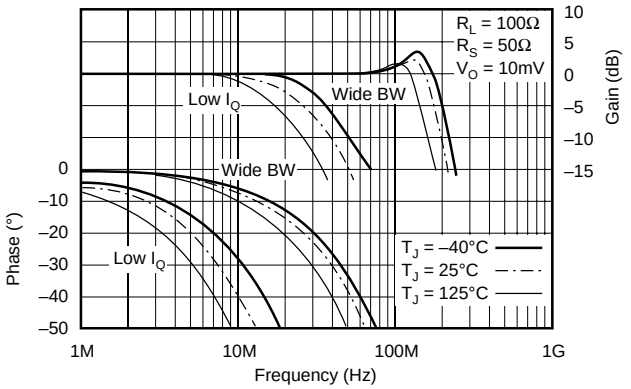
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

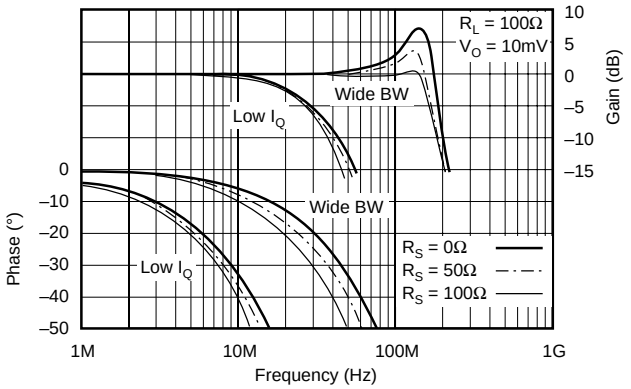
GAIN and PHASE vs FREQUENCY
vs QUIESCENT CURRENT



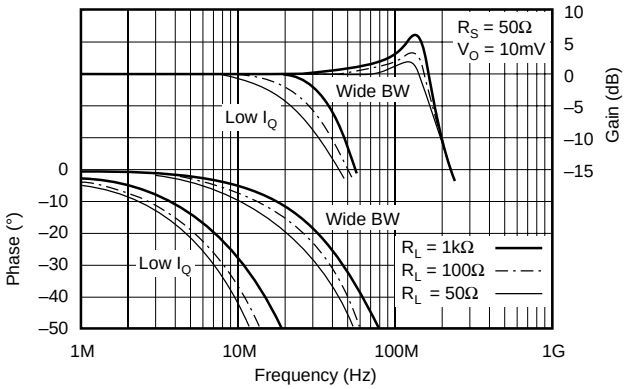
GAIN and PHASE vs FREQUENCY
vs TEMPERATURE



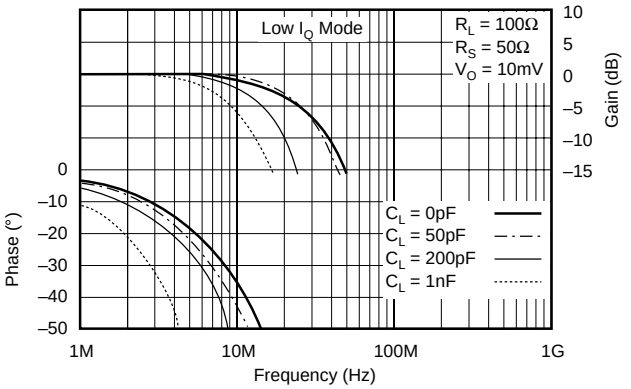
GAIN and PHASE vs FREQUENCY
vs SOURCE RESISTANCE



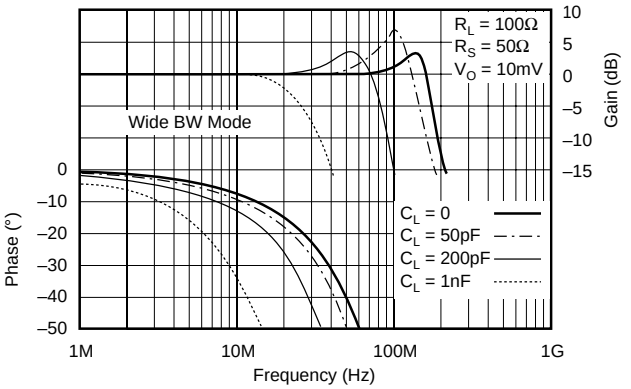
GAIN and PHASE vs FREQUENCY
vs LOAD RESISTANCE



GAIN and PHASE vs FREQUENCY
vs LOAD CAPACITANCE



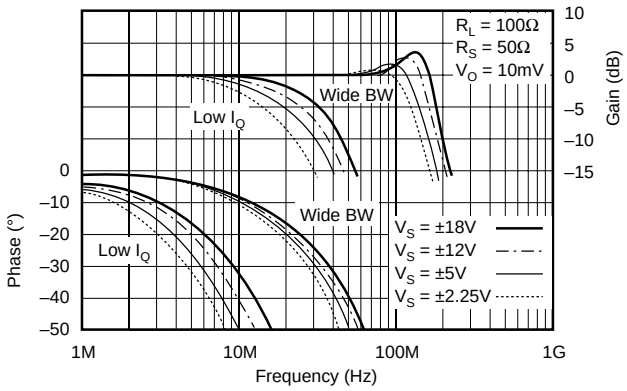
GAIN and PHASE vs FREQUENCY
vs LOAD CAPACITANCE



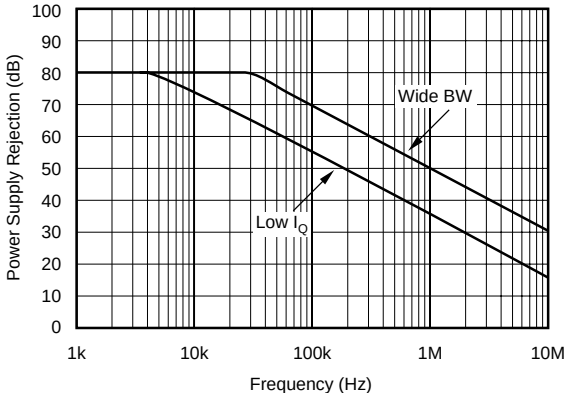
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

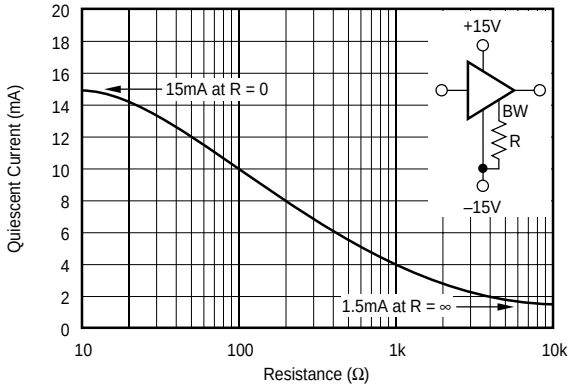
GAIN and PHASE vs FREQUENCY
vs POWER SUPPLY VOLTAGE



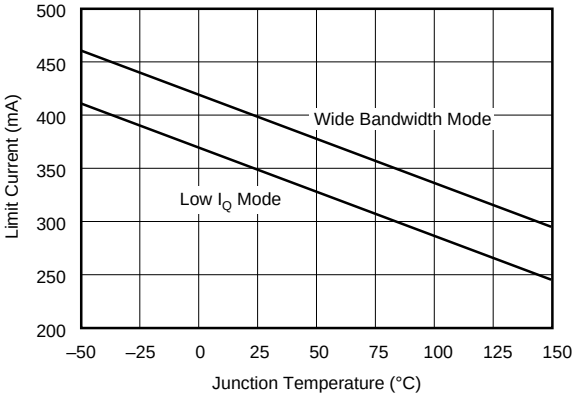
POWER SUPPLY REJECTION vs FREQUENCY



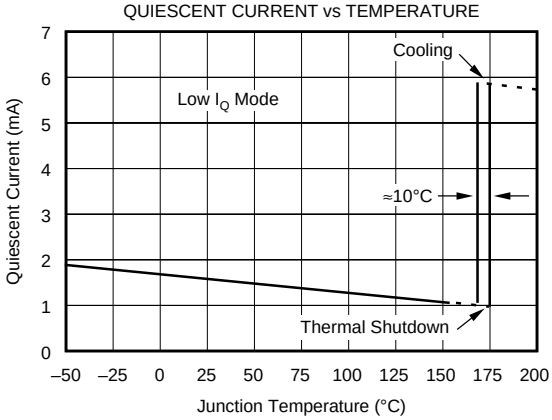
QUIESCENT CURRENT
vs BANDWIDTH CONTROL RESISTANCE



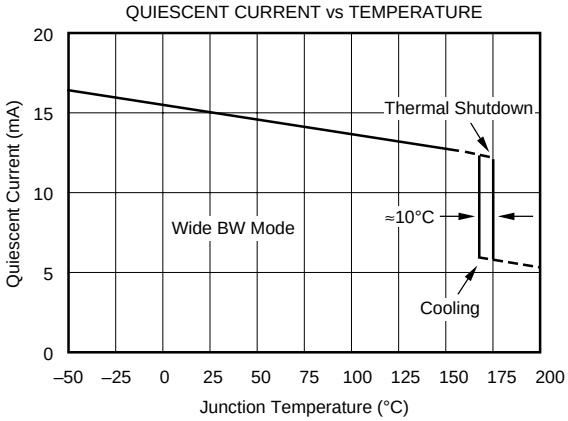
SHORT CIRCUIT CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



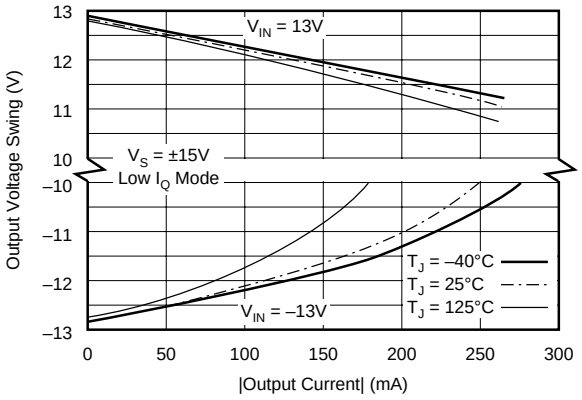
QUIESCENT CURRENT vs TEMPERATURE



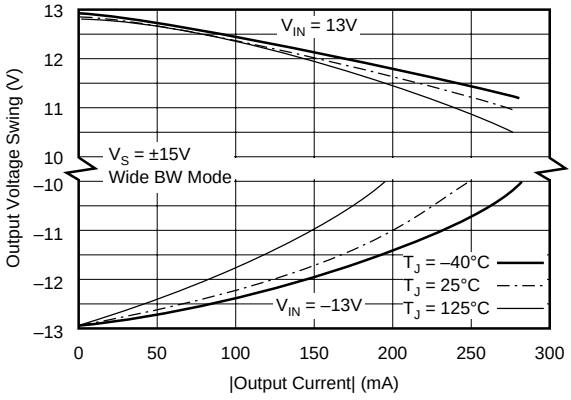
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

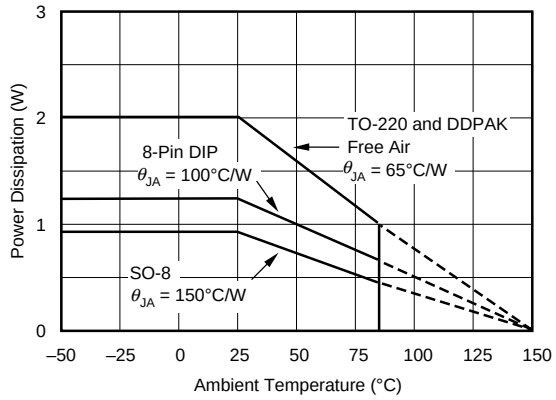
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



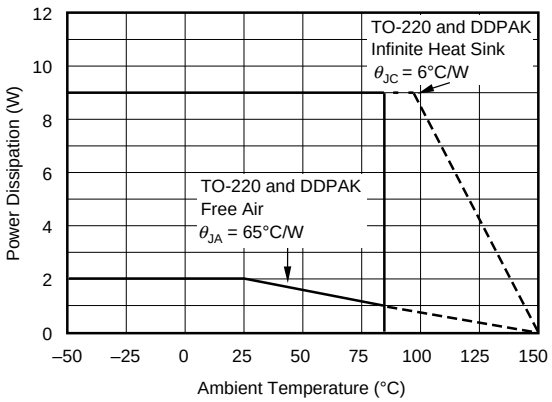
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



MAXIMUM POWER DISSIPATION vs TEMPERATURE

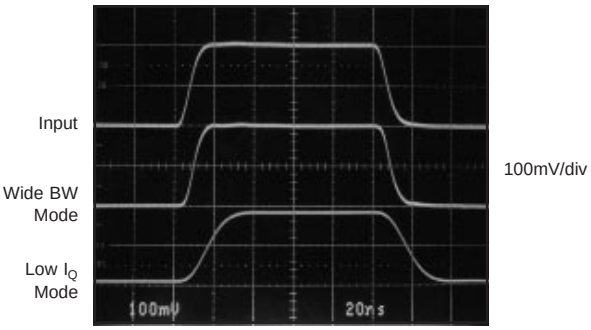


MAXIMUM POWER DISSIPATION vs TEMPERATURE



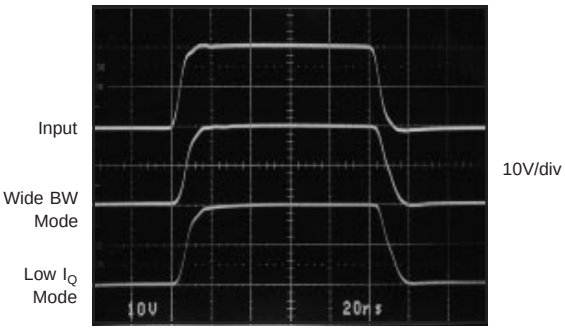
SMALL-SIGNAL RESPONSE

R_S = 50Ω, R_L = 100Ω



LARGE-SIGNAL RESPONSE

R_S = 50Ω, R_L = 100Ω



APPLICATION INFORMATION

Figure 1 is a simplified circuit diagram of the BUF634 showing its open-loop complementary follower design.

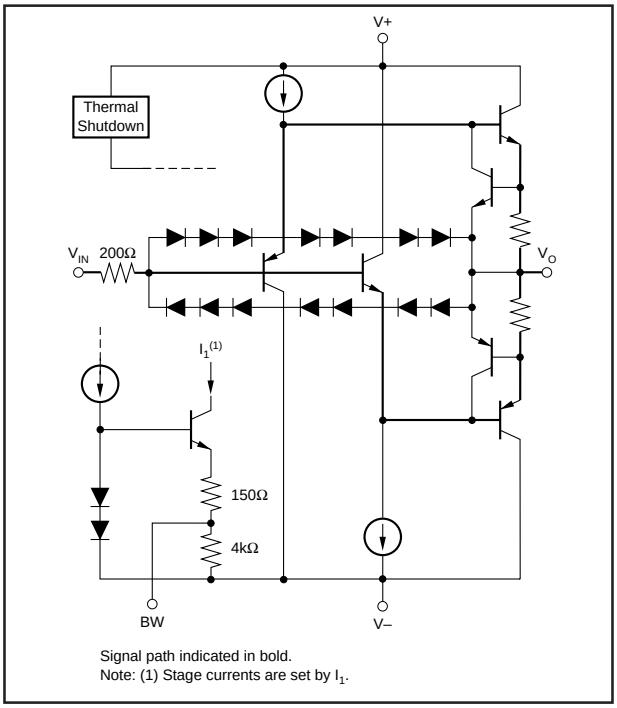


FIGURE 1. Simplified Circuit Diagram.

Figure 2 shows the BUF634 connected as an open-loop buffer. The source impedance and optional input resistor, R_S, influence frequency response—see typical curves. Power supplies should be bypassed with capacitors connected close to the device pins. Capacitor values as low as 0.1µF will assure stable operation in most applications, but high output current and fast output slewing can demand large current transients from the power supplies. Solid tantalum 10µF capacitors are recommended.

High frequency open-loop applications may benefit from special bypassing and layout considerations—see "High Frequency Applications" at end of applications discussion.

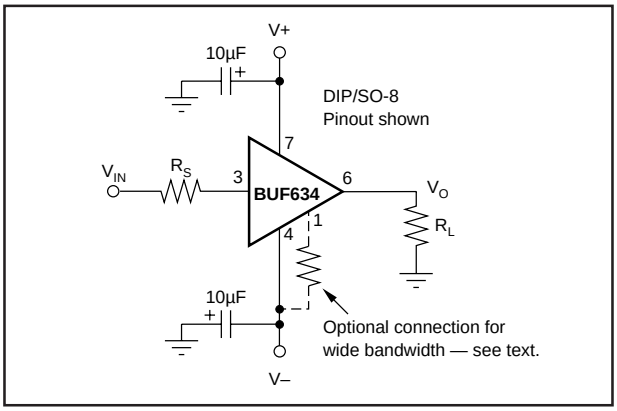


FIGURE 2. Buffer Connections.

OUTPUT CURRENT

The BUF634 can deliver up to ±250mA continuous output current. Internal circuitry limits output current to approximately ±350mA—see typical performance curve "Short Circuit Current vs Temperature". For many applications, however, the continuous output current will be limited by thermal effects.

The output voltage swing capability varies with junction temperature and output current—see typical curves "Output Voltage Swing vs Output Current." Although all four package types are tested for the same output performance using a high speed test, the higher junction temperatures with the DIP and SO-8 package types will often provide less output voltage swing. Junction temperature is reduced in the DDPAK surface-mount power package because it is soldered directly to the circuit board. The TO-220 package used with a good heat sink further reduces junction temperature, allowing maximum possible output swing.

THERMAL PROTECTION

Power dissipated in the BUF634 will cause the junction temperature to rise. A thermal protection circuit in the BUF634 will disable the output when the junction temperature reaches approximately 175°C. When the thermal protection is activated, the output stage is disabled, allowing the device to cool. Quiescent current is approximately 6mA during thermal shutdown. When the junction temperature cools to approximately 165°C the output circuitry is again enabled. This can cause the protection circuit to cycle on and off with a period ranging from a fraction of a second to several minutes or more, depending on package type, signal, load and thermal environment.

The thermal protection circuit is designed to prevent damage during abnormal conditions. Any tendency to activate the thermal protection circuit during normal operation is a sign of an inadequate heat sink or excessive power dissipation for the package type.

TO-220 package provides the best thermal performance. When the TO-220 is used with a properly sized heat sink, output is not limited by thermal performance. See Application Bulletin AB-037 for details on heat sink calculations. The DDPAK also has excellent thermal characteristics. Its mounting tab should be soldered to a circuit board copper area for good heat dissipation. Figure 3 shows typical thermal resistance from junction to ambient as a function of the copper area. The mounting tab of the TO-220 and DDPAK packages is electrically connected to the V– power supply.

The DIP and SO-8 surface-mount packages are excellent for applications requiring high output current with low average power dissipation. To achieve the best possible thermal performance with the DIP or SO-8 packages, solder the device directly to a circuit board. Since much of the heat is dissipated by conduction through the package pins, sockets will degrade thermal performance. Use wide circuit board traces on all the device pins, including pins that are not connected. With the DIP package, use traces on both sides of the printed circuit board if possible.

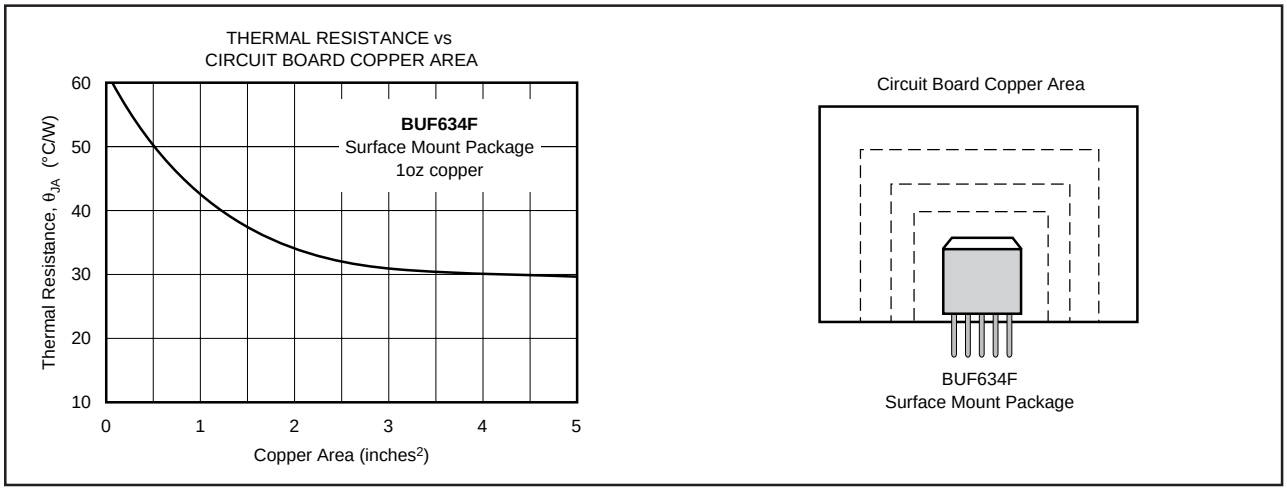


FIGURE 3. Thermal Resistance vs Circuit Board Copper Area.

POWER DISSIPATION

Power dissipation depends on power supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S - V_O$. Power dissipation can be minimized by using the lowest possible power supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power supply voltage. Dissipation with AC signals is lower. Application Bulletin AB-039 explains how to calculate or measure power dissipation with unusual signals and loads.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered. The thermal protection should trigger more than 45°C above the maximum expected ambient condition of your application.

INPUT CHARACTERISTICS

Internal circuitry is protected with a diode clamp connected from the input to output of the BUF634—see Figure 1. If the output is unable to follow the input within approximately 3V (such as with an output short-circuit), the input will conduct increased current from the input source. This is limited by the internal 200Ω resistor. If the input source can be damaged by this increase in load current, an additional resistor can be connected in series with the input.

BANDWIDTH CONTROL PIN

The –3dB bandwidth of the BUF634 is approximately 30MHz in the low quiescent current mode (1.5mA typical). To select this mode, leave the bandwidth control pin open (no connection).

Bandwidth can be extended to approximately 180MHz by connecting the bandwidth control pin to V–. This increases the quiescent current to approximately 15mA. Intermediate bandwidths can be set by connecting a resistor in series with the bandwidth control pin—see typical curve "Quiescent Current vs Resistance" for resistor selection. Characteristics of the bandwidth control pin can be seen in the simplified circuit diagram, Figure 1.

The rated output current and slew rate are not affected by the bandwidth control, but the current limit value changes slightly. Output voltage swing is somewhat improved in the wide bandwidth mode. The increased quiescent current when in wide bandwidth mode produces greater power dissipation during low output current conditions. This quiescent power is equal to the total supply voltage, (V+) + |(V–)|, times the quiescent current.

BOOSTING OP AMP OUTPUT CURRENT

The BUF634 can be connected inside the feedback loop of most op amps to increase output current—see Figure 4. When connected inside the feedback loop, the BUF634's offset voltage and other errors are corrected by the feedback of the op amp.

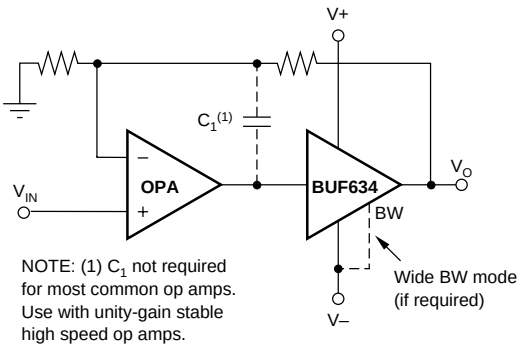
To assure that the op amp remains stable, the BUF634's phase shift must remain small throughout the loop gain of the circuit. For a G=+1 op amp circuit, the BUF634 must contribute little additional phase shift (approximately 20° or less) at the unity-gain frequency of the op amp. Phase shift is affected by various operating conditions that may affect stability of the op amp—see typical Gain and Phase curves.

Most general-purpose or precision op amps remain unity-gain stable with the BUF634 connected inside the feedback loop as shown. Large capacitive loads may require the BUF634 to be connected for wide bandwidth for stable operation. High speed or fast-settling op amps generally require the wide bandwidth mode to remain stable and to assure good dynamic performance. To check for stability with an op amp, look for oscillations or excessive ringing on signal pulses with the intended load and worst case conditions that affect phase response of the buffer.

HIGH FREQUENCY APPLICATIONS

The BUF634's excellent bandwidth and fast slew rate make it useful in a variety of high frequency open-loop applications. When operated open-loop, circuit board layout and bypassing technique can affect dynamic performance.

For best results, use a ground plane type circuit board layout and bypass the power supplies with 0.1µF ceramic chip capacitors at the device pins in parallel with solid tantalum 10µF capacitors. Source resistance will affect high-frequency peaking and step response overshoot and ringing. Best response is usually achieved with a series input resistor of 25Ω to 200Ω, depending on the signal source. Response with some loads (especially capacitive) can be improved with a resistor of 10Ω to 150Ω in series with the output.



OP AMP	RECOMMENDATIONS
OPA177, OPA1013 OPA111, OPA2111 OPA121, OPA234(1), OPA130(1)	Use Low I_Q mode. G = 1 stable.
OPA27, OPA2107 OPA602, OPA131(1)	Low I_Q mode is stable. Increasing C_L may cause excessive ringing or instability. Use Wide BW mode.
OPA627, OPA132(1)	Use Wide BW mode, C_1 = 200pF. G = 1 stable.
OPA637, OPA37	Use Wide BW mode. These op amps are not G = 1 stable. Use in G > 4.

NOTE: (1) Single, dual, and quad versions.

FIGURE 4. Boosting Op Amp Output Current.

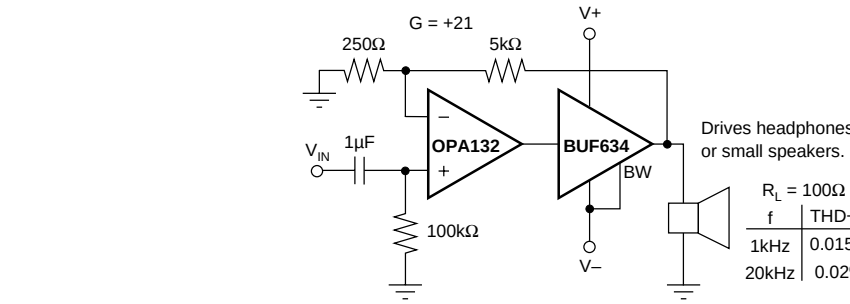


FIGURE 5. High Performance Headphone Driver.

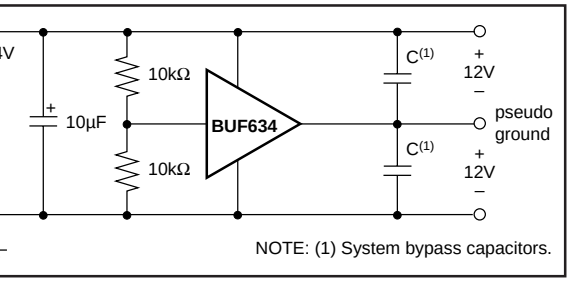


FIGURE 6. Pseudo-Ground Driver.

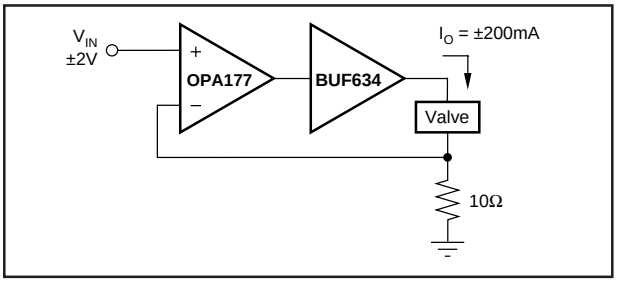


FIGURE 7. Current-Output Valve Driver.

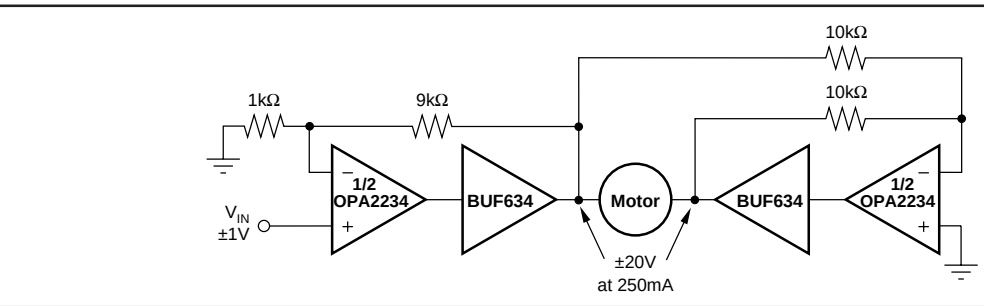


FIGURE 8. Bridge-Connected Motor Driver.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BUF634F	OBSOLETE	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI		BUF634F	
BUF634F/500	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS)	CU SN	Level-2-260C-1 YEAR		BUF634F	Samples
BUF634F/500E3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS)	CU SN	Level-2-260C-1 YEAR		BUF634F	Samples
BUF634FKTTT	ACTIVE	DDPAK/ TO-263	KTT	5	50	TBD	Call TI	Call TI		BUF634F	Samples
BUF634FKTTTE3	ACTIVE	DDPAK/ TO-263	KTT	5	50	TBD	Call TI	Call TI		BUF634F	Samples
BUF634P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		BUF634P	Samples
BUF634PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		BUF634P	Samples
BUF634T	ACTIVE	TO-220	KC	5	49	TBD	Call TI	Call TI		BUF634T	Samples
BUF634TG3	ACTIVE	TO-220	KC	5	49	TBD	Call TI	Call TI		BUF634T	Samples
BUF634U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		BUF 634U	Samples
BUF634U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		BUF 634U	Samples
BUF634U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		BUF 634U	Samples
BUF634UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		BUF 634U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

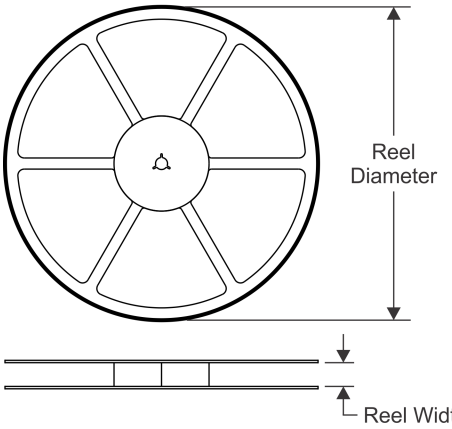
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

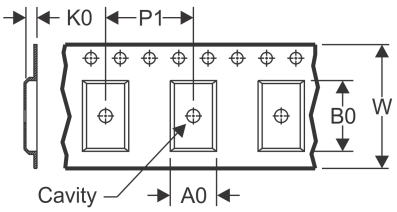
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

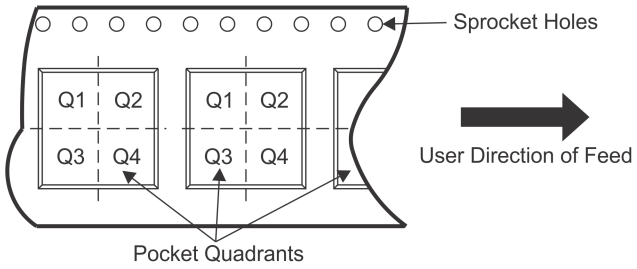


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

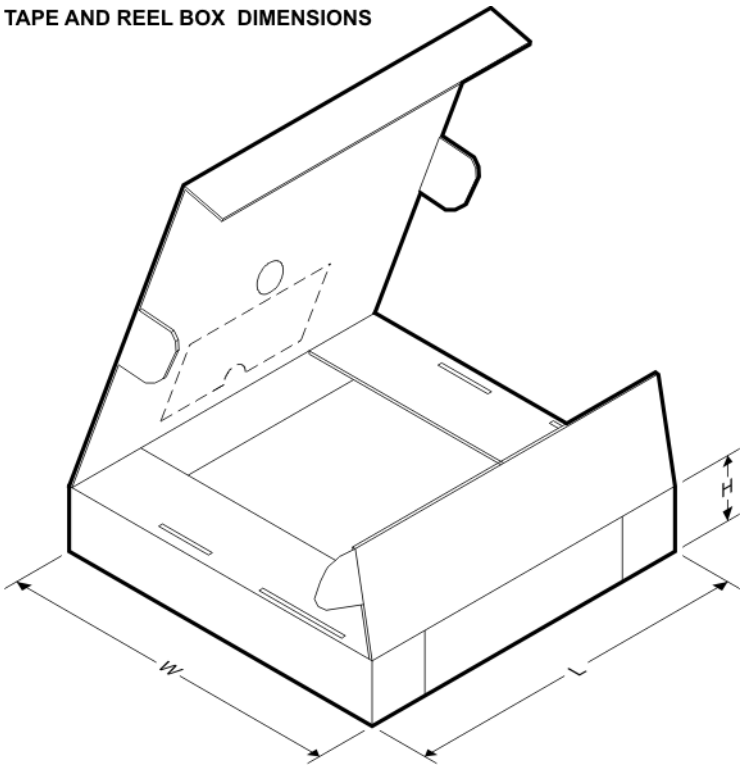
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF634U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

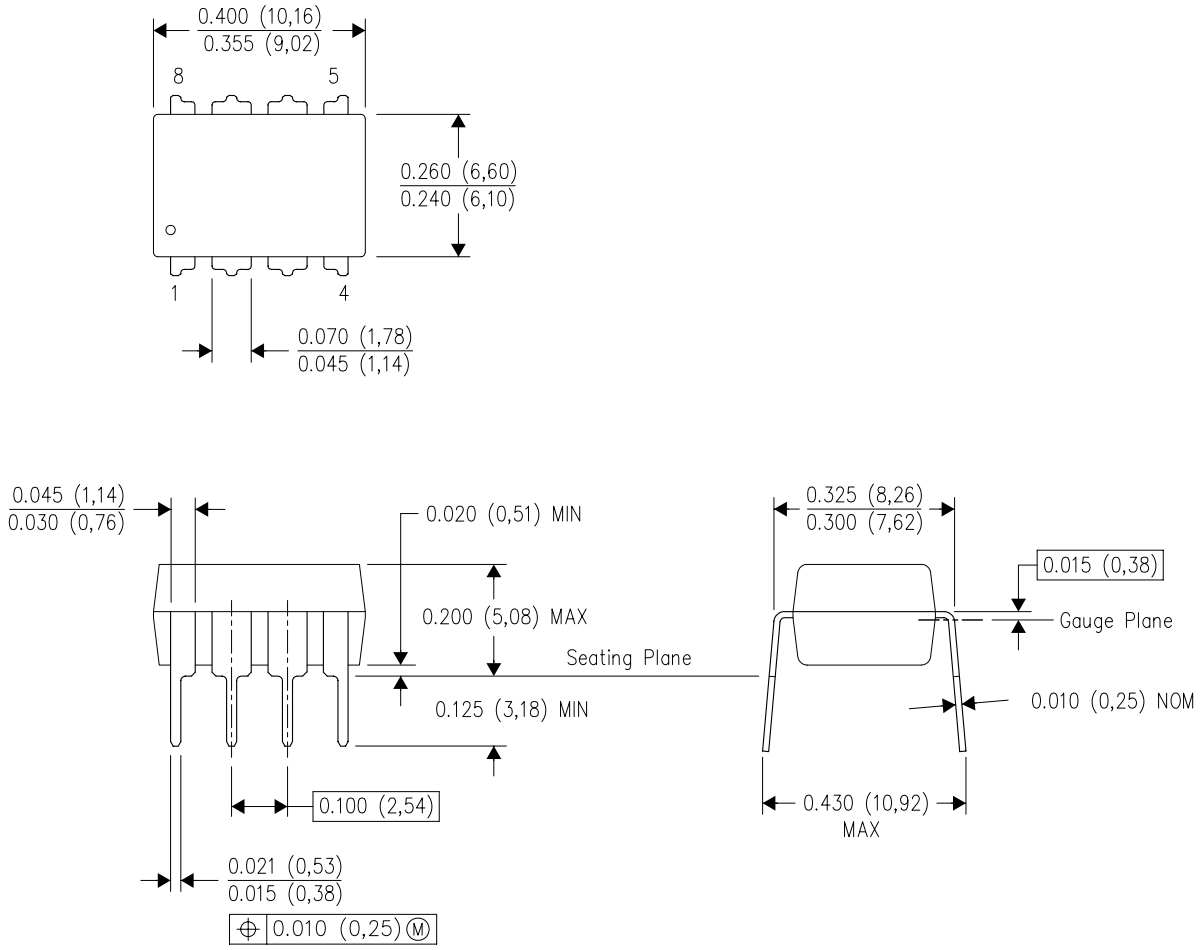
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

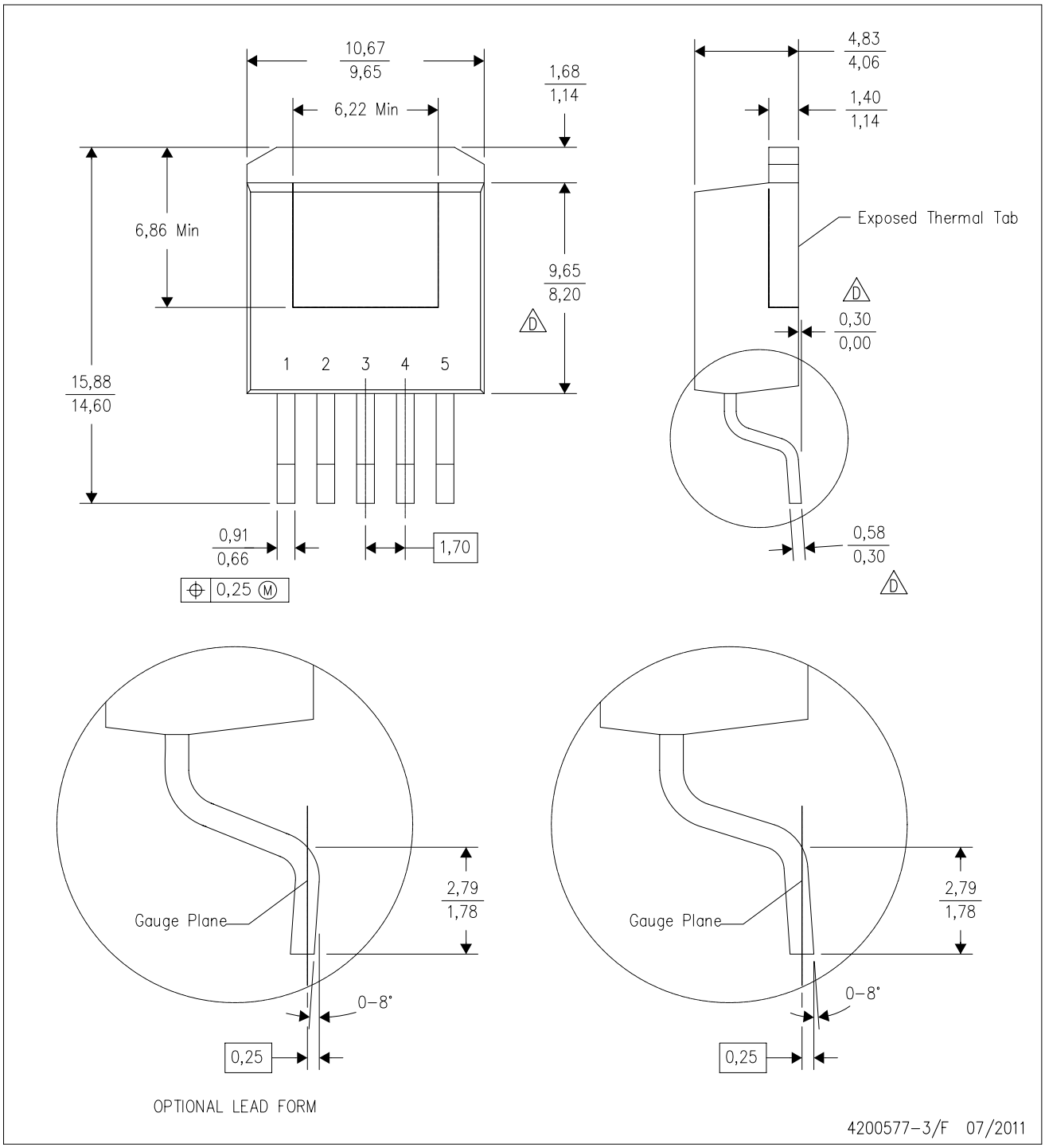
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF634U/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



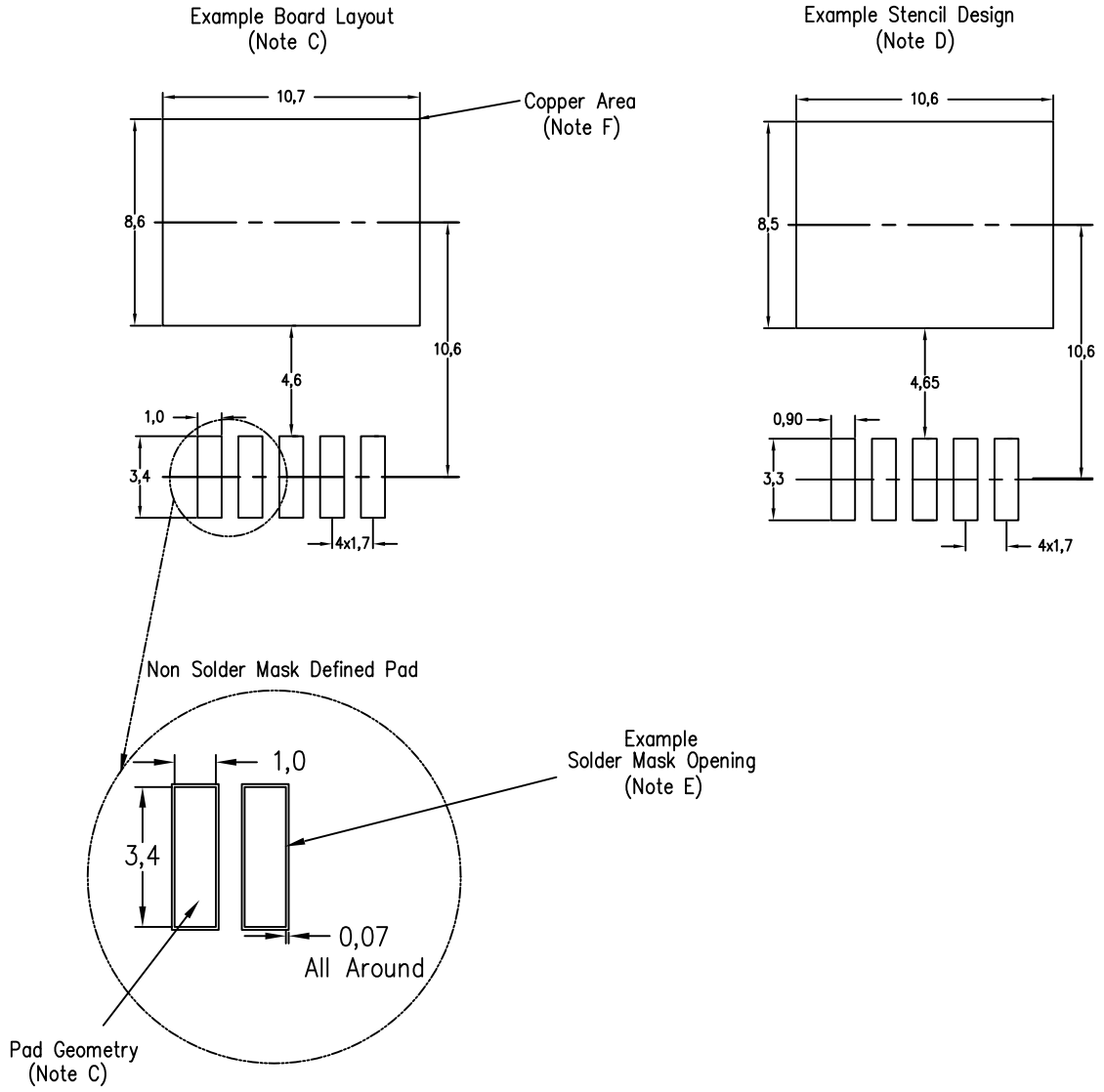
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



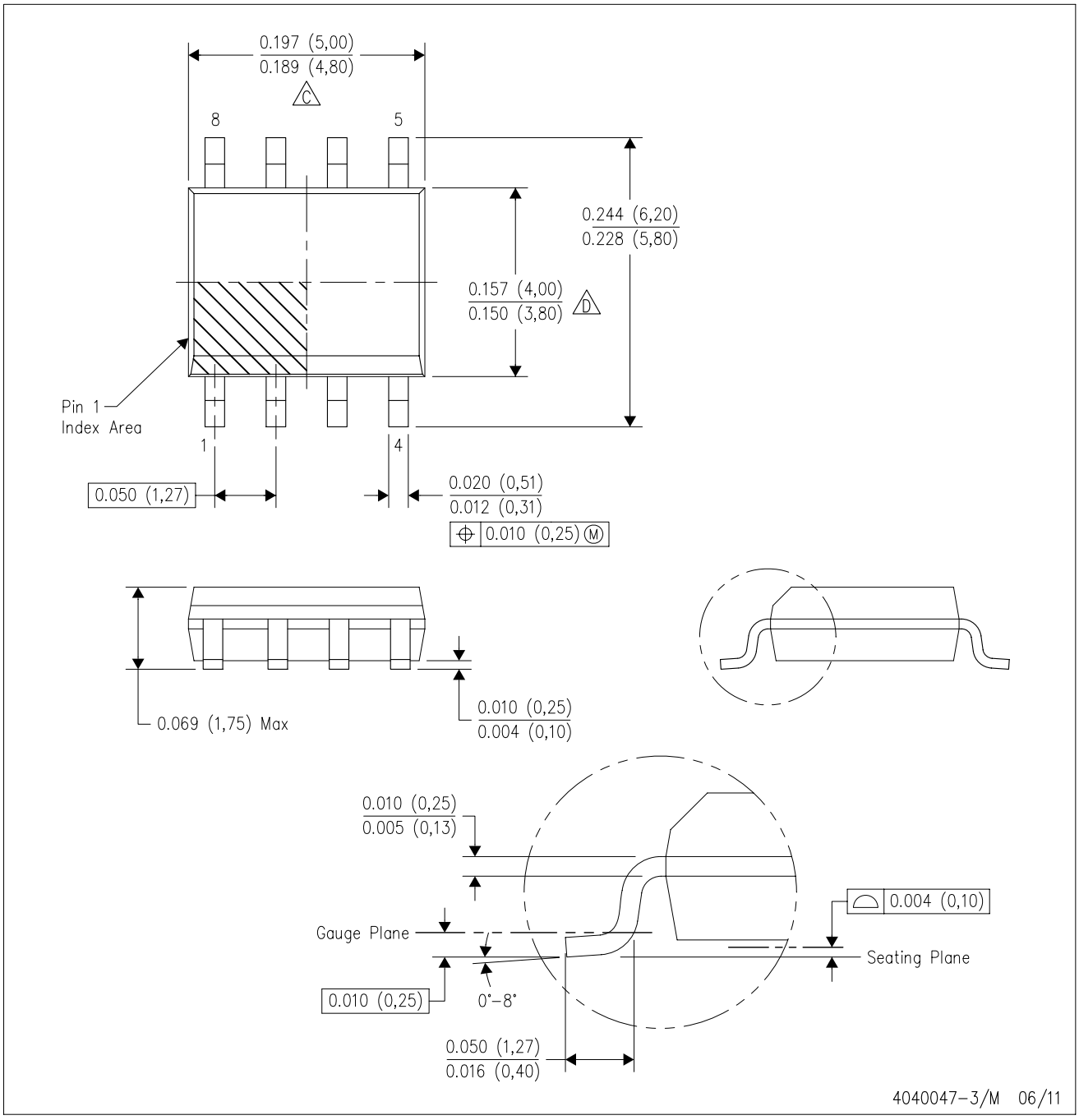
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



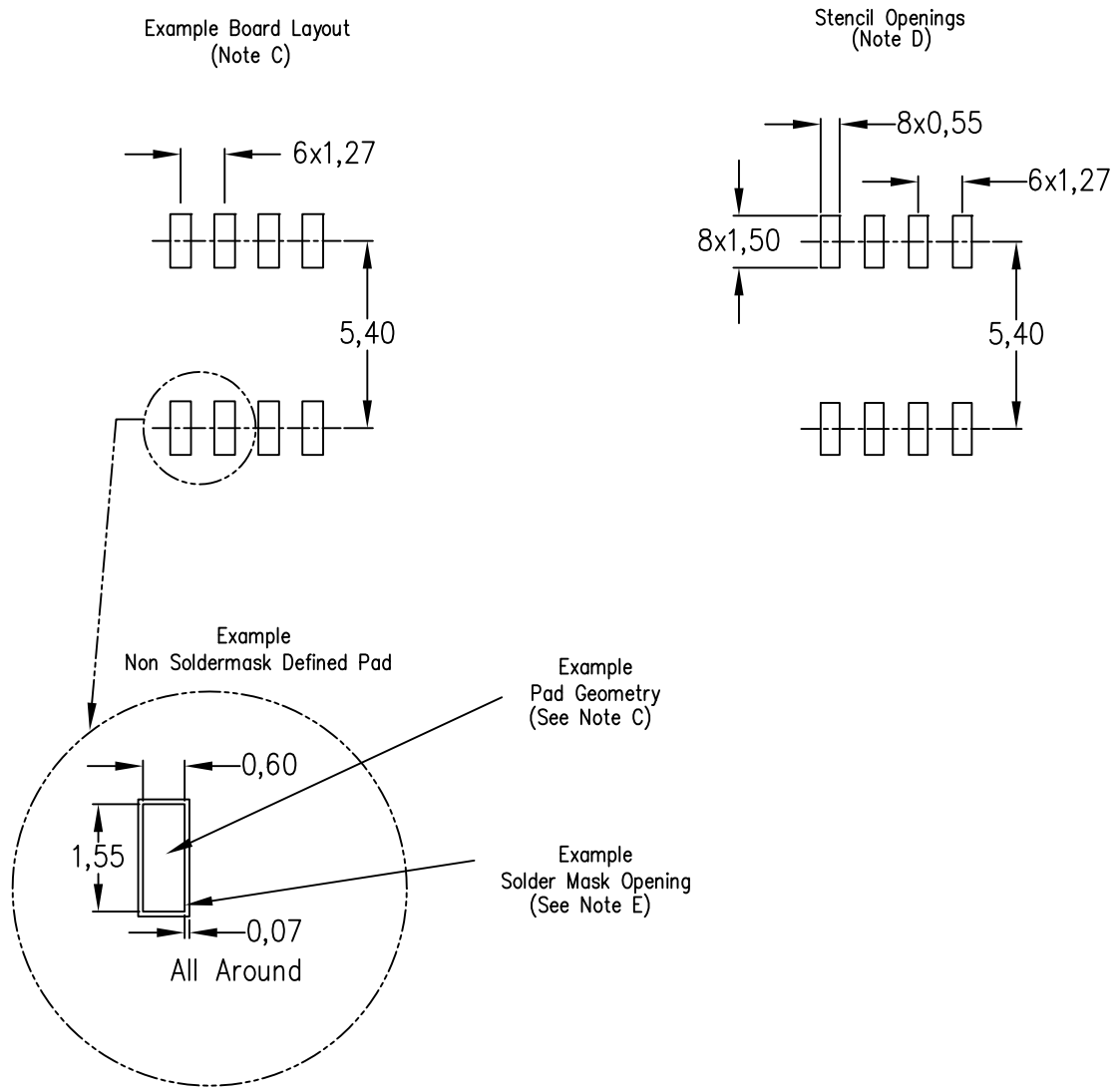
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



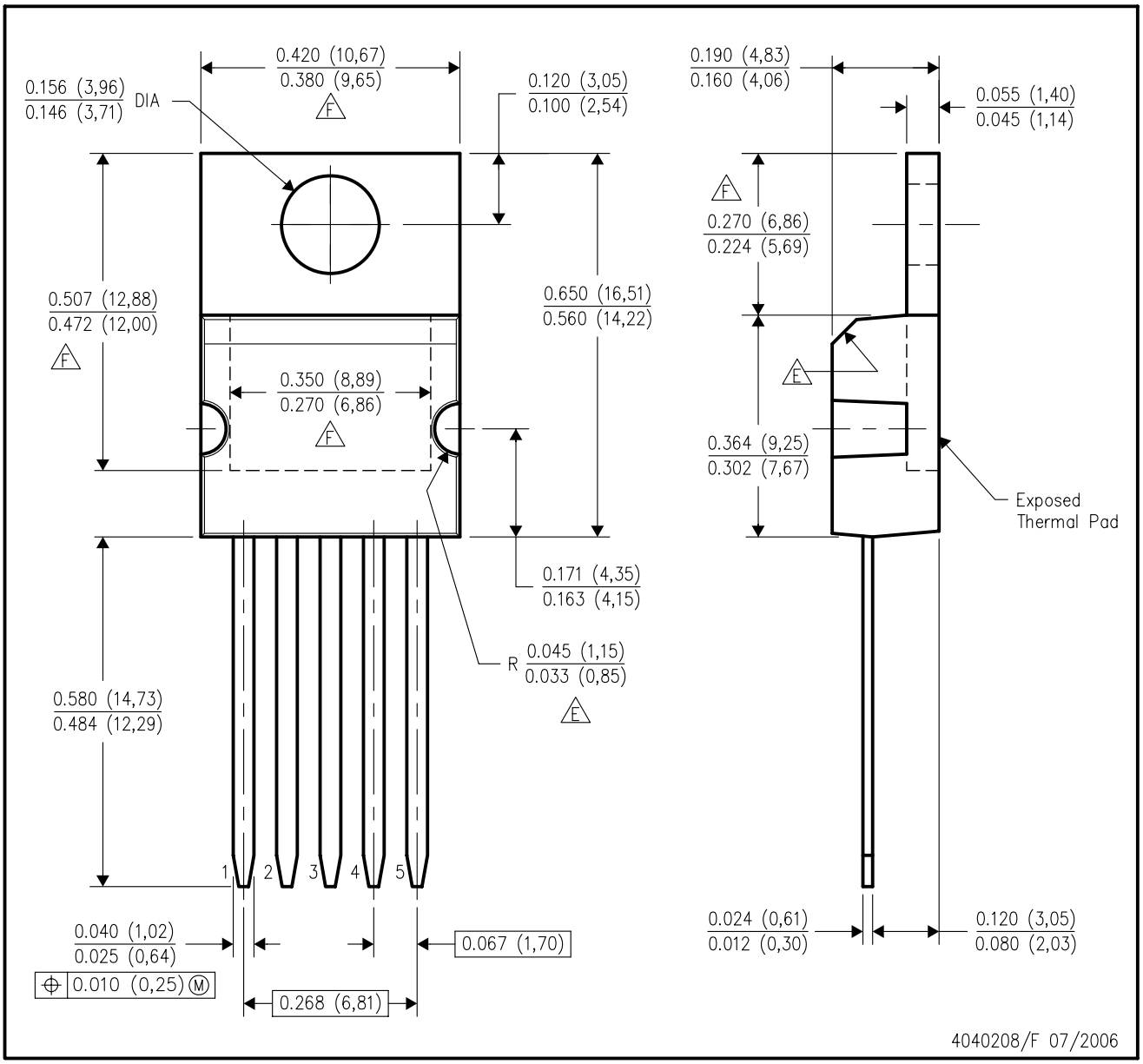
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

KC (R–PSFM–T5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. All lead dimensions apply before solder dip.
D. The center lead is in electrical contact with the mounting tab.
E. These features are optional.
F. Thermal pad contour optional within these dimensions.

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