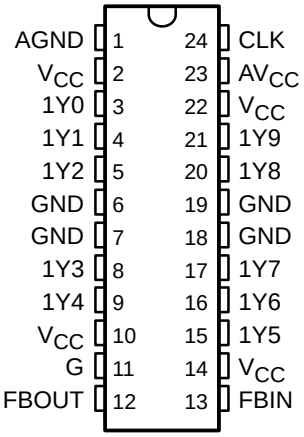
- **Designed to Meet PC SDRAM Registered DIMM Specification**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency 25 MHz to 125 MHz**
- **tPhase Error Minus Jitter at 66 MHz to 100 MHz Is ±150 ps**
- **Jitter (pk – pk) at 66 MHz to 100 MHz is ±80ps**
- **Jitter (cyc – cyc) at 66 MHz to 100 MHz is |100 ps|**
- **Available in Plastic 24-Pin TSSOP**
- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to One Bank of Ten Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback (FBIN) Terminal Is Used to Synchronize the Outputs to the Clock Input**
- **On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Operates at 3.3-V**

PW PACKAGE
(TOP VIEW)



description

The CDC2510B is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC2510B operates at 3.3-V V_{CC}. It also provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of ten outputs provides ten low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. All outputs can be enabled or disabled via a single output enable input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC2510B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2510B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, and following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground.

The CDC2510B is characterized for operation from 0°C to 70°C.

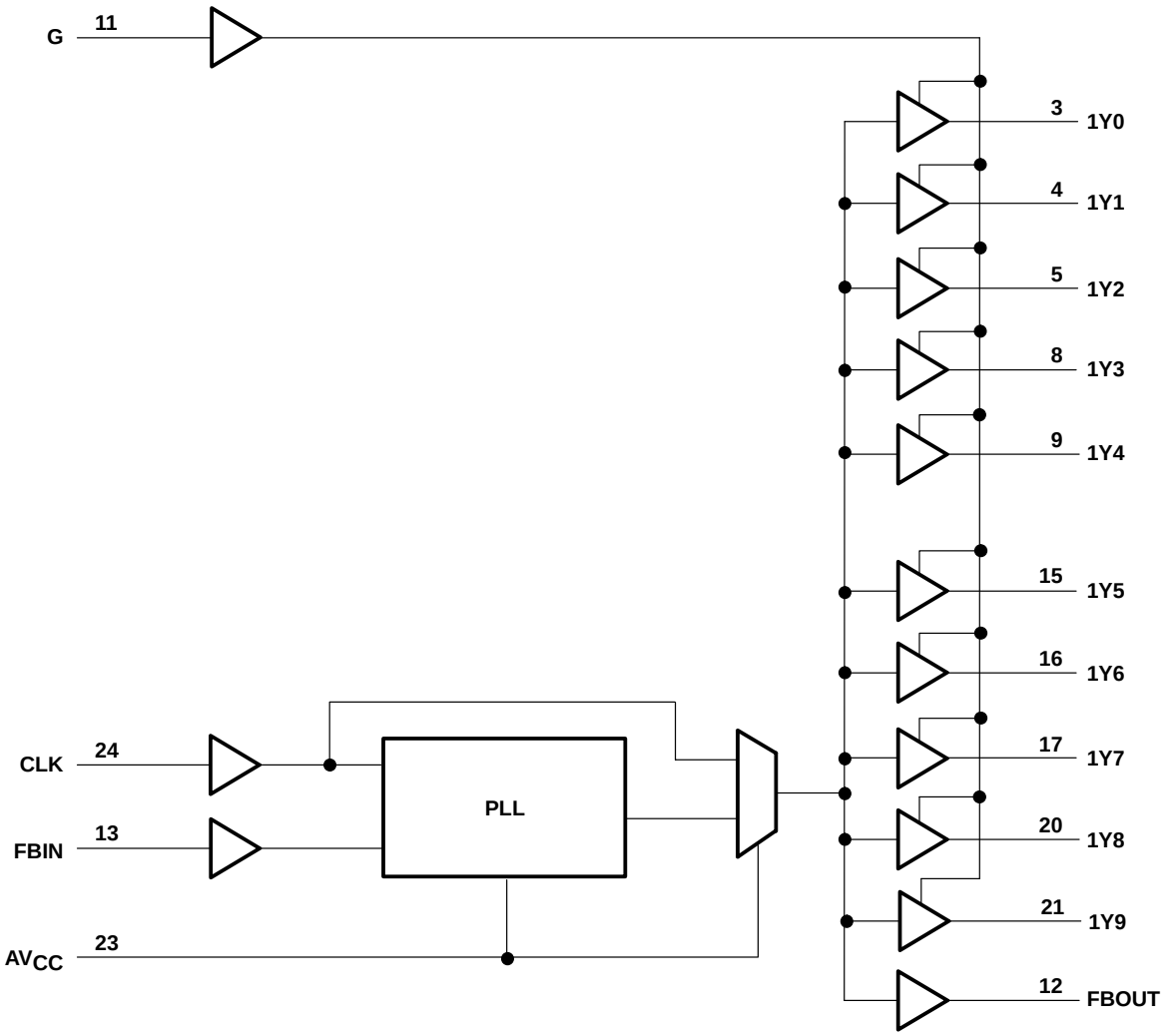
For application information refer to application reports *High Speed Distribution Design Techniques for CDC509/516/2509/2510/2516* (literature number SLMA003) and *Using CDC2509A/2510A PLL with Spread Spectrum Clocking (SSC)* (literature number SCAA039).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE

INPUTS		OUTPUTS	
G	CLK	1Y (0:9)	FBOUT
X	L	L	L
L	H	L	H
H	H	H	H

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 70°C	CDC2510BPWR

Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the CDC2510B clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs 1Y(0:9). When G is low, outputs 1Y(0:9) are disabled to a logic-low state. When G is high, all outputs 1Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has an integrated 25-Ω series-damping resistor.
1Y (0:9)	3, 4, 5, 8, 9 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:9) is enabled via the G input. These outputs can be disabled to a logic-low state by deasserting the G control input. Each output has an integrated 25-Ω series-damping resistor.
AV_{CC}	23	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V_{CC}	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, AV_{CC} (see Note 1) . . . . . $AV_{CC} < V_{CC}$ +0.7 V
Supply voltage range, V_{CC}, AV_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 2) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 2 and 3) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Maximum power dissipation at $T_A = 55°C$ (in still air) (see Note 4) . . . . . 0.7 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. AV_{CC} **must not** exceed V_{CC}.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 4.6 V maximum.
4. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

recommended operating conditions (see Note 5)

	MIN	MAX	UNIT
Supply voltage, V_{CC}, AV_{CC}	3	3.6	V
High-level input voltage, V_{IH}	2		V
Low-level input voltage, V_{IL}		0.8	V
Input voltage, V_I	0	V_{CC}	V
High-level output current, I_{OH}		–12	mA
Low-level output current, I_{OL}		12	mA
Operating free-air temperature, T_A	0	70	°C

NOTE 5: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		AV_{CC}, V_{CC}	MIN	TYP‡	MAX	UNIT
V_{IK}	I_I = –18 mA		3 V			–1.2	V
V_{OH}	I_{OH} = –100 µA		MIN to MAX	V_{CC}–0.2			V
	I_{OH} = –12 mA		3 V	2.1			
	I_{OH} = –6 mA		3 V	2.4			
V_{OL}	I_{OL} = 100 µA		MIN to MAX			0.2	V
	I_{OL} = 12 mA		3 V			0.8	
	I_{OL} = 6 mA		3 V			0.55	
I_I	$V_I = V_{CC}$ or GND		3.6 V			±5	µA
I_{CC}§	$V_I = V_{CC}$ or GND,	I_O = 0, Outputs: low or high	3.6 V			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND	3.3 V to 3.6 V			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		6		pF

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ For I_{CC} of AV_{CC} and I_{CC} vs Frequency (see Figures 7 and 8).

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{clk}	Clock frequency	25	125	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time†		1	ms

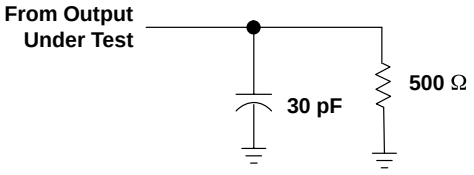
† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Note 6 and Figures 1 and 2)‡

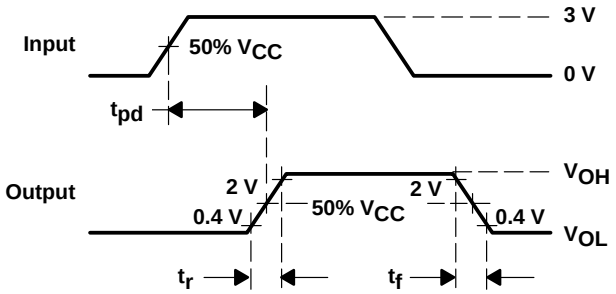
PARAMETER	FROM (INPUT)/CONDITION	TO (OUTPUT)	V_{CC}, AV_{CC} = 3.3 V ± 0.165 V			V_{CC}, AV_{CC} = 3.3 V ± 0.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{phase\ error,\ -\ jitter}$ (see Notes 7 and 8, Figures 3, 4, and 5)	CLKIN↑ = 66 MHz to 100 MHz	FBIN↑	–150		150	–200		200	ps
$t_{sk(o)}$§	Any Y or FBOUT	Any Y or FBOUT						200	ps
$Jitter_{(pk-pk)}$ (see Figure 6)	Clkin = 66 MHz to 100 MHz	Any Y or FBOUT				–80		80	ps
$Jitter_{(cycle-cycle)}$ (See Figure 6)		Any Y or FBOUT						|100|	
Duty cycle reference (see Figure 4)	F(clkin > 60 MHz)	Any Y or FBOUT				45%		55%	
t_r		Any Y or FBOUT		1.3	1.9	0.8		2.1	ns
t_f		Any Y or FBOUT		1.7	2.5	1.2		2.7	ns

‡ These parameters are not production tested.
§ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
NOTES: 6. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
7. This is considered as static phase error.
8. Phase error does not include jitter. The total phase error is –230 ps to 230 ps for the 5% V_{CC} range.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, Z_O = 50 Ω, t_r ≤ 1.2 ns, t_f ≤ 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

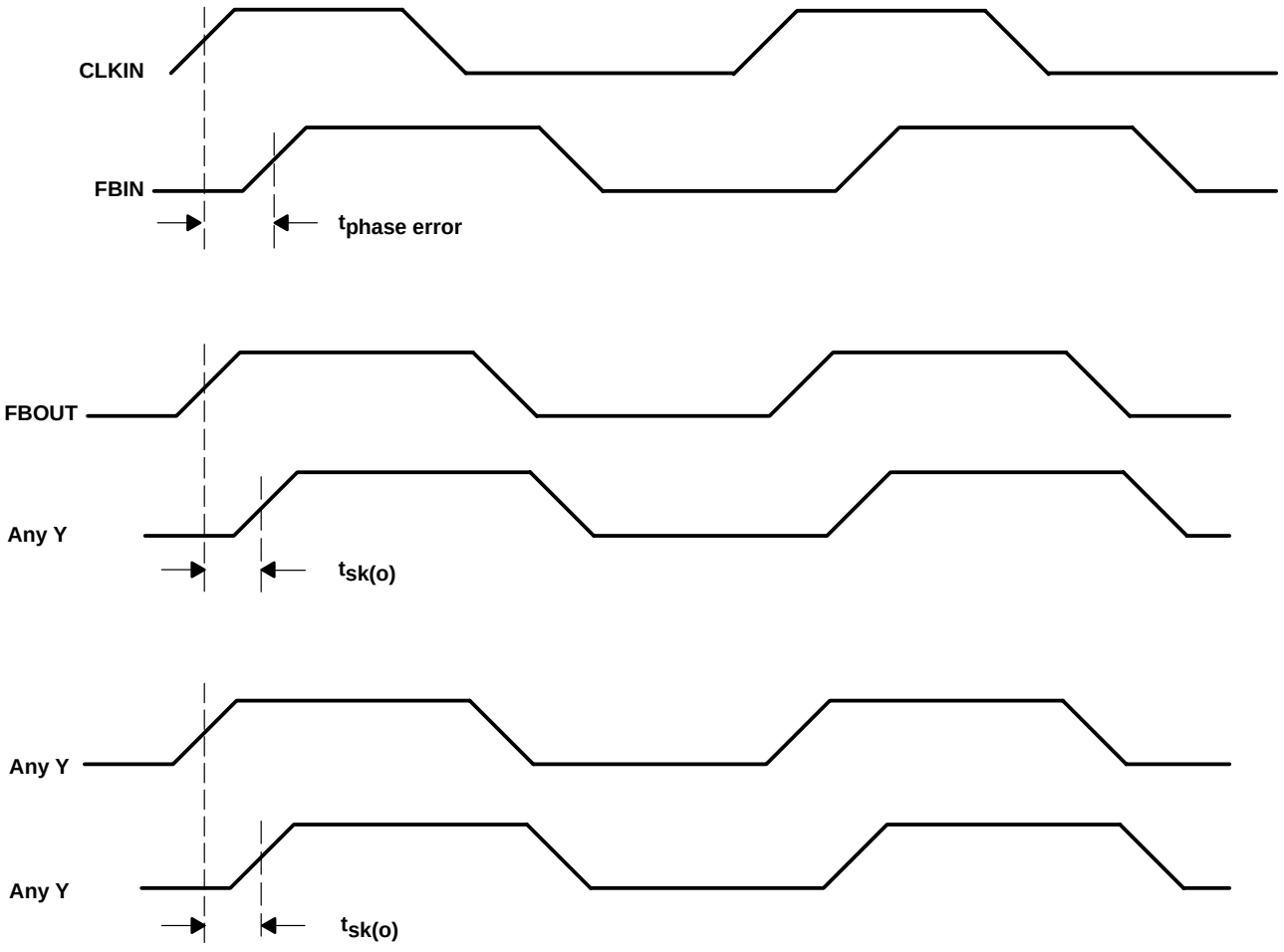


Figure 2. Phase Error and Skew Calculations

TYPICAL CHARACTERISTICS

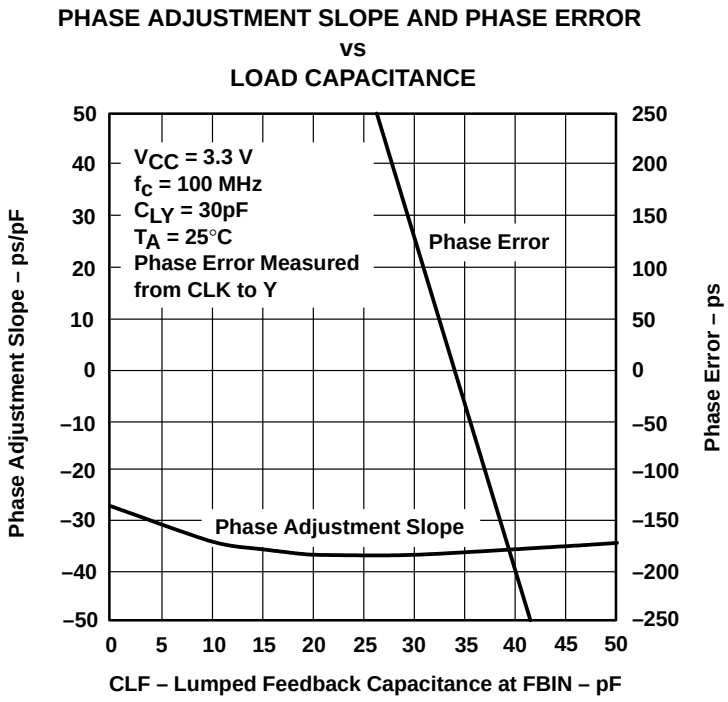


Figure 3

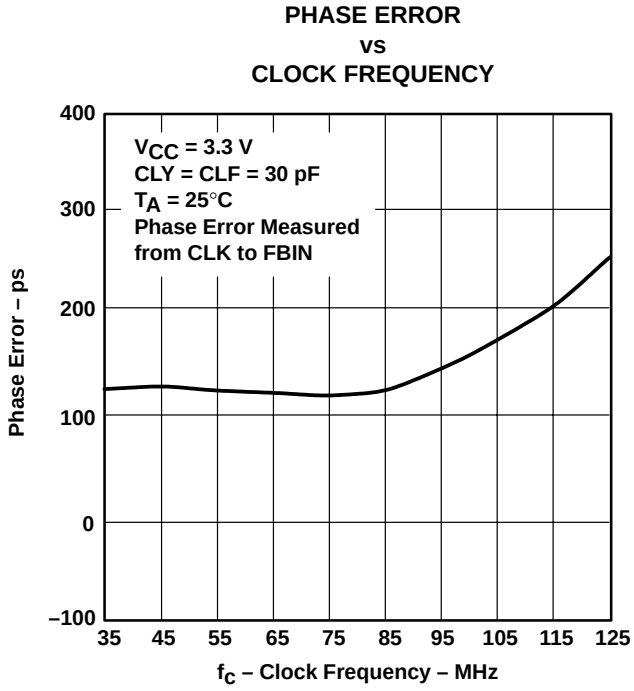


Figure 4

NOTES: A. CLY = Lumped capacitive load at Y
B. CLF = Lumped feedback capacitance at FBIN

TYPICAL CHARACTERISTICS

PHASE ERROR vs SUPPLY VOLTAGE

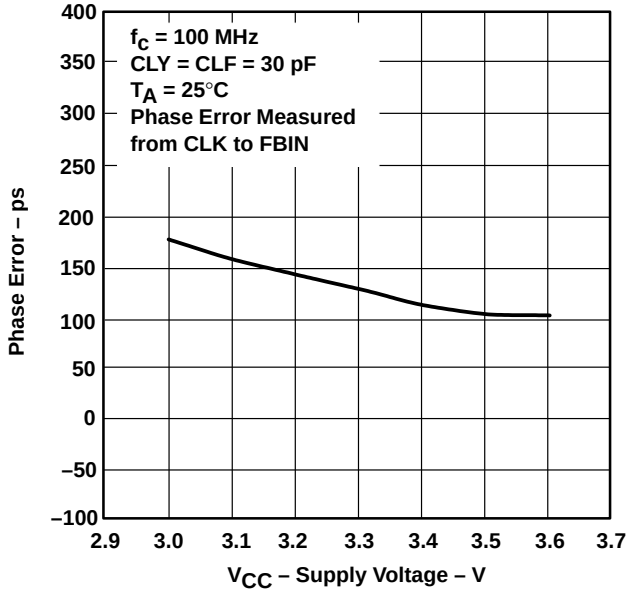


Figure 5

JITTER vs CLOCK FREQUENCY

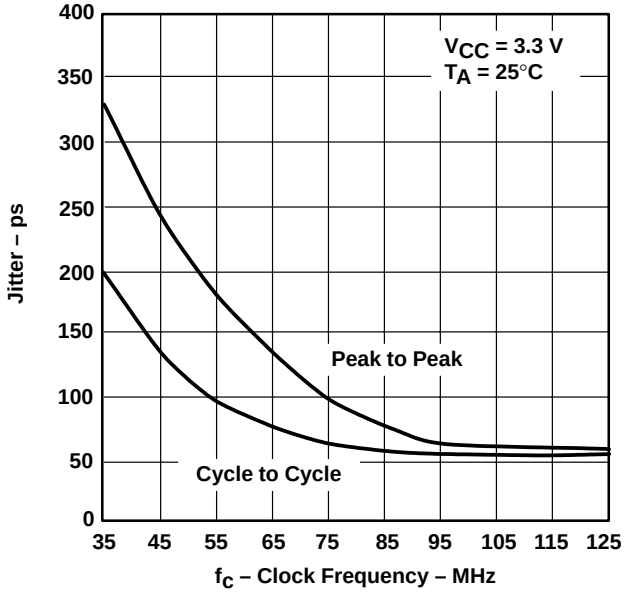


Figure 6

ANALOG SUPPLY CURRENT vs CLOCK FREQUENCY

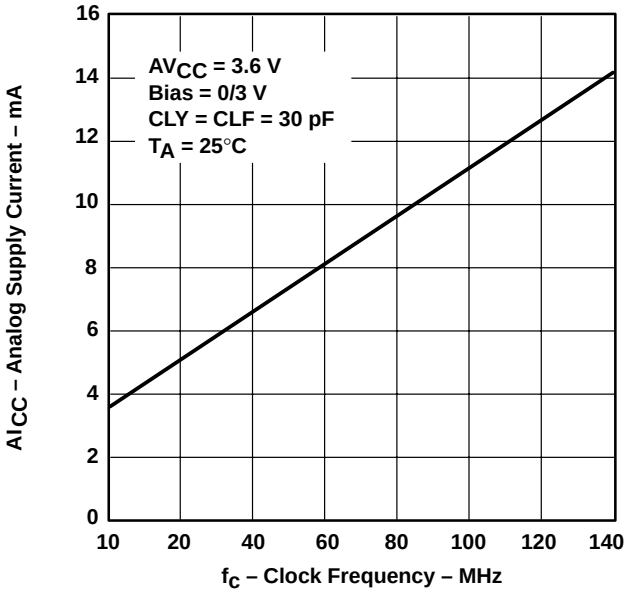


Figure 7

SUPPLY CURRENT vs CLOCK FREQUENCY

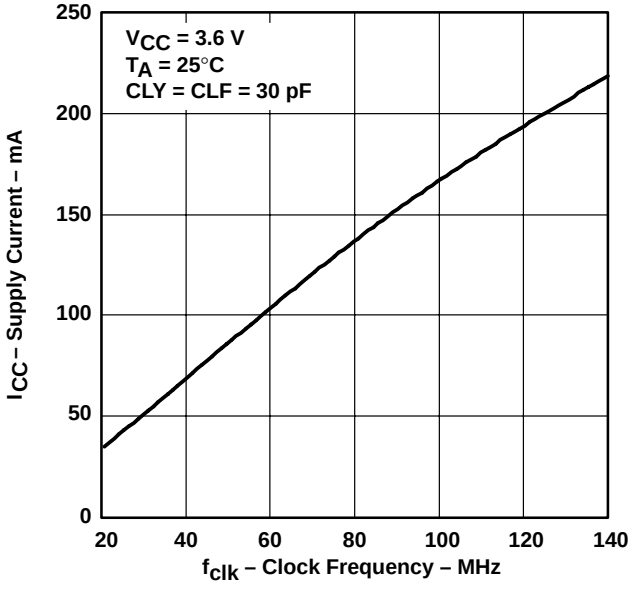


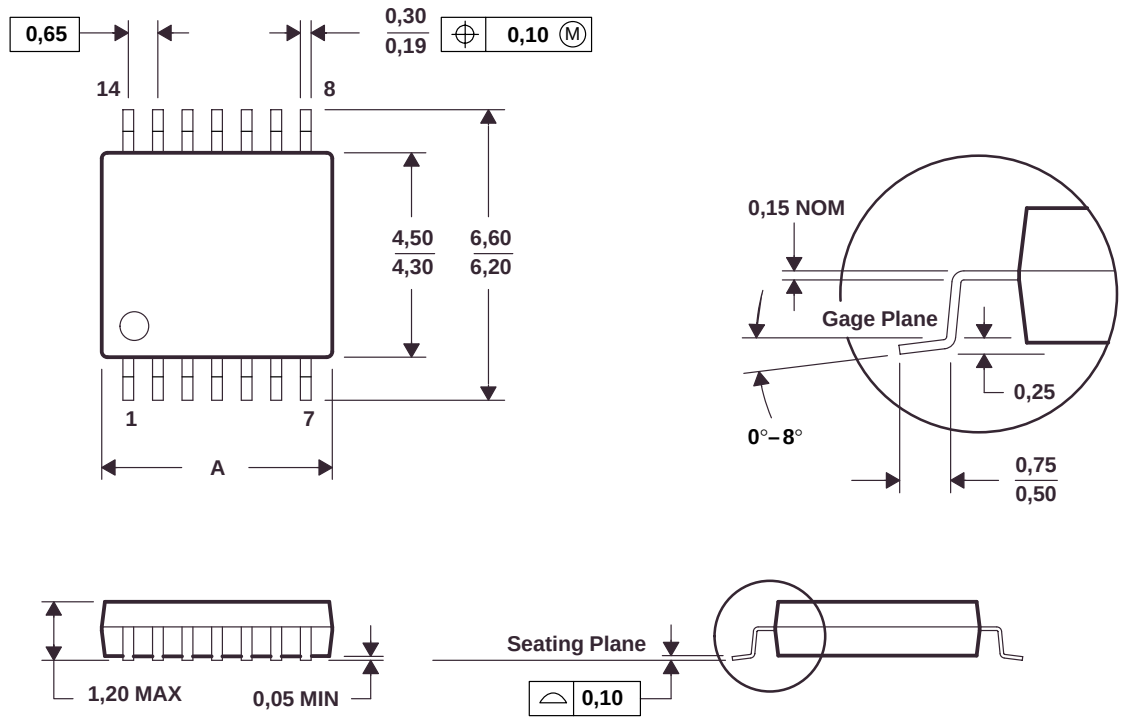
Figure 8

NOTES: A. CLY = Lumped capacitive load at Y
B. CLF = Lumped feedback capacitance at FBIN

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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