

CDC857-2, CDC857-3 2.5-/3.3-V PHASE-LOCK LOOP CLOCK DRIVERS

SCAS627A – SEPTEMBER 1999 – DECEMBER 1999

- Phase-Lock Loop Clock Distribution for Double Data Rate Synchronous DRAM Applications
- Distributes One Differential Clock Input to Ten Differential Outputs
- External Feedback Pins ($\overline{\text{FBIN}}$, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Clock Input
- Operates at $V_{CC} = 2.5\text{ V}$ and $AV_{CC} = 3.3\text{ V}$
- Packaged in Plastic 48-Pin (DGG) Thin Shrink Small-Outline Package (TSSOP)
- Spread Spectrum Clocking Tracking Capability to Reduce EMI

description

The CDC857-2 and CDC857-3 are high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. They use a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. The CDC857-3 operates at 3.3 V (PLL) and 2.5 V (output buffer). The CDC857-2 operates at 2.5 V (PLL and output buffer).

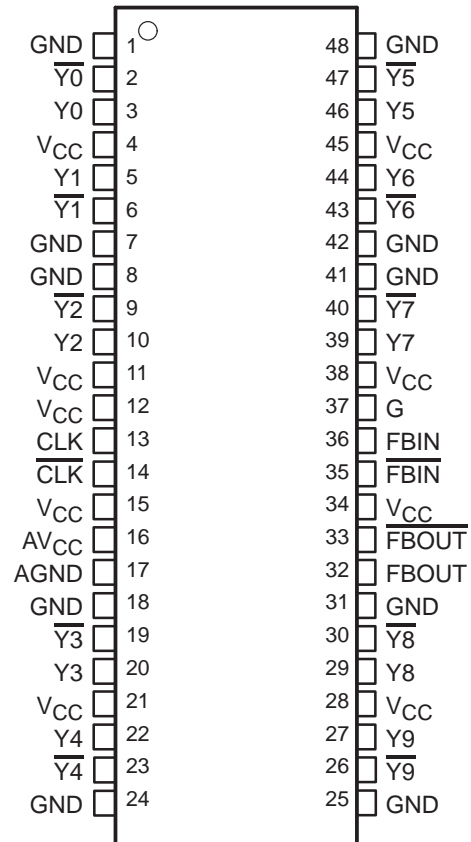
One bank of ten inverting and noninverting outputs provide ten low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50%, independent of the duty cycle at CLK.

All outputs can be enabled or disabled via a single output enable input. When the G input is high, the outputs switch in phase and frequency with CLK; when the G input is low, the outputs are disabled to high impedance state (3-state).

Unlike many products containing PLLs, the CDC857 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC857 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping AV_{CC} to ground. If AV_{CC} is at GND and $V_{CC} = \text{ON}$, 2 falling edges on G cause the PLL to run with FBOUT being enabled and all other outputs being disabled, after AV_{CC} ramps up to its specified V_{CC} value, with G being kept low. The CDC857 is characterized for operation from 0°C to 85°C.

DGG PACKAGE
(TOP VIEW)



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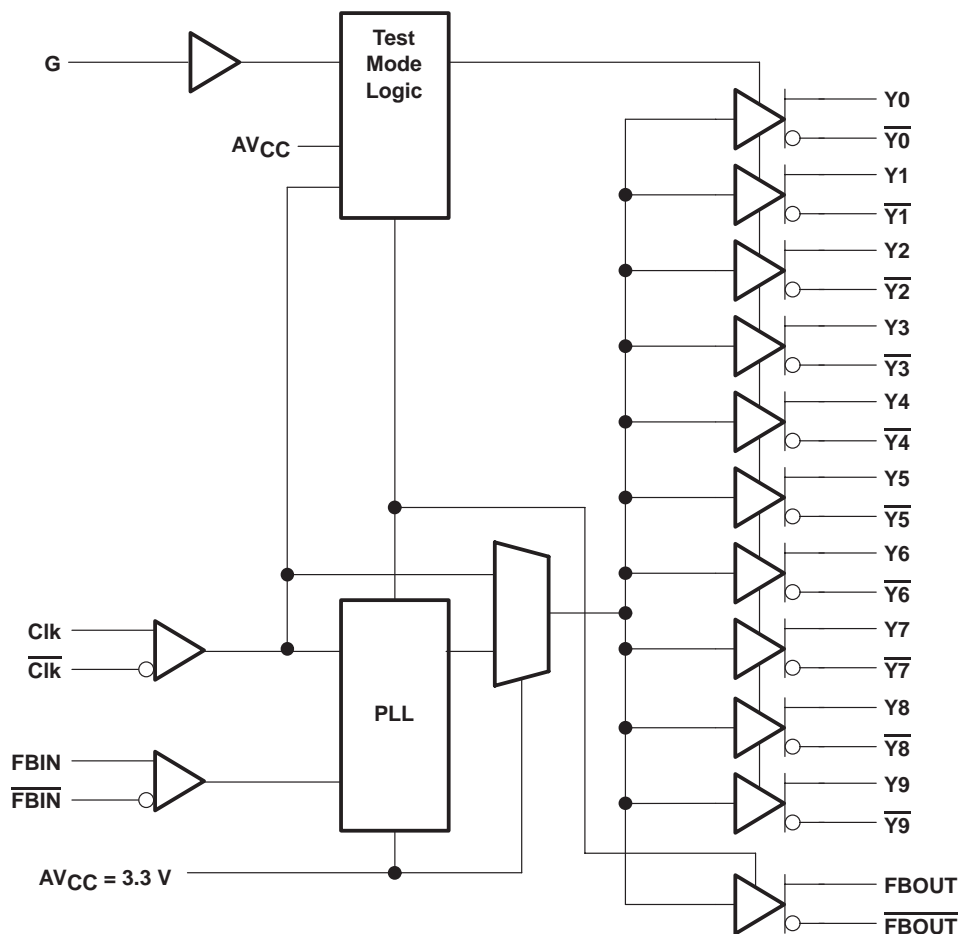
CDC857-2, CDC857-3 2.5-/3.3-V PHASE-LOCK LOOP CLOCK DRIVERS

SCAS627A – SEPTEMBER 1999 – DECEMBER 1999

FUNCTION TABLE

INPUTS			OUTPUTS				PLL
G	CLK	CLK	Y	Y	FBOU	FBOU	
L	X	X	Z	Z	Z	Z	OFF
H	L	H	L	H	L	H	RUN
H	H	L	H	L	H	L	RUN
H	< 20 MHz	< 20 MHz	Z	Z	Z	Z	OFF

logic symbol



NOTE A: All outputs are connected to $V_{CC} = 2.5\text{ V}$.

CDC857-2, CDC857-3

2.5-/3.3-V PHASE-LOCK LOOP CLOCK DRIVERS

SCAS627A – SEPTEMBER 1999 – DECEMBER 1999

SPECIAL TEST MODES

INPUTS				OUTPUTS				COMMENTS
V _{CC}	AV _{CC}	G	CLK _†	Y	\bar{Y}	FBOU _T	$\overline{\text{FBOU}}_{\text{T}}$	
ON	0 V	L	L	Z	Z	Z	Z	Clock Mode
ON	0 V	L	H	Z	Z	Z	Z	Clock Mode
ON	0 V	H	L	L	H	L	H	Clock Mode
ON	0 V	H	H	H	L	H	L	Clock Mode
ON	UP _‡	↓ _§	L	Z	Z	L	H	PLL Mode
ON	UP _‡	↓ _§	H	Z	Z	H	L	PLL Mode

† Only one signal shown for this differential input.

‡ AV_{CC} ramped up after two (2) high-to-low transitions on G input & G being low.

§ At least two (2) high-to-low transitions during AV_{CC} = 0.

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGND	17	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
AV _{CC}	16	Power	Analog power supply. AV _{CC} provides the power reference for the analog circuitry. In addition, AV _{CC} can be used to bypass the PLL for test purposes. When AV _{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. During disable (G = 0), the PLL is powered down.
CLK $\overline{\text{CLK}}$	13 14	I	Clock input, CLK provides the clock signal to be distributed by the CDC857 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN $\overline{\text{FBIN}}$	36 35	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOU _T to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
FBOU _T $\overline{\text{FBOU}}_{\text{T}}$	32 33	O	Feedback output. FBOU _T is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOU _T completes the feedback loop of the PLL.
G	37	I	Output bank enable. G is the output enable for outputs Y and \bar{Y} . When G is low outputs Y are disabled to a high-impedance state. When G is high, all outputs Y are enabled and switch at the same frequency as CLK.
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	Ground	Ground
V _{CC}	4, 11, 12, 15, 21, 28, 34, 38, 45	Power	Power supply
Y ₀ , Y ₁ , Y ₂ , Y ₃ , Y ₄ , Y ₅ , Y ₆ , Y ₇ , Y ₈ , Y ₉	3, 5, 10, 20, 22, 46, 44, 39, 29, 27	O	Clock outputs. These outputs provide low-skew copies of CLK.
$\overline{\text{Y}}_0$, $\overline{\text{Y}}_1$, $\overline{\text{Y}}_2$, $\overline{\text{Y}}_3$, $\overline{\text{Y}}_4$, $\overline{\text{Y}}_5$, $\overline{\text{Y}}_6$, $\overline{\text{Y}}_7$, $\overline{\text{Y}}_8$, $\overline{\text{Y}}_9$	2, 6, 9, 19, 23, 47, 43, 40, 30, 26	O	Clock outputs. These outputs provide low-skew copies of $\overline{\text{CLK}}$.

CDC857-2, CDC857-3

2.5-/3.3-V PHASE-LOCK LOOP CLOCK DRIVERS

SCAS627A – SEPTEMBER 1999 – DECEMBER 1999

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} or AV_{CC}	-0.5 V to 4.6 V
Input voltage range V_I (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O , (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous total output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Package thermal impedance, θ_{JA} (see Note 3)	89°C/W
Storage temperature range T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			2.3		2.7	V
Analog supply voltage, AV_{CC}	CDC857-2		2.3		2.7	V
	CDC857-3		3		3.6	V
Low-level input voltage, $V_{IL(G)}$		G input			$0.3 \times V_{CC}$	V
High-level input voltage, $V_{IH(G)}$		G input		$0.7 \times V_{CC}$		V
DC input signal voltage (see Note 5)		CLK, FBIN	-0.3		$V_{CC} + 0.3$	V
Differential input signal voltage, V_{ID} (see Note 6)	dc	CLK, FBIN	0.35		$V_{CC} + 0.6$	V
	ac	CLK, FBIN	0.7		$V_{CC} + 0.6$	V
Differential cross-point input voltage (see Note 7)			$V_{CC}/2 - 0.2$	$V_{CC}/2$	$V_{CC}/2 + 0.2$	V
High-level output current, I_{OH}					-12	mA
Low-level output current, I_{OL}					12	mA
Input slew rate, SR			1			V/ns
Operating free-air temperature, T_A			0		85	°C

- NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
 5. DC input signal voltage specifies the allowable dc execution of differential input.
 6. Differential input signal voltage specifies the differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input level and V_{CP} is the complementary input level (see figure 3).
 7. Differential cross-point voltage is expected to track variations of V_{CC} and is the voltage at which the differential signals must be crossing.



CDC857-2, CDC857-3 2.5-/3.3-V PHASE-LOCK LOOP CLOCK DRIVERS

SCAS627A – SEPTEMBER 1999 – DECEMBER 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}	Input voltage	All input pins V _{CC} = 2.3 V, I _I = -18 mA			-1.2	V
V _{OH}	High-level output voltage	V _{CC} = min to max, I _{OH} = -1 mA	V _{CC} -0.1			V
		V _{CC} = 2.3 V, I _{OH} = -12 mA	1.7			
V _{OL}	Low-level output voltage	V _{CC} = min to max, I _{OL} = 1 mA			0.1	V
		V _{CC} = 2.3 V, I _{OL} = 12 mA			0.6	
I _{OH}	High-level output current	V _{CC} = 2.3 V, V _O = 1 V	-18	-32		mA
I _{OL}	Low-level output current	V _{CC} = 2.3 V, V _O = 1.2 V	26	35		mA
V _O	Output voltage swing	For load condition see Figure 3	1.1		V _{CC} -0.4	V
I _I	Input current	G	V _{CC} = 2.7 V, V _I = 0 V to 2.7 V		±10	μA
		CLK, FBIN	V _{CC} = 2.7 V, V _I = 0 V to 2.7 V		±10	
I _{OZ}	High-impedance output current	V _{CC} = 2.7 V, V _O = V _{CC} or GND			±10	μA
V _{OC}	Output crossing point voltage‡		(V _{CC} /2)-0.1	V _{CC} /2	(V _{CC} /2)+0.1	V
I _{CCZ}	Supply current, disabled	A _{VCC} and V _{CC} = max, G = L or no input CLK signal		500	800	μA
I _{CC}	Supply current on V _{CC} (see Figure 7)	V _{CC} = 2.7 V, f _O = 167 MHz, All outputs switching 16 pF in 60 Ω environment, See Figure 3		235	300	mA
A _I CC	Supply current on A _V CC	CDC857-2	A _{VCC} = 2.7 V, f _O = 167 MHz	9	12	mA
		CDC857-3	A _{VCC} = 3.6 V, f _O = 167 MHz	15	19	
C _I	Input capacitance	V _{CC} = 2.5 V, V _I = V _{CC} or GND		2		pF
C _O	Output capacitance	V _{CC} = 2.5 V, V _O = V _{CC} or GND		3		pF

† All typical values are at respective nominal V_{CC}.

‡ The value of V_{OC} is expected to be |V_{VTR} + V_{VCP}|/2. In case of each clock directly terminated by a 120-Ω resistor, where V_{VTR} is the true input signal voltage and V_{VCP} is the complementary input signal voltage (see Figure 3).

CDC857-2, CDC857-3

2.5-/3.3-V PHASE-LOCK LOOP CLOCK DRIVERS

SCAS627A – SEPTEMBER 1999 – DECEMBER 1999

timing requirements over recommended ranges or supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
f_C Clock frequency		66	167	MHz
Input clock duty cycle		40%	60%	
Stabilization time [†]			0.1	ms

[†] Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

switching characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}^{\ddagger} Low-to-high level propagation delay time (see Figure 5)	CLK mode/CLK to any output	1.5	3.5	6	ns
t_{PHL}^{\ddagger} High-to-low level propagation delay time (see Figure 5)	CLK mode/CLK to any output	1.5	3.5	6	ns
t_{en} Output enable time	CLK mode/G to any Y output		3		ns
t_{dis} Output disable time	CLK mode/G to any Y output		3		ns
$t_{(jitter)}$ Jitter (peak-to-peak)	66 MHz			120	ps
	100/125/133/167 MHz			75	
$t_{(jitter)}$ Jitter (cycle-to-cycle)	66 MHz			110	ps
	100/125/133/167 MHz			65	
$t_{(phase\ error)}$ Phase error (see Figure 4)	All differential input and output terminals are terminated with 120 Ω /16 pF as shown in Figure 2	-150		150	ps
$t_{skew(0)}$ Output skew (see Figure 4)				100	ps
$t_{skew(p)}$ Pulse skew				100	ps
Duty cycle [§] (see Figure 6)	66 MHz to 100 MHz	49.5%		50.5%	
	101 MHz to 167 MHz	49%		51%	
t_r, t_f Output rise and fall times (20% – 80%)	Load = 120 Ω /16 pF	650	800	950	ps

[‡] Refers to transition of noninverting output.

[§] While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WH}/t_C , where the cycle time (t_C) decreases as the frequency goes up.



APPLICATION EXAMPLE

Table 1. Clock Structure and SDRAM Loads per Clock

CLOCK STRUCTURE	NUMBER of SDRAM LOADS PER CLOCK	CAPACITIVE LOADING ON THE PLL OUTPUTS (pF)	
		MIN	MAX
1	2	5	8
2	4	10	16

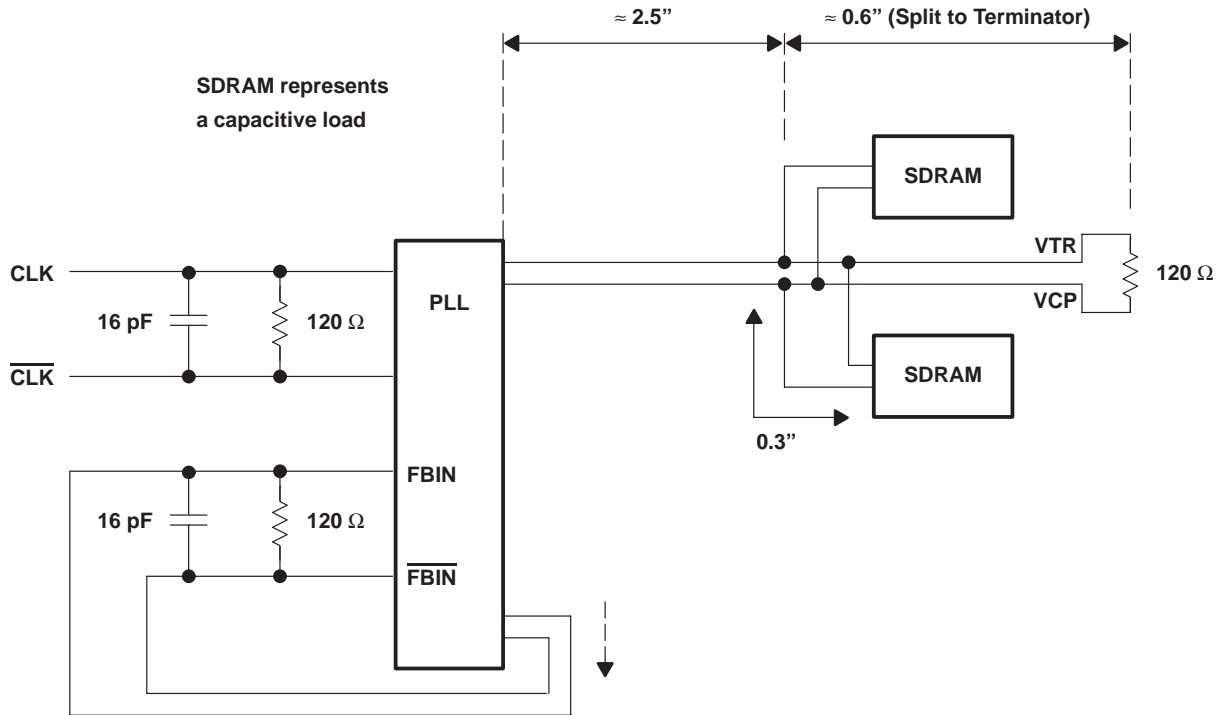


Figure 1. Clock Structure #1

CDC857-2, CDC857-3 2.5-/3.3-V PHASE-LOCK LOOP CLOCK DRIVERS

SCAS627A – SEPTEMBER 1999 – DECEMBER 1999

APPLICATION EXAMPLE

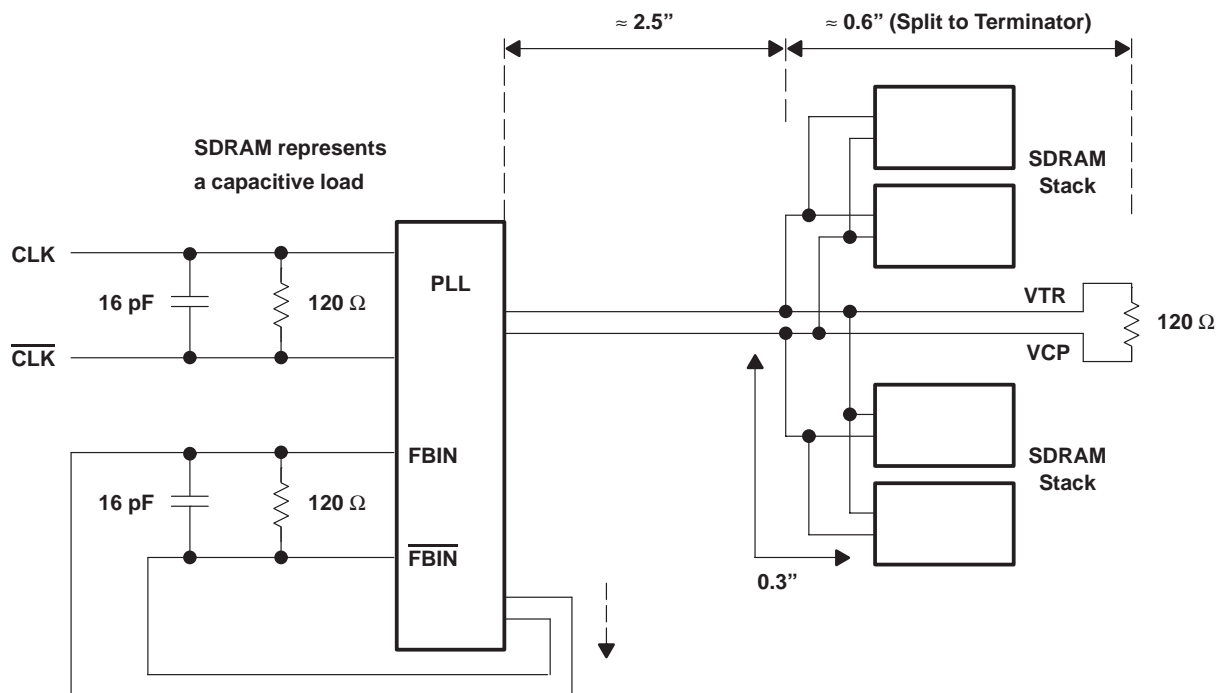


Figure 2. Clock Structure #2

differential clock signals

Figure 3 shows the differential clocks are directly terminated by a 120-Ω resistor.

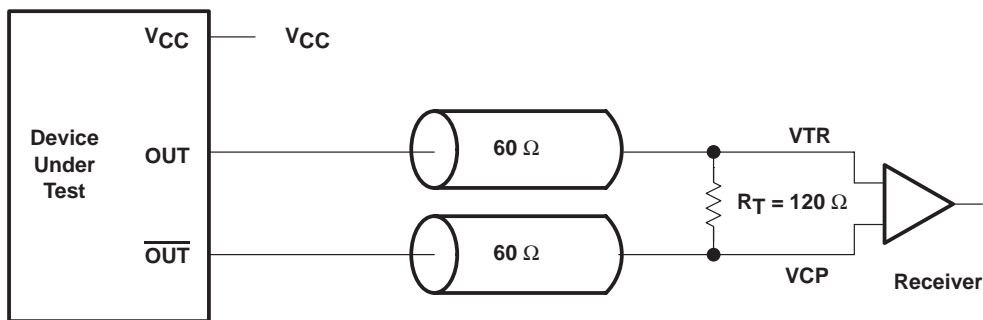


Figure 3. Differential Signal Using Direct Termination Resistor

PARAMETER MEASUREMENT INFORMATION

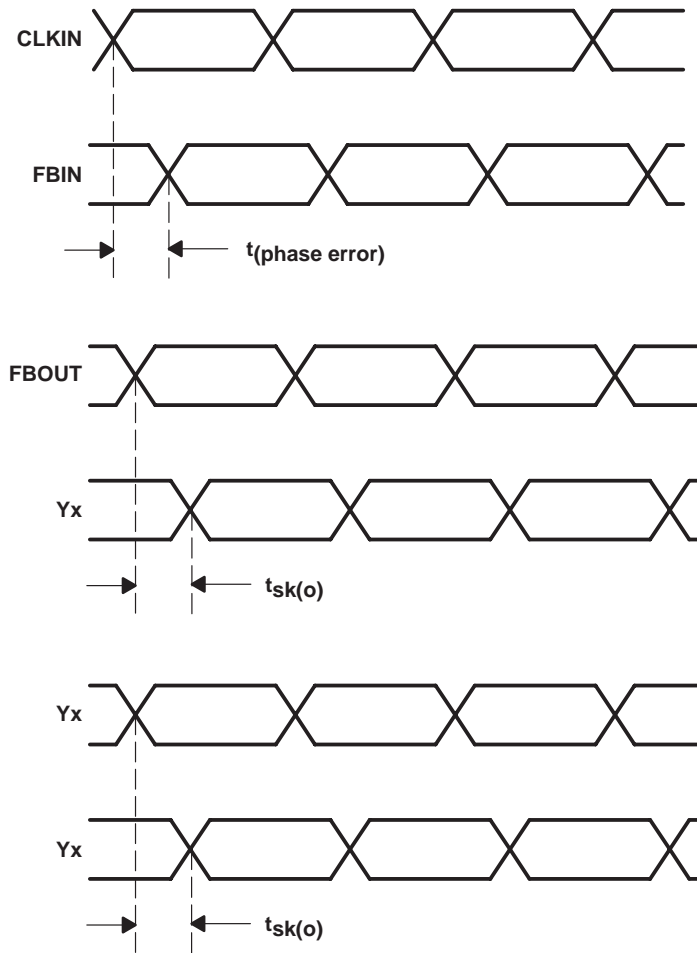


Figure 4. Phase Error and Skew Waveforms

PARAMETER MEASUREMENT INFORMATION

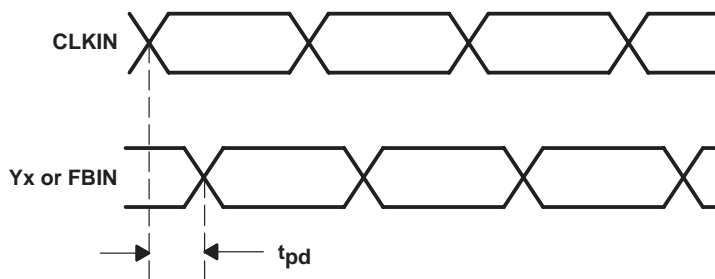
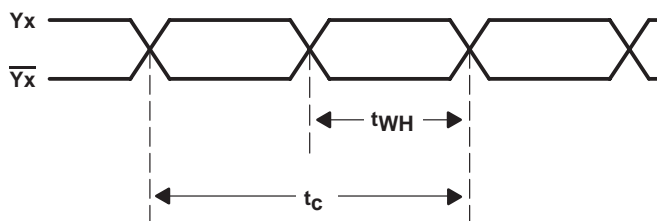
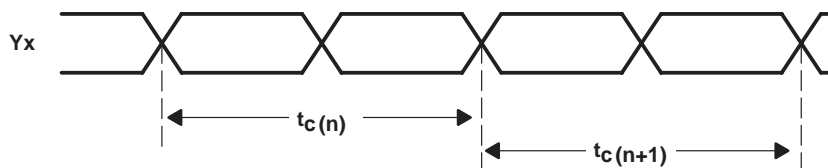


Figure 5. Propagation Delay Time; t_{pLH} , t_{pHL}



NOTE A: Duty cycle = t_{WH}/t_c

Figure 6. Output Duty Cycle



NOTE A: Cycle-to-cycle jitter = $|t_{c(n)} - t_{c(n+1)}|$ over 2000 consecutive cycles.

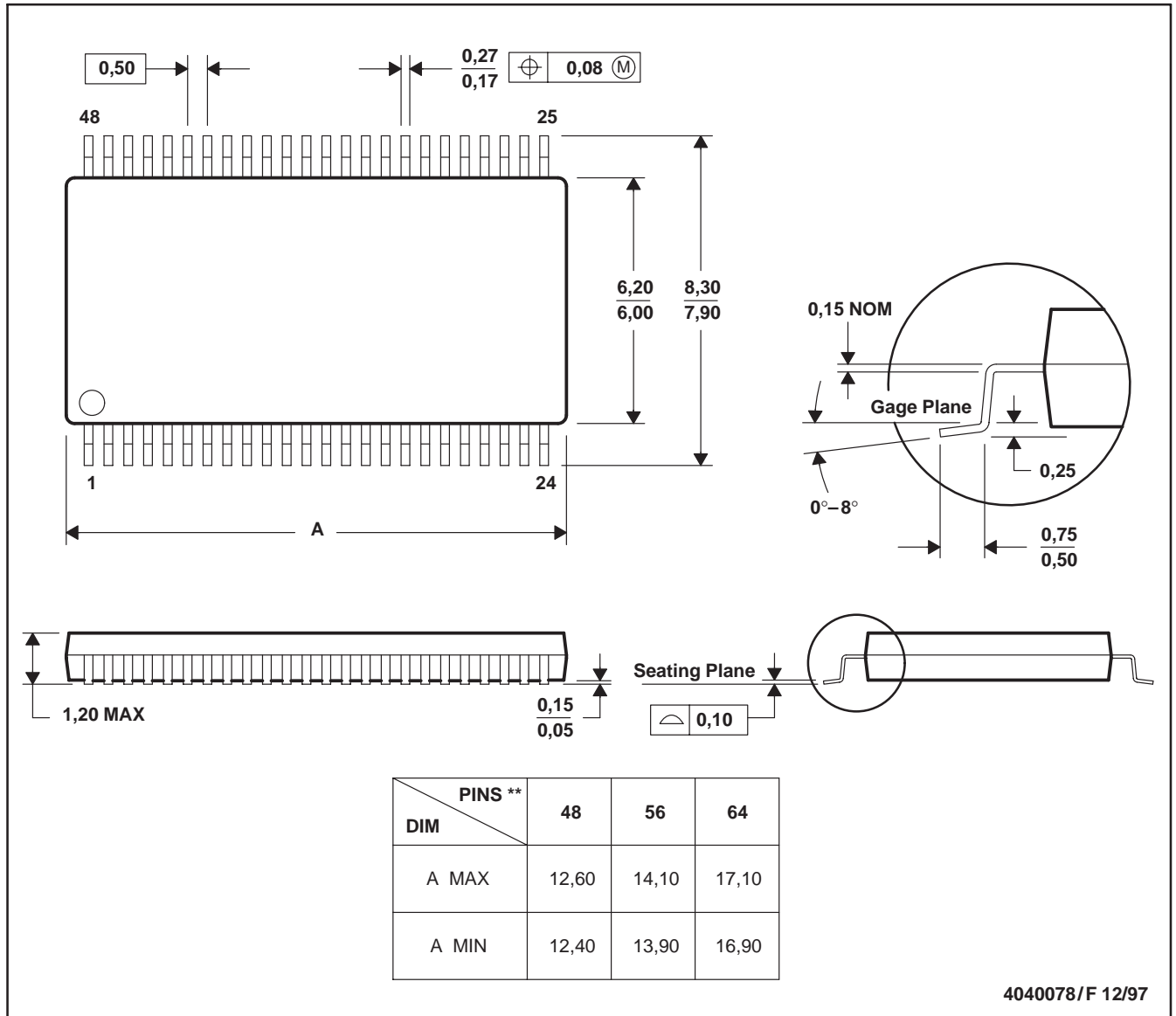
Figure 7. Cycle-to-Cycle Jitter

MECHANICAL DATA

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



- NOTES: B. All linear dimensions are in millimeters.
 C. This drawing is subject to change without notice.
 D. Body dimensions do not include mold protrusion not to exceed 0,15.
 E. Falls within JEDEC MO-153

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC857-2DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC857-2DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0

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