Three-Phase Brushless Motor Driver

Check for Samples: DRV3204-Q1

FEATURES

- **3-Phase Pre-Drivers for N-Channel MOS Field-Effect Transistors (MOSFETs)**
- **Pulse-Width Modulation (PWM) Frequency up to 20 kHz**
- **Fault Diagnostics**
- **Charge Pump**
- **Phase Comparators**
- **Microcontroller (MCU) Reset Generator**
- **Serial Port I/F (SPI)**
- **Motor-Current Sense**
- **5-V Regulator**
- **Low-Current Sleep Mode**
- **Motor Operation VB Range From 5.3 V to 18 V**
- **MCU Operation VB Range From 4.5 V to 18 V**
- **48-Pin PHP**

APPLICATIONS

Automotive

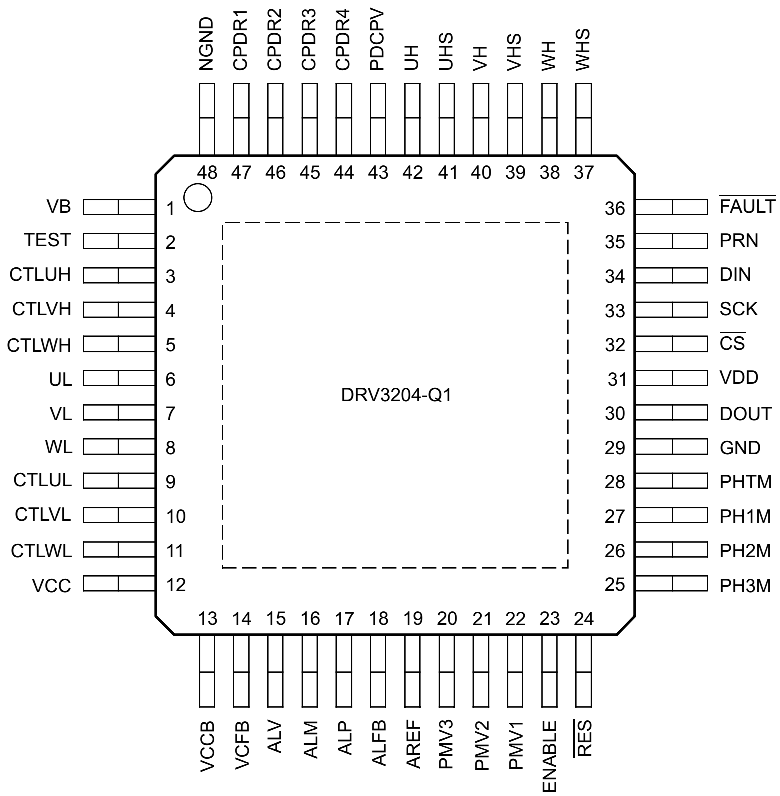
DESCRIPTION

The DRV3204-Q1 device is a field-effect transistor (FET) pre-driver designed for three-phase motor control for applications such as an oil pump or a water pump. The device has three high-side pre-FET drivers and three low-side drivers which are under the control of an external MCU. A charge pump supplies the power for the high side, and there is no requirement for a bootstrap capacitor. For commutation, this integrated circuit (IC) sends a conditional motor signal and output to the MCU. Diagnostics provide undervoltage, overvoltage, overcurrent, overtemperature and power-bridge faults. One can measure the motor current using an integrated current-sense amplifier and comparator in a battery common-mode range, which allows the use of the motor current in a high-side current-sense application. External resistors set the gain. One can configure the pre-drivers and other internal settings through the SPI.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE INFORMATION

48-PIN PHP
(Top View)



PIN FUNCTIONS

PIN			MAXIMUM RATING	FUNCTION
NAME	NO.	TYPE		
ALFB	18	O	–0.3 V–40 V	Motor current-sense amplifier feedback
ALM	16	I	–0.3 V–40 V	Motor current- sense amplifier negative input
ALP	17	I	–0.3 V–40 V	Motor current- sense amplifier positive input
ALV	15	O	–0.3 V–6 V	Motor current- sense amplifier output
AREF	19	O	–0.3 V–40 V	Reference output of motor current- sense amplifier
CPDR1	47	O	–0.3 V–40 V	Charge-pump output
CPDR2	46	O	–0.3 V–40 V	Charge- pump output
CPDR3	45	O	–0.3 V–40 V	Charge- pump output
CPDR4	44	O	–0.3 V–40 V	Charge- pump output
CS	32	I	–0.3 V–6 V	SPI chip select
CTLUH	3	I	–0.3 V–6 V	Pre-driver parallel input
CTLUL	9	I	–0.3 V–6 V	Pre-driver parallel input
CTLVH	4	I	–0.3 V–6 V	Pre-driver parallel input
CTLVL	10	I	–0.3 V–6 V	Pre-driver parallel input
CTLWH	5	I	–0.3 V–6 V	Pre-driver parallel input
CTLWL	11	I	–0.3 V–6 V	Pre-driver parallel input

PIN FUNCTIONS (continued)

PIN			MAXIMUM RATING	FUNCTION
NAME	NO.	TYPE		
DIN	34	I	–0.3 V–6 V	SPI data input
DOUT	30	O	–0.3 V–6 V	SPI data output
ENABLE	23	I	–0.3 V–40 V	Enable input
$\overline{\text{FAULT}}$	36	O	–0.3 V–6 V	Diagnosis output
GND	29	I	–0.3 V–0.3 V	GND
NGND	48	I	–0.3 V–0.3 V	Power GND
PDCPV	43	O	–0.3 V–40 V	Charge pump output
PH1M	27	I	–1 V–40 V	Phase comparator input
PH2M	26	I	–1 V–40 V	Phase comparator input
PH3M	25	I	–1 V–40 V	Phase comparator input
PHTM	28	I	–1 V–40 V	Phase comparator reference input
PMV1	22	O	–0.3 V–6 V	Phase comparator output
PMV2	21	O	–0.3 V–6 V	Phase comparator output
PMV3	20	O	–0.3 V–6 V	Phase comparator output
PRN	35	I	–0.3 V–6 V	Watchdog timer-pulse input
$\overline{\text{RES}}$	24	O	–0.3 V–6 V	MCU reset output
SCK	33	I	–0.3 V–6 V	SPI clock
TEST	2	I	–0.3 V–20 V	TEST input
UH	42	O	–5 V–40 V	Pre-driver output
UHS	41	O	–5 V–40 V	Pre-driver reference
UL	6	O	–0.3 V–20 V	Pre-driver output
VB	1	I	–0.3 V–40 V	VB input
VCC	12	I	–0.3 V–6 V	VCC supply input
VCCB	13	O	–0.3 V–40 V	VCC regulator base driver of PNP external transistor
VCFB	14	I	–0.3 V–40 V	VCC regulator current-sense input
VDD	31	O	–0.3 V–3.6 V	VDD supply output
VH	40	O	–5 V–40 V	Pre-driver output
VHS	39	O	–5 V–40 V	Pre-driver reference
VL	7	O	–0.3 V–20 V	Pre-driver output
WH	38	O	–5 V–40 V	Pre-driver output
WHS	37	O	–5 V–40 V	Pre-driver reference
WL	8	O	–0.3 V–20 V	Pre-driver output

BLOCK DIAGRAM

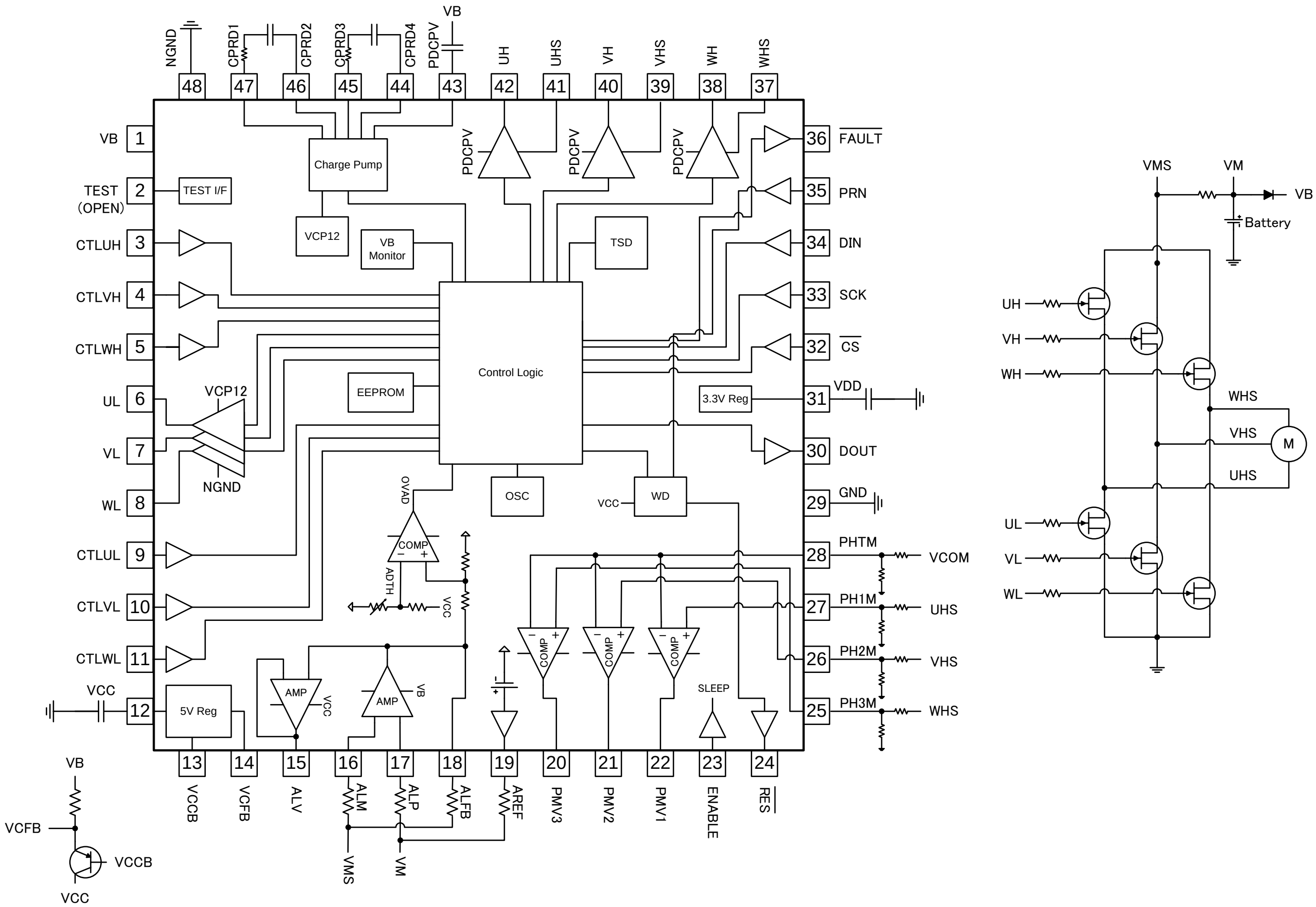


Figure 1. Top Block Diagram

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
ESD(1)					
ESD all pins	ESD performance of all pins to any other pin	HBM model	–2	2	kV
		CDM model	–500	500	V
TEMPERATURE					
T_A	Operating temperature range		–40	125	ºC
T_J	Junction temperature		–40	150	ºC
T_{stg}	Storage temperature		–55	175	ºC

(1) Performance of ESD testing is according to the ACE-Q100 standard.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV3204-Q1 PHP 48 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	26.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	11.5	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	7.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	7.1	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

SUPPLY VOLTAGE AND CURRENT

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUT						
VB1(1)1	VB supply voltage (motor operation)		5.3	12	18	V
VB2(1)1	VB supply voltage (MCU operation)		4.5	12	18	V
Ivb	VB operating current	ENABLE = High, no PWM	—	18	27	mA
Ivbq	VB quiescent current	ENABLE = Low	—	50	100	µA

(1) Performance of supply voltage 5.3 V–18 V is according to the ACE-Q100 (Grade 0) standard.

WATCHDOG

Description

A watchdog monitors the PRN signal and VCC supply level and generates a reset to the MCU via the $\overline{\text{RES}}$ pin if the status of PRN is not normal or VCC is lower than the specified threshold level. Detection of a special pattern on the PRN input during power up can disable the watchdog.

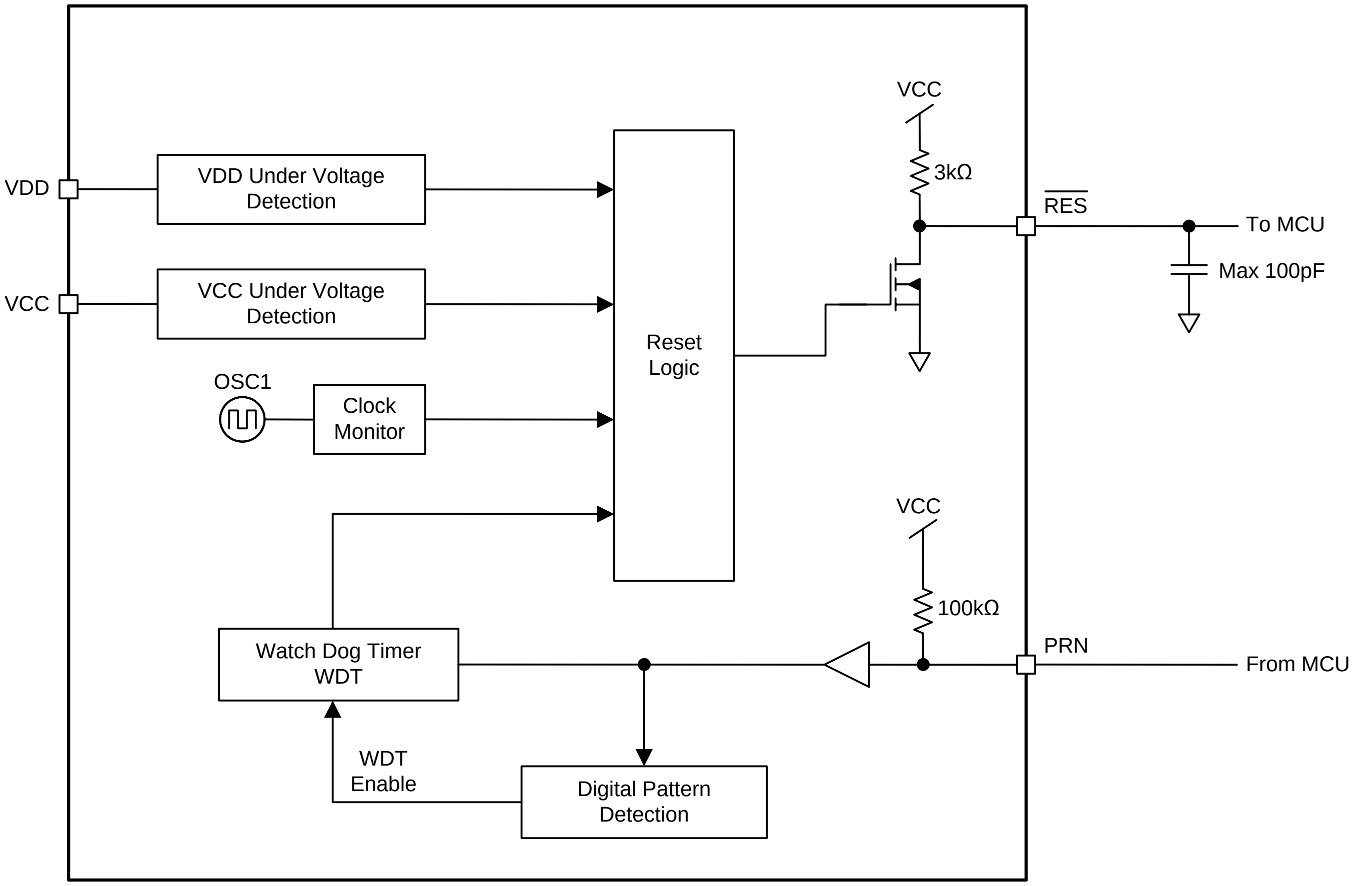
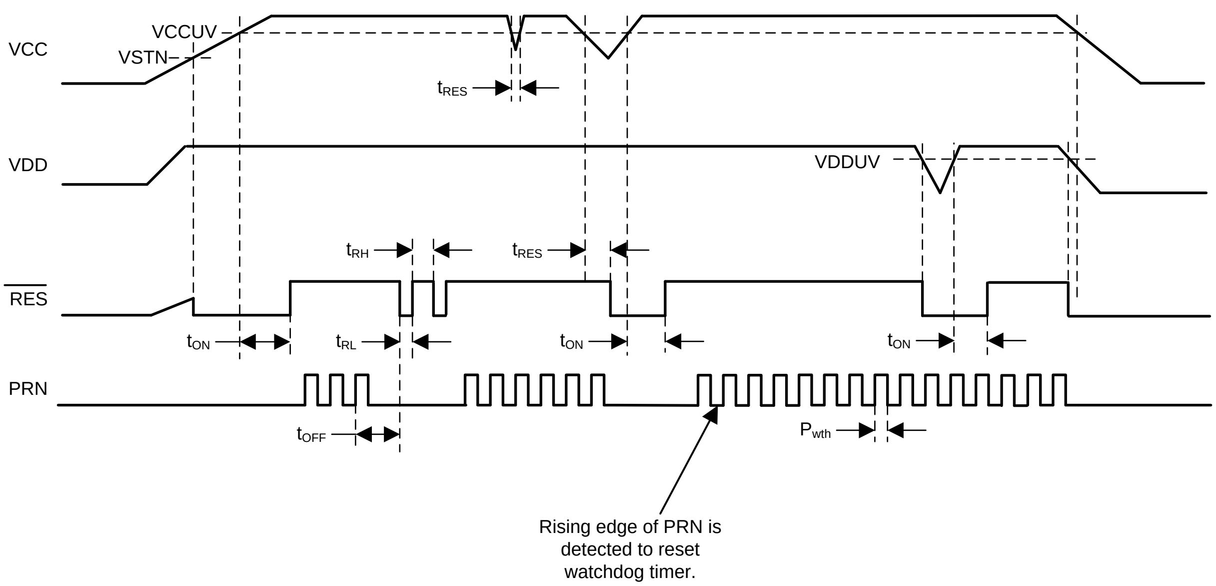


Figure 2. Watchdog Block Diagram



NOTE: VCC undervoltage condition sets RES = Low.

Figure 3. Watchdog Timing Chart

WATCHDOG ELECTRICAL CHARACTERISTICS(1)

VB = 12 V, T_A = –40°C to 125°C, (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG						
VSTN(2)	Function start VCC voltage $\overline{RES}$	See Figure 3	–	0.8	1.3	V
t_{ON}(2)	Power-on time $\overline{RES}$		2.5	3	3.5	ms
t_{OFF}(2)	Clock-off reset time $\overline{RES}$		64	80	96	ms
t_{RL}(2)	Reset-pulse low time $\overline{RES}$		16	20	24	ms
t_{RH}(2)	Reset-pulse high time $\overline{RES}$		64	80	96	ms
t_{RES}(2)	Reset delay time $\overline{RES}$		30	71.5	90	µs
P_{wth}(2)	Pulse duration PRN		2	–	–	µs

(1) The timing parameters are invalid if watch dog timer is disabled.
(2) Specified by design

SERIAL PORT I/F

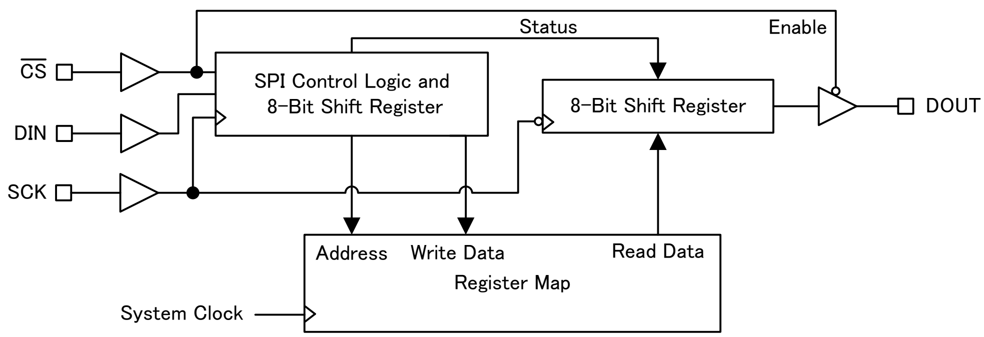


Figure 4. Block Diagram of SPI

Description

Seting device configuration and reading out diagnostic information is via SPI. SPI operates in slave mode. SPI uses four signals according to the timing chart of Figure 5.

$\overline{CS}$ - Chip Select

The MCU uses $\overline{CS}$ to select this IC. $\overline{CS}$ is normally high, and communication is possible only when it is forced low. When $\overline{CS}$ falls, communication between this IC and the MCU starts. The transmitted data are latched and the DOUT output pin comes out of high impedance. When $\overline{CS}$ rises, communication stops. The DOUT output pin goes into high impedance. The next falling edge starts another communication. There is a minimum waiting time between two communications (t_{wait}). The pin has an internal pullup.

SCK – Synchronization Serial Clock

The MCU uses SCK to synchronize communication. SCK is normally low, and the valid clock-pulse number is 16. At each falling edge, the MCU writes a new bit on the DIN input, and this IC writes a new bit on the DOUT output pin. At each rising edge, this IC reads the new bit on DIN, and the MCU reads the new bit on DOUT. The maximum clock frequency is 4 MHz. The pin has an internal pulldown.

DIN – Serial Input Data

DIN receives 16-bit data. The order of received bits is from the MSB (first) to the LSB (last). The pin has an internal pulldown. Update of the internal register with the received bits occurs only if the number of clock pulses is 16 while $\overline{CS}$ is low.

DOUT – Serial Output Data

DOUT transmits 16-bit data. It is a three-state output, and it is in the high-impedance state when $\overline{CS}$ is high. The order of serial data-bit transmission is from the MSB (first) to the LSB (last).

SPI ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SPI						
f_{op}	SPI clock frequency			–	4	MHz
t_{lead} (1)	Enable lead time		200	–	–	ns
t_{wait} (1)	Wait time between two successive communications		5	–	–	µs
t_{lag} (1)	Enable lag time		100	–	–	ns
t_{pw} (1)	SCLK pulse duration		100	–	–	ns
t_{su} (1)	Data setup time		100	–	–	ns
t_h (1)	Data hold time		100	–	–	ns
t_{dis} (1)	Data-output disable time		–	–	200	ns
t_{en} (1)	Data-output enable time		–	–	100	ns
t_v (2)	Data delay time, SCK to DOUT	C_L = 50 pF, see Figure 6.	0	-	100	ns

(1) Specified by design
(2) Specified by design

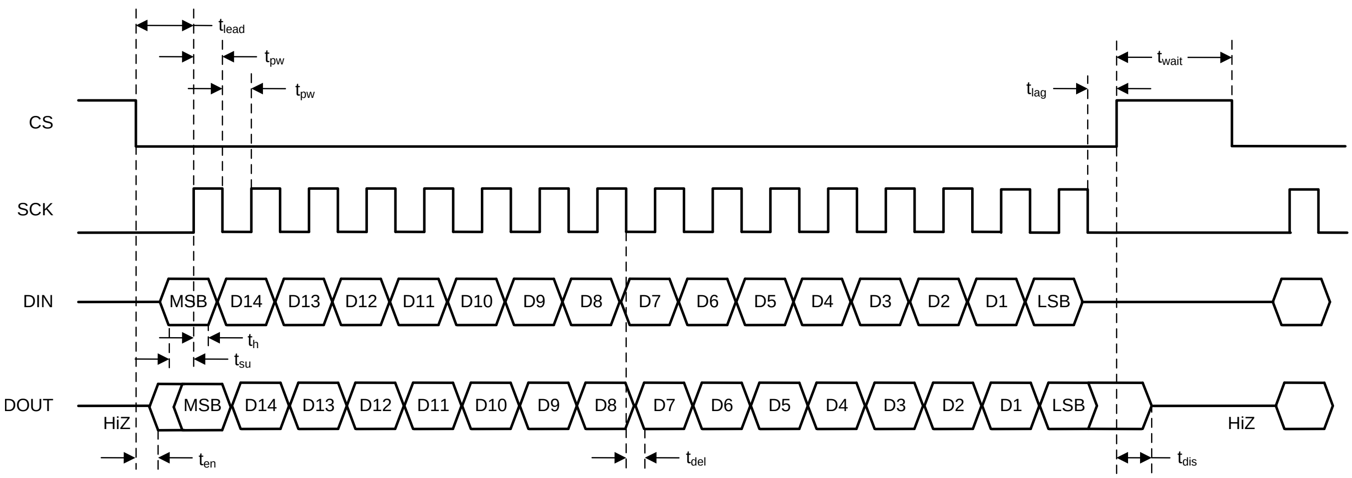


Figure 5. SPI Timing Diagram

Table 1. SPI Serial Input Format

	MSB	D14	D13	D12	D11	D10	D9	D8
DIN	RW[1]	RW[0]	Addr[5]	Addr[4]	Addr[3]	Addr[2]	Addr[1]	Addr[0]
	D7	D6	D5	D4	D3	D2	D1	LSB
DIN	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]

Table 2. SPI Serial Output Data Format

	MSB	D14	D13	D12	D11	D10	D9	D8
DOUT	0	Frame fault	0	0	0	0	0	1
	D7	D6	D5	D4	D3	D2	D1	LSB
DOUT	Data[7]	Data[6]	Data[5]	Data[4]	Data[3]	Data[2]	Data[1]	Data[0]

SPI serial input and output format

RW[1:0] : 01: write mode; 00: read mode

Addr[5:0] : Address of SPI access

Data[7:0] : Input data to write or output data to read
Frame fault : 0: No error exists in the previous SPI frame.
: 1: Error exists in the previous SPI frame.

Table 3. SPI Register Map

<table>
<tr><th>Register Name</th><th>Addr (Hex)</th><th>b7</th><th>b6</th><th>b5</th><th>b4</th><th>b3</th><th>b2</th><th>b1</th><th>b0</th><th>Reset (Hex)</th></tr>
<tr><td>Reserved</td><td>00</td><td colspan="8">RSVD</td><td>00</td></tr>
<tr><td>CFGUNLK</td><td>01</td><td colspan="4">RSVD</td><td colspan="4">CFGUNLK</td><td>00</td></tr>
<tr><td>FLTCFG</td><td>02</td><td>FLGLATCH_EN</td><td colspan="3">MTOCTH</td><td>RSVD</td><td>VCCUVTH</td><td colspan="2">VBUVTH</td><td>00</td></tr>
<tr><td>Reserved</td><td>03</td><td colspan="8">RSVD</td><td>00</td></tr>
<tr><td>FLTEN0</td><td>04</td><td>FE_MTOC</td><td>FE_VCCOC</td><td>FE_VCCOV</td><td>FE_VDDOV</td><td>FE_CPOV</td><td>FE_CPUV</td><td>FE_VBOV</td><td>FE_VBUV</td><td>FF</td></tr>
<tr><td>FLTEN1</td><td>05</td><td colspan="7">RSVD</td><td>FE_TSD</td><td>01</td></tr>
<tr><td>SDNEN0</td><td>06</td><td>SE_MTOC</td><td>SE_VCCOC</td><td>SE_VCCOV</td><td>SE_VDDOV</td><td>SE_CPOV</td><td>SE_CPUV</td><td>SE_VBOV</td><td>SE_VBUV</td><td>FF</td></tr>
<tr><td>SDNEN1</td><td>07</td><td colspan="7">RSVD</td><td>SE_TSD</td><td>01</td></tr>
<tr><td>FLTFLG0</td><td>08</td><td>MTOC</td><td>VCCOC</td><td>VCCOV</td><td>VDDOV</td><td>CPOV</td><td>CPUV</td><td>VBOV</td><td>VBUV</td><td>00</td></tr>
<tr><td>FLTFLG1</td><td>09</td><td colspan="7">RSVD</td><td>TSD</td><td>00</td></tr>
<tr><td>CSCFG</td><td>0A</td><td colspan="5">RSVD</td><td colspan="3">CSOFFSET</td><td>00</td></tr>
<tr><td>PDCFG</td><td>0B</td><td colspan="6">RSVD</td><td colspan="2">DEADT</td><td>00</td></tr>
<tr><td>DIAG</td><td>0C</td><td colspan="5">RSVD</td><td>VCCUVRST</td><td>WDTRST</td><td>CMRST</td><td>00</td></tr>
<tr><td>SPARE</td><td>0D</td><td colspan="6">SPARE</td><td colspan="2">SEL_COMP_HYS</td><td>00</td></tr>
<tr><td>Reserved</td><td>0E–3F</td><td colspan="8">RSVD</td><td>00</td></tr>
</table>

REGISTER DESCRIPTIONS

Access type: R = Read and W = Write.
Reserved register: Read of reserved bits return 0 and write has no effect.

CFGUNLK (address 0x01): Configuration Unlock Register

<table>
<tr><th>Bit</th><th>Name</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>3:0</td><td>CFGUNLK</td><td>RW</td><td>0000</td><td>DRV3204 SPI register map has lock and unlock mode, and it is in lock mode by default. MCU can write values of the following registers in unlock mode;
• FLTCFG
• FLTEN0 and FLTEN1
• SDNEN0 and SDNEN1
• CSCFG
• PDCFG
• WDCFG
In lock mode, read returns the values, but writing the registers have no effect.
Device enters unlock mode by writing 0x5, 0x8, 0x7 to CFGUNLK register in series. Device exits from unlock mode by writing 0x0.</td></tr>
</table>

FLTCFG (address 0x02): Fault Detection Configuration Register

Bit	Name	Type	Reset	Description
7	FLGLATCH_EN	RW	0	Fault-flag (FLTFLG*) latch enable 0: Fault events do not latch fault-flag register bits. 1: Latching of fault-flag register bits by the fault events occurs. The flag bits remain asserted until cleared.
6:4	MTOCTH	RW	000	Motor overcurrent detection threshold 000: 2 V 001: 2.5 V 010: 3 V 011: 3.5 V 100: 4 V Others: 2 V
3	RSVD	R	0	Reserved
2	VCCUVTH	RW	0	VCC undervoltage detection threshold 0: 4 V 1: 4.2 V
1:0	VBUVTH	RW	00	VB undervoltage detection threshold 00: 4 V 01: 4.5 V 10: 5 V 11: 5.5 V

FLTEN0 (address 0x04): FAULT Pin Enable Register 0

Bit	Name	Type	Reset	Description
7	FE_MTOC	RW	1	FAULT pin enable of FLTFLG0 register bits. 0: Assertion of the FAULT pin does not occur when the fault flag bit is 1 1: Assertion of the FAULT pin to low level occurs when the fault flag bit is 1. See Figure 6
6	FE_VCCOC	RW	1	
5	FE_VCCOV	RW	1	
4	FE_VDDOV	RW	1	
3	FE_CPOV	RW	1	
2	FE_CPUV	RW	1	
1	FE_VBOV	RW	1	
0	FE_VBUV	RW	1	

FLTEN1 (address 0x05): FAULT Pin Enable Register 1

Bit	Name	Type	Reset	Description
7:1	RSVD	R	0000 000	Reserved
0	FE_TSD	RW	1	FAULT pin enable of TSD flag bit 0: Assertion of the FAULT pin does not occur when the fault flag bit is 1 1: Assertion of the FAULT pin to low level occurs when the TSD flag bit is 1. See Figure 6

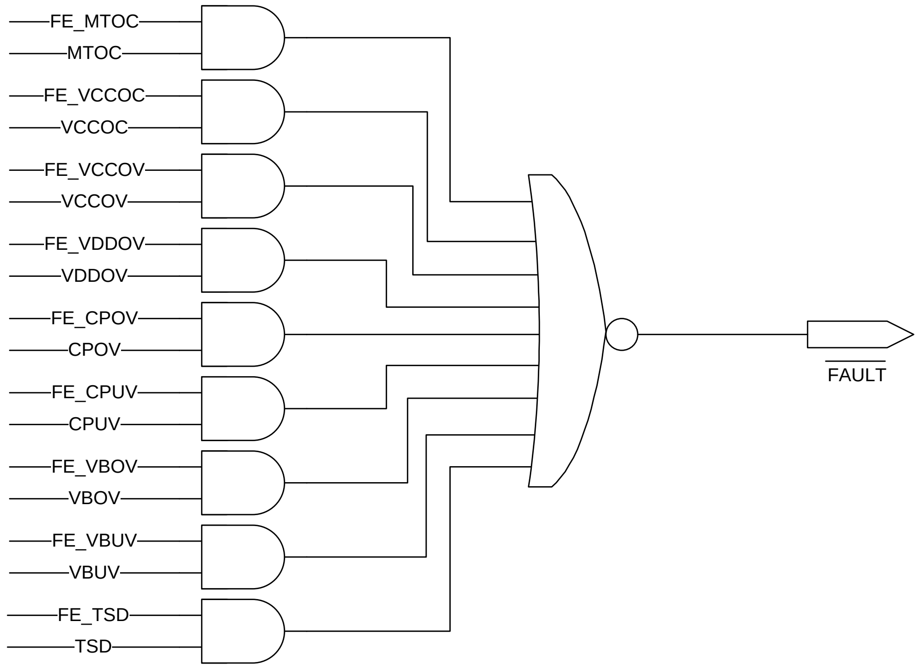


Figure 6. FAULT Pin Enable Logic

SDNEN0 (address 0x06): Pre-Driver Shutdown Enable Register 0

Bit	Name	Type	Reset	Description
7	SE_MTOC	RW	1	Pre-driver shutdown enable of FLTFLG0 register bits 0: Disabling of the pre-driver outputs does not occur when the fault flag bit is 1. 1: Disabling of the pre-driver outputs occurs when the fault flag bit is 1. Both the high-side and low-side FETs turn off. See Figure 7.
6	SE_VCCOC	RW	1	
5	SE_VCCOV	RW	1	
4	SE_VDDOV	RW	1	
3	SE_CPOV	RW	1	
2	SE_CPUV	RW	1	
1	SE_VBOV	RW	1	
0	SE_VBUV	RW	1	

SDNEN1 (address 0x07): Pre-Driver Shutdown Enable Register 1

Bit	Name	Type	Reset	Description
7:1	RSVD	R	0000 000	Reserved
0	SE_TSD	RW	1	Pre-driver shutdown enable of TSD flag bits 0: Disabling of the pre-driver outputs does not occur when the TSD flag bit is 1. 1: Disabling of the pre-driver outputs occurs when the TSD flag bit is 1. Both the high-side and low-side FETs turn off. See Figure 7.

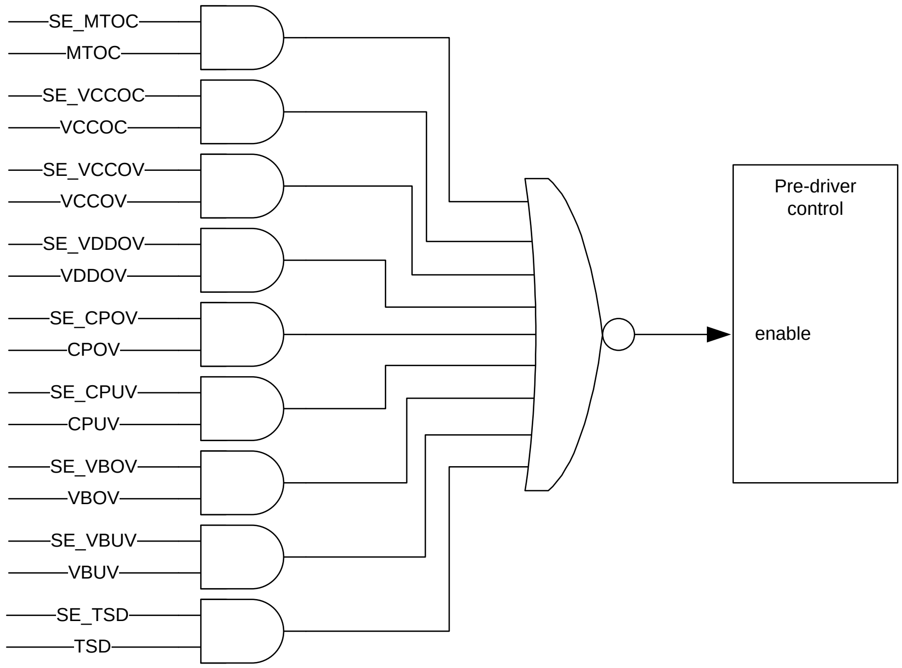


Figure 7. Pre-Driver Shutdown Logic

FLTFLG0 (address 0x08): Fault Flag Register 0

Bit	Name	Type(1)	Reset	Description
				Fault flag bits of the following conditions;(2)
7	MTOC	RW	0	MTOC: Motor overcurrent. (OVAD)
6	VCCOC	RW	0	VCCOC: VCC overcurrent
5	VCCOV	RW	0	VCCOV: VCC overvoltage
4	VDDOV	RW	0	VDDOV: VDD overvoltage
3	CPOV	RW	0	CPOV: Charge-pump overvoltage
2	CPUV	RW	0	CPUV: Charge-pump undervoltage
1	VBOV	RW	0	VBOV: VB overvoltage
0	VBUV	RW	0	VBUV: VB undervoltage If FLTCFG.FLGLATCH_EN = 1 0: Read = No fault condition exists since last cleared. Write = No effect 1: Read = Fault condition exists. Write = Clear the flag. If FLTCFG.FLGLATCH_EN = 0 0: Read = No fault condition Write = No effect 1: Read = Fault condition Write = No effect

(1) R: Read, W: Write
(2) Assertion of the fault flags may occur during power up.

FLGFLT1 (address 0x09): Fault Flag Register 1

Bit	Name	Type (1)	Reset	Description
7:1	RSVD	R	0000 000	Reserved
0	VBUV	RW	1	Fault flag bit of thermal shutdown condition. (2) If FLTCFG.FLGLATCH_EN = 1 0: Read = No fault condition exists since last cleared. Write = No effect 1: Read = Fault condition exists. Write = Clear the flag If FLTCFG.FLGLATCH_EN = 0 0: Read = No fault condition Write = No effect 1: Read = Fault condition Write = No effect

(1) R: Read, W: Write
(2) Assertion of the fault flags may occur during power up.

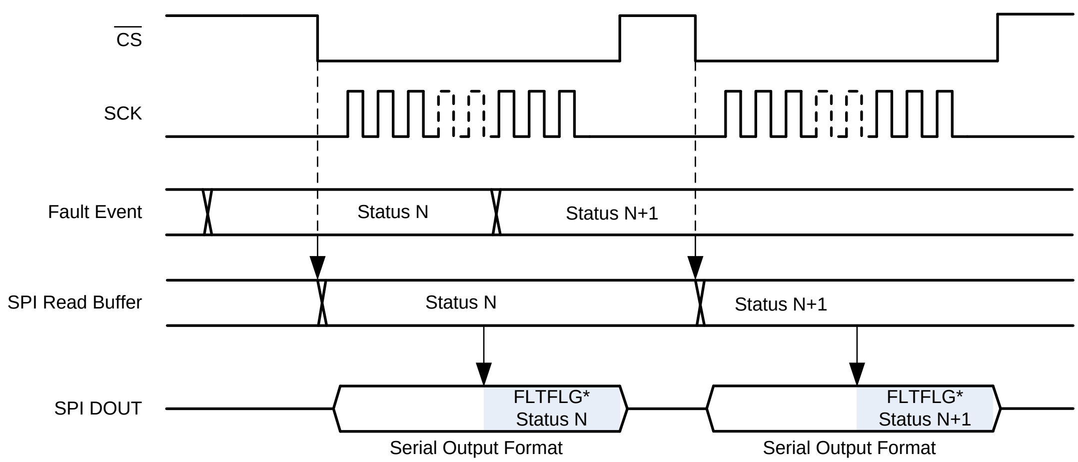
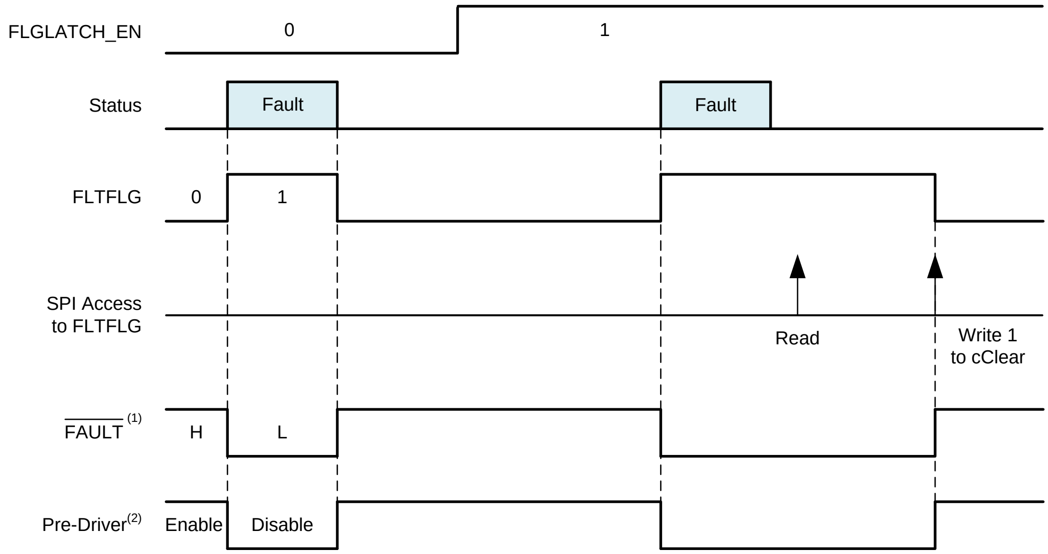


Figure 8. SPI Data-Out Timing Chart of Fault Flag Registers



(1) Assertion of FAULT occurs if FLTEN = 1.

(2) Disabling of pre-driveroccurs if SDNEN = 1.

Figure 9. FLGFLG and FLGLATCH_EN

CSCFG (address 0x0A): Current Sense Configuration Register

Bit	Name	Type (1)	Reset	Description
7:3	RSVD	R	0000 0	Reserved
2:0	CSOFFSET	RW	000	Current-sense offset 000: 0.5 V 001: 1 V 010: 1.5 V 011: 2 V 100: 2.5 V Others: 0.5 V

(1) R: Read W: Write

PDCFG (address 0x0B): Pre-Driver Configuration Register

Bit	Name	Type (1)	Reset	Description
7:2	RSVD	R	0000 00	Reserved
1:0	DEADT	RW	00	Dead time (= t_{dead}) 00: 2 µs 01: 1.5 µs 10: 1 µs 11: 0.5 µs The actual dead time has ±0.2 µs variation from the typical value.

(1) R: Read W: Write

DIAG (address 0x0C): Diagnosis Register

Bit	Name	Type	Reset	Description
7:3	RSVD	R	0000 0	Reserved
2	VCCUVRST	R	0	nRES reset source information
1	WDTRST	R	0	Bit 2 = VCCUVRST - VCC undervoltage
0	CMRST	R	0	Bit 1 = WDTRST - watchdog timer

Bit	Name	Type	Reset	Description
				Bit 0 = CMRST - clock monitor 0: Read = Reset has not occurred. Write = No effect 1: Read = A corresponding reset source caused the last reset condition. Write = No effect Read access to this register clears the bits.

SPARE (address 0x0D): Spare Register

Bit	Name	Type (1)	Reset	Description
7:2	SPARE	RW	000000	Spare registers for future use. Read and write have no effect.
1:0	SEL_COMP_HYS	RW	00	Select phase comparator hysteresis voltage. The following show the typical values. 00: 0 V 01: 25 mV 10: 50 mV 11: 100 mV

(1) R: Read W: Write

CHARGE PUMP

Description:

The charge-pump block generates a supply for the high-side and low-side pre-drivers to maintain the gate voltage on the external FETs. Use of an external storage capacitor (CCP) and bucket capacitors (C1, C2) supports pre-driver slope and switching-frequency requirements. R1 and R2 can reduce switching current if required. The charge pump has voltage-supervisor functions such as over- and undervoltage, and selectable stop conditions for pre-drivers.

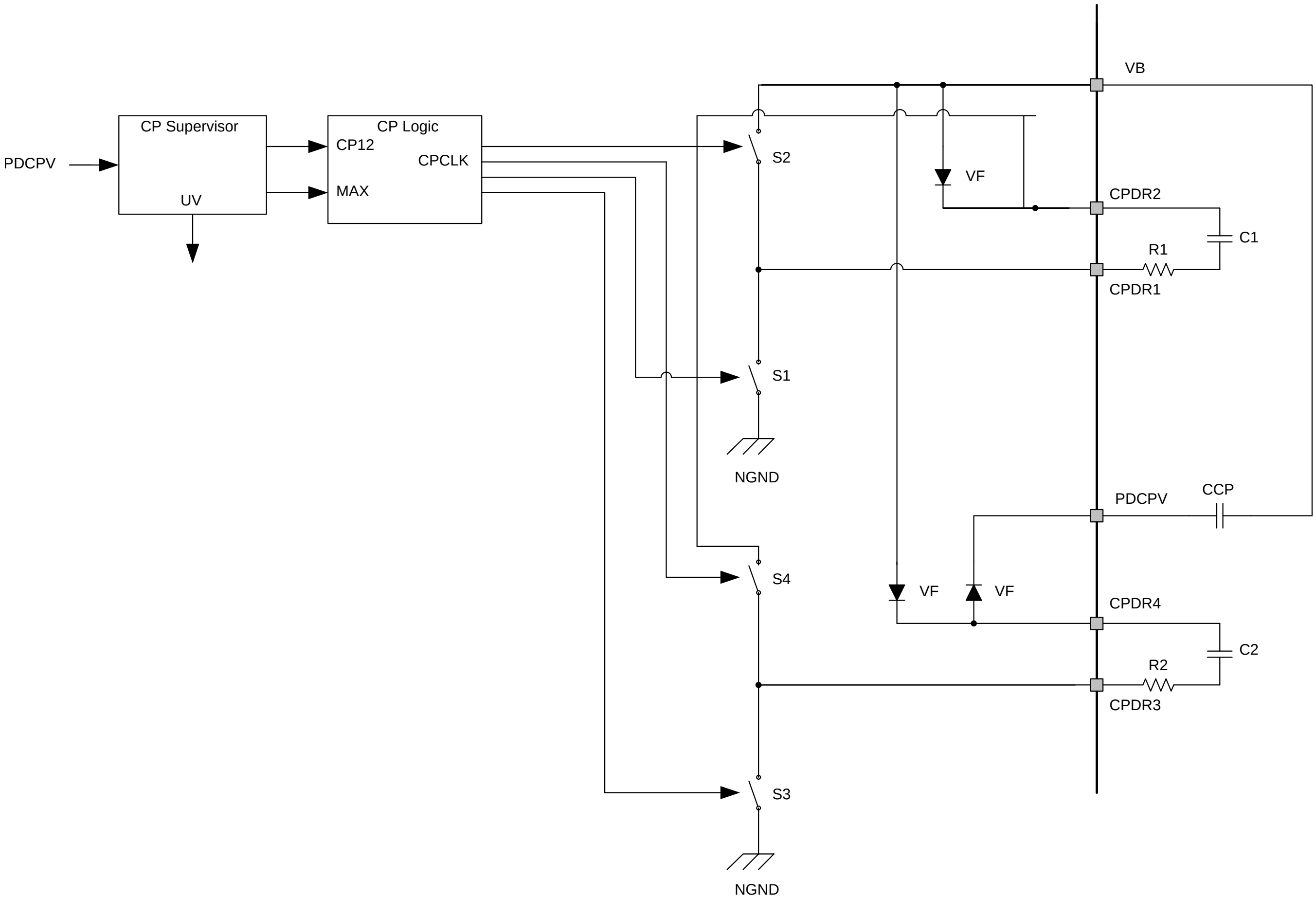


Figure 10. Charge-Pump Block Diagram

Table 4. Charge-Pump Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = -40°C to 125℃ (unless otherwise specified)						
CHARGE PUMP						
Vchv1_0	Output voltage	VB = 5.3 V, Iload = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+7	VB+8	–	V
Vchv1_1	Output voltage	VB = 5.3 V, Ioad = 5 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+5.5	VB+6.5	–	V
Vchv1_2	Output voltage	VB = 5.3 V, Ioad = 8 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+4.5	VB+5.5	–	V
Vchv2_0	Output voltage	VB = 12V, Ioad = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+10	VB+12	VB+14	V
Vchv2_1	Output voltage	VB = 12 V, Ioad = 11 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+9.5	VB+11.5	VB+13.5	V
Vchv2_2	Output voltage	VB = 12 V, Ioad = 18 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+9	VB+11	VB+13	V
Vchv3_0	Output voltage	VB = 18 V, Ioad = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+10	VB+12	VB+14	V
Vchv3_1	Output voltage	VB = 18 V, Ioad = 13 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+10	VB+12	VB+14	V
Vchv3_2	Output voltage	VB = 18 V, Ioad = 22 mA, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω	VB+10	VB+12	VB+14	V
VchvOV	Overvoltage detection threshold		35	37.5	40	V

Table 4. Charge-Pump Electrical Characteristics (continued)

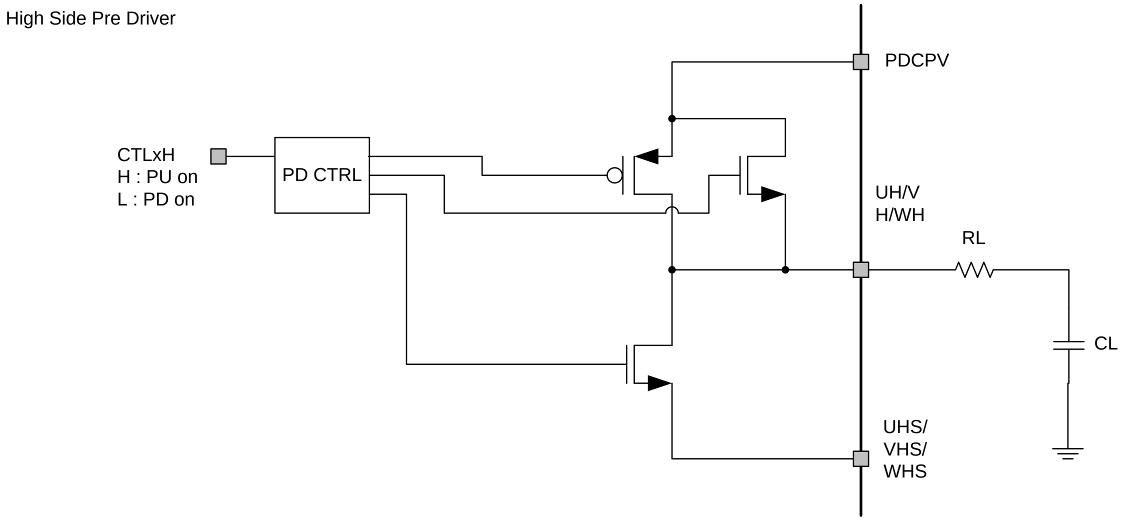
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VchvUV	Undervoltage detection threshold		VB+4	VB+4.5	VB+5	V
t_{chv} (1)	Rise time	VB = 5.3 V, C1 = C2 = 47 nF, CCP = 2.2 µF, R1 = R2 = 0 Ω, Vchv, UV released		1	2	ms
Ron	On-resistance, S1–S4	See Figure 10		8		Ω

(1) Specified by design

Pre-Driver

Description:

The pre-driver block provides three high-side pre-drivers and three low-side pre-drivers to drive external N-channel MOSFETs. The turnon side of the high-side pre-drivers supplies the large N-channel transistor current for quick charge, and PMOS supports output voltages up to PDCPV. The turnoff side of the high-side pre-drivers supplies the large N-channel transistor current for quick discharge. The low-side pre-drivers supply the large N-channel transistor current for charge and discharge. VCP12 (created by a charge pump) controls the output voltage of the low-side pre-driver to output less than 18 V. The pre-driver has a stop condition in some fault conditions (*Fault Detection*) and SPI set (*Serial Port I/F*).



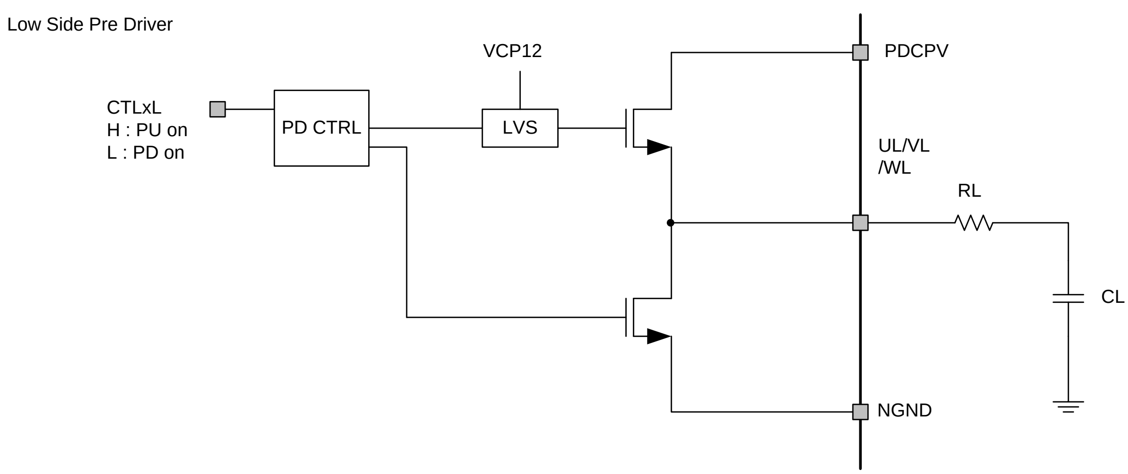


Figure 11. Pre-Driver Block Diagram

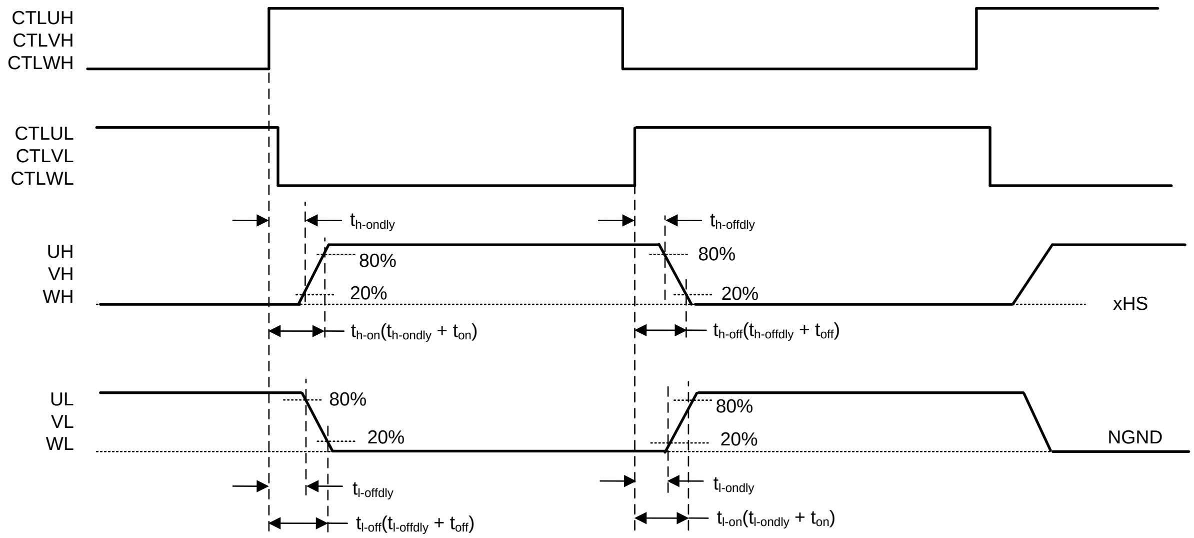
Table 5. Pre-Driver Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V unless otherwise stated, T_A = -40°C to 125℃, unless otherwise specified						
HIGH-SIDE PRE-DRIVER						
VOH_H	Output voltage, turnon side	Isink =10 mA, PDCPV - xH		1.35	2.7	V
VOL_H	Output voltage, turnoff side	Isource = 10 mA, xH - xHS		25	50	mV

Table 5. Pre-Driver Electrical Characteristics (continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RONH_HP	On-resistance, turnon side (Pch)	U(V/W)H = PDCPV – 1 V		135	270	Ω
RONH_HN	On-resistance, turnon side (Nch)	U(V/W)H = PDCPV – 2.5 V		4	8	Ω
RONL_H	On-resistance turnoff side			2.5	5	Ω
t_{on_h1} (1)	Turnon time	C_L = 12 nF, R_L = 0 Ω from 20% to 80%	50	–	200	ns
t_{off_h1} (1)	Turnoff time	C_L = 12 nF, R_L = 0 Ω from 80% to 20%	50	–	200	ns
$t_{h\text{-}ondly1}$ (1)	Output delay time	C_L = 12 nF, R_L = 0 Ω to 20%, no dead time	–	200	–	ns
$t_{h\text{-}offdly1}$ (1)	Output delay time	C_L = 12 nF, R_L = 0 Ω to 80%, no dead time	–	200	–	ns
VGS_hs	Gate-source high -side voltage difference	xH-xHS	–0.3		18	V
LOW-SIDE PRE-DRIVER						
VOH_L1	Output voltage, turnon side	VB = 12 V, Isink =1 0 mA, xL -NGND	10	12	14	V
VOH_L2	Output voltage, turnon side	VB = 5.3 V, Isink = 10 mA, xL - NGND	5.5	7.5	10	V
VOL_L	Output voltage, turnoff side	Isource = 10 mA, xL - NGND	–	25	50	mV
RONH_L	On-resistance, turnon side		–	6	12	Ω
RONL_L	On-resistance, turnoff side			2.5	5	Ω
t_{on_l} (2)	Turnon time	C_L = 18 nF, R_L = 0 Ω, from 20% to 80% of 12 V, from 20% to 80% of 6 V (VB = 5.3 V)	50	–	200	ns
t_{off_h} (2)	Turnoff time	C_L = 18 nF, R_L = 0 Ω, from 80% to 20% of 12 V, from 80% to 20% of 6 V (VB = 5.3 V)	50	–	200	ns
$t_{l\text{-}ondly}$ (2)	Output delay time	C_L = 18 nF, R_L = 0 Ω, to 20% of 12 V, to 20% of V_{OH} = 6 V (VB = 5.3 V), no dead time	–	200	–	ns
$t_{l\text{-}offdly}$ (2)	Output delay time	C_L = 18 nF, R_L = 0 Ω, to 80% of 12 V, to 80% of V_{OH} = 6 V (VB = 5.3 V), no dead time	–	200	–	ns
t_{diff1} (2)	Differential time1	(Th-on) – (Tl-off), no dead time, See Figure 12	–200	0	200	ns
t_{diff2} (2)	Differential time2	(Tl-on) – (Tl-off), no dead time, See Figure 12	–200	0	200	ns
t_{dead} (2)	Dead time	OSC1 = 10 MHz SPI register PDCFG.DEADT	2 1.5 1 0.5		2.2 1.7 1.2 0.7	µs

(1) Specified by design
(2) Specified by design



NOTE: This diagram excludes dead time to explain the timing parameters of the pre-driver.

Figure 12. Delay Time From Input to Output

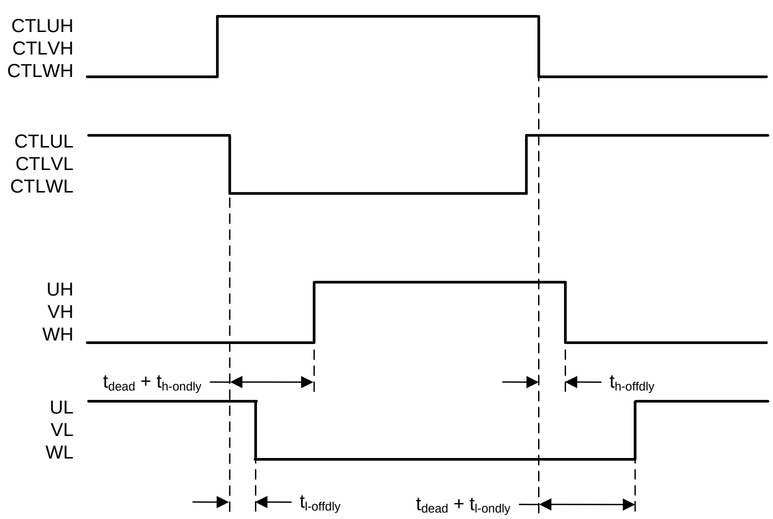


Figure 13. Dead Time

Phase Comparator

Description:

The three-channel comparator module monitors the external FETs by detecting the drain-source voltage across the high-side and low-side FETs. PHTM is the threshold level of the comparators usable for sensorless communication. Figure 14 shows an example of the threshold level.

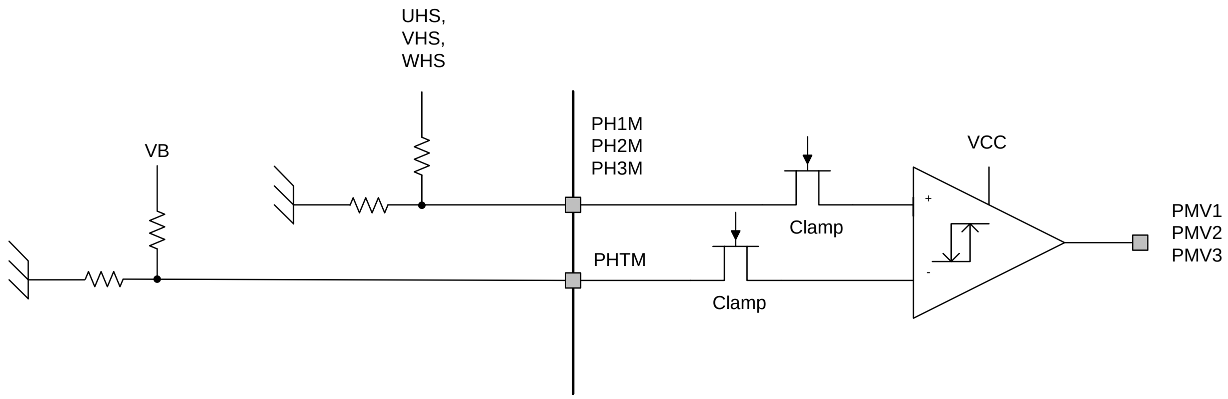


Figure 14. Phase Comparator Block Diagram

Table 6. Phase Comparator Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = –40°C to 125℃ (unless otherwise specified)						
PHASE COMPARTOR						
Viofs	Input offset voltage		–15	–	15	mV
Vinm	Input voltage range, PHTM		1.3	–	4.5	V
Vinp	Input voltage range, PHxM		–1	–	VB	V
Vhys	Threshold hysteresis voltage	SPI register SPARE. SEL_COMP_HYS	–	0	–	mV
			12.5	25	50	
			25	50	100	
			50	100	200	
V_{OH}	Output high voltage	Isink = 2.5 mA	0.9×VCC	–	–	V
V_{OL}	Output low voltage	Isource = 2.5 mA	–	–	0.1×VCC	V
t_{res_tr} (1)	Response time, rising	C_L = 100 pF	–	0.7	1.5	µs
t_{res_tf} (1)	Response time, falling	C_L = 100 pF	–	0.7	1.5	µs

(1) Specified by design

Motor-Current Sense

Description:

Operational amplifier is operating with an external resistor network for higher flexibility to adjust the current measurement to application requirements. The first-stage amplifier is operating with the external resistor and the output voltage up to VB at ALFB. The gain of amplifier is adjustable by external resistors from ×10 to ×30. The second-stage amplifier is buffer to MCU at ALV. Current sense has comparator for motor overcurrent (OVAD). ADTH is overcurrent threshold level and set value by SPI. Figure 15 shows the curve of detection level. ALFB is divided by 2 and compare this value with ADTH. In recommended application, zero-point adjustment is required as large error offset in initial condition.

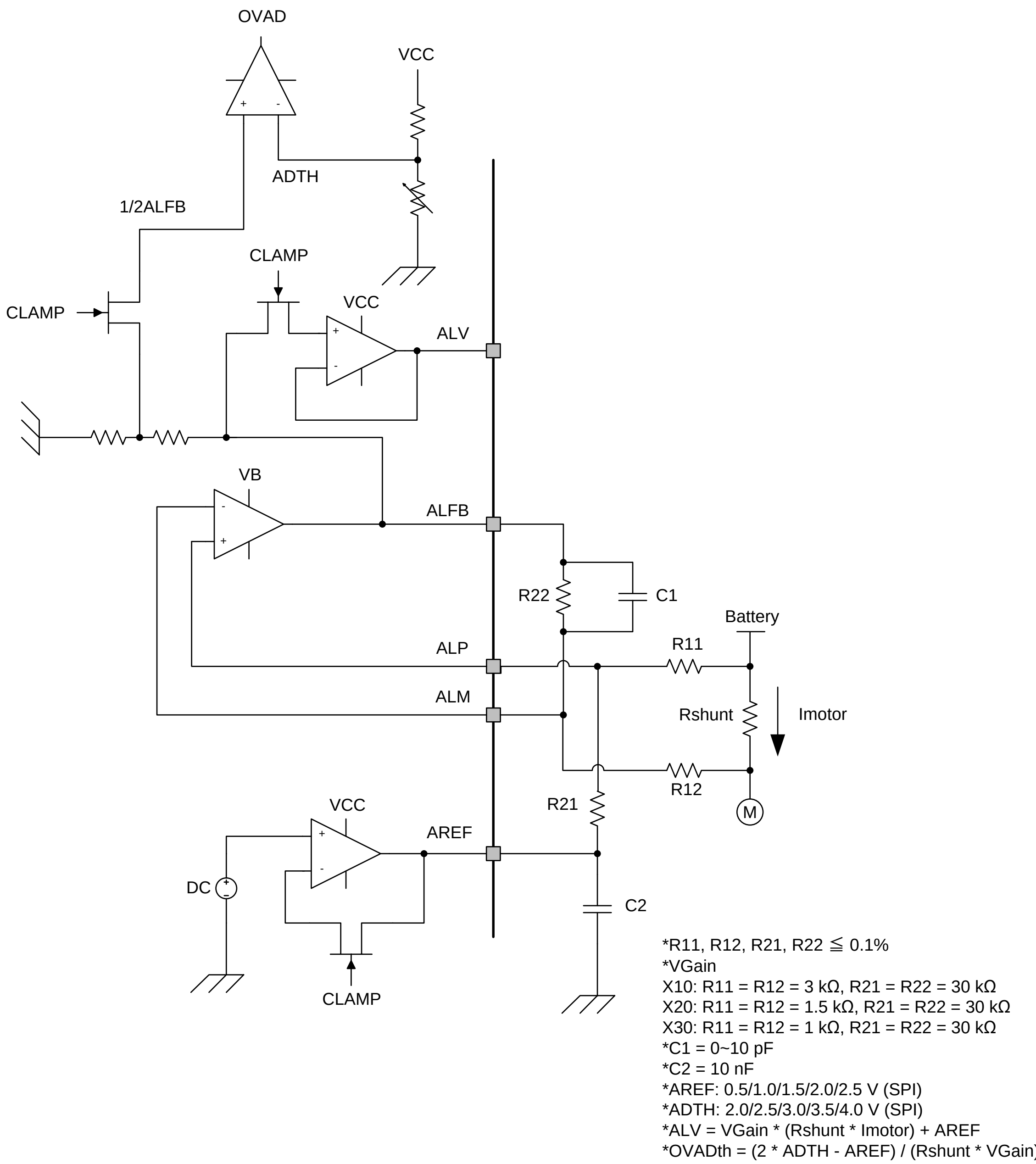


Figure 15. Motor Current-Sense Block Diagram

Table 7. Motor Current-Sense Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = –40°C to 125℃ (unless otherwise specified)						
MOTOR CURRENT SENSE						
VOfs	Input offset voltage		–5		5	mV
VO_0	Output voltage, ALV	Imotor = 0 A, SPI register CSCFG. CSOFFSET	–	0.5 1 1.5 2 2.5	–	V
VLine	Linearity, ALV	Rshunt = 1 mΩ, R11 = R12 = 1 kΩ, R21 = R22 = 30 kΩ	29.4	30	30.6	mV/A
VGain	Gain		10		30	
Tset_TR1[1]	Settling time (rise), ALV ±1%	Rshunt = 1 mΩ, VGain = 30, C_L = 100 pF, Imotor = 0 A → 30 A, (ALV: 1 V → 1.9 V, AREF = 1 V)	–	1	2.5	µs
Tset_TR2[2]	Settling time(rise), ALV ±1%	Rshunt = 1 mΩ, VGain = 30, C_L = 100 pF, Imotor = 0 A → 100 A, (ALV: 1 V → 4 V, AREF = 1 V)	–	1	2.5	µs
Tset_TF1[2]	Settling time(fall), ALV ±1%	Rshunt = 1 mΩ, VGain = 30, C_L = 100 pF, Imotor = 30 A→0, (ALV: 1.9 V → 1 V, AREF = 1 V)	–	1	2.5	µs
Tset_TF2[2]	Settling time(fall), ALV ±1%	Rshunt = 1 mΩ, VGain = 30, C_L = 100 pF, Imotor = 100 A→0, (ALV: .4 V → 1 V, AREF = 1 V)	–	1	2.5	µs
OVADth	Overcurrent threshold	Rshunt = 1 mΩ, VGain = 30, AREF = 1.0V, ADTH = 2.5 V, SPI register FLTCFG. MTOCTH, OVADth = (2 × ADTH -– AREF) / (Rshunt × VGain)	119.7	133	146.3	A
TDEL_OVAD[2]	Propagation delay (rise or fall)		–	–	1.5	µs
tfiltMTOC	filtering time	OSC1 = 9 MHz–11 MHz	0.8	1	1.2	µs

(1) Specified by design
(2) Specified by design

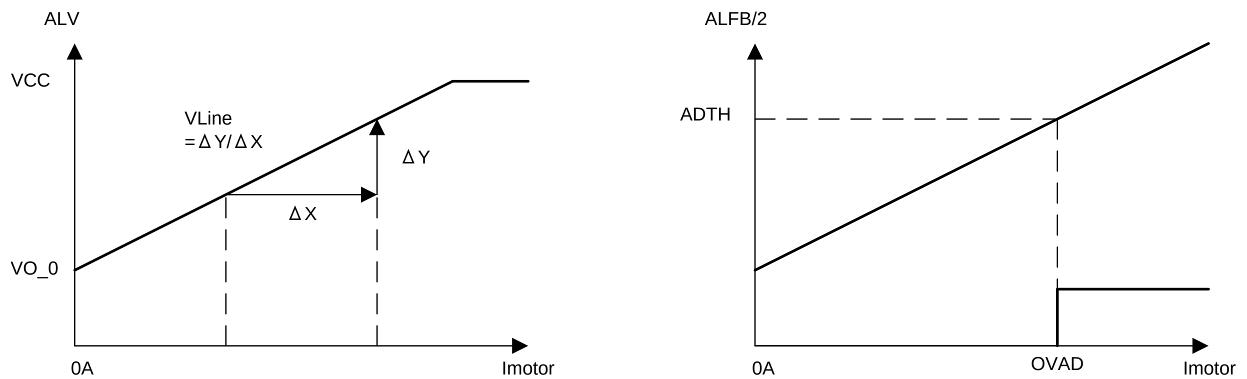
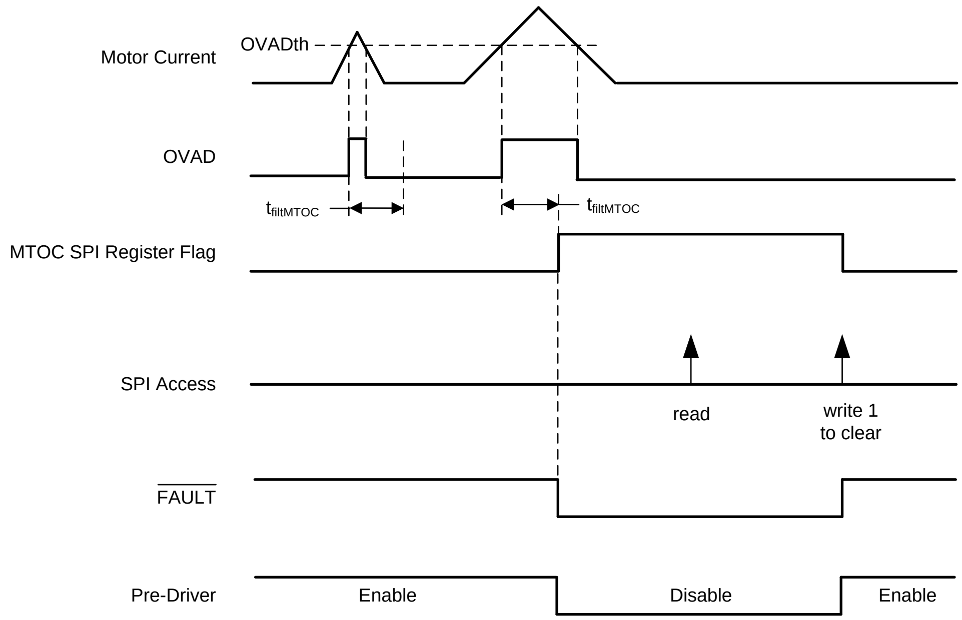


Figure 16. Motor Current Sense and Overcurrent



(1) MCU must set the FLTCFG.FLGLATCH_EN bit to 1 to get the latch-type operation shown in this figure.

(2) When MTOC condition is detected, $\overline{\text{FAULT}}$ is asserted to low if FE_MTOC bit is 1.

(3) When MTOC condition is detected, Pre Driver is disabled if SE_MTOC is 1.

Figure 17. Motor Overcurrent Event

Regulators

Description:

The regulator block offers 5v LDO and 3.3v LDO. The VCC LDO regulates VB down to 5v with an external PNP controlled by the regulator block. This 5V is supplied to MCU and other components.

The VDD regulator regulates VB down to 3.3V with internal FET and controller. The 5V LDO is protected against short to GND fault. Overvoltage and under voltage events of both supplies are detected. The under voltage of the 5V LDO is set by SPI.

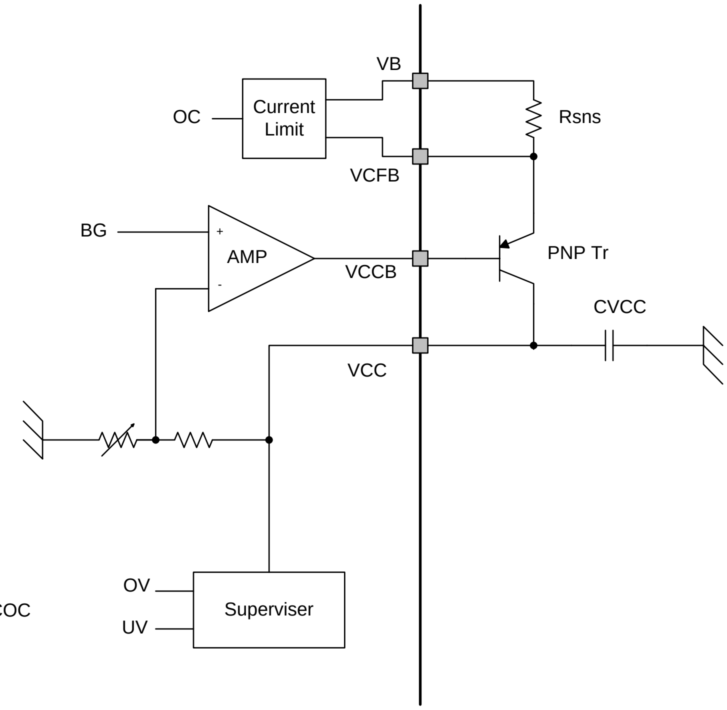


Figure 18. VCC Block Diagram (External Driver)

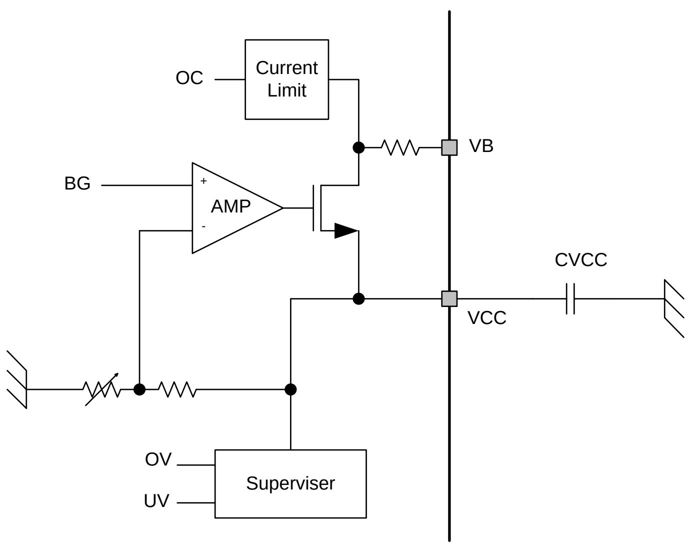


Figure 19. VDD Block Diagram

Table 8. VCC and VDD Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = –40°C to 125℃ (unless otherwise specified)						
VCC						
VCC1	Output Voltage		4.9	5	5.1	V
VCC2	Output Voltage	VB = 4.5 V, ILVCC = 5 mA–150 mA	4.25		4.5	V
IBVCC	Base Current		1.5			mA
hfePNP	DC current gain of external PNP		100	–	–	

Table 8. VCC and VDD Electrical Characteristics (continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VLRVCC	Load regulation	ILVCC = 5 mA–150 mA	–20	–	20	mV
CVCC	External Capacitance		22		100	µF
RVCC	ESR of external Capacitor				300	mΩ
VCCUV	Under voltage detection threshold	SPI register FLTCFG. VCCUVTH	3.7 3.9	4 4.2	4.3 4.5	V
VCCUVHYS	Under voltage detection threshold hysteresis		50	100	200	mV
VCCOV	Overvoltage detection threshold		6	6.5	7	V
VCCOC	Current Limit	Rsns=0.51Ω, 0.2V=Rsns[(1)], VCCOC	300	400	550	mA
Tvcc1[(2)]	Rise Time	VCC > VCCUV, CVCC=22µF			0.5	ms
Tvcc2[(2)]	Rise Time	VCC > VCCUV, CVCC=100µF			1.5	ms
VDD						
VDD	Output Voltage		3	3.3	3.6	V
CVDD	Load Capacitance			1		µF
VDDUV	Under voltage detection threshold		2.1	2.3	2.5	V
VDDOV	Overvoltage detection threshold		4	4.3	4.6	V
Tvdd[(3)]	Rise Time	VDD > VDDUV, CVDD=1µF			100	µs

(1) No variation of the external components
(2) Specified by design
(3) Specified by design

VB Monitor

Description:

The VB monitoring system has two comparators for under- and overvoltage, and has pre-driver stop controlling system respectively. Overvoltage provides pre-driver stop condition selectable (SPI control). On the other hand, under voltage must stop pre-driver operation under detection (no selectable). System should return to normal operation automatically after undetected level.

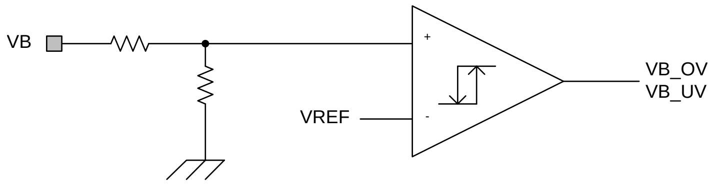


Figure 20. VB Monitor Block Diagram

Table 9. Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)						
VB MONITOR						
VBOV	VB overvoltage detection threshold level		26.5	27.5	28.5	V
VBUV	VB Undervoltage detection threshold level	SPI register FLTCFG. VBUVTH	3.65 4.15 4.65 5.15	4 4.5 5 5.5	4.35 4.85 5.35 5.85	V

Thermal Shut Down

Description:

The device has temperature sensors that produce pre-driver stop condition if the chip temperature exceeds 175 degree.

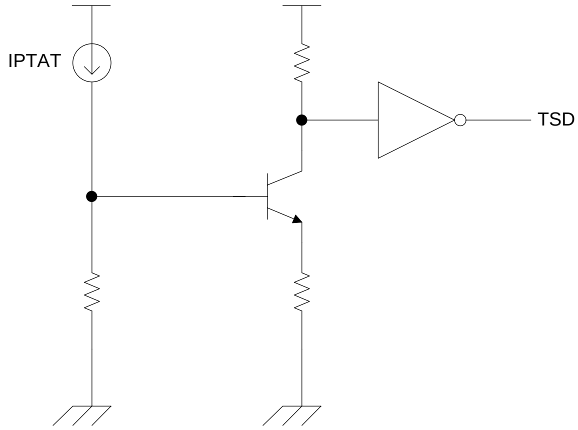


Figure 21. Thermal Shutdown Block Diagram

Table 10. Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)						
THERMAL SHUT DOWN						
TSD (1)	Thermal shut down threshold level		155	175	195	°C

(1) Specified by design

Table 10. Electrical Characteristics (continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TSDhys(1)	Thermal shut down hysteresis		5	10	15	°C

Oscillator

Description:

Oscillator block generates two 10-MHZ clock signals. OSC1 is the primary clock used for internal logic synchronization and timing control. OSC2 is the secondary clock used to monitor the status of OSC1.

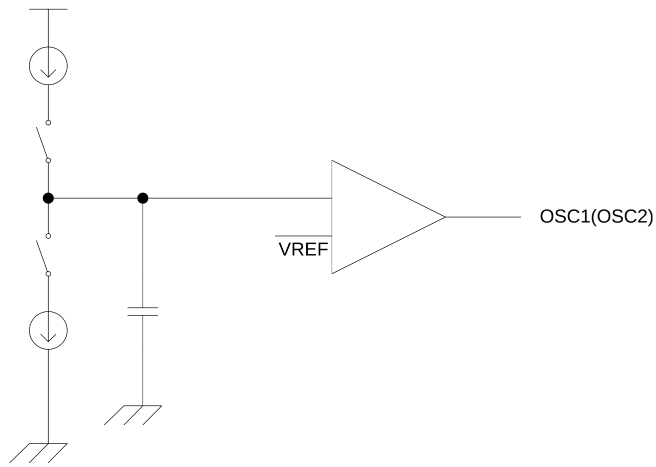
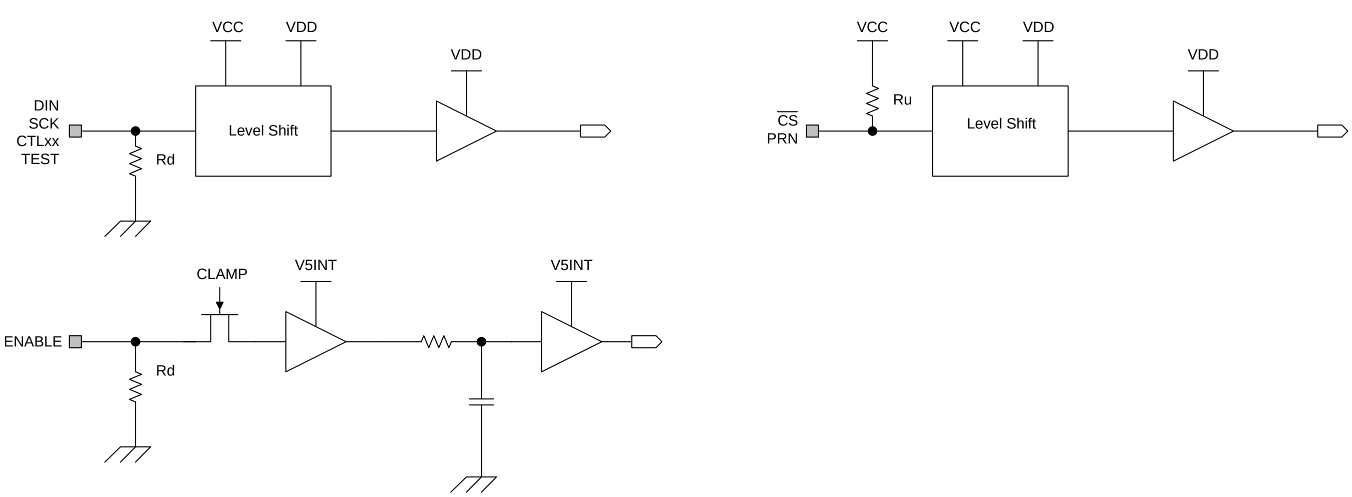


Figure 22. Oscillator Block Diagram

Table 11. Oscillator Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = –40°C to 125℃ (unless otherwise specified)						
OSCILLATOR						
OSC1	OSC1 frequency		9	10	11	MHz
OSC2	OSC2 frequency			10		MHz

I/O



* V5INT is the internal power supply.

Figure 23. Input Buffer1 Block Diagram

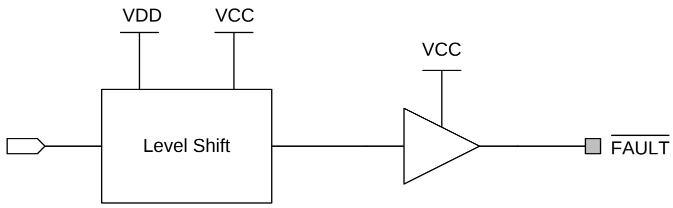


Figure 24. Output Buffer1 Block Diagram

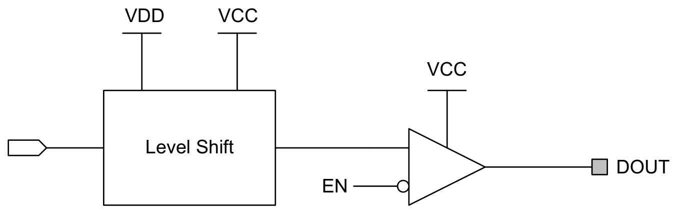


Figure 25. Output Buffer2 Block Diagram

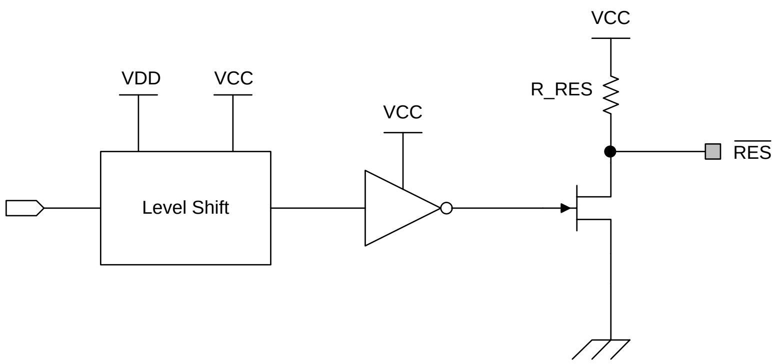


Figure 26. Output Buffer3 Block Diagram

Table 12. Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB = 12 V, T_A = –40°C to 125℃ (unless otherwise specified)						
Input Buffer1						
V_{IH}	Input threshold logic high		0.7 × VCC			V
V_{IL}	Input threshold logic low				0.3 × VCC	V
Ru or Rd	Input pullup or pulldown resistance		50	100	150	kΩ
Output Buffer1(2)						
V_{OH}	Output level logic high	Isink = 2.5 mA	0.9 × VCC			V
V_{OL}	Output level logic low	Isource = 2.5 mA			0.1 × VCC	V
Output Buffer3						
R_RES	Pull up Resistor		2	3	4	kΩ
V_{OL}	Output level logic low	Isource = 2 mA			0.1 × VCC	V

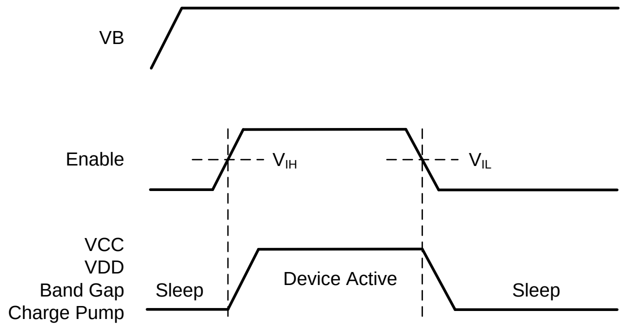


Figure 27. ENABLE Timing Chart

Table 13. Recommended Pin Termination

PIN NAME	DESCRIPTION	TERMINATION
TEST	Test mode input	OPEN

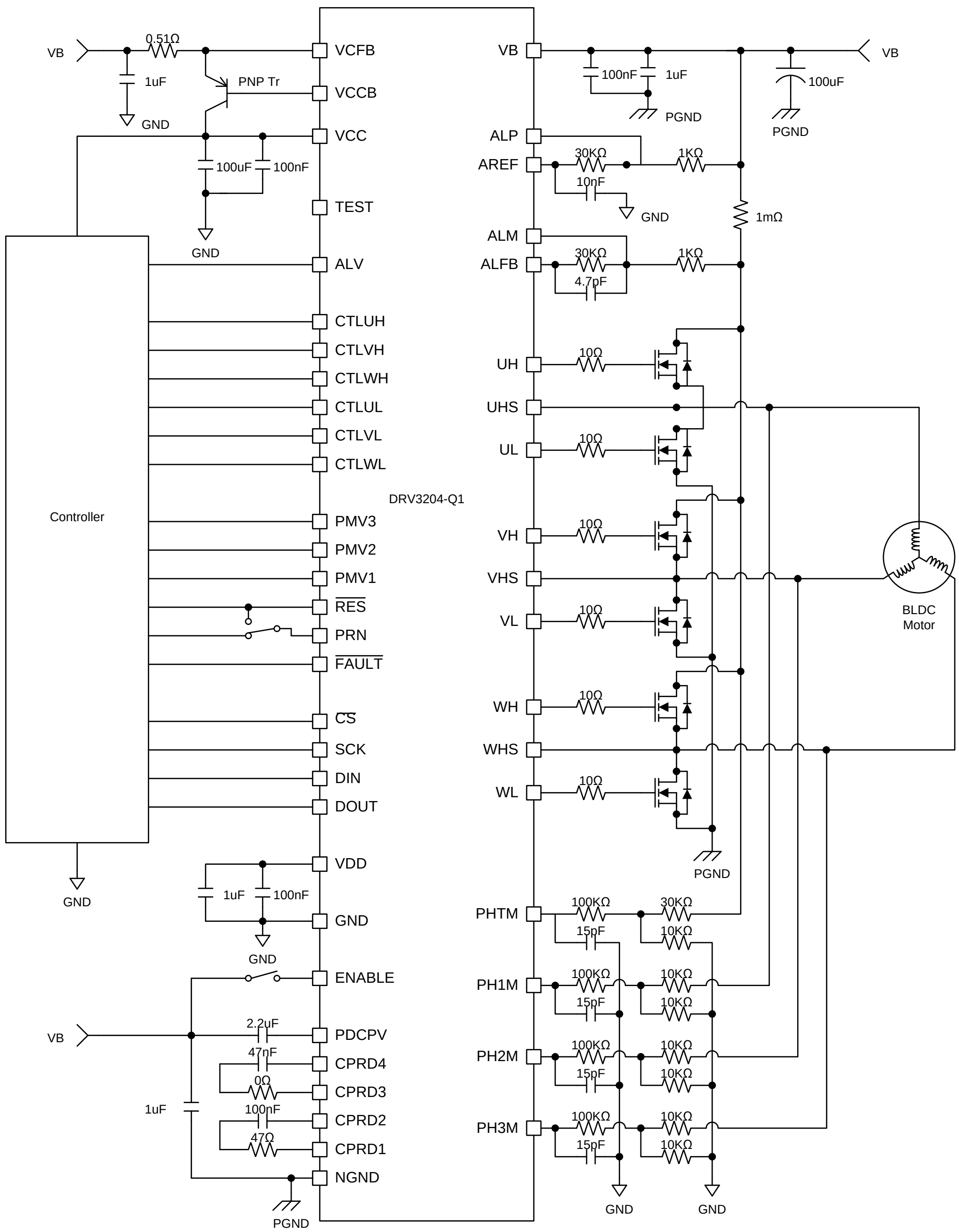
Fault Detection

Table 14. Fault Detection

ITEMS	SPI FLTFLG	Pre Driver(1)	FAULT(2)	RES	Others
VB – Overvoltage	VBOV	Disable	L	H	
VB – Undervoltage	VBUV	Disable	L	H	
CP – Overvoltage	CPOV	Disable	L	H	
CP – Undervoltage	CPUV	Disable	L	H	
VCC – Overvoltage	VCCOV	Disable	L	H	
VCC – Under Voltage	–	Disable(3)	H	L	
VCC – Overcurrent	VCCOC	Disable	L	H	
Motor – Overcurrent	MTOC	Disable	L	H	
VDD – Overvoltage	VDDOV	Disable	L	H	
VDD – Undervoltage	–	Disable(3)	H	L	
Thermal shutdown	TSD	Disable	L	H	
Watch Dog	–	–	H	L	
Clock Monitor	–	–	H	L	
SPI format error	–	–	H	H	SPI serial out error bit

(1) Pre-driver is disabled if the conditions occur and SDNEN register bits are 1.
(2) $\overline{\text{FAULT}}$ pin is asserted to low if the conditions occur and FLTEN register bits are 1.
(3) Pre-driver is disabled by VCC undervoltage and VDD undervoltage conditions regardless of SPI register setting.

Application Description



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV3204QPHPQ1	ACTIVE	HTQFP	PHP	48	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 150	DRV3204	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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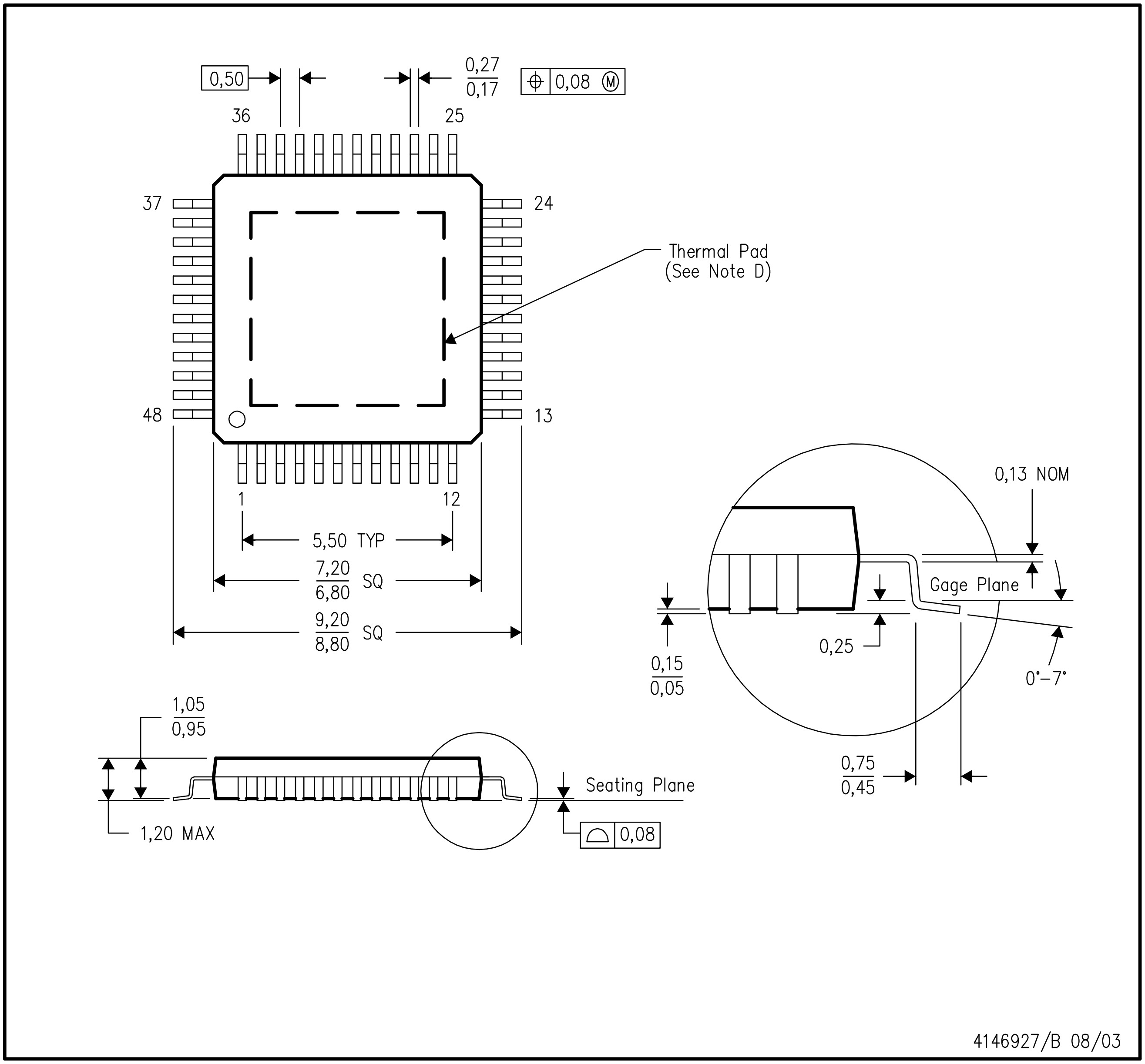
PHP (S-PQFP-G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

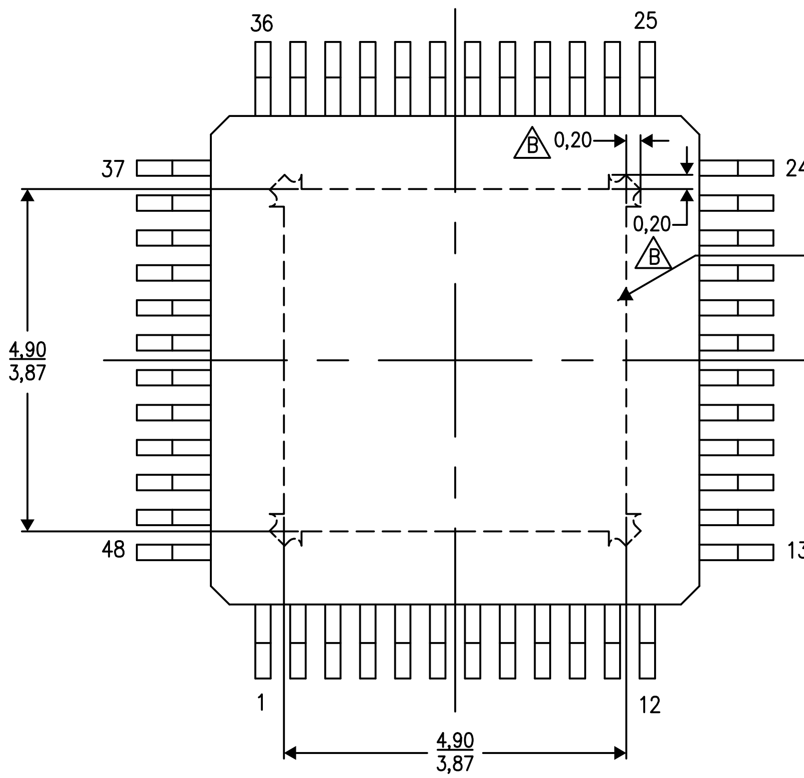
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206329–4/N 04/12

NOTE: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

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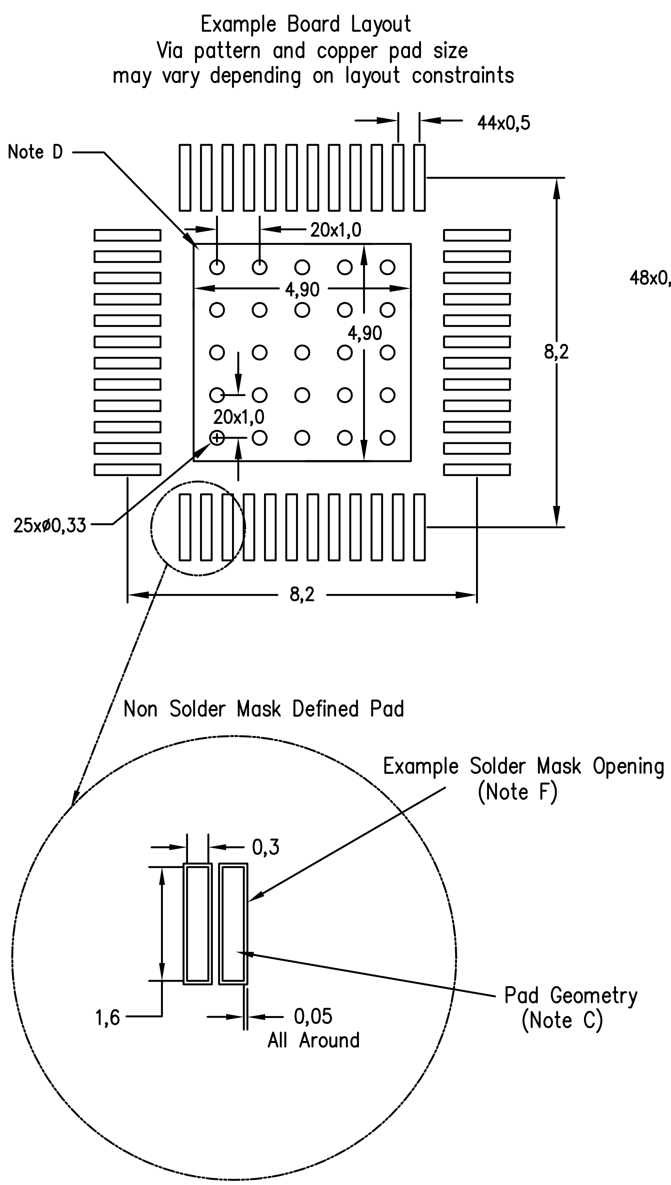
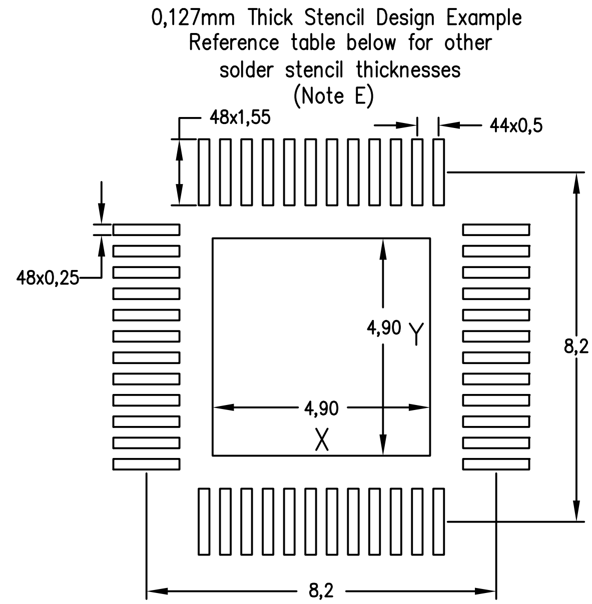
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.20	5.20
0.127mm	4.90	4.90
0.152mm	4.50	4.50
0.178mm	4.25	4.25

4207626-4/H 04/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

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