LM4985

LM4985 Stereo 135mW Low Noise Headphone Amplifier with Selectable Capacitively Coupled or Output Capacitor-less (OCL) Output and Digitally Controlled (I2C) Volume Control

Literature Number: SNAS346B

National Semiconductor

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LM4985 Boomer® Audio Power Amplifier Series

Stereo 135mW Low Noise Headphone Amplifier with Selectable Capacitively Coupled or Output Capacitor-less (OCL) Output and Digitally Controlled (I^2C) Volume Control

General Description

The LM4985 is a stereo audio power amplifier with internal digitally controlled volume control. This amplifier is capable of delivering $68mW_{RMS}$ per channel into a 16Ω load or $38mW_{RMS}$ per channel into a 32Ω load at 1% THD when powered by a 3.6V power supply and operating in the OCL mode.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. To that end, the LM4985 features two functions that optimize system cost and minimize PCB area: an integrated, digitally controlled (I^2C bus) volume control and an operational mode that eliminates output signal coupling capacitors (OCL mode). Since the LM4985 does not require bootstrap capacitors, snubber networks, or output coupling capacitors, it is optimally suited for low-power, battery powered portable systems. For added design flexibility, the LM4985 can also be configured for single-ended capacitively coupled outputs.

The LM4985 features a current shutdown mode for micropower dissipation and thermal shutdown protection.

Key Specifications (V_{DD} = 3.6V)

■ PSRR: 217Hz and 1kHz	
Output Capacitor-less (OCL)	
f_{RIPPLE} = 217Hz	77dB (typ)
f_{RIPPLE} = 1kHz	76dB (typ)
Capacitor Coupled (C-CUPL)	
f_{RIPPLE} = 217Hz	63dB (typ)
f_{RIPPLE} = 1kHz	62dB (typ)
■ Output Power per channel (f_{IN} = 1kHz, THD+N = 1%), R_L = 16Ω,OCL	
V_{DD} = 2.5V	31mW (typ)
V_{DD} = 3.6V	68mW (typ)
V_{DD} = 5.0V	135mW (typ)
■ THD+N (f = 1kHz)	
R_{LOAD} = 16Ω, OCL, P_{OUT} = 60mW	0.60
R_{LOAD} = 32Ω, OCL, P_{OUT} = 33mW	0.031
■ Shutdown Current	0.1µA (typ)

Features

- OCL or capacitively coupled outputs (patent pending)
- I^2C Digitally Controlled Volume Control
- Available in space-saving 0.4mm lead-pitch micro SMD package
- Volume control range: –76dB to +18dB
- Ultra low current shutdown mode
- 2.3V - 5.5V operation
- Ultra low noise

Applications

- Mobile Phones
- PDAs
- Portable electronics devices
- MP3 Players

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Block Diagram

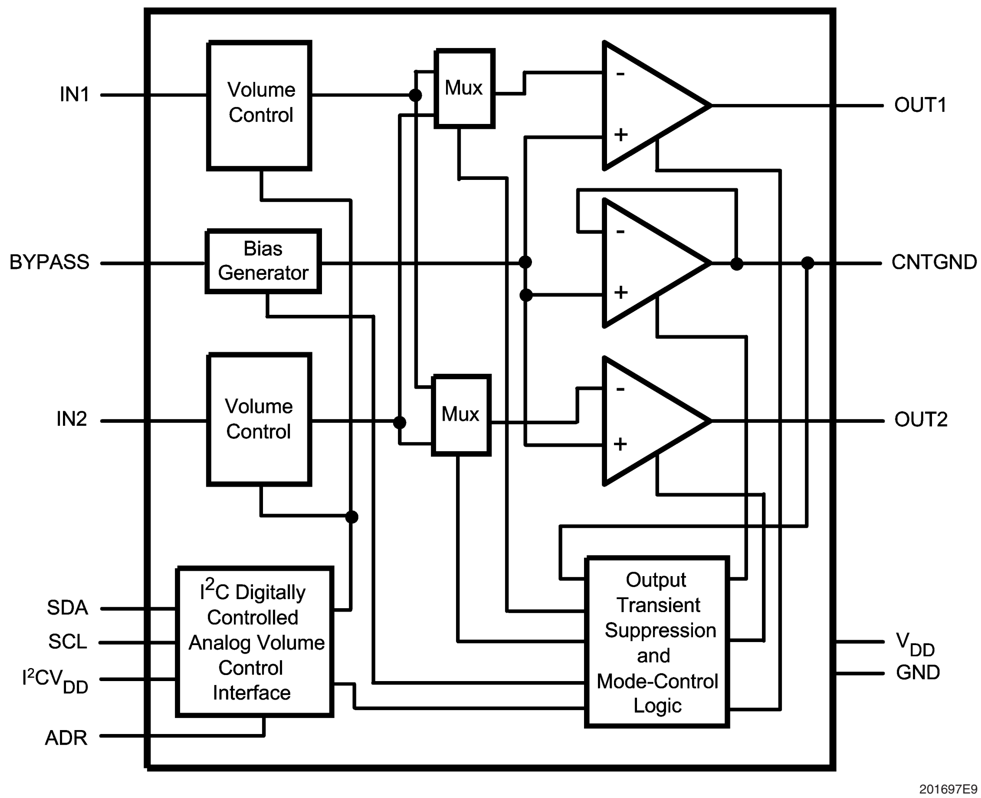


FIGURE 1. Block Diagram

Typical Application

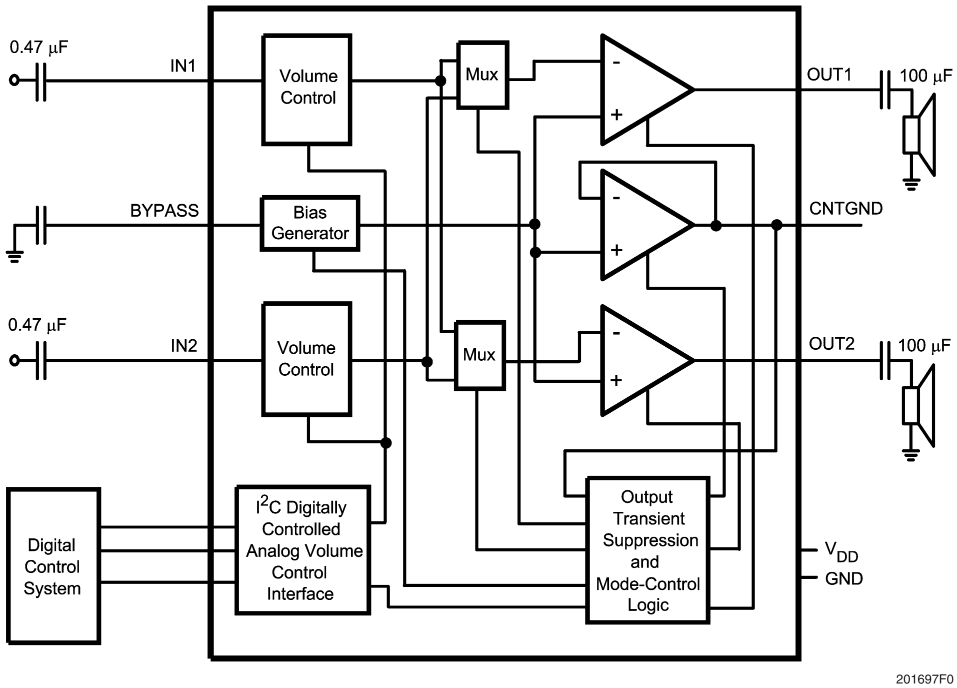


FIGURE 2. Typical Capacitively Coupled Output Configuration Circuit

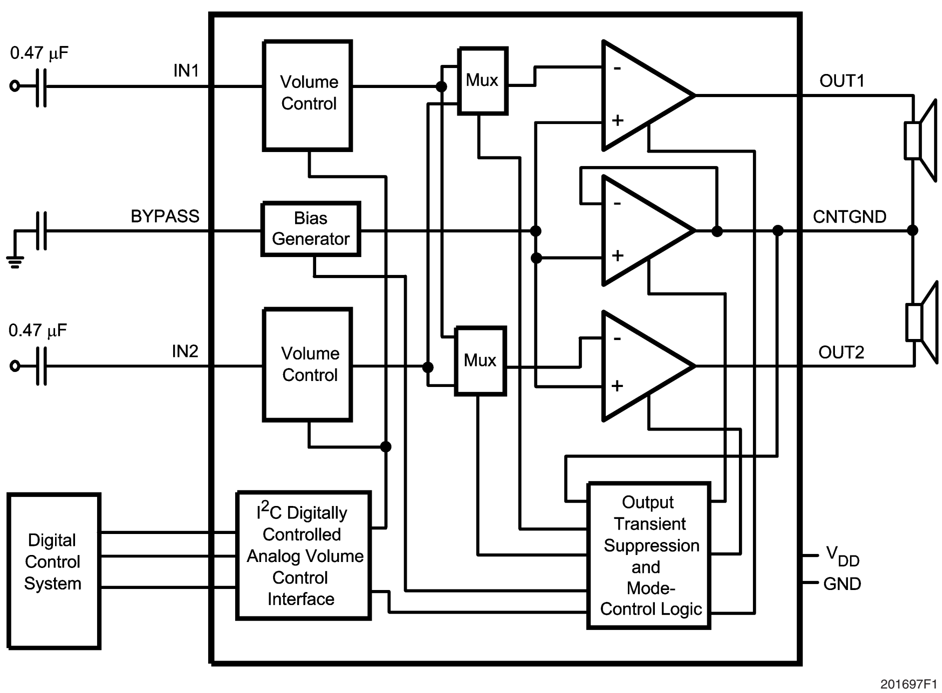
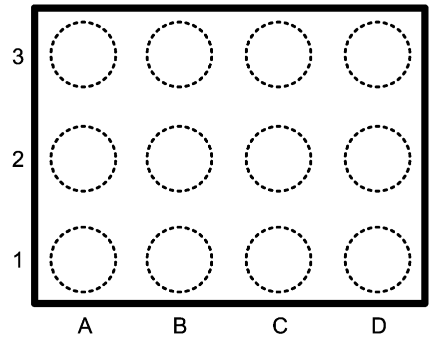


FIGURE 3. Typical OCL Output Configuration Circuit

Connection Diagrams

micro SMD Package



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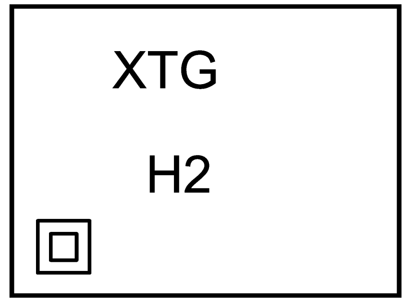
Top View
Order Number LM4985TM
See NS Package Number TMD12AAA

micro SMD Marking



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Top View
X – Date Code
T – Die Traceability
G – Boomer Family
H2 – LM4985TM

Pin Reference, Name, and Function

Reference	Name	Function
A1	ADR	I^2C serial interface address input.
A2	IN2	Analog signal input two.
A3	OUT2	Power amplifier two output.
B1	SDA	I^2C serial interface data input.
B2	BYPASS	The internal $V_{DD}/2$ ac bypass node.
B3	CNTGND	In OCL mode, this is the ac ground return. It is biased to $V_{DD}/2$. Leave unconnected for C-CUPL mode.
C1	SCL	I2C serial interface clock input.
C2	GND	The LM4985's power supply ground input.
C3	V_{DD}	The LM4985's power supply voltage input.
D1	I^2CV_{DD}	I^2C serial interface power supply input. Can be connected to the same supply that is connected to the V_{DD} pin.
D2	IN1	Analog signal input one.
D3	OUT1	Power amplifier one output.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD}, I^2CV_{DD})	6.0V
Storage Temperature	–65˚C to +150˚C
Input Voltage (IN1, IN2, OUT1, OUT2, BYPASS, CNTGND, GND pins relative to the V_{DD} pin)	-0.3V to V_{DD} + 0.3V
Input Voltage (ADR, SDA, SCL pins, relative to the I^2CV_{DD} pin)	-0.3V to I^2CV_{DD} + 0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150˚C
Thermal Resistance	
θ_{JA}	109˚C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40˚C \le T_A \le 85˚C$
Supply Voltage	
V_{DD}	$2.3V \le V_{CC} \le 5.5V$
I^2CV_{DD}	$1.7V \le I^2CV_{DD} \le 5.5V$

Electrical Characteristics V_{DD} = 5V (Notes 1, 2)

The following specifications apply for R_L = 16Ω, f = 1kHz, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25˚C.

Symbol	Parameter	Conditions	LM4985		Units (Limits)
			Typ (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_{OUT} = 0A Single-Channel no load OCL Single-Channel no load C-CUPL Dual-Channel no load OCL Dual-Channel no load C-CUPL	 2 1.5 3 2.3	 4.9 3.8	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	1.0	µA (max)
V_{SDIH}	Logic Voltage Input High			3.5	V (min)
V_{SDIL}	Logic Voltage Input Low			1.5	V (max)
P_O	Output Power	THD ≤ 1%; f_{IN} = 1kHz R_{LOAD} = 16Ω OCL R_{LOAD} = 16Ω C-CUPL R_{LOAD} = 32Ω OCL R_{LOAD} = 32Ω C-CUPL	 135 135 79 80	 115 70 	mW (min)
THD+N	Total Harmonic Distortion + Noise	R_{LOAD} = 16Ω OCL, P_O = 100mW R_{LOAD} = 16Ω C-CUPL, P_O = 100mW R_{LOAD} = 32Ω OCL, P_O = 60mW R_{LOAD} = 32Ω C-CUPL, P_O = 70mW	0.08 0.02 0.04 0.01		%
V_{ON}	Output Noise Voltage	V_{IN} = AC GND, A_V = 0dB, A-weighted	15		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVp-p (Note 9) f_{IN} = 217Hz sinewave OCL C-CUPL	 77 65	57	dB (min)
		f_{IN} = 1kHz sinewave OCL C-CUPL	 77 65	 60 	
Xtalk	Channel-to-channel Crosstalk	P_{out} = 40mW. OCL R_{LOAD} = 16Ω R_{LOAD}= 32Ω P_{out} = 50mW. C-CUPL R_{LOAD} = 16Ω R_{LOAD}= 32Ω	 51 56 58 68		 dB dB

Electrical Characteristics V_{DD} = 5V (Notes 1, 2) (Continued)

The following specifications apply for R_L = 16Ω, f = 1kHz, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25˚C.

Symbol	Parameter	Conditions	LM4985		Units (Limits)
			Typ (Note 6)	Limit (Notes 7, 8)	
T_{WU}	Wake Up Time form Shutdown	C_{BYPASS}= 4.7µF (Note 11)			msec
		WT1 = 0, WT0 = 0 OCL C-CUPL	 75 285		
		WT1 = 0, WT0 = 1 OCL C-CUPL	 110 530		
		WT1 = 1, WT0 = 0 OCL C-CUPL	 180 1030		
		WT1 = 1, WT0 = 1 OCL C-CUPL	 320 2050		
R_{IN}	Input Resistance	Stereo mode Mono mode	20 10		kΩ
A_{VMIN}	Minimum Gain	Code = 00000	–76		dB (min)
A_{VMAX}	Maximum Gain	Code = 11111	18		dB (min)
ΔA_V	Gain Accuracy per Step	18dB ≥ A_V ≥ −44dB −44dB ≥ A_V > −76dB	±0.5 ±1.0		dB
V_{OS}	Output Offset Voltage	OCL R_{LOAD} = 32Ω V_{IN} = AC GND	2.0	20	mV (max)

Electrical Characteristics V_{DD} = 3.6V (Notes 1, 2)

The following specifications apply for R_L = 16Ω, f = 1kHz, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25˚C.

Symbol	Parameter	Conditions	LM4985		Units (Limits)
			Typ (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_{OUT} = 0A Single-Channel no load OCL Single-Channel no load C-CUPL Dual-Channel no load OCL Dual-Channel no load C-CUPL	 1.8 1.0 2.1 2.3	 3.1 4 3	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1	1.0	µA (max)
V_{SDIH}	Logic Voltage Input High			2.52	V (min)
V_{SDIL}	Logic Voltage Input Low			1.08	V (max)
P_O	Output Power	THD+N < 1%, f_{IN} = 1kHz R_{LOAD} = 16Ω OCL R_{LOAD} = 16Ω C-CUPL R_{LOAD} = 32Ω OCL R_{LOAD} = 32Ω C-CUPL	 68 70 38 41	 60 34 	mW (min)

Electrical Characteristics V_{DD} = 3.6V (Notes 1, 2) (Continued)

The following specifications apply for R_L = 16Ω, f = 1kHz, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25˚C.

Symbol	Parameter	Conditions	LM4985 Typ (Note 6)	LM4985 Limit (Notes 7, 8)	Units (Limits)
THD+N	Total Harmonic Distortion + Noise	R_{LOAD} = 16Ω OCL, P_O = 60mW R_{LOAD} = 16Ω C-CUPL, P_O = 60mW R_{LOAD} = 32Ω OCL, P_O = 33mW R_{LOAD} = 32Ω C-CUPL, P_O = 38mW	0.06 0.03 0.03 0.03		%
V_{ON}	Output Noise Voltage	V_{IN} = AC GND, A_V = 0dB, A-weighted	15		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVp-p (Note 9) f_{IN} = 217Hz sinewave OCL C-CUPL f_{IN} = 1kHz sinewave OCL C-CUPL	 77 63 76 62	 55 57 	dB (min)
Xtalk	Channel-to-Channel Crosstalk	P_{out} = 40mW. OCL R_{LOAD} = 16Ω R_{LOAD}= 32Ω P_{out} = 50mW. C-CUPL R_{LOAD} = 16Ω R_{LOAD}= 32Ω	 51 56 58 69		 dB dB
T_{WU}	Wake Up Time from Shutdown	C_{BYPASS}= 4.7µF (Note 11)			
		WT1 = 0, WT0 = 0 OCL C-CUPL	 66 222	 93 	msec
		WT1 = 0, WT0 = 1 OCL C-CUPL	 92 405		msec
		WT1 = 1, WT0 = 0 OCL C-CUPL	 143 774		msec
		WT1 = 1, WT0 =1 OCL C-CUPL	 246 1532		msec
R_{IN}	Input Resistance	Stereo mode Mono mode	20 10		kΩ
A_{VMIN}	Minimum Gain	Code = 00000	–76	–72	dB (max)
A_{VMAX}	Maximum Gain	Code = 11111	18	17	dB (min)
ΔA_V	Gain Accuracy per Step	18dB ≥ A_V ≥–44dB –44dB ≥ A_V > –76dB	± 0.5 ± 1.0	± 1.0 ± 2.0	dB
V_{OS}	Output Offset Voltage	OCL R_{LOAD} = 32Ω V_{IN} = AC GND	2.0	20	mV (max)

Electrical Characteristics V_{DD} = 2.5V (Notes 1, 2)

The following specifications apply for R_L = 16Ω, f = 1kHz, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25˚C.

Symbol	Parameter	Conditions	LM4985		Units (Limits)
			Typ (Note 6)	Limit (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_{OUT} = 0A Single-Channel no load OCL Single-Channel no load C-CUPL Dual-Channel no load OCL Dual-Channel no load C-CUPL	 1.6 1 2.1 1.6		mA
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = GND	0.1		µA
V_{SDIH}	Logic Voltage Input High			1.75	V (min)
V_{SDIL}	Logic Voltage Input Low			0.75	V (max)
P_O	Output Power	THD+N < 1%, f_{IN} = 1kHz R_{LOAD} = 16Ω OCL R_{LOAD} = 16Ω C-CUPL R_{LOAD} = 32Ω OCL R_{LOAD} = 32Ω C-CUPL	 31 33 19 19		mW
THD+N	Total Harmonic Distortion + Noise	R_{LOAD} = 16Ω OCL, P_O = 26mW R_{LOAD} = 16Ω C-CUPL, P_O = 20mW R_{LOAD} = 32Ω OCL, P_O = 16mW R_{LOAD} = 32Ω C-CUPL, P_O = 15mW	0.07 0.05 0.06 0.04		%
V_{ON}	Output Noise Voltage	V_{IN} = AC GND, A_V = 0dB, A-weighted	10		µV
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVp-p (Note 9) f_{IN} = 217Hz sinewave OCL C-CUPL f_{IN} = 1kHz sinewave OCL C-CUPL	 75 59 75 59		dB
Xtalk	Channel-to-Channel Crosstalk	P_{out} = 20mW, OCL R_{LOAD} = 16Ω R_{LOAD}= 32Ω P_{out} = 20mW. C-CUPL R_{LOAD} = 16Ω R_{LOAD}= 32Ω	 50 55 58 67		 dB dB
T_{WU}	Wake Up Time from Shutdown	C_{BYPASS} = 4.7µF (Note 11)			
		WT1 = 0, WT0 = 0 OCL C-CUPL	 66 214		msec
		WT1 = 0, WT0 = 1 OCL C-CUPL	 92 544		
		WT1 = 1, WT0 = 0 OCL C-CUPL	 145 1053		
		WT1 = 1, WT0 = 1 OCL C-CUPL	 250 2098		
R_{IN}	Input Resistance	Stereo mode Mono mode	20 10		kΩ
A_{VMIN}	Minimum Gain	Code = 00000	–76		dB

Electrical Characteristics V_{DD} = 2.5V (Notes 1, 2) (Continued)

The following specifications apply for R_L = 16Ω, f = 1kHz, and C_B = 4.7µF unless otherwise specified. Limits apply to T_A = 25˚C.

Symbol	Parameter	Conditions	LM4985		Units (Limits)
			Typ (Note 6)	Limit (Notes 7, 8)	
A_{VMAX}	Maximum Gain	Code = 11111	18		dB
ΔA_V	Gain Accuracy per Step	18dB ≥ A_V ≥ −44dB −44dB ≥ A_V > −76dB	± 0.5 ± 1.0		dB
V_{OS}	Output Offset Voltage	OCL R_{LOAD} = 32Ω V_{IN} = AC GND	2.0		mV

Note 1: All voltages are measured with respect to the GND pin unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by TJMAX, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4985, see power derating currents for more information.

Note 4: Human Body Model: 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model: 200pF ≤ C_{mm} ≤ 220pF discharged through all pins.

Note 6: Typicals are measured at 25˚C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 9: 10Ω terminated input.

Note 10: The LDA10A package has its exposed-DAP soldered to an exposed 1.2in^2 area of 1oz. Printed circuit board copper.

Note 11: The wake-up time (T_{WU}) is calculated using the following formula; $T_{WU} = [C_{BYPASS} (VDD) / 2 (I_{BYPASS})] + 40ms$.

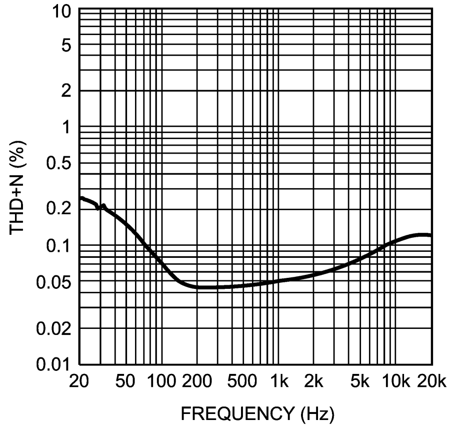
External Components Description (*Figure 2*)

Components		Functional Description
1.	C_I	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a high-pass filter with R_i at $f_c = 1/(2\pi R_i C_i)$. Refer to the section **Proper Selection of External Components,** for an explanation of how to determine the value of C_i.
2.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the **Power Supply Bypassing** section for information concerning proper placement and selection of the supply bypass capacitor.
3.	C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, **Proper Selection of Proper Components**, for information concerning proper placement and selection of C_B
6.	C_o	Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with R_L at $f_o = 1/(2\pi R_L C_o)$

Typical Performance Characteristics

T_A = 25°C, A_V = 0dB, f_{IN} = 1kHz unless otherwise stated.

THD+N vs Frequency
V_{DD} = 2.5V, R_L = 16Ω
P_{OUT} = 20mW, C-CUPL



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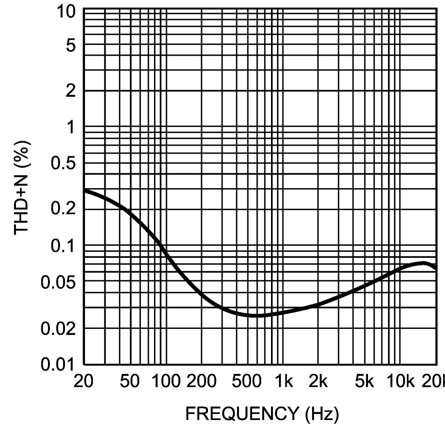
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 16Ω
P_{OUT} = 50mW, C-CUPL



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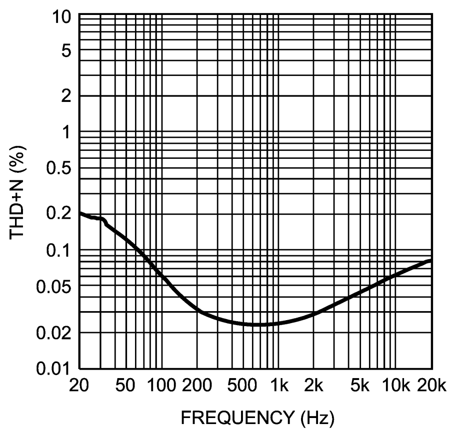
THD+N vs Frequency
V_{DD} = 5V, R_L = 16Ω
P_{OUT} = 50mW, C-CUPL



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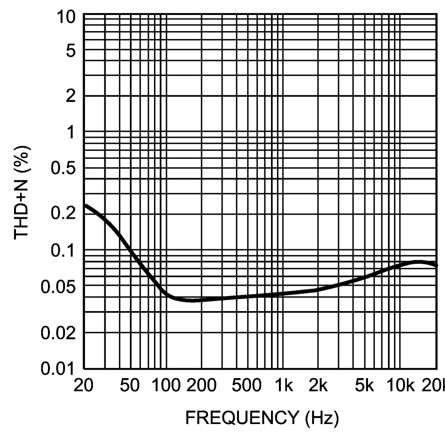
THD+N vs Frequency
V_{DD} = 2.5V, R_L = 32Ω
P_{OUT} = 15mW, C-CUPL



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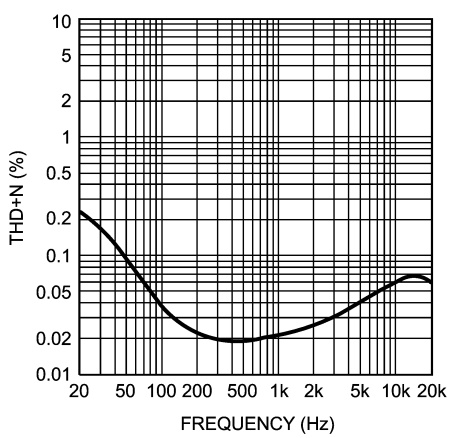
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω
P_{OUT} = 35mW, C-CUPL



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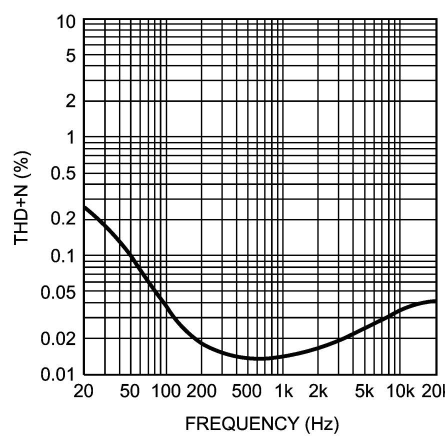
THD+N vs Frequency
V_{DD} = 5.0V, R_L = 32Ω
P_{OUT} = 60mW, C-CUPL



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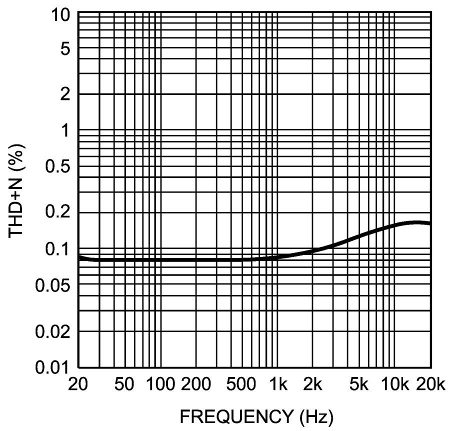
Typical Performance Characteristics (Continued)

THD+N vs Frequency
V_{DD} = 2.5V, R_L = 16Ω
P_{OUT} = 20mW, OCL



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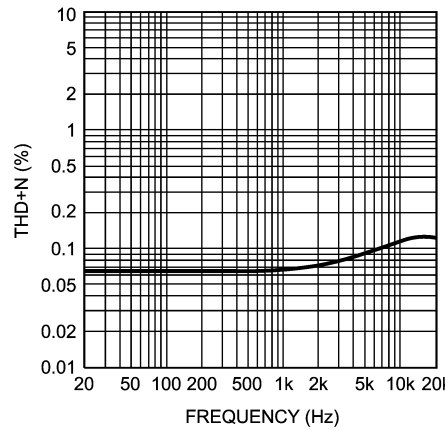
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 16Ω
P_{OUT} = 50mW, OCL



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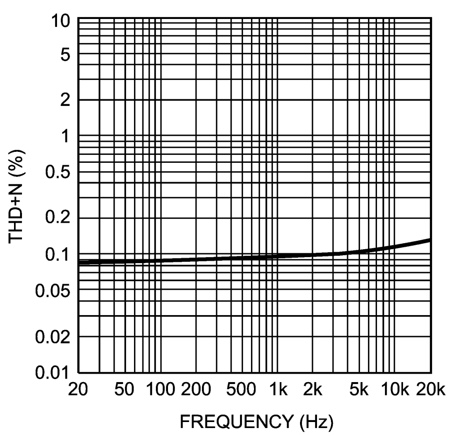
THD+N vs Frequency
V_{DD} = 5.0V, R_L = 16Ω
P_{OUT} = 50mW, OCL



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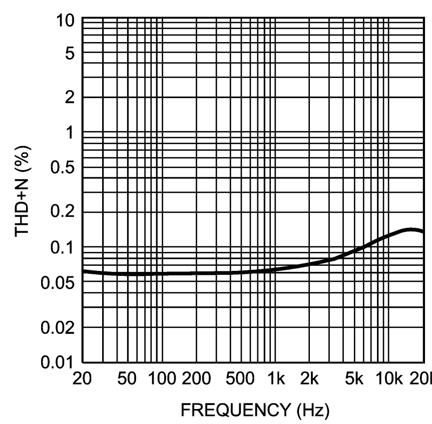
THD+N vs Frequency
V_{DD} = 2.5V, R_L = 32Ω
P_{OUT} = 15mW, OCL



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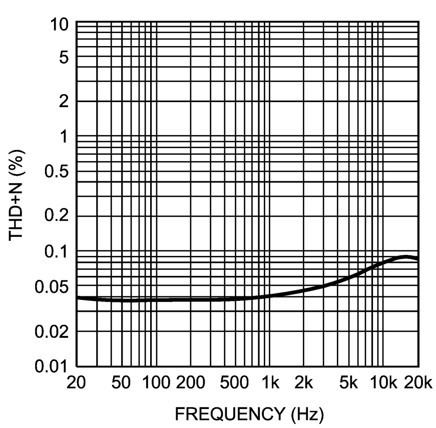
THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω
P_{OUT} = 35mW, OCL



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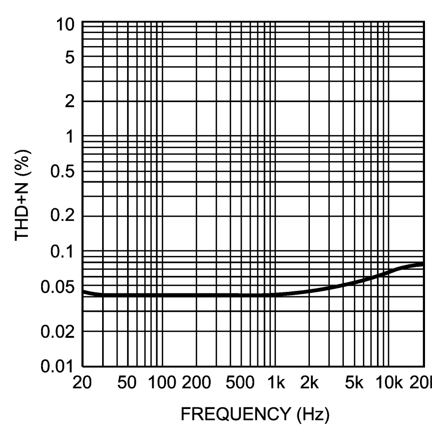
THD+N vs Frequency
V_{DD} = 5.0V, R_L = 32Ω
P_{OUT} = 60mW, OCL



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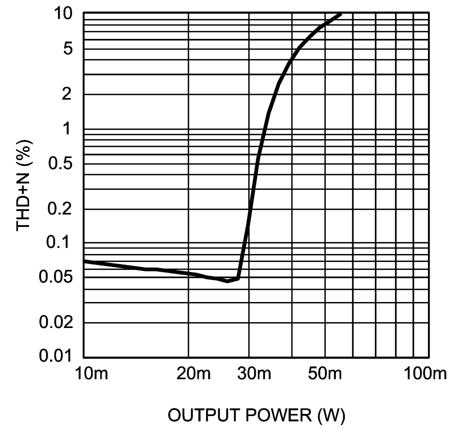
Typical Performance Characteristics (Continued)

THD+N vs Output Power
V_{DD} = 2.5V, R_L = 16Ω
C-CUPL



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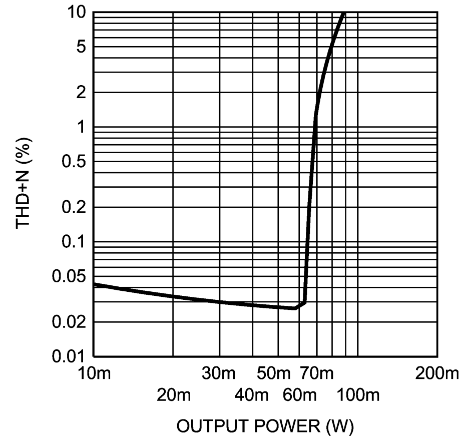
THD+N vs Output Power
V_{DD} = 3.6V, R_L = 16Ω
C-CUPL



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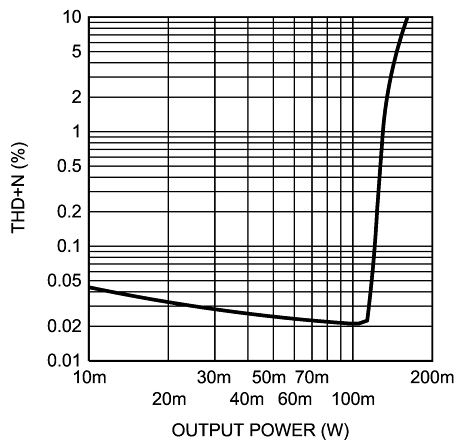
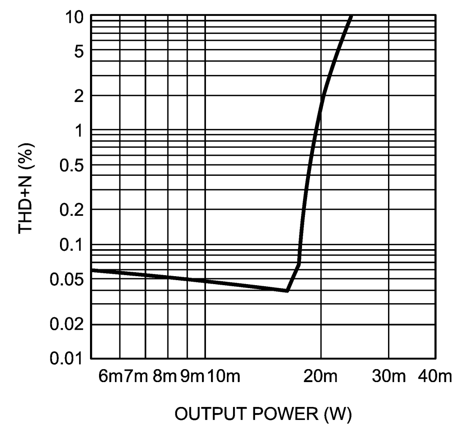
THD+N vs Output Power
V_{DD} = 5.0V, R_L = 16Ω
C-CUPL



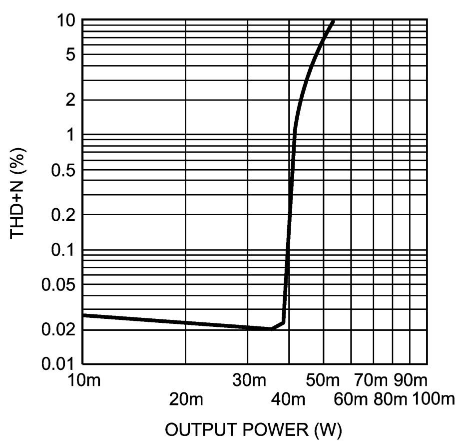
201697C7

THD+N vs Output Power
V_{DD} = 2.5V, R_L = 32Ω
C-CUPL



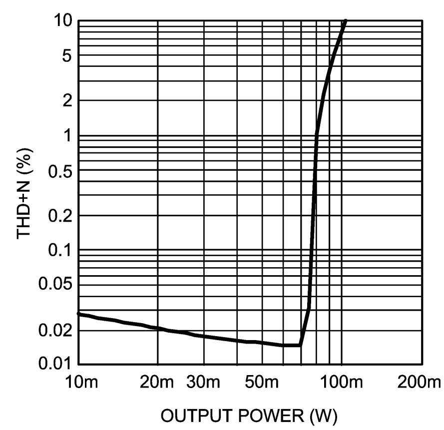
201697F2

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 32Ω
C-CUPL



201697F3

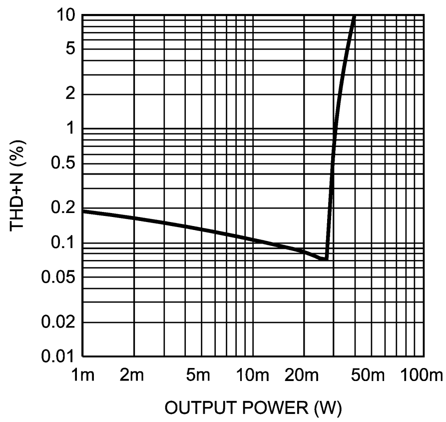
THD+N vs Output Power
V_{DD} = 5.0V, R_L = 32Ω
C-CUPL



201697H4

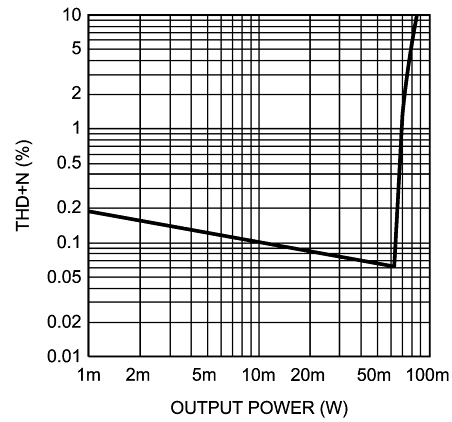
Typical Performance Characteristics (Continued)

THD+N vs Output Power
V_{DD} = 2.5V, R_L = 16Ω
OCL



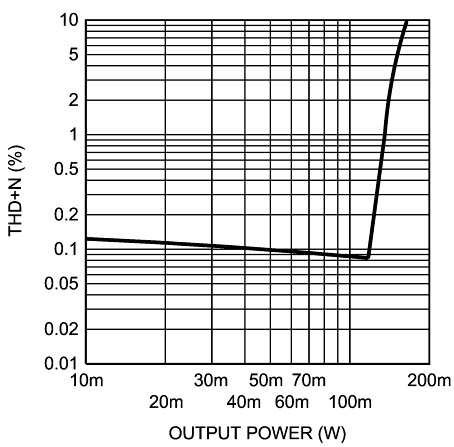
20169758

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 16Ω
OCL



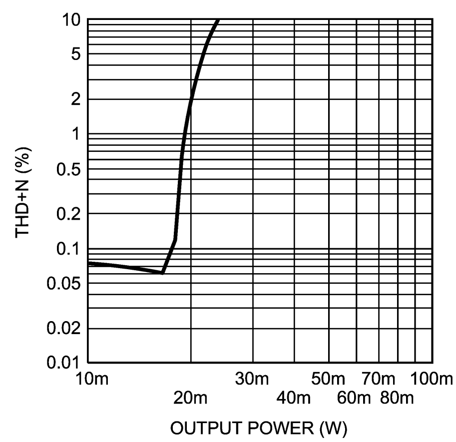
20169759

THD+N vs Output Power
V_{DD} = 5.0V, R_L = 16Ω
OCL



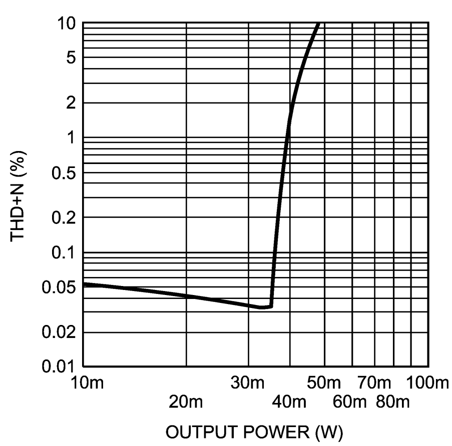
20169760

THD+N vs Output Power
V_{DD} = 2.5V, R_L = 32Ω
OCL



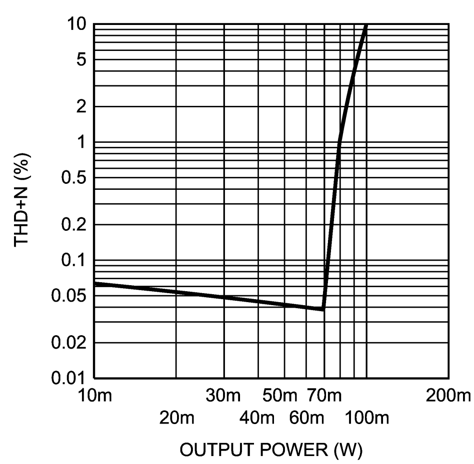
20169761

THD+N vs Output Power
V_{DD} = 3.6V, R_L = 32Ω
OCL



20169762

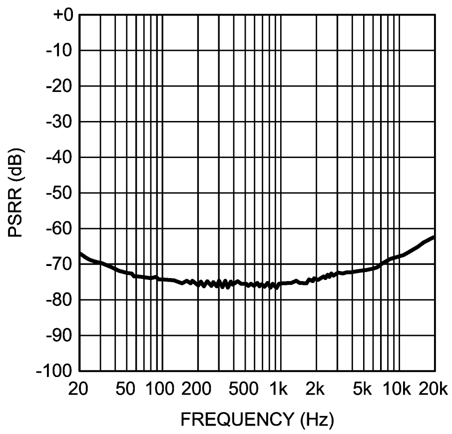
THD+N vs Output Power
V_{DD} = 5.0V, R_L = 32Ω
OCL



20169763

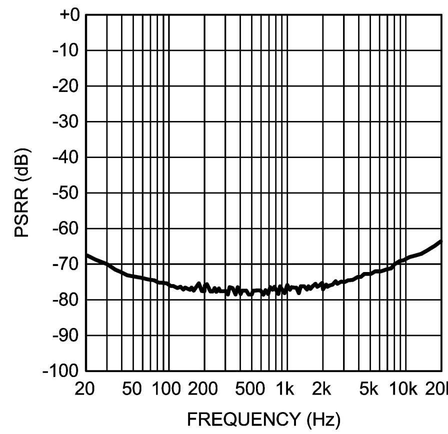
Typical Performance Characteristics (Continued)

PSRR vs Frequency
V_{DD} = 2.5V, R_L = 16Ω
V_{RIPPLE} = 200mVpp, OCL



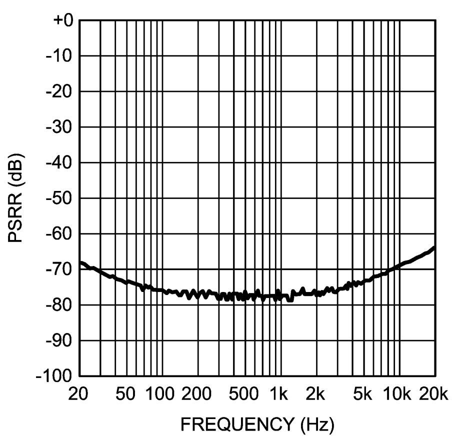
20169776

PSRR vs Frequency
V_{DD} = 3.6V, R_L = 16Ω
V_{RIPPLE} = 200mVpp, OCL



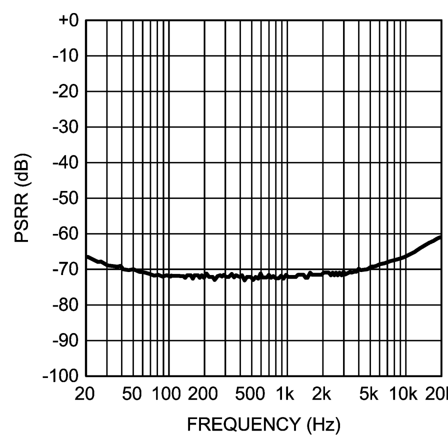
201697H5

PSRR vs Frequency
V_{DD} = 5.0V, R_L = 16Ω
V_{RIPPLE} = 200mVpp, OCL



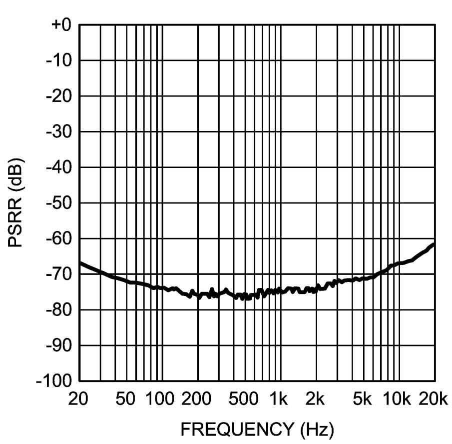
201697H6

PSRR vs Frequency
V_{DD} = 2.5V, R_L = 32Ω
V_{RIPPLE} = 200mVpp, OCL



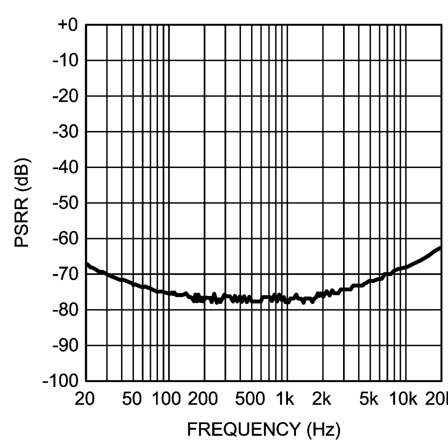
201697H7

PSRR vs Frequency
V_{DD} = 3.6V, R_L = 32Ω
V_{RIPPLE} = 200mVpp, OCL



201697H8

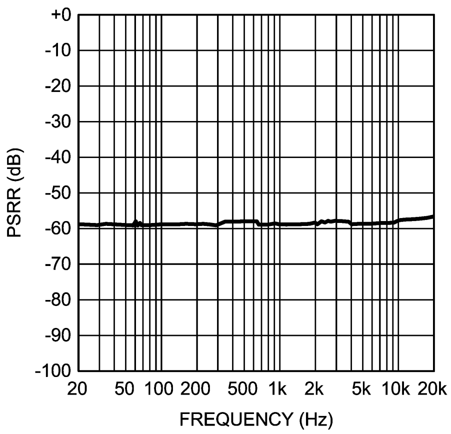
PSRR vs Frequency
V_{DD} = 5.0V, R_L = 32Ω
V_{RIPPLE} = 200mVpp, OCL



201697H9

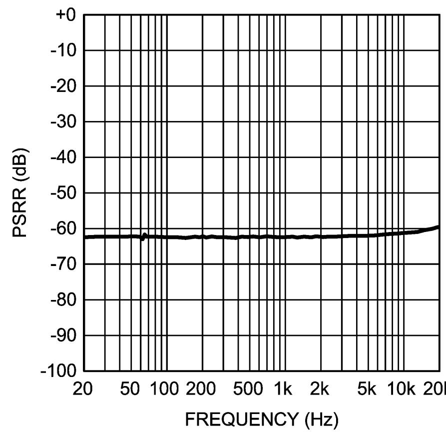
Typical Performance Characteristics (Continued)

PSRR vs Frequency
V_{DD} = 2.5V, R_L = 16Ω
V_{RIPPLE} = 200mVpp, C-CUPL



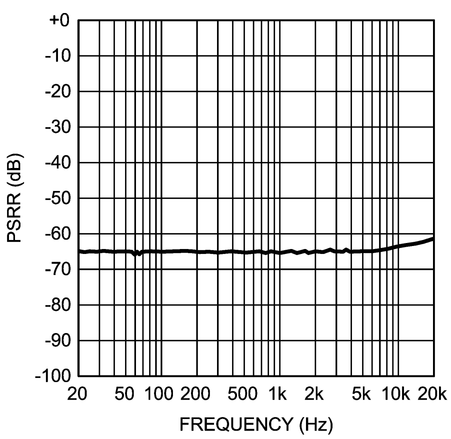
201697I0

PSRR vs Frequency
V_{DD} = 3.6V, R_L = 16Ω
V_{RIPPLE} = 200mVpp, C-CUPL



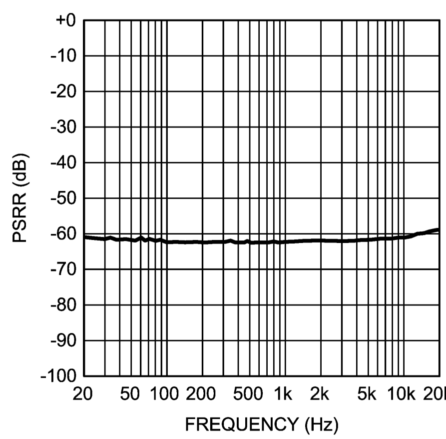
201697I1

PSRR vs Frequency
V_{DD} = 5.0V, R_L = 16Ω
V_{RIPPLE} = 200mVpp, C-CUPL



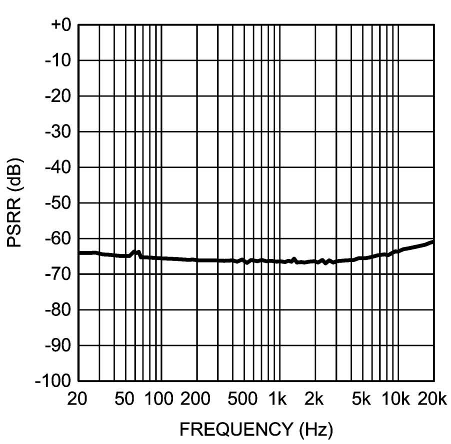
201697I2

PSRR vs Frequency
V_{DD} = 2.5V, R_L = 32Ω
V_{RIPPLE} = 200mVpp, C-CUPL



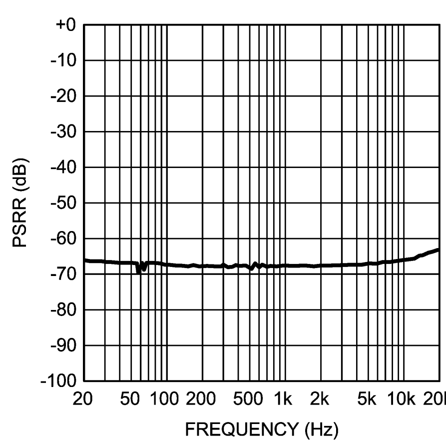
201697I3

PSRR vs Frequency
V_{DD} = 3.6V, R_L = 32Ω
V_{RIPPLE} = 200mVpp, C-CUPL



201697I4

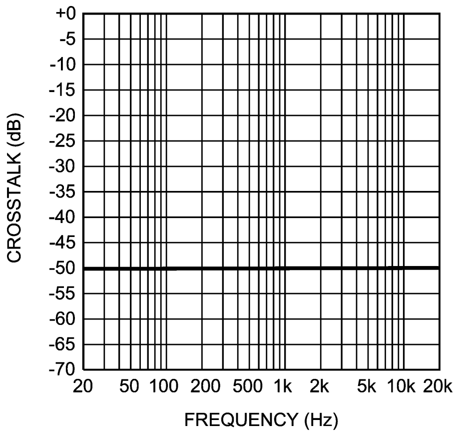
PSRR vs Frequency
V_{DD} = 5.0V, R_L = 32Ω
V_{RIPPLE} = 200mVpp, C-CUPL



201697I5

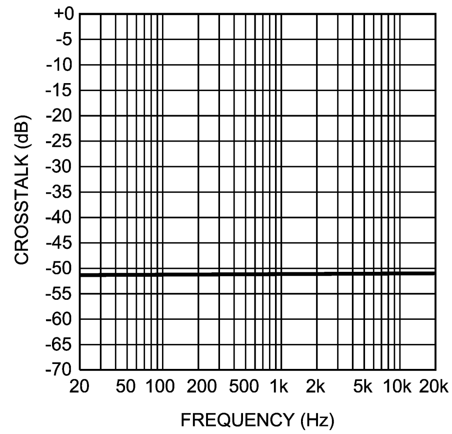
Typical Performance Characteristics (Continued)

Crosstalk vs Frequency
V_{DD} = 2.5V, R_L = 16Ω
P_{OUT} = 20mW. OCL



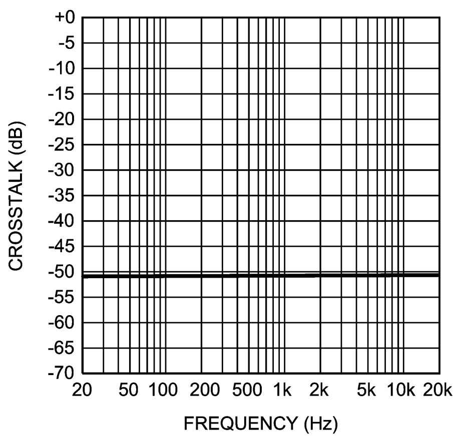
201697I6

Crosstalk vs Frequency
V_{DD} = 3.6V, R_L = 16Ω
P_{OUT} = 40mW, OCL



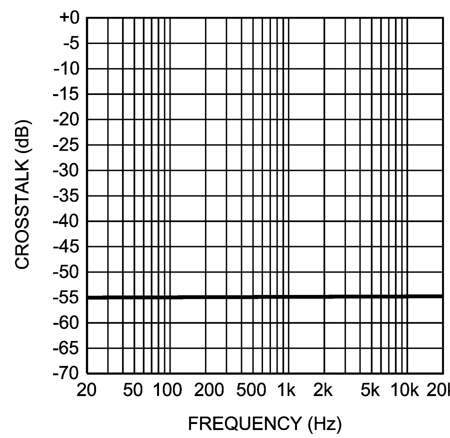
201697G8

Crosstalk vs Frequency
V_{DD} = 5.0V, R_L = 16Ω
P_{OUT} = 40mW, OCL



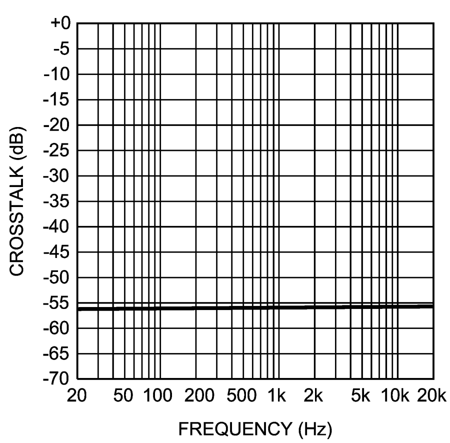
201697G9

Crosstalk vs Frequency
V_{DD} = 2.5V, R_L = 32Ω
P_{OUT} = 20mW, OCL



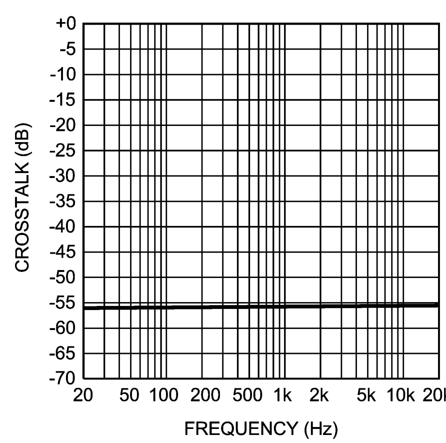
201697H0

Crosstalk vs Frequency
V_{DD} = 3.6V, R_L = 32Ω
P_{OUT} = 40mW, OCL



201697H1

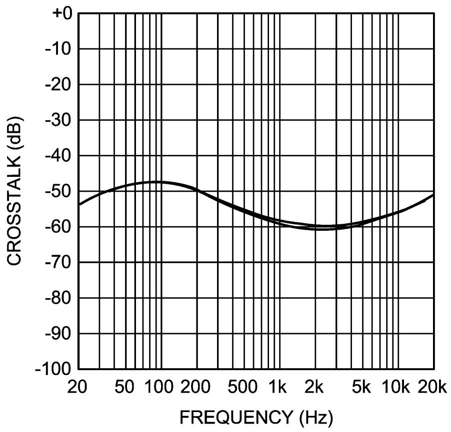
Crosstalk vs Frequency
V_{DD} = 5.0V, R_L = 32Ω
P_{OUT} = 50mW, OCL



201697H2

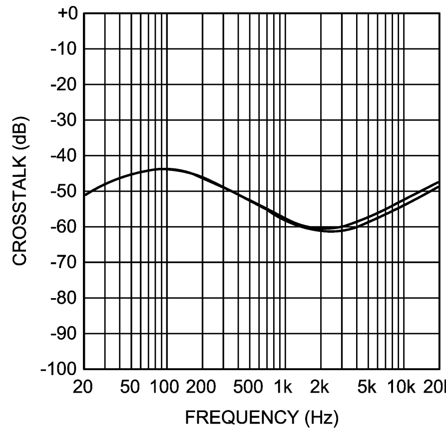
Typical Performance Characteristics (Continued)

Crosstalk vs Frequency
V_{DD} = 2.5V, R_L = 16Ω
P_{OUT} = 20mW, C-CUPL



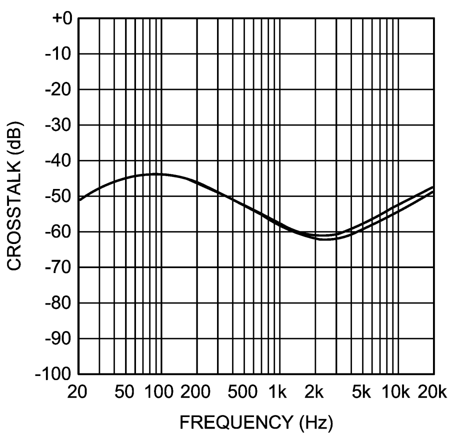
201697D7

Crosstalk vs Frequency
V_{DD} = 3.6V, R_L = 16Ω
P_{OUT} = 50mW, C-CUPL



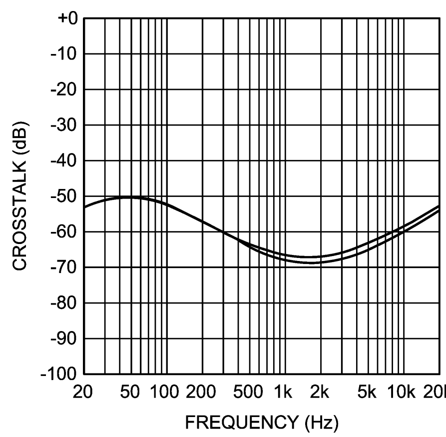
201697D8

Crosstalk vs Frequency
V_{DD} = 5.0V, R_L = 16Ω
P_{OUT} = 50mW, C-CUPL



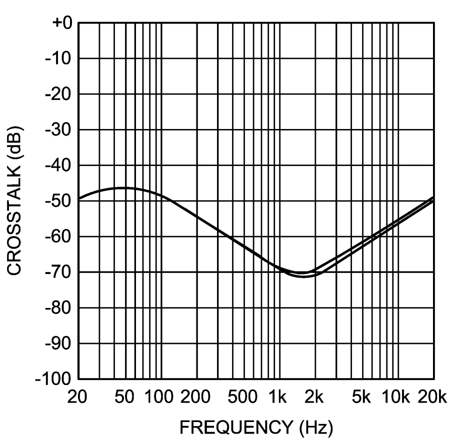
201697D9

Crosstalk vs Frequency
V_{DD} = 2.5V, R_L = 32Ω
P_{OUT} = 20mW, C-CUPL



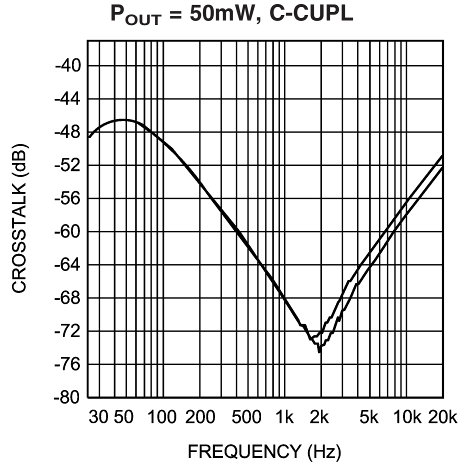
201697E0

Crosstalk vs Frequency
V_{DD} = 3.6V, R_L = 32Ω
P_{OUT} = 50mW, C-CUPL



201697E1

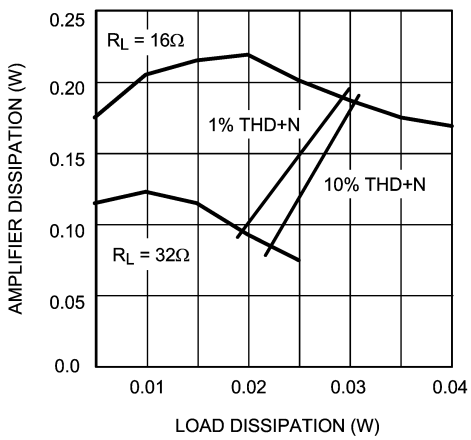
Crosstalk vs Frequency
V_{DD} = 5.0V, R_L = 32Ω
P_{OUT} = 50mW, C-CUPL



201697E2

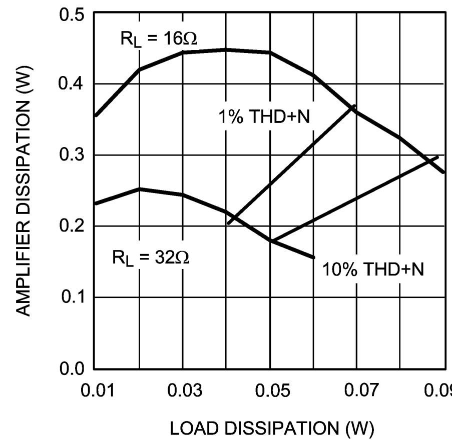
Typical Performance Characteristics (Continued)

Load Dissipation vs Amplifier Dissipation
V_{DD} = 2.5V, C-CUPL



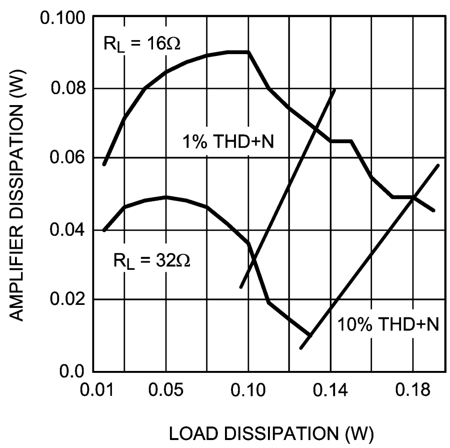
20169755

Load Dissipation vs Amplifier Dissipation
V_{DD} = 3.6V, C-CUPL



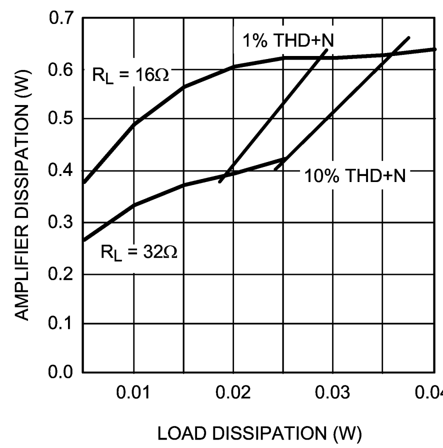
20169756

Load Dissipation vs Amplifier Dissipation
V_{DD} = 5.0V, C-CUPL



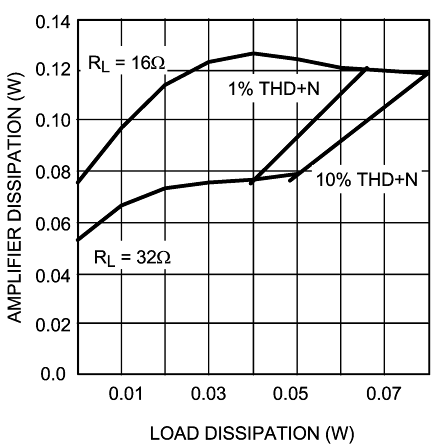
20169757

Load Dissipation vs Amplifier Dissipation
V_{DD} = 2.5V, OCL



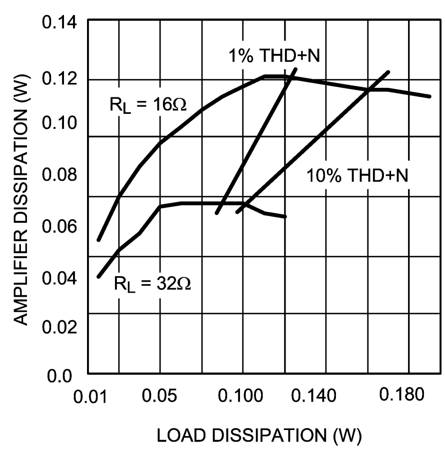
20169738

Load Dissipation vs Amplifier Dissipation
V_{DD} = 3.6V, OCL



20169739

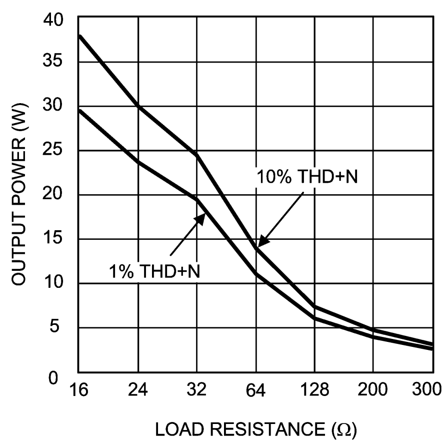
Load Dissipation vs Amplifier Dissipation
V_{DD} = 5.0V, OCL



20169740

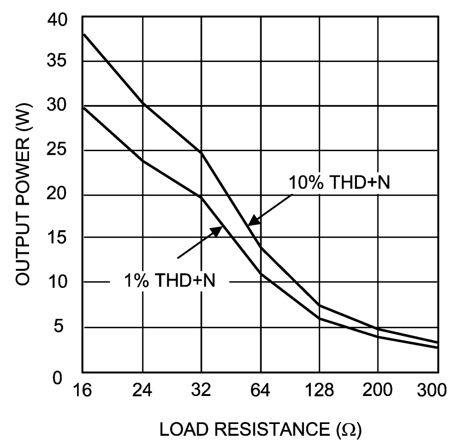
Typical Performance Characteristics (Continued)

Output Power vs Load Resistance
V_{DD} = 2.5V, C-CUPL



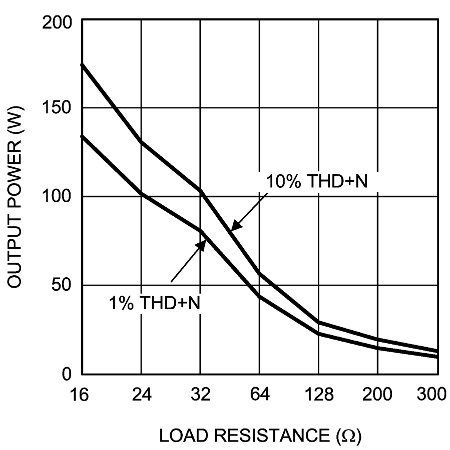
20169741

Output Power vs Load Resistance
V_{DD} = 3.6V, C-CUPL



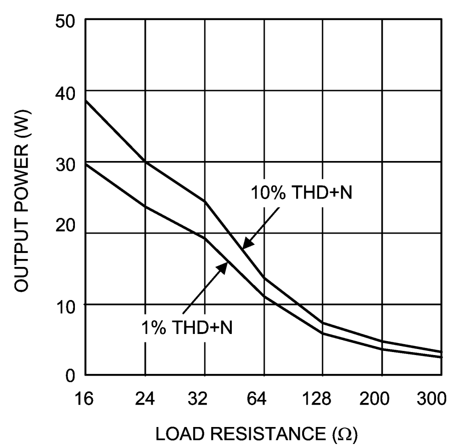
20169742

Output Power vs Load Resistance
V_{DD} = 5.0V, C-CUPL



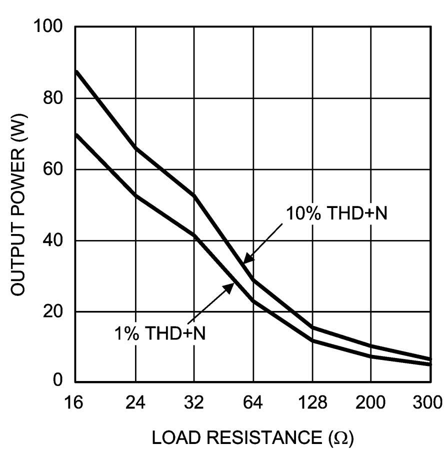
20169743

Output Power vs Load Resistance
V_{DD} = 2.5V, OCL



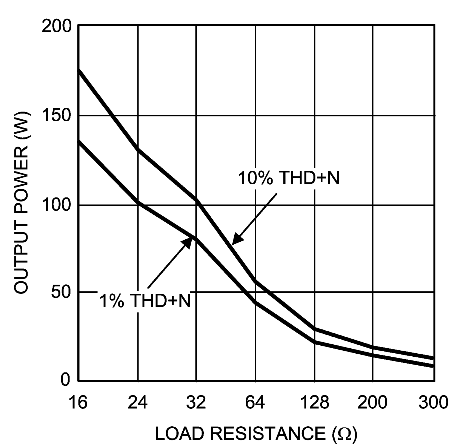
20169744

Output Power vs Load Resistance
V_{DD} = 3.6V, OCL



20169745

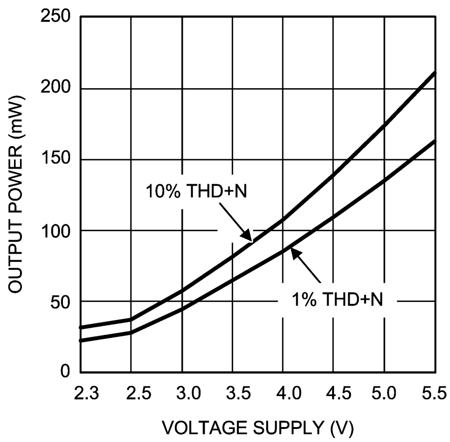
Output Power vs Load Resistance
V_{DD} = 5.0V, OCL



20169746

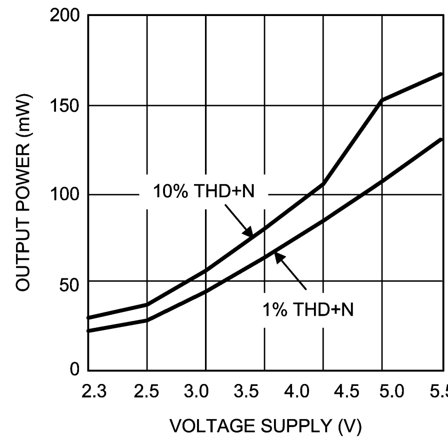
Typical Performance Characteristics (Continued)

Output Power vs Supply Voltage
R_L = 16Ω, C-CUPL



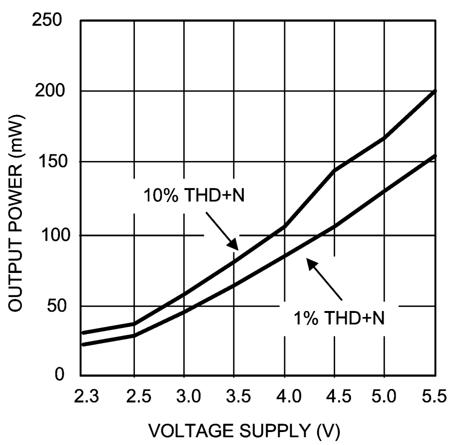
20169747

Output Power vs Supply Voltage
R_L = 32Ω, C-CUPL



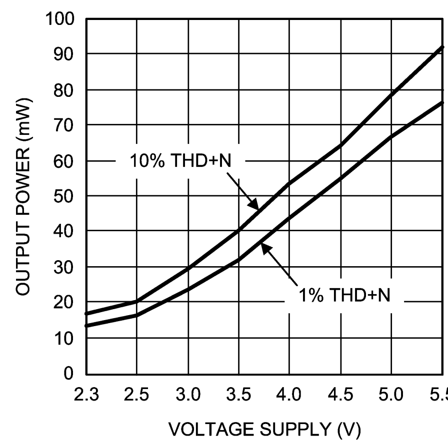
20169748

Output Power vs Supply Voltage
R_L = 16Ω, OCL



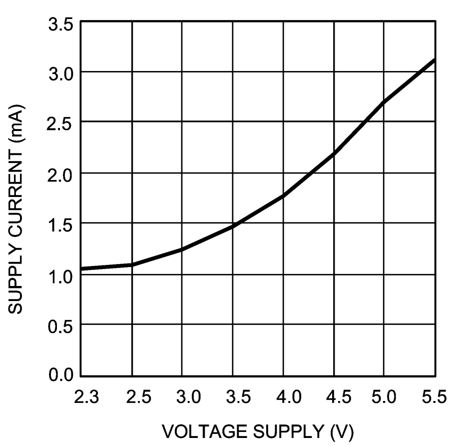
20169749

Output Power vs Supply Voltage
R_L = 32Ω, OCL



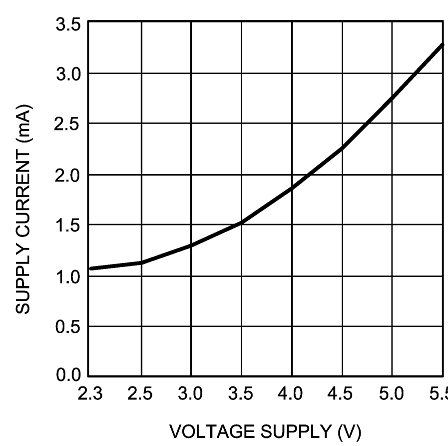
20169750

Supply Current vs Supply Voltage
R_L = 16Ω, C-CUPL



20169751

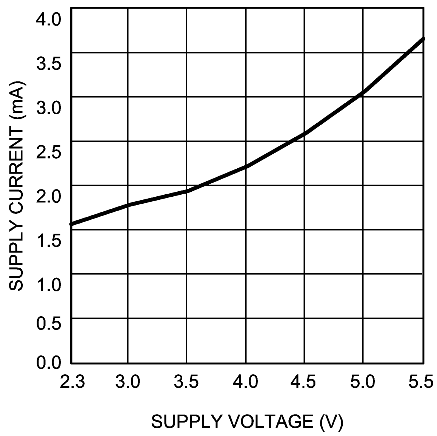
Supply Current vs Supply Voltage
R_L = 32Ω, C-CUPL



20169752

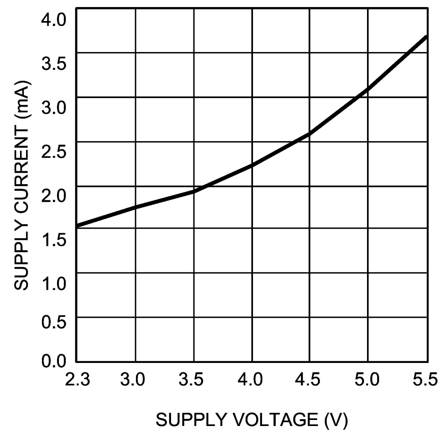
Typical Performance Characteristics (Continued)

Supply Current vs Supply Voltage
R_L = 16Ω, OCL



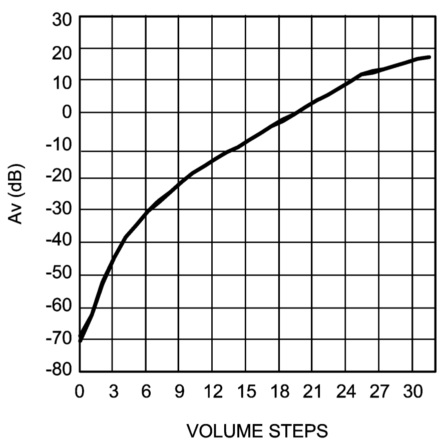
20169753

Supply Current vs Supply Voltage
R_L = 32Ω, OCL



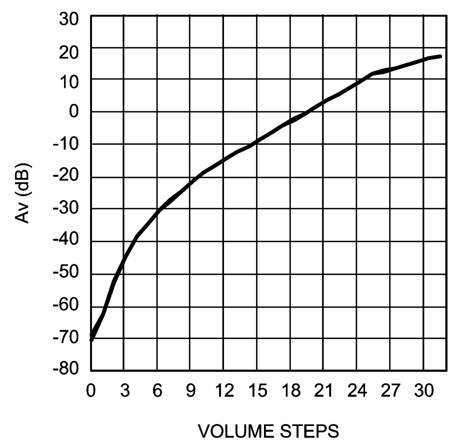
20169754

Gain vs Volume Steps
V_{CC} = 2.5V, R_L = 16Ω, OCL



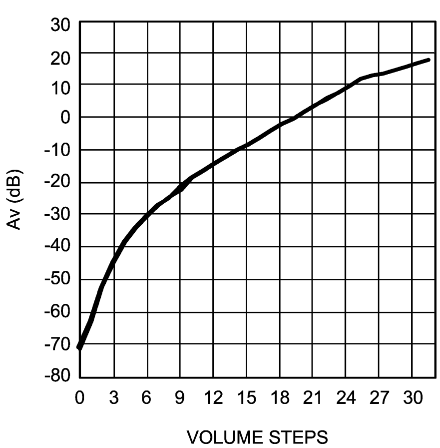
201697F7

Gain vs Volume Steps
V_{CC} = 3.6V, R_L = 16Ω, OCL



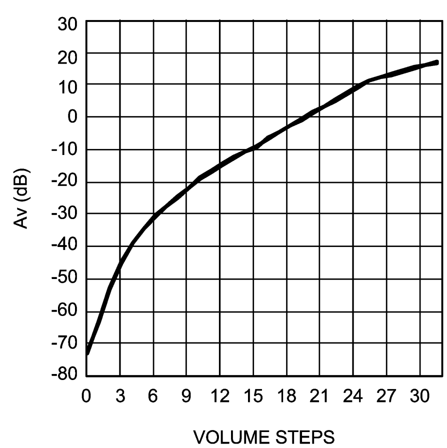
201697F5

Gain vs Volume Steps
V_{CC} = 5V, R_L = 16Ω, OCL



201697G4

Gain vs Volume Steps
V_{CC} = 2.5V, R_L = 16Ω, C-CUPL



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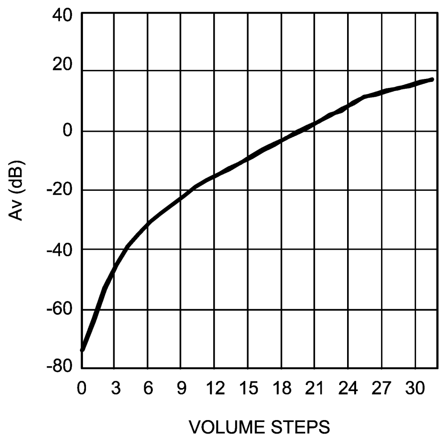
Typical Performance Characteristics (Continued)

Gain vs Volume Steps
V_{CC} = 3.6V, R_L = 16Ω, C-CUPL



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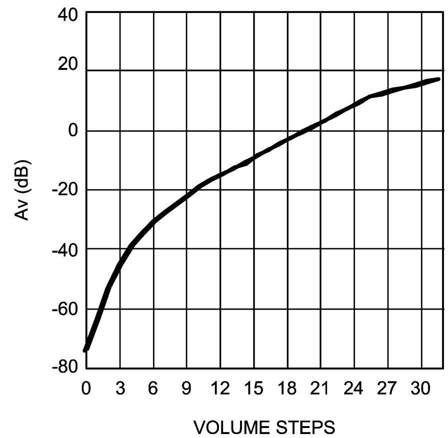
Gain vs Volume Steps
V_{CC} = 5V, R_L = 16Ω, C-CUPL



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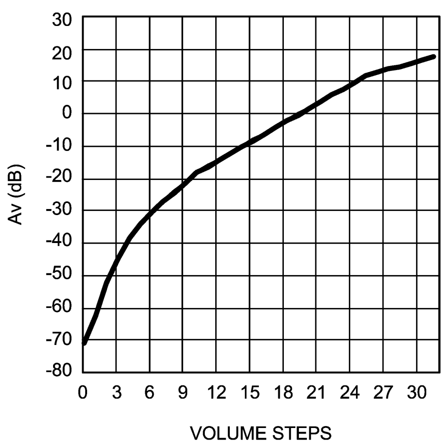
Gain vs Volume Steps
V_{CC} = 2.5V, R_L = 32Ω, OCL



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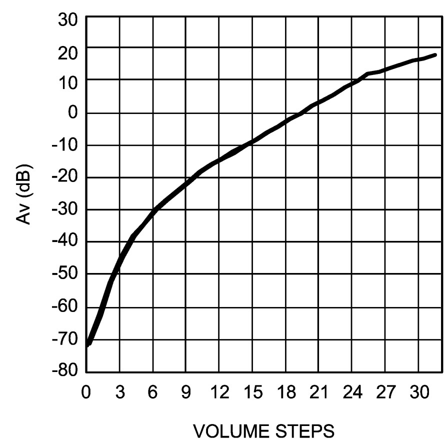
Gain vs Volume Steps
V_{CC} = 3.6V, R_L = 32Ω, OCL



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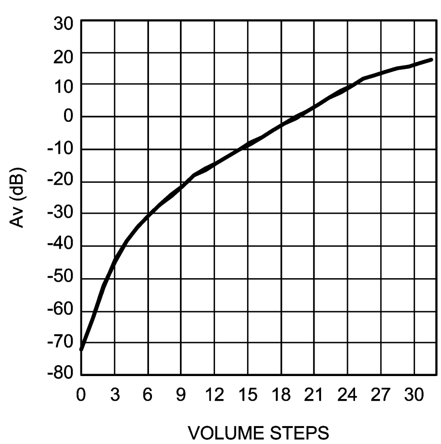
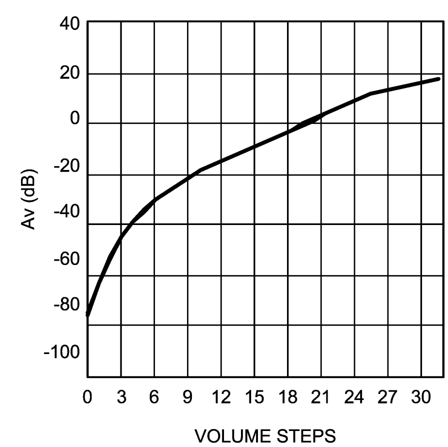
Gain vs Volume Steps
V_{CC} = 5V, R_L = 32Ω, OCL



201697G6

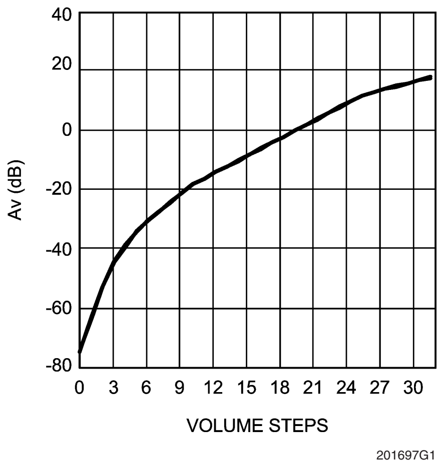
Gain vs Volume Steps
V_{CC} = 2.5V, R_L = 32Ω, C-CUPL



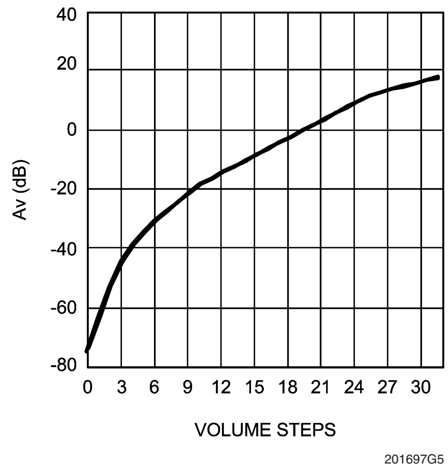
201697F8

Typical Performance Characteristics (Continued)

Gain vs Volume Steps
V_{CC} = 3.6V, R_L = 32Ω, C-CUPL



Gain vs Volume Steps
V_{CC} = 5V, R_L = 32Ω, C-CUPL



Application Information

AMPLIFIER CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4985 has three internal power amplifiers. Two of the amplifiers which amplify signals applied to their inputs, have internally configurable gain. The remaining third amplifier provides both half-supply output bias and AC ground return.

Loads, such as a headphone speaker, are connected between OUT1 and CNTGND or OUT2 and CNTGND. This configuration does not require an output coupling capacitor. The classical single-ended amplifier configuration, where one side of the load is connected to ground, requires large, expensive output coupling capacitors.

A configuration such as the one used in the LM4985 has a major advantage over single supply, single-ended amplifiers. Since the outputs OUT1, OUT2, and CNTGND are all biased at 1/2 V_{DD}, no net DC voltage exists across each load. This eliminates the need for output coupling capacitors which are required in a single-supply, single-ended amplifier configuration. Without output coupling capacitors in a typical single-supply, single-ended amplifier, the bias voltage is placed across the load resulting in both increased internal IC power dissipation and possible loudspeaker damage.

The LM4985 eliminates these output coupling capacitors when operating in Output Capacitor-less (OCL) mode. Unless shorted to ground, VoC is internally configured to apply a 1/2 V_{DD} bias voltage to a stereo headphone jack's sleeve. This voltage matches the bias voltage present on VoA and VoB outputs that drive the headphones. The headphones operate in a manner similar to a bridge-tied load (BTL). Because the same DC voltage is applied to both headphone speaker terminals this results in no net DC current flow through the speaker. AC current flows through a headphone speaker as an audio signal's output amplitude increases on the speaker's terminal.

The headphone jack's sleeve is not connected to circuit ground when used in OCL mode. Using the headphone output jack as a line-level output will place the LM4985's 1/2 V_{DD} bias voltage on a plug's sleeve connection. This presents no difficulty when the external equipment uses capacitively coupled inputs. For the very small minority of equipment that is DC coupled, the LM4985 monitors the current supplied by the amplifier that drives the headphone jack's sleeve. If this current exceeds 500mA_{PEAK}, the amplifier is shutdown, protecting the LM4985 and the external equipment.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier. When operating in capacitor-coupled mode (C-CUPL), Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = 2(V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

When operating in the OCL mode, the LM4985's three operational amplifiers produce a maximum power dissipation given in Equation 2:

$$P_{DMAX} = [2(V_{DD})^2 / (2\pi^2 R_L)] + [V_{DD}^2 / (4\pi R_L)] \quad (2)$$

The maximum power dissipation point obtained from Equation 1 or Equation 2 must not be greater than the power dissipation that results from Equation 3:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (3)$$

For package TMD12AAA, θ_{JA} = 190˚C/W. T_{JMAX} = 150˚C for the LM4985. Depending on the ambient temperature, T_A, of the system surroundings, Equation 3 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 2 is greater than that of Equation 3, then either the supply voltage must be decreased, the load impedance increased or T_A reduced.

For a typical application using a 3.6V power supply, with a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 144˚C provided that device operation is around the maximum power dissipation point. Thus, for typical applications, power dissipation is not an issue. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible.

Typical applications employ a regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4985. A bypass capacitor value in the range of 0.1µF to 1µF is recommended for C_S.

MICRO POWER SHUTDOWN

The LM4985's micropower shutdown is activated or deactivated through its I^2C digital interface . Please refer to Table 1 for the I^2C Address, Register Select, and Mode Control registers. Each amplifier within the LM4985 can be shutdown individually.

Please observe the following protocol when placing an individual amplifier channel in shutdown while the other channel remains active. The protocol requires activating both channels' shutdown simultaneously, then deactivating the shutdown of the channel whose output is desired (or leaving the desire channel in shutdown mode). Also, when operating in the C-CUPL mode, a short delay time is required between activating one channel after placing both channels in shutdown. If the user finds that both channels activate when only one was chosen, increase the delay.

SELECTION OF INPUT CAPACITOR SIZE

Amplifying the lowest audio frequencies requires a high value input coupling capacitor, C_i. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have little ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor.

In addition to system cost and size, turn on time is affected by the size of the input coupling capacitor C_i. A larger input

Application Information (Continued)

coupling capacitor requires more charge to reach its quiescent DC voltage. This charge comes from the output via the feedback Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on time can be minimized. A small value of C_i (in the range of 0.22µF to 0.68µF), is recommended.

MAXIMIZING OCL MODE CHANNEL-to-CHANNEL SEPARATION

The OCL mode AC ground return (CNT_GND pin) is shared by both amplifiers. As such, any resistance between the CNT_GND pin and the load will create a voltage divider with respect to the load resistance. In a typical circuit, the amount of CNT_GND resistance can be very small, but still significant. It is significant because of the relatively low load impedances for which the LM4985 was designed to drive: 16Ω to 32Ω. The ratio of this voltage divider will determine the magnitude of any residual signal present at the CNT_GND pin. It is this residual signal that leads to channel-to-channel separation (crosstalk) degradation.

For example, for a 60dB channel-to-channel separation while driving a 16Ω load, the resistance between the LM4985's CNT_GND pin and the load must be less than 16mΩ. This is achieved by ensuring that the trace that connects the CNT_GND pin to the headphone jack sleeve should be as short and massive as possible, given the physical constraints of any specific printed circuit board layout and design.

DEMONSTRATION BOARD AND PCB LAYOUT

Information concerning PCB layout considerations and demonstration board use and performance is found in Application Note AN-1452.

I²C Control Register

Table 1 shows the actions that are implemented by manipulating the bits within the two internal I²C control registers.

Table 1. LM4985 I²C Control Register Addressing and Data Format Chart

	LM4985 I2C Contorl Register Addressing and Data Chart								
I2C Address		A6	A5	A4	A3	A2	A1	A0	Function
		1	1	0	0	1	1	A0	
Register Select	D7	D6	D5	D4	D3	D2	RS1	RS0	
	0	0	0	0	0	0	0	0	Read and write the mode control register
	0	0	0	0	0	0	0	1	Read and write the volume control register
Mode Control Register	D7	D6	D5	D4	D3	D2	D1	D0	
		WT1	WT0	PHG	SDCH1	SDCH2	CHSEL1	CHSEL2	
	0	X	X	X	X	X	X	X	D7 must always be set to 0
	–	0	0	X	X	X	X	X	Wake-up time: 80ms (OCL), 250ms (C-CUPL)
	–	0	1	X	X	X	X	X	Wake-up time: 110ms (OCL), 450ms (C-CUPL)
	–	1	0	X	X	X	X	X	Wake-up time: 170ms (OCL), 850ms (C-CUPL)
	–	1	1	X	X	X	X	X	Wake-up time: 290ms (OCL), 1650ms (C-CUPL)
	–	X	X	1	X	X	X	X	Output capacitor-less mode **active**
	–	X	X	0	X	X	X	X	Output capacitor-less mode **inactive**
	–	X	X	X	0	0	X	X	Amplifier's SHUTDOWN mode **active**
	–	X	X	X	0	1	X	X	Illegal mode
	–	X	X	X	1	0	X	X	Illegal mode
	–	X	X	X	1	1	X	X	Amplifier's SHUTDOWN mode **inactive**
	–	X	X	X	X	X	0	02	Amplifier's Chan. 1 is **Input 1**, Chan 2. is **Input 2**
	–	X	X	X	X	X	0	1	Amplifier's Chan. 1 is **Input 1**, Chan 2. is **Input 1**
	–	X	X	X	X	X	1	0	Amplifier's Chan. 1 is **Input 2**, Chan 2. is **Input 2**
	–	X	X	X	X	X	1	1	Amplifier's Chan. 1 is **Input 2**, Chan 2. is **Input 1**

Volume Control Settings Binary Values

The minimum volume setting is set to –76dB when 00000 is loaded into the volume control register. Incrementing the volume control register in binary fashion increases the volume control setting, reaching full scale at 11111. Table C1 shows the value of the gain for each of the 32 binary volume control settings.

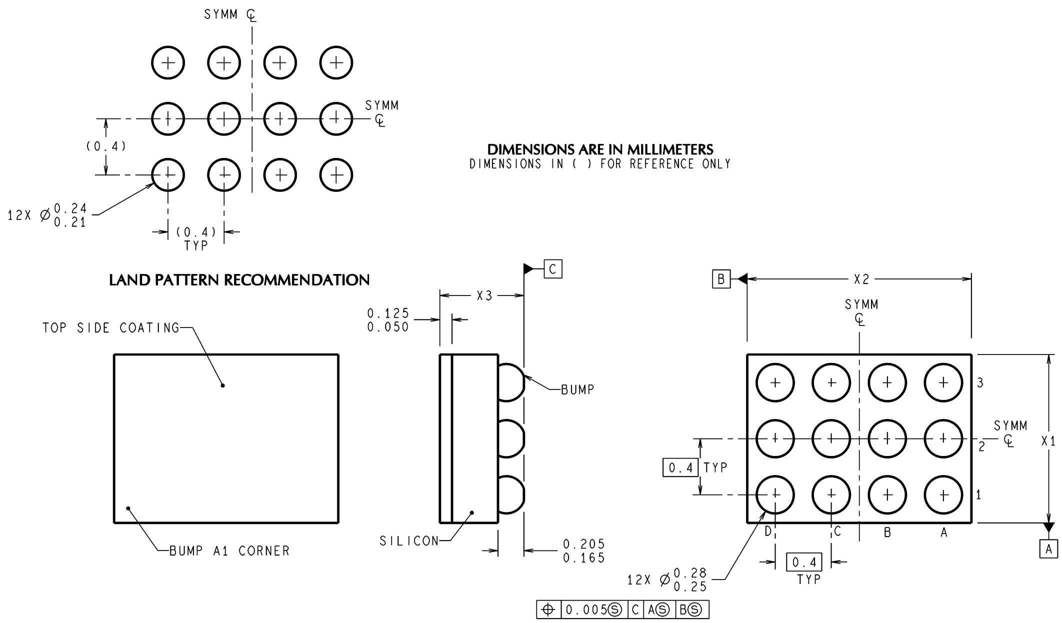
Table C1. Binary Values for the Different Volume Control Gain Settings

Gain	B4	B3	B2	B1	B0
18	1	1	1	1	1
17	1	1	1	1	0
16	1	1	1	0	1
15	1	1	1	0	0
14	1	1	0	1	1
13	1	1	0	1	0
12	1	1	0	0	1
10	1	1	0	0	0
8	1	0	1	1	1
6	1	0	1	1	0
4	1	0	1	0	1
2	1	0	1	0	0
0	1	0	0	1	1
–2	1	0	0	1	0
–4	1	0	0	0	1
–6	1	0	0	0	0
–8	0	1	1	1	1
–10	0	1	1	1	0
–12	0	1	1	0	1
–14	0	1	1	0	0
–16	0	1	0	1	1
–18	0	1	0	1	0
–21	0	1	0	0	1
–24	0	1	0	0	0
–27	0	0	1	1	1
–30	0	0	1	1	0
–34	0	0	1	0	1
–38	0	0	1	0	0
–44	0	0	0	1	1
–52	0	0	0	1	0
–62	0	0	0	0	1
–76	0	0	0	0	0

Revision History

Rev	Date	Description
1.0	05/17/06	Initial WEB release.

Physical Dimensions inches (millimeters) unless otherwise noted



TMD12XXX (Rev A)

micro SMD
Order Number LM4985TM
NS Package Number TMD12AAA
X_1 = 1.215mm ± 0.03mm X_2 = 1.615mm ± 0.03mm X_3 = 0.600mm ± 0.075mm

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