# OMAP-L138 C6-Integra™ DSP+ARM® Processor

**Check for Samples: OMAP-L138**

## 1 OMAP-L138 C6-Integra™ DSP+ARM® Processor

### 1.1 Features

- Highlights
  - Dual Core SoC
    - 375/456-MHz ARM926EJ-S™ RISC MPU
    - 375/456-MHz C674x Fixed/Floating-Point VLIW DSP
  - Supports TI's Basic Secure Boot
  - Enhanced Direct-Memory-Access Controller (EDMA3)
  - Serial ATA (SATA) Controller
  - DDR2/Mobile DDR Memory Controller
  - Two Multimedia Card (MMC)/Secure Digital (SD) Card Interface
  - LCD Controller
  - Video Port Interface (VPIF)
  - 10/100 Mb/s Ethernet MAC (EMAC)
  - Programmable Real-Time Unit Subsystem
  - Three Configurable UART Modules
  - USB 1.1 OHCI (Host) With Integrated PHY
  - USB 2.0 OTG Port With Integrated PHY
  - One Multichannel Audio Serial Port
  - Two Multichannel Buffered Serial Ports
- Dual Core SoC
  - 375/456-MHz ARM926EJ-S™ RISC MPU
  - 375/456-MHz C674x Fixed/Floating-Point VLIW DSP
- ARM926EJ-S Core
  - 32-Bit and 16-Bit (Thumb®) Instructions
  - DSP Instruction Extensions
  - Single Cycle MAC
  - ARM® Jazelle® Technology
  - EmbeddedICE-RT™ for Real-Time Debug
- ARM9 Memory Architecture
  - 16K-Byte Instruction Cache
  - 16K-Byte Data Cache
  - 8K-Byte RAM (Vector Table)
  - 64K-Byte ROM
- C674x™ Instruction Set Features
  - Superset of the C67x+™ and C64x+™ ISAs
  - Up to 3648/2746 C674x MIPS/MFLOPS
  - Byte-Addressable (8-/16-/32-/64-Bit Data)
  - 8-Bit Overflow Protection
  - Bit-Field Extract, Set, Clear
  - Normalization, Saturation, Bit-Counting
  - Compact 16-Bit Instructions
- C674x Two Level Cache Memory Architecture
  - 32K-Byte L1P Program RAM/Cache
  - 32K-Byte L1D Data RAM/Cache
  - 256K-Byte L2 Unified Mapped RAM/Cache
  - Flexible RAM/Cache Partition (L1 and L2)
- Enhanced Direct-Memory-Access Controller 3 (EDMA3):
  - 2 Channel Controllers
  - 3 Transfer Controllers
  - 64 Independent DMA Channels
  - 16 Quick DMA Channels
  - Programmable Transfer Burst Size
- TMS320C674x Floating-Point VLIW DSP Core
  - Load-Store Architecture With Non-Aligned Support
  - 64 General-Purpose Registers (32 Bit)
  - Six ALU (32-/40-Bit) Functional Units
    - Supports 32-Bit Integer, SP (IEEE Single Precision/32-Bit) and DP (IEEE Double Precision/64-Bit) Floating Point
    - Supports up to Four SP Additions Per Clock, Four DP Additions Every 2 Clocks
    - Supports up to Two Floating Point (SP or DP) Reciprocal Approximation (RCPxP) and Square-Root Reciprocal Approximation (RSQRxP) Operations Per Cycle
  - Two Multiply Functional Units
    - Mixed-Precision IEEE Floating Point Multiply Supported up to:
      - 2 SP x SP → SP Per Clock
      - 2 SP x SP → DP Every Two Clocks
      - 2 SP x DP → DP Every Three Clocks
      - 2 DP x DP → DP Every Four Clocks
    - Fixed Point Multiply Supports Two 32 x 32-Bit Multiplies, Four 16 x 16-Bit Multiplies, or Eight 8 x 8-Bit Multiplies per Clock Cycle, and Complex Multiples
  - Instruction Packing Reduces Code Size
  - All Instructions Conditional

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  - Hardware Support for Modulo Loop Operation
  - Protected Mode Operation
  - Exceptions Support for Error Detection and Program Redirection
- Software Support
  - TI DSP/BIOS™
  - Chip Support Library and DSP Library
- 128K-Byte RAM Shared Memory
- 1.8V or 3.3V LVCMOS IOs (except for USB and DDR2 interfaces)
- Two External Memory Interfaces:
  - EMIFA
    - NOR (8-/16-Bit-Wide Data)
    - NAND (8-/16-Bit-Wide Data)
    - 16-Bit SDRAM With 128 MB Address Space
  - DDR2/Mobile DDR Memory Controller
    - 16-Bit DDR2 SDRAM With 512 MB Address Space or
    - 16-Bit mDDR SDRAM With 256 MB Address Space
- Three Configurable 16550 type UART Modules:
  - With Modem Control Signals
  - 16-byte FIFO
  - 16x or 13x Oversampling Option
- LCD Controller
- Two Serial Peripheral Interfaces (SPI) Each With Multiple Chip-Selects
- Two Multimedia Card (MMC)/Secure Digital (SD) Card Interface with Secure Data I/O (SDIO) Interfaces
- Two Master/Slave Inter-Integrated Circuit ($I^2C$ Bus™)
- One Host-Port Interface (HPI) With 16-Bit-Wide Muxed Address/Data Bus For High Bandwidth
- Programmable Real-Time Unit Subsystem (PRUSS)
  - Two Independent Programmable Realtime Unit (PRU) Cores
    - 32-Bit Load/Store RISC architecture
    - 4K Byte instruction RAM per core
    - 512 Bytes data RAM per core
    - PRU Subsystem (PRUSS) can be disabled via software to save power
    - Register 30 of each PRU is exported from the subsystem in addition to the normal R31 output of the PRU cores.
  - Standard power management mechanism
    - Clock gating
    - Entire subsystem under a single PSC clock gating domain
  - Dedicated interrupt controller
  - Dedicated switched central resource
- USB 1.1 OHCI (Host) With Integrated PHY (USB1)
- USB 2.0 OTG Port With Integrated PHY (USB0)
  - USB 2.0 High-/Full-Speed Client
  - USB 2.0 High-/Full-/Low-Speed Host
  - End Point 0 (Control)
  - End Points 1,2,3,4 (Control, Bulk, Interrupt or ISOC) Rx and Tx
- One Multichannel Audio Serial Port:
  - Two Clock Zones and 16 Serial Data Pins
  - Supports TDM, I2S, and Similar Formats
  - DIT-Capable
  - FIFO buffers for Transmit and Receive
- Two Multichannel Buffered Serial Ports:
  - Supports TDM, I2S, and Similar Formats
  - AC97 Audio Codec Interface
  - Telecom Interfaces (ST-Bus, H100)
  - 128-channel TDM
  - FIFO buffers for Transmit and Receive
- 10/100 Mb/s Ethernet MAC (EMAC):
  - IEEE 802.3 Compliant
  - MII Media Independent Interface
  - RMII Reduced Media Independent Interface
  - Management Data I/O (MDIO) Module
- Video Port Interface (VPIF):
  - Two 8-bit SD (BT.656), Single 16-bit or Single Raw (8-/10-/12-bit) Video Capture Channels
  - Two 8-bit SD (BT.656), Single 16-bit Video Display Channels
- Universal Parallel Port (uPP):
  - High-Speed Parallel Interface to FPGAs and Data Converters
  - Data Width on Each of Two Channels is 8- to 16-bit Inclusive
  - Single Data Rate or Dual Data Rate Transfers
  - Supports Multiple Interfaces with START, ENABLE and WAIT Controls
- Serial ATA (SATA) Controller:
  - Supports SATA I (1.5 Gbps) and SATA II (3.0 Gbps)
  - Supports all SATA Power Management Features
  - Hardware-Assisted Native Command Queueing (NCQ) for up to 32 Entries
  - Supports Port Multiplier and Command-Based Switching
- Real-Time Clock With 32 KHz Oscillator and Separate Power Rail
- Three 64-Bit General-Purpose Timers (Each Configurable as Two 32-Bit Timers)
- One 64-bit General-Purpose/Watchdog Timer (Configurable as Two 32-bit General-Purpose Timers)


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- **Two Enhanced Pulse Width Modulators (eHRPWM):**
  - **Dedicated 16-Bit Time-Base Counter With Period And Frequency Control**
  - **6 Single Edge, 6 Dual Edge Symmetric or 3 Dual Edge Asymmetric Outputs**
  - **Dead-Band Generation**
  - **PWM Chopping by High-Frequency Carrier**
  - **Trip Zone Input**
- **Three 32-Bit Enhanced Capture Modules (eCAP):**
  - **Configurable as 3 Capture Inputs or 3 Auxiliary Pulse Width Modulator (APWM) outputs**
  - **Single Shot Capture of up to Four Event Time-Stamps**
- **361-Ball Pb-Free Plastic Ball Grid Array (PBGA) [ZCE Suffix], 0.65-mm Ball Pitch**
- **361-Ball Pb-Free Plastic Ball Grid Array (PBGA) [ZWT Suffix], 0.80-mm Ball Pitch**
- **Commercial, Extended or Industrial Temperature**

## 1.2 Description

The OMAP-L138 C6-Integra™ DSP+ARM® processor is a low-power applications processor based on an ARM926EJ-S™ and a C674x DSP core. It provides significantly lower power than other members of the TMS320C6000™ platform of DSPs.

The device enables OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution.

The dual-core architecture of the device provides benefits of both DSP and Reduced Instruction Set Computer (RISC) technologies, incorporating a high-performance TMS320C674x DSP core and an ARM926EJ-S core.

The ARM926EJ-S is a 32-bit RISC processor core that performs 32-bit or 16-bit instructions and processes 32-bit, 16-bit, or 8-bit data. The core uses pipelining so that all parts of the processor and memory system can operate continuously.

The ARM core has a coprocessor 15 (CP15), protection module, and Data and program Memory Management Units (MMUs) with table look-aside buffers. It has separate 16K-byte instruction and 16K-byte data caches. Both are four-way associative with virtual index virtual tag (VIVT). The ARM core also has a 8KB RAM (Vector Table) and 64KB ROM.

The device DSP core uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 32KB direct mapped cache and the Level 1 data cache (L1D) is a 32KB 2-way set-associative cache. The Level 2 program cache (L2P) consists of a 256KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or combinations of the two. Although the DSP L2 is accessible by ARM and other hosts in the system, an additional 128KB RAM shared memory is available for use by other hosts without affecting DSP performance.

For security enabled devices, TI's Basic Secure Boot allows users to protect proprietary intellectual property and prevents external entities from modifying user-developed algorithms. By starting from a hardware-based "root-of-trust", the secure boot flow guarantees a known good starting point for code execution. By default, the JTAG port is locked down to prevent emulation and debug attacks but can be enabled during the secure boot process during application development. The boot modules themselves are encrypted while sitting in external non-volatile memory, such as flash or EEPROM, and are decrypted and authenticated when loaded during secure boot. This protects the users' IP and enables them to securely set up the system and begin device operation with known, trusted code. Basic Secure Boot utilizes either SHA-1 or SHA-256, and AES-128 for boot image validation. It also uses AES-128 for boot image encryption. The secure boot flow employs a multi-layer encryption scheme which not only protects the boot process but offers the ability to securely upgrade boot and application software code. A 128-bit device-specific cipher key, known only to the device and generated using a NIST-800-22 certified random

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number generator, is used to protect user encryption keys. When an update is needed, the customer creates a new encrypted image using its encryption keys. Then the device can acquire the image via an external interface, such as Ethernet, and overwrite the existing code. For more details on the supported security features or TI's Basic Secure Boot, refer to the *TMS320C674x/OMAP-L1x Processor Security User's Guide* (SPRUGQ9).

The peripheral set includes: a 10/100 Mb/s Ethernet MAC (EMAC) with a Management Data Input/Output (MDIO) module; one USB2.0 OTG interface; one USB1.1 OHCI interface; two inter-integrated circuit (I2C) Bus interfaces; one multichannel audio serial port (McASP) with 16 serializers and FIFO buffers; two multichannel buffered serial ports (McBSP) with FIFO buffers; two SPI interfaces with multiple chip selects; four 64-bit general-purpose timers each configurable (one configurable as watchdog); a configurable 16-bit host port interface (HPI) ; up to 9 banks of 16 pins of general-purpose input/output (GPIO) with programmable interrupt/event generation modes, multiplexed with other peripherals; three UART interfaces (each with $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$); two enhanced high-resolution pulse width modulator (eHRPWM) peripherals; 3 32-bit enhanced capture (eCAP) module peripherals which can be configured as 3 capture inputs or 3 auxiliary pulse width modulator (APWM) outputs; and 2 external memory interfaces: an asynchronous and SDRAM external memory interface (EMIFA) for slower memories or peripherals, and a higher speed DDR2/Mobile DDR controller.

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the device and a network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode. Additionally an Management Data Input/Output (MDIO) interface is available for PHY configuration. The EMAC supports both MII and RMII interfaces.

The SATA controller provides a high-speed interface to mass data storage devices. The SATA controller supports both SATA I (1.5 Gbps) and SATA II (3.0 Gbps).

The Universal Parallel Port (uPP) provides a high-speed interface to many types of data converters, FPGAs or other parallel devices. The UPP supports programmable data widths between 8- to 16-bits on each of two channels. Single-data rate and double-data rate transfers are supported as well as START, ENABLE and WAIT signals to provide control for a variety of data converters.

A Video Port Interface (VPIF) is included providing a flexible video input/output port.

The rich peripheral set provides the ability to control external peripheral devices and communicate with external processors. For details on each of the peripherals, see the related sections later in this document and the associated peripheral reference guides.

The device has a complete set of development tools for the ARM and DSP. These include C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a Windows™ debugger interface for visibility into source code execution.

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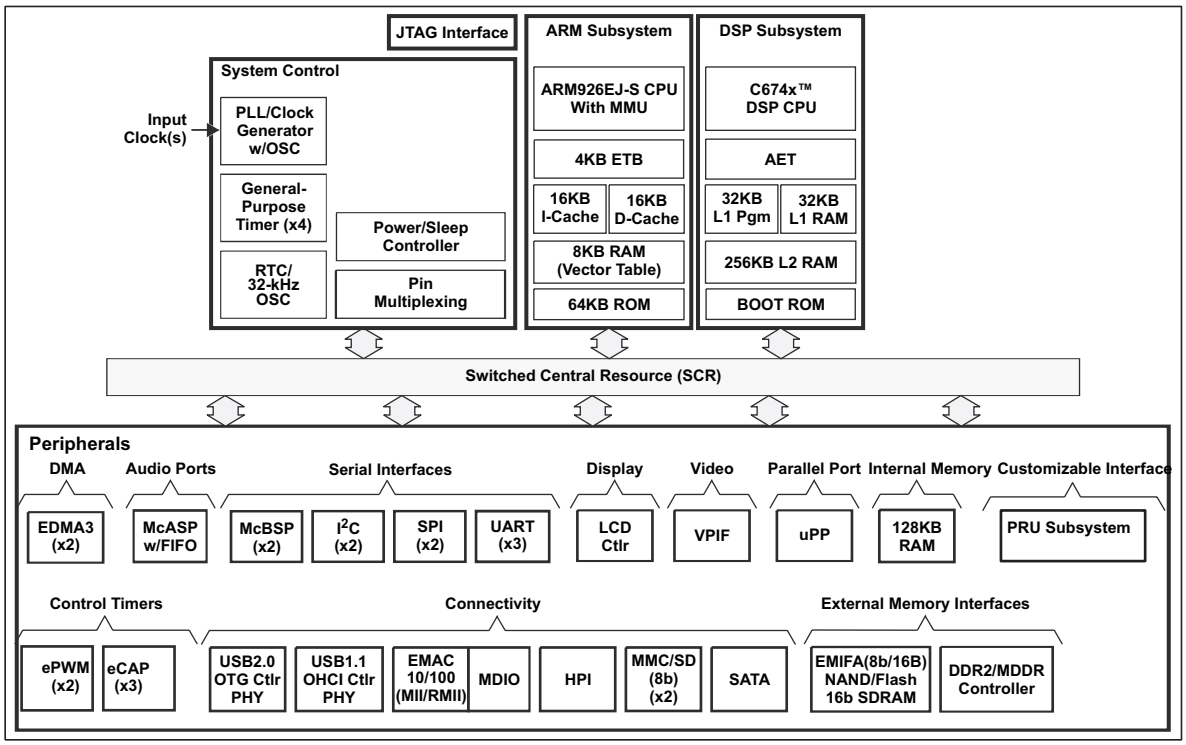
## 1.3 Functional Block Diagram




(1) Note: Not all peripherals are available at the same time due to multiplexing.

**Figure 1-1. Functional Block Diagram**

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## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the changes made to the SPRS586B device-specific data manual to make it an SPRS586C revision.

### Revision History

| See | ADDITIONS/MODIFICATIONS/DELETIONS |
|---|---|
| Section 1.1 Features | Added a bullet about TI's Basic Secure Boot. |
| Section 1.2 Description | Added a paragraph about TI's Basic Secure Boot. |
| Section 2 Device Overview | Moved Documentation Support to Section 6, Device and Documentation Support.<br>Table 2-1, Characteristics of OMAP-L138:<br>• Corrected DDR2 max to 156 MHz and mDDR max to 150 MHz. |
| Section 2.8 Terminal Functions | Table 2-11, Serial Peripheral Interface (SPI) Terminal Functions:<br>• Changed signal type to I/O for signal C16, C18, G17, and H17.<br>Table 2-14, Enhanced Pulse Width Modulator (eHRPWM) Terminal Functions:<br>• Changed signal type to Input for signal A4, C16, and D2.<br>Table 2-22, Ethernet Media Access Controller (EMAC) Terminal Functions:<br>• Changed signal type to I/O for signal W18. |
| Section 2.9 Unused Pin Configurations | Table 2-32, Unused USB0 and USB1 Signal Configurations:<br>• Updated USB1_DM and USB1_DP. |
| Section 4 Device Operating Conditions | Section 4.1, Absolute Maximum Ratings Over Operating Junction Temperature Range:<br>• Updated ESD Stress Voltage MAX values. |
| | Section 4.2, Recommended Operating Conditions:<br>• Added DVDD18 under Supply Voltage. |
| Section 5.3 Power Supplies | Section 5.3.1, Power-On Sequence:<br>• Changed step 1 regarding RTC (RTC_CVDD).<br>• Changed VDDA_12_PLL0 to PLL0_VDDA, and VDDA_12_PLL1 to PLL1_VDDA in step 2b. |
| Section 5.6 Clock PLLs | Section 5.6.1, PLL Device-Specific Information<br>• Updated PLLn to PLL0 or PLL1, as appropriate in Figure 5-8.<br>• Added paragraph below figure.<br>• Updated PLLREF in Table 5-4.<br>Section 5.6.3, Dynamic Voltage and Frequency Scaling (DVFS):<br>• Updated Maximum internal clock frequency specifications in Table 5-5. |
| Section 5.10.6 EMIFA Electrical Data/Timing | Table 5-23, Timing Requirements for EMIFA Asynchronous Memory Interface:<br>• Updated parameter E.<br>Table 5-24, Switching Characteristics for EMIFA Asynchronous Memory Interface:<br>• Updated parameter 1.<br>Figure 5-14, Asynchronous Memory Read Timing for EMIFA:<br>• Removed unused parameters 29 and 30.<br>Figure 5-15, Asynchronous Memory Write Timing for EMIFA:<br>• Removed unused parameters 31 and 32. |
| Section 5.23.2 Management Data Input/Output (MDIO) Electrical Data/Timing: | Table 5-107, Timing Requirements for (MDIO) Input:<br>• Updated parameters 4 and 5. |
| Section 5.24.1 LCD Interface Display Driver (LIDD Mode) | Table 5-111, Switching Characteristics Over Recommended Operating Conditions for LCD LIDD Mode :<br>• Updated description for parameters 12 and 13 for LCD_PCLK. |
| Section 5.29 Enhanced High-Resolution Pulse-Width Modulator (eHRPWM) | Table 5-127, eHRPWM Module Control and Status Registers Grouped by Submodule<br>• Updated offset addresses for HRCNFG. |
| Section 5.29.2 Trip-Zone Input Timing | Table 5-131, High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz):<br>• Updated note regarding MEM step size. |

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## Revision History (continued)

| See | ADDITIONS/MODIFICATIONS/DELETIONS |
|---|---|
| Section 5.31.1 Clock Source | Figure 5-85, Clock Source:<br>• Replaced Real Time Clock with RTC Power Source. |
| Section 6.1 DeviceSupport | Figure 6-1, Device Nomenclature:<br>• Added Basic Secure Boot marking.<br>• Added note referring to Silicon B. |


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# 2 Device Overview

## 2.1 Device Characteristics

Table 2-1 provides an overview of the device. The table shows significant features of the device, including the capacity of on-chip RAM, peripherals, and the package type with pin count.

**Table 2-1. Characteristics of OMAP-L138**

| HARDWARE FEATURES | | OMAP-L138 |
|---|---|---|
| Peripherals<br>Not all peripherals pins are available at the same time (for more detail, see the Device Configurations section). | DDR2/mDDR Controller | DDR2, 16-bit bus width, up to 156 MHz<br>Mobile DDR, 16-bit bus width, up to 150 MHz |
| | EMIFA | Asynchronous (8/16-bit bus width) RAM, Flash,<br>16-bit SDRAM, NOR, NAND |
| | Flash Card Interface | 2 MMC and SD cards supported |
| | EDMA3 | 64 independent channels, 16 QDMA channels,<br>2 channel controllers, 3 transfer controllers |
| | Timers | 4 64-Bit General Purpose (each configurable as 2 separate 32-bit timers, one configurable as Watch Dog) |
| | UART | 3 (each with RTS and CTS flow control) |
| | SPI | 2 (Each with one hardware chip select) |
| | $I^2C$ | 2 (both Master/Slave) |
| | Multichannel Audio Serial Port [McASP] | 1 (each with transmit/receive, FIFO buffer, 16 serializers) |
| | Multichannel Buffered Serial Port [McBSP] | 2 (each with transmit/receive, FIFO buffer, 16) |
| | 10/100 Ethernet MAC with Management Data I/O | 1 (MII or RMII Interface) |
| | eHRPWM | 4 Single Edge, 4 Dual Edge Symmetric, or<br>2 Dual Edge Asymmetric Outputs |
| | eCAP | 3 32-bit capture inputs or 3 32-bit auxiliary PWM outputs |
| | UHPI | 1 (16-bit multiplexed address/data) |
| | USB 2.0 (USB0) | High-Speed OTG Controller with on-chip OTG PHY |
| | USB 1.1 (USB1) | Full-Speed OHCI (as host) with on-chip PHY |
| | General-Purpose Input/Output Port | 9 banks of 16-bit |
| | LCD Controller | 1 |
| | SATA Controller | 1 (Supports both SATA I and SATAII) |
| | Universal Parallel Port (uPP) | 1 |
| | Video Port Interface (VPIF) | 1 (video in and video out) |
| | PRU Subsystem (PRUSS) | 2 Programmable PRU Cores |
| On-Chip Memory | Size (Bytes) | 488KB RAM |
| | Organization | **DSP**<br>32KB L1 Program (L1P)/Cache (up to 32KB)<br>32KB L1 Data (L1D)/Cache (up to 32KB)<br>256KB Unified Mapped RAM/Cache (L2)<br>DSP Memories can be made accessible to ARM, EDMA3, and other peripherals.<br>**ARM**<br>16KB I-Cache<br>16KB D-Cache<br>8KB RAM (Vector Table)<br>64KB ROM<br>**ADDITIONAL SHARED MEMORY**<br>128KB RAM |
| Security | Secure Boot | TI Basic Secure Boot |
| C674x CPU ID + CPU Rev ID | Control Status Register (CSR.[31:16]) | 0x1400 |
| C674x Megamodule Revision | Revision ID Register (MM_REVID[15:0]) | 0x0000 |
| JTAG BSDL_ID | DEVIDR0 Register | 0x0B7D_102F |

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**Table 2-1. Characteristics of OMAP-L138 (continued)**

| HARDWARE FEATURES | | OMAP-L138 |
|---|---|---|
| CPU Frequency | MHz | 674x DSP 375 MHz (1.2V) or 456 MHz (1.3V) |
| | | ARM926 375 MHz (1.2V) or 456 MHz (1.3V) |
| Voltage | Core (V) | Variable (1.2V-1.0V) for 375 MHz version<br>Variable (1.3V-1.0V) for 456 MHz version |
| | I/O (V) | 1.8V or 3.3 V |
| Packages | | 13 mm x 13 mm, 361-Ball 0.65 mm pitch, PBGA (ZCE) |
| | | 16 mm x 16 mm, 361-Ball 0.80 mm pitch, PBGA (ZWT) |
| Product Status(1) | Product Preview (PP),<br>Advance Information (AI),<br>or Production Data (PD) | 375 MHz versions - PD<br>456 MHz versions - PD |

(1) ADVANCE INFORMATION concerns new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice. PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

## 2.2 Device Compatibility

The ARM926EJ-S RISC CPU is compatible with other ARM9 CPUs from ARM Holdings plc.

The C674x DSP core is code-compatible with the C6000™ DSP platform and supports features of both the C64x+ and C67x+ DSP families.

## 2.3 ARM Subsystem

The ARM Subsystem includes the following features:

- ARM926EJ-S RISC processor
- ARMv5TEJ (32/16-bit) instruction set
- Little endian
- System Control Co-Processor 15 (CP15)
- MMU
- 16KB Instruction cache
- 16KB Data cache
- Write Buffer
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)
- ARM Interrupt controller

### *2.3.1 ARM926EJ-S RISC CPU*

The ARM Subsystem integrates the ARM926EJ-S processor. The ARM926EJ-S processor is a member of ARM9 family of general-purpose microprocessors. This processor is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM926EJ-S processor supports the 32-bit ARM and 16 bit THUMB instruction sets, enabling the user to trade off between high performance and high code density. Specifically, the ARM926EJ-S processor supports the ARMv5TEJ instruction set, which includes features for efficient execution of Java byte codes, providing Java performance similar to Just in Time (JIT) Java interpreter, but without associated code overhead.

The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debug. The ARM926EJ-S processor has a Harvard architecture and provides a complete high performance subsystem, including:

- ARM926EJ -S integer core
- CP15 system control coprocessor
- Memory Management Unit (MMU)


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- Separate instruction and data caches
- Write buffer
- Separate instruction and data (internal RAM) interfaces
- Separate instruction and data AHB bus interfaces
- Embedded Trace Module and Embedded Trace Buffer (ETM/ETB)

For more complete details on the ARM9, refer to the *ARM926EJ-S Technical Reference Manual*, available at http://www.arm.com

### 2.3.2 CP15

The ARM926EJ-S system control coprocessor (CP15) is used to configure and control instruction and data caches, Memory Management Unit (MMU), and other ARM subsystem functions. The CP15 registers are programmed using the MRC and MCR ARM instructions, when the ARM in a privileged mode such as supervisor or system mode.

### 2.3.3 MMU

A single set of two level page tables stored in main memory is used to control the address translation, permission checks and memory region attributes for both data and instruction accesses. The MMU uses a single unified Translation Lookaside Buffer (TLB) to cache the information held in the page tables. The MMU features are:

- Standard ARM architecture v4 and v5 MMU mapping sizes, domains and access protection scheme.
- Mapping sizes are:
  - 1MB (sections)
  - 64KB (large pages)
  - 4KB (small pages)
  - 1KB (tiny pages)
- Access permissions for large pages and small pages can be specified separately for each quarter of the page (subpage permissions)
- Hardware page table walks
- Invalidate entire TLB, using CP15 register 8
- Invalidate TLB entry, selected by MVA, using CP15 register 8
- Lockdown of TLB entries, using CP15 register 10

### 2.3.4 Caches and Write Buffer

The size of the Instruction cache is 16KB, Data cache is 16KB. Additionally, the caches have the following features:

- Virtual index, virtual tag, and addressed using the Modified Virtual Address (MVA)
- Four-way set associative, with a cache line length of eight words per line (32-bytes per line) and with two dirty bits in the Dcache
- Dcache supports write-through and write-back (or copy back) cache operation, selected by memory region using the C and B bits in the MMU translation tables
- Critical-word first cache refilling
- Cache lockdown registers enable control over which cache ways are used for allocation on a line fill, providing a mechanism for both lockdown, and controlling cache corruption
- Dcache stores the Physical Address TAG (PA TAG) corresponding to each Dcache entry in the TAG RAM for use during the cache line write-backs, in addition to the Virtual Address TAG stored in the TAG RAM. This means that the MMU is not involved in Dcache write-back operations, removing the possibility of TLB misses related to the write-back address.
- Cache maintenance operations provide efficient invalidation of, the entire Dcache or Icache, regions of the Dcache or Icache, and regions of virtual memory.

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The write buffer is used for all writes to a noncachable bufferable region, write-through region and write misses to a write-back region. A separate buffer is incorporated in the Dcache for holding write-back for cache line evictions or cleaning of dirty cache lines. The main write buffer has 16-word data buffer and a four-address buffer. The Dcache write-back has eight data word entries and a single address entry.

### 2.3.5 Advanced High-Performance Bus (AHB)

The ARM Subsystem uses the AHB port of the ARM926EJ-S to connect the ARM to the Config bus and the external memories. Arbiters are employed to arbitrate access to the separate D-AHB and I-AHB by the Config Bus and the external memories bus.

### 2.3.6 Embedded Trace Macrocell (ETM) and Embedded Trace Buffer (ETB)

To support real-time trace, the ARM926EJ-S processor provides an interface to enable connection of an Embedded Trace Macrocell (ETM). The ARM926ES-J Subsystem in the device also includes the Embedded Trace Buffer (ETB). The ETM consists of two parts:

- Trace Port provides real-time trace capability for the ARM9.
- Triggering facilities provide trigger resources, which include address and data comparators, counter, and sequencers.

The device trace port is not pinned out and is instead only connected to the Embedded Trace Buffer. The ETB has a 4KB buffer memory. ETB enabled debug tools are required to read/interpret the captured trace data.

### 2.3.7 ARM Memory Mapping

By default the ARM has access to most on and off chip memory areas, including the DSP Internal memories, EMIFA, DDR2, and the additional 128K byte on chip shared SRAM. Likewise almost all of the on chip peripherals are accessible to the ARM by default.

See Table 2-4 for a detailed top level device memory map that includes the ARM memory space.


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## 2.4 DSP Subsystem

The DSP Subsystem includes the following features:

- C674x DSP CPU
- 32KB L1 Program (L1P)/Cache (up to 32KB)
- 32KB L1 Data (L1D)/Cache (up to 32KB)
- 256KB Unified Mapped RAM/Cache (L2)
- Boot ROM (cannot be used for application code)
- Little endian

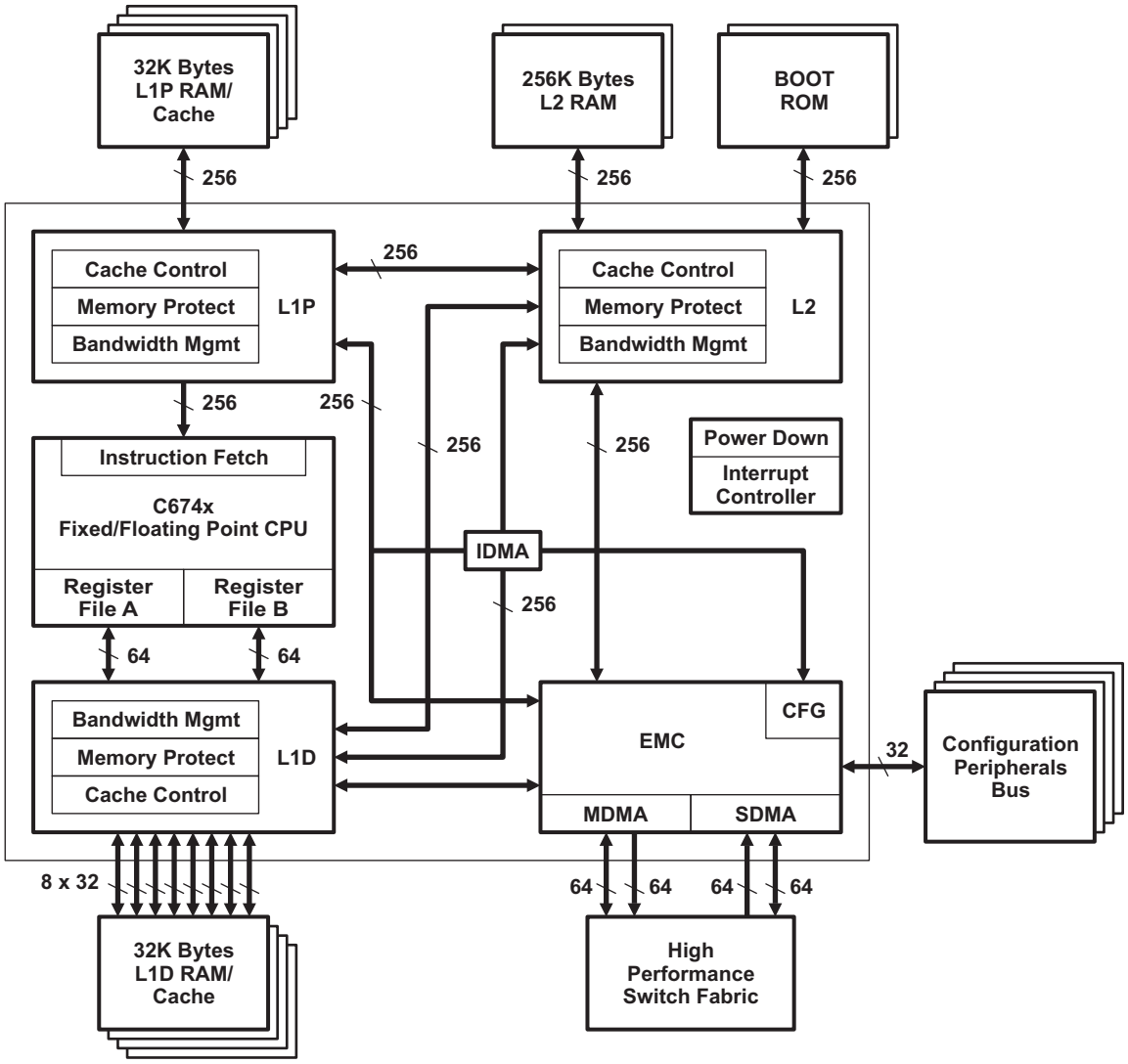


**Figure 2-1. C674x Megamodule Block Diagram**

### 2.4.1 C674x DSP CPU Description

The C674x Central Processing Unit (CPU) consists of eight functional units, two register files, and two data paths as shown in Figure 2-2. The two general-purpose register files (A and B) each contain 32 32-bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40-bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register).

The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

The C674x CPU combines the performance of the C64x+ core with the floating-point capabilities of the C67x+ core.

Each C674x .M unit can perform one of the following each clock cycle: one 32 x 32 bit multiply, one 16 x 32 bit multiply, two 16 x 16 bit multiplies, two 16 x 32 bit multiplies, two 16 x 16 bit multiplies with add/subtract capabilities, four 8 x 8 bit multiplies, four 8 x 8 bit multiplies with add operations, and four 16 x 16 multiplies with add/subtract capabilities (including a complex multiply). There is also support for Galois field multiplication for 8-bit and 32-bit data. Many communications algorithms such as FFTs and modems require complex multiplication. The complex multiply (CMPY) instruction takes for 16-bit inputs and produces a 32-bit real and a 32-bit imaginary output. There are also complex multiplies with rounding capability that produces one 32-bit packed output that contain 16-bit real and 16-bit imaginary values. The 32 x 32 bit multiply instructions provide the extended precision necessary for high-precision algorithms on a variety of signed and unsigned 32-bit data types.

The .L or (Arithmetic Logic Unit) now incorporates the ability to do parallel add/subtract operations on a pair of common inputs. Versions of this instruction exist to work on 32-bit data or on pairs of 16-bit data performing dual 16-bit add and subtracts in parallel. There are also saturated forms of these instructions.

The C674x core enhances the .S unit in several ways. On the previous cores, dual 16-bit MIN2 and MAX2 comparisons were only available on the .L units. On the C674x core they are also available on the .S unit which increases the performance of algorithms that do searching and sorting. Finally, to increase data packing and unpacking throughput, the .S unit allows sustained high performance for the quad 8-bit/16-bit and dual 16-bit instructions. Unpack instructions prepare 8-bit data for parallel 16-bit operations. Pack instructions return parallel results to output precision including saturation support.

Other new features include:

- **SPLOOP** - A small instruction buffer in the CPU that aids in creation of software pipelining loops where multiple iterations of a loop are executed in parallel. The SPLOOP buffer reduces the code size associated with software pipelining. Furthermore, loops in the SPLOOP buffer are fully interruptible.
- **Compact Instructions** - The native instruction size for the C6000 devices is 32 bits. Many common instructions such as MPY, AND, OR, ADD, and SUB can be expressed as 16 bits if the C674x compiler can restrict the code to use certain registers in the register file. This compression is performed by the code generation tools.
- **Instruction Set Enhancement** - As noted above, there are new instructions such as 32-bit multiplications, complex multiplications, packing, sorting, bit manipulation, and 32-bit Galois field multiplication.
- **Exceptions Handling** - Intended to aid the programmer in isolating bugs. The C674x CPU is able to detect and respond to exceptions, both from internally detected sources (such as illegal op-codes) and from system events (such as a watchdog time expiration).
- **Privilege** - Defines user and supervisor modes of operation, allowing the operating system to give a basic level of protection to sensitive resources. Local memory is divided into multiple pages, each with read, write, and execute permissions.


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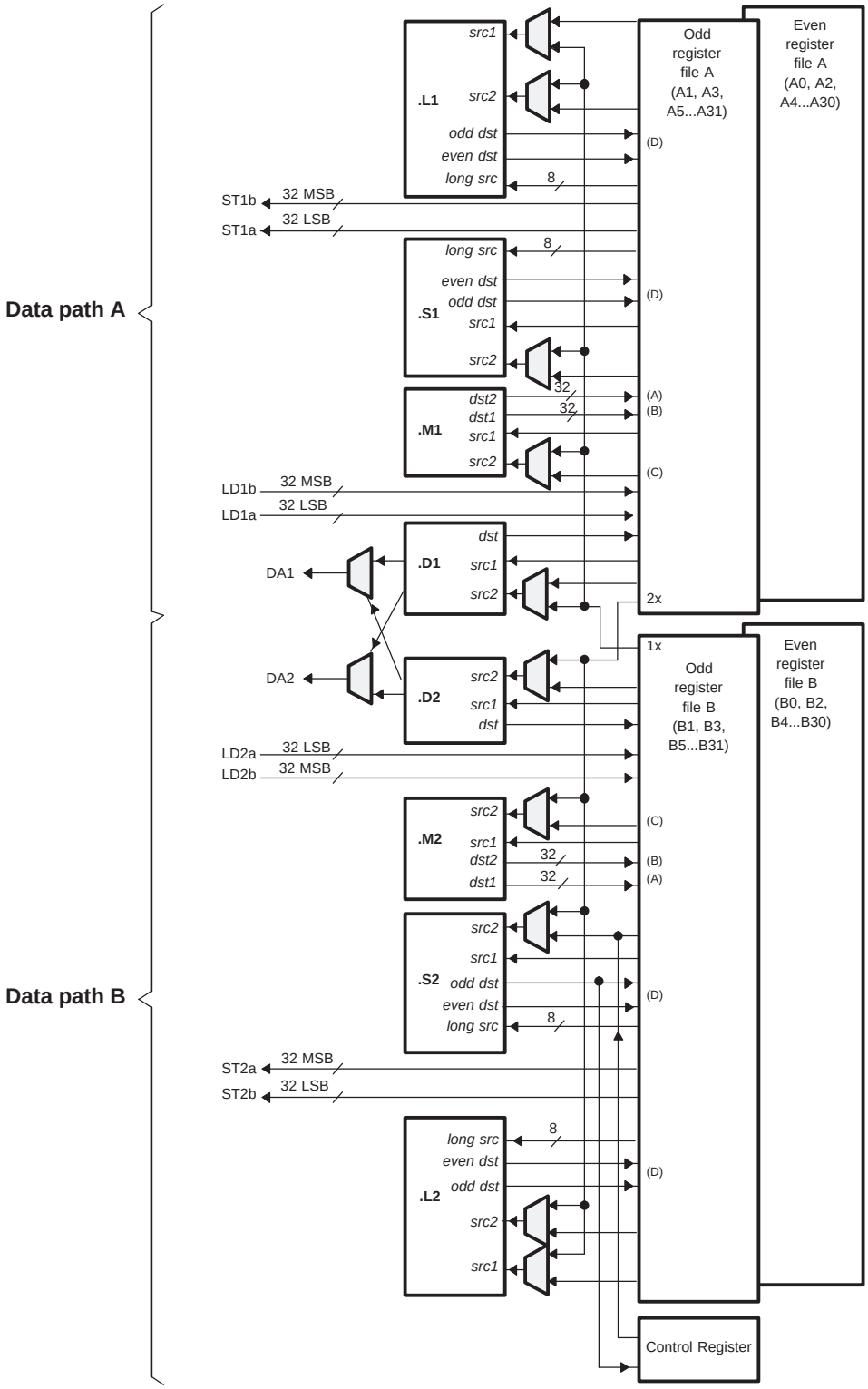
- **Time-Stamp Counter** - Primarily targeted for Real-Time Operating System (RTOS) robustness, a free-running time-stamp counter is implemented in the CPU which is ***not*** sensitive to system stalls.

For more details on the C674x CPU and its enhancements over the C64x architecture, see the following documents:

- *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (literature number SPRUFE8)
- *TMS320C64x Technical Overview* (literature number SPRU395)




A. On .M unit, *dst2* is 32 MSB.
B. On .M unit, *dst1* is 32 LSB.
C. On C64x CPU .M unit, *src2* is 32 bits; on C64x+ CPU .M unit, *src2* is 64 bits.
D. On .L and .S units, *odd dst* connects to odd register files and *even dst* connects to even register files.

**Figure 2-2. TMS320C674x CPU (DSP Core) Data Paths**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### 2.4.2 DSP Memory Mapping

The DSP memory map is shown in Section 2.5.

By default the DSP also has access to most on and off chip memory areas, with the exception of the ARM RAM, ROM, and AINTC interrupt controller.

Additionally, the DSP megamodule includes the capability to limit access to its internal memories through its SDMA port; without needing an external MPU unit.

#### 2.4.2.1 ARM Internal Memories

The DSP does not have access to the ARM internal memory.

#### 2.4.2.2 External Memories

The DSP has access to the following External memories:

- Asynchronous EMIF / SDRAM / NAND / NOR Flash (EMIFA)
- SDRAM (DDR2)

#### 2.4.2.3 DSP Internal Memories

The DSP has access to the following DSP memories:

- L2 RAM
- L1P RAM
- L1D RAM

#### 2.4.2.4 C674x CPU

The C674x core uses a two-level cache-based architecture. The Level 1 Program cache (L1P) is 32 KB direct mapped cache and the Level 1 Data cache (L1D) is 32 KB 2-way set associated cache. The Level 2 memory/cache (L2) consists of a 256 KB memory space that is shared between program and data space. L2 memory can be configured as mapped memory, cache, or a combination of both.

Table 2-2 shows a memory map of the C674x CPU cache registers for the device.

**Table 2-2. C674x Cache Registers**

| Byte Address | Register Name | Register Description |
|---|---|---|
| 0x0184 0000 | L2CFG | L2 Cache configuration register |
| 0x0184 0020 | L1PCFG | L1P Size Cache configuration register |
| 0x0184 0024 | L1PCC | L1P Freeze Mode Cache configuration register |
| 0x0184 0040 | L1DCFG | L1D Size Cache configuration register |
| 0x0184 0044 | L1DCC | L1D Freeze Mode Cache configuration register |
| 0x0184 0048 - 0x0184 0FFC | - | Reserved |
| 0x0184 1000 | EDMAWEIGHT | L2 EDMA access control register |
| 0x0184 1004 - 0x0184 1FFC | - | Reserved |
| 0x0184 2000 | L2ALLOC0 | L2 allocation register 0 |
| 0x0184 2004 | L2ALLOC1 | L2 allocation register 1 |
| 0x0184 2008 | L2ALLOC2 | L2 allocation register 2 |
| 0x0184 200C | L2ALLOC3 | L2 allocation register 3 |
| 0x0184 2010 - 0x0184 3FFF | - | Reserved |
| 0x0184 4000 | L2WBAR | L2 writeback base address register |
| 0x0184 4004 | L2WWC | L2 writeback word count register |
| 0x0184 4010 | L2WIBAR | L2 writeback invalidate base address register |
| 0x0184 4014 | L2WIWC | L2 writeback invalidate word count register |
| 0x0184 4018 | L2IBAR | L2 invalidate base address register |

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**Table 2-2. C674x Cache Registers (continued)**

| Byte Address | Register Name | Register Description |
|---|---|---|
| 0x0184 401C | L2IWC | L2 invalidate word count register |
| 0x0184 4020 | L1PIBAR | L1P invalidate base address register |
| 0x0184 4024 | L1PIWC | L1P invalidate word count register |
| 0x0184 4030 | L1DWIBAR | L1D writeback invalidate base address register |
| 0x0184 4034 | L1DWIWC | L1D writeback invalidate word count register |
| 0x0184 4038 | - | Reserved |
| 0x0184 4040 | L1DWBAR | L1D Block Writeback |
| 0x0184 4044 | L1DWWC | L1D Block Writeback |
| 0x0184 4048 | L1DIBAR | L1D invalidate base address register |
| 0x0184 404C | L1DIWC | L1D invalidate word count register |
| 0x0184 4050 - 0x0184 4FFF | - | Reserved |
| 0x0184 5000 | L2WB | L2 writeback all register |
| 0x0184 5004 | L2WBINV | L2 writeback invalidate all register |
| 0x0184 5008 | L2INV | L2 Global Invalidate without writeback |
| 0x0184 500C - 0x0184 5027 | - | Reserved |
| 0x0184 5028 | L1PINV | L1P Global Invalidate |
| 0x0184 502C - 0x0184 5039 | - | Reserved |
| 0x0184 5040 | L1DWB | L1D Global Writeback |
| 0x0184 5044 | L1DWBINV | L1D Global Writeback with Invalidate |
| 0x0184 5048 | L1DINV | L1D Global Invalidate without writeback |
| 0x0184 8000 – 0x0184 80FF | MAR0 - MAR63 | Reserved 0x0000 0000 – 0x3FFF FFFF |
| 0x0184 8100 – 0x0184 817F | MAR64 – MAR95 | Memory Attribute Registers for EMIFA SDRAM Data (CS0)<br>External memory addresses 0x4000 0000 – 0x5FFF FFFF |
| 0x0184 8180 – 0x0184 8187 | MAR96 - MAR97 | Memory Attribute Registers for EMIFA Async Data (CS2)<br>External memory addresses 0x6000 0000 – 0x61FF FFFF |
| 0x0184 8188 – 0x0184 818F | MAR98 – MAR99 | Memory Attribute Registers for EMIFA Async Data (CS3)<br>External memory addresses 0x6200 0000 – 0x63FF FFFF |
| 0x0184 8190 – 0x0184 8197 | MAR100 – MAR101 | Memory Attribute Registers for EMIFA Async Data (CS4)<br>External memory addresses 0x6400 0000 – 0x65FF FFFF |
| 0x0184 8198 – 0x0184 819F | MAR102 – MAR103 | Memory Attribute Registers for EMIFA Async Data (CS5)<br>External memory addresses 0x6600 0000 – 0x67FF FFFF |
| 0x0184 81A0 – 0x0184 81FF | MAR104 – MAR127 | Reserved 0x6800 0000 – 0x7FFF FFFF |
| 0x0184 8200 | MAR128 | Memory Attribute Register for Shared RAM<br>External memory addresses 0x8000 0000 – 0x8001 FFFF |
| | | Reserved 0x8002 0000 – 0x81FF FFFF |
| 0x0184 8204 – 0x0184 82FF | MAR129 – MAR191 | Reserved 0x8200 0000 – 0xBFFF FFFF |
| 0x0184 8300 – 0x0184 837F | MAR192 – MAR223 | Memory Attribute Registers for DDR2 Data (CS2)<br>External memory addresses 0xC000 0000 – 0xDFFF FFFF |
| 0x0184 8380 – 0x0184 83FF | MAR224 – MAR255 | Reserved 0xE000 0000 – 0xFFFF FFFF |

**Table 2-3. C674x L1/L2 Memory Protection Registers**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A000 | L2MPFAR | L2 memory protection fault address register |
| 0x0184 A004 | L2MPFSR | L2 memory protection fault status register |
| 0x0184 A008 | L2MPFCR | L2 memory protection fault command register |
| 0x0184 A00C - 0x0184 A0FF | - | Reserved |
| 0x0184 A100 | L2MPLK0 | L2 memory protection lock key bits [31:0] |
| 0x0184 A104 | L2MPLK1 | L2 memory protection lock key bits [63:32] |
| 0x0184 A108 | L2MPLK2 | L2 memory protection lock key bits [95:64] |


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**Table 2-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A10C | L2MPLK3 | L2 memory protection lock key bits [127:96] |
| 0x0184 A110 | L2MPLKCMD | L2 memory protection lock key command register |
| 0x0184 A114 | L2MPLKSTAT | L2 memory protection lock key status register |
| 0x0184 A118 - 0x0184 A1FF | - | Reserved |
| 0x0184 A200 | L2MPPA0 | L2 memory protection page attribute register 0 (controls memory address 0x0080 0000 - 0x0080 1FFF) |
| 0x0184 A204 | L2MPPA1 | L2 memory protection page attribute register 1 (controls memory address 0x0080 2000 - 0x0080 3FFF) |
| 0x0184 A208 | L2MPPA2 | L2 memory protection page attribute register 2 (controls memory address 0x0080 4000 - 0x0080 5FFF) |
| 0x0184 A20C | L2MPPA3 | L2 memory protection page attribute register 3 (controls memory address 0x0080 6000 - 0x0080 7FFF) |
| 0x0184 A210 | L2MPPA4 | L2 memory protection page attribute register 4 (controls memory address 0x0080 8000 - 0x0080 9FFF) |
| 0x0184 A214 | L2MPPA5 | L2 memory protection page attribute register 5 (controls memory address 0x0080 A000 - 0x0080 BFFF) |
| 0x0184 A218 | L2MPPA6 | L2 memory protection page attribute register 6 (controls memory address 0x0080 C000 - 0x0080 DFFF) |
| 0x0184 A21C | L2MPPA7 | L2 memory protection page attribute register 7 (controls memory address 0x0080 E000 - 0x0080 FFFF) |
| 0x0184 A220 | L2MPPA8 | L2 memory protection page attribute register 8 (controls memory address 0x0081 0000 - 0x0081 1FFF) |
| 0x0184 A224 | L2MPPA9 | L2 memory protection page attribute register 9 (controls memory address 0x0081 2000 - 0x0081 3FFF) |
| 0x0184 A228 | L2MPPA10 | L2 memory protection page attribute register 10 (controls memory address 0x0081 4000 - 0x0081 5FFF) |
| 0x0184 A22C | L2MPPA11 | L2 memory protection page attribute register 11 (controls memory address 0x0081 6000 - 0x0081 7FFF) |
| 0x0184 A230 | L2MPPA12 | L2 memory protection page attribute register 12 (controls memory address 0x0081 8000 - 0x0081 9FFF) |
| 0x0184 A234 | L2MPPA13 | L2 memory protection page attribute register 13 (controls memory address 0x0081 A000 - 0x0081 BFFF) |
| 0x0184 A238 | L2MPPA14 | L2 memory protection page attribute register 14 (controls memory address 0x0081 C000 - 0x0081 DFFF) |
| 0x0184 A23C | L2MPPA15 | L2 memory protection page attribute register 15 (controls memory address 0x0081 E000 - 0x0081 FFFF) |
| 0x0184 A240 | L2MPPA16 | L2 memory protection page attribute register 16 (controls memory address 0x0082 0000 - 0x0082 1FFF) |
| 0x0184 A244 | L2MPPA17 | L2 memory protection page attribute register 17 (controls memory address 0x0082 2000 - 0x0082 3FFF) |
| 0x0184 A248 | L2MPPA18 | L2 memory protection page attribute register 18 (controls memory address 0x0082 4000 - 0x0082 5FFF) |
| 0x0184 A24C | L2MPPA19 | L2 memory protection page attribute register 19 (controls memory address 0x0082 6000 - 0x0082 7FFF) |
| 0x0184 A250 | L2MPPA20 | L2 memory protection page attribute register 20 (controls memory address 0x0082 8000 - 0x0082 9FFF) |
| 0x0184 A254 | L2MPPA21 | L2 memory protection page attribute register 21 (controls memory address 0x0082 A000 - 0x0082 BFFF) |
| 0x0184 A258 | L2MPPA22 | L2 memory protection page attribute register 22 (controls memory address 0x0082 C000 - 0x0082 DFFF) |
| 0x0184 A25C | L2MPPA23 | L2 memory protection page attribute register 23 (controls memory address 0x0082 E000 - 0x0082 FFFF) |
| 0x0184 A260 | L2MPPA24 | L2 memory protection page attribute register 24 (controls memory address 0x0083 0000 - 0x0083 1FFF) |

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**Table 2-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A264 | L2MPPA25 | L2 memory protection page attribute register 25 (controls memory address 0x0083 2000 - 0x0083 3FFF) |
| 0x0184 A268 | L2MPPA26 | L2 memory protection page attribute register 26 (controls memory address 0x0083 4000 - 0x0083 5FFF) |
| 0x0184 A26C | L2MPPA27 | L2 memory protection page attribute register 27 (controls memory address 0x0083 6000 - 0x0083 7FFF) |
| 0x0184 A270 | L2MPPA28 | L2 memory protection page attribute register 28 (controls memory address 0x0083 8000 - 0x0083 9FFF) |
| 0x0184 A274 | L2MPPA29 | L2 memory protection page attribute register 29 (controls memory address 0x0083 A000 - 0x0083 BFFF) |
| 0x0184 A278 | L2MPPA30 | L2 memory protection page attribute register 30 (controls memory address 0x0083 C000 - 0x0083 DFFF) |
| 0x0184 A27C | L2MPPA31 | L2 memory protection page attribute register 31 (controls memory address 0x0083 E000 - 0x0083 FFFF) |
| 0x0184 A280 | L2MPPA32 | L2 memory protection page attribute register 32 (controls memory address 0x0070 0000 - 0x0070 7FFF) |
| 0x0184 A284 | L2MPPA33 | L2 memory protection page attribute register 33 (controls memory address 0x0070 8000 - 0x0070 FFFF) |
| 0x0184 A288 | L2MPPA34 | L2 memory protection page attribute register 34 (controls memory address 0x0071 0000 - 0x0071 7FFF) |
| 0x0184 A28C | L2MPPA35 | L2 memory protection page attribute register 35 (controls memory address 0x0071 8000 - 0x0071 FFFF) |
| 0x0184 A290 | L2MPPA36 | L2 memory protection page attribute register 36 (controls memory address 0x0072 0000 - 0x0072 7FFF) |
| 0x0184 A294 | L2MPPA37 | L2 memory protection page attribute register 37 (controls memory address 0x0072 8000 - 0x0072 FFFF) |
| 0x0184 A298 | L2MPPA38 | L2 memory protection page attribute register 38 (controls memory address 0x0073 0000 - 0x0073 7FFF) |
| 0x0184 A29C | L2MPPA39 | L2 memory protection page attribute register 39 (controls memory address 0x0073 8000 - 0x0073 FFFF) |
| 0x0184 A2A0 | L2MPPA40 | L2 memory protection page attribute register 40 (controls memory address 0x0074 0000 - 0x0074 7FFF) |
| 0x0184 A2A4 | L2MPPA41 | L2 memory protection page attribute register 41 (controls memory address 0x0074 8000 - 0x0074 FFFF) |
| 0x0184 A2A8 | L2MPPA42 | L2 memory protection page attribute register 42 (controls memory address 0x0075 0000 - 0x0075 7FFF) |
| 0x0184 A2AC | L2MPPA43 | L2 memory protection page attribute register 43 (controls memory address 0x0075 8000 - 0x0075 FFFF) |
| 0x0184 A2B0 | L2MPPA44 | L2 memory protection page attribute register 44 (controls memory address 0x0076 0000 - 0x0076 7FFF) |
| 0x0184 A2B4 | L2MPPA45 | L2 memory protection page attribute register 45 (controls memory address 0x0076 8000 - 0x0076 FFFF) |
| 0x0184 A2B8 | L2MPPA46 | L2 memory protection page attribute register 46 (controls memory address 0x0077 0000 - 0x0077 7FFF) |
| 0x0184 A2BC | L2MPPA47 | L2 memory protection page attribute register 47 (controls memory address 0x0077 8000 - 0x0077 FFFF) |
| 0x0184 A2C0 | L2MPPA48 | L2 memory protection page attribute register 48 (controls memory address 0x0078 0000 - 0x0078 7FFF) |
| 0x0184 A2C4 | L2MPPA49 | L2 memory protection page attribute register 49 (controls memory address 0x0078 8000 - 0x0078 FFFF) |
| 0x0184 A2C8 | L2MPPA50 | L2 memory protection page attribute register 50 (controls memory address 0x0079 0000 - 0x0079 7FFF) |
| 0x0184 A2CC | L2MPPA51 | L2 memory protection page attribute register 51 (controls memory address 0x0079 8000 - 0x0079 FFFF) |
| 0x0184 A2D0 | L2MPPA52 | L2 memory protection page attribute register 52 (controls memory address 0x007A 0000 - 0x007A 7FFF) |


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**Table 2-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A2D4 | L2MPPA53 | L2 memory protection page attribute register 53 (controls memory address 0x007A 8000 - 0x007A FFFF) |
| 0x0184 A2D8 | L2MPPA54 | L2 memory protection page attribute register 54 (controls memory address 0x007B 0000 - 0x007B 7FFF) |
| 0x0184 A2DC | L2MPPA55 | L2 memory protection page attribute register 55 (controls memory address 0x007B 8000 - 0x007B FFFF) |
| 0x0184 A2E0 | L2MPPA56 | L2 memory protection page attribute register 56 (controls memory address 0x007C 0000 - 0x007C 7FFF) |
| 0x0184 A2E4 | L2MPPA57 | L2 memory protection page attribute register 57 (controls memory address 0x007C 8000 - 0x007C FFFF) |
| 0x0184 A2E8 | L2MPPA58 | L2 memory protection page attribute register 58 (controls memory address 0x007D 0000 - 0x007D 7FFF) |
| 0x0184 A2EC | L2MPPA59 | L2 memory protection page attribute register 59 (controls memory address 0x007D 8000 - 0x007D FFFF) |
| 0x0184 A2F0 | L2MPPA60 | L2 memory protection page attribute register 60 (controls memory address 0x007E 0000 - 0x007E 7FFF) |
| 0x0184 A2F4 | L2MPPA61 | L2 memory protection page attribute register 61 (controls memory address 0x007E 8000 - 0x007E FFFF) |
| 0x0184 A2F8 | L2MPPA62 | L2 memory protection page attribute register 62 (controls memory address 0x007F 0000 - 0x007F 7FFF) |
| 0x0184 A2FC | L2MPPA63 | L2 memory protection page attribute register 63 (controls memory address 0x007F 8000 - 0x007F FFFF) |
| 0x0184 A300 - 0x0184 A3FF | - | Reserved |
| 0x0184 A400 | L1PMPFAR | L1P memory protection fault address register |
| 0x0184 A404 | L1PMPFSR | L1P memory protection fault status register |
| 0x0184 A408 | L1PMPFCR | L1P memory protection fault command register |
| 0x0184 A40C - 0x0184 A4FF | - | Reserved |
| 0x0184 A500 | L1PMPLK0 | L1P memory protection lock key bits [31:0] |
| 0x0184 A504 | L1PMPLK1 | L1P memory protection lock key bits [63:32] |
| 0x0184 A508 | L1PMPLK2 | L1P memory protection lock key bits [95:64] |
| 0x0184 A50C | L1PMPLK3 | L1P memory protection lock key bits [127:96] |
| 0x0184 A510 | L1PMPLKCMD | L1P memory protection lock key command register |
| 0x0184 A514 | L1PMPLKSTAT | L1P memory protection lock key status register |
| 0x0184 A518 - 0x0184 A5FF | - | Reserved |
| 0x0184 A600 - 0x0184 A63F | - | Reserved (1) |
| 0x0184 A640 | L1PMPPA16 | L1P memory protection page attribute register 16 (controls memory address 0x00E0 0000 - 0x00E0 07FF) |
| 0x0184 A644 | L1PMPPA17 | L1P memory protection page attribute register 17 (controls memory address 0x00E0 0800 - 0x00E0 0FFF) |
| 0x0184 A648 | L1PMPPA18 | L1P memory protection page attribute register 18 (controls memory address 0x00E0 1000 - 0x00E0 17FF) |
| 0x0184 A64C | L1PMPPA19 | L1P memory protection page attribute register 19 (controls memory address 0x00E0 1800 - 0x00E0 1FFF) |
| 0x0184 A650 | L1PMPPA20 | L1P memory protection page attribute register 20 (controls memory address 0x00E0 2000 - 0x00E0 27FF) |
| 0x0184 A654 | L1PMPPA21 | L1P memory protection page attribute register 21 (controls memory address 0x00E0 2800 - 0x00E0 2FFF) |
| 0x0184 A658 | L1PMPPA22 | L1P memory protection page attribute register 22 (controls memory address 0x00E0 3000 - 0x00E0 37FF) |
| 0x0184 A65C | L1PMPPA23 | L1P memory protection page attribute register 23 (controls memory address 0x00E0 3800 - 0x00E0 3FFF) |

(1) These addresses correspond to the L1P memory protection page attribute registers 0-15 (L1PMPPA0-L1PMPPA15) of the C674x megamodule. These registers are not supported for this device.

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**Table 2-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 A660 | L1PMPPA24 | L1P memory protection page attribute register 24 (controls memory address 0x00E0 4000 - 0x00E0 47FF) |
| 0x0184 A664 | L1PMPPA25 | L1P memory protection page attribute register 25 (controls memory address 0x00E0 4800 - 0x00E0 4FFF) |
| 0x0184 A668 | L1PMPPA26 | L1P memory protection page attribute register 26 (controls memory address 0x00E0 5000 - 0x00E0 57FF) |
| 0x0184 A66C | L1PMPPA27 | L1P memory protection page attribute register 27 (controls memory address 0x00E0 5800 - 0x00E0 5FFF) |
| 0x0184 A670 | L1PMPPA28 | L1P memory protection page attribute register 28 (controls memory address 0x00E0 6000 - 0x00E0 67FF) |
| 0x0184 A674 | L1PMPPA29 | L1P memory protection page attribute register 29 (controls memory address 0x00E0 6800 - 0x00E0 6FFF) |
| 0x0184 A678 | L1PMPPA30 | L1P memory protection page attribute register 30 (controls memory address 0x00E0 7000 - 0x00E0 77FF) |
| 0x0184 A67C | L1PMPPA31 | L1P memory protection page attribute register 31 (controls memory address 0x00E0 7800 - 0x00E0 7FFF) |
| 0x0184 A67F – 0x0184 ABFF | - | Reserved |
| 0x0184 AC00 | L1DMPFAR | L1D memory protection fault address register |
| 0x0184 AC04 | L1DMPFSR | L1D memory protection fault status register |
| 0x0184 AC08 | L1DMPFCR | L1D memory protection fault command register |
| 0x0184 AC0C - 0x0184 ACFF | - | Reserved |
| 0x0184 AD00 | L1DMPLK0 | L1D memory protection lock key bits [31:0] |
| 0x0184 AD04 | L1DMPLK1 | L1D memory protection lock key bits [63:32] |
| 0x0184 AD08 | L1DMPLK2 | L1D memory protection lock key bits [95:64] |
| 0x0184 AD0C | L1DMPLK3 | L1D memory protection lock key bits [127:96] |
| 0x0184 AD10 | L1DMPLKCMD | L1D memory protection lock key command register |
| 0x0184 AD14 | L1DMPLKSTAT | L1D memory protection lock key status register |
| 0x0184 AD18 - 0x0184 ADFF | - | Reserved |
| 0x0184 AE00 - 0x0184 AE3F | - | Reserved (2) |
| 0x0184 AE40 | L1DMPPA16 | L1D memory protection page attribute register 16 (controls memory address 0x00F0 0000 - 0x00F0 07FF) |
| 0x0184 AE44 | L1DMPPA17 | L1D memory protection page attribute register 17 (controls memory address 0x00F0 0800 - 0x00F0 0FFF) |
| 0x0184 AE48 | L1DMPPA18 | L1D memory protection page attribute register 18 (controls memory address 0x00F0 1000 - 0x00F0 17FF) |
| 0x0184 AE4C | L1DMPPA19 | L1D memory protection page attribute register 19 (controls memory address 0x00F0 1800 - 0x00F0 1FFF) |
| 0x0184 AE50 | L1DMPPA20 | L1D memory protection page attribute register 20 (controls memory address 0x00F0 2000 - 0x00F0 27FF) |
| 0x0184 AE54 | L1DMPPA21 | L1D memory protection page attribute register 21 (controls memory address 0x00F0 2800 - 0x00F0 2FFF) |
| 0x0184 AE58 | L1DMPPA22 | L1D memory protection page attribute register 22 (controls memory address 0x00F0 3000 - 0x00F0 37FF) |
| 0x0184 AE5C | L1DMPPA23 | L1D memory protection page attribute register 23 (controls memory address 0x00F0 3800 - 0x00F0 3FFF) |
| 0x0184 AE60 | L1DMPPA24 | L1D memory protection page attribute register 24 (controls memory address 0x00F0 4000 - 0x00F0 47FF) |
| 0x0184 AE64 | L1DMPPA25 | L1D memory protection page attribute register 25 (controls memory address 0x00F0 4800 - 0x00F0 4FFF) |
| 0x0184 AE68 | L1DMPPA26 | L1D memory protection page attribute register 26 (controls memory address 0x00F0 5000 - 0x00F0 57FF) |

(2) These addresses correspond to the L1D memory protection page attribute registers 0-15 (L1DMPPA0-L1DMPPA15) of the C674x megamaodule. These registers are not supported for this device.


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**Table 2-3. C674x L1/L2 Memory Protection Registers (continued)**

| HEX ADDRESS RANGE | REGISTER ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0184 AE6C | L1DMPPA27 | L1D memory protection page attribute register 27 (controls memory address 0x00F0 5800 - 0x00F0 5FFF) |
| 0x0184 AE70 | L1DMPPA28 | L1D memory protection page attribute register 28 (controls memory address 0x00F0 6000 - 0x00F0 67FF) |
| 0x0184 AE74 | L1DMPPA29 | L1D memory protection page attribute register 29 (controls memory address 0x00F0 6800 - 0x00F0 6FFF) |
| 0x0184 AE78 | L1DMPPA30 | L1D memory protection page attribute register 30 (controls memory address 0x00F0 7000 - 0x00F0 77FF) |
| 0x0184 AE7C | L1DMPPA31 | L1D memory protection page attribute register 31 (controls memory address 0x00F0 7800 - 0x00F0 7FFF) |
| 0x0184 AE80 – 0x0185 FFFF | - | Reserved |

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## 2.5 Memory Map Summary

**Table 2-4. Top Level Memory Map**

| Start Address | End Address | Size | ARM Mem Map | DSP Mem Map | EDMA Mem Map | PRUSS Mem Map | Master Peripheral Mem Map | LCDC Mem Map |
|---|---|---|---|---|---|---|---|---|
| 0x0000 0000 | 0x0000 0FFF | 4K | | | | PRUSS Local Address Space | | |
| 0x0000 1000 | 0x006F FFFF | | | | | | | |
| 0x0070 0000 | 0x007F FFFF | 1024K | | DSP L2 ROM (1) | | | | |
| 0x0080 0000 | 0x0083 FFFF | 256K | | DSP L2 RAM | | | | |
| 0x0084 0000 | 0x00DF FFFF | | | | | | | |
| 0x00E0 0000 | 0x00E0 7FFF | 32K | | DSP L1P RAM | | | | |
| 0x00E0 8000 | 0x00EF FFFF | | | | | | | |
| 0x00F0 0000 | 0x00F0 7FFF | 32K | | DSP L1D RAM | | | | |
| 0x00F0 8000 | 0x017F FFFF | | | | | | | |
| 0x0180 0000 | 0x0180 FFFF | 64K | | DSP Interrupt Controller | | | | |
| 0x0181 0000 | 0x0181 0FFF | 4K | | DSP Powerdown Controller | | | | |
| 0x0181 1000 | 0x0181 1FFF | 4K | | DSP Security ID | | | | |
| 0x0181 2000 | 0x0181 2FFF | 4K | | DSP Revision ID | | | | |
| 0x0181 3000 | 0x0181 FFFF | 52K | | - | | | | |
| 0x0182 0000 | 0x0182 FFFF | 64K | | DSP EMC | | | | |
| 0x0183 0000 | 0x0183 FFFF | 64K | | DSP Internal Reserved | | | | |
| 0x0184 0000 | 0x0184 FFFF | 64K | | DSP Memory System | | | | |
| 0x0185 0000 | 0x01BB FFFF | | | | | | | |
| 0x01BC 0000 | 0x01BC 0FFF | 4K | ARM ETB memory | | | | | |
| 0x01BC 1000 | 0x01BC 17FF | 2K | ARM ETB reg | | | | | |
| 0x01BC 1800 | 0x01BC 18FF | 256 | ARM Ice Crusher | | | | | |
| 0x01BC 1900 | 0x01BF FFFF | | | | | | | |
| 0x01C0 0000 | 0x01C0 7FFF | 32K | EDMA3 CC | | | | | |
| 0x01C0 8000 | 0x01C0 83FF | 1K | EDMA3 TC0 | | | | | |
| 0x01C0 8400 | 0x01C0 87FF | 1K | EDMA3 TC1 | | | | | |
| 0x01C0 8800 | 0x01C0 FFFF | | | | | | | |
| 0x01C1 0000 | 0x01C1 0FFF | 4K | PSC 0 | | | | | |
| 0x01C1 1000 | 0x01C1 1FFF | 4K | PLL Controller 0 | | | | | |
| 0x01C1 2000 | 0x01C1 3FFF | | | | | | | |
| 0x01C1 4000 | 0x01C1 4FFF | 4K | SYSCFG0 | | | | | |
| 0x01C1 5000 | 0x01C1 FFFF | | | | | | | |
| 0x01C2 0000 | 0x01C2 0FFF | 4K | Timer0 | | | | | |
| 0x01C2 1000 | 0x01C2 1FFF | 4K | Timer1 | | | | | |
| 0x01C2 2000 | 0x01C2 2FFF | 4K | I2C 0 | | | | | |
| 0x01C2 3000 | 0x01C2 3FFF | 4K | RTC | | | | | |
| 0x01C2 4000 | 0x01C3 FFFF | | | | | | | |
| 0x01C4 0000 | 0x01C4 0FFF | 4K | MMC/SD 0 | | | | | |
| 0x01C4 1000 | 0x01C4 1FFF | 4K | SPI 0 | | | | | |
| 0x01C4 2000 | 0x01C4 2FFF | 4K | UART 0 | | | | | |

(1) The DSP L2 ROM is used for boot purposes and cannot be programmed with application code


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**Table 2-4. Top Level Memory Map (continued)**

| Start Address | End Address | Size | ARM Mem Map | DSP Mem Map | EDMA Mem Map | PRUSS Mem Map | Master Peripheral Mem Map | LCDC Mem Map |
|---|---|---|---|---|---|---|---|---|
| 0x01C4 3000 | 0x01CF FFFF | | | | | | | |
| 0x01D0 0000 | 0x01D0 0FFF | 4K | McASP 0 Control | | | | | |
| 0x01D0 1000 | 0x01D0 1FFF | 4K | McASP 0 AFIFO Ctrl | | | | | |
| 0x01D0 2000 | 0x01D0 2FFF | 4K | McASP 0 Data | | | | | |
| 0x01D0 3000 | 0x01D0 BFFF | | | | | | | |
| 0x01D0 C000 | 0x01D0 CFFF | 4K | UART 1 | | | | | |
| 0x01D0 D000 | 0x01D0 DFFF | 4K | UART 2 | | | | | |
| 0x01D0 E000 | 0x01D0 FFFF | | | | | | | |
| 0x01D1 0000 | 0x01D1 07FF | 2K | McBSP0 | | | | | |
| 0x01D1 0800 | 0x01D1 0FFF | 2K | McBSP0 FIFO Ctrl | | | | | |
| 0x01D1 1000 | 0x01D1 17FF | 2K | McBSP1 | | | | | |
| 0x01D1 1800 | 0x01D1 1FFF | 2K | McBSP1 FIFO Ctrl | | | | | |
| 0x01D1 2000 | 0x01DF FFFF | | | | | | | |
| 0x01E0 0000 | 0x01E0 FFFF | 64K | USB0 | | | | | |
| 0x01E1 0000 | 0x01E1 0FFF | 4K | UHPI | | | | | |
| 0x01E1 1000 | 0x01E1 2FFF | | | | | | | |
| 0x01E1 3000 | 0x01E1 3FFF | 4K | LCD Controller | | | | | |
| 0x01E1 4000 | 0x01E1 4FFF | 4K | Memory Protection Unit 1 (MPU 1) | | | | | |
| 0x01E1 5000 | 0x01E1 5FFF | 4K | Memory Protection Unit 2 (MPU 2) | | | | | |
| 0x01E1 6000 | 0x01E1 6FFF | 4K | UPP | | | | | |
| 0x01E1 7000 | 0x01E1 7FFF | 4K | VPIF | | | | | |
| 0x01E1 8000 | 0x01E1 9FFF | 8K | SATA | | | | | |
| 0x01E1 A000 | 0x01E1 AFFF | 4K | PLL Controller 1 | | | | | |
| 0x01E1 B000 | 0x01E1 BFFF | 4K | MMCSD1 | | | | | |
| 0x01E1 C000 | 0x01E1 FFFF | | | | | | | |
| 0x01E2 0000 | 0x01E2 1FFF | 8K | EMAC Control Module RAM | | | | | |
| 0x01E2 2000 | 0x01E2 2FFF | 4K | EMAC Control Module Registers | | | | | |
| 0x01E2 3000 | 0x01E2 3FFF | 4K | EMAC Control Registers | | | | | |
| 0x01E2 4000 | 0x01E2 4FFF | 4K | EMAC MDIO port | | | | | |
| 0x01E2 5000 | 0x01E2 5FFF | 4K | USB1 | | | | | |
| 0x01E2 6000 | 0x01E2 6FFF | 4K | GPIO | | | | | |
| 0x01E2 7000 | 0x01E2 7FFF | 4K | PSC 1 | | | | | |
| 0x01E2 8000 | 0x01E2 8FFF | 4K | I2C 1 | | | | | |
| 0x01E2 9000 | 0x01E2 BFFF | | | | | | | |
| 0x01E2 C000 | 0x01E2 CFFF | 4K | SYSCFG1 | | | | | |
| 0x01E2 D000 | 0x01E2 FFFF | | | | | | | |
| 0x01E3 0000 | 0x01E3 7FFF | 32K | EDMA3 CC1 | | | | | |
| 0x01E3 8000 | 0x01E3 83FF | 1K | EDMA3 TC2 | | | | | |
| 0x01E3 8400 | 0x01EF FFFF | | | | | | | |
| 0x01F0 0000 | 0x01F0 0FFF | 4K | eHRPWM 0 | | | | | |
| 0x01F0 1000 | 0x01F0 1FFF | 4K | HRPWM 0 | | | | | |
| 0x01F0 2000 | 0x01F0 2FFF | 4K | eHRPWM 1 | | | | | |
| 0x01F0 3000 | 0x01F0 3FFF | 4K | HRPWM 1 | | | | | |
| 0x01F0 4000 | 0x01F0 5FFF | | | | | | | |
| 0x01F0 6000 | 0x01F0 6FFF | 4K | ECAP 0 | | | | | |
| 0x01F0 7000 | 0x01F0 7FFF | 4K | ECAP 1 | | | | | |

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**Table 2-4. Top Level Memory Map (continued)**

| Start Address | End Address | Size | ARM Mem Map | DSP Mem Map | EDMA Mem Map | PRUSS Mem Map | Master Peripheral Mem Map | LCDC Mem Map |
|---|---|---|---|---|---|---|---|---|
| 0x01F0 8000 | 0x01F0 8FFF | 4K | ECAP 2 | | | | | |
| 0x01F0 9000 | 0x01F0 BFFF | | | | | | | |
| 0x01F0 C000 | 0x01F0 CFFF | 4K | Timer2 | | | | | |
| 0x01F0 D000 | 0x01F0 DFFF | 4K | Timer3 | | | | | |
| 0x01F0 E000 | 0x01F0 EFFF | 4K | SPI1 | | | | | |
| 0x01F0 F000 | 0x01F0 FFFF | | | | | | | |
| 0x01F1 0000 | 0x01F1 0FFF | 4K | McBSP0 FIFO Data | | | | | |
| 0x01F1 1000 | 0x01F1 1FFF | 4K | McBSP1 FIFO Data | | | | | |
| 0x01F1 2000 | 0x116F FFFF | | | | | | | |
| 0x1170 0000 | 0x117F FFFF | 1024K | DSP L2 ROM(2) | | | | | |
| 0x1180 0000 | 0x1183 FFFF | 256K | DSP L2 RAM | | | | | |
| 0x1184 0000 | 0x11DF FFFF | | | | | | | |
| 0x11E0 0000 | 0x11E0 7FFF | 32K | DSP L1P RAM | | | | | |
| 0x11E0 8000 | 0x11EF FFFF | | | | | | | |
| 0x11F0 0000 | 0x11F0 7FFF | 32K | DSP L1D RAM | | | | | |
| 0x11F0 8000 | 0x3FFF FFFF | | | | | | | |
| 0x4000 0000 | 0x5FFF FFFF | 512M | EMIFA SDRAM data (CS0) | | | | | |
| 0x6000 0000 | 0x61FF FFFF | 32M | EMIFA async data (CS2) | | | | | |
| 0x6200 0000 | 0x63FF FFFF | 32M | EMIFA async data (CS3) | | | | | |
| 0x6400 0000 | 0x65FF FFFF | 32M | EMIFA async data (CS4) | | | | | |
| 0x6600 0000 | 0x67FF FFFF | 32M | EMIFA async data (CS5) | | | | | |
| 0x6800 0000 | 0x6800 7FFF | 32K | EMIFA Control Regs | | | | | |
| 0x6800 8000 | 0x7FFF FFFF | | | | | | | |
| 0x8000 0000 | 0x8001 FFFF | 128K | Shared RAM | | | | | |
| 0x8002 0000 | 0xAFFF FFFF | | | | | | | |
| 0xB000 0000 | 0xB000 7FFF | 32K | DDR2 Control Regs | | | | | |
| 0xB000 8000 | 0xBFFF FFFF | | | | | | | |
| 0xC000 0000 | 0xDFFF FFFF | 512M | DDR2 Data | | | | | |
| 0xE000 0000 | 0xFFFC FFFF | | | | | | | |
| 0xFFFD 0000 | 0xFFFD FFFF | 64K | ARM local ROM | | | | | |
| 0xFFFE 0000 | 0xFFFE DFFF | | | | | | | |
| 0xFFFE E000 | 0xFFFE FFFF | 8K | ARM Interrupt Controller | | | | | |
| 0xFFFF 0000 | 0xFFFF 1FFF | 8K | ARM local RAM | | | ARM Local RAM (PRU0 only) | | |
| 0xFFFF 2000 | 0xFFFF FFFF | | | | | | | |

(2) The DSP L2 ROM is used for boot purposes and cannot be programmed with application code


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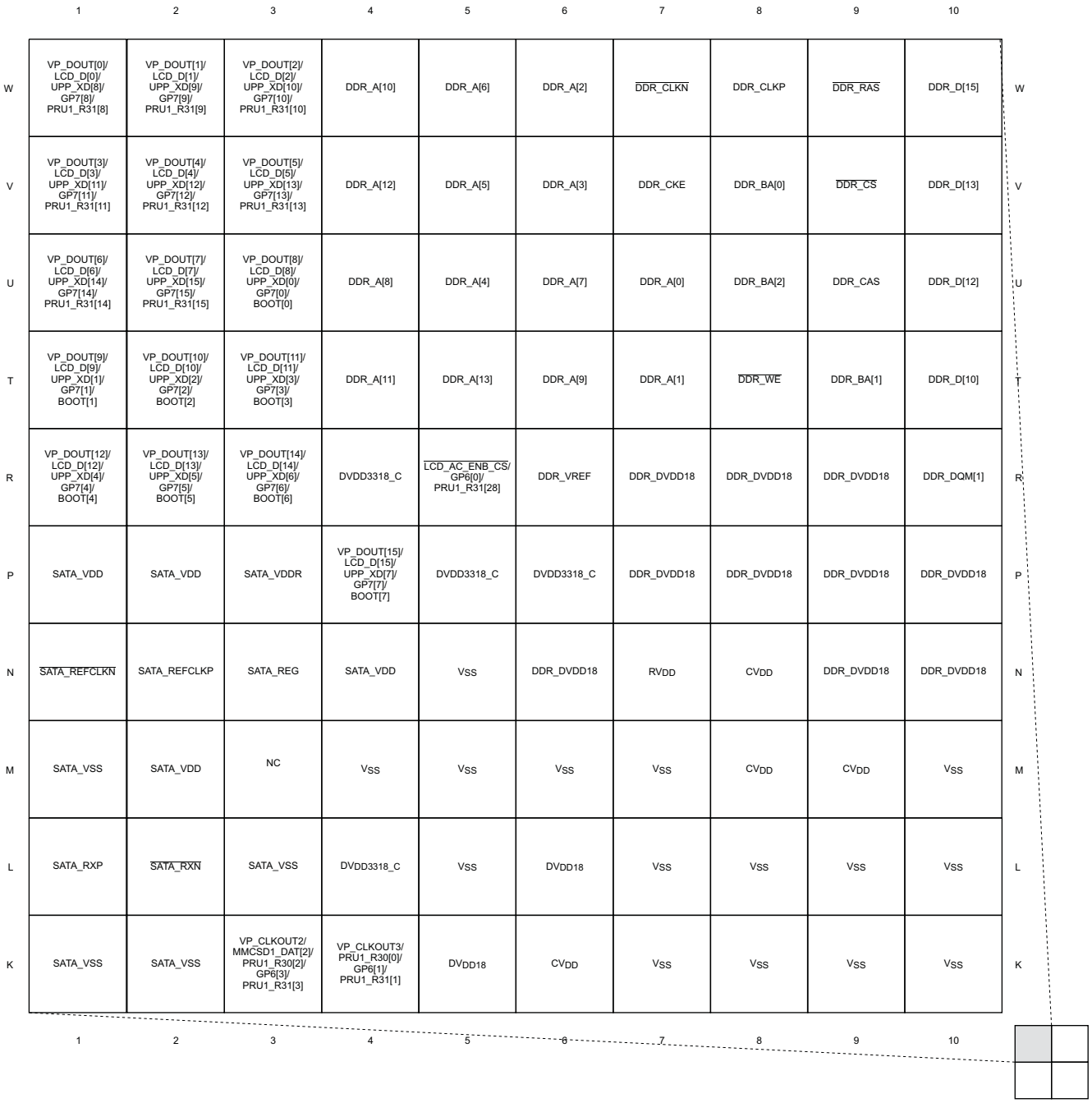
## 2.6 Pin Assignments

Extensive use of pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using a combination of hardware configuration at device reset and software programmable register settings.

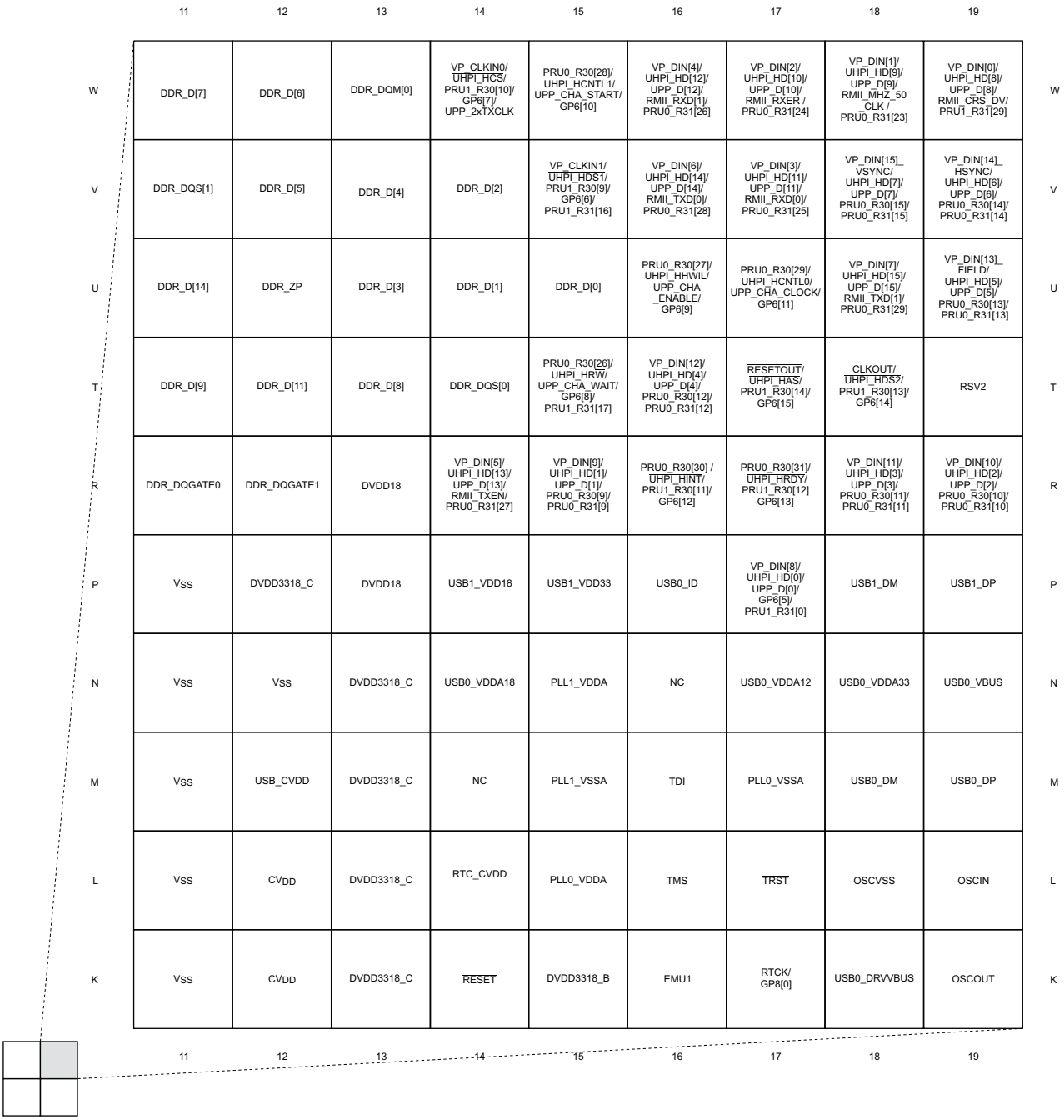
### *2.6.1 Pin Map (Bottom View)*

The following graphics show the bottom view of the ZCE and ZWT packages pin assignments in four quadrants (A, B, C, and D). The pin assignments for both packages are identical.



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| W | VP_DOUT[0]/ LCD_D[0]/ UPP_XD[8]/ GP7[8]/ PRU1_R31[8] | VP_DOUT[1]/ LCD_D[1]/ UPP_XD[9]/ GP7[9]/ PRU1_R31[9] | VP_DOUT[2]/ LCD_D[2]/ UPP_XD[10]/ GP7[10]/ PRU1_R31[10] | DDR_A[10] | DDR_A[6] | DDR_A[2] | DDR_CLKN | DDR_CLKP | DDR_RAS | DDR_D[15] | W |
| V | VP_DOUT[3]/ LCD_D[3]/ UPP_XD[11]/ GP7[11]/ PRU1_R31[11] | VP_DOUT[4]/ LCD_D[4]/ UPP_XD[12]/ GP7[12]/ PRU1_R31[12] | VP_DOUT[5]/ LCD_D[5]/ UPP_XD[13]/ GP7[13]/ PRU1_R31[13] | DDR_A[12] | DDR_A[5] | DDR_A[3] | DDR_CKE | DDR_BA[0] | DDR_CS | DDR_D[13] | V |
| U | VP_DOUT[6]/ LCD_D[6]/ UPP_XD[14]/ GP7[14]/ PRU1_R31[14] | VP_DOUT[7]/ LCD_D[7]/ UPP_XD[15]/ GP7[15]/ PRU1_R31[15] | VP_DOUT[8]/ LCD_D[8]/ UPP_XD[0]/ GP7[0]/ BOOT[0] | DDR_A[8] | DDR_A[4] | DDR_A[7] | DDR_A[0] | DDR_BA[2] | DDR_CAS | DDR_D[12] | U |
| T | VP_DOUT[9]/ LCD_D[9]/ UPP_XD[1]/ GP7[1]/ BOOT[1] | VP_DOUT[10]/ LCD_D[10]/ UPP_XD[2]/ GP7[2]/ BOOT[2] | VP_DOUT[11]/ LCD_D[11]/ UPP_XD[3]/ GP7[3]/ BOOT[3] | DDR_A[11] | DDR_A[13] | DDR_A[9] | DDR_A[1] | DDR_WE | DDR_BA[1] | DDR_D[10] | T |
| R | VP_DOUT[12]/ LCD_D[12]/ UPP_XD[4]/ GP7[4]/ BOOT[4] | VP_DOUT[13]/ LCD_D[13]/ UPP_XD[5]/ GP7[5]/ BOOT[5] | VP_DOUT[14]/ LCD_D[14]/ UPP_XD[6]/ GP7[6]/ BOOT[6] | DVDD3318_C | LCD_AC_ENB_CS/ GP6[0]/ PRU1_R31[28] | DDR_VREF | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | DDR_DQM[1] | R |
| P | SATA_VDD | SATA_VDD | SATA_VDDR | VP_DOUT[15]/ LCD_D[15]/ UPP_XD[7]/ GP7[7]/ BOOT[7] | DVDD3318_C | DVDD3318_C | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | DDR_DVDD18 | P |
| N | SATA_REFCLKN | SATA_REFCLKP | SATA_REG | SATA_VDD | $V_{SS}$ | DDR_DVDD18 | $RV_{DD}$ | $CV_{DD}$ | DDR_DVDD18 | DDR_DVDD18 | N |
| M | SATA_VSS | SATA_VDD | NC | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $CV_{DD}$ | $CV_{DD}$ | $V_{SS}$ | M |
| L | SATA_RXP | SATA_RXN | SATA_VSS | $DV_{DD3318_C}$ | $V_{SS}$ | $DV_{DD18}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | L |
| K | SATA_VSS | SATA_VSS | VP_CLKOUT2/ MMCSD1_DAT[2]/ PRU1_R30[2]/ GP6[3]/ PRU1_R31[3] | VP_CLKOUT3/ PRU1_R30[0]/ GP6[1]/ PRU1_R31[1] | $DV_{DD18}$ | $CV_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | K |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

**Figure 2-3. Pin Map (Quad A)**



| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |
|---|---|---|---|---|---|---|---|---|---|---|
| W | DDR_D[7] | DDR_D[6] | DDR_DQM[0] | VP_CLKIN0/ UHPI_HCS/ PRU1_R30[10]/ GP6[7]/ UPP_2xTXCLK | PRU0_R30[28]/ UHPI_HCNTL1/ UPP_CHA_START/ GP6[10] | VP_DIN[4]/ UHPI_HD[12]/ UPP_D[12]/ RMII_RXD[1]/ PRU0_R31[26] | VP_DIN[2]/ UHPI_HD[10]/ UPP_D[10]/ RMII_RXER / PRU0_R31[24] | VP_DIN[1]/ UHPI_HD[9]/ UPP_D[9]/ RMII_MHZ_50 _CLK / PRU0_R31[23] | VP_DIN[0]/ UHPI_HD[8]/ UPP_D[8]/ RMII_CRS_DV/ PRU1_R31[29] | W |
| V | DDR_DQS[1] | DDR_D[5] | DDR_D[4] | DDR_D[2] | VP_CLKIN1/ UHPI_HDS1/ PRU1_R30[9]/ GP6[6]/ PRU1_R31[16] | VP_DIN[6]/ UHPI_HD[14]/ UPP_D[14]/ RMII_TXD[0]/ PRU0_R31[28] | VP_DIN[3]/ UHPI_HD[11]/ UPP_D[11]/ RMII_RXD[0]/ PRU0_R31[25] | VP_DIN[15]_ VSYNC/ UHPI_HD[7]/ UPP_D[7]/ PRU0_R30[15]/ PRU0_R31[15] | VP_DIN[14]_ HSYNC/ UHPI_HD[6]/ UPP_D[6]/ PRU0_R30[14]/ PRU0_R31[14] | V |
| U | DDR_D[14] | DDR_ZP | DDR_D[3] | DDR_D[1] | DDR_D[0] | PRU0_R30[27]/ UHPI_HHWIL/ UPP_CHA _ENABLE/ GP6[9] | PRU0_R30[29]/ UHPI_HCNTL0/ UPP_CHA_CLOCK/ GP6[11] | VP_DIN[7]/ UHPI_HD[15]/ UPP_D[15]/ RMII_TXD[1]/ PRU0_R31[29] | VP_DIN[13]_ FIELD/ UHPI_HD[5]/ UPP_D[5]/ PRU0_R30[13]/ PRU0_R31[13] | U |
| T | DDR_D[9] | DDR_D[11] | DDR_D[8] | DDR_DQS[0] | PRU0_R30[26]/ UHPI_HRW/ UPP_CHA_WAIT/ GP6[8]/ PRU1_R31[17] | VP_DIN[12]/ UHPI_HD[4]/ UPP_D[4]/ PRU0_R30[12]/ PRU0_R31[12] | RESETOUT/ UHPI_HAS/ PRU1_R30[14]/ GP6[15] | CLKOUT/ UHPI_HDS2/ PRU1_R30[13]/ GP6[14] | RSV2 | T |
| R | DDR_DQGATE0 | DDR_DQGATE1 | DVDD18 | VP_DIN[5]/ UHPI_HD[13]/ UPP_D[13]/ RMII_TXEN/ PRU0_R31[27] | VP_DIN[9]/ UHPI_HD[1]/ UPP_D[1]/ PRU0_R30[9]/ PRU0_R31[9] | PRU0_R30[30] / UHPI_HINT/ PRU1_R30[11]/ GP6[12] | PRU0_R30[31]/ UHPI_HRDY/ PRU1_R30[12] GP6[13] | VP_DIN[11]/ UHPI_HD[3]/ UPP_D[3]/ PRU0_R30[11]/ PRU0_R31[11] | VP_DIN[10]/ UHPI_HD[2]/ UPP_D[2]/ PRU0_R30[10]/ PRU0_R31[10] | R |
| P | $V_{SS}$ | DVDD3318_C | DVDD18 | USB1_VDD18 | USB1_VDD33 | USB0_ID | VP_DIN[8]/ UHPI_HD[0]/ UPP_D[0]/ GP6[5]/ PRU1_R31[0] | USB1_DM | USB1_DP | P |
| N | $V_{SS}$ | $V_{SS}$ | DVDD3318_C | USB0_VDDA18 | PLL1_VDDA | NC | USB0_VDDA12 | USB0_VDDA33 | USB0_VBUS | N |
| M | $V_{SS}$ | USB_CVDD | DVDD3318_C | NC | PLL1_VSSA | TDI | PLL0_VSSA | USB0_DM | USB0_DP | M |
| L | $V_{SS}$ | $CV_{DD}$ | DVDD3318_C | RTC_CVDD | PLL0_VDDA | TMS | TRST | OSCVSS | OSCIN | L |
| K | $V_{SS}$ | $CV_{DD}$ | DVDD3318_C | RESET | DVDD3318_B | EMU1 | RTCK/ GP8[0] | USB0_DRVVBUS | OSCOUT | K |
| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |

**Figure 2-4. Pin Map (Quad B)**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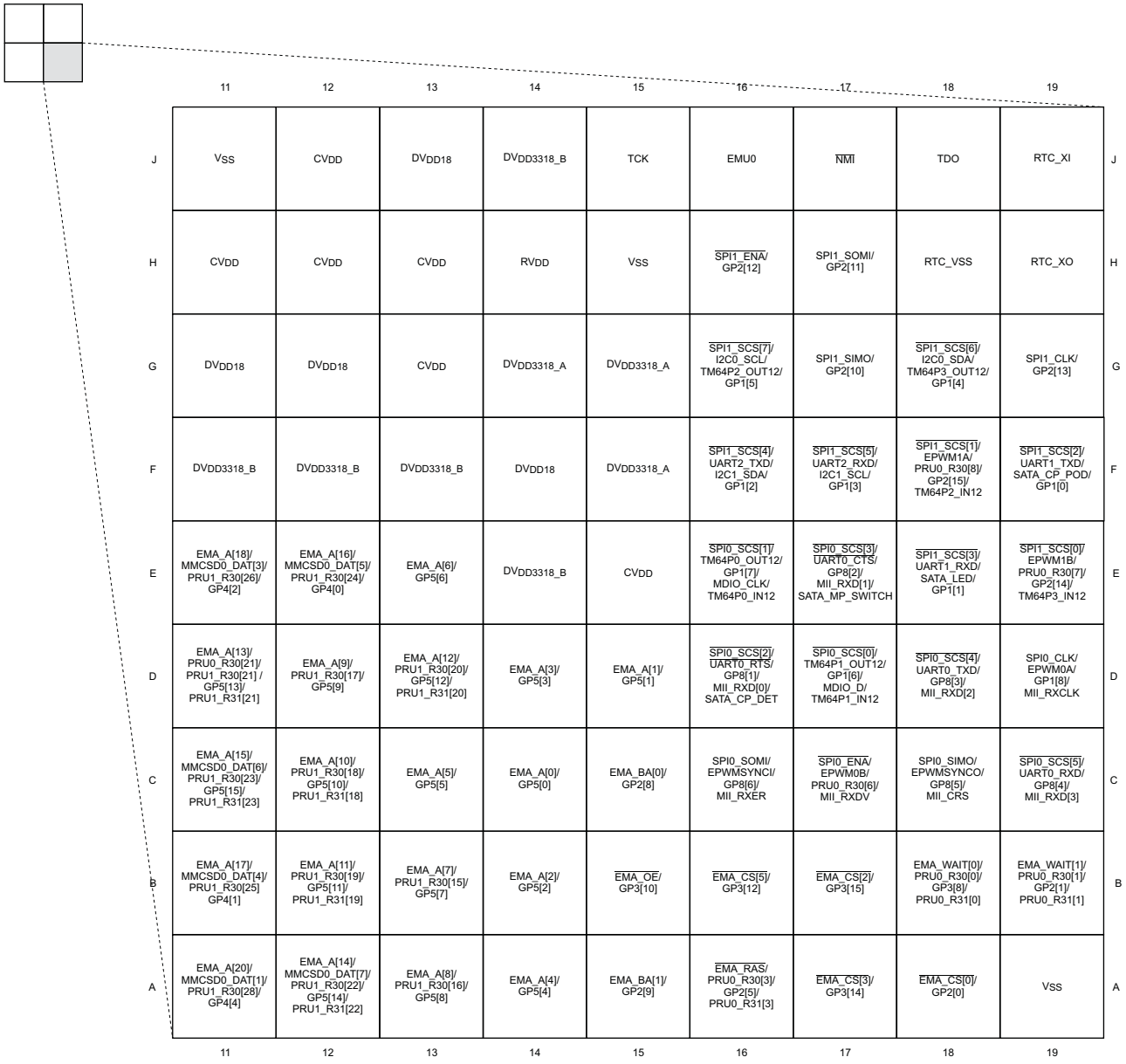
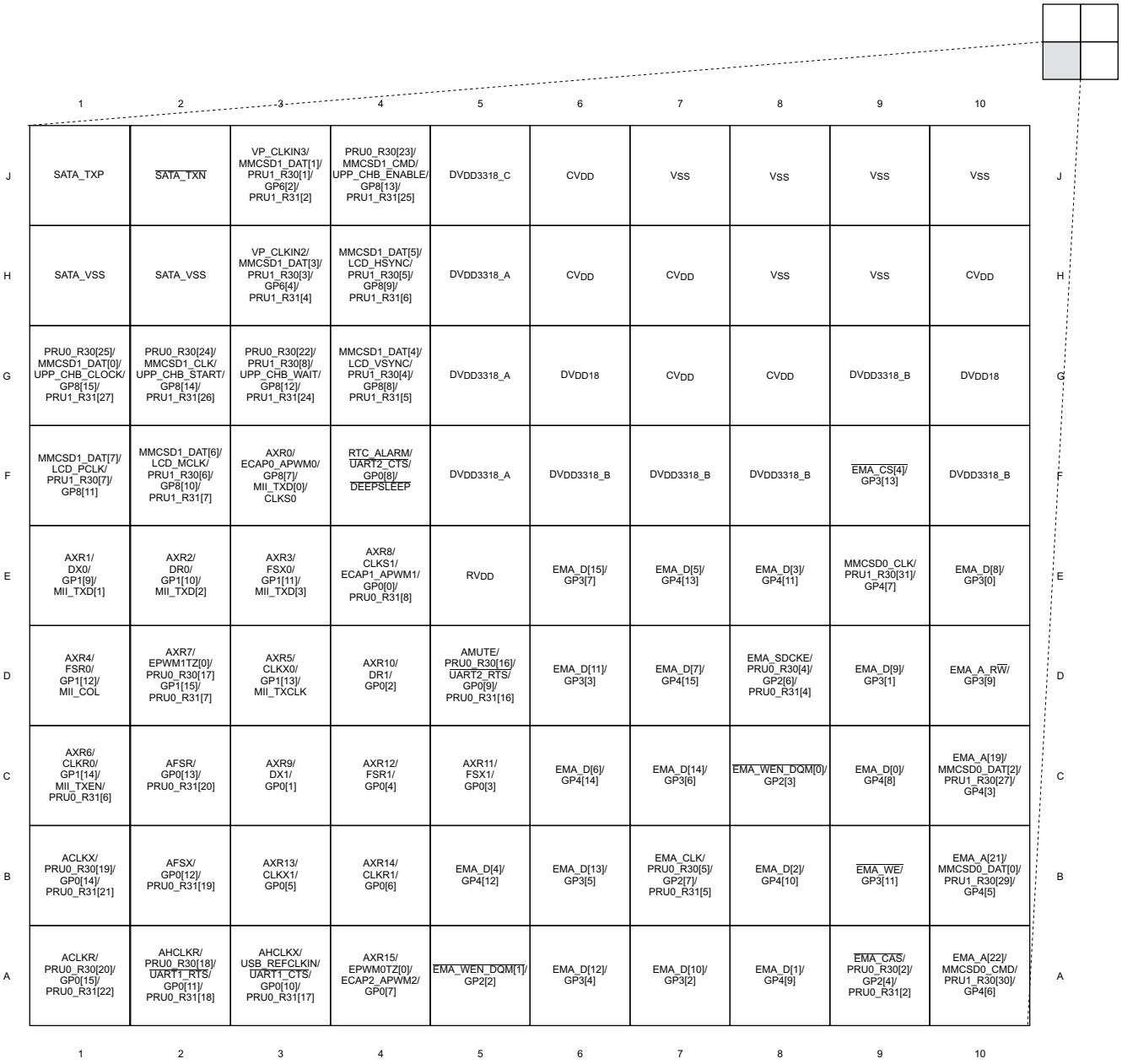


| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |
|---|---|---|---|---|---|---|---|---|---|---|
| J | $V_{SS}$ | $CV_{DD}$ | $DV_{DD18}$ | $DV_{DD3318_B}$ | TCK | EMU0 | $\overline{NMI}$ | TDO | RTC_XI | J |
| H | $CV_{DD}$ | $CV_{DD}$ | $CV_{DD}$ | $RV_{DD}$ | $V_{SS}$ | $\overline{SPI1_ENA}$/ GP2[12] | SPI1_SOMI/ GP2[11] | RTC_VSS | RTC_XO | H |
| G | $DV_{DD18}$ | $DV_{DD18}$ | $CV_{DD}$ | $DV_{DD3318_A}$ | $DV_{DD3318_A}$ | $\overline{SPI1_SCS[7]}$/ I2C0_SCL/ TM64P2_OUT12/ GP1[5] | SPI1_SIMO/ GP2[10] | $\overline{SPI1_SCS[6]}$/ I2C0_SDA/ TM64P3_OUT12/ GP1[4] | SPI1_CLK/ GP2[13] | G |
| F | $DV_{DD3318_B}$ | $DV_{DD3318_B}$ | $DV_{DD3318_B}$ | $DV_{DD18}$ | $DV_{DD3318_A}$ | $\overline{SPI1_SCS[4]}$/ UART2_TXD/ I2C1_SDA/ GP1[2] | $\overline{SPI1_SCS[5]}$/ UART2_RXD/ I2C1_SCL/ GP1[3] | $\overline{SPI1_SCS[1]}$/ EPWM1A/ PRU0_R30[8]/ GP2[15]/ TM64P2_IN12 | $\overline{SPI1_SCS[2]}$/ UART1_TXD/ SATA_CP_POD/ GP1[0] | F |
| E | EMA_A[18]/ MMCSD0_DAT[3]/ PRU1_R30[26]/ GP4[2] | EMA_A[16]/ MMCSD0_DAT[5]/ PRU1_R30[24]/ GP4[0] | EMA_A[6]/ GP5[6] | $DV_{DD3318_B}$ | $CV_{DD}$ | $\overline{SPI0_SCS[1]}$/ TM64P0_OUT12/ GP1[7]/ MDIO_CLK/ TM64P0_IN12 | $\overline{SPI0_SCS[3]}$/ $\overline{UART0_CTS}$/ GP8[2]/ MII_RXD[1]/ SATA_MP_SWITCH | $\overline{SPI1_SCS[3]}$/ UART1_RXD/ SATA_LED/ GP1[1] | $\overline{SPI1_SCS[0]}$/ EPWM1B/ PRU0_R30[7]/ GP2[14]/ TM64P3_IN12 | E |
| D | EMA_A[13]/ PRU0_R30[21]/ PRU1_R30[21] / GP5[13]/ PRU1_R31[21] | EMA_A[9]/ PRU1_R30[17]/ GP5[9] | EMA_A[12]/ PRU1_R30[20]/ GP5[12]/ PRU1_R31[20] | EMA_A[3]/ GP5[3] | EMA_A[1]/ GP5[1] | $\overline{SPI0_SCS[2]}$/ $\overline{UART0_RTS}$/ GP8[1]/ MII_RXD[0]/ SATA_CP_DET | $\overline{SPI0_SCS[0]}$/ TM64P1_OUT12/ GP1[6]/ MDIO_D/ TM64P1_IN12 | $\overline{SPI0_SCS[4]}$/ $\overline{UART0_TXD}$/ GP8[3]/ MII_RXD[2] | SPI0_CLK/ EPWM0A/ GP1[8]/ MII_RXCLK | D |
| C | EMA_A[15]/ MMCSD0_DAT[6]/ PRU1_R30[23]/ GP5[15]/ PRU1_R31[23] | EMA_A[10]/ PRU1_R30[18]/ GP5[10]/ PRU1_R31[18] | EMA_A[5]/ GP5[5] | EMA_A[0]/ GP5[0] | EMA_BA[0]/ GP2[8] | SPI0_SOMI/ EPWMSYNCI/ GP8[6]/ MII_RXER | $\overline{SPI0_ENA}$/ EPWM0B/ PRU0_R30[6]/ MII_RXDV | SPI0_SIMO/ EPWMSYNCO/ GP8[5]/ MII_CRS | $\overline{SPI0_SCS[5]}$/ $\overline{UART0_RXD}$/ GP8[4]/ MII_RXD[3] | C |
| B | EMA_A[17]/ MMCSD0_DAT[4]/ PRU1_R30[25] GP4[1] | EMA_A[11]/ PRU1_R30[19]/ GP5[11]/ PRU1_R31[19] | EMA_A[7]/ PRU1_R30[15]/ GP5[7] | EMA_A[2]/ GP5[2] | $\overline{EMA_OE}$/ GP3[10] | $\overline{EMA_CS[5]}$/ GP3[12] | $\overline{EMA_CS[2]}$/ GP3[15] | EMA_WAIT[0]/ PRU0_R30[0]/ GP3[8]/ PRU0_R31[0] | EMA_WAIT[1]/ PRU0_R30[1]/ GP2[1]/ PRU0_R31[1] | B |
| A | EMA_A[20]/ MMCSD0_DAT[1]/ PRU1_R30[28]/ GP4[4] | EMA_A[14]/ MMCSD0_DAT[7]/ PRU1_R30[22]/ GP5[14]/ PRU1_R31[22] | EMA_A[8]/ PRU1_R30[16]/ GP5[8] | EMA_A[4]/ GP5[4] | EMA_BA[1]/ GP2[9] | $\overline{EMA_RAS}$/ PRU0_R30[3]/ GP2[5]/ PRU0_R31[3] | $\overline{EMA_CS[3]}$/ GP3[14] | $\overline{EMA_CS[0]}$/ GP2[0] | $V_{SS}$ | A |
| | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | |

**Figure 2-5. Pin Map (Quad C)**



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| J | SATA_TXP | SATA_TXN | VP_CLKIN3/ MMCSD1_DAT[1]/ PRU1_R30[1]/ GP6[2]/ PRU1_R31[2] | PRU0_R30[23]/ MMCSD1_CMD/ UPP_CHB_ENABLE/ GP8[13]/ PRU1_R31[25] | DVDD3318_C | CVDD | VSS | VSS | VSS | VSS | J |
| H | SATA_VSS | SATA_VSS | VP_CLKIN2/ MMCSD1_DAT[3]/ PRU1_R30[3]/ GP6[4]/ PRU1_R31[4] | MMCSD1_DAT[5]/ LCD_HSYNC/ PRU1_R30[5]/ GP8[9]/ PRU1_R31[6] | DVDD3318_A | CVDD | CVDD | VSS | VSS | CVDD | H |
| G | PRU0_R30[25]/ MMCSD1_DAT[0]/ UPP_CHB_CLOCK/ GP8[15]/ PRU1_R31[27] | PRU0_R30[24]/ MMCSD1_CLK/ UPP_CHB_START/ GP8[14]/ PRU1_R31[26] | PRU0_R30[22]/ PRU1_R30[8]/ UPP_CHB_WAIT/ GP8[12]/ PRU1_R31[24] | MMCSD1_DAT[4]/ LCD_VSYNC/ PRU1_R30[4]/ GP8[8]/ PRU1_R31[5] | DVDD3318_A | DVDD18 | CVDD | CVDD | DVDD3318_B | DVDD18 | G |
| F | MMCSD1_DAT[7]/ LCD_PCLK/ PRU1_R30[7]/ GP8[11] | MMCSD1_DAT[6]/ LCD_MCLK/ PRU1_R30[6]/ GP8[10]/ PRU1_R31[7] | AXR0/ ECAP0_APWM0/ GP8[7]/ MII_TXD[0]/ CLKS0 | RTC_ALARM/ UART2_CTS/ GP0[8]/ DEEPSLEEP | DVDD3318_A | DVDD3318_B | DVDD3318_B | DVDD3318_B | EMA_CS[4]/ GP3[13] | DVDD3318_B | F |
| E | AXR1/ DX0/ GP1[9]/ MII_TXD[1] | AXR2/ DR0/ GP1[10]/ MII_TXD[2] | AXR3/ FSX0/ GP1[11]/ MII_TXD[3] | AXR8/ CLKS1/ ECAP1_APWM1/ GP0[0]/ PRU0_R31[8] | RVDD | EMA_D[15]/ GP3[7] | EMA_D[5]/ GP4[13] | EMA_D[3]/ GP4[11] | MMCSD0_CLK/ PRU1_R30[31]/ GP4[7] | EMA_D[8]/ GP3[0] | E |
| D | AXR4/ FSR0/ GP1[12]/ MII_COL | AXR7/ EPWM1TZ[0]/ PRU0_R30[17] GP1[15]/ PRU0_R31[7] | AXR5/ CLKX0/ GP1[13]/ MII_TXCLK | AXR10/ DR1/ GP0[2] | AMUTE/ PRU0_R30[16]/ UART2_RTS/ GP0[9]/ PRU0_R31[16] | EMA_D[11]/ GP3[3] | EMA_D[7]/ GP4[15] | EMA_SDCKE/ PRU0_R30[4]/ GP2[6]/ PRU0_R31[4] | EMA_D[9]/ GP3[1] | EMA_A_RW/ GP3[9] | D |
| C | AXR6/ CLKR0/ GP1[14]/ MII_TXEN/ PRU0_R31[6] | AFSR/ GP0[13]/ PRU0_R31[20] | AXR9/ DX1/ GP0[1] | AXR12/ FSR1/ GP0[4] | AXR11/ FSX1/ GP0[3] | EMA_D[6]/ GP4[14] | EMA_D[14]/ GP3[6] | EMA_WEN_DQM[0]/ GP2[3] | EMA_D[0]/ GP4[8] | EMA_A[19]/ MMCSD0_DAT[2]/ PRU1_R30[27]/ GP4[3] | C |
| B | ACLKX/ PRU0_R30[19]/ GP0[14]/ PRU0_R31[21] | AFSX/ GP0[12]/ PRU0_R31[19] | AXR13/ CLKX1/ GP0[5] | AXR14/ CLKR1/ GP0[6] | EMA_D[4]/ GP4[12] | EMA_D[13]/ GP3[5] | EMA_CLK/ PRU0_R30[5]/ GP2[7]/ PRU0_R31[5] | EMA_D[2]/ GP4[10] | EMA_WE/ GP3[11] | EMA_A[21]/ MMCSD0_DAT[0]/ PRU1_R30[29]/ GP4[5] | B |
| A | ACLKR/ PRU0_R30[20]/ GP0[15]/ PRU0_R31[22] | AHCLKR/ PRU0_R30[18]/ UART1_RTS/ GP0[11]/ PRU0_R31[18] | AHCLKX/ USB_REFCLKIN/ UART1_CTS/ GP0[10]/ PRU0_R31[17] | AXR15/ EPWM0TZ[0]/ ECAP2_APWM2/ GP0[7] | EMA_WEN_DQM[1]/ GP2[2] | EMA_D[12]/ GP3[4] | EMA_D[10]/ GP3[2] | EMA_D[1]/ GP4[9] | EMA_CAS/ PRU0_R30[2]/ GP2[4]/ PRU0_R31[2] | EMA_A[22]/ MMCSD0_CMD/ PRU1_R30[30]/ GP4[6] | A |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | |

**Figure 2-6. Pin Map (Quad D)**

## 2.7 Pin Multiplexing Control

Device level pin multiplexing is controlled by registers PINMUX0 - PINMUX19 in the SYSCFG module.

For the device family, pin multiplexing can be controlled on a pin-by-pin basis. Each pin that is multiplexed with several different functions has a corresponding 4-bit field in one of the PINMUX registers.

Pin multiplexing selects which of several peripheral pin functions controls the pin's IO buffer **output** data and **output enable** values only. The default pin multiplexing control for almost every pin is to select 'none' of the peripheral functions in which case the pin's IO buffer is held tri-stated.

Note that the **input** from each pin is always routed to **all** of the peripherals that share the pin; the PINMUX registers have no effect on input from a pin.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## 2.8 Terminal Functions

Table 2-5 to Table 2-31 identify the external signal names, the associated pin/ball numbers along with the mechanical package designator, the pin type (I, O, IO, OZ, or PWR), whether the pin/ball has any internal pullup/pulldown resistors, whether the pin/ball is configurable as an IO in GPIO mode, and a functional pin description.

### 2.8.1 Device Reset, NMI and JTAG

**Table 2-5. Reset, NMI and JTAG Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **RESET** | | | | | |
| **$\overline{\text{RESET}}$** | K14 | I | IPU | B | Device reset input |
| **$\overline{\text{NMI}}$** | J17 | I | IPU | B | Non-Maskable Interrupt |
| **$\overline{\text{RESETOUT}}$** / $\overline{\text{UHPI_HAS}}$ / PRU1_R30[14] / GP6[15] | T17 | O(4) | CP[21] | C | Reset output |
| **JTAG** | | | | | |
| **TMS** | L16 | I | IPU | B | JTAG test mode select |
| **TDI** | M16 | I | IPU | B | JTAG test data input |
| **TDO** | J18 | O | IPU | B | JTAG test data output |
| **TCK** | J15 | I | IPU | B | JTAG test clock |
| **$\overline{\text{TRST}}$** | L17 | I | IPD | B | JTAG test reset |
| **EMU0** | J16 | I/O | IPU | B | Emulation pin |
| **EMU1** | K16 | I/O | IPU | B | Emulation pin |
| **RTCK**/ GP8[0](5) | K17 | I/O | IPD | B | General-purpose input/output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor, IPU = Internal Pullup resistor. CP[n] = configurable pull-up/pull-down (where n is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.
(4) Open drain mode for $\overline{\text{RESETOUT}}$ function.
(5) GP8[0] is initially configured as a reserved function after reset and will not be in a predictable state. This signal will only be stable after the GPIO configuration for this pin has been completed. Users should carefully consider the system implications of this pin being in an unknown state after reset.

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### 2.8.2 High-Frequency Oscillator and PLL

**Table 2-6. High-Frequency Oscillator and PLL Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **CLKOUT** / $\overline{\text{UHPI_HDS2}}$ / PRU1_R30[13] / GP6[14] | T18 | O | CP[22] | C | PLL Observation Clock |
| **1.2-V OSCILLATOR** | | | | | |
| **OSCIN** | L19 | I | — | — | Oscillator input |
| **OSCOUT** | K19 | O | — | — | Oscillator output |
| **OSCVSS** | L18 | GND | — | — | Oscillator ground |
| **1.2-V PLL0** | | | | | |
| **PLL0_VDDA** | L15 | PWR | — | — | PLL analog $V_{DD}$ (1.2-V filtered supply) |
| **PLL0_VSSA** | M17 | GND | — | — | PLL analog $V_{SS}$ (for filter) |
| **1.2-V PLL1** | | | | | |
| **PLL1_VDDA** | N15 | PWR | — | — | PLL analog $V_{DD}$ (1.2-V filtered supply) |
| **PLL1_VSSA** | M15 | GND | — | — | PLL analog $V_{SS}$ (for filter) |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.3 Real-Time Clock and 32-kHz Oscillator

**Table 2-7. Real-Time Clock (RTC) and 1.2-V, 32-kHz Oscillator Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **RTC_XI** | J19 | I | — | — | RTC 32-kHz oscillator input |
| **RTC_XO** | H19 | O | — | — | RTC 32-kHz oscillator output |
| **RTC_ALARM** / $\overline{\text{UART2_CTS}}$ / GP0[8] / $\overline{\text{DEEPSLEEP}}$ | F4 | O | CP[0] | A | RTC Alarm |
| **RTC_CVDD** | L14 | PWR | — | — | RTC module core power (isolated from chip $CV_{DD}$) |
| **RTC_$V_{ss}$** | H18 | GND | — | — | Oscillator ground |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

### 2.8.4 DEEPSLEEP Power Control

**Table 2-8. DEEPSLEEP Power Control Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| RTC_ALARM / $\overline{\text{UART2_CTS}}$ / GP0[8] / **$\overline{\text{DEEPSLEEP}}$** | F4 | I | CP[0] | A | DEEPSLEEP power control output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.
(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 2.8.5 External Memory Interface A (EMIFA)

**Table 2-9. External Memory Interface A (EMIFA) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **EMA_D[15]** / GP3[7] | E6 | I/O | CP[17] | B | EMIFA data bus |
| **EMA_D[14]** / GP3[6] | C7 | I/O | CP[17] | B | |
| **EMA_D[13]** / GP3[5] | B6 | I/O | CP[17] | B | |
| **EMA_D[12]** / GP3[4] | A6 | I/O | CP[17] | B | |
| **EMA_D[11]** / GP3[3] | D6 | I/O | CP[17] | B | |
| **EMA_D[10]** / GP3[2] | A7 | I/O | CP[17] | B | |
| **EMA_D[9]** / GP3[1] | D9 | I/O | CP[17] | B | |
| **EMA_D[8]** / GP3[0] | E10 | I/O | CP[17] | B | |
| **EMA_D[7]** / GP4[15] | D7 | I/O | CP[17] | B | |
| **EMA_D[6]** / GP4[14] | C6 | I/O | CP[17] | B | |
| **EMA_D[5]** / GP4[13] | E7 | I/O | CP[17] | B | |
| **EMA_D[4]** / GP4[12] | B5 | I/O | CP[17] | B | |
| **EMA_D[3]** / GP4[11] | E8 | I/O | CP[17] | B | |
| **EMA_D[2]** / GP4[10] | B8 | I/O | CP[17] | B | |
| **EMA_D[1]** / GP4[9] | A8 | I/O | CP[17] | B | |
| **EMA_D[0]** / GP4[8] | C9 | I/O | CP[17] | B | |
| **EMA_A[22]** / MMCSD0_CMD / PRU1_R30[30] / GP4[6] | A10 | O | CP[18] | B | EMIFA address bus |
| **EMA_A[21]** / MMCSD0_DAT[0] / PRU1_R30[29] / GP4[5] | B10 | O | CP[18] | B | |
| **EMA_A[20]** / MMCSD0_DAT[1] / PRU1_R30[28] / GP4[4] | A11 | O | CP[18] | B | |
| **EMA_A[19]** / MMCSD0_DAT[2] / PRU1_R30[27] / GP4[3] | C10 | O | CP[18] | B | |
| **EMA_A[18]** / MMCSD0_DAT[3] / PRU1_R30[26] / GP4[2] | E11 | O | CP[18] | B | |
| **EMA_A[17]** / MMCSD0_DAT[4] / PRU1_R30[25] / GP4[1] | B11 | O | CP[18] | B | |
| **EMA_A[16]** / MMCSD0_DAT[5] / PRU1_R30[24] / GP4[0] | E12 | O | CP[18] | B | |
| **EMA_A[15]** / MMCSD0_DAT[6] / PRU1_R30[23] / GP5[15] / PRU1_R31[23] | C11 | O | CP[19] | B | |
| **EMA_A[14]** / MMCSD0_DAT[7] / PRU1_R30[22] / GP5[14] / PRU1_R31[22] | A12 | O | CP[19] | B | |
| **EMA_A[13]** / PRU0_R30[21] / PRU1_R30[21] / GP5[13] / PRU1_R31[21] | D11 | O | CP[19] | B | |
| **EMA_A[12]** / PRU1_R30[20] / GP5[12] / PRU1_R31[20] | D13 | O | CP[19] | B | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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**Table 2-9. External Memory Interface A (EMIFA) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **EMA_A[11]** / PRU1_R30[19] / GP5[11] / PRU1_R31[19] | B12 | O | CP[19] | B | EMIFA address bus |
| **EMA_A[10]** / PRU1_R30[18] / GP5[10] / PRU1_R31[18] | C12 | O | CP[19] | B | |
| **EMA_A[9]** / PRU1_R30[17] / GP5[9] | D12 | O | CP[19] | B | |
| **EMA_A[8]** / PRU1_R30[16] / GP5[8] | A13 | O | CP[19] | B | |
| **EMA_A[7]** / PRU1_R30[15] / GP5[7] | B13 | O | CP[20] | B | |
| **EMA_A[6]** / GP5[6] | E13 | O | CP[20] | B | |
| **EMA_A[5]** / GP5[5] | C13 | O | CP[20] | B | |
| **EMA_A[4]** / GP5[4] | A14 | O | CP[20] | B | |
| **EMA_A[3]** / GP5[3] | D14 | O | CP[20] | B | |
| **EMA_A[2]** / GP5[2] | B14 | O | CP[20] | B | |
| **EMA_A[1]** / GP5[1] | D15 | O | CP[20] | B | |
| **EMA_A[0]** / GP5[0] | C14 | O | CP[20] | B | |
| **EMA_BA[0]** / GP2[8] | C15 | O | CP[16] | B | EMIFA bank address |
| **EMA_BA[1]** / GP2[9] | A15 | O | CP[16] | B | |
| **EMA_CLK** / PRU0_R30[5] / GP2[7] / PRU0_R31[5] | B7 | O | CP[16] | B | EMIFA clock |
| **EMA_SDCKE** / PRU0_R30[4] / GP2[6] / PRU0_R31[4] | D8 | O | CP[16] | B | EMIFA SDRAM clock enable |
| **$\overline{\text{EMA_RAS}}$** / PRU0_R30[3] / GP2[5] / PRU0_R31[3] | A16 | O | CP[16] | B | EMIFA SDRAM row address strobe |
| **$\overline{\text{EMA_CAS}}$** / PRU0_R30[2] / GP2[4] / PRU0_R31[2] | A9 | O | CP[16] | B | EMIFA SDRAM column address strobe |
| **$\overline{\text{EMA_CS[0]}}$** / GP2[0] | A18 | O | CP[16] | B | EMIFA SDRAM Chip Select |
| **$\overline{\text{EMA_CS[2]}}$** / GP3[15] | B17 | O | CP[16] | B | EMIFA Async chip select |
| **$\overline{\text{EMA_CS[3]}}$** / GP3[14] | A17 | O | CP[16] | B | |
| **$\overline{\text{EMA_CS[4]}}$** / GP3[13] | F9 | O | CP[16] | B | |
| **$\overline{\text{EMA_CS[5]}}$** / GP3[12] | B16 | O | CP[16] | B | |
| **EMA_A_$\overline{\text{RW}}$** / GP3[9] | D10 | O | CP[16] | B | EMIFA Async Read/Write control |
| **$\overline{\text{EMA_WE}}$** / GP3[11] | B9 | O | CP[16] | B | EMIFA SDRAM write enable |
| **$\overline{\text{EMA_WEN_DQM[1]}}$** / GP2[2] | A5 | O | CP[16] | B | EMIFA write enable/data mask for EMA_D[15:8] |
| **$\overline{\text{EMA_WEN_DQM[0]}}$** / GP2[3] | C8 | O | CP[16] | B | EMIFA write enable/data mask for EMA_D[7:0] |
| **$\overline{\text{EMA_OE}}$** / GP3[10] | B15 | O | CP[16] | B | EMIFA output enable |
| **EMA_WAIT[0]** / PRU0_R30[0] / GP3[8] / PRU0_R31[0] | B18 | I | CP[16] | B | EMIFA wait input/interrupt |
| **EMA_WAIT[1]** / PRU0_R30[1] / GP2[1] / PRU0_R31[1] | B19 | I | CP[16] | B | |

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### 2.8.6 DDR2 Controller (DDR2)

**Table 2-10. DDR2 Controller (DDR2) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| **DDR_D[15]** | W10 | I/O | IPD | DDR2 SDRAM data bus |
| **DDR_D[14]** | U11 | I/O | IPD | |
| **DDR_D[13]** | V10 | I/O | IPD | |
| **DDR_D[12]** | U10 | I/O | IPD | |
| **DDR_D[11]** | T12 | I/O | IPD | |
| **DDR_D[10]** | T10 | I/O | IPD | |
| **DDR_D[9]** | T11 | I/O | IPD | |
| **DDR_D[8]** | T13 | I/O | IPD | |
| **DDR_D[7]** | W11 | I/O | IPD | |
| **DDR_D[6]** | W12 | I/O | IPD | |
| **DDR_D[5]** | V12 | I/O | IPD | |
| **DDR_D[4]** | V13 | I/O | IPD | |
| **DDR_D[3]** | U13 | I/O | IPD | |
| **DDR_D[2]** | V14 | I/O | IPD | |
| **DDR_D[1]** | U14 | I/O | IPD | |
| **DDR_D[0]** | U15 | I/O | IPD | |
| **DDR_A[13]** | T5 | O | IPD | DDR2 row/column address |
| **DDR_A[12]** | V4 | O | IPD | |
| **DDR_A[11]** | T4 | O | IPD | |
| **DDR_A[10]** | W4 | O | IPD | |
| **DDR_A[9]** | T6 | O | IPD | |
| **DDR_A[8]** | U4 | O | IPD | |
| **DDR_A[7]** | U6 | O | IPD | |
| **DDR_A[6]** | W5 | O | IPD | |
| **DDR_A[5]** | V5 | O | IPD | |
| **DDR_A[4]** | U5 | O | IPD | |
| **DDR_A[3]** | V6 | O | IPD | |
| **DDR_A[2]** | W6 | O | IPD | |
| **DDR_A[1]** | T7 | O | IPD | |
| **DDR_A[0]** | U7 | O | IPD | |
| **DDR_CLKP** | W8 | O | IPD | DDR2 clock (positive) |
| **$\overline{\text{DDR_CLKN}}$** | W7 | O | IPD | DDR2 clock (negative) |
| **DDR_CKE** | V7 | O | IPD | DDR2 clock enable |
| **$\overline{\text{DDR_WE}}$** | T8 | O | IPD | DDR2 write enable |
| **$\overline{\text{DDR_RAS}}$** | W9 | O | IPD | DDR2 row address strobe |
| **$\overline{\text{DDR_CAS}}$** | U9 | O | IPD | DDR2 column address strobe |
| **$\overline{\text{DDR_CS}}$** | V9 | O | IPD | DDR2 chip select |
| **DDR_DQM[0]** | W13 | O | IPD | DDR2 data mask outputs |
| **DDR_DQM[1]** | R10 | O | IPD | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.


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**Table 2-10. DDR2 Controller (DDR2) Terminal Functions (continued)**

| SIGNAL | | TYPE[1] | PULL[2] | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| **DDR_DQS[0]** | T14 | I/O | IPD | DDR2 data strobe inputs/outputs |
| **DDR_DQS[1]** | V11 | I/O | IPD | |
| **DDR_BA[2]** | U8 | O | IPD | DDR2 SDRAM bank address |
| **DDR_BA[1]** | T9 | O | IPD | |
| **DDR_BA[0]** | V8 | O | IPD | |
| **DDR_DQGATE0** | R11 | O | IPD | DDR2 loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE1 with same constraints as used for DDR clock and data. |
| **DDR_DQGATE1** | R12 | I | IPD | DDR2 loopback signal for external DQS gating. Route to DDR and back to DDR_DQGATE0 with same constraints as used for DDR clock and data. |
| **DDR_ZP** | U12 | O | — | DDR2 reference output for drive strength calibration of N and P channel outputs. Tie to ground via 50 ohm resistor @ 5% tolerance. |
| **DDR_VREF** | R6 | I | — | DDR voltage input for the DDR2/mDDR I/O buffers. Note even in the case of mDDR an external resistor divider connected to this pin is necessary. |
| **DDR_DVDD18** | N6, N9, N10, P7, P8, P9, P10, R7, R8, R9 | PWR | — | DDR PHY 1.8V power supply pins |

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### 2.8.7 Serial Peripheral Interface Modules (SPI)

**Table 2-11. Serial Peripheral Interface (SPI) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **SPI0** | | | | | |
| **SPI0_CLK** / EPWM0A / GP1[8] / MII_RXCLK | D19 | I/O | CP[7] | A | SPI0 clock |
| **SPI0_ENA** / EPWM0B / PRU0_R30[6] / MII_RXDV | C17 | I/O | CP[7] | A | SPI0 enable |
| **SPI0_SCS[0]** / TM64P1_OUT12 / GP1[6] / MDIO_D / TM64P1_IN12 | D17 | I/O | CP[10] | A | SPI0 chip selects |
| **SPI0_SCS[1]** / TM64P0_OUT12 / GP1[7] / MDIO_CLK / TM64P0_IN12 | E16 | I/O | CP[10] | A | |
| **SPI0_SCS[2]** / UART0_RTS / GP8[1] / MII_RXD[0] /SATA_CP_DET | D16 | I/O | CP[9] | A | |
| **SPI0_SCS[3]** / UART0_CTS / GP8[2] / MII_RXD[1] / SATA_MP_SWITCH | E17 | I/O | CP[9] | A | |
| **SPI0_SCS[4]** / UART0_TXD / GP8[3] / MII_RXD[2] | D18 | I/O | CP[8] | A | |
| **SPI0_SCS[5]** / UART0_RXD / GP8[4] / MII_RXD[3] | C19 | I/O | CP[8] | A | |
| **SPI0_SIMO** / EPWMSYNCO / GP8[5] / MII_CRS | C18 | I/O | CP[7] | A | SPI0 data slave-in-master-out |
| **SPI0_SOMI** / EPWMSYNCI / GP8[6] / MII_RXER | C16 | I/O | CP[7] | A | SPI0 data slave-out-master-in |
| **SPI1** | | | | | |
| **SPI1_CLK** / GP2[13] | G19 | I/O | CP[15] | A | SPI1 clock |
| **SPI1_ENA** / GP2[12] | H16 | I/O | CP[15] | A | SPI1 enable |
| **SPI1_SCS[0]** / EPWM1B / PRU0_R30[7] / GP2[14] / TM64P3_IN12 | E19 | I/O | CP[14] | A | SPI1 chip selects |
| **SPI1_SCS[1]** / EPWM1A / PRU0_R30[8] / GP2[15] / TM64P2_IN12 | F18 | I/O | CP[14] | A | |
| **SPI1_SCS[2]** / UART1_TXD / SATA_CP_POD / GP1[0] | F19 | I/O | CP[13] | A | |
| **SPI1_SCS[3]** / UART1_RXD / SATA_LED / GP1[1] | E18 | I/O | CP[13] | A | |
| **SPI1_SCS[4]** / UART2_TXD / I2C1_SDA / GP1[2] | F16 | I/O | CP[12] | A | |
| **SPI1_SCS[5]** / UART2_RXD / I2C1_SCL / GP1[3] | F17 | I/O | CP[12] | A | |
| **SPI1_SCS[6]** / I2C0_SDA / TM64P3_OUT12 / GP1[4] | G18 | I/O | CP[11] | A | |
| **SPI1_SCS[7]** / I2C0_SCL / TM64P2_OUT12 / GP1[5] | G16 | I/O | CP[11] | A | |
| **SPI1_SIMO** / GP2[10] | G17 | I/O | CP[15] | A | SPI1 data slave-in-master-out |
| **SPI1_SOMI** / GP2[11] | H17 | I/O | CP[15] | A | SPI1 data slave-out-master-in |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.8 Programmable Real-Time Unit (PRU)

**Table 2-12. Programmable Real-Time Unit (PRU) Terminal Functions**

| SIGNAL | | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **PRU0_R30[31]** / $\overline{\text{UHPI_HRDY}}$ / PRU1_R30[12] / GP6[13] | R17 | O | CP[23] | C | PRU0 Output Signals |
| **PRU0_R30[30]** / $\overline{\text{UHPI_HINT}}$ / PRU1_R30[11] / GP6[12] | R16 | O | CP[23] | C | |
| **PRU0_R30[29]**/ UHPI_HCNTL0 / UPP_CHA_CLOCK / GP6[11] | U17 | O | CP[24] | C | |
| **PRU0_R30[28]** / UHPI_HCNTL1 / UPP_CHA_START / GP6[10] | W15 | O | CP[24] | C | |
| **PRU0_R30[27]** / UHPI_HHWIL / UPP_CHA_ENABLE / GP6[9] | U16 | O | CP[24] | C | |
| **PRU0_R30[26]** / UHPI_HR$\overline{\text{W}}$ / UPP_CHA_WAIT / GP6[8] / PRU1_R31[17] | T15 | O | CP[24] | C | |
| **PRU0_R30[25]** / MMCSD1_DAT[0] / UPP_CHB_CLOCK / GP8[15] / PRU1_R31[27] | G1 | O | CP30] | C | |
| **PRU0_R30[24]** / MMCSD1_CLK / UPP_CHB_START / GP8[14] / PRU1_R31[26] | G2 | O | CP[30] | C | |
| **PRU0_R30[23]** / MMCSD1_CMD / UPP_CHB_ENABLE / GP8[13] / PRU1_R31[25] | J4 | O | CP[30] | C | |
| **PRU0_R30[22]** / PRU1_R30[8] / UPP_CHB_WAIT / GP8[12] / PRU1_R31[24] | G3 | O | CP[30] | C | |
| EMA_A[13] / **PRU0_R30[21]** / PRU1_R30[21] / GP5[13] / PRU1_R31[21] | D11 | O | CP[19] | B | |
| ACLKR / **PRU0_R30[20] /** GP0[15] / PRU0_R31[22] | A1 | O | CP[0] | A | |
| ACLKX / **PRU0_R30[19]** / GP0[14] / PRU0_R31[21] | B1 | O | CP[0] | A | |
| AHCLKR / **PRU0_R30[18]** / $\overline{\text{UART1_RTS}}$ / GP0[11] / PRU0_R31[18] | A2 | O | CP[0] | A | |
| AXR7 / EPWM1TZ[0] / **PRU0_R30[17]** / GP1[15] / PRU0_R31[7] | D2 | O | CP[4] | A | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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**Table 2-12. Programmable Real-Time Unit (PRU) Terminal Functions (continued)**

| SIGNAL | | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| AMUTE / **PRU0_R30[16]** / UART2_RTS / GP0[9] / PRU0_R31[16] | D5 | O | CP[0] | A | PRU0 Output Signals |
| VP_DIN[15]_VSYNC / UHPI_HD[7] / UPP_D[7] / **PRU0_R30[15]** / PRU0_R31[15] | V18 | O | CP[27] | C | |
| VP_DIN[14]_HSYNC / UHPI_HD[6] / UPP_D[6] / **PRU0_R30[14]** / PRU0_R31[14] | V19 | O | CP[27] | C | |
| VP_DIN[13]_FIELD / UHPI_HD[5] / UPP_D[5] / **PRU0_R30[13]** / PRU0_R31[13] | U19 | O | CP[27] | C | |
| VP_DIN[12] / UHPI_HD[4] / UPP_D[4] / **PRU0_R30[12]** / PRU0_R31[12] | T16 | O | CP[27] | C | |
| VP_DIN[11] / UHPI_HD[3] / UPP_D[3] / **PRU0_R30[11]** / PRU0_R31[11] | R18 | O | CP[27] | C | |
| VP_DIN[10] / UHPI_HD[2] / UPP_D[2] / **PRU0_R30[10]** / PRU0_R31[10] | R19 | O | CP[27] | C | |
| VP_DIN[9] / UHPI_HD[1] / UPP_D[1] / **PRU0_R30[9]** / PRU0_R31[9] | R15 | O | CP[27] | C | |
| SPI1_SCS[1] / EPWM1A / **PRU0_R30[8]** / GP2[15] / TM64P2_IN12 | F18 | O | CP[14] | A | |
| SPI1_SCS[0] / EPWM1B / **PRU0_R30[7]** / GP2[14] / TM64P3_IN12 | E19 | O | CP[14] | A | |
| SPI0_ENA / EPWM0B / **PRU0_R30[6]** / MII_RXDV | C17 | O | CP[7] | A | |
| EMA_CLK / **PRU0_R30[5]** / GP2[7] / PRU0_R31[5] | B7 | O | CP[16] | B | |
| EMA_SDCKE / **PRU0_R30[4]** / GP2[6] / PRU0_R31[4] | D8 | O | CP[16] | B | |
| EMA_RAS / **PRU0_R30[3]** / GP2[5] / PRU0_R31[3] | A16 | O | CP[16] | B | |
| EMA_CAS / **PRU0_R30[2]** / GP2[4] / PRU0_R31[2] | A9 | O | CP[16] | B | |
| EMA_WAIT[1] / **PRU0_R30[1]** / GP2[1] / PRU0_R31[1] | B19 | O | CP[16] | B | |
| EMA_WAIT[0] / **PRU0_R30[0]** / GP3[8] / PRU0_R31[0] | B18 | O | CP[16] | B | |


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**Table 2-12. Programmable Real-Time Unit (PRU) Terminal Functions (continued)**

| SIGNAL | | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| VP_DIN[7] / UHPI_HD[15] / UPP_D[15] / RMII_TXD[1] / **PRU0_R31[29]** | U18 | I | CP[26] | C | PRU0 Input Signals |
| VP_DIN[6] / UHPI_HD[14] / UPP_D[14] / RMII_TXD[0] / **PRU0_R31[28]** | V16 | I | CP[26] | C | |
| VP_DIN[5] / UHPI_HD[13] / UPP_D[13] / RMII_TXEN / **PRU0_R31[27]** | R14 | I | CP[26] | C | |
| VP_DIN[4] / UHPI_HD[11] / UPP_D[12] / RMII_RXD[1] / **PRU0_R31[26]** | W16 | I | CP[26] | C | |
| VP_DIN[3] / UHPI_HD[11] / UPP_D[11] / RMII_RXD[0] / **PRU0_R31[25]** | V17 | I | CP[26] | C | |
| VP_DIN[2] / UHPI_HD[10] / UPP_D[10] / RMII_RXER / **PRU0_R31[24]** | W17 | I | CP[26] | C | |
| VP_DIN[1] / UHPI_HD[9] / UPP_D[9] / RMII_MHZ_50_CLK / **PRU0_R31[23]** | W18 | I | CP[26] | C | |
| ACLKR / PRU0_R30[20] / GP0[15] / **PRU0_R31[22]** | A1 | I | CP[0] | A | |
| ACLKX / PRU0_R30[19] / GP0[14] / **PRU0_R31[21]** | B1 | I | CP[0] | A | |
| AFSR / GP0[13] / **PRU0_R31[20]** | C2 | I | CP[0] | A | |
| AFSX / GP0[12] / **PRU0_R31[19]** | B2 | I | CP[0] | A | |
| AHCLKR / PRU0_R30[18] / $\overline{\text{UART1_RTS}}$ / GP0[11] / **PRU0_R31[18]** | A2 | I | CP[0] | A | |
| AHCLKX / USB_REFCLKIN / $\overline{\text{UART1_CTS}}$ / GP0[10] / **PRU0_R31[17]** | A3 | I | CP[0] | A | |
| AMUTE / PRU0_R30[16] / $\overline{\text{UART2_RTS}}$ / GP0[9] / **PRU0_R31[16]** | D5 | I | CP[0] | A | |
| VP_DIN[15]_VSYNC / UHPI_HD[7] / UPP_D[7] / PRU0_R30[15] / **PRU0_R31[15]** | V18 | I | CP[27] | C | |
| VP_DIN[14]_HSYNC / UHPI_HD[6] / UPP_D[6] / PRU0_R30[14] / **PRU0_R31[14]** | V19 | I | CP[27] | C | |
| VP_DIN[13]_FIELD / UHPI_HD[5] / UPP_D[5] / PRU0_R30[13] / **PRU0_R31[13]** | U19 | I | CP[27] | C | |
| VP_DIN[12] / UHPI_HD[4] / UPP_D[4] / PRU0_R30[12] / **PRU0_R31[12]** | T16 | I | CP[27] | C | |
| VP_DIN[11] / UHPI_HD[3] / UPP_D[3] / PRU0_R30[11] / **PRU0_R31[11]** | R18 | I | CP[27] | C | |
| VP_DIN[10] / UHPI_HD[4] / UPP_D[4] / PRU0_R30[10] / **PRU0_R31[10]** | R19 | I | CP[27] | C | |
| VP_DIN[9] / UHPI_HD[1] / UPP_D[1] / PRU0_R30[9] / **PRU0_R31[9]** | R15 | I | CP[27] | C | |
| AXR8 / CLKS1 / ECAP1_APWM1 / GP0[0] / **PRU0_R31[8]** | E4 | I | CP[3] | A | |
| AXR7 / EPWM1TZ[0] / PRU0_R30[17] / GP1[15] / **PRU0_R31[7]** | D2 | I | CP[4] | A | |
| AXR6 / CLKR0 / GP1[14] / MII_TXEN / **PRU0_R31[6]** | C1 | I | CP[5] | A | |
| EMA_CLK / PRU0_R30[5] / GP2[7] / **PRU0_R31[5]** | B7 | I | CP[16] | B | |
| EMA_SDCKE / PRU0_R30[4] / GP2[6] / **PRU0_R31[4]** | D8 | I | CP[16] | B | |
| $\overline{\text{EMA_RAS}}$ / PRU0_R30[3] / GP2[5] / **PRU0_R31[3]** | A16 | I | CP[16] | B | |
| $\overline{\text{EMA_CAS}}$ / PRU0_R30[2] / GP2[4] / **PRU0_R31[2]** | A9 | I | CP[16] | B | |
| EMA_WAIT[1] / PRU0_R30[1] / GP2[1] / **PRU0_R31[1]** | B19 | I | CP[16] | B | |
| EMA_WAIT[0] / PRU0_R30[0] / GP3[8] / **PRU0_R31[0]** | B18 | I | CP[16] | B | |

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**Table 2-12. Programmable Real-Time Unit (PRU) Terminal Functions (continued)**

| SIGNAL | | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| MMCSD0_CLK / **PRU1_R30[31]** /GP4[7] | E9 | O | CP[18] | B | PRU1 Output Signals |
| EMA_A[22] / MMCSD0_CMD / **PRU1_R30[30]** / GP4[6] | A10 | O | CP[18] | B | |
| EMA_A[21] / MMCSD0_DAT[0] / **PRU1_R30[29]** / GP4[5] | B10 | O | CP[18] | B | |
| EMA_A[20] / MMCSD0_DAT[1] / **PRU1_R30[28]** / GP4[4] | A11 | O | CP[18] | B | |
| EMA_A[19] / MMCSD0_DAT[2] / **PRU1_R30[27]** / GP4[3] | C10 | O | CP[18] | B | |
| EMA_A[18] / MMCSD0_DAT[3] / **PRU1_R30[26]** / GP4[2] | E11 | O | CP[18] | B | |
| EMA_A[17] / MMCSD0_DAT[4] / **PRU1_R30[25]** / GP4[1] | B11 | O | CP[18] | B | |
| EMA_A[16] / MMCSD0_DAT[5] / **PRU1_R30[24]** / GP4[0] | E12 | O | CP[18] | B | |
| EMA_A[15] / MMCSD0_DAT[6] / **PRU1_R30[23]** / GP5[15] / PRU1_R31[23] | C11 | O | CP[19] | B | |
| EMA_A[14] / MMCSD0_DAT[7] / **PRU1_R30[22]** / GP5[14] / PRU1_R31[22] | A12 | O | CP[19] | B | |
| EMA_A[13] / PRU0_R30[21] / **PRU1_R30[21]** / GP5[13] / PRU1_R31[21] | D11 | O | CP[19] | B | |
| EMA_A[12] / **PRU1_R30[20]** / GP5[12] / PRU1_R31[20] | D13 | O | CP[19] | B | |
| EMA_A[11] / **PRU1_R30[19]** / GP5[11] / PRU1_R31[19] | B12 | O | CP[19] | B | |
| EMA_A[10] / **PRU1_R30[18]** / GP5[10] / PRU1_R31[18] | C12 | O | CP[19] | B | |
| EMA_A[9] / **PRU1_R30[17]** / GP5[9] | D12 | O | CP[19] | B | |
| EMA_A[8] / **PRU1_R30[16]** / GP5[8] | A13 | O | CP[19] | B | |
| EMA_A[7] / **PRU1_R30[15]** / GP5[7] | B13 | O | CP[20] | B | |
| $\overline{\text{RESETOUT}}$ / $\overline{\text{UHPI_HAS}}$ / **PRU1_R30[14]** / GP6[15] | T17 | O | CP[21] | C | |
| CLKOUT / $\overline{\text{UHPI_HDS2}}$ / **PRU1_R30[13]** / GP6[14] | T18 | O | CP[22] | C | |
| PRU0_R30[31] / $\overline{\text{UHPI_HRDY}}$ / **PRU1_R30[12]** / GP6[13] | R17 | O | CP[23] | C | |
| PRU0_R30[30] / $\overline{\text{UHPI_HINT}}$ / **PRU1_R30[11]** / GP6[12] | R16 | O | CP[23] | C | |
| VP_CLKIN0 / $\overline{\text{UHPI_HCS}}$ / **PRU1_R30[10]** / GP6[7] / UPP_2xTXCLK | W14 | O | CP[25] | C | |
| VP_CLKIN1 / $\overline{\text{UHPI_HDS1}}$ / **PRU1_R30[9]** / GP6[6] / PRU1_R31[16] | V15 | O | CP[25] | C | |
| PRU0_R30[22] / **PRU1_R30[8]** / UPP_CHB_WAIT / GP8[12] / PRU1_R31[24] | G3 | O | CP[30] | C | |
| MMCSD1_DAT[7] / LCD_PCLK / **PRU1_R30[7]** / GP8[11] | F1 | O | CP[31] | C | |
| MMCSD1_DAT[6] / LCD_MCLK / **PRU1_R30[6]** / GP8[10] / PRU1_R31[7] | F2 | O | CP[31] | C | |
| MMCSD1_DAT[5] / LCD_HSYNC / **PRU1_R30[5]** / GP8[9] / PRU1_R31[6] | H4 | O | CP[31] | C | |
| MMCSD1_DAT[4] / LCD_VSYNC / **PRU1_R30[4]** / GP8[8] / PRU1_R31[5] | G4 | O | CP[31] | C | |
| VP_CLKIN2 / MMCSD1_DAT[3] / **PRU1_R30[3]** / GP6[4] / PRU1_R31[4] | H3 | O | CP[30] | C | |
| VP_CLKOUT2 / MMCSD1_DAT[2] / **PRU1_R30[2]** / GP6[3] / PRU1_R31[3] | K3 | O | CP[30] | C | |
| VP_CLKIN3 / MMCSD1_DAT[1] / **PRU1_R30[1]** / GP6[2] / PRU1_R31[2] | J3 | O | CP[30] | C | |
| VP_CLKOUT3 / **PRU1_R30[0]** / GP6[1] / PRU1_R31[1] | K4 | O | CP[30] | C | |


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**Table 2-12. Programmable Real-Time Unit (PRU) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| VP_DIN[0] / UHPI_HD[8] / UPP_D[8] / RMII_CRS_DV / **PRU1_R31[29]** | W19 | I | CP[26] | C | PRU1 Input Signals |
| $\overline{\text{LCD_AC_ENB_CS}}$ / GP6[0] / **PRU1_R31[28]** | R5 | I | CP[31] | C | |
| PRU0_R30[25] / MMCSD1_DAT[0] / UPP_CHB_CLOCK / GP8[15] / **PRU1_R31[27]** | G1 | I | CP[30] | C | |
| PRU0_R30[24] / MMCSD1_CLK / UPP_CHB_START / GP8[14] / **PRU1_R31[26]** | G2 | I | CP[30] | C | |
| PRU0_R30[23] / MMCSD1_CMD / UPP_CHB_ENABLE / GP8[13] / **PRU1_R31[25]** | J4 | I | CP[30] | C | |
| PRU0_R30[22] / PRU1_R30[8] / UPP_CHB_WAIT / GP8[12] / **PRU1_R31[24]** | G3 | I | CP[30] | C | |
| MMCSD0_CLK / PRU1_R30[31] /GP4[7] | E9 | I | CP[18] | B | |
| EMA_A[22] / MMCSD0_CMD / PRU1_R30[30] / GP4[6] | A10 | I | CP[18] | B | |
| EMA_A[21] / MMCSD0_DAT[0] / PRU1_R30[29] / GP4[5] | B10 | I | CP[18] | B | |
| EMA_A[20] / MMCSD0_DAT[1] / PRU1_R30[28] / GP4[4] | A11 | I | CP[18] | B | |
| EMA_A[19] / MMCSD0_DAT[2] / PRU1_R30[27] / GP4[3] | C10 | I | CP[18] | B | |
| EMA_A[18] / MMCSD0_DAT[3] / PRU1_R30[26] / GP4[2] | E11 | I | CP[18] | B | |
| PRU0_R30[26] / UHPI_HR$\overline{\text{W}}$ / UPP_CHA_WAIT / GP6[8] / **PRU1_R31[17]** | T15 | I | CP[24] | C | |
| VP_CLKIN1 / $\overline{\text{UHPI_HDS1}}$ / PRU1_R30[9] / GP6[6] / **PRU1_R31[16]** | V15 | I | CP[25] | C | |
| VP_DOUT[7] / LCD_D[7] / UPP_XD[15] / GP7[15] / **PRU1_R31[15]** | U2 | I | CP[28] | C | |
| VP_DOUT[6] / LCD_D[6] / UPP_XD[14] / GP7[14] / **PRU1_R31[14]** | U1 | I | CP[28] | C | |
| VP_DOUT[5] / LCD_D[5] / UPP_XD[13] / GP7[13] / **PRU1_R31[13]** | V3 | I | CP[28] | C | |
| VP_DOUT[4] / LCD_D[4] / UPP_XD[12] / GP7[12] / **PRU1_R31[12]** | V2 | I | CP[28] | C | |
| VP_DOUT[3] / LCD_D[3] / UPP_XD[11] / GP7[11] / **PRU1_R31[11]** | V1 | I | CP[28] | C | |
| VP_DOUT[2] / LCD_D[2] / UPP_XD[10] / GP7[10] / **PRU1_R31[10]** | W3 | I | CP[28] | C | |
| VP_DOUT[1] / LCD_D[1] / UPP_XD[9] / GP7[9] / **PRU1_R31[9]** | W2 | I | CP[28] | C | |
| VP_DOUT[0] / LCD_D[0] / UPP_XD[8] / GP7[8] / **PRU1_R31[8]** | W1 | I | CP[28] | C | |
| MMCSD1_DAT[6] / LCD_MCLK / PRU1_R30[6] / GP8[10] / **PRU1_R31[7]** | F2 | I | CP[31] | C | |
| MMCSD1_DAT[5] / LCD_HSYNC / PRU1_R30[5] / GP8[9] / **PRU1_R31[6]** | H4 | I | CP[31] | C | |
| MMCSD1_DAT[4] / LCD_VSYNC / PRU1_R30[4] / GP8[8] / **PRU1_R31[5]** | G4 | I | CP[31] | C | |
| VP_CLKIN2 / MMCSD1_DAT[3] / PRU1_R30[3] / GP6[4] / **PRU1_R31[4]** | H3 | I | CP[30] | C | |
| VP_CLKOUT2 / MMCSD1_DAT[2] / PRU1_R30[2] / GP6[3] / **PRU1_R31[3]** | K3 | I | CP[30] | C | |
| VP_CLKIN3 / MMCSD1_DAT[1] / PRU1_R30[1] / GP6[2] / **PRU1_R31[2]** | J3 | I | CP[30] | C | |
| VP_CLKOUT3 / PRU1_R30[0] / GP6[1] / **PRU1_R31[1]** | K4 | I | CP[30] | C | |
| VP_DIN[8] / UHPI_HD[0] / UPP_D[0] / GP6[5] / **PRU1_R31[0]** | P17 | I | CP[27] | C | |

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### 2.8.9 Enhanced Capture/Auxiliary PWM Modules (eCAP0)

The eCAP Module pins function as either input captures or auxiliary PWM 32-bit outputs, depending upon how the eCAP module is programmed.

**Table 2-13. Enhanced Capture Module (eCAP) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **eCAP0** | | | | | |
| AXR0 / **ECAP0_APWM0** / GP8[7] / MII_TXD[0] / CLKS0 | F3 | I/O | CP[6] | A | enhanced capture 0 input or auxiliary PWM 0 output |
| **eCAP1** | | | | | |
| AXR8 / CLKS1 / **ECAP1_APWM1** / GP0[0] / PRU0_R31[8] | E4 | I/O | CP[3] | A | enhanced capture 1 input or auxiliary PWM 1 output |
| **eCAP2** | | | | | |
| AXR15 / EPWM0TZ[0] / **ECAP2_APWM2** / GP0[7] | A4 | I/O | CP[1] | A | enhanced capture 2 input or auxiliary PWM 2 output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.10 Enhanced Pulse Width Modulators (eHRPWM)

**Table 2-14. Enhanced Pulse Width Modulator (eHRPWM) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **eHRPWM0** | | | | | |
| SPI0_CLK / **EPWM0A** / GP1[8] / MII_RXCLK | D19 | I/O | CP[7] | A | eHRPWM0 A output (with high-resolution) |
| $\overline{\text{SPI0_ENA}}$ / **EPWM0B** / PRU0_R30[6] / MII_RXDV | C17 | I/O | CP[7] | A | eHRPWM0 B output |
| AXR15 / **EPWM0TZ[0]** / ECAP2_APWM2 / GP0[7] | A4 | I | CP[1] | A | eHRPWM0 trip zone input |
| SPI0_SOMI / **EPWMSYNCI** / GP8[6] / MII_RXER | C16 | I | CP[7] | A | eHRPWM0 sync input |
| SPI0_SIMO / **EPWMSYNCO** / GP8[5] / MII_CRS | C18 | I/O | CP[7] | A | eHRPWM0 sync output |
| **eHRPWM1** | | | | | |
| $\overline{\text{SPI1_SCS[1]}}$ / **EPWM1A** / PRU0_R30[8] / GP2[15] / TM64P2_IN12 | F18 | I/O | CP[14] | A | eHRPWM1 A output (with high-resolution) |
| $\overline{\text{SPI1_SCS[0]}}$ / **EPWM1B** / PRU0_R30[7] / GP2[14] / TM64P3_IN12 | E19 | I/O | CP[14] | A | eHRPWM1 B output |
| AXR7 / **EPWM1TZ[0]** / PRU0_R30[17] / GP1[15] / PRU0_R31[7] | D2 | I | CP[4] | A | eHRPWM1 trip zone input |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 2.8.11 Boot

**Table 2-15. Boot Mode Selection Terminal Functions(1)**

| SIGNAL | | TYPE(2) | PULL(3) | POWER GROUP(4) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| VP_DOUT[15] / LCD_D[15] / UPP_XD[7] / GP7[7] / **BOOT[7]** | P4 | I | CP[29] | C | Boot Mode Selection Pins |
| VP_DOUT[14] / LCD_D[14] / UPP_XD[6] / GP7[6] / **BOOT[6]** | R3 | I | CP[29] | C | |
| VP_DOUT[13] / LCD_D[13] / UPP_XD[5] / GP7[5] / **BOOT[5]** | R2 | I | CP[29] | C | |
| VP_DOUT[12] / LCD_D[12] / UPP_XD[4] / GP7[4] / **BOOT[4]** | R1 | I | CP[29] | C | |
| VP_DOUT[11] / LCD_D[11] / UPP_XD[3] / GP7[3] / **BOOT[3]** | T3 | I | CP[29] | C | |
| VP_DOUT[10] / LCD_D[10] / UPP_XD[2] / GP7[2] / **BOOT[2]** | T2 | I | CP[29] | C | |
| VP_DOUT[9] / LCD_D[9] / UPP_XD[1] / GP7[1] / **BOOT[1]** | T1 | I | CP[29] | C | |
| VP_DOUT[8] / LCD_D[8] / UPP_XD[0] / GP7[0] / **BOOT[0]** | U3 | I | CP[29] | C | |

(1) Boot decoding is defined in the bootloader application report.
(2) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.
(3) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.
(4) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.12 Universal Asynchronous Receiver/Transmitters (UART0, UART1, UART2)

**Table 2-16. Universal Asynchronous Receiver/Transmitter (UART) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **UART0** | | | | | |
| SPI0_SCS[5] / **UART0_RXD** / GP8[4] / MII_RXD[3] | C19 | I | CP[8] | A | UART0 receive data |
| SPI0_SCS[4] / **UART0_TXD** / GP8[3] / MII_RXD[2] | D18 | O | CP[8] | A | UART0 transmit data |
| SPI0_SCS[2] / **UART0_RTS** / GP8[1] / MII_RXD[0] / SATA_CP_DET | D16 | O | CP[9] | A | UART0 ready-to-send output |
| SPI0_SCS[3] / **UART0_CTS** / GP8[2] / MII_RXD[1] / SATA_MP_SWITCH | E17 | I | CP[9] | A | UART0 clear-to-send input |
| **UART1** | | | | | |
| SPI1_SCS[3] / **UART1_RXD** / SATA_LED / GP1[1] | E18 | I | CP[13] | A | UART1 receive data |
| SPI1_SCS[2] / **UART1_TXD** / SATA_CP_POD / GP1[0] | F19 | O | CP[13] | A | UART1 transmit data |
| AHCLKR / PRU0_R30[18] / **UART1_RTS** /GP0[11] / PRU0_R31[18] | A2 | O | CP[0] | A | UART1 ready-to-send output |
| AHCLKX / USB_REFCLKIN / **UART1_CTS** / GP0[10] / PRU0_R31[17] | A3 | I | CP[0] | A | UART1 clear-to-send input |
| **UART2** | | | | | |
| SPI1_SCS[5] / **UART2_RXD** / I2C1_SCL /GP1[3] | F17 | I | CP[12] | A | UART2 receive data |
| SPI1_SCS[4] / **UART2_TXD** / I2C1_SDA /GP1[2] | F16 | O | CP[12] | A | UART2 transmit data |
| AMUTE / PRU0_R30[16] / **UART2_RTS** / GP0[9] / PRU0_R31[16] | D5 | O | CP[0] | A | UART2 ready-to-send output |
| RTC_ALARM / **UART2_CTS** / GP0[8] / DEEPSLEEP | F4 | I | CP[0] | A | UART2 clear-to-send input |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 2.8.13 Inter-Integrated Circuit Modules(I2C0, I2C1)

**Table 2-17. Inter-Integrated Circuit (I2C) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **I2C0** | | | | | |
| SPI1_SCS[6] / **I2C0_SDA** / TM64P3_OUT12 / GP1[4] | G18 | I/O | CP[11] | A | I2C0 serial data |
| SPI1_SCS[7] / **I2C0_SCL** / TM64P2_OUT12 / GP1[5] | G16 | I/O | CP[11] | A | I2C0 serial clock |
| **I2C1** | | | | | |
| SPI1_SCS[4] / UART2_TXD / **I2C1_SDA** / GP1[2] | F16 | I/O | CP[12] | A | I2C1 serial data |
| SPI1_SCS[5] / UART2_RXD / **I2C1_SCL** / GP1[3] | F17 | I/O | CP[12] | A | I2C1 serial clock |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module.The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.14 Timers

**Table 2-18. Timers Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **TIMER0** | | | | | |
| $\overline{\text{SPI0_SCS[1]}}$ / TM64P0_OUT12 / GP1[7] / MDIO_CLK /**TM64P0_IN12** | E16 | I | CP[10] | A | Timer0 lower input |
| $\overline{\text{SPI0_SCS[1]}}$ / **TM64P0_OUT12** / GP1[7] / MDIO_CLK / TM64P0_IN12 | E16 | O | CP[10] | A | Timer0 lower output |
| **TIMER1 (Watchdog)** | | | | | |
| $\overline{\text{SPI0_SCS[0]}}$ / TM64P1_OUT12 / GP1[6] / MDIO_D / **TM64P1_IN12** | D17 | I | CP[10] | A | Timer1 lower input |
| $\overline{\text{SPI0_SCS[0]}}$ / **TM64P1_OUT12** / GP1[6] / MDIO_D / TM64P1_IN12 | D17 | O | CP[10] | A | Timer1 lower output |
| **TIMER2** | | | | | |
| $\overline{\text{SPI1_SCS[1]}}$ / EPWM1A / PRU0_R30[8] / GP2[15] / **TM64P2_IN12** | F18 | I | CP[14] | A | Timer2 lower input |
| $\overline{\text{SPI1_SCS[7]}}$ / I2C0_SCL / **TM64P2_OUT12** / GP1[5] | G16 | O | CP[11] | A | Timer2 lower output |
| **TIMER3** | | | | | |
| $\overline{\text{SPI1_SCS[0]}}$ / EPWM1B / PRU0_R30[7] / GP2[14] / **TM64P3_IN12** | E19 | I | CP[14] | A | Timer3 lower input |
| $\overline{\text{SPI1_SCS[6]}}$ / I2C0_SDA / **TM64P3_OUT12** / GP1[4] | G18 | O | CP[11] | A | Timer3 lower output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 2.8.15 Multichannel Audio Serial Ports (McASP)

**Table 2-19. Multichannel Audio Serial Ports Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **McASP0** | | | | | |
| **AXR15** / EPWM0TZ[0] / ECAP2_APWM2 / GP0[7] | A4 | I/O | CP[1] | A | McASP0 serial data |
| **AXR14** / CLKR1 / GP0[6] | B4 | I/O | CP[2] | A | |
| **AXR13** / CLKX1 / GP0[5] | B3 | I/O | CP[2] | A | |
| **AXR12** / FSR1 / GP0[4] | C4 | I/O | CP[2] | A | |
| **AXR11** / FSX1 / GP0[3] | C5 | I/O | CP[2] | A | |
| **AXR10** / DR1 / GP0[2] | D4 | I/O | CP[2] | A | |
| **AXR9** / DX1 / GP0[1] | C3 | I/O | CP[2] | A | |
| **AXR8** / CLKS1 / ECAP1_APWM1 / GP0[0] / PRU0_R31[8] | E4 | I/O | CP[3] | A | |
| **AXR7** / EPWM1TZ[0] / PRU0_R30[17] / GP1[15] / PRU0_R31[7] | D2 | I/O | CP[4] | A | |
| **AXR6** / CLKR0 / GP1[14] / MII_TXEN / PRU0_R31[6] | C1 | I/O | CP[5] | A | |
| **AXR5** / CLKX0 / GP1[13] / MII_TXCLK | D3 | I/O | CP[5] | A | |
| **AXR4** / FSR0 / GP1[12] / MII_COL | D1 | I/O | CP[5] | A | |
| **AXR3** / FSX0 / GP1[11] / MII_TXD[3] | E3 | I/O | CP[5] | A | |
| **AXR2** / DR0 / GP1[10] / MII_TXD[2] | E2 | I/O | CP[5] | A | |
| **AXR1** / DX0 / GP1[9] / MII_TXD[1] | E1 | I/O | CP[5] | A | |
| **AXR0** / ECAP0_APWM0 / GP8[7]/ MII_TXD[0] / CLKS0 | F3 | I/O | CP[6] | A | |
| **AHCLKX** / USB_REFCLKIN / $\overline{\text{UART1_CTS}}$ / GP0[10] / PRU0_R31[17] | A3 | I/O | CP[0] | A | McASP0 transmit master clock |
| **ACLKX** / PRU0_R30[19] / GP0[14] / PRU0_R31[21] | B1 | I/O | CP[0] | A | McASP0 transmit bit clock |
| **AFSX** / GP0[12] / PRU0_R31[19] | B2 | I/O | CP[0] | A | McASP0 transmit frame sync |
| **AHCLKR** / PRU0_R30[18] / $\overline{\text{UART1_RTS}}$ / GP0[11] / PRU0_R31[18] | A2 | I/O | CP[0] | A | McASP0 receive master clock |
| **ACLKR** / PRU0_R30[20] / GP0[15] / PRU0_R31[22] | A1 | I/O | CP[0] | A | McASP0 receive bit clock |
| **AFSR** / GP0[13] / PRU0_R31[20] | C2 | I/O | CP[0] | A | McASP0 receive frame sync |
| **AMUTE** / PRU0_R30[16] / $\overline{\text{UART2_RTS}}$ / GP0[9] / PRU0_R31[16] | D5 | I/O | CP[0] | A | McASP0 mute output |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.16 Multichannel Buffered Serial Ports (McBSP)

**Table 2-20. Multichannel Buffered Serial Ports (McBSPs) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **McBSP0** | | | | | |
| AXR0 / ECAP0_APWM0 / GP8[7] / MII_TXD[0] / **CLKS0** | F3 | I | CP[6] | A | McBSP0 sample rate generator clock input |
| AXR6 / **CLKR0** / GP1[14] / MII_TXEN / PRU0_R31[6] | C1 | I/O | CP[5] | A | McBSP0 receive clock |
| AXR4 / **FSR0** / GP1[12] / MII_COL | D1 | I/O | CP[5] | A | McBSP0 receive frame sync |
| AXR2 / **DR0** / GP1[10] / MII_TXD[2] | E2 | I | CP[5] | A | McBSP0 receive data |
| AXR5 / **CLKX0** / GP1[13] / MII_TXCLK | D3 | I/O | CP[5] | A | McBSP0 transmit clock |
| AXR3 / **FSX0** / GP1[11] / MII_TXD[3] | E3 | I/O | CP[5] | A | McBSP0 transmit frame sync |
| AXR1 / **DX0** / GP1[9] / MII_TXD[1] | E1 | O | CP[5] | A | McBSP0 transmit data |
| **McBSP1** | | | | | |
| AXR8 / **CLKS1** / ECAP1_APWM1 / GP0[0] / PRU0_R31[8] | E4 | I | CP[3] | A | McBSP1 sample rate generator clock input |
| AXR14 / **CLKR1** / GP0[6] | B4 | I/O | CP[2] | A | McBSP1 receive clock |
| AXR12 / **FSR1** / GP0[4] | C4 | I/O | CP[2] | A | McBSP1 receive frame sync |
| AXR10 / **DR1** / GP0[2] | D4 | I | CP[2] | A | McBSP1 receive data |
| AXR13 / **CLKX1** / GP0[5] | B3 | I/O | CP[2] | A | McBSP1 transmit clock |
| AXR11 / **FSX1** / GP0[3] | C5 | I/O | CP[2] | A | McBSP1 transmit frame sync |
| AXR9 / **DX1** / GP0[1] | C3 | O | CP[2] | A | McBSP1 transmit data |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 2.8.17 Universal Serial Bus Modules (USB0, USB1)

**Table 2-21. Universal Serial Bus (USB) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **USB0 2.0 OTG (USB0)** | | | | | |
| **USB0_DM** | M18 | A | IPD | — | USB0 PHY data minus |
| **USB0_DP** | M19 | A | IPD | — | USB0 PHY data plus |
| **USB0_VDDA33** | N18 | PWR | — | — | USB0 PHY 3.3-V supply |
| **USB0_ID** | P16 | A | — | — | USB0 PHY identification (mini-A or mini-B plug) |
| **USB0_VBUS** | N19 | A | — | — | USB0 bus voltage |
| **USB0_DRVVBUS** | K18 | 0 | IPD | B | USB0 controller VBUS control output. |
| AHCLKX / **USB_REFCLKIN** / $\overline{\text{UART1_CTS}}$ / GP0[10] / PRU0_R31[17] | A3 | I | CP[0] | A | USB_REFCLKIN. Optional clock input |
| **USB0_VDDA18** | N14 | PWR | — | — | USB0 PHY 1.8-V supply input |
| **USB0_VDDA12** | N17 | A | — | — | USB0 PHY 1.2-V LDO output for bypass cap |
| **USB_CVDD** | M12 | PWR | — | — | USB0 and USB1 core logic 1.2-V supply input |
| **USB1 1.1 OHCI (USB1)** | | | | | |
| **USB1_DM** I | P18 | A | — | — | USB1 PHY data minus |
| **USB1_DP** | P19 | A | — | — | USB1 PHY data plus |
| AHCLKX / **USB_REFCLKIN** / $\overline{\text{UART1_CTS}}$ / GP0[10] / PRU0_R31[17] | A3 | I | CP[0] | A | USB_REFCLKIN. Optional clock input |
| **USB1_VDDA33** | P15 | PWR | — | — | USB1 PHY 3.3-V supply |
| **USB1_VDDA18** | P14 | PWR | — | — | USB1 PHY 1.8-V supply |
| **USB_CVDD** | M12 | PWR | — | — | USB0 and USB1 core logic 1.2-V supply input |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.18 Ethernet Media Access Controller (EMAC)

**Table 2-22. Ethernet Media Access Controller (EMAC) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **MII** | | | | | |
| AXR6 / CLKR0 / GP1[14] / **MII_TXEN** / PRU0_R31[6] | C1 | O | CP[5] | A | EMAC MII Transmit enable output |
| AXR5 / CLKX0 / GP1[13] / **MII_TXCLK** | D3 | I | CP[5] | A | EMAC MII Transmit clock input |
| AXR4 / FSR0 / GP1[12] / **MII_COL** | D1 | I | CP[5] | A | EMAC MII Collision detect input |
| AXR3 / FSX0 / GP1[11] / **MII_TXD[3]** | E3 | O | CP[5] | A | EMAC MII transmit data |
| AXR2 / DR0 / GP1[10] / **MII_TXD[2]** | E2 | O | CP[5] | A | |
| AXR1 / DX0 / GP1[9] / **MII_TXD[1]** | E1 | O | CP[5] | A | |
| AXR0 / ECAP0_APWM0 / GP8[7] / **MII_TXD[0]** / CLKS0 | F3 | O | CP[6] | A | |
| SPI0_SOMI / EPWMSYNCI / GP8[6] / **MII_RXER** | C16 | I | CP[7] | A | EMAC MII receive error input |
| SPI0_SIMO / EPWMSYNCO / GP8[5] / **MII_CRS** | C18 | I | CP[7] | A | EMAC MII carrier sense input |
| SPI0_CLK / EPWM0A / GP1[8] / **MII_RXCLK** | D19 | I | CP[7] | A | EMAC MII receive clock input |
| $\overline{\text{SPI0_ENA}}$ / EPWM0B / PRU0_R30[6] / **MII_RXDV** | C17 | I | CP[7] | A | EMAC MII receive data valid input |
| $\overline{\text{SPI0_SCS[5]}}$ /UART0_RXD / GP8[4] / **MII_RXD[3]** | C19 | I | CP[8] | A | EMAC MII receive data |
| $\overline{\text{SPI0_SCS[4]}}$ /UART0_TXD / GP8[3] / **MII_RXD[2]** | D18 | I | CP[8] | A | |
| $\overline{\text{SPI0_SCS[3]}}$ / $\overline{\text{UART0_CTS}}$ / GP8[2] / **MII_RXD[1]** / SATA_MP_SWITCH | E17 | I | CP[9] | A | |
| $\overline{\text{SPI0_SCS[2]}}$ / $\overline{\text{UART0_RTS}}$ / GP8[1] / **MII_RXD[0]** / SATA_CP_DET | D16 | I | CP[9] | A | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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**Table 2-22. Ethernet Media Access Controller (EMAC) Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **RMII** | | | | | |
| VP_DIN[1] / UHPI_HD[9] / UPP_D[9] / **RMII_MHZ_50_CLK** / PRU0_R31[23] | W18 | I/O | CP[26] | C | EMAC 50-MHz clock input or output |
| VP_DIN[2] / UHPI_HD[10] / UPP_D[10] / **RMII_RXER** / PRU0_R31[24] | W17 | I | CP[26] | C | EMAC RMII receiver error |
| VP_DIN[3] / UHPI_HD[11] / UPP_D[11] / **RMII_RXD[0]** / PRU0_R31[25] | V17 | I | CP[26] | C | EMAC RMII receive data |
| VP_DIN[4] / UHPI_HD[12] / UPP_D[12] / **RMII_RXD[1]** /PRU0_R31[26] | W16 | I | CP[26] | C | |
| VP_DIN[0] / UHPI_HD[8] / UPP_D[8] / **RMII_CRS_DV** / PRU1_R31[29] | W19 | I | CP[26] | C | EMAC RMII carrier sense data valid |
| VP_DIN[5] / UHPI_HD[13] / UPP_D[13] / **RMII_TXEN** / PRU0_R31[27] | R14 | O | CP[26] | C | EMAC RMII transmit enable |
| VP_DIN[6] / UHPI_HD[14] / UPP_D[14] / **RMII_TXD[0]** / PRU0_R31[28] | V16 | O | CP[26] | C | EMAC RMII transmit data |
| VP_DIN[7] / UHPI_HD[15] / UPP_D[15] / **RMII_TXD[1]** / PRU0_R31[29] | U18 | O | CP[26] | C | |
| **MDIO** | | | | | |
| $\overline{\text{SPI0_SCS[0]}}$ / TM64P1_OUT12 / GP1[6] / **MDIO_D** / TM64P1_IN12 | D17 | I/O | CP[10] | A | MDIO serial data |
| $\overline{\text{SPI0_SCS[1]}}$ / TM64P0_OUT12 / GP1[7] / **MDIO_CLK** / TM64P0_IN12 | E16 | O | CP[10] | A | MDIO clock |


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### 2.8.19 Multimedia Card/Secure Digital (MMC/SD)

**Table 2-23. Multimedia Card/Secure Digital (MMC/SD) Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **MMCSD0** | | | | | |
| **MMCSD0_CLK** / PRU1_R30[31] /GP4[7] | E9 | O | CP[18] | B | MMCSD0 Clock |
| EMA_A[22] / **MMCSD0_CMD** / PRU1_R30[30] / GP4[6] | A10 | I/O | CP[18] | B | MMCSD0 Command |
| EMA_A[14] / **MMCSD0_DAT[7]** / PRU1_R30[22] / GP5[14] / PRU1_R31[22] | A12 | I/O | CP[19] | B | MMC/SD0 data |
| EMA_A[15] / **MMCSD0_DAT[6]** / PRU1_R30[23] / GP5[15] / PRU1_R31[23] | C11 | I/O | CP[19] | B | |
| EMA_A[16] / **MMCSD0_DAT[5]** / PRU1_R30[24] / GP4[0] | E12 | I/O | CP[18] | B | |
| EMA_A[17] / **MMCSD0_DAT[4]** / PRU1_R30[25] / GP4[1] | B11 | I/O | CP[18] | B | |
| EMA_A[18] / **MMCSD0_DAT[3]** / PRU1_R30[26] / GP4[2] | E11 | I/O | CP[18] | B | |
| EMA_A[19] / **MMCSD0_DAT[2]** / PRU1_R30[27] / GP4[3] | C10 | I/O | CP[18] | B | |
| EMA_A[20] / **MMCSD0_DAT[1]** / PRU1_R30[28] / GP4[4] | A11 | I/O | CP[18] | B | |
| EMA_A[21] / **MMCSD0_DAT[0]** / PRU1_R30[29] / GP4[5] | B10 | I/O | CP[18] | B | |
| **MMCSD1** | | | | | |
| PRU0_R30[24] / **MMCSD1_CLK** / UPP_CHB_START / GP8[14] / PRU1_R31[26]/ | G2 | O | CP[30] | C | MMCSD1 Clock |
| PRU0_R30[23] / **MMCSD1_CMD** / UPP_CHB_ENABLE / GP8[13] / PRU1_R31[25] | J4 | I/O | CP[30] | C | MMCSD1 Command |
| **MMCSD1_DAT[7]** / LCD_PCLK / PRU1_R30[7] / GP8[11] | F1 | I/O | CP[31] | C | MMC/SD1 data |
| **MMCSD1_DAT[6]** / LCD_MCLK / PRU1_R30[6] / GP8[10] / PRU1_R31[7] | F2 | I/O | CP[31] | C | |
| **MMCSD1_DAT[5]** / LCD_HSYNC / PRU1_R30[5] / GP8[9] / PRU1_R31[6] | H4 | I/O | CP[31] | C | |
| **MMCSD1_DAT[4]** / LCD_VSYNC / PRU1_R30[4] / GP8[8] / PRU1_R31[5] | G4 | I/O | CP[31] | C | |
| VP_CLKIN2 / **MMCSD1_DAT[3]** / PRU1_R30[3] / GP6[4] / PRU1_R31[4] | H3 | I/O | CP[30] | C | |
| VP_CLKOUT2 / **MMCSD1_DAT[2]** / PRU1_R30[2] / GP6[3] / PRU1_R31[3] | K3 | I/O | CP[30] | C | |
| VP_CLKIN3 / **MMCSD1_DAT[1]**/ PRU1_R30[1] / GP6[2] / PRU1_R31[2] | J3 | I/O | CP[30] | C | |
| PRU0_R30[25] / **MMCSD1_DAT[0]** / UPP_CHB_CLOCK / GP8[15]/ PRU1_R31[27] | G1 | I/O | CP[30] | C | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 2.8.20 Liquid Crystal Display Controller(LCD)

**Table 2-24. Liquid Crystal Display Controller (LCD) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| VP_DOUT[15] / **LCD_D[15]** / UPP_XD[7] / GP7[7] / BOOT[7] | P4 | I/O | CP[29] | C | LCD data bus |
| VP_DOUT[14] / **LCD_D[14]** / UPP_XD[6] / GP7[6] / BOOT[6] | R3 | I/O | CP[29] | C | |
| VP_DOUT[13] / **LCD_D[13]** / UPP_XD[5] / GP7[5] / BOOT[5] | R2 | I/O | CP[29] | C | |
| VP_DOUT[12] / **LCD_D[12]** / UPP_XD[4] / GP7[4] / BOOT[4] | R1 | I/O | CP[29] | C | |
| VP_DOUT[11] / **LCD_D[11]** / UPP_XD[3] / GP7[3] / BOOT[3] | T3 | I/O | CP[29] | C | |
| VP_DOUT[10] / **LCD_D[10]** / UPP_XD[2] / GP7[2] / BOOT[2] | T2 | I/O | CP[29] | C | |
| VP_DOUT[9] / **LCD_D[9]** / UPP_XD[1] / GP7[1] / BOOT[1] | T1 | I/O | CP[29] | C | |
| VP_DOUT[8] / **LCD_D[8]** / UPP_XD[0] / GP7[0] / BOOT[0] | U3 | I/O | CP[29] | C | |
| VP_DOUT[7] / **LCD_D[7]** / UPP_XD[15] / GP7[15] / PRU1_R31[15] | U2 | I/O | CP[28] | C | |
| VP_DOUT[6] / **LCD_D[6]** / UPP_XD[14] / GP7[14] / PRU1_R31[14] | U1 | I/O | CP[28] | C | |
| VP_DOUT[5] / **LCD_D[5]** / UPP_XD[13] / GP7[13] / PRU1_R31[13] | V3 | I/O | CP[28] | C | |
| VP_DOUT[4] / **LCD_D[4]** / UPP_XD[12] / GP7[12] / PRU1_R31[12] | V2 | I/O | CP[28] | C | |
| VP_DOUT[3] / **LCD_D[3]** / UPP_XD[11] / GP7[11] / PRU1_R31[11] | V1 | I/O | CP[28] | C | |
| VP_DOUT[2] / **LCD_D[2]** / UPP_XD[10] / GP7[10] / PRU1_R31[10] | W3 | I/O | CP[28] | C | |
| VP_DOUT[1] / **LCD_D[1]** / UPP_XD[9] / GP7[9] / PRU1_R31[9] | W2 | I/O | CP[28] | C | |
| VP_DOUT[0] / **LCD_D[0]** / UPP_XD[8] / GP7[8] / PRU1_R31[8] | W1 | I/O | CP[28] | C | |
| MMCSD1_DAT[7] / **LCD_PCLK** / PRU1_R30[7] / GP8[11] | F1 | O | CP[31] | C | LCD pixel clock |
| MMCSD1_DAT[5] / **LCD_HSYNC** / PRU1_R30[5] / GP8[9] / PRU1_R31[6] | H4 | O | CP[31] | C | LCD horizontal sync |
| MMCSD1_DAT[4] / **LCD_VSYNC** / PRU1_R30[4] / GP8[8] / PRU1_R31[5] | G4 | O | CP[31] | C | LCD vertical sync |
| **$\overline{\text{LCD_AC_ENB_CS}}$** / GP6[0]/ / PRU1_R31[28] | R5 | O | CP[31] | C | LCD AC bias enable chip select |
| MMCSD1_DAT[6] / **LCD_MCLK** / PRU1_R30[6] / GP8[10] / PRU1_R31[7] | F2 | O | CP[31] | C | LCD memory clock |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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### 2.8.21 Serial ATA Controller (SATA)

**Table 2-25. Serial ATA Controller (SATA) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| **SATA_RXP** | L1 | I | — | — | SATA receive data (positive) |
| **SATA_RXN** | L2 | I | — | — | SATA receive data (negative) |
| **SATA_TXP** | J1 | O | — | — | SATA transmit data (positive) |
| **SATA_TXN** | J2 | O | — | — | SATA transmit data (negative) |
| **SATA_REFCLKP** | N2 | I | — | — | SATA PHY reference clock (positive) |
| **SATA_REFCLKN** | N1 | I | — | — | SATA PHY reference clock (negative) |
| SPI0_SCS[3] / UART0_CTS / GP8[2] / MII_RXD[1] / **SATA_MP_SWITCH** | E17 | I | CP[9] | A | SATA mechanical presence switch input |
| SPI0_SCS[2] / UART0_RTS / GP8[1] / MII_RXD[0] / **SATA_CP_DET** | D16 | I | CP[9] | A | SATA cold presence detect input |
| SPI1_SCS[2] / UART1_TXD / **SATA_CP_POD** / GP1[0] | F19 | O | CP[13] | A | SATA cold presence power-on output |
| SPI1_SCS[3] / UART1_RXD / **SATA_LED** / GP1[1] | E18 | O | CP[13] | A | SATA LED control output |
| **SATA_REG** | N3 | A | — | — | SATA PHY PLL regulator output. Requires an external 0.1uF filter capacitor. |
| **SATA_VDDR** | P3 | PWR | — | — | SATA PHY 1.8V internal regulator supply |
| **SATA_VDD** | M2, P1, P2, N4 | PWR | — | — | SATA PHY 1.2V logic supply |
| **SATA_VSS** | H1, H2, K1, K2, L3, M1 | GND | — | — | SATA PHY ground reference |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.

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### 2.8.22 Universal Host-Port Interface (UHPI)

**Table 2-26. Universal Host-Port Interface (UHPI) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| VP_DIN[7] / **UHPI_HD[15]** / UPP_D[15] / RMII_TXD[1] / PRU0_R31[29] | U18 | I/O | CP[26] | C | UHPI data bus |
| VP_DIN[6] / **UHPI_HD[14]** / UPP_D[14] / RMII_TXD[0] / PRU0_R31[28] | V16 | I/O | CP[26] | C | |
| VP_DIN[5] / **UHPI_HD[13]** / UPP_D[13] / RMII_TXEN / PRU0_R31[27] | R14 | I/O | CP[26] | C | |
| VP_DIN[4] / **UHPI_HD[12]** / UPP_D[12] / RMII_RXD[1] / PRU0_R31[26] | W16 | I/O | CP[26] | C | |
| VP_DIN[3] / **UHPI_HD[11]** / UPP_D[11] / RMII_RXD[0] / PRU0_R31[25] | V17 | I/O | CP[26] | C | |
| VP_DIN[2] / **UHPI_HD[10]** / UPP_D[10] / RMII_RXER / PRU0_R31[24] | W17 | I/O | CP[26] | C | |
| VP_DIN[1] / **UHPI_HD[9]** / UPP_D[9] / RMII_MHZ_50_CLK / PRU0_R31[23] | W18 | I/O | CP[26] | C | |
| VP_DIN[0] / **UHPI_HD[8]** / UPP_D[8] / RMII_CRS_DV / PRU1_R31[29] | W19 | I/O | CP[26] | C | |
| VP_DIN[15]_VSYNC / **UHPI_HD[7]** / UPP_D[7] / PRU0_R30[15] / PRU0_R31[15] | V18 | I/O | CP[27] | C | |
| VP_DIN[14]_HSYNC / **UHPI_HD[6]** / UPP_D[6] / PRU0_R30[14] / PRU0_R31[14] | V19 | I/O | CP[27] | C | |
| VP_DIN[13]_FIELD / **UHPI_HD[5]** / UPP_D[5] / PRU0_R30[13] / PRU0_R31[13] | U19 | I/O | CP[27] | C | |
| VP_DIN[12] / **UHPI_HD[4]** / UPP_D[4] / PRU0_R30[12] / PRU0_R31[12] | T16 | I/O | CP[27] | C | |
| VP_DIN[11] / **UHPI_HD[3]** / UPP_D[3] / PRU0_R30[11] / PRU0_R31[11] | R18 | I/O | CP[27] | C | |
| VP_DIN[10] / **UHPI_HD[2]** / UPP_D[2] / PRU0_R30[10] / PRU0_R31[10] | R19 | I/O | CP[27] | C | |
| VP_DIN[9] / **UHPI_HD[1]** / UPP_D[1] / PRU0_R30[9] / PRU0_R31[9] | R15 | I/O | CP[27] | C | |
| VP_DIN[8] / **UHPI_HD[0]** / UPP_D[0] / GP6[5] / PRU1_R31[0] | P17 | I/O | CP[27] | C | |
| PRU0_R30[29] / **UHPI_HCNTL0** / UPP_CHA_CLOCK / GP6[11] | U17 | I | CP[24] | C | UHPI access control |
| PRU0_R30[28] / **UHPI_HCNTL1** / UPP_CHA_START / GP6[10] | W15 | I | CP[24] | C | |
| PRU0_R30[27] / **UHPI_HHWIL** / UPP_CHA_ENABLE / GP6[9] | U16 | I | CP[24] | C | UHPI half-word identification control |
| PRU0_R30[26] / **UHPI_HR$\overline{W}$** / UPP_CHA_WAIT / GP6[8]/PRU1_R31[17] | T15 | I | CP[24] | C | UHPI read/write |
| VP_CLKIN0 / **$\overline{\text{UHPI_HCS}}$** / PRU1_R30[10] / GP6[7] / UPP_2xTXCLK | W14 | I | CP[25] | C | UHPI chip select |
| VP_CLKIN1 / **$\overline{\text{UHPI_HDS1}}$** / PRU1_R30[9] / GP6[6] / PRU1_R31[16] | V15 | I | CP[25] | C | UHPI data strobe |
| CLKOUT / **$\overline{\text{UHPI_HDS2}}$** / PRU1_R30[13] / GP6[14] | T18 | I | CP[22] | C | |
| PRU0_R30[30] / **$\overline{\text{UHPI_HINT}}$** / PRU1_R30[11] / GP6[12] | R16 | O | CP[23] | C | UHPI host interrupt |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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**Table 2-26. Universal Host-Port Interface (UHPI) Terminal Functions (continued)**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| PRU0_R30[31] / **UHPI_HRDY** / PRU1_R30[12] /GP6[13] | R17 | O | CP[23] | C | UHPI ready |
| RESETOUT / **UHPI_HAS** / PRU1_R30[14] / GP6[15] | T17 | I | CP[21] | C | UHPI address strobe |

### 2.8.23 Universal Parallel Port (uPP)

**Table 2-27. Universal Parallel Port (uPP) Terminal Functions**

| SIGNAL | | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| VP_CLKIN0 / $\overline{\text{UHPI_HCS}}$ /PRU1_R30[10] / GP6[7] / **UPP_2xTXCLK** | W14 | I | CP[25] | C | uPP 2x transmit clock input |
| PRU0_R30[25] /MMCSD1_DAT[0] / **UPP_CHB_CLOCK** / GP8[15]/PRU1_R31[27] | G1 | I/O | CP[30] | C | uPP channel B clock |
| PRU0_R30[24]/ MMCSD1_CLK / **UPP_CHB_START** / GP8[14] / PRU1_R31[26] | G2 | I/O | CP[30] | C | uPP channel B start |
| PRU0_R30[23] / MMCSD1_CMD / **UPP_CHB_ENABLE** / GP8[13]/PRU1_R31[25] | J4 | I/O | CP[30] | C | uPP channel B enable |
| PRU0_R30[22] / PRU1_R30[8] / **UPP_CHB_WAIT** / GP8[12]/ PRU1_R31[24] | G3 | I/O | CP[30] | C | uPP channel B wait |
| PRU0_R30[29] /UHPI_HCNTL0 / **UPP_CHA_CLOCK** / GP6[11] | U17 | I/O | CP[24] | C | uPP channel A clock |
| PRU0_R30[28] / UHPI_HCNTL1 / **UPP_CHA_START** / GP6[10] | W15 | I/O | CP[24] | C | uPP channel A start |
| PRU0_R30[27] / UHPI_HHWIL / **UPP_CHA_ENABLE** / GP6[9] | U16 | I/O | CP[24] | C | uPP channel A enable |
| PRU0_R30[26] /UHPI_$\overline{\text{HRW}}$ / **UPP_CHA_WAIT** / GP6[8] / PRU1_R31[17] | T15 | I/O | CP[24] | C | uPP channel A wait |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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**Table 2-27. Universal Parallel Port (uPP) Terminal Functions (continued)**

| SIGNAL | | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| VP_DOUT[7] / LCD_D[7] / **UPP_XD[15]** / GP7[15] / PRU1_R31[15] | U2 | I/O | CP[28] | C | |
| VP_DOUT[6] / LCD_D[6] / **UPP_XD[14]** / GP7[14] / PRU1_R31[14] | U1 | I/O | CP[28] | C | |
| VP_DOUT[5] / LCD_D[5] / **UPP_XD[13]** / GP7[13] / PRU1_R31[13] | V3 | I/O | CP[28] | C | |
| VP_DOUT[4] / LCD_D[4] / **UPP_XD[12]** / GP7[12] / PRU1_R31[12] | V2 | I/O | CP[28] | C | |
| VP_DOUT[3] / LCD_D[3] / **UPP_XD[11]** / GP7[11] / PRU1_R31[11] | V1 | I/O | CP[28] | C | |
| VP_DOUT[2] / LCD_D[2] / **UPP_XD[10]** / GP7[10] / PRU1_R31[10] | W3 | I/O | CP[28] | C | |
| VP_DOUT[1] / LCD_D[1] / **UPP_XD[9]** / GP7[9] / PRU1_R31[9] | W2 | I/O | CP[28] | C | |
| VP_DOUT[0] / LCD_D[0] / **UPP_XD[8]** / GP7[8] / PRU1_R31[8] | W1 | I/O | CP[28] | C | |
| VP_DOUT[15] / LCD_D[15] / **UPP_XD[7]** / GP7[7] / BOOT[7] | P4 | I/O | CP[29] | C | |
| VP_DOUT[14] / LCD_D[14] / **UPP_XD[6]** / GP7[6] / BOOT[6] | R3 | I/O | CP[29] | C | |
| VP_DOUT[13] / LCD_D[13] / **UPP_XD[5]** / GP7[5] / BOOT[5] | R2 | I/O | CP[29] | C | |
| VP_DOUT[12] / LCD_D[12] / **UPP_XD[4]** / GP7[4] / BOOT[4] | R1 | I/O | CP[29] | C | |
| VP_DOUT[11] / LCD_D[11] / **UPP_XD[3]** / GP7[3] / BOOT[3] | T3 | I/O | CP[29] | C | |
| VP_DOUT[10] / LCD_D[10] / **UPP_XD[2]** / GP7[2] / BOOT[2] | T2 | I/O | CP[29] | C | |
| VP_DOUT[9] / LCD_D[9] / **UPP_XD[1]** / GP7[1] / BOOT[1] | T1 | I/O | CP[29] | C | |
| VP_DOUT[8] / LCD_D[8] / **UPP_XD[0]** / GP7[0] / BOOT[0] | U3 | I/O | CP[29] | C | |
| VP_DIN[7] / UHPI_HD[15] / **UPP_D[15]** / RMII_TXD[1] / PRU0_R31[29] | U18 | I/O | CP[26] | C | |
| VP_DIN[6] / UHPI_HD[14] / **UPP_D[14]** / RMII_TXD[0] / PRU0_R31[28] | V16 | I/O | CP[26] | C | uPP data bus |
| VP_DIN[5] / UHPI_HD[13] / **UPP_D[13]** / RMII_TXEN / PRU0_R31[27] | R14 | I/O | CP[26] | C | |
| VP_DIN[4] / UHPI_HD[12] / **UPP_D[12]** / RMII_RXD[1] / PRU0_R31[26] | W16 | I/O | CP[26] | C | |
| VP_DIN[3] / UHPI_HD[11] / **UPP_D[11]** / RMII_RXD[0] / PRU0_R31[25] | V17 | I/O | CP[26] | C | |
| VP_DIN[2] / UHPI_HD[10] / **UPP_D[10]** / RMII_RXER / PRU0_R31[24] | W17 | I/O | CP[26] | C | |
| VP_DIN[1] / UHPI_HD[9] / **UPP_D[9]** / RMII_MHZ_50_CLK / PRU0_R31[23] | W18 | I/O | CP[26] | C | |
| VP_DIN[0] / UHPI_HD[8] / **UPP_D[8]** / RMII_CRS_DV / PRU1_R31[29] | W19 | I/O | CP[26] | C | |
| VP_DIN[15]_VSYNC / UHPI_HD[7] / **UPP_D[7]**/PRU0_R30[15] / PRU0_R31[15] | V18 | I/O | CP[27] | C | |
| VP_DIN[14]_HSYNC / UHPI_HD[6] / **UPP_D[6]**/ PRU0_R30[14] / PRU0_R31[14] | V19 | I/O | CP[27] | C | |
| VP_DIN[13]_FIELD / UHPI_HD[5] / **UPP_D[5] /**PRU0_R30[13] / PRU0_R31[13] | U19 | I/O | CP[27] | C | |
| VP_DIN[12] / UHPI_HD[4] / **UPP_D[4]**/ PRU0_R30[12] / PRU0_R31[12] | T16 | I/O | CP[27] | C | |
| VP_DIN[11] / UHPI_HD[3] / **UPP_D[3]**/ PRU0_R30[11] / PRU0_R31[11] | R18 | I/O | CP[27] | C | |
| VP_DIN[10] / UHPI_HD[2] / **UPP_D[2]**/ PRU0_R30[10] / PRU0_R31[10] | R19 | I/O | CP[27] | C | |
| VP_DIN[9] / UHPI_HD[1] / **UPP_D[1]**/ PRU0_R30[9] / PRU0_R31[9] | R15 | I/O | CP[27] | C | |
| VP_DIN[8] / UHPI_HD[0] / **UPP_D[0]** / GP6[5] / PRU1_R31[0] | P17 | I/O | CP[27] | C | |

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### 2.8.24 Video Port Interface (VPIF)

**Table 2-28. Video Port Interface (VPIF) Terminal Functions**

| SIGNAL NAME | NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **VIDEO INPUT** | | | | | |
| **VP_CLKIN0** / $\overline{\text{UHPI_HCS}}$ / PRU1_R30[10] / GP6[7] / UPP_2xTXCLK | W14 | I | CP[25] | C | VPIF capture channel 0 input clock |
| **VP_CLKIN1** / $\overline{\text{UHPI_HDS1}}$/PRU1_R30[9] / GP6[6] / PRU1_R31[16] | V15 | I | CP[25] | C | VPIF capture channel 1 input clock |
| **VP_DIN[15]_VSYNC** / UHPI_HD[7] / UPP_D[7] / PRU0_R30[15] / PRU0_R31[15] | V18 | I | CP[27] | C | VPIF capture data bus |
| **VP_DIN[14]_HSYNC** / UHPI_HD[6] / UPP_D[6] / RU0_R30[14] / PRU0_R31[14] | V19 | I | CP[27] | C | |
| **VP_DIN[13]_FIELD** / UHPI_HD[5] / UPP_D[5] / PRU0_R30[13] / PRU0_R31[13] | U19 | I | CP[27] | C | |
| **VP_DIN[12]** / UHPI_HD[4] / UPP_D[4] / PRU0_R30[12] / PRU0_R31[12] | T16 | I | CP[27] | C | |
| **VP_DIN[11]** / UHPI_HD[3] / UPP_D[3] / PRU0_R30[11] / PRU0_R31[11] | R18 | I | CP[27] | C | |
| **VP_DIN[10]** / UHPI_HD[2] / UPP_D[2] / PRU0_R30[10] / PRU0_R31[10] | R19 | I | CP[27] | C | |
| **VP_DIN[9]** / UHPI_HD[1] / UPP_D[1] / PRU0_R30[9] / PRU0_R31[9] | R15 | I | CP[27] | C | |
| **VP_DIN[8]** / UHPI_HD[0] / UPP_D[0] / GP6[5] / PRU1_R31[0] | P17 | I | CP[27] | C | |
| **VP_DIN[7]** / UHPI_HD[15] / UPP_D[15] / RMII_TXD[1] / PRU0_R31[29] | U18 | I | CP[26] | C | |
| **VP_DIN[6]** / UHPI_HD[14] / UPP_D[14] / RMII_TXD[0] / PRU0_R31[28] | V16 | I | CP[26] | C | |
| **VP_DIN[5]** / UHPI_HD[13] / UPP_D[13] / RMII_TXEN / PRU0_R31[27] | R14 | I | CP[26] | C | |
| **VP_DIN[4]** / UHPI_HD[12] / UPP_D[12] / RMII_RXD[1] / PRU0_R31[26] | W16 | I | CP[26] | C | |
| **VP_DIN[3]** / UHPI_HD[11] / UPP_D[11] / MII_RXD[0] / PRU0_R31[25] | V17 | I | CP[26] | C | |
| **VP_DIN[2]** / UHPI_HD[10] / UPP_D[10] / RMII_RXER / PRU0_R31[24] | W17 | I | CP[26] | C | |
| **VP_DIN[1]** / UHPI_HD[9] / UPP_D[9] / RMII_MHZ_50_CLK / PRU0_R31[23] | W18 | I | CP[26] | C | |
| **VP_DIN[0]** / UHPI_HD[8] / UPP_D[8] / RMII_CRS_DV / PRU1_R31[29] | W19 | I | CP[26] | C | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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**Table 2-28. Video Port Interface (VPIF) Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| **VIDEO OUTPUT** | | | | | |
| **VP_CLKIN2** / MMCSD1_DAT[3] / PRU1_R30[3] / GP6[4] / PRU1_R31[4] | H3 | I | CP[30] | C | VPIF display channel 2 input clock |
| **VP_CLKOUT2** / MMCSD1_DAT[2] / PRU1_R30[2] / GP6[3] / PRU1_R31[3] | K3 | O | CP[30] | C | VPIF display channel 2 output clock |
| **VP_CLKIN3** / MMCSD1_DAT[1] / PRU1_R30[1] / GP6[2] / PRU1_R31[2] | J3 | I | CP[30] | C | VPIF display channel 3 input clock |
| **VP_CLKOUT3** / PRU1_R30[0] / GP6[1] / PRU1_R31[1] | K4 | O | CP[30] | C | VPIF display channel 3 output clock |
| **VP_DOUT[15]** / LCD_D[15] / UPP_XD[7] / GP7[7] / BOOT[7] | P4 | O | CP[29] | C | VPIF display data bus |
| **VP_DOUT[14]** / LCD_D[14] / UPP_XD[6] / GP7[6] / BOOT[6] | R3 | O | CP[29] | C | |
| **VP_DOUT[13]** / LCD_D[13] / UPP_XD[5] / GP7[5] / BOOT[5] | R2 | O | CP[29] | C | |
| **VP_DOUT[12]** / LCD_D[12] / UPP_XD[4] / GP7[4] / BOOT[4] | R1 | O | CP[29] | C | |
| **VP_DOUT[11]** / LCD_D[11] / UPP_XD[3] / GP7[3] / BOOT[3] | T3 | O | CP[29] | C | |
| **VP_DOUT[10]** / LCD_D[10] / UPP_XD[2] / GP7[2] / BOOT[2] | T2 | O | CP[29] | C | |
| **VP_DOUT[9]** / LCD_D[9] / UPP_XD[1] / GP7[1] / BOOT[1] | T1 | O | CP[29] | C | |
| **VP_DOUT[8]** / LCD_D[8] / UPP_XD[0] / GP7[0] / BOOT[0] | U3 | O | CP[29] | C | |
| **VP_DOUT[7]** / LCD_D[7] / UPP_XD[15] / GP7[15] / PRU1_R31[15] | U2 | O | CP[28] | C | |
| **VP_DOUT[6]** / LCD_D[6] / UPP_XD[14] / GP7[14] / PRU1_R31[14] | U1 | O | CP[28] | C | |
| **VP_DOUT[5]** / LCD_D[5] / UPP_XD[13] / GP7[13] / PRU1_R31[13] | V3 | O | CP[28] | C | |
| **VP_DOUT[4]** / LCD_D[4] / UPP_XD[12] / GP7[12] / PRU1_R31[12] | V2 | O | CP[28] | C | |
| **VP_DOUT[3]** / LCD_D[3] / UPP_XD[11] / GP7[11] / PRU1_R31[11] | V1 | O | CP[28] | C | |
| **VP_DOUT[2]** / LCD_D[2] / UPP_XD[10] / GP7[10] / PRU1_R31[10] | W3 | O | CP[28] | C | |
| **VP_DOUT[1]** / LCD_D[1] / UPP_XD[9] / GP7[9] / PRU1_R31[9] | W2 | O | CP[28] | C | |
| **VP_DOUT[0]** / LCD_D[0] / UPP_XD[8] / GP7[8] / PRU1_R31[8] | W1 | O | CP[28] | C | |

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### 2.8.25 General Purpose Input Output

**Table 2-29. General Purpose Input Output Terminal Functions**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **GP0** | | | | | |
| ACLKR / PRU0_R30[20] / **GP0[15]** / PRU0_R31[22] | A1 | I/O | CP[0] | A | GPIO Bank 0 |
| ACLKX / PRU0_R30[19] / **GP0[14]** / PRU0_R31[21] | B1 | I/O | CP[0] | A | |
| AFSR / **GP0[13]** / PRU0_R31[20] | C2 | I/O | CP[0] | A | |
| AFSX / **GP0[12]** / PRU0_R31[19] | B2 | I/O | CP[0] | A | |
| AHCLKR / PRU0_R30[18] / $\overline{\text{UART1_RTS}}$ / **GP0[11]** / PRU0_R31[18] | A2 | I/O | CP[0] | A | |
| AHCLKX / USB_REFCLKIN / $\overline{\text{UART1_CTS}}$ / **GP0[10]** / PRU0_R31[17] | A3 | I/O | CP[0] | A | |
| AMUTE / PRU0_R30[16] / $\overline{\text{UART2_RTS}}$ / **GP0[9]** / PRU0_R31[16] | D5 | I/O | CP[0] | A | |
| RTC_ALARM / $\overline{\text{UART2_CTS}}$ / **GP0[8]** / $\overline{\text{DEEPSLEEP}}$ | F4 | I/O | CP[0] | A | |
| AXR15 / EPWM0TZ[0] / ECAP2_APWM2 / **GP0[7]** | A4 | I/O | CP[1] | A | |
| AXR14 / CLKR1 / **GP0[6]** | B4 | I/O | CP[2] | A | |
| AXR13 / CLKX1 / **GP0[5]** | B3 | I/O | CP[2] | A | |
| AXR12 / FSR1 / **GP0[4]** | C4 | I/O | CP[2] | A | |
| AXR11 / FSX1 / **GP0[3]** | C5 | I/O | CP[2] | A | |
| AXR10 / DR1 / **GP0[2]** | D4 | I/O | CP[2] | A | |
| AXR9 / DX1 / **GP0[1]** | C3 | I/O | CP[2] | A | |
| AXR8 / CLKS1 / ECAP1_APWM1 /**GP0[0]** / PRU0_R31[8] | E4 | I/O | CP[3] | A | |

(1) I = Input, O = Output, I/O = Bidirectional, Z = High impedance, PWR = Supply voltage, GND = Ground, A = Analog signal.
**Note:** The pin type shown refers to the input, output or high-impedance state of the pin function when configured as the signal name highlighted in bold. All multiplexed signals may enter a high-impedance state when the configured function is input-only or the configured function supports high-Z operation. All GPIO signals can be used as input or output. For multiplexed pins where functions have different types (ie., input versus output), the table reflects the pin function direction for that particular peripheral.

(2) IPD = Internal Pulldown resistor; IPU = Internal Pullup resistor; CP[*n*] = configurable pull-up/pull-down (where *n* is the pin group) using the PUPDENA and PUPDSEL registers in the System Module. The pull-up and pull-down control of these pins is not active until the device is out of reset. During reset, all of the pins associated with these registers are pulled down. If the application requires a pull-up, an external pull-up can be used. For electrical specifications on the pull-up and and internal pull-down circuits, see the Device Operating Conditions section.

(3) This signal is part of a dual-voltage IO group (A, B or C). These groups can be operated at 3.3V or 1.8V nominal. The three groups can be operated at independent voltages but all pins withina group will operate at the same voltage. Group A operates at the voltage of power supply DVDD3318_A. Group B operates at the voltage of power supply DVDD3318_B. Group C operates at the voltage of power supply DVDD3318_C.


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**Table 2-29. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **GP1** | | | | | |
| AXR7 / EPWM1TZ[0] / PRU0_R30[17] / **GP1[15]** / PRU0_R31[7] | D2 | I/O | CP[4] | A | GPIO Bank 1 |
| AXR6 / CLKR0 / **GP1[14]** / MII_TXEN / PRU0_R31[6] | C1 | I/O | CP[5] | A | |
| AXR5 / CLKX0 / **GP1[13]** / MII_TXCLK | D3 | I/O | CP[5] | A | |
| AXR4 / FSR0 / **GP1[12]** / MII_COL | D1 | I/O | CP[5] | A | |
| AXR3 / FSX0 / **GP1[11]** / MII_TXD[3] | E3 | I/O | CP[5] | A | |
| AXR2 / DR0 / **GP1[10]** / MII_TXD[2] | E2 | I/O | CP[5] | A | |
| AXR1 / DX0 / **GP1[9]** / MII_TXD[1] | E1 | I/O | CP[5] | A | |
| SPI0_CLK / EPWM0A / **GP1[8]** / MII_RXCLK | D19 | I/O | CP[7] | A | |
| $\overline{\text{SPI0_SCS[1]}}$ / TM64P0_OUT12 / **GP1[7]** / MDIO_CLK / TM64P0_IN12 | E16 | I/O | CP[10] | A | |
| $\overline{\text{SPI0_SCS[0]}}$ / TM64P1_OUT12 / **GP1[6]** / MDIO_D / TM64P1_IN12 | D17 | I/O | CP[10] | A | |
| $\overline{\text{SPI1_SCS[7]}}$ / I2C0_SCL / TM64P2_OUT12 / **GP1[5]** | G16 | I/O | CP[11] | A | |
| $\overline{\text{SPI1_SCS[6]}}$ / I2C0_SDA / TM64P3_OUT12 / **GP1[4]** | G18 | I/O | CP[11] | A | |
| $\overline{\text{SPI1_SCS[5]}}$ / UART2_RXD / I2C1_SCL / **GP1[3]** | F17 | I/O | CP[12] | A | |
| $\overline{\text{SPI1_SCS[4]}}$ / UART2_TXD / I2C1_SDA / **GP1[2]** | F16 | I/O | CP[12] | A | |
| $\overline{\text{SPI1_SCS[3]}}$ / UART1_RXD / SATA_LED / **GP1[1]** | E18 | I/O | CP[13] | A | |
| $\overline{\text{SPI1_SCS[2]}}$ / UART1_TXD / SATA_CP_POD / **GP1[0]** | F19 | I/O | CP[13] | A | |

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**Table 2-29. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **GP2** | | | | | |
| $\overline{\text{SPI1_SCS[1]}}$ / EPWM1A / PRU0_R30[8] / **GP2[15]** / TM64P2_IN12 | F18 | I/O | CP[14] | A | GPIO Bank 2 |
| $\overline{\text{SPI1_SCS[0]}}$ / EPWM1B / PRU0_R30[7] / **GP2[14]** / TM64P3_IN12 | E19 | I/O | CP[14] | A | |
| SPI1_CLK / **GP2[13]** | G19 | I/O | CP[15] | A | |
| $\overline{\text{SPI1_ENA}}$ / **GP2[12]** | H16 | I/O | CP[15] | A | |
| SPI1_SOMI / **GP2[11]** | H17 | I/O | CP[15] | A | |
| SPI1_SIMO / **GP2[10]** | G17 | I/O | CP[15] | A | |
| EMA_BA[1] / **GP2[9]** | A15 | I/O | CP[16] | B | |
| EMA_BA[0] / **GP2[8]** | C15 | I/O | CP[16] | B | |
| EMA_CLK / PRU0_R30[5] / **GP2[7]** / PRU0_R31[5] | B7 | I/O | CP[16] | B | |
| EMA_SDCKE / PRU0_R30[4] / **GP2[6]** / PRU0_R31[4] | D8 | I/O | CP[16] | B | |
| $\overline{\text{EMA_RAS}}$ / PRU0_R30[3] / **GP2[5]** / PRU0_R31[3] | A16 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CAS}}$ / PRU0_R30[2] / **GP2[4]** / PRU0_R31[2] | A9 | I/O | CP[16] | B | |
| $\overline{\text{EMA_WEN_DQM[0]}}$ / **GP2[3]** | C8 | I/O | CP[16] | B | |
| $\overline{\text{EMA_WEN_DQM[1]}}$ / **GP2[2]** | A5 | I/O | CP[16] | B | |
| EMA_WAIT[1] / PRU0_R30[1] / **GP2[1]** / PRU0_R31[1] | B19 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CS[0]}}$ / **GP2[0]** | A18 | I/O | CP[16] | B | |
| **GP3** | | | | | |
| $\overline{\text{EMA_CS[2]}}$ / **GP3[15]** | B17 | I/O | CP[16] | B | GPIO Bank 3 |
| $\overline{\text{EMA_CS[3]}}$ / **GP3[14]** | A17 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CS[4]}}$ / **GP3[13]** | F9 | I/O | CP[16] | B | |
| $\overline{\text{EMA_CS[5]}}$ / **GP3[12]** | B16 | I/O | CP[16] | B | |
| $\overline{\text{EMA_WE}}$ / **GP3[11]** | B9 | I/O | CP[16] | B | |
| $\overline{\text{EMA_OE}}$ / **GP3[10]** | B15 | I/O | CP[16] | B | |
| EMA_A_$\overline{\text{RW}}$ / **GP3[9]** | D10 | I/O | CP[16] | B | |
| EMA_WAIT[0] / PRU0_R30[0] / **GP3[8]** / PRU0_R31[0] | B18 | I/O | CP[16] | B | |
| EMA_D[15] / **GP3[7]** | E6 | I/O | CP[17] | B | |
| EMA_D[14] / **GP3[6]** | C7 | I/O | CP[17] | B | |
| EMA_D[13] / **GP3[5]** | B6 | I/O | CP[17] | B | |
| EMA_D[12] / **GP3[4]** | A6 | I/O | CP[17] | B | |
| EMA_D[11] / **GP3[3]** | D6 | I/O | CP[17] | B | |
| EMA_D[10] / **GP3[2]** | A7 | I/O | CP[17] | B | |
| EMA_D[9] / **GP3[1]** | D9 | I/O | CP[17] | B | |
| EMA_D[8] / **GP3[0]** | E10 | I/O | CP[17] | B | |


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**Table 2-29. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL NAME | SIGNAL NO. | TYPE[1] | PULL[2] | POWER GROUP[3] | DESCRIPTION |
|---|---|---|---|---|---|
| **GP4** | | | | | |
| EMA_D[7] / **GP4[15]** | D7 | I/O | CP[17] | B | GPIO Bank 4 |
| EMA_D[6] / **GP4[14]** | C6 | I/O | CP[17] | B | |
| EMA_D[5] / **GP4[13]** | E7 | I/O | CP[17] | B | |
| EMA_D[4] / **GP4[12]** | B5 | I/O | CP[17] | B | |
| EMA_D[3] / **GP4[11]** | E8 | I/O | CP[17] | B | |
| EMA_D[2] / **GP4[10]** | B8 | I/O | CP[17] | B | |
| EMA_D[1] / **GP4[9]** | A8 | I/O | CP[17] | B | |
| EMA_D[0] / **GP4[8]** | C9 | I/O | CP[17] | B | |
| MMCSD0_CLK / PRU1_R30[31] / **GP4[7]** | E9 | I/O | CP[18] | B | |
| EMA_A[22] / MMCSD0_CMD / PRU1_R30[30] / **GP4[6]** | A10 | I/O | CP[18] | B | |
| EMA_A[21] / MMCSD0_DAT[0] / PRU1_R30[29] / **GP4[5]** | B10 | I/O | CP[18] | B | |
| EMA_A[20] / MMCSD0_DAT[1] / PRU1_R30[28] / **GP4[4]** | A11 | I/O | CP[18] | B | |
| EMA_A[19] / MMCSD0_DAT[2] / PRU1_R30[27] / **GP4[3]** | C10 | I/O | CP[18] | B | |
| EMA_A[18] / MMCSD0_DAT[3] / PRU1_R30[26] / **GP4[2]** | E11 | I/O | CP[18] | B | |
| EMA_A[17] / MMCSD0_DAT[4] / PRU1_R30[25] / **GP4[1]** | B11 | I/O | CP[18] | B | |
| EMA_A[16] / MMCSD0_DAT[5] / PRU1_R30[24] / **GP4[0]** | E12 | I/O | CP[18] | B | |
| **GP5** | | | | | |
| EMA_A[15] / MMCSD0_DAT[6] / PRU1_R30[23] / **GP5[15]** / PRU1_R31[23] | C11 | I/O | CP[19] | B | GPIO Bank 5 |
| EMA_A[14] / MMCSD0_DAT[7] / PRU1_R30[22] / **GP5[14]** / PRU1_R31[22] | A12 | I/O | CP[19] | B | |
| EMA_A[13] / PRU0_R30[21] / PRU1_R30[21] / **GP5[13]** / PRU1_R31[21] | D11 | I/O | CP[19] | B | |
| EMA_A[12] / PRU1_R30[20] / **GP5[12]** / PRU1_R31[20] | D13 | I/O | CP[19] | B | |
| EMA_A[11] / PRU1_R30[19] / **GP5[11]** / PRU1_R31[19] | B12 | I/O | CP[19] | B | |
| EMA_A[10] / PRU1_R30[18] / **GP5[10]** / PRU1_R31[18] | C12 | I/O | CP[19] | B | |
| EMA_A[9] / PRU1_R30[17] / **GP5[9]** | D12 | I/O | CP[19] | B | |
| EMA_A[8] / PRU1_R30[16] / **GP5[8]** | A13 | I/O | CP[19] | B | |
| EMA_A[7] / PRU1_R30[15] / **GP5[7]** | B13 | I/O | CP[20] | B | |
| EMA_A[6] / **GP5[6]** | E13 | I/O | CP[20] | B | |
| EMA_A[5] / **GP5[5]** | C13 | I/O | CP[20] | B | |
| EMA_A[4] / **GP5[4]** | A14 | I/O | CP[20] | B | |
| EMA_A[3] / **GP5[3]** | D14 | I/O | CP[20] | B | |
| EMA_A[2] / **GP5[2]** | B14 | I/O | CP[20] | B | |
| EMA_A[1] / **GP5[1]** | D15 | I/O | CP[20] | B | |
| EMA_A[0] / **GP5[0]** | C14 | I/O | CP[20] | B | |

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**Table 2-29. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **GP6** | | | | | |
| $\overline{\text{RESETOUT}}$ / $\overline{\text{UHPI_HAS}}$ / PRU1_R30[14] / **GP6[15]** | T17 | I/O | CP[21] | C | GPIO Bank 6 |
| CLKOUT / $\overline{\text{UHPI_HDS2}}$ / PRU1_R30[13] / **GP6[14]** | T18 | I/O | CP[22] | C | |
| PRU0_R30[31] / $\overline{\text{UHPI_HRDY}}$ / PRU1_R30[12] / **GP6[13]** | R17 | I/O | CP[23] | C | |
| PRU0_R30[30] / $\overline{\text{UHPI_HINT}}$ / PRU1_R30[11] / **GP6[12]** | R16 | I/O | CP[23] | C | |
| PRU0_R30[29] / UHPI_HCNTL0 / UPP_CHA_CLOCK / **GP6[11]** | U17 | I/O | CP[24] | C | |
| PRU0_R30[28] / UHPI_HCNTL1 / UPP_CHA_START / **GP6[10]** | W15 | I/O | CP[24] | C | |
| /PRU0_R30[27] / UHPI_HHWIL / UPP_CHA_ENABLE / **GP6[9]** | U16 | I/O | CP[24] | C | |
| PRU0_R30[26] / UHPI_HR$\overline{\text{W}}$ / UPP_CHA_WAIT**GP6[8]** / PRU1_R31[17] | T15 | I/O | CP[24] | C | |
| VP_CLKIN0 / $\overline{\text{UHPI_HCS}}$ / PRU1_R30[10] **GP6[7]** / UPP_2xTXCLK | W14 | I/O | CP[25] | C | |
| VP_CLKIN1 / $\overline{\text{UHPI_HDS1}}$ / PRU1_R30[9] / **GP6[6]** / PRU1_R31[16] | V15 | I/O | CP[25] | C | |
| VP_DIN[8] / UHPI_HD[0] / UPP_D[0] / **GP6[5]** / PRU1_R31[0] | P17 | I/O | CP[27] | C | |
| VP_CLKIN2 / MMCSD1_DAT[3] / PRU1_R30[3] / **GP6[4]** / PRU1_R31[4] | H3 | I/O | CP[30] | C | |
| VP_CLKOUT2 / MMCSD1_DAT[2] / PRU1_R30[2] / **GP6[3]** / PRU1_R31[3] | K3 | I/O | CP[30] | C | |
| VP_CLKIN3 / MMCSD1_DAT[1] / PRU1_R30[1] / **GP6[2]** / PRU1_R31[2] | J3 | I/O | CP[30] | C | |
| VP_CLKOUT3 / PRU1_R30[0] / **GP6[1]** / PRU1_R31[1] | K4 | I/O | CP[30] | C | |
| $\overline{\text{LCD_AC_ENB_CS}}$ / **GP6[0]** / PRU1_R31[28] | R5 | I/O | CP[31] | C | |
| **GP7** | | | | | |
| VP_DOUT[7] / LCD_D[7] / UPP_XD[15] / **GP7[15]** / PRU1_R31[15] | U2 | I/O | CP[28] | C | GPIO Bank 7 |
| VP_DOUT[6] / LCD_D[6] / UPP_XD[14] / **GP7[14]** / PRU1_R31[14] | U1 | I/O | CP[28] | C | |
| VP_DOUT[5] / LCD_D[5] / UPP_XD[13] / **GP7[13]** / PRU1_R31[13] | V3 | I/O | CP[28] | C | |
| VP_DOUT[4] / LCD_D[4] / UPP_XD[12] / **GP7[12]** / PRU1_R31[12] | V2 | I/O | CP[28] | C | |
| VP_DOUT[3] / LCD_D[3] / UPP_XD[11] / **GP7[11]** / PRU1_R31[11] | V1 | I/O | CP[28] | C | |
| VP_DOUT[2] / LCD_D[2] / UPP_XD[10] / **GP7[10]** / PRU1_R31[10] | W3 | I/O | CP[28] | C | |
| VP_DOUT[1] / LCD_D[1] / UPP_XD[9] / **GP7[9]** / PRU1_R31[9] | W2 | I/O | CP[28] | C | |
| VP_DOUT[0] / LCD_D[0] / UPP_XD[8] / **GP7[8]** / PRU1_R31[8] | W1 | I/O | CP[28] | C | |
| VP_DOUT[15] / LCD_D[15] / UPP_XD[7] / **GP7[7]** / BOOT[7] | P4 | I/O | CP[29] | C | |
| VP_DOUT[14] / LCD_D[14] / UPP_XD[6] / **GP7[6]** / BOOT[6] | R3 | I/O | CP[29] | C | |
| VP_DOUT[13] / LCD_D[13] / UPP_XD[5] / **GP7[5]**/ BOOT[5] | R2 | I/O | CP[29] | C | |
| VP_DOUT[12] / LCD_D[12] / UPP_XD[4] / **GP7[4]** / BOOT[4] | R1 | I/O | CP[29] | C | |
| VP_DOUT[11] / LCD_D[11] / UPP_XD[3] / **GP7[3]** / BOOT[3] | T3 | I/O | CP[29] | C | |
| VP_DOUT[10] / LCD_D[10] / UPP_XD[2] / **GP7[2]** / BOOT[2] | T2 | I/O | CP[29] | C | |
| VP_DOUT[9] / LCD_D[9] / UPP_XD[1] / **GP7[1]** / BOOT[1] | T1 | I/O | CP[29] | C | |
| VP_DOUT[8] / LCD_D[8] / UPP_XD[0] / **GP7[0]** / BOOT[0] | U3 | I/O | CP[29] | C | |


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**Table 2-29. General Purpose Input Output Terminal Functions (continued)**

| SIGNAL NAME | NO. | TYPE(1) | PULL(2) | POWER GROUP(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **GP8** | | | | | |
| PRU0_R30[25] / MMCSD1_DAT[0] / UPP_CHB_CLOCK / **GP8[15]** / PRU1_R31[27] | G1 | I/O | CP30] | C | GPIO Bank 8 |
| PRU0_R30[24] / MMCSD1_CLK / UPP_CHB_START / **GP8[14]** / PRU1_R31[26] | G2 | I/O | CP[30] | C | |
| PRU0_R30[23] / MMCSD1_CMD / UPP_CHB_ENABLE / **GP8[13]** / PRU1_R31[25] | J4 | I/O | CP[30] | C | |
| PRU0_R30[22] / PRU1_R30[8] / UPP_CHB_WAIT / **GP8[12]** / PRU1_R31[24] | G3 | I/O | CP[30] | C | |
| MMCSD1_DAT[7] / LCD_PCLK / PRU1_R30[7] / **GP8[11]** | F1 | I/O | CP[31] | C | |
| MMCSD1_DAT[6] / LCD_MCLK / PRU1_R30[6] / **GP8[10]** / PRU1_R31[7] | F2 | I/O | CP[31] | C | |
| MMCSD1_DAT[5] / LCD_HSYNC / PRU1_R30[5] / **GP8[9]** / PRU1_R31[6] | H4 | I/O | CP[31] | C | |
| MMCSD1_DAT[4] / LCD_VSYNC / PRU1_R30[4] / **GP8[8]** / PRU1_R31[5] | G4 | I/O | CP[31] | C | |
| AXR0 / ECAP0_APWM0 / **GP8[7]** / MII_TXD[0] / CLKS0 | F3 | I/O | CP[6] | A | |
| SPI0_SOMI / EPWMSYNCI / **GP8[6]** / MII_RXER | C16 | I/O | CP[7] | A | |
| SPI0_SIMO / EPWMSYNCO / **GP8[5]** / MII_CRS | C18 | I/O | CP[7] | A | |
| $\overline{\text{SPI0_SCS[5]}}$ / UART0_RXD / **GP8[4]** / MII_RXD[3] | C19 | I/O | CP[8] | A | |
| $\overline{\text{SPI0_SCS[4]}}$ / UART0_TXD / **GP8[3]** / MII_RXD[2] | D18 | I/O | CP[8] | A | |
| $\overline{\text{SPI0_SCS[3]}}$ / $\overline{\text{UART0_CTS}}$ / **GP8[2]** / MII_RXD[1] / SATA_MP_SWITCH | E17 | I/O | CP[9] | A | |
| $\overline{\text{SPI0_SCS[2]}}$ / $\overline{\text{UART0_RTS}}$ / **GP8[1]** / MII_RXD[0] / SATA_CP_DET | D16 | I/O | CP[9] | A | |
| RTCK / **GP8[0]**(1) | K17 | I/O | IPD | B | |

(1) GP8[0] is initially configured as a reserved function after reset and will not be in a predictable state. This signal will only be stable after the GPIO configuration for this pin has been completed. Users should carefully consider the system implications of this pin being in an unknown state after reset.

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### 2.8.26 Reserved and No Connect

**Table 2-30. Reserved and No Connect Terminal Functions**

| SIGNAL | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **RSV2** | T19 | PWR | Reserved. For proper device operation, this pin must be tied either directly to CVDD or left unconnected (do not connect to ground). |
| **NC** | M3, M14, N16 | — | Pin M3 should be left unconnected (***do not*** connect to power or ground)<br>Pins M14 and N16 may be left unconnected or connected to ground (VSS) |

(1) PWR = Supply voltage.


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### 2.8.27 Supply and Ground

**Table 2-31. Supply and Ground Terminal Functions**

| SIGNAL | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **CVDD** (Core supply) | E15, G7, G8, G13, H6, H7, H10, H11, H12, H13, J6, J12, K6, K12, L12, M8, M9, N8 | PWR | Variable (1.3V - 1.0V) core supply voltage pins |
| **RVDD** (Internal RAM supply) | E5, H14, N7 | PWR | 1.3V internal ram supply voltage pins (for 456 MHz versions)<br>1.2V internal ram supply voltage pins (for 375 MHz versions) |
| **DVDD18** (I/O supply) | F14, G6, G10, G11, G12, J13, K5, L6, P13, R13 | PWR | 1.8V I/O supply voltage pins. DVDD18 must be powered even if all of the DVDD3318_x supplies are operated at 3.3V. |
| **DVDD3318_A** (I/O supply) | F5, F15, G5, G14, G15, H5 | PWR | 1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group A |
| **DVDD3318_B** (I/O supply) | E14, F6, F7, F8, F10, F11, F12, F13, G9, J14, K15 | PWR | 1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group B |
| **DVDD3318_C** (I/O supply) | J5, K13, L4, L13, M13, N13, P5, P6, P12, R4 | PWR | 1.8V or 3.3-V dual-voltage LVCMOS I/O supply voltage pins, Group C |
| **VSS** (Ground) | A19, H8, H9, H15, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, L5, L7, L8, L9, L10, L11, M4, M5, M6, M7, M10, M11, N5, N11, N12, P11 | GND | Ground pins. |
| **USB0_VDDA33** | N18 | PWR | USB0 PHY 3.3-V supply |
| **USB0_VDDA18** | N14 | PWR | USB0 PHY 1.8-V supply input |
| **USB0_VDDA12** | N17 | A | USB0 PHY 1.2-V LDO output for bypass cap |
| **USB_CVDD** | M12 | PWR | USB0 core logic 1.2-V supply input |
| **USB1_VDDA33** | P15 | PWR | USB1 PHY 3.3-V supply |
| **USB1_VDDA18** | P14 | PWR | USB1 PHY 1.8-V supply |
| **SATA_VDD** | M2, N4, P1, P2 | PWR | SATA PHY 1.2V logic supply |
| **SATA_VSS** | H1, H2, K1, K2, L3, M1 | GND | SATA PHY ground reference |
| **DDR_DVDD18** | N6, N9, N10, P7, P8, P9, P10, R7, R8, R9 | PWR | DDR PHY 1.8V power supply pins |

(1) PWR = Supply voltage, GND - Ground.

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## 2.9 Unused Pin Configurations

All signals multiplexed with multiple functions may be used as an alternate function if a given peripheral is not used. Unused non-multiplexed signals and some other specific signals should be handled as specified in the tables below.

If NMI is unused, it should be pulled-high externally through a 10k-ohm resistor to supply DVDD3318_B.

**Table 2-32. Unused USB0 and USB1 Signal Configurations**

| SIGNAL NAME | Configuration (When USB0 and USB1 are not used) | Configuration (When only USB1 is not used) |
|---|---|---|
| USB0_DM | No Connect | Use as USB0 function |
| USB0_DP | No Connect | Use as USB0 function |
| USB0_ID | No Connect | Use as USB0 function |
| USB0_VBUS | No Connect | Use as USB0 function |
| USB0_DRVVBUS | No Connect | Use as USB0 function |
| USB0_VDDA33 | No Connect | 3.3V |
| USB0_VDDA18 | No Connect | 1.8V |
| USB0_VDDA12 | No Connect | Internal USB PHY output connected to an external filter capacitor |
| USB1_DM | No Connect | VSS or No Connect |
| USB1_DP | No Connect | VSS or No Connect |
| USB1_VDDA33 | No Connect | No Connect |
| USB1_VDDA18 | No Connect | No Connect |
| USB_REFCLKIN | No Connect or other peripheral function | Use for USB0 or other peripheral function |
| USB_CVDD | 1.2V | 1.2V |

**Table 2-33. Unused SATA Signal Configuration**

| SIGNAL NAME | Configuration |
|---|---|
| SATA_RXP | No Connect |
| $\overline{\text{SATA_RXN}}$ | No Connect |
| SATA_TXP | No Connect |
| $\overline{\text{SATA_TXN}}$ | No Connect |
| SATA_REFCLKP | No Connect |
| $\overline{\text{SATA_REFCLKN}}$ | No Connect |
| SATA_MP_SWITCH | May be used as GPIO or other peripheral function |
| SATA_CP_DET | May be used as GPIO or other peripheral function |
| SATA_CP_POD | May be used as GPIO or other peripheral function |
| SATA_LED | May be used as GPIO or other peripheral function |
| SATA_REG | No Connect |
| SATA_VDDR | No Connect |
| SATA_VDD | Prior to silicon revision 2.0, this supply must be connected to a static 1.2V nominal supply. For silicon revision 2.0 and later, this supply may be left unconnected for additional power conservation. |
| SATA_VSS | VSS |

**Table 2-34. Unused RTC Signal Configuration**

| SIGNAL NAME | Configuration |
|---|---|
| RTC_XI | May be held high (CVDD) or low |
| $\overline{\text{RTC_XO}}$ | No Connect |
| RTC_ALARM | May be used as GPIO or other peripheral function |


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**Table 2-34. Unused RTC Signal Configuration (continued)**

| SIGNAL NAME | Configuration |
|---|---|
| RTC_CVDD | Connect to CVDD |
| RTC_VSS | VSS |

**Table 2-35. Unused DDR2/mDDR Controller Signal Configuration**

| SIGNAL NAME | Configuration (1) |
|---|---|
| DDR_D[15:0] | No Connect |
| DDR_A[13:0] | No Connect |
| DDR_CLKP | No Connect |
| DDR_CLKN | No Connect |
| DDR_CKE | No Connect |
| DDR_WE | No Connect |
| DDR_RAS | No Connect |
| DDR_CAS | No Connect |
| DDS_CS | No Connect |
| DDR_DQM[1:0] | No Connect |
| DDR_DQS[1:0] | No Connect |
| DDR_BA[2:0] | No Connect |
| DDR_DQGATE0 | No Connect |
| DDR_DQGATE1 | No Connect |
| DDR_ZP | No Connect |
| DDR_VREF | No Connect |
| DDR_DVDD18 | No Connect |

(1) To minimize power consumption, the DDR2/mDDR controller input receivers should be placed in power-down mode by setting VTPIO[14]=1.

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# 3 Device Configuration

## 3.1 Boot Modes

This device supports a variety of boot modes through an internal ARM ROM bootloader . This device does not support dedicated hardware boot modes; therefore, all boot modes utilize the internal ARM ROM . The input states of the BOOT pins are sampled and latched into the BOOTCFG register, which is part of the system configuration (SYSCFG) module, when device reset is deasserted. Boot mode selection is determined by the values of the BOOT pins.

See *Using the OMAP-L1x8 Bootloader Application Report* (SPRAB41) for more details on the ROM Boot Loader.

The following boot modes are supported:

- NAND Flash boot
  - 8-bit NAND
  - 16-bit NAND (supported on ROM revisions after d800k002 -- see the bootloader documents mentioned above to determine the ROM revision)
- NOR Flash boot
  - NOR Direct boot (8-bit or 16-bit)
  - NOR Legacy boot (8-bit or 16-bit)
  - NOR AIS boot (8-bit or 16-bit)
- HPI Boot
- I2C0/I2C1 Boot
  - EEPROM (Master Mode)
  - External Host (Slave Mode)
- SPI0/SPI1 Boot
  - Serial Flash (Master Mode)
  - SERIAL EEPROM (Master Mode)
  - External Host (Slave Mode)
- UART0/UART1/UART2 Boot
  - External Host

## 3.2 SYSCFG Module

The following system level features of the chip are controlled by the SYSCFG peripheral:

- Readable Device, Die, and Chip Revision ID
- Control of Pin Multiplexing
- Priority of bus accesses different bus masters in the system
- Capture at power on reset the chip BOOT pin values and make them available to software
- Control of the DeepSleep power management function
- Enable and selection of the programmable pin pullups and pulldowns


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- Special case settings for peripherals:
  - Locking of PLL controller settings
  - Default burst sizes for EDMA3 transfer controllers
  - Selection of the source for the eCAP module input capture (including on chip sources)
  - McASP AMUTEIN selection and clearing of AMUTE status for the McASP
  - Control of the reference clock source and other side-band signals for both of the integrated USB PHYs
  - Clock source selection for EMIFA
  - DDR2 Controller PHY settings
  - SATA PHY power management controls
- Selects the source of emulation suspend signal (from either ARM or DSP) of peripherals supporting this function.
- Control of on-chip inter-processor interrupts for signaling between ARM and DSP

Many registers are accessible only by a host (ARM or DSP) when it is operating in its privileged mode. (ex. from the kernel, but not from user space code).

**Table 3-1. System Configuration (SYSCFG) Module Register Access**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | REGISTER ACCESS |
|---|---|---|---|
| 0x01C1 4000 | REVID | Revision Identification Register | — |
| 0x01C1 4008 | DIEIDR0 | Device Identification Register 0 | — |
| 0x01C1 400C | DIEIDR1 | Device Identification Register 1 | — |
| 0x01C1 4010 | DIEIDR2 | Device Identification Register 2 | — |
| 0x01C1 4014 | DIEIDR3 | Device Identification Register 3 | — |
| 0x01C1 4020 | BOOTCFG | Boot Configuration Register | Privileged mode |
| 0x01C1 4038 | KICK0R | Kick 0 Register | Privileged mode |
| 0x01C1 403C | KICK1R | Kick 1 Register | Privileged mode |
| 0x01C1 4040 | HOST0CFG | Host 0 Configuration Register | — |
| 0x01C1 4044 | HOST1CFG | Host 1 Configuration Register | — |
| 0x01C1 40E0 | IRAWSTAT | Interrupt Raw Status/Set Register | Privileged mode |
| 0x01C1 40E4 | IENSTAT | Interrupt Enable Status/Clear Register | Privileged mode |
| 0x01C1 40E8 | IENSET | Interrupt Enable Register | Privileged mode |
| 0x01C1 40EC | IENCLR | Interrupt Enable Clear Register | Privileged mode |
| 0x01C1 40F0 | EOI | End of Interrupt Register | Privileged mode |
| 0x01C1 40F4 | FLTADDRR | Fault Address Register | Privileged mode |
| 0x01C1 40F8 | FLTSTAT | Fault Status Register | — |
| 0x01C1 4110 | MSTPRI0 | Master Priority 0 Registers | Privileged mode |
| 0x01C1 4114 | MSTPRI1 | Master Priority 1 Registers | Privileged mode |
| 0x01C1 4118 | MSTPRI2 | Master Priority 2 Registers | Privileged mode |
| 0x01C1 4120 | PINMUX0 | Pin Multiplexing Control 0 Register | Privileged mode |
| 0x01C1 4124 | PINMUX1 | Pin Multiplexing Control 1 Register | Privileged mode |
| 0x01C1 4128 | PINMUX2 | Pin Multiplexing Control 2 Register | Privileged mode |
| 0x01C1 412C | PINMUX3 | Pin Multiplexing Control 3 Register | Privileged mode |
| 0x01C1 4130 | PINMUX4 | Pin Multiplexing Control 4 Register | Privileged mode |
| 0x01C1 4134 | PINMUX5 | Pin Multiplexing Control 5 Register | Privileged mode |
| 0x01C1 4138 | PINMUX6 | Pin Multiplexing Control 6 Register | Privileged mode |
| 0x01C1 413C | PINMUX7 | Pin Multiplexing Control 7 Register | Privileged mode |
| 0x01C1 4140 | PINMUX8 | Pin Multiplexing Control 8 Register | Privileged mode |
| 0x01C1 4144 | PINMUX9 | Pin Multiplexing Control 9 Register | Privileged mode |
| 0x01C1 4148 | PINMUX10 | Pin Multiplexing Control 10 Register | Privileged mode |

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**Table 3-1. System Configuration (SYSCFG) Module Register Access (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | REGISTER ACCESS |
|---|---|---|---|
| 0x01C1 414C | PINMUX11 | Pin Multiplexing Control 11 Register | Privileged mode |
| 0x01C1 4150 | PINMUX12 | Pin Multiplexing Control 12 Register | Privileged mode |
| 0x01C1 4154 | PINMUX13 | Pin Multiplexing Control 13 Register | Privileged mode |
| 0x01C1 4158 | PINMUX14 | Pin Multiplexing Control 14 Register | Privileged mode |
| 0x01C1 415C | PINMUX15 | Pin Multiplexing Control 15 Register | Privileged mode |
| 0x01C1 4160 | PINMUX16 | Pin Multiplexing Control 16 Register | Privileged mode |
| 0x01C1 4164 | PINMUX17 | Pin Multiplexing Control 17 Register | Privileged mode |
| 0x01C1 4168 | PINMUX18 | Pin Multiplexing Control 18 Register | Privileged mode |
| 0x01C1 416C | PINMUX19 | Pin Multiplexing Control 19 Register | Privileged mode |
| 0x01C1 4170 | SUSPSRC | Suspend Source Register | Privileged mode |
| 0x01C1 4174 | CHIPSIG | Chip Signal Register | — |
| 0x01C1 4178 | CHIPSIG_CLR | Chip Signal Clear Register | — |
| 0x01C1 417C | CFGCHIP0 | Chip Configuration 0 Register | Privileged mode |
| 0x01C1 4180 | CFGCHIP1 | Chip Configuration 1 Register | Privileged mode |
| 0x01C1 4184 | CFGCHIP2 | Chip Configuration 2 Register | Privileged mode |
| 0x01C1 4188 | CFGCHIP3 | Chip Configuration 3 Register | Privileged mode |
| 0x01C1 418C | CFGCHIP4 | Chip Configuration 4 Register | Privileged mode |
| 0x01E2 C000 | VTPIO_CTL | VTPIO COntrol Register | Privileged mode |
| 0x01E2 C004 | DDR_SLEW | DDR Slew Register | Privileged mode |
| 0x01E2 C008 | DeepSleep | DeepSleep Register | Privileged mode |
| 0x01E2 C00C | PUPD_ENA | Pullup / Pulldown Enable Register | Privileged mode |
| 0x01E2 C010 | PUPD_SEL | Pullup / Pulldown Selection Register | Privileged mode |
| 0x01E2 C014 | RXACTIVE | RXACTIVE Control Register | Privileged mode |
| 0x01E2 C018 | PWRDN | PWRDN Control Register | Privileged mode |


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## 3.3 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the device always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The device features internal pullup (IPU) and internal pulldown (IPD) resistors on most pins to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor needs to be used in the following situations:

- Boot and Configuration Pins: If the pin is both routed out and 3-stated (not driven), an external pullup/pulldown resistor is strongly recommended, even if the IPU/IPD matches the desired value/state.
- Other Input Pins: If the IPU/IPD does not match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the boot and configuration pins, if they are both routed out and 3-stated (not driven), it is strongly recommended that an external pullup/pulldown resistor be implemented. Although, internal pullup/pulldown resistors exist on these pins and they may match the desired configuration value, providing external connectivity can help ensure that valid logic levels are latched on these device boot and configuration pins. In addition, applying external pullup/pulldown resistors on the boot and configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest $V_{IL}$ level of all inputs connected to the net. For a pullup resistor, this should be above the highest $V_{IH}$ level of all inputs on the net. A reasonable choice would be to target the $V_{OL}$ or $V_{OH}$ levels for the logic family of the limiting device; which, by definition, have margin to the $V_{IL}$ and $V_{IH}$ levels.
- Select a pullup/pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the IO supply rail.
- For most systems, a 1-kΩ resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.
- For most systems, a 20-kΩ resistor can be used to compliment the IPU/IPD on the boot and configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.
- For more detailed information on input current ($I_I$), and the low-/high-level input voltages ($V_{IL}$ and $V_{IH}$) for the device, see Section 4.2, Recommended Operating Conditions.
- For the internal pullup/pulldown resistors for all device pins, see the peripheral/system-specific terminal functions table.

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# 4 Device Operating Conditions

## 4.1 Absolute Maximum Ratings Over Operating Junction Temperature Range (Unless Otherwise Noted) (1)

| | | |
|---|---|---|
| Supply voltage ranges | Core Logic, Variable and Fixed (CVDD, RVDD, RTC_CVDD, PLL0_VDDA , PLL1_VDDA , SATA_VDD, USB_CVDD )(2) | -0.5 V to 1.4 V |
| | I/O, 1.8V (USB0_VDDA18, USB1_VDDA18, SATA_VDDR, DDR_DVDD18)(2) | -0.5 V to 2 V |
| | I/O, 3.3V (DVDD3318_A, DVDD3318_B, DVDD3318_C, USB0_VDDA33, USB1_VDDA33)(2) | -0.5 V to 3.8V |
| Input voltage ($V_I$) ranges | Oscillator inputs (OSCIN, RTC_XI), 1.2V | -0.3 V to CVDD + 0.3V |
| | Dual-voltage LVCMOS inputs, 3.3V or 1.8V (Steady State) | -0.3V to DVDD + 0.3V |
| | Dual-voltage LVCMOS inputs, operated at 3.3V(Transient) | DVDD + 20% up to 20% of Signal Period |
| | Dual-voltage LVCMOS inputs, operated at 1.8V(Transient) | DVDD + 30% up to 30% of Signal Period |
| | USB 5V Tolerant IOs: (USB0_DM, USB0_DP, USB0_ID, USB1_DM, USB1_DP) | 5.25V(3) |
| | USB0 VBUS Pin | 5.50V(3) |
| Output voltage ($V_O$) ranges | Dual-voltage LVCMOS outputs, 3.3V or 1.8V (Steady State) | -0.5 V to DVDD + 0.3V |
| | Dual-voltage LVCMOS outputs, operated at 3.3V(Transient) (Transient) | DVDD + 20% up to 20% of Signal Period |
| | Dual-voltage LVCMOS outputs, operated at 1.8V(Transient) (Transient) | DVDD + 30% up to 30% of Signal Period |
| Clamp Current | Input or Output Voltages 0.3V above or below their respective power rails. Limit clamp current that flows through the I/O's internal diode protection cells. | ±20mA |
| Operating Junction Temperature ranges, $T_J$ | Commercial (default) | 0°C to 90°C |
| | Industrial (D suffix) | -40°C to 90°C |
| | Extended (A suffix) | -40°C to 105°C |
| Storage temperature range, $T_{stg}$ | (default) | -55°C to 150°C |
| ESD Stress Voltage, $V_{ESD}$ (4) | Human Body Model (HBM) (5) | >1000 V |
| | Charged Device Model (CDM) (6) | >500 V |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VSS, USB0_VSSA33, USB0_VSSA, PLL0_VSSA, OSCVSS, RTC_VSS
(3) Up to a maximum of 24 hours.
(4) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
(5) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001-2010. JEDEC document JEP 155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Pins listed as 1000V may actually have higher performance.
(6) Level listed above is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP 157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250V may actually have higher performance.


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## 4.2 Recommended Operating Conditions

| | NAME | DESCRIPTION | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Supply Voltage | CVDD | Core Logic Supply Voltage (variable) | 1.3V operating point | 1.25 | 1.3 | 1.35 | V |
| | | | 1.2V operating point | 1.14 | 1.2 | 1.32 | |
| | | | 1.1V operating point | 1.05 | 1.1 | 1.16 | |
| | | | 1.0V operating point | 0.95 | 1.0 | 1.05 | |
| | RVDD | Internal RAM Supply Voltage | 456 MHz versions | 1.25 | 1.3 | 1.35 | V |
| | | | 375 MHz versions | 1.14 | 1.2 | 1.32 | |
| | RTC_CVDD (1) | RTC Core Logic Supply Voltage | | 0.9 | 1.2 | 1.32 | V |
| | PLL0_VDDA | PLL0 Supply Voltage | | 1.14 | 1.2 | 1.32 | V |
| | PLL1_VDDA | PLL1 Supply Voltage | | 1.14 | 1.2 | 1.32 | V |
| | SATA_VDD | SATA Core Logic Supply Voltage | | 1.14 | 1.2 | 1.32 | V |
| | USB_CVDD | USB0, USB1 Core Logic Supply Voltage | | 1.14 | 1.2 | 1.32 | V |
| | USB0_VDDA18 | USB0 PHY Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| | USB0_VDDA33 | USB0 PHY Supply Voltage | | 3.15 | 3.3 | 3.45 | V |
| | USB1_VDDA18 | USB1 PHY Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| | USB1_VDDA33 | USB1 PHY Supply Voltage | | 3.15 | 3.3 | 3.45 | V |
| | DVDD18(2) | 1.8V Logic Supply | | 1.71 | 1.8 | 1.89 | V |
| | SATA_VDDR | SATA PHY Internal Regulator Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| | DDR_DVDD18(2) | DDR2 PHY Supply Voltage | | 1.71 | 1.8 | 1.89 | V |
| | DDR_VREF | DDR2/mDDR reference voltage | | 0.49* DDR_DVDD18 | 0.5* DDR_DVDD18 | 0.51* DDR_DVDD18 | V |
| | DDR_ZP | DDR2/mDDR impedance control, connected via 50Ω resistor to Vss | | | Vss | | V |
| | DVDD3318_A | Power Group A Dual-voltage IO Supply Voltage | 1.8V operating point | 1.71 | 1.8 | 1.89 | V |
| | | | 3.3V operating point | 3.15 | 3.3 | 3.45 | V |
| | DVDD3318_B | Power Group B Dual-voltage IO Supply Voltage | 1.8V operating point | 1.71 | 1.8 | 1.89 | V |
| | | | 3.3V operating point | 3.15 | 3.3 | 3.45 | V |
| | DVDD3318_C | Power Group C Dual-voltage IO Supply Voltage | 1.8V operating point | 1.71 | 1.8 | 1.89 | V |
| | | | 3.3V operating point | 3.15 | 3.3 | 3.45 | V |
| Supply Ground | VSS | Core Logic Digital Ground | | 0 | 0 | 0 | V |
| | PLL0_VSSA | PLL0 Ground | | | | | |
| | PLL1_VSSA | PLL1 Ground | | | | | |
| | SATA_VSS | SATA PHY Ground | | | | | |
| | OSCVSS(3) | Oscillator Ground | | | | | |
| | RTC_VSS(3) | RTC Oscillator Ground | | | | | |
| | USB0_VSSA | USB0 PHY Ground | | | | | |
| | USB0_VSSA33 | USB0 PHY Ground | | | | | |
| Voltage Input High | $V_{IH}$ | High-level input voltage, Dual-voltage I/O, 3.3V(4) | | 2 | | | V |
| | | High-level input voltage, Dual-voltage I/O, 1.8V (4) | | 0.65*DVDD | | | V |
| | | High-level input voltage, RTC_XI | | 0.8*RTC_CVDD | | | V |
| | | High-level input voltage, OSCIN | | 0.8*CVDD | | | V |
| Voltage Input Low | $V_{IL}$ | Low-level input voltage, Dual-voltage I/O, 3.3V(4) | | | | 0.8 | V |
| | | Low-level input voltage, Dual-voltage I/O, 1.8V (4) | | | | 0.35*DVDD | V |
| | | Low-level input voltage, RTC_XI | | | | 0.2*RTC_CVDD | V |
| | | Low-level input voltage, OSCIN | | | | 0.2*CVDD | V |

(1) The RTC provides an option for isolating the RTC_CVDD from the CVDD to reduce current leakage when the RTC is powered independently. If these power supplies are not isolated (CTRL.SPLITPOWER=0), RTC_CVDD must be equal to or greater than CVDD. If these power supplies are isolated (CTRL.SPLITPOWER=1), RTC_CVDD may be lower than CVDD.
(2) DVDD18 must be powered even if all of the DVDD3318_x supplies are operated at 3.3V.
(3) When an external crystal is used oscillator (OSC_VSS, RTC_VSS) ground must be kept separate from other grounds and connected directly to the crystal load capacitor ground. These pins are shorted to VSS on the device itself and should not be connected to VSS on the circuit board. If a crystal is not used and the clock input is driven directly, then the oscillator VSS may be connected to board ground.
(4) These IO specifications apply to the dual-voltage IOs only and do not apply to DDR2/mDDR or SATA interfaces. DDR2/mDDR IOs are 1.8V IOs and adhere to the JESD79-2A standard.

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## Recommended Operating Conditions *(continued)*

| | NAME | DESCRIPTION | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| USB | USB0_VBUS | USB external charge pump input | | 0 | | 5.25 | V |
| Differential Clock Input Voltage | | Differential input voltage, SATA_REFCLKP and $\overline{\text{SATA_REFCLKN}}$ | | 250 | | 2000 | mV |
| Transition Time | $t_t$ | Transition time, 10%-90%, All Inputs (unless otherwise specified in the electrical data sections) | | | | 0.25P or 10 (5) | ns |
| Operating Frequency | $F_{PLL0_SYSCLK1,6}$ | Commercial temperature grade (default) | CVDD = 1.3V operating point | 0 | | 456 (6) | MHz |
| | | | CVDD = 1.2V operating point | 0 | | 375 (7) | |
| | | | CVDD = 1.1V operating point | 0 | | 200 (6) | |
| | | | CVDD = 1.0V operating point | 0 | | 100 (6) | |
| | | Industrial temperature grade (D suffix) | CVDD = 1.3V operating point | 0 | | 456 (6) | MHz |
| | | | CVDD = 1.2V operating point | 0 | | 375 (7) | |
| | | | CVDD = 1.1V operating point | 0 | | 200 (6) | |
| | | | CVDD = 1.0V operating point | 0 | | 100 (6) | |
| | | Extended temperature grade (A suffix) | CVDD = 1.2V operating point | 0 | | 375 (7) | MHz |
| | | | CVDD = 1.1V operating point | 0 | | 200 (6) | |
| | | | CVDD = 1.0V operating point | 0 | | 100 (6) | |

(5) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.
(6) This operating point is not supported on revision 1.x silicon.
(7) This operating point is 300 MHz on revision 1.x silicon.


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## 4.3 Notes on Recommended Power-On Hours (POH)

**The information in the section below is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.**

To avoid significant degradation, the device power-on hours (POH) must be limited to the following:

**Table 4-1. Recommended Power-On Hours**

| Silicon Revision | Speed Grade | Operating Junction Temperature (Tj) | Nominal CVDD Voltage (V) | Power-On Hours [POH] (hours) |
|---|---|---|---|---|
| A | 300 MHZ | 0 to 90 °C | 1.2V | 100,000 |
| B | 300 MHz | 0 to 90 °C | 1.2V | 100,000 |
| B | 375 MHz | 0 to 90 °C | 1.2V | 100,000 |
| B | 375 MHz | -40 to 105 °C | 1.2V | 75,000 (1) |
| B | 456 MHz | 0 to 90 °C | 1.3V | 100,000 |
| B | 456 MHz | -40 to 90 °C | 1.3V | 100,000 |

(1) 100,000 POH can be achieved at this temperature condition if the device operation is limited to 345 MHz

**Note:** Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

**The above notations cannot be deemed a warranty or deemed to extend or modify the warranty under TI's standard terms and conditions for TI semiconductor products.**

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## 4.4 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Junction Temperature (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage (dual-voltage LVCMOS IOs at 3.3V)(1) | DVDD= 3.15V, $I_{OH}$ = -4 mA | 2.4 | | | V |
| | | DVDD= 3.15V, $I_{OH}$ = -100 µA | 2.95 | | | V |
| | High-level output voltage (dual-voltage LVCMOS IOs at 1.8V)(1) | DVDD= 1.71V, $I_{OH}$ = -2 mA | DVDD-0.45 | | | V |
| $V_{OL}$ | Low-level output voltage (dual-voltage LVCMOS I/Os at 3.3V) | DVDD= 3.15V, $I_{OL}$ = 4mA | | | 0.4 | V |
| | | DVDD= 3.15V, $I_{OL}$ = 100 µA | | | 0.2 | V |
| | Low-level output voltage (dual-voltage LVCMOS I/Os at 1.8V) | DVDD= 1.71V, $I_{OL}$ = 2mA | | | 0.45 | V |
| $I_I$ (2) | Input current(1) (dual-voltage LVCMOS I/Os) | $V_I$ = VSS to DVDD without opposing internal resistor | | | ±9 | µA |
| | | $V_I$ = VSS to DVDD with opposing internal pullup resistor (3) | 70 | | 310 | µA |
| | | $V_I$ = VSS to DVDD with opposing internal pulldown resistor (3) | -75 | | -270 | µA |
| | Input current (DDR2/mDDR I/Os) | $V_I$ = VSS to DVDD with opposing internal pulldown resistor (3) | -77 | | -286 | µA |
| $I_{OH}$ | High-level output current(1) (dual-voltage LVCMOS I/Os) | | | | -6 | mA |
| $I_{OL}$ | Low-level output current(1) (dual-voltage LVCMOS I/Os) | | | | 6 | mA |
| Capacitance | Input capacitance (dual-voltage LVCMOS) | | | 3 | | pF |
| | Output capacitance (dual-voltage LVCMOS) | | | 3 | | pF |

(1) These IO specifications apply to the dual-voltage IOs only and do not apply to DDR2/mDDR or SATA interfaces. DDR2/mDDR IOs are 1.8V IOs and adhere to the JESD79-2A standard. USB0 I/Os adhere to the USB2.0 standard. USB1 I/Os adhere to the USB1.1 standard. SATA I/Os adhere to the SATA-I and SATA-II standards.

(2) $I_I$ applies to input-only pins and bi-directional pins. For input-only pins, $I_I$ indicates the input leakage current. For bi-directional pins, $I_I$ indicates the input leakage current and off-state (Hi-Z) output leakage current.

(3) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor. The pull-up and pull-down strengths shown represent the minimum and maximum strength across process variation.


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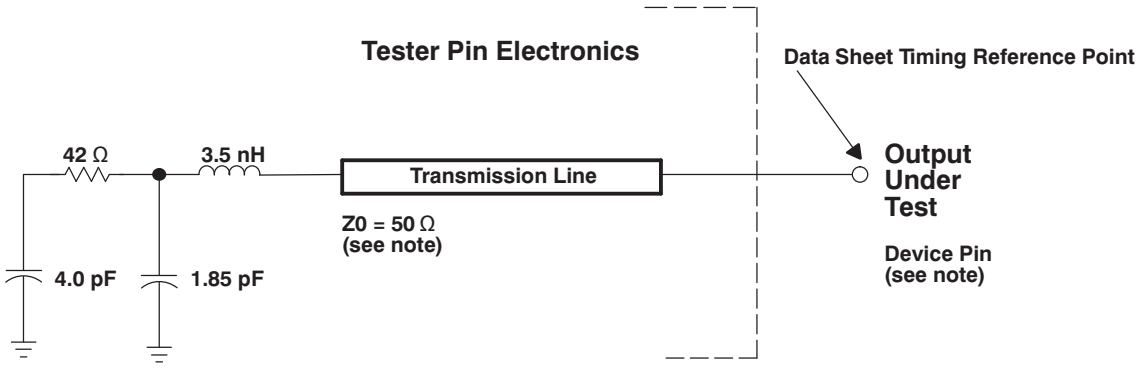
# 5 Peripheral Information and Electrical Specifications

## 5.1 Parameter Information

### *5.1.1 Parameter Information Device-Specific Information*




A. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin and the input signals are driven between 0V and the appropriate IO supply rail for the signal.

**Figure 5-1. Test Load Circuit for AC Timing Measurements**

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

#### 5.1.1.1 Signal Transition Levels

All input and output timing parameters are referenced to $V_{ref}$ for both "0" and "1" logic levels.

For 3.3 V I/O, $V_{ref}$ = 1.65 V.

For 1.8 V I/O, $V_{ref}$ = 0.9 V.

For 1.2 V I/O, $V_{ref}$ = 0.6 V.

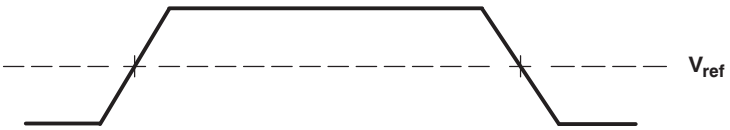



**Figure 5-2. Input and Output Voltage Reference Levels for AC Timing Measurements**

All rise and fall transition timing parameters are referenced to $V_{IL}$ MAX and $V_{IH}$ MIN for input clocks, $V_{OL}$MAX and $V_{OH}$ MIN for output clocks

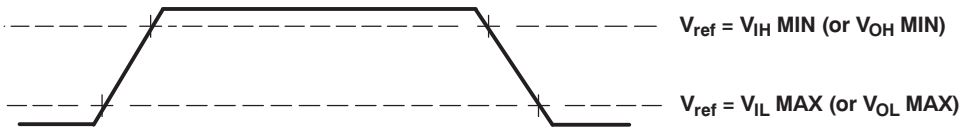



**Figure 5-3. Rise and Fall Transition Time Voltage Reference Levels**

## 5.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals ***must*** transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.

## 5.3 Power Supplies

### *5.3.1 Power-On Sequence*

The device should be powered-on in the following order:

1. RTC (RTC_CVDD) may be powered from an external device (such as a battery) prior to all other supplies being applied or powered-up at the same time as CVDD. If the RTC is not used, RTC_CVDD should be connected to CVDD. RTC_CVDD should not be left unpowered while CVDD is powered.
2. Core logic supplies:
   (a) All variable 1.3V - 1.0V core logic supplies (CVDD)
   (b) All static core logic supplies (RVDD, PLL0_VDDA, PLL1_VDDA, USB_CVDD, SATA_VDD). If voltage scaling is not used on the device, groups 2a) and 2b) can be controlled from the same power supply and powered up together.
3. All static 1.8V IO supplies (DVDD18, DDR_DVDD18, USB0_VDDA18, USB1_VDDA18 and SATA_VDDR) and any of the LVCMOS IO supply groups used at 1.8V nominal (DVDD3318_A, DVDD3318_B, or DVDD3318_C).
4. All analog 3.3V PHY supplies (USB0_VDDA33 and USB1_VDDA33; these are not required if both USB0 and USB1 are not used) and any of the LVCMOS IO supply groups used at 3.3V nominal (DVDD3318_A, DVDD3318_B, or DVDD3318_C).

There is no specific required voltage ramp rate for any of the supplies as long as the LVCMOS supplies operated at 3.3V (DVDD3318_A, DVDD3318_B, or DVDD3318_C) never exceed the STATIC 1.8V supplies by more than 2 volts.

RESET must be maintained active until all power supplies have reached their nominal values.

### *5.3.2 Power-Off Sequence*

The power supplies can be powered-off in any order as long as LVCMOS supplies operated at 3.3V (DVDD3318_A, DVDD3318_B, or DVDD3318_C) never exceed static 1.8V supplies by more than 2 volts. There is no specific required voltage ramp down rate for any of the supplies (except as required to meet the above mentioned voltage condition).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## 5.4 Reset

### 5.4.1 Power-On Reset (POR)

A power-on reset (POR) is required to place the device in a known good state after power-up. Power-On Reset is initiated by bringing RESET and TRST low at the same time. POR sets all of the device internal logic to its default state. All pins are tri-stated with the exception of RESETOUT which remains active through the reset sequence. RESETOUT is an output for use by other controllers in the system that indicates the device is currently in reset.

RTCK is maintained active through a POR.

A summary of the effects of Power-On Reset is given below:

- All internal logic (including emulation logic and the PLL logic) is reset to its default state
- Internal memory is not maintained through a POR
- RESETOUT goes active
- All device pins go to a high-impedance state
- The RTC peripheral is not reset during a POR. A software sequence is required to reset the RTC

A watchdog reset triggers a POR.

### 5.4.2 Warm Reset

A warm reset provides a limited reset to the device. Warm Reset is initiated by bringing only RESET low (TRST is maintained high through a warm reset). Warm reset sets certain portions of the device to their default state while leaving others unaltered. All pins are tri-stated with the exception of RESETOUT which remains active through the reset sequence. RESETOUT is an output for use by other controllers in the system that indicates the device is currently in reset.

RTCK is maintained active through a POR.

A summary of the effects of Warm Reset is given below:

- All internal logic (except for the emulation logic and the PLL logic) is reset to its default state
- Internal memory is maintained through a warm reset
- RESETOUT goes active
- All device pins go to a high-impedance state
- The RTC peripheral is not reset during a warm reset. A software sequence is required to reset the RTC

### 5.4.3 Reset Electrical Data Timings

Table 5-1 assumes testing over the recommended operating conditions.

**Table 5-1. Reset Timing Requirements ((1), (2))**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{w(RSTL)}$ | Pulse width, $\overline{RESET}$/$\overline{TRST}$ low | 100 | | 100 | | 100 | | ns |
| 2 | $t_{su(BPV-RSTH)}$ | Setup time, boot pins valid before $\overline{RESET}$/$\overline{TRST}$ high | 20 | | 20 | | 20 | | ns |
| 3 | $t_{h(RSTH-BPV)}$ | Hold time, boot pins valid after $\overline{RESET}$/$\overline{TRST}$ high | 20 | | 20 | | 20 | | ns |
| 4 | $t_{d(RSTH-RESETOUTH)}$ | $\overline{RESET}$ high to $\overline{RESETOUT}$ high; Warm reset | | 14 | | 16 | | 20 | cycles(3) |
| | | $\overline{RESET}$ high to $\overline{RESETOUT}$ high; Power-on Reset | | 14 | | 16 | | 20 | |
| 5 | $t_{d(RSTL-RESETOUTL)}$ | Delay time, $\overline{RESET}$/$\overline{TRST}$ low to $\overline{RESETOUT}$ low | | 14 | | 16 | | 20 | ns |

(1) $\overline{RESETOUT}$ is multiplexed with other pin functions. See the Terminal Functions table, Table 2-5 for details.
(2) For power-on reset (POR), the reset timings in this table refer to $\overline{RESET}$ and $\overline{TRST}$ together. For warm reset, the reset timings in this table refer to $\overline{RESET}$ only ($\overline{TRST}$ is held high).
(3) OSCIN cycles.

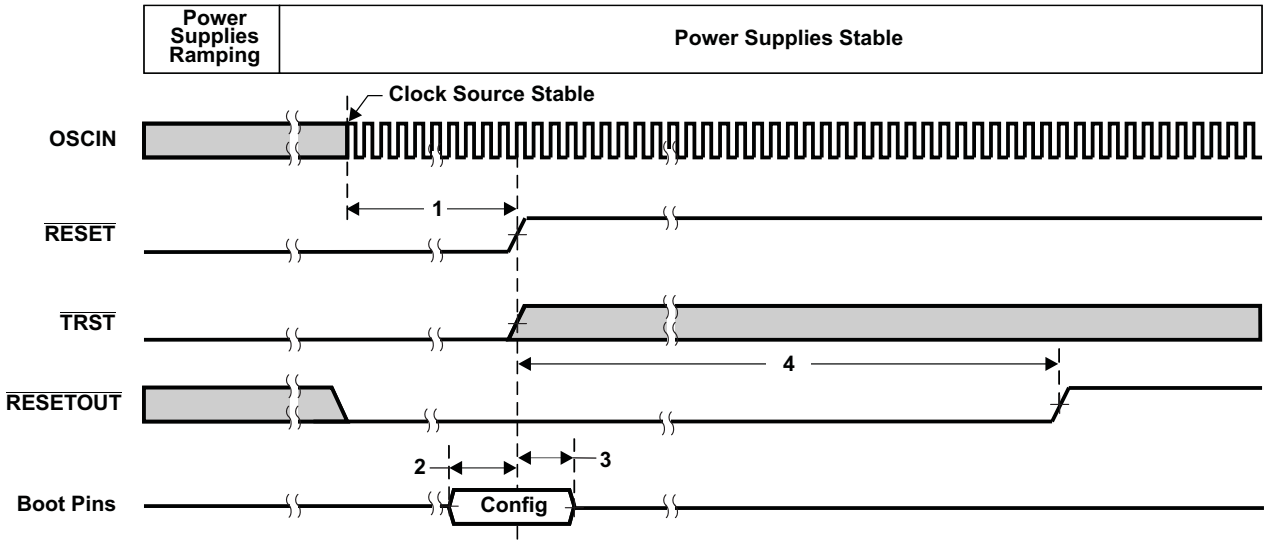


**Figure 5-4. Power-On Reset (RESET and TRST active) Timing**


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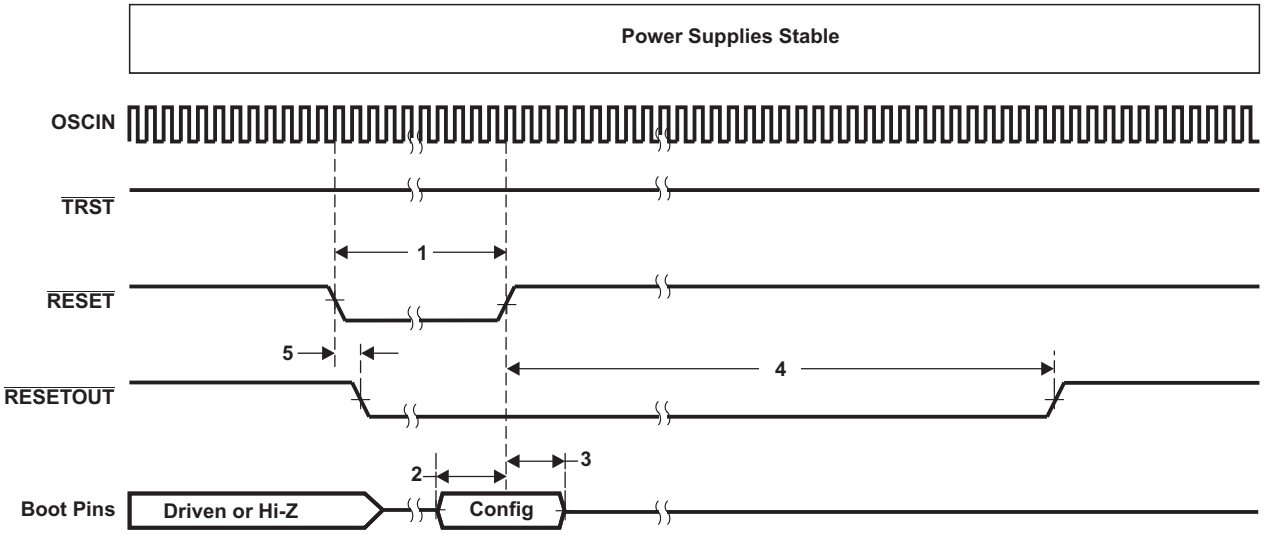


**Figure 5-5. Warm Reset (RESET active, TRST high) Timing**

## 5.5 Crystal Oscillator or External Clock Input

The device includes two choices to provide an external clock input, which is fed to the on-chip PLLs to generate high-frequency system clocks. These options are illustrated in Figure 5-6 and Figure 5-7. For input clock frequencies between 12 and 20 MHz, a crystal with 80 ohm max ESR is recommended. For input clock frequencies between 20 and 30 MHz, a crystal with 60 ohm max ESR is recommended. Typical load capacitance values are 10-20 pF, where the load capacitance is the series combination of C1 and C2.

Figure 5-6 illustrates the option that uses on-chip 1.2V oscillator with external crystal circuit. Figure 5-7 illustrates the option that uses an external 1.2V clock input.

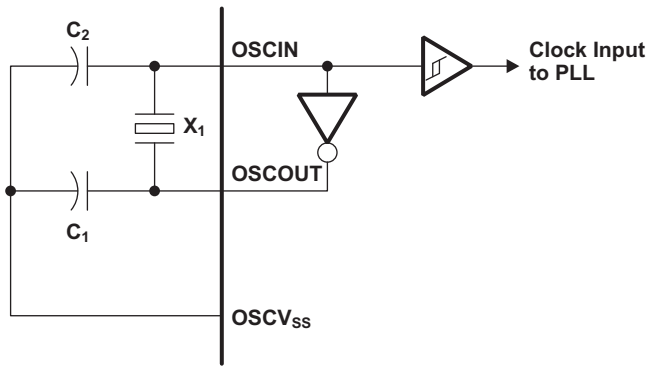


**Figure 5-6. On-Chip Oscillator**

**Table 5-2. Oscillator Timing Requirements**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{osc}$ | Oscillator frequency range (OSCIN/OSCOUT) | 12 | 30 | MHz |


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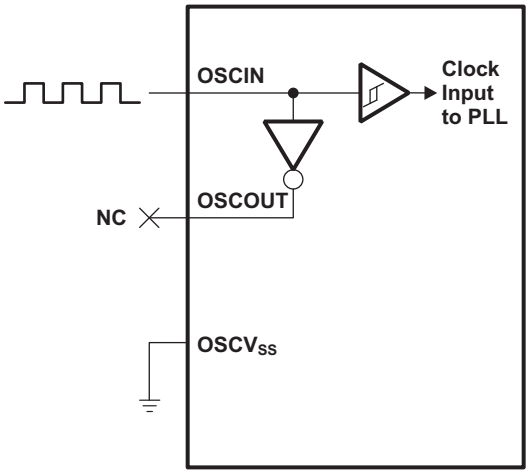


**Figure 5-7. External 1.2V Clock Source**

**Table 5-3. OSCIN Timing Requirements for an Externally Driven Clock**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{OSCIN}$ | OSCIN frequency range | 12 | 50 | MHz |
| $t_{c(OSCIN)}$ | Cycle time, external clock driven on OSCIN | 20 | | ns |
| $t_{w(OSCINH)}$ | Pulse width high, external clock on OSCIN | 0.4 $t_{c(OSCIN)}$ | | ns |
| $t_{w(OSCINL)}$ | Pulse width low, external clock on OSCIN | 0.4 $t_{c(OSCIN)}$ | | ns |
| $t_{t(OSCIN)}$ | Transition time, OSCIN | | 0.25P or 10 (1) | ns |
| $t_{j(OSCIN)}$ | Period jitter, OSCIN | | 0.02P | ns |

(1) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

## 5.6 Clock PLLs

The device has two PLL controllers that provide clocks to different parts of the system. PLL0 provides clocks (though various dividers) to most of the components of the device. PLL1 provides clocks to the mDDR/DDR2 Controller and provides an alternate clock source for the ASYNC3 clock domain. This allows the peripherals on the ASYNC3 clock domain to be immune to frequency scaling operation on PLL0.

The PLL controller provides the following:

- Glitch-Free Transitions (on changing clock settings)
- Domain Clocks Alignment
- Clock Gating
- PLL power down

The various clock outputs given by the controller are as follows:

- Domain Clocks: SYSCLK [1:n]
- Auxiliary Clock from reference clock source: AUXCLK

Various dividers that can be used are as follows:

- Post-PLL Divider: POSTDIV
- SYSCLK Divider: D1, ¼, Dn

Various other controls supported are as follows:

- PLL Multiplier Control: PLLM
- Software programmable PLL Bypass: PLLEN

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### 5.6.1 PLL Device-Specific Information

The device DSP generates the high-frequency internal clocks it requires through an on-chip PLL.

The PLL requires some external filtering components to reduce power supply noise as shown in Figure 5-8.

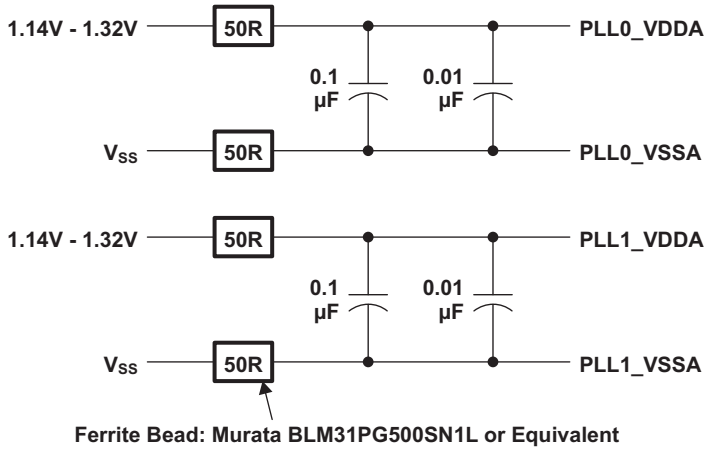


**Figure 5-8. PLL External Filtering Components**

The external filtering components shown above provide noise immunity for the PLLs. PLL0_VDDA and PLL1_VDDA should not be connected together to provide noise immunity between the two PLLs. Likewise, PLL0_VSSA and PLL1_VSSA should not be connected together.

The input to the PLL is either from the on-chip oscillator or from an external clock on the OSCIN pin. PLL0 outputs seven clocks that have programmable divider options. PLL1 outputs three clocks that have programmable divider options. Figure 5-9 illustrates the high-level view of the PLL Topology.

The PLLs are disabled by default after a device reset. They must be configured by software according to the allowable operating conditions listed in Table 5-4 before enabling the device to run from the PLL by setting PLLEN = 1.


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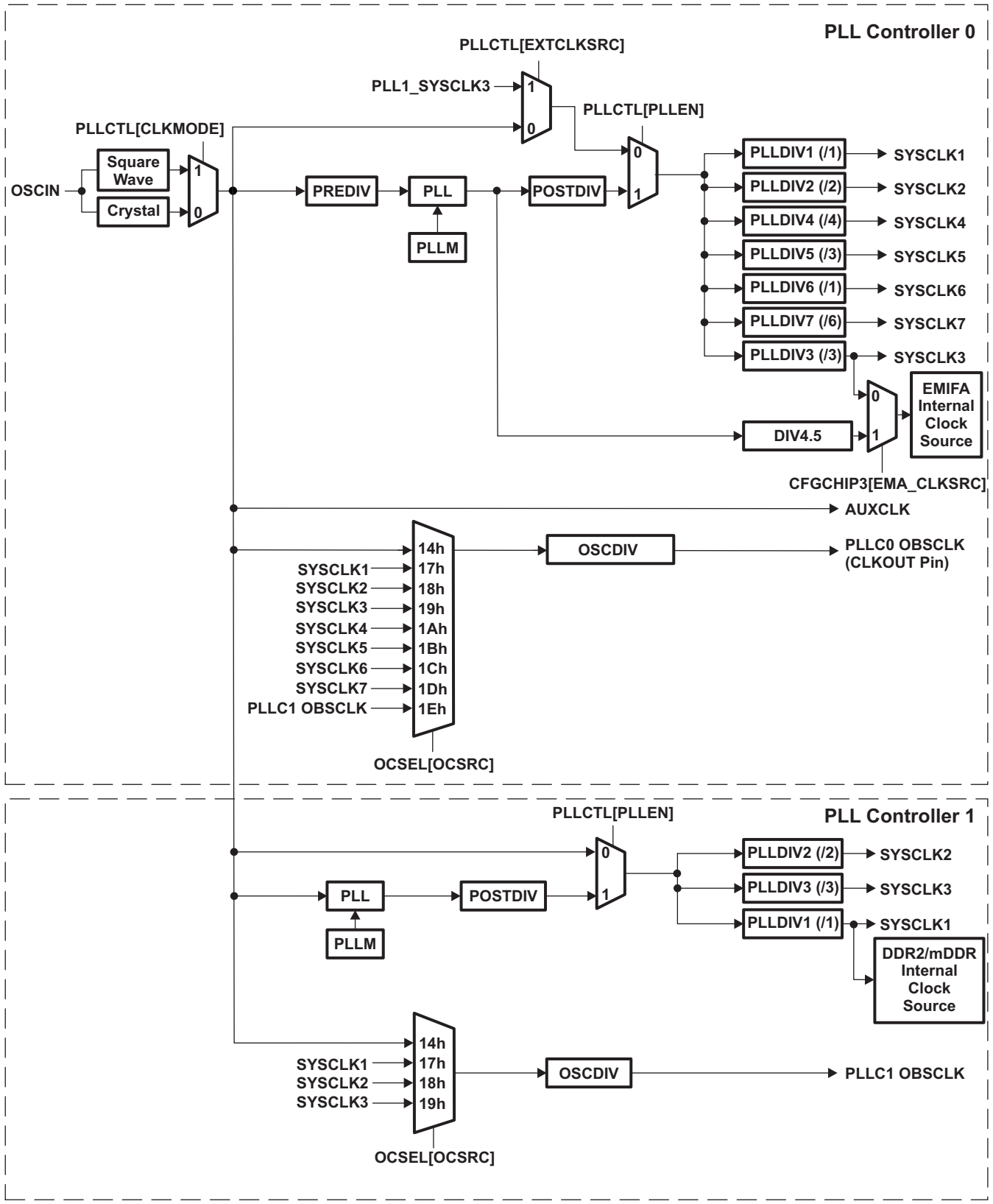


**Figure 5-9. PLL Topology**

**Table 5-4. Allowed PLL Operating Conditions (PLL0 and PLL1)**

| NO. | PARAMETER | Default Value | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | **PLLRST**: Assertion time during initialization | N/A | 1000 | N/A | ns |
| 2 | **Lock time**: The time that the application has to wait for the PLL to acquire lock before setting PLLEN, after changing PREDIV, PLLM, or OSCIN | N/A | N/A | Max PLL Lock Time = $\frac{2000\,N}{\sqrt{m}}$ where N = Pre-Divider Ratio M = PLL Multiplier (1) | OSCIN cycles |
| 3 | **PREDIV**: Pre-divider value | /1 | /1 | /32 | - |
| 4 | **PLLREF**: PLL input frequency | | 12 | 30 (if internal oscillator is used) 50 (if external clock is used) | MHz |
| 5 | **PLLM**: PLL multiplier values | x20 | x4 | x32 | |
| 6 | **PLLOUT**: PLL output frequency | N/A | 300 | 600 | MHz |
| 7 | **POSTDIV**: Post-divider value | /1 | /1 | /32 | - |

(1) The multiplier values must be chosen such that the PLL output frequency (at PLLOUT) is between 300 and 600 MHz, but the frequency going into the SYSCLK dividers (after the post divider) cannot exceed the maximum clock frequency defined for the device at a given voltage operating point.

### 5.6.2 Device Clock Generation

PLL0 is controlled by PLL Controller 0 and PLL1 is controlled by PLL Controller 1. PLLC0 and PLLC1 manage the clock ratios, alignment, and gating for the system clocks to the chip. The PLLCs are responsible for controlling all modes of the PLL through software, in terms of pre-division of the clock inputs (PLLC0 only), multiply factors within the PLLs, and post-division for each of the chip-level clocks from the PLLs outputs. PLLC0 also controls reset propagation through the chip, clock alignment, and test points.

PLLC0 provides clocks for the majority of the system but PLLC1 provides clocks to the mDDR/DDR2 Controller and the ASYNC3 clock domain to provide frequency scaling immunity to a defined set or peripherals. The ASYNC3 clock domain can either derive its clock from PLL1_SYSCLK2 (for frequency scaling immunity from PLL0) or from PLL0_SYSCLK2 (for synchronous timing with PLL0) depending on the application requirements. In addition, some peripherals have specific clock options independent of the ASYNC clock domain.

### 5.6.3 Dynamic Voltage and Frequency Scaling (DVFS)

The processor supports multiple operating points by scaling voltage and frequency to minimize power consumption for a given level of processor performance.

Frequency scaling is achieved by modifying the setting of the PLL controllers' multipliers, post-dividers (POSTDIV), and system clock dividers (SYSCLKn). Modification of the POSTDIV and SYSCLK values does not require relocking the PLL and provides lower latency to switch between operating points, but at the expense of the frequencies being limited by the integer divide values (only the divide values are altered the PLL multiplier is left unmodified). Non integer divide frequency values can be achieved by changing both the multiplier and the divide values, but when the PLL multiplier is changed the PLL must relock, incurring additional latency to change between operating points. Detailed information on modifying the PLL Controller settings can be found in the *OMAP-L138 Applications Processor System Reference Guide* (SPRUGM7).


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Voltage scaling is enabled from outside the device by controlling an external voltage regulator. The processor may communicate with the regulator using GPIOs, I2C or some other interface. When switching between voltage-frequency operating points, the voltage must always support the desired frequency. When moving from a high-performance operating point to a lower performance operating point, the frequency should be lowered first followed by the voltage. When moving from a low-performance operating point to a higher performance operating point, the voltage should be raised first followed by the frequency. Voltage operating points refer to the CVdd voltage at that point. Other static supplies must be maintained at their nominal voltages at all operating points.

The maximum voltage slew rate for CVdd supply changes is 1 mV/us.

For additional information on power management solutions from TI for this processor, follow the Power Management link in the Product Folder on www.ti.com for this processor.

The processor supports multiple clock domains some of which have clock ratio requirements to each other. SYSCLK1:SYSCLK2:SYSCLK4:SYSCLK6 are synchronous to each other and the SYSCLKn dividers must always be configured such that the ratio between these domains is 1:2:4:1. The ASYNC and ASYNC3 clock domains are asynchronous to the other clock domains and have no specific ratio requirement.

Table 5-5 summarizes the maximum internal clock frequencies at each of the voltage operating points.

**Table 5-5. Maximum Internal Clock Frequencies at Each Voltage Operating Point**

| CLOCK SOURCE | CLOCK DOMAIN | | 1.3V NOM | 1.2V NOM | 1.1V NOM | 1.0V NOM |
|---|---|---|---|---|---|---|
| PLL0_SYSCLK1 | DSP subsystem | | 456 MHz | 375 MHz | 200 MHz | 100 MHz |
| PLL0_SYSCLK2 | SYSCLK2 clock domain peripherals and optional clock source for ASYNC3 clock domain peripherals | | 228 MHz | 187.5 MHz | 100 MHz | 50 MHz |
| PLL0_SYSCLK3 | Optional clock for ASYNC1 clock domain (See ASYNC1 row) | | | | | |
| PLL0_SYSCLK4 | SYSCLK4 domain peripherals | | 114 MHz | 93.75 MHz | 50 MHz | 25 MHz |
| PLL0_SYSCLK5 | Not used on this processor | | - | - | - | - |
| PLL0_SYSCLK6 | ARM subsystem | | 456 MHz | 375 MHz | 200 MHz | 100 MHz |
| PLL0_SYSCLK7 | Optional 50 MHz clock source for EMAC RMII interface | | 50 MHz | 50 MHz | - | - |
| PLL1_SYSCLK1 | DDR2/mDDR Interface clock source (memory interface clock is one-half of the value shown) | | 312 MHz | 312 MHz | 300 MHz | 266 MHz |
| PLL1_SYSCLK2 | Optional clock source for ASYNC3 clock domain peripherals | | 152 MHz | 150 MHz | 100 MHz | 75 MHz |
| PLL1_SYSCLK3 | Alternate clock source input to PLL Controller 0 | | 75 MHz | 75 MHz | 75 MHz | 75 MHz |
| McASP AUXCLK | Bypass clock source for the McASP | | 50 MHz | 50 MHz | 50 MHz | 50 MHz |
| PLL0_AUXCLK | Bypass clock source for the USB0 and USB1 | | 48 MHz | 48 MHz | 48 MHz | 48 MHz |
| ASYNC1 | ASYNC Clock Domain (EMIFA) | Async Mode | 148 MHz | 148 MHz | 66.6 MHz | 50 MHz |
| | | SDRAM Mode | 100 MHz | 100 MHz | 66.6 MHz | 50 MHz |
| ASYNC2 | ASYNC2 Clock Domain (multiple peripherals) | | 50 MHz | 50 MHz | 50 MHz | 50 MHz |
| ASYNC3 | ASYNC3 Clock Domain (multiple peripherals) | | 152 MHz | 150 MHz | 100 MHz | 75 MHz |

Some interfaces have specific limitations on supported modes/speeds at each operating point. See the corresponding peripheral sections of this document for more information.

TI provides software components (called the Power Manager) to perform DVFS and abstract the task from the user. The Power Manager controls changing operating points (both frequency and voltage) and handles the related tasks involved such as informing/controlling peripherals to provide graceful transitions between operating points. The Power Manager is bundled as a component of DSP/BIOS.

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## 5.7 Interrupts

The device has a large number of interrupts to service the needs of its many peripherals and subsystems. Both the ARM and C674x CPUs are capable of servicing these interrupts equally. The interrupts can be selectively enabled or disabled in either of the controllers. Also, the ARM and DSP can communicate with each other through interrupts controlled by registers in the SYSCFG module.

### *5.7.1 ARM CPU Interrupts*

The ARM9 CPU core supports two direct interrupts: FIQ and IRQ. The ARM Interrupt Controller (AINTC) extends the number of interrupts to 100, and provides features like programmable masking, priority, hardware nesting support, and interrupt vector generation.

#### 5.7.1.1 ARM Interrupt Controller (AINTC) Interrupt Signal Hierarchy

The ARM Interrupt controller organizes interrupts into the following hierarchy:

- Peripheral Interrupt Requests
  - Individual Interrupt Sources from Peripherals
- 101 System Interrupts
  - One or more Peripheral Interrupt Requests are combined (fixed configuration) to generate a System Interrupt.
  - After prioritization, the AINTC will provide an interrupt vector based unique to each System Interrupt
- 32 Interrupt Channels
  - Each System Interrupt is mapped to one of the 32 Interrupt Channels
  - Channel Number determines the first level of prioritization, Channel 0 is highest priority and 31 lowest.
  - If more than one system interrupt is mapped to a channel, priority within the channel is determined by system interrupt number (0 highest priority)
- Host Interrupts (FIQ and IRQ)
  - Interrupt Channels 0 and 1 generate the ARM FIQ interrupt
  - Interrupt Channels 2 through 31 Generate the ARM IRQ interrupt
- Debug Interrupts
  - Two Debug Interrupts are supported and can be used to trigger events in the debug subsystem
  - Sources can be selected from any of the System Interrupts or Host Interrupts

#### 5.7.1.2 AINTC Hardware Vector Generation

The AINTC also generates an interrupt vector in hardware for both IRQ and FIQ host interrupts. This may be used to accelerate interrupt dispatch. A unique vector is generated for each of the 100 system interrupts. The vector is computed in hardware as:

VECTOR = BASE + (SYSTEM INTERRUPT NUMBER × SIZE)

Where BASE and SIZE are programmable. The computed vector is a 32-bit address which may dispatched to using a single instruction of type LDR PC, [PC, #-<offset_12>] at the FIQ and IRQ vector locations (0xFFFF0018 and 0xFFFF001C respectively).


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#### 5.7.1.3 AINTC Hardware Interrupt Nesting Support

Interrupt nesting occurs when an interrupt service routine re-enables interrupts, to allow the CPU to interrupt the ISR if a higher priority event occurs. The AINTC provides hardware support to facilitate interrupt nesting. It supports both global and per host interrupt (FIQ and IRQ in this case) automatic nesting. If enabled, the AINTC will automatically update an internal nesting register that temporarily masks interrupts at and below the priority of the current interrupt channel. Then if the ISR re-enables interrupts; only higher priority channels will be able to interrupt it. The nesting level is restored by the ISR by writing to the nesting level register on completion. Support for nesting can be enabled/disabled by software, with the option of automatic nesting on a global or per host interrupt basis; or manual nesting.

#### 5.7.1.4 AINTC System Interrupt Assignments

**Table 5-6. AINTC System Interrupt Assignments**

| System Interrupt | Interrupt Name | Source |
|---|---|---|
| 0 | COMMTX | ARM |
| 1 | COMMRX | ARM |
| 2 | NINT | ARM |
| 3 | PRU_EVTOUT0 | PRUSS Interrupt |
| 4 | PRU_EVTOUT1 | PRUSS Interrupt |
| 5 | PRU_EVTOUT2 | PRUSS Interrupt |
| 6 | PRU_EVTOUT3 | PRUSS Interrupt |
| 7 | PRU_EVTOUT4 | PRUSS Interrupt |
| 8 | PRU_EVTOUT5 | PRUSS Interrupt |
| 9 | PRU_EVTOUT6 | PRUSS Interrupt |
| 10 | PRU_EVTOUT7 | PRUSS Interrupt |
| 11 | EDMA3_0_CC0_INT0 | EDMA3_0 Channel Controller 0 Shadow Region 0 Transfer Completion Interrupt |
| 12 | EDMA3_0_CC0_ERRINT | EDMA3_0 Channel Controller 0 Error Interrupt |
| 13 | EDMA3_0_TC0_ERRINT | EDMA3_0 Transfer Controller 0 Error Interrupt |
| 14 | EMIFA_INT | EMIFA |
| 15 | IIC0_INT | I2C0 |
| 16 | MMCSD0_INT0 | MMCSD0 MMC/SD Interrupt |
| 17 | MMCSD0_INT1 | MMCSD0 SDIO Interrupt |
| 18 | PSC0_ALLINT | PSC0 |
| 19 | RTC_IRQS[1:0] | RTC |
| 20 | SPI0_INT | SPI0 |
| 21 | T64P0_TINT12 | Timer64P0 Interrupt 12 |
| 22 | T64P0_TINT34 | Timer64P0 Interrupt 34 |
| 23 | T64P1_TINT12 | Timer64P1 Interrupt 12 |
| 24 | T64P1_TINT34 | Timer64P1 Interrupt 34 |
| 25 | UART0_INT | UART0 |
| 26 | - | Reserved |
| 27 | PROTERR | SYSCFG Protection Shared Interrupt |
| 28 | SYSCFG_CHIPINT0 | SYSCFG CHIPSIG Register |
| 29 | SYSCFG_CHIPINT1 | SYSCFG CHIPSIG Register |
| 30 | SYSCFG_CHIPINT2 | SYSCFG CHIPSIG Register |
| 31 | SYSCFG_CHIPINT3 | SYSCFG CHIPSIG Register |
| 32 | EDMA3_0_TC1_ERRINT | EDMA3_0 Transfer Controller 1 Error Interrupt |
| 33 | EMAC_C0RXTHRESH | EMAC - Core 0 Receive Threshold Interrupt |
| 34 | EMAC_C0RX | EMAC - Core 0 Receive Interrupt |

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**Table 5-6. AINTC System Interrupt Assignments (continued)**

| System Interrupt | Interrupt Name | Source |
|---|---|---|
| 35 | EMAC_C0TX | EMAC - Core 0 Transmit Interrupt |
| 36 | EMAC_C0MISC | EMAC - Core 0 Miscellaneous Interrupt |
| 37 | EMAC_C1RXTHRESH | EMAC - Core 1 Receive Threshold Interrupt |
| 38 | EMAC_C1RX | EMAC - Core 1 Receive Interrupt |
| 39 | EMAC_C1TX | EMAC - Core 1 Transmit Interrupt |
| 40 | EMAC_C1MISC | EMAC - Core 1 Miscellaneous Interrupt |
| 41 | DDR2_MEMERR | DDR2 Controller |
| 42 | GPIO_B0INT | GPIO Bank 0 Interrupt |
| 43 | GPIO_B1INT | GPIO Bank 1 Interrupt |
| 44 | GPIO_B2INT | GPIO Bank 2 Interrupt |
| 45 | GPIO_B3INT | GPIO Bank 3 Interrupt |
| 46 | GPIO_B4INT | GPIO Bank 4 Interrupt |
| 47 | GPIO_B5INT | GPIO Bank 5 Interrupt |
| 48 | GPIO_B6INT | GPIO Bank 6 Interrupt |
| 49 | GPIO_B7INT | GPIO Bank 7 Interrupt |
| 50 | GPIO_B8INT | GPIO Bank 8 Interrupt |
| 51 | IIC1_INT | I2C1 |
| 52 | LCDC_INT | LCD Controller |
| 53 | UART_INT1 | UART1 |
| 54 | MCASP_INT | McASP0 Combined RX / TX Interrupts |
| 55 | PSC1_ALLINT | PSC1 |
| 56 | SPI1_INT | SPI1 |
| 57 | UHPI_ARMINT | UHPI ARM Interrupt |
| 58 | USB0_INT | USB0 Interrupt |
| 59 | USB1_HCINT | USB1 OHCI Host Controller Interrupt |
| 60 | USB1_RWAKEUP | USB1 Remote Wakeup Interrupt |
| 61 | UART2_INT | UART2 |
| 62 | - | Reserved |
| 63 | EHRPWM0 | HiResTimer / PWM0 Interrupt |
| 64 | EHRPWM0TZ | HiResTimer / PWM0 Trip Zone Interrupt |
| 65 | EHRPWM1 | HiResTimer / PWM1 Interrupt |
| 66 | EHRPWM1TZ | HiResTimer / PWM1 Trip Zone Interrupt |
| 67 | SATA_INT | SATA Controller |
| 68 | T64P2_ALL | Timer64P2 - Combined TINT12 and TINT34 |
| 69 | ECAP0 | ECAP0 |
| 70 | ECAP1 | ECAP1 |
| 71 | ECAP2 | ECAP2 |
| 72 | MMCSD1_INT0 | MMCSD1 MMC/SD Interrupt |
| 73 | MMCSD1_INT1 | MMCSD1 SDIO Interrupt |
| 74 | T64P2_CMPINT0 | Timer64P2 - Compare 0 |
| 75 | T64P2_CMPINT1 | Timer64P2 - Compare 1 |
| 76 | T64P2_CMPINT2 | Timer64P2 - Compare 2 |
| 77 | T64P2_CMPINT3 | Timer64P2 - Compare 3 |
| 78 | T64P2_CMPINT4 | Timer64P2 - Compare 4 |
| 79 | T64P2_CMPINT5 | Timer64P2 - Compare 5 |
| 80 | T64P2_CMPINT6 | Timer64P2 - Compare 6 |
| 81 | T64P2_CMPINT7 | Timer64P2 - Compare 7 |


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**Table 5-6. AINTC System Interrupt Assignments (continued)**

| System Interrupt | Interrupt Name | Source |
|---|---|---|
| 82 | T64P3_CMPINT0 | Timer64P3 - Compare 0 |
| 83 | T64P3_CMPINT1 | Timer64P3 - Compare 1 |
| 84 | T64P3_CMPINT2 | Timer64P3 - Compare 2 |
| 85 | T64P3_CMPINT3 | Timer64P3 - Compare 3 |
| 86 | T64P3_CMPINT4 | Timer64P3 - Compare 4 |
| 87 | T64P3_CMPINT5 | Timer64P3 - Compare 5 |
| 88 | T64P3_CMPINT6 | Timer64P3 - Compare 6 |
| 89 | T64P3_CMPINT7 | Timer64P3 - Compare 7 |
| 90 | ARMCLKSTOPREQ | PSC0 |
| 91 | uPP_ALLINT | uPP Combined Interrupt<br>• Channel I End-of-Line Interrupt<br>• Channel I End-of-Window Interrupt<br>• Channel I DMA Access Interrupt<br>• Channel I Overflow-Underrun Interrupt<br>• Channel I DMA Programming Error Interrupt<br>• Channel Q End-of-Line Interrupt<br>• Channel Q End-of-Window Interrupt<br>• Channel Q DMA Access Interrupt<br>• Channel Q Overflow-Underrun Interrupt<br>• Channel Q DMA Programming Error Interrupt |
| 92 | VPIF_ALLINT | VPIF Combined Interrupt<br>• Channel 0 Frame Interrupt<br>• Channel 1 Frame Interrupt<br>• Channel 2 Frame Interrupt<br>• Channel 3 Frame Interrupt<br>• Error Interrupt |
| 93 | EDMA3_1_CC0_INT0 | EDMA3_1 Channel Controller 0 Shadow Region 0 Transfer Completion Interrupt |
| 94 | EDMA3_1_CC0_ERRINT | EDMA3_1Channel Controller 0 Error Interrupt |
| 95 | EDMA3_1_TC0_ERRINT | EDMA3_1 Transfer Controller 0 Error Interrupt |
| 96 | T64P3_ALL | Timer64P 3 - Combined TINT12 and TINT34 |
| 97 | MCBSP0_RINT | McBSP0 Receive Interrupt |
| 98 | MCBSP0_XINT | McBSP0 Transmit Interrupt |
| 99 | MCBSP1_RINT | McBSP1 Receive Interrupt |
| 100 | MCBSP1_XINT | McBSP1 Transmit Interrupt |

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### 5.7.1.5 AINTC Memory Map

**Table 5-7. AINTC Memory Map**

| BYTE ADDRESS | ACRONYM | DESCRIPTION |
|---|---|---|
| 0xFFFE E000 | REV | Revision Register |
| 0xFFFE E004 | CR | Control Register |
| 0xFFFE E008 - 0xFFFE E00F | - | Reserved |
| 0xFFFE E010 | GER | Global Enable Register |
| 0xFFFE E014 - 0xFFFE E01B | - | Reserved |
| 0xFFFE E01C | GNLR | Global Nesting Level Register |
| 0xFFFE E020 | SISR | System Interrupt Status Indexed Set Register |
| 0xFFFE E024 | SICR | System Interrupt Status Indexed Clear Register |
| 0xFFFE E028 | EISR | System Interrupt Enable Indexed Set Register |
| 0xFFFE E02C | EICR | System Interrupt Enable Indexed Clear Register |
| 0xFFFE E030 | - | Reserved |
| 0xFFFE E034 | HIEISR | Host Interrupt Enable Indexed Set Register |
| 0xFFFE E038 | HIEICR | Host Interrupt Enable Indexed Clear Register |
| 0xFFFE E03C - 0xFFFE E04F | - | Reserved |
| 0xFFFE E050 | VBR | Vector Base Register |
| 0xFFFE E054 | VSR | Vector Size Register |
| 0xFFFE E058 | VNR | Vector Null Register |
| 0xFFFE E05C - 0xFFFE E07F | - | Reserved |
| 0xFFFE E080 | GPIR | Global Prioritized Index Register |
| 0xFFFE E084 | GPVR | Global Prioritized Vector Register |
| 0xFFFE E088 - 0xFFFE E1FF | - | Reserved |
| 0xFFFE E200 | SRSR[1] | System Interrupt Status Raw / Set Registers |
| 0xFFFE E204 | SRSR[2] | |
| 0xFFFE E208 | SRSR[3] | |
| 0xFFFE E20C | SRSR[4] | |
| 0xFFFE E210- 0xFFFE E27F | - | Reserved |
| 0xFFFE E280 | SECR[1] | System Interrupt Status Enabled / Clear Registers |
| 0xFFFE E284 | SECR[2] | |
| 0xFFFE E288 | SECR[3] | |
| 0xFFFE E28C | SECR[4] | |
| 0xFFFE E290 - 0xFFFE E2FF | - | Reserved |
| 0xFFFE E300 | ESR[1] | System Interrupt Enable Set Registers |
| 0xFFFE E304 | ESR[2] | |
| 0xFFFE E308 | ESR[3] | |
| 0xFFFE E30C | ESR[4] | |
| 0xFFFE E310 - 0xFFFE E37F | - | Reserved |
| 0xFFFE E380 | ECR[1] | System Interrupt Enable Clear Registers |
| 0xFFFE E384 | ECR[2] | |
| 0xFFFE E388 | ECR[3] | |
| 0xFFFE E38C | ECR[4] | |
| 0xFFFE E390 - 0xFFFE E3FF | - | Reserved |


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**Table 5-7. AINTC Memory Map (continued)**

| BYTE ADDRESS | ACRONYM | DESCRIPTION |
|---|---|---|
| 0xFFFE E400 - 0xFFFE E45B | CMR[0] | Channel Map Registers |
| 0xFFFE E404 | CMR[1] | |
| 0xFFFE E408 | CMR[2] | |
| 0xFFFE E40C | CMR[3] | |
| 0xFFFE E410 | CMR[4] | |
| 0xFFFE E414 | CMR[5] | |
| 0xFFFE E418 | CMR[6] | |
| 0xFFFE E41C | CMR[7] | |
| 0xFFFE E420 | CMR[8] | |
| 0xFFFE E424 | CMR[9] | |
| 0xFFFE E428 | CMR[10] | |
| 0xFFFE E42C | CMR[11] | |
| 0xFFFE E430 | CMR[12] | |
| 0xFFFE E434 | CMR[13] | |
| 0xFFFE E438 | CMR[14] | |
| 0xFFFE E43C | CMR[15] | |
| 0xFFFE E440 | CMR[16] | |
| 0xFFFE E444 | CMR[17] | |
| 0xFFFE E448 | CMR[18] | |
| 0xFFFE E44C | CMR[19] | |
| 0xFFFE E450 | CMR[20] | |
| 0xFFFE E454 | CMR[21] | |
| 0xFFFE E458 | CMR[22] | |
| 0xFFFE E45C | CMR[23] | |
| 0xFFFE E460 | CMR[24] | |
| 0xFFFE E464 | CMR[25] | |
| 0xFFFE E468 - 0xFFFE E8FF | - | Reserved |
| 0xFFFE E900 | HIPIR[1] | Host Interrupt Prioritized Index Registers |
| 0xFFFE E904 | HIPIR[2] | |
| 0xFFFE E908 - 0xFFFE F0FF | - | Reserved |
| 0xFFFE F100 | HINLR[1] | Host Interrupt Nesting Level Registers |
| 0xFFFE F104 | HINLR[2] | |
| 0xFFFE F108 - 0xFFFE F4FF | - | Reserved |
| 0xFFFE F500 | HIER | Host Interrupt Enable Register |
| 0xFFFE F504 - 0xFFFE F5FF | - | Reserved |
| 0xFFFE F600 | HIPVR[1] | Host Interrupt Prioritized Vector Registers |
| 0xFFFE F604 | HIPVR[2] | |
| 0xFFFE F608 - 0xFFFE FFFF | - | Reserved |

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### 5.7.2 DSP Interrupts

The C674x DSP interrupt controller combines device events into 12 prioritized interrupts. The source for each of the 12 CPU interrupts is user programmable and is listed in Table 5-8. Also, the interrupt controller controls the generation of the CPU exceptions, NMI, and emulation interrupts. Table 5-9 summarizes the C674x interrupt controller registers and memory locations.

Refer to the *C674x DSP MegaModule Reference Guide* (SPRUFK5) and the *TMS320C674x DSP CPU and Instruction Set Reference Guide* (SPRUFE8) for details of the C674x interrupts.

**Table 5-8. OMAP-L138 DSP Interrupts**

| EVT# | Interrupt Name | Source |
|---|---|---|
| 0 | EVT0 | C674x Int Ctl 0 |
| 1 | EVT1 | C674x Int Ctl 1 |
| 2 | EVT2 | C674x Int Ctl 2 |
| 3 | EVT3 | C674x Int Ctl 3 |
| 4 | T64P0_TINT12 | Timer64P0 - TINT12 |
| 5 | SYSCFG_CHIPINT2 | SYSCFG CHIPSIG Register |
| 6 | PRU_EVTOUT0 | PRUSS Interrupt |
| 7 | EHRPWM0 | HiResTimer/PWM0 Interrupt |
| 8 | EDMA3_0_CC0_INT1 | EDMA3_0 Channel Controller 0 Shadow Region 1 Transfer Completion Interrupt |
| 9 | EMU_DTDMA | C674x-ECM |
| 10 | EHRPWM0TZ | HiResTimer/PWM0 Trip Zone Interrupt |
| 11 | EMU_RTDXRX | C674x-RTDX |
| 12 | EMU_RTDXTX | C674x-RTDX |
| 13 | IDMAINT0 | C674x-EMC |
| 14 | IDMAINT1 | C674x-EMC |
| 15 | MMCSD0_INT0 | MMCSD0 MMC/SD Interrupt |
| 16 | MMCSD0_INT1 | MMCSD0 SDIO Interrupt |
| 17 | PRU_EVTOUT1 | PRUSS Interrupt |
| 18 | EHRPWM1 | HiResTimer/PWM1 Interrupt |
| 19 | USB0_INT | USB0 Interrupt |
| 20 | USB1_HCINT | USB1 OHCI Host Controller Interrupt |
| 21 | USB1_RWAKEUP | USB1 Remote Wakeup Interrupt |
| 22 | PRU_EVTOUT2 | PRUSS Interrupt |
| 23 | EHRPWM1TZ | HiResTimer/PWM1 Trip Zone Interrupt |
| 24 | SATA_INT | SATA Controller |
| 25 | T64P2_TINTALL | Timer64P2 Combined TINT12 and TINT 34 Interrupt |
| 26 | EMAC_C0RXTHRESH | EMAC - Core 0 Receive Threshold Interrupt |
| 27 | EMAC_C0RX | EMAC - Core 0 Receive Interrupt |
| 28 | EMAC_C0TX | EMAC - Core 0 Transmit Interrupt |
| 29 | EMAC_C0MISC | EMAC - Core 0 Miscellaneous Interrupt |
| 30 | EMAC_C1RXTHRESH | EMAC - Core 1 Receive Threshold Interrupt |
| 31 | EMAC_C1RX | EMAC - Core 1 Receive Interrupt |
| 32 | EMAC_C1TX | EMAC - Core 1 Transmit Interrupt |
| 33 | EMAC_C1MISC | EMAC - Core 1 Miscellaneous Interrupt |
| 34 | UHPI_DSPINT | UHPI DSP Interrupt |
| 35 | PRU_EVTOUT3 | PRUSS Interrupt |
| 36 | IIC0_INT | I2C0 |
| 37 | SP0_INT | SPI0 |


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**Table 5-8. OMAP-L138 DSP Interrupts (continued)**

| EVT# | Interrupt Name | Source |
|---|---|---|
| 38 | UART0_INT | UART0 |
| 39 | PRU_EVTOUT5 | PRUSS Interrupt |
| 40 | T64P1_TINT12 | Timer64P1 Interrupt 12 |
| 41 | GPIO_B1INT | GPIO Bank 1 Interrupt |
| 42 | IIC1_INT | I2C1 |
| 43 | SPI1_INT | SPI1 |
| 44 | PRU_EVTOUT6 | PRUSS Interrupt |
| 45 | ECAP0 | ECAP0 |
| 46 | UART_INT1 | UART1 |
| 47 | ECAP1 | ECAP1 |
| 48 | T64P1_TINT34 | Timer64P1 Interrupt 34 |
| 49 | GPIO_B2INT | GPIO Bank 2 Interrupt |
| 50 | PRU_EVTOUT7 | PRUSS Interrupt |
| 51 | ECAP2 | ECAP2 |
| 52 | GPIO_B3INT | GPIO Bank 3 Interrupt |
| 53 | MMCSD1_INT1 | MMCSD1 SDIO Interrupt |
| 54 | GPIO_B4INT | GPIO Bank 4 Interrupt |
| 55 | EMIFA_INT | EMIFA |
| 56 | EDMA3_0_CC0_ERRINT | EDMA3_0 Channel Controller 0 Error Interrupt |
| 57 | EDMA3_0_TC0_ERRINT | EDMA3_0 Transfer Controller 0 Error Interrupt |
| 58 | EDMA3_0_TC1_ERRINT | EDMA3_0 Transfer Controller 1 Error Interrupt |
| 59 | GPIO_B5INT | GPIO Bank 5 Interrupt |
| 60 | DDR2_MEMERR | DDR2 Memory Error Interrupt |
| 61 | MCASP0_INT | McASP0 Combined RX/TX Interrupts |
| 62 | GPIO_B6INT | GPIO Bank 6 Interrupt |
| 63 | RTC_IRQS | RTC Combined |
| 64 | T64P0_TINT34 | Timer64P0 Interrupt 34 |
| 65 | GPIO_B0INT | GPIO Bank 0 Interrupt |
| 66 | PRU_EVTOUT4 | PRUSS Interrupt |
| 67 | SYSCFG_CHIPINT3 | SYSCFG_CHIPSIG Register |
| 68 | MMCSD1_INT0 | MMCSD1 MMC/SD Interrupt |
| 69 | UART2_INT | UART2 |
| 70 | PSC0_ALLINT | PSC0 |
| 71 | PSC1_ALLINT | PSC1 |
| 72 | GPIO_B7INT | GPIO Bank 7 Interrupt |
| 73 | LCDC_INT | LDC Controller |
| 74 | PROTERR | SYSCFG Protection Shared Interrupt |
| 75 | GPIO_B8INT | GPIO Bank 8 Interrupt |
| 76 - 77 | - | Reserved |
| 78 | T64P2_CMPINT0 | Timer64P2 - Compare Interrupt 0 |
| 79 | T64P2_CMPINT1 | Timer64P2 - Compare Interrupt 1 |
| 80 | T64P2_CMPINT2 | Timer64P2 - Compare Interrupt 2 |
| 81 | T64P2_CMPINT3 | Timer64P2 - Compare Interrupt 3 |
| 82 | T64P2_CMPINT4 | Timer64P2 - Compare Interrupt 4 |
| 83 | T64P2_CMPINT5 | Timer64P2 - Compare Interrupt 5 |
| 84 | T64P2_CMPINT6 | Timer64P2 - Compare Interrupt 6 |
| 85 | T64P2_CMPINT7 | Timer64P2 - Compare Interrupt 7 |

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**Table 5-8. OMAP-L138 DSP Interrupts (continued)**

| EVT# | Interrupt Name | Source |
|---|---|---|
| 86 | T64P3_TINTALL | Timer64P3 Combined TINT12 and TINT 34 Interrupt |
| 87 | MCBSP0_RINT | McBSP0 Receive Interrupt |
| 88 | MCBSP0_XINT | McBSP0 Transmit Interrupt |
| 89 | MCBSP1_RINT | McBSP1 Receive Interrupt |
| 90 | MCBSP1_XINT | McBSP1 Transmit Interrupt |
| 91 | EDMA3_1_CC0_INT1 | EDMA3_1 Channel Controller 0 Shadow Region 1 Transfer Completion Interrupt |
| 92 | EDMA3_1_CC0_ERRINT | EDMA3_1 Channel Controller 0 Error Interrupt |
| 93 | EDMA3_1_TC0_ERRINT | EDMA3_1 Transfer Controller 0 Error Interrupt |
| 94 | UPP_INT | uPP Combined Interrupt |
| 95 | VPIF_INT | VPIF Combined Interrupt |
| 96 | INTERR | C674x-Int Ctl |
| 97 | EMC_IDMAERR | C674x-EMC |
| 98 - 112 | - | Reserved |
| 113 | PMC_ED | C674x-PMC |
| 114 - 115 | - | Reserved |
| 116 | UMC_ED1 | C674x-UMC |
| 117 | UMC_ED2 | C674x-UMC |
| 118 | PDC_INT | C674x-PDC |
| 119 | SYS_CMPA | C674x-SYS |
| 120 | PMC_CMPA | C674x-PMC |
| 121 | PMC_CMPA | C674x-PMC |
| 122 | DMC_CMPA | C674x-DMC |
| 123 | DMC_CMPA | C674x-DMC |
| 124 | UMC_CMPA | C674x-UMC |
| 125 | UMC_CMPA | C674x-UMC |
| 126 | EMC_CMPA | C674x-EMC |
| 127 | EMC_BUSERR | C674x-EMC |


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**Table 5-9. C674x DSP Interrupt Controller Registers**

| BYTE ADDRESS | ACRONYM | DESCRIPTION |
|---|---|---|
| 0x0180 0000 | EVTFLAG0 | Event flag register 0 |
| 0x0180 0004 | EVTFLAG1 | Event flag register 1 |
| 0x0180 0008 | EVTFLAG2 | Event flag register 2 |
| 0x0180 000C | EVTFLAG3 | Event flag register 3 |
| 0x0180 0020 | EVTSET0 | Event set register 0 |
| 0x0180 0024 | EVTSET1 | Event set register 1 |
| 0x0180 0028 | EVTSET2 | Event set register 2 |
| 0x0180 002C | EVTSET3 | Event set register 3 |
| 0x0180 0040 | EVTCLR0 | Event clear register 0 |
| 0x0180 0044 | EVTCLR1 | Event clear register 1 |
| 0x0180 0048 | EVTCLR2 | Event clear register 2 |
| 0x0180 004C | EVTCLR3 | Event clear register 3 |
| 0x0180 0080 | EVTMASK0 | Event mask register 0 |
| 0x0180 0084 | EVTMASK1 | Event mask register 1 |
| 0x0180 0088 | EVTMASK2 | Event mask register 2 |
| 0x0180 008C | EVTMASK3 | Event mask register 3 |
| 0x0180 00A0 | MEVTFLAG0 | Masked event flag register 0 |
| 0x0180 00A4 | MEVTFLAG1 | Masked event flag register 1 |
| 0x0180 00A8 | MEVTFLAG2 | Masked event flag register 2 |
| 0x0180 00AC | MEVTFLAG3 | Masked event flag register 3 |
| 0x0180 00C0 | EXPMASK0 | Exception mask register 0 |
| 0x0180 00C4 | EXPMASK1 | Exception mask register 1 |
| 0x0180 00C8 | EXPMASK2 | Exception mask register 2 |
| 0x0180 00CC | EXPMASK3 | Exception mask register 3 |
| 0x0180 00E0 | MEXPFLAG0 | Masked exception flag register 0 |
| 0x0180 00E4 | MEXPFLAG1 | Masked exception flag register 1 |
| 0x0180 00E8 | MEXPFLAG2 | Masked exception flag register 2 |
| 0x0180 00EC | MEXPFLAG3 | Masked exception flag register 3 |
| 0x0180 0104 | INTMUX1 | Interrupt mux register 1 |
| 0x0180 0108 | INTMUX2 | Interrupt mux register 2 |
| 0x0180 010C | INTMUX3 | Interrupt mux register 3 |
| 0x0180 0140 - 0x0180 0144 | - | Reserved |
| 0x0180 0180 | INTXSTAT | Interrupt exception status |
| 0x0180 0184 | INTXCLR | Interrupt exception clear |
| 0x0180 0188 | INTDMASK | Dropped interrupt mask register |
| 0x0180 01C0 | EVTASRT | Event assert register |

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## 5.8 Power and Sleep Controller (PSC)

The Power and Sleep Controllers (PSC) are responsible for managing transitions of system power on/off, clock on/off, resets (device level and module level). It is used primarily to provide granular power control for on chip modules (peripherals and CPU). A PSC module consists of a Global PSC (GPSC) and a set of Local PSCs (LPSCs). The GPSC contains memory mapped registers, PSC interrupts, a state machine for each peripheral/module it controls. An LPSC is associated with every module that is controlled by the PSC and provides clock and reset control.

The PSC includes the following features:

- Provides a software interface to:
  - Control module clock enable/disable
  - Control module reset
  - Control CPU local reset
- Supports IcePick emulation features: power, clock and reset

  PSC0 controls 16 local PSCs.

  PSC1 controls 32 local PSCs.

**Table 5-10. Power and Sleep Controller (PSC) Registers**

| PSC0 BYTE ADDRESS | PSC1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C1 0000 | 0x01E2 7000 | REVID | Peripheral Revision and Class Information Register |
| 0x01C1 0018 | 0x01E2 7018 | INTEVAL | Interrupt Evaluation Register |
| 0x01C1 0040 | 0x01E2 7040 | MERRPR0 | Module Error Pending Register 0 (module 0-15) (PSC0)<br>Module Error Pending Register 0 (module 0-31) (PSC1) |
| 0x01C1 0050 | 0x01E2 7050 | MERRCR0 | Module Error Clear Register 0 (module 0-15) (PSC0)<br>Module Error Clear Register 0 (module 0-31) (PSC1) |
| 0x01C1 0060 | 0x01E2 7060 | PERRPR | Power Error Pending Register |
| 0x01C1 0068 | 0x01E2 7068 | PERRCR | Power Error Clear Register |
| 0x01C1 0120 | 0x01E2 7120 | PTCMD | Power Domain Transition Command Register |
| 0x01C1 0128 | 0x01E2 7128 | PTSTAT | Power Domain Transition Status Register |
| 0x01C1 0200 | 0x01E2 7200 | PDSTAT0 | Power Domain 0 Status Register |
| 0x01C1 0204 | 0x01E2 7204 | PDSTAT1 | Power Domain 1 Status Register |
| 0x01C1 0300 | 0x01E2 7300 | PDCTL0 | Power Domain 0 Control Register |
| 0x01C1 0304 | 0x01E2 7304 | PDCTL1 | Power Domain 1 Control Register |
| 0x01C1 0400 | 0x01E2 7400 | PDCFG0 | Power Domain 0 Configuration Register |
| 0x01C1 0404 | 0x01E2 7404 | PDCFG1 | Power Domain 1 Configuration Register |
| 0x01C1 0800 | 0x01E2 7800 | MDSTAT0 | Module 0 Status Register |
| 0x01C1 0804 | 0x01E2 7804 | MDSTAT1 | Module 1 Status Register |
| 0x01C1 0808 | 0x01E2 7808 | MDSTAT2 | Module 2 Status Register |
| 0x01C1 080C | 0x01E2 780C | MDSTAT3 | Module 3 Status Register |
| 0x01C1 0810 | 0x01E2 7810 | MDSTAT4 | Module 4 Status Register |
| 0x01C1 0814 | 0x01E2 7814 | MDSTAT5 | Module 5 Status Register |
| 0x01C1 0818 | 0x01E2 7818 | MDSTAT6 | Module 6 Status Register |
| 0x01C1 081C | 0x01E2 781C | MDSTAT7 | Module 7 Status Register |
| 0x01C1 0820 | 0x01E2 7820 | MDSTAT8 | Module 8 Status Register |
| 0x01C1 0824 | 0x01E2 7824 | MDSTAT9 | Module 9 Status Register |
| 0x01C1 0828 | 0x01E2 7828 | MDSTAT10 | Module 10 Status Register |
| 0x01C1 082C | 0x01E2 782C | MDSTAT11 | Module 11 Status Register |
| 0x01C1 0830 | 0x01E2 7830 | MDSTAT12 | Module 12 Status Register |
| 0x01C1 0834 | 0x01E2 7834 | MDSTAT13 | Module 13 Status Register |


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**Table 5-10. Power and Sleep Controller (PSC) Registers (continued)**

| PSC0 BYTE ADDRESS | PSC1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C1 0838 | 0x01E2 7838 | MDSTAT14 | Module 14 Status Register |
| 0x01C1 083C | 0x01E2 783C | MDSTAT15 | Module 15 Status Register |
| - | 0x01E2 7840 | MDSTAT16 | Module 16 Status Register |
| - | 0x01E2 7844 | MDSTAT17 | Module 17 Status Register |
| - | 0x01E2 7848 | MDSTAT18 | Module 18 Status Register |
| - | 0x01E2 784C | MDSTAT19 | Module 19 Status Register |
| - | 0x01E2 7850 | MDSTAT20 | Module 20 Status Register |
| - | 0x01E2 7854 | MDSTAT21 | Module 21 Status Register |
| - | 0x01E2 7858 | MDSTAT22 | Module 22 Status Register |
| - | 0x01E2 785C | MDSTAT23 | Module 23 Status Register |
| - | 0x01E2 7860 | MDSTAT24 | Module 24 Status Register |
| - | 0x01E2 7864 | MDSTAT25 | Module 25 Status Register |
| - | 0x01E2 7868 | MDSTAT26 | Module 26 Status Register |
| - | 0x01E2 786C | MDSTAT27 | Module 27 Status Register |
| - | 0x01E2 7870 | MDSTAT28 | Module 28 Status Register |
| - | 0x01E2 7874 | MDSTAT29 | Module 29 Status Register |
| - | 0x01E2 7878 | MDSTAT30 | Module 30 Status Register |
| - | 0x01E2 787C | MDSTAT31 | Module 31 Status Register |
| 0x01C1 0A00 | 0x01E2 7A00 | MDCTL0 | Module 0 Control Register |
| 0x01C1 0A04 | 0x01E2 7A04 | MDCTL1 | Module 1 Control Register |
| 0x01C1 0A08 | 0x01E2 7A08 | MDCTL2 | Module 2 Control Register |
| 0x01C1 0A0C | 0x01E2 7A0C | MDCTL3 | Module 3 Control Register |
| 0x01C1 0A10 | 0x01E2 7A10 | MDCTL4 | Module 4 Control Register |
| 0x01C1 0A14 | 0x01E2 7A14 | MDCTL5 | Module 5 Control Register |
| 0x01C1 0A18 | 0x01E2 7A18 | MDCTL6 | Module 6 Control Register |
| 0x01C1 0A1C | 0x01E2 7A1C | MDCTL7 | Module 7 Control Register |
| 0x01C1 0A20 | 0x01E2 7A20 | MDCTL8 | Module 8 Control Register |
| 0x01C1 0A24 | 0x01E2 7A24 | MDCTL9 | Module 9 Control Register |
| 0x01C1 0A28 | 0x01E2 7A28 | MDCTL10 | Module 10 Control Register |
| 0x01C1 0A2C | 0x01E2 7A2C | MDCTL11 | Module 11 Control Register |
| 0x01C1 0A30 | 0x01E2 7A30 | MDCTL12 | Module 12 Control Register |
| 0x01C1 0A34 | 0x01E2 7A34 | MDCTL13 | Module 13 Control Register |
| 0x01C1 0A38 | 0x01E2 7A38 | MDCTL14 | Module 14 Control Register |
| 0x01C1 0A3C | 0x01E2 7A3C | MDCTL15 | Module 15 Control Register |
| - | 0x01E2 7A40 | MDCTL16 | Module 16 Control Register |
| - | 0x01E2 7A44 | MDCTL17 | Module 17 Control Register |
| - | 0x01E2 7A48 | MDCTL18 | Module 18 Control Register |
| - | 0x01E2 7A4C | MDCTL19 | Module 19 Control Register |
| - | 0x01E2 7A50 | MDCTL20 | Module 20 Control Register |
| - | 0x01E2 7A54 | MDCTL21 | Module 21 Control Register |
| - | 0x01E2 7A58 | MDCTL22 | Module 22 Control Register |
| - | 0x01E2 7A5C | MDCTL23 | Module 23 Control Register |
| - | 0x01E2 7A60 | MDCTL24 | Module 24 Control Register |
| - | 0x01E2 7A64 | MDCTL25 | Module 25 Control Register |
| - | 0x01E2 7A68 | MDCTL26 | Module 26 Control Register |
| - | 0x01E2 7A6C | MDCTL27 | Module 27 Control Register |
| - | 0x01E2 7A70 | MDCTL28 | Module 28 Control Register |

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**Table 5-10. Power and Sleep Controller (PSC) Registers (continued)**

| PSC0 BYTE ADDRESS | PSC1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| - | 0x01E2 7A74 | MDCTL29 | Module 29 Control Register |
| - | 0x01E2 7A78 | MDCTL30 | Module 30 Control Register |
| - | 0x01E2 7A7C | MDCTL31 | Module 31 Control Register |

### 5.8.1 Power Domain and Module Topology

The device includes two PSC modules.

Each PSC module controls clock states for several of the on chip modules, controllers and interconnect components. Table 5-11 and Table 5-12 lists the set of peripherals/modules that are controlled by the PSC, the power domain they are associated with, the LPSC assignment and the default (power-on reset) module states. The module states and terminology are defined in Section 5.8.1.2.

**Table 5-11. PSC0 Default Module Configuration**

| LPSC Number | Module Name | Power Domain | Default Module State | Auto Sleep/Wake Only |
|---|---|---|---|---|
| 0 | EDMA3 Channel Controller 0 | AlwaysON (PD0) | SwRstDisable | — |
| 1 | EDMA3 Transfer Controller 0 | AlwaysON (PD0) | SwRstDisable | — |
| 2 | EDMA3 Transfer Controller 1 | AlwaysON (PD0) | SwRstDisable | — |
| 3 | EMIFA (Br7) | AlwaysON (PD0) | SwRstDisable | — |
| 4 | SPI 0 | AlwaysON (PD0) | SwRstDisable | — |
| 5 | MMC/SD 0 | AlwaysON (PD0) | SwRstDisable | — |
| 6 | ARM Interrupt Controller | AlwaysON (PD0) | SwRstDisable | — |
| 7 | ARM RAM/ROM | AlwaysON (PD0) | Enable | Yes |
| 8 | — | — | — | — |
| 9 | UART 0 | AlwaysON (PD0) | SwRstDisable | — |
| 10 | SCR0 (Br 0, Br 1, Br 2, Br 8) | AlwaysON (PD0) | Enable | Yes |
| 11 | SCR1 (Br 4) | AlwaysON (PD0) | Enable | Yes |
| 12 | SCR2 (Br 3, Br 5, Br 6) | AlwaysON (PD0) | Enable | Yes |
| 13 | PRUSS | AlwaysON (PD0) | SwRstDisable | — |
| 14 | ARM | AlwaysON (PD0) | SwRstDisable | — |
| 15 | DSP | PD_DSP (PD1) | Enable | — |


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**Table 5-12. PSC1 Default Module Configuration**

| LPSC Number | Module Name | Power Domain | Default Module State | Auto Sleep/Wake Only |
|---|---|---|---|---|
| 0 | EDMA3 Channel Controller 1 | AlwaysON (PD0) | SwRstDisable | — |
| 1 | USB0 (USB2.0) | AlwaysON (PD0) | SwRstDisable | — |
| 2 | USB1 (USB1.1) | AlwaysON (PD0) | SwRstDisable | — |
| 3 | GPIO | AlwaysON (PD0) | SwRstDisable | — |
| 4 | UHPI | AlwaysON (PD0) | SwRstDisable | — |
| 5 | EMAC | AlwaysON (PD0) | SwRstDisable | — |
| 6 | DDR2 (and SCR_F3) | AlwaysON (PD0) | SwRstDisable | — |
| 7 | McASP0 ( + McASP0 FIFO) | AlwaysON (PD0) | SwRstDisable | — |
| 8 | SATA | AlwaysON (PD0) | SwRstDisable | — |
| 9 | VPIF | AlwaysON (PD0) | SwRstDisable | — |
| 10 | SPI 1 | AlwaysON (PD0) | SwRstDisable | — |
| 11 | I2C 1 | AlwaysON (PD0) | SwRstDisable | — |
| 12 | UART 1 | AlwaysON (PD0) | SwRstDisable | — |
| 13 | UART 2 | AlwaysON (PD0) | SwRstDisable | — |
| 14 | McBSP0 ( + McBSP0 FIFO) | AlwaysON (PD0) | SwRstDisable | — |
| 15 | McBSP1 ( + McBSP1 FIFO) | AlwaysON (PD0) | SwRstDisable | — |
| 16 | LCDC | AlwaysON (PD0) | SwRstDisable | — |
| 17 | eHRPWM0/1 | AlwaysON (PD0) | SwRstDisable | — |
| 18 | MMCSD1 | AlwaysON (PD0) | SwRstDisable | — |
| 19 | uPP | AlwaysON (PD0) | SwRstDisable | — |
| 20 | ECAP0/1/2 | AlwaysON (PD0) | SwRstDisable | — |
| 21 | EDMA3 Transfer Controller 2 | AlwaysON (PD0) | SwRstDisable | — |
| 22 | — | — | — | — |
| 23 | — | — | — | — |
| 24 | SCR_F0 (and bridge F0) | AlwaysON (PD0) | Enable | Yes |
| 25 | SCR_F1 (and bridge F1) | AlwaysON (PD0) | Enable | Yes |
| 26 | SCR_F2 (and bridge F2) | AlwaysON (PD0) | Enable | Yes |
| 27 | SCR_F6 (and bridge F3) | AlwaysON (PD0) | Enable | Yes |
| 28 | SCR_F7 (and bridge F4) | AlwaysON (PD0) | Enable | Yes |
| 29 | SCR_F8 (and bridge F5) | AlwaysON (PD0) | Enable | Yes |
| 30 | Bridge F7 (DDR Controller path) | AlwaysON (PD0) | Enable | Yes |
| 31 | Shared RAM (including SCR_F4 and bridge F6) | PD_SHRAM | Enable | — |

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#### 5.8.1.1 Power Domain States

A power domain can only be in one of the two states: ON or OFF, defined as follows:

- ON: power to the domain is on
- OFF: power to the domain is off

For both PSC0 and PSC1, the Always ON domain, or PD0 power domain, is always in the ON state when the chip is powered-on. This domain is not programmable to OFF state.

- On PSC0 PD1/PD_DSP Domain: Controls the sleep state for DSP L1 and L2 Memories
- On PSC1 PD1/PD_SHRAM Domain: Controls the sleep state for the 128K Shared RAM

#### 5.8.1.2 Module States

The PSC defines several possible states for a module. This states are essentially a combination of the module reset asserted or de-asserted and module clock on/enabled or off/disabled. The module states are defined in Table 5-13.

**Table 5-13. Module States**

| Module State | Module Reset | Module Clock | Module State Definition |
|---|---|---|---|
| Enable | De-asserted | On | A module in the enable state has its module reset de-asserted and it has its clock on. This is the normal operational state for a given module |
| Disable | De-asserted | Off | A module in the disabled state has its module reset de-asserted and it has its module clock off. This state is typically used for disabling a module clock to save power. The device is designed in full static CMOS, so when you stop a module clock, it retains the module's state. When the clock is restarted, the module resumes operating from the stopping point. |
| SyncReset | Asserted | On | A module state in the SyncReset state has its module reset asserted and it has its clock on. Generally, software is not expected to initiate this state |
| SwRstDisable | Asserted | Off | A module in the SwResetDisable state has its module reset asserted and it has its clock disabled. After initial power-on, several modules come up in the SwRstDisable state. Generally, software is not expected to initiate this state |
| Auto Sleep | De-asserted | Off | A module in the Auto Sleep state also has its module reset de-asserted and its module clock disabled, similar to the Disable state. However this is a special state, once a module is configured in this state by software, it can "automatically" transition to "Enable" state whenever there is an internal read/write request made to it, and after servicing the request it will "automatically" transition into the sleep state (with module reset re de-asserted and module clock disabled), without any software intervention. The transition from sleep to enabled and back to sleep state has some cycle latency associated with it. It is not envisioned to use this mode when peripherals are fully operational and moving data. |
| Auto Wake | De-asserted | Off | A module in the Auto Wake state also has its module reset de-asserted and its module clock disabled, similar to the Disable state. However this is a special state, once a module is configured in this state by software, it will "automatically" transition to "Enable" state whenever there is an internal read/write request made to it, and will remain in the "Enabled" state from then on (with module reset re de-asserted and module clock on), without any software intervention. The transition from sleep to enabled state has some cycle latency associated with it. It is not envisioned to use this mode when peripherals are fully operational and moving data. |


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## 5.9 Enhanced Direct Memory Access Controller (EDMA3)

The EDMA3 controller handles all data transfers between memories and the device slave peripherals on the device. These data transfers include cache servicing, non-cacheable memory accesses, user-programmed data transfers, and host accesses.

### *5.9.1 EDMA3 Channel Synchronization Events*

Each EDMA3 channel controller supports up to 32 channels which service peripherals and memory. Table 5-14 lists the source of the EDMA3 synchronization events associated with each of the programmable EDMA channels.

**Table 5-14. EDMA Synchronization Events**

| EDMA3 Channel Controller 0 | | | |
|---|---|---|---|
| **Event** | **Event Name / Source** | **Event** | **Event Name / Source** |
| 0 | McASP0 Receive | 16 | MMCSD0 Receive |
| 1 | McASP0 Transmit | 17 | MMCSD0 Transmit |
| 2 | McBSP0 Receive | 18 | SPI1 Receive |
| 3 | McBSP0 Transmit | 19 | SPI1 Transmit |
| 4 | McBSP1 Receive | 20 | PRU_EVTOUT6 |
| 5 | McBSP1 Transmit | 21 | PRU_EVTOUT7 |
| 6 | GPIO Bank 0 Interrupt | 22 | GPIO Bank 2 Interrupt |
| 7 | GPIO Bank 1 Interrup | 23 | GPIO Bank 3 Interrupt |
| 8 | UART0 Receive | 24 | I2C0 Receive |
| 9 | UART0 Transmit | 25 | I2C0 Transmit |
| 10 | Timer64P0 Event Out 12 | 26 | I2C1 Receive |
| 11 | Timer64P0 Event Out 34 | 27 | I2C1 Transmit |
| 12 | UART1 Receive | 28 | GPIO Bank 4 Interrupt |
| 13 | UART1 Transmit | 29 | GPIO Bank 5 Interrupt |
| 14 | SPI0 Receive | 30 | UART2 Receive |
| 15 | SPI0 Transmit | 31 | |
| **EDMA3 Channel Controller 1** | | | |
| Event | Event Name / Source | Event | Event Name / Source |
| 0 | Timer64P2 Compare Event 0 | 16 | GPIO Bank 6 Interrupt |
| 1 | Timer64P2 Compare Event 1 | 17 | GPIO Bank 7 Interrupt |
| 2 | Timer64P2 Compare Event 2 | 18 | GPIO Bank 8 Interrupt |
| 3 | Timer64P2 Compare Event 3 | 19 | Reserved |
| 4 | Timer64P2 Compare Event 4 | 20 | Reserved |
| 5 | Timer64P2 Compare Event 5 | 21 | Reserved |
| 6 | Timer64P2 Compare Event 6 | 22 | Reserved |
| 7 | Timer64P2 Compare Event 7 | 23 | Reserved |
| 8 | Timer64P3 Compare Event 0 | 24 | Timer64P2 Event Out 12 |
| 9 | Timer64P3 Compare Event 1 | 25 | Timer64P2 Event Out 34 |
| 10 | Timer64P3 Compare Event 2 | 26 | Timer64P3 Event Out 12 |
| 11 | Timer64P3 Compare Event 3 | 27 | Timer64P3 Event Out 34 |
| 12 | Timer64P3 Compare Event 4 | 28 | MMCSD1 Receive |
| 13 | Timer64P3 Compare Event 5 | 29 | MMCSD1 Transmit |
| 14 | Timer64P3 Compare Event 6 | 30 | Reserved |
| 15 | Timer64P3 Compare Event 7 | 31 | Reserved |

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### 5.9.2 EDMA3 Peripheral Register Descriptions

Table 5-15 is the list of EDMA3 Channel Controller Registers and Table 5-16 is the list of EDMA3 Transfer Controller registers.

**Table 5-15. EDMA3 Channel Controller (EDMA3CC) Registers**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS | EDMA3_1 Channel Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C0 0000 | 0x01E3 0000 | PID | Peripheral Identification Register |
| 0x01C0 0004 | 0x01E3 0004 | CCCFG | EDMA3CC Configuration Register |
| **Global Registers** | | | |
| 0x01C0 0200 | 0x01E3 0200 | QCHMAP0 | QDMA Channel 0 Mapping Register |
| 0x01C0 0204 | 0x01E3 0204 | QCHMAP1 | QDMA Channel 1 Mapping Register |
| 0x01C0 0208 | 0x01E3 0208 | QCHMAP2 | QDMA Channel 2 Mapping Register |
| 0x01C0 020C | 0x01E3 020C | QCHMAP3 | QDMA Channel 3 Mapping Register |
| 0x01C0 0210 | 0x01E3 0210 | QCHMAP4 | QDMA Channel 4 Mapping Register |
| 0x01C0 0214 | 0x01E3 0214 | QCHMAP5 | QDMA Channel 5 Mapping Register |
| 0x01C0 0218 | 0x01E3 0218 | QCHMAP6 | QDMA Channel 6 Mapping Register |
| 0x01C0 021C | 0x01E3 021C | QCHMAP7 | QDMA Channel 7 Mapping Register |
| 0x01C0 0240 | 0x01E3 0240 | DMAQNUM0 | DMA Channel Queue Number Register 0 |
| 0x01C0 0244 | 0x01E3 0244 | DMAQNUM1 | DMA Channel Queue Number Register 1 |
| 0x01C0 0248 | 0x01E3 0248 | DMAQNUM2 | DMA Channel Queue Number Register 2 |
| 0x01C0 024C | 0x01E3 024C | DMAQNUM3 | DMA Channel Queue Number Register 3 |
| 0x01C0 0260 | 0x01E3 0260 | QDMAQNUM | QDMA Channel Queue Number Register |
| 0x01C0 0284 | 0x01E3 0284 | QUEPRI | Queue Priority Register(1) |
| 0x01C0 0300 | 0x01E3 0300 | EMR | Event Missed Register |
| 0x01C0 0308 | 0x01E3 0308 | EMCR | Event Missed Clear Register |
| 0x01C0 0310 | 0x01E3 0310 | QEMR | QDMA Event Missed Register |
| 0x01C0 0314 | 0x01E3 0314 | QEMCR | QDMA Event Missed Clear Register |
| 0x01C0 0318 | 0x01E3 0318 | CCERR | EDMA3CC Error Register |
| 0x01C0 031C | 0x01E3 031C | CCERRCLR | EDMA3CC Error Clear Register |
| 0x01C0 0320 | 0x01E3 0320 | EEVAL | Error Evaluate Register |
| 0x01C0 0340 | 0x01E3 0340 | DRAE0 | DMA Region Access Enable Register for Region 0 |
| 0x01C0 0348 | 0x01E3 0348 | DRAE1 | DMA Region Access Enable Register for Region 1 |
| 0x01C0 0350 | 0x01E3 0350 | DRAE2 | DMA Region Access Enable Register for Region 2 |
| 0x01C0 0358 | 0x01E3 0358 | DRAE3 | DMA Region Access Enable Register for Region 3 |
| 0x01C0 0380 | 0x01E3 0380 | QRAE0 | QDMA Region Access Enable Register for Region 0 |
| 0x01C0 0384 | 0x01E3 0384 | QRAE1 | QDMA Region Access Enable Register for Region 1 |
| 0x01C0 0388 | 0x01E3 0388 | QRAE2 | QDMA Region Access Enable Register for Region 2 |
| 0x01C0 038C | 0x01E3 038C | QRAE3 | QDMA Region Access Enable Register for Region 3 |
| 0x01C0 0400 - 0x01C0 043C | 0x01E3 0400 - 0x01E3 043C | Q0E0-Q0E15 | Event Queue Entry Registers Q0E0-Q0E15 |
| 0x01C0 0440 - 0x01C0 047C | 0x01E3 0440 - 0x01E3 047C | Q1E0-Q1E15 | Event Queue Entry Registers Q1E0-Q1E15 |
| 0x01C0 0600 | 0x01E3 0600 | QSTAT0 | Queue 0 Status Register |
| 0x01C0 0604 | 0x01E3 0604 | QSTAT1 | Queue 1 Status Register |
| 0x01C0 0620 | 0x01E3 0620 | QWMTHRA | Queue Watermark Threshold A Register |
| 0x01C0 0640 | 0x01E3 0640 | CCSTAT | EDMA3CC Status Register |

(1) On previous architectures, the EDMA3TC priority was controlled by the queue priority register (QUEPRI) in the EDMA3CC memory-map. However for this device, the priority control for the transfer controllers is controlled by the chip-level registers in the System Configuration Module. You should use the chip-level registers and not QUEPRI to configure the TC priority.


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**Table 5-15. EDMA3 Channel Controller (EDMA3CC) Registers (continued)**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS | EDMA3_1 Channel Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| **Global Channel Registers** | | | |
| 0x01C0 1000 | 0x01E3 1000 | ER | Event Register |
| 0x01C0 1008 | 0x01E3 1008 | ECR | Event Clear Register |
| 0x01C0 1010 | 0x01E3 1010 | ESR | Event Set Register |
| 0x01C0 1018 | 0x01E3 1018 | CER | Chained Event Register |
| 0x01C0 1020 | 0x01E3 1020 | EER | Event Enable Register |
| 0x01C0 1028 | 0x01E3 1028 | EECR | Event Enable Clear Register |
| 0x01C0 1030 | 0x01E3 1030 | EESR | Event Enable Set Register |
| 0x01C0 1038 | 0x01E3 1038 | SER | Secondary Event Register |
| 0x01C0 1040 | 0x01E3 1040 | SECR | Secondary Event Clear Register |
| 0x01C0 1050 | 0x01E3 1050 | IER | Interrupt Enable Register |
| 0x01C0 1058 | 0x01E3 1058 | IECR | Interrupt Enable Clear Register |
| 0x01C0 1060 | 0x01E3 1060 | IESR | Interrupt Enable Set Register |
| 0x01C0 1068 | 0x01E3 1068 | IPR | Interrupt Pending Register |
| 0x01C0 1070 | 0x01E3 1070 | ICR | Interrupt Clear Register |
| 0x01C0 1078 | 0x01E3 1078 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 1080 | 0x01E3 1080 | QER | QDMA Event Register |
| 0x01C0 1084 | 0x01E3 1084 | QEER | QDMA Event Enable Register |
| 0x01C0 1088 | 0x01E3 1088 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 108C | 0x01E3 108C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 1090 | 0x01E3 1090 | QSER | QDMA Secondary Event Register |
| 0x01C0 1094 | 0x01E3 1094 | QSECR | QDMA Secondary Event Clear Register |
| **Shadow Region 0 Channel Registers** | | | |
| 0x01C0 2000 | 0x01E3 2000 | ER | Event Register |
| 0x01C0 2008 | 0x01E3 2008 | ECR | Event Clear Register |
| 0x01C0 2010 | 0x01E3 2010 | ESR | Event Set Register |
| 0x01C0 2018 | 0x01E3 2018 | CER | Chained Event Register |
| 0x01C0 2020 | 0x01E3 2020 | EER | Event Enable Register |
| 0x01C0 2028 | 0x01E3 2028 | EECR | Event Enable Clear Register |
| 0x01C0 2030 | 0x01E3 2030 | EESR | Event Enable Set Register |
| 0x01C0 2038 | 0x01E3 2038 | SER | Secondary Event Register |
| 0x01C0 2040 | 0x01E3 2040 | SECR | Secondary Event Clear Register |
| 0x01C0 2050 | 0x01E3 2050 | IER | Interrupt Enable Register |
| 0x01C0 2058 | 0x01E3 2058 | IECR | Interrupt Enable Clear Register |
| 0x01C0 2060 | 0x01E3 2060 | IESR | Interrupt Enable Set Register |
| 0x01C0 2068 | 0x01E3 2068 | IPR | Interrupt Pending Register |
| 0x01C0 2070 | 0x01E3 2070 | ICR | Interrupt Clear Register |
| 0x01C0 2078 | 0x01E3 2078 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 2080 | 0x01E3 2080 | QER | QDMA Event Register |
| 0x01C0 2084 | 0x01E3 2084 | QEER | QDMA Event Enable Register |
| 0x01C0 2088 | 0x01E3 2088 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 208C | 0x01E3 208C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2090 | 0x01E3 2090 | QSER | QDMA Secondary Event Register |
| 0x01C0 2094 | 0x01E3 2094 | QSECR | QDMA Secondary Event Clear Register |

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**Table 5-15. EDMA3 Channel Controller (EDMA3CC) Registers (continued)**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS | EDMA3_1 Channel Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| **Shadow Region 1 Channel Registers** | | | |
| 0x01C0 2200 | 0x01E3 2200 | ER | Event Register |
| 0x01C0 2208 | 0x01E3 2208 | ECR | Event Clear Register |
| 0x01C0 2210 | 0x01E3 2210 | ESR | Event Set Register |
| 0x01C0 2218 | 0x01E3 2218 | CER | Chained Event Register |
| 0x01C0 2220 | 0x01E3 2220 | EER | Event Enable Register |
| 0x01C0 2228 | 0x01E3 2228 | EECR | Event Enable Clear Register |
| 0x01C0 2230 | 0x01E3 2230 | EESR | Event Enable Set Register |
| 0x01C0 2238 | 0x01E3 2238 | SER | Secondary Event Register |
| 0x01C0 2240 | 0x01E3 2240 | SECR | Secondary Event Clear Register |
| 0x01C0 2250 | 0x01E3 2250 | IER | Interrupt Enable Register |
| 0x01C0 2258 | 0x01E3 2258 | IECR | Interrupt Enable Clear Register |
| 0x01C0 2260 | 0x01E3 2260 | IESR | Interrupt Enable Set Register |
| 0x01C0 2268 | 0x01E3 2268 | IPR | Interrupt Pending Register |
| 0x01C0 2270 | 0x01E3 2270 | ICR | Interrupt Clear Register |
| 0x01C0 2278 | 0x01E3 2278 | IEVAL | Interrupt Evaluate Register |
| 0x01C0 2280 | 0x01E3 2280 | QER | QDMA Event Register |
| 0x01C0 2284 | 0x01E3 2284 | QEER | QDMA Event Enable Register |
| 0x01C0 2288 | 0x01E3 2288 | QEECR | QDMA Event Enable Clear Register |
| 0x01C0 228C | 0x01E3 228C | QEESR | QDMA Event Enable Set Register |
| 0x01C0 2290 | 0x01E3 2290 | QSER | QDMA Secondary Event Register |
| 0x01C0 2294 | 0x01E3 2294 | QSECR | QDMA Secondary Event Clear Register |
| 0x01C0 4000 - 0x01C0 4FFF | 0x01E3 4000 - 0x01E3 4FFF | — | Parameter RAM (PaRAM) |

**Table 5-16. EDMA3 Transfer Controller (EDMA3TC) Registers**

| EDMA3_0 Transfer Controller 0 BYTE ADDRESS | EDMA3_0 Transfer Controller 1 BYTE ADDRESS | EDMA3_1 Transfer Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|---|
| 0x01C0 8000 | 0x01C0 8400 | 0x01E3 8000 | PID | Peripheral Identification Register |
| 0x01C0 8004 | 0x01C0 8404 | 0x01E3 8004 | TCCFG | EDMA3TC Configuration Register |
| 0x01C0 8100 | 0x01C0 8500 | 0x01E3 8100 | TCSTAT | EDMA3TC Channel Status Register |
| 0x01C0 8120 | 0x01C0 8520 | 0x01E3 8120 | ERRSTAT | Error Status Register |
| 0x01C0 8124 | 0x01C0 8524 | 0x01E3 8124 | ERREN | Error Enable Register |
| 0x01C0 8128 | 0x01C0 8528 | 0x01E3 8128 | ERRCLR | Error Clear Register |
| 0x01C0 812C | 0x01C0 852C | 0x01E3 812C | ERRDET | Error Details Register |
| 0x01C0 8130 | 0x01C0 8530 | 0x01E3 8130 | ERRCMD | Error Interrupt Command Register |
| 0x01C0 8140 | 0x01C0 8540 | 0x01E3 8140 | RDRATE | Read Command Rate Register |
| 0x01C0 8240 | 0x01C0 8640 | 0x01E3 8240 | SAOPT | Source Active Options Register |
| 0x01C0 8244 | 0x01C0 8644 | 0x01E3 8244 | SASRC | Source Active Source Address Register |
| 0x01C0 8248 | 0x01C0 8648 | 0x01E3 8248 | SACNT | Source Active Count Register |
| 0x01C0 824C | 0x01C0 864C | 0x01E3 824C | SADST | Source Active Destination Address Register |
| 0x01C0 8250 | 0x01C0 8650 | 0x01E3 8250 | SABIDX | Source Active B-Index Register |
| 0x01C0 8254 | 0x01C0 8654 | 0x01E3 8254 | SAMPPRXY | Source Active Memory Protection Proxy Register |
| 0x01C0 8258 | 0x01C0 8658 | 0x01E3 8258 | SACNTRLD | Source Active Count Reload Register |
| 0x01C0 825C | 0x01C0 865C | 0x01E3 825C | SASRCBREF | Source Active Source Address B-Reference Register |
| 0x01C0 8260 | 0x01C0 8660 | 0x01E3 8260 | SADSTBREF | Source Active Destination Address B-Reference Register |


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**Table 5-16. EDMA3 Transfer Controller (EDMA3TC) Registers (continued)**

| EDMA3_0 Transfer Controller 0 BYTE ADDRESS | EDMA3_0 Transfer Controller 1 BYTE ADDRESS | EDMA3_1 Transfer Controller 0 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|---|
| 0x01C0 8280 | 0x01C0 8680 | 0x01E3 8280 | DFCNTRLD | Destination FIFO Set Count Reload Register |
| 0x01C0 8284 | 0x01C0 8684 | 0x01E3 8284 | DFSRCBREF | Destination FIFO Set Source Address B-Reference Register |
| 0x01C0 8288 | 0x01C0 8688 | 0x01E3 8288 | DFDSTBREF | Destination FIFO Set Destination Address B-Reference Register |
| 0x01C0 8300 | 0x01C0 8700 | 0x01E3 8300 | DFOPT0 | Destination FIFO Options Register 0 |
| 0x01C0 8304 | 0x01C0 8704 | 0x01E3 8304 | DFSRC0 | Destination FIFO Source Address Register 0 |
| 0x01C0 8308 | 0x01C0 8708 | 0x01E3 8308 | DFCNT0 | Destination FIFO Count Register 0 |
| 0x01C0 830C | 0x01C0 870C | 0x01E3 830C | DFDST0 | Destination FIFO Destination Address Register 0 |
| 0x01C0 8310 | 0x01C0 8710 | 0x01E3 8310 | DFBIDX0 | Destination FIFO B-Index Register 0 |
| 0x01C0 8314 | 0x01C0 8714 | 0x01E3 8314 | DFMPPRXY0 | Destination FIFO Memory Protection Proxy Register 0 |
| 0x01C0 8340 | 0x01C0 8740 | 0x01E3 8340 | DFOPT1 | Destination FIFO Options Register 1 |
| 0x01C0 8344 | 0x01C0 8744 | 0x01E3 8344 | DFSRC1 | Destination FIFO Source Address Register 1 |
| 0x01C0 8348 | 0x01C0 8748 | 0x01E3 8348 | DFCNT1 | Destination FIFO Count Register 1 |
| 0x01C0 834C | 0x01C0 874C | 0x01E3 834C | DFDST1 | Destination FIFO Destination Address Register 1 |
| 0x01C0 8350 | 0x01C0 8750 | 0x01E3 8350 | DFBIDX1 | Destination FIFO B-Index Register 1 |
| 0x01C0 8354 | 0x01C0 8754 | 0x01E3 8354 | DFMPPRXY1 | Destination FIFO Memory Protection Proxy Register 1 |
| 0x01C0 8380 | 0x01C0 8780 | 0x01E3 8380 | DFOPT2 | Destination FIFO Options Register 2 |
| 0x01C0 8384 | 0x01C0 8784 | 0x01E3 8384 | DFSRC2 | Destination FIFO Source Address Register 2 |
| 0x01C0 8388 | 0x01C0 8788 | 0x01E3 8388 | DFCNT2 | Destination FIFO Count Register 2 |
| 0x01C0 838C | 0x01C0 878C | 0x01E3 838C | DFDST2 | Destination FIFO Destination Address Register 2 |
| 0x01C0 8390 | 0x01C0 8790 | 0x01E3 8390 | DFBIDX2 | Destination FIFO B-Index Register 2 |
| 0x01C0 8394 | 0x01C0 8794 | 0x01E3 8394 | DFMPPRXY2 | Destination FIFO Memory Protection Proxy Register 2 |
| 0x01C0 83C0 | 0x01C0 87C0 | 0x01E3 83C0 | DFOPT3 | Destination FIFO Options Register 3 |
| 0x01C0 83C4 | 0x01C0 87C4 | 0x01E3 83C4 | DFSRC3 | Destination FIFO Source Address Register 3 |
| 0x01C0 83C8 | 0x01C0 87C8 | 0x01E3 83C8 | DFCNT3 | Destination FIFO Count Register 3 |
| 0x01C0 83CC | 0x01C0 87CC | 0x01E3 83CC | DFDST3 | Destination FIFO Destination Address Register 3 |
| 0x01C0 83D0 | 0x01C0 87D0 | 0x01E3 83D0 | DFBIDX3 | Destination FIFO B-Index Register 3 |
| 0x01C0 83D4 | 0x01C0 87D4 | 0x01E3 83D4 | DFMPPRXY3 | Destination FIFO Memory Protection Proxy Register 3 |

Table 5-17 shows an abbreviation of the set of registers which make up the parameter set for each of 128 EDMA3 events. Each of the parameter register sets consist of 8 32-bit word entries. Table 5-18 shows the parameter set entry registers with relative memory address locations within each of the parameter sets.

**Table 5-17. EDMA3 Parameter Set RAM**

| EDMA3_0 Channel Controller 0 BYTE ADDRESS RANGE | EDMA3_1 Channel Controller 0 BYTE ADDRESS RANGE | DESCRIPTION |
|---|---|---|
| 0x01C0 4000 - 0x01C0 401F | 0x01E3 4000 - 0x01E3 401F | Parameters Set 0 (8 32-bit words) |
| 0x01C0 4020 - 0x01C0 403F | 0x01E3 4020 - 0x01E3 403F | Parameters Set 1 (8 32-bit words) |
| 0x01C0 4040 - 0x01CC0 405F | 0x01E3 4040 - 0x01CE3 405F | Parameters Set 2 (8 32-bit words) |
| 0x01C0 4060 - 0x01C0 407F | 0x01E3 4060 - 0x01E3 407F | Parameters Set 3 (8 32-bit words) |
| 0x01C0 4080 - 0x01C0 409F | 0x01E3 4080 - 0x01E3 409F | Parameters Set 4 (8 32-bit words) |
| 0x01C0 40A0 - 0x01C0 40BF | 0x01E3 40A0 - 0x01E3 40BF | Parameters Set 5 (8 32-bit words) |
| ... | ... | ... |
| 0x01C0 4FC0 - 0x01C0 4FDF | 0x01E3 4FC0 - 0x01E3 4FDF | Parameters Set 126 (8 32-bit words) |
| 0x01C0 4FE0 - 0x01C0 4FFF | 0x01E3 4FE0 - 0x01E3 4FFF | Parameters Set 127 (8 32-bit words) |

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**Table 5-18. Parameter Set Entries**

| OFFSET BYTE ADDRESS WITHIN THE PARAMETER SET | ACRONYM | PARAMETER ENTRY |
|---|---|---|
| 0x0000 | OPT | Option |
| 0x0004 | SRC | Source Address |
| 0x0008 | A_B_CNT | A Count, B Count |
| 0x000C | DST | Destination Address |
| 0x0010 | SRC_DST_BIDX | Source B Index, Destination B Index |
| 0x0014 | LINK_BCNTRLD | Link Address, B Count Reload |
| 0x0018 | SRC_DST_CIDX | Source C Index, Destination C Index |
| 0x001C | CCNT | C Count |


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## 5.10 External Memory Interface A (EMIFA)

EMIFA is one of two external memory interfaces supported on the device. It is primarily intended to support asynchronous memory types, such as NAND and NOR flash and Asynchronous SRAM. However on this device, EMIFA also provides a secondary interface to SDRAM.

### *5.10.1 EMIFA Asynchronous Memory Support*

EMIFA supports asynchronous:

- SRAM memories
- NAND Flash memories
- NOR Flash memories

The EMIFA data bus width is up to 16-bits.The device supports up to 23 address lines and two external wait/interrupt inputs. Up to four asynchronous chip selects are supported by EMIFA (EMA_CS[5:2]).

Each chip select has the following individually programmable attributes:

- Data Bus Width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn around time
- Extended Wait Option With Programmable Timeout
- Select Strobe Option
- NAND flash controller supports 1-bit and 4-bit ECC calculation on blocks of 512 bytes.

### *5.10.2 EMIFA Synchronous DRAM Memory Support*

The device supports 16-bit SDRAM in addition to the asynchronous memories listed in Section 5.10.1. It has a single SDRAM chip select (EMA_CS[0]). SDRAM configurations that are supported are:

- One, Two, and Four Bank SDRAM devices
- Devices with Eight, Nine, Ten, and Eleven Column Address
- CAS Latency of two or three clock cycles
- Sixteen Bit Data Bus Width

Additionally, the SDRAM interface of EMIFA supports placing the SDRAM in Self Refresh and Powerdown Modes. Self Refresh mode allows the SDRAM to be put into a low power state while still retaining memory contents; since the SDRAM will continue to refresh itself even without clocks from the device. Powerdown mode achieves even lower power, except the device must periodically wake the SDRAM up and issue refreshes if data retention is required.

Finally, note that the EMIFA does not support Mobile SDRAM devices.

Table 5-19 shows the supported SDRAM configurations for EMIFA.

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**Table 5-19. EMIFA Supported SDRAM Configurations(1)**

| SDRAM Memory Data Bus Width (bits) | Number of Memories | EMIFA Data Bus Size (bits) | Rows | Columns | Banks | Total Memory (Mbits) | Total Memory (Mbytes) | Memory Density (Mbits) |
|---|---|---|---|---|---|---|---|---|
| 16 | 1 | 16 | 16 | 8 | 1 | 256 | 32 | 256 |
| | 1 | 16 | 16 | 8 | 2 | 512 | 64 | 512 |
| | 1 | 16 | 16 | 8 | 4 | 1024 | 128 | 1024 |
| | 1 | 16 | 16 | 9 | 1 | 512 | 64 | 512 |
| | 1 | 16 | 16 | 9 | 2 | 1024 | 128 | 1024 |
| | 1 | 16 | 16 | 9 | 4 | 2048 | 256 | 2048 |
| | 1 | 16 | 16 | 10 | 1 | 1024 | 128 | 1024 |
| | 1 | 16 | 16 | 10 | 2 | 2048 | 256 | 2048 |
| | 1 | 16 | 16 | 10 | 4 | 4096 | 512 | 4096 |
| | 1 | 16 | 16 | 11 | 1 | 2048 | 256 | 2048 |
| | 1 | 16 | 16 | 11 | 2 | 4096 | 512 | 4096 |
| | 1 | 16 | 15 | 11 | 4 | 4096 | 512 | 4096 |
| 8 | 2 | 16 | 16 | 8 | 1 | 256 | 32 | 128 |
| | 2 | 16 | 16 | 8 | 2 | 512 | 64 | 256 |
| | 2 | 16 | 16 | 8 | 4 | 1024 | 128 | 512 |
| | 2 | 16 | 16 | 9 | 1 | 512 | 64 | 256 |
| | 2 | 16 | 16 | 9 | 2 | 1024 | 128 | 512 |
| | 2 | 16 | 16 | 9 | 4 | 2048 | 256 | 1024 |
| | 2 | 16 | 16 | 10 | 1 | 1024 | 128 | 512 |
| | 2 | 16 | 16 | 10 | 2 | 2048 | 256 | 1024 |
| | 2 | 16 | 16 | 10 | 4 | 4096 | 512 | 2048 |
| | 2 | 16 | 16 | 11 | 1 | 2048 | 256 | 1024 |
| | 2 | 16 | 16 | 11 | 2 | 4096 | 512 | 2048 |
| | 2 | 16 | 15 | 11 | 4 | 4096 | 512 | 2048 |

(1) The shaded cells indicate configurations that are possible on the EMIFA interface but as of this writing SDRAM memories capable of supporting these densities are not available in the market.

### 5.10.3 EMIFA SDRAM Loading Limitations

EMIFA supports SDRAM up to 100 MHz with up to two SDRAM or asynchronous memory loads. Additional loads will limit the SDRAM operation to lower speeds and the maximum speed should be confirmed by board simulation using IBIS models.

### 5.10.4 EMIFA Connection Examples

Figure 5-10 illustrates an example of how SDRAM, NOR, and NAND flash devices might be connected to EMIFA simultaneously. The SDRAM chip select must be EMA_CS[0]. Note that the NOR flash is connected to EMA_CS[2] and the NAND flash is connected to EMA_CS[3] in this example. Note that any type of asynchronous memory may be connected to EMA_CS[5:2].

The on-chip bootloader makes some assumptions on which chip select the contains the boot image, and this depends on the boot mode. For NOR boot mode; the on-chip bootloader requires that the image be stored in NOR flash on EMA_CS[2]. For NAND boot mode, the bootloader requires that the boot image is stored in NAND flash on EMA_CS[3]. It is always possible to have the image span multiple chip selects, but this must be supported by second stage boot code stored in the external flash.


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A likely use case with more than one EMIFA chip select used for NAND flash is illustrated in Figure 5-11. This figure shows how two multiplane NAND flash devices with two chip selects each would connect to the EMIFA. In this case if NAND is the boot memory, then the boot image needs to be stored in the NAND area selected by EMA_CS[3]. Part of the application image could spill over into the NAND regions selected by other EMIFA chip selects; but would rely on the code stored in the EMA_CS[3] area to bootload it.

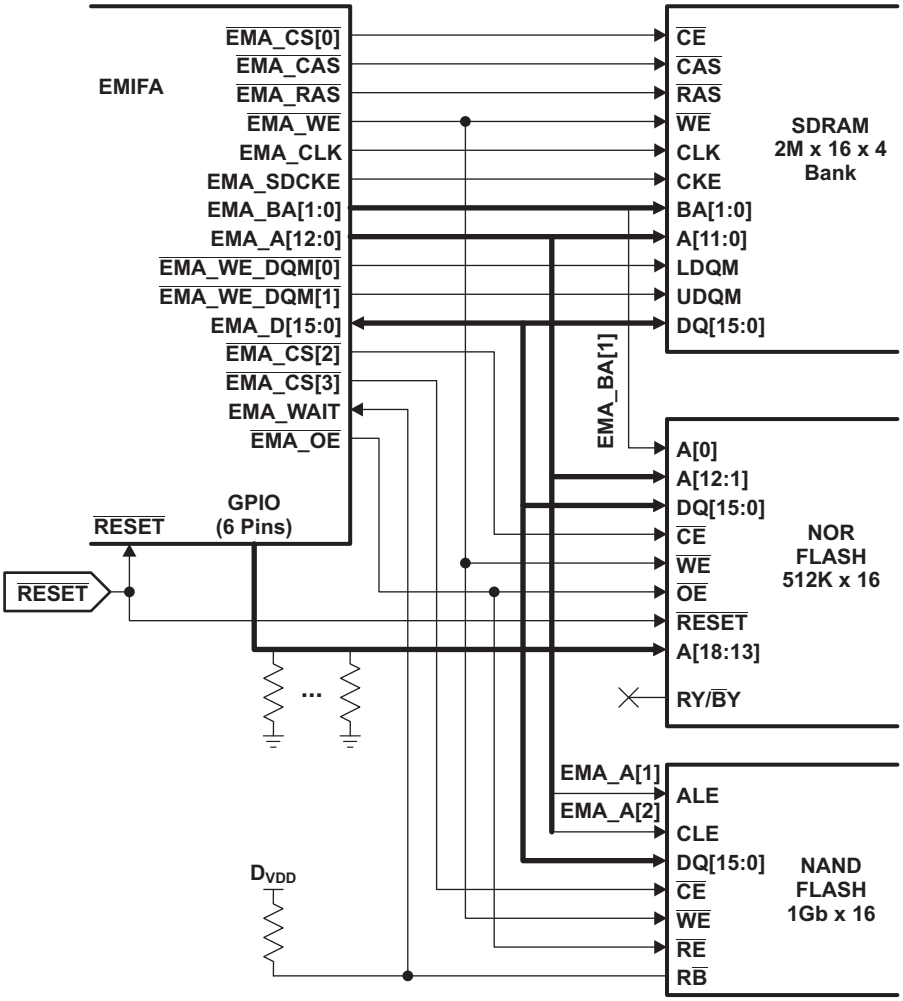


**Figure 5-10. Connection Diagram: SDRAM, NOR, NAND**

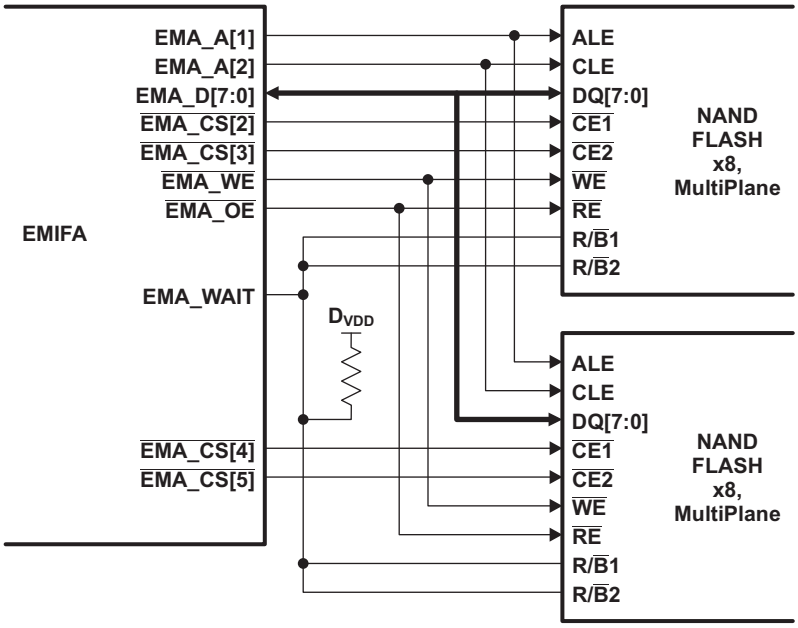


**Figure 5-11. EMIFA Connection Diagram: Multiple NAND Flash Planes**


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### 5.10.5 External Memory Interface Register Descriptions

**Table 5-20. External Memory Interface (EMIFA) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x6800 0000 | MIDR | Module ID Register |
| 0x6800 0004 | AWCC | Asynchronous Wait Cycle Configuration Register |
| 0x6800 0008 | SDCR | SDRAM Configuration Register |
| 0x6800 000C | SDRCR | SDRAM Refresh Control Register |
| 0x6800 0010 | CE2CFG | Asynchronous 1 Configuration Register |
| 0x6800 0014 | CE3CFG | Asynchronous 2 Configuration Register |
| 0x6800 0018 | CE4CFG | Asynchronous 3 Configuration Register |
| 0x6800 001C | CE5CFG | Asynchronous 4 Configuration Register |
| 0x6800 0020 | SDTIMR | SDRAM Timing Register |
| 0x6800 003C | SDSRETR | SDRAM Self Refresh Exit Timing Register |
| 0x6800 0040 | INTRAW | EMIFA Interrupt Raw Register |
| 0x6800 0044 | INTMSK | EMIFA Interrupt Mask Register |
| 0x6800 0048 | INTMSKSET | EMIFA Interrupt Mask Set Register |
| 0x6800 004C | INTMSKCLR | EMIFA Interrupt Mask Clear Register |
| 0x6800 0060 | NANDFCR | NAND Flash Control Register |
| 0x6800 0064 | NANDFSR | NAND Flash Status Register |
| 0x6800 0070 | NANDF1ECC | NAND Flash 1 ECC Register (CS2 Space) |
| 0x6800 0074 | NANDF2ECC | NAND Flash 2 ECC Register (CS3 Space) |
| 0x6800 0078 | NANDF3ECC | NAND Flash 3 ECC Register (CS4 Space) |
| 0x6800 007C | NANDF4ECC | NAND Flash 4 ECC Register (CS5 Space) |
| 0x6800 00BC | NAND4BITECCLOAD | NAND Flash 4-Bit ECC Load Register |
| 0x6800 00C0 | NAND4BITECC1 | NAND Flash 4-Bit ECC Register 1 |
| 0x6800 00C4 | NAND4BITECC2 | NAND Flash 4-Bit ECC Register 2 |
| 0x6800 00C8 | NAND4BITECC3 | NAND Flash 4-Bit ECC Register 3 |
| 0x6800 00CC | NAND4BITECC4 | NAND Flash 4-Bit ECC Register 4 |
| 0x6800 00D0 | NANDERRADD1 | NAND Flash 4-Bit ECC Error Address Register 1 |
| 0x6800 00D4 | NANDERRADD2 | NAND Flash 4-Bit ECC Error Address Register 2 |
| 0x6800 00D8 | NANDERRVAL1 | NAND Flash 4-Bit ECC Error Value Register 1 |
| 0x6800 00DC | NANDERRVAL2 | NAND Flash 4-Bit ECC Error Value Register 2 |

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### 5.10.6 EMIFA Electrical Data/Timing

Table 5-21 through Table 5-24 assume testing over recommended operating conditions.

**Table 5-21. Timing Requirements for EMIFA SDRAM Interface**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 19 | $t_{su(EMA_DV-EM_CLKH)}$ | Input setup time, read data valid on EMA_D[15:0] before EMA_CLK rising | 2 | | 3 | | 3 | | ns |
| 20 | $t_{h(CLKH-DIV)}$ | Input hold time, read data valid on EMA_D[15:0] after EMA_CLK rising | 1.6 | | 1.6 | | 1.6 | | ns |

**Table 5-22. Switching Characteristics for EMIFA SDRAM Interface**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(CLK)}$ | Cycle time, EMIF clock EMA_CLK | 10 | | 15 | | 20 | | ns |
| 2 | $t_{w(CLK)}$ | Pulse width, EMIF clock EMA_CLK high or low | 3 | | 5 | | 8 | | ns |
| 3 | $t_{d(CLKH-CSV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_CS[0]}$ valid | | 7 | | 9.5 | | 13 | ns |
| 4 | $t_{oh(CLKH-CSIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_CS[0]}$ invalid | 1 | | 1 | | 1 | | ns |
| 5 | $t_{d(CLKH-DQMV)}$ | Delay time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] valid | | 7 | | 9.5 | | 13 | ns |
| 6 | $t_{oh(CLKH-DQMIV)}$ | Output hold time, EMA_CLK rising to EMA_$\overline{WE}$_DQM[1:0] invalid | 1 | | 1 | | 1 | | ns |
| 7 | $t_{d(CLKH-AV)}$ | Delay time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] valid | | 7 | | 9.5 | | 13 | ns |
| 8 | $t_{oh(CLKH-AIV)}$ | Output hold time, EMA_CLK rising to EMA_A[12:0] and EMA_BA[1:0] invalid | 1 | | 1 | | 1 | | ns |
| 9 | $t_{d(CLKH-DV)}$ | Delay time, EMA_CLK rising to EMA_D[15:0] valid | | 7 | | 9.5 | | 13 | ns |
| 10 | $t_{oh(CLKH-DIV)}$ | Output hold time, EMA_CLK rising to EMA_D[15:0] invalid | 1 | | 1 | | 1 | | ns |
| 11 | $t_{d(CLKH-RASV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_RAS}$ valid | | 7 | | 9.5 | | 13 | ns |
| 12 | $t_{oh(CLKH-RASIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_RAS}$ invalid | 1 | | 1 | | 1 | | ns |
| 13 | $t_{d(CLKH-CASV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_CAS}$ valid | | 7 | | 9.5 | | 13 | ns |
| 14 | $t_{oh(CLKH-CASIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_CAS}$ invalid | 1 | | 1 | | 1 | | ns |
| 15 | $t_{d(CLKH-WEV)}$ | Delay time, EMA_CLK rising to $\overline{EMA_WE}$ valid | | 7 | | 9.5 | | 13 | ns |
| 16 | $t_{oh(CLKH-WEIV)}$ | Output hold time, EMA_CLK rising to $\overline{EMA_WE}$ invalid | 1 | | 1 | | 1 | | ns |
| 17 | $t_{dis(CLKH-DHZ)}$ | Delay time, EMA_CLK rising to EMA_D[15:0] tri-stated | | 7 | | 9.5 | | 13 | ns |
| 18 | $t_{ena(CLKH-DLZ)}$ | Output hold time, EMA_CLK rising to EMA_D[15:0] driving | 1 | | 1 | | 1 | | ns |


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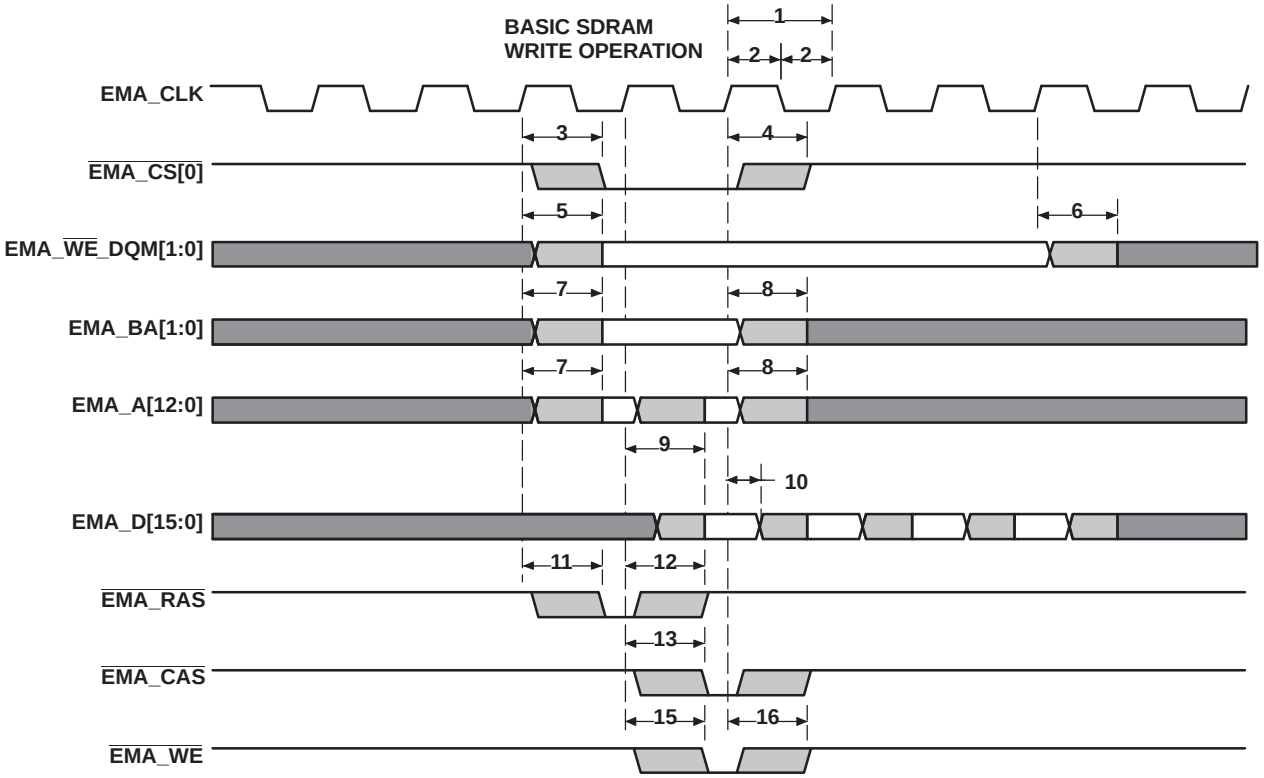


**Figure 5-12. EMIFA Basic SDRAM Write Operation**

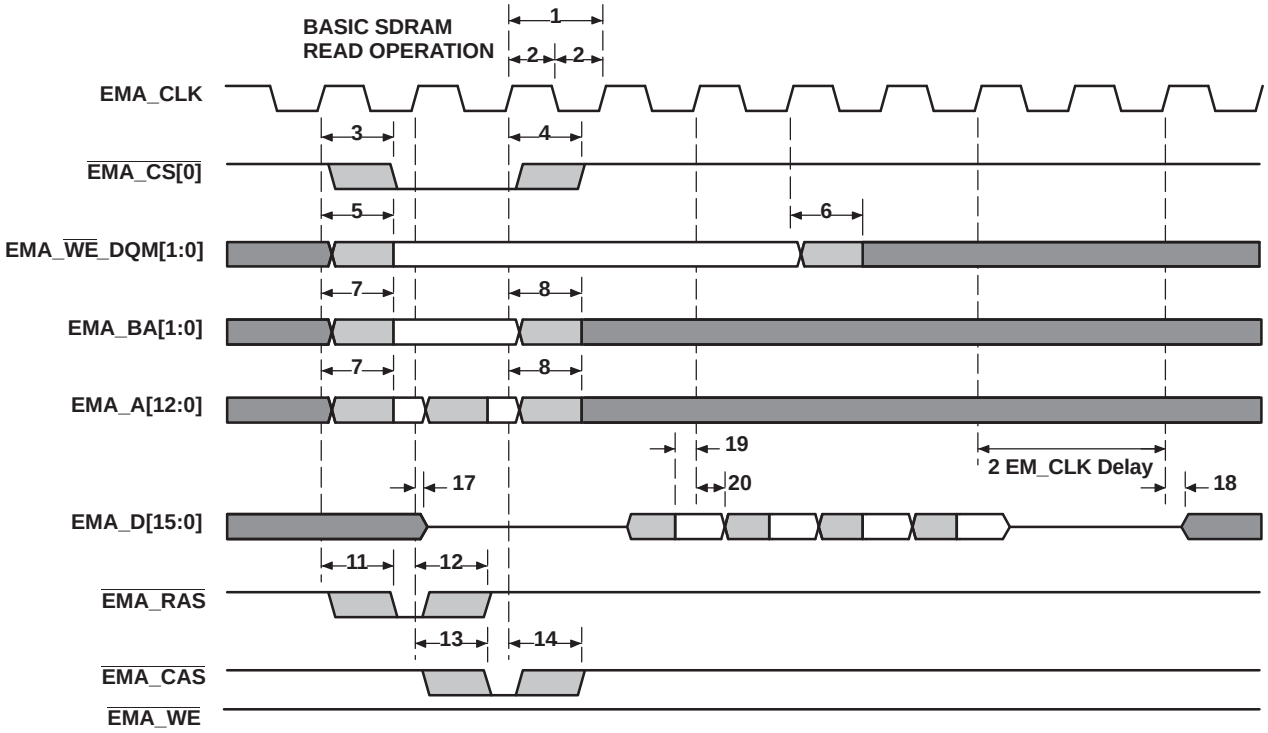


**Figure 5-13. EMIFA Basic SDRAM Read Operation**

**Table 5-23. Timing Requirements for EMIFA Asynchronous Memory Interface (1)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| **READS and WRITES** | | | | | | | | | |
| E | $t_{c(CLK)}$ | Cycle time, EMIFA module clock | 6.75 | | 15 | | 20 | | ns |
| 2 | $t_{w(EM_WAIT)}$ | Pulse duration, EM_WAIT assertion and deassertion | 2E | | 2E | | 2E | | ns |
| **READS** | | | | | | | | | |
| 12 | $t_{su(EMDV-EMOEH)}$ | Setup time, EM_D[15:0] valid before $\overline{EM_OE}$ high | 3 | | 5 | | 7 | | ns |
| 13 | $t_{h(EMOEH-EMDIV)}$ | Hold time, EM_D[15:0] valid after $\overline{EM_OE}$ high | 0 | | 0 | | 0 | | ns |
| 14 | $t_{su\ (EMOEL-EMWAIT)}$ | Setup Time, EM_WAIT asserted before end of Strobe Phase(2) | 4E+3 | | 4E+3 | | 4E+3 | | ns |
| **WRITES** | | | | | | | | | |
| 28 | $t_{su\ (EMWEL-EMWAIT)}$ | Setup Time, EM_WAIT asserted before end of Strobe Phase(2) | 4E+3 | | 4E+3 | | 4E+3 | | ns |

(1) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL0 output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns

(2) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAIT must be asserted to add extended wait states. Figure 5-16 and Figure 5-17 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.


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## Table 5-24. Switching Characteristics for EMIFA Asynchronous Memory Interface (1) (2) (3)

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | Nom | MAX | |
| **READS and WRITES** | | | | | | |
| 1 | $t_{d(TURNAROUND)}$ | Turn around time | (TA)*E - 3 | (TA)*E | (TA)*E + 3 | ns |
| **READS** | | | | | | |
| 3 | $t_{c(EMRCYCLE)}$ | EMIF read cycle time (EW = 0) | (RS+RST+RH)*E - 3 | (RS+RST+RH)*E | (RS+RST+RH)*E + 3 | ns |
| | | EMIF read cycle time (EW = 1) | (RS+RST+RH+(EWC*16))*E - 3 | (RS+RST+RH+(EWC*16))*E | (RS+RST+RH+(EWC*16))*E + 3 | ns |
| 4 | $t_{su(EMCEL-EMOEL)}$ | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS = 0) | (RS)*E-3 | (RS)*E | (RS)*E+3 | ns |
| | | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_OE}$ low (SS = 1) | -3 | 0 | +3 | ns |
| 5 | $t_{h(EMOEH-EMCEH)}$ | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 0) | (RH)*E - 3 | (RH)*E | (RH)*E + 3 | ns |
| | | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 1) | -3 | 0 | +3 | ns |
| 6 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_OE}$ low | (RS)*E-3 | (RS)*E | (RS)*E+3 | ns |
| 7 | $t_{h(EMOEH-EMBAIV)}$ | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_BA[1:0]}$ invalid | (RH)*E-3 | (RH)*E | (RH)*E+3 | ns |
| 8 | $t_{su(EMBAV-EMOEL)}$ | Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_OE}$ low | (RS)*E-3 | (RS)*E | (RS)*E+3 | ns |
| 9 | $t_{h(EMOEH-EMAIV)}$ | Output hold time, $\overline{EMA_OE}$ high to $\overline{EMA_A[13:0]}$ invalid | (RH)*E-3 | (RH)*E | (RH)*E+3 | ns |
| 10 | $t_{w(EMOEL)}$ | $\overline{EMA_OE}$ active low width (EW = 0) | (RST)*E-3 | (RST)*E | (RST)*E+3 | ns |
| | | $\overline{EMA_OE}$ active low width (EW = 1) | (RST+(EWC*16))*E-3 | (RST+(EWC*16))*E | (RST+(EWC*16))*E+3 | ns |
| 11 | $t_{d(EMWAITH-EMOEH)}$ | Delay time from EMA_WAIT deasserted to $\overline{EMA_OE}$ high | 3E-3 | 4E | 4E+3 | ns |
| **WRITES** | | | | | | |
| 15 | $t_{c(EMWCYCLE)}$ | EMIF write cycle time (EW = 0) | (WS+WST+WH)*E-3 | (WS+WST+WH)*E | (WS+WST+WH)*E+3 | ns |
| | | EMIF write cycle time (EW = 1) | (WS+WST+WH+(EWC*16))*E - 3 | (WS+WST+WH+(EWC*16))*E | (WS+WST+WH+(EWC*16))*E + 3 | ns |
| 16 | $t_{su(EMCEL-EMWEL)}$ | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS = 0) | (WS)*E - 3 | (WS)*E | (WS)*E + 3 | ns |
| | | Output setup time, $\overline{EMA_CE[5:2]}$ low to $\overline{EMA_WE}$ low (SS = 1) | -3 | 0 | +3 | ns |
| 17 | $t_{h(EMWEH-EMCEH)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 0) | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| | | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_CE[5:2]}$ high (SS = 1) | -3 | 0 | +3 | ns |
| 18 | $t_{su(EMDQMV-EMWEL)}$ | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 19 | $t_{h(EMWEH-EMDQMIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 20 | $t_{su(EMBAV-EMWEL)}$ | Output setup time, $\overline{EMA_BA[1:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 21 | $t_{h(EMWEH-EMBAIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_BA[1:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |
| 22 | $t_{su(EMAV-EMWEL)}$ | Output setup time, $\overline{EMA_A[13:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 23 | $t_{h(EMWEH-EMAIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_A[13:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |

(1) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait Cycle Configuration Registers. These support the following range of values: TA[4-1], RS[16-1], RST[64-1], RH[8-1], WS[16-1], WST[64-1], WH[8-1], and MEW[1-256].
(2) E = EMA_CLK period or in ns. EMA_CLK is selected either as SYSCLK3 or the PLL0 output clock divided by 4.5. As an example, when SYSCLK3 is selected and set to 100MHz, E=10ns.
(3) EWC = external wait cycles determined by EMA_WAIT input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

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**Table 5-24. Switching Characteristics for EMIFA Asynchronous Memory Interface (1) (2) (3) (continued)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | Nom | MAX | |
| 24 | $t_{w(EMWEL)}$ | $\overline{EMA_WE}$ active low width (EW = 0) | (WST)*E-3 | (WST)*E | (WST)*E+3 | ns |
| | | $\overline{EMA_WE}$ active low width (EW = 1) | (WST+(EWC*16))*E-3 | (WST+(EWC*16))*E | (WST+(EWC*16))*E+3 | ns |
| 25 | $t_{d(EMWAITH-EMWEH)}$ | Delay time from EMA_WAIT deasserted to $\overline{EMA_WE}$ high | 3E-3 | 4E | 4E+3 | ns |
| 26 | $t_{su(EMDV-EMWEL)}$ | Output setup time, $\overline{EMA_D[15:0]}$ valid to $\overline{EMA_WE}$ low | (WS)*E-3 | (WS)*E | (WS)*E+3 | ns |
| 27 | $t_{h(EMWEH-EMDIV)}$ | Output hold time, $\overline{EMA_WE}$ high to $\overline{EMA_D[15:0]}$ invalid | (WH)*E-3 | (WH)*E | (WH)*E+3 | ns |

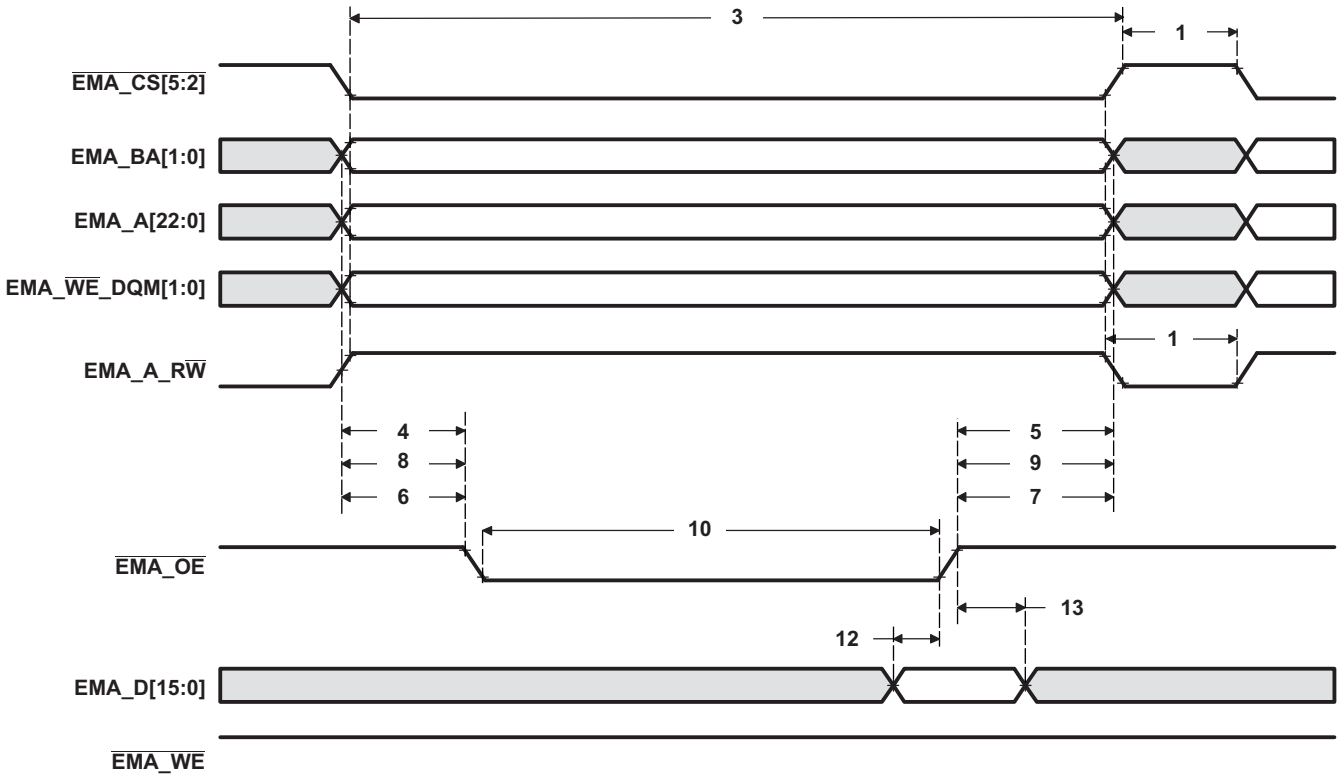


**Figure 5-14. Asynchronous Memory Read Timing for EMIFA**


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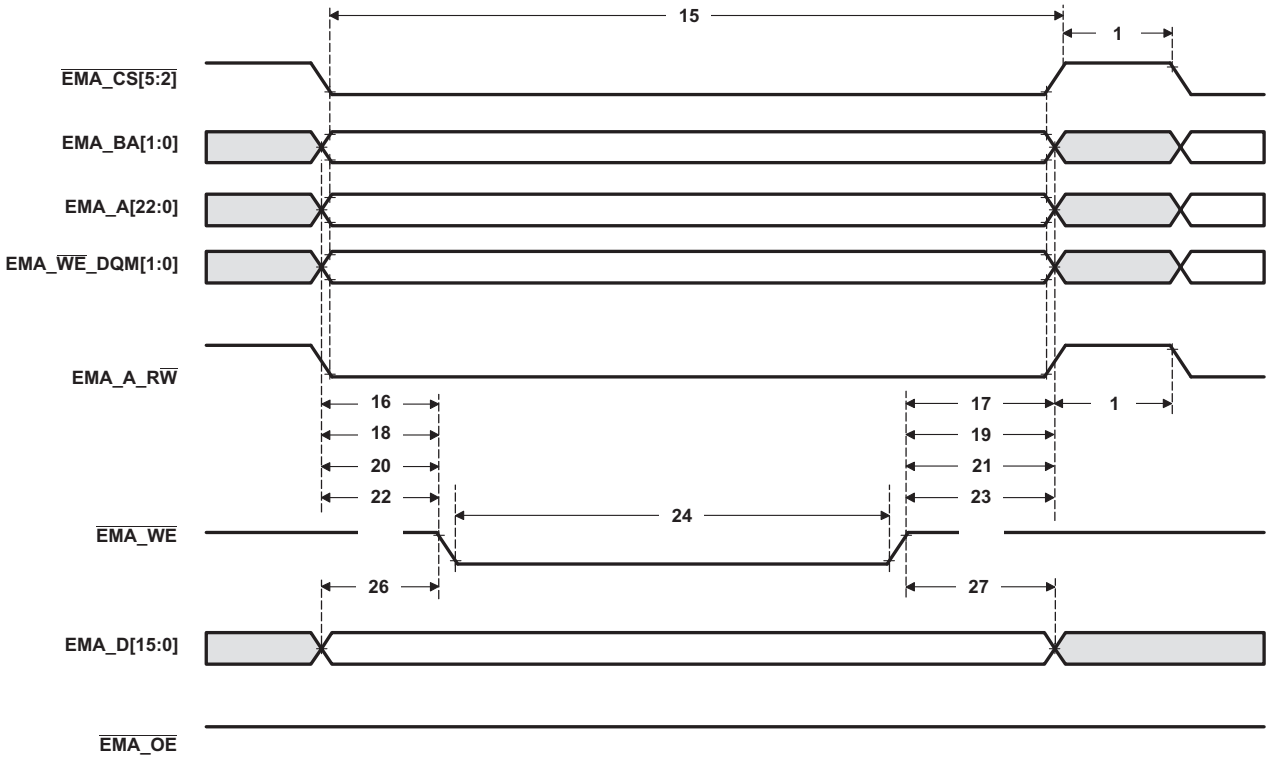


**Figure 5-15. Asynchronous Memory Write Timing for EMIFA**

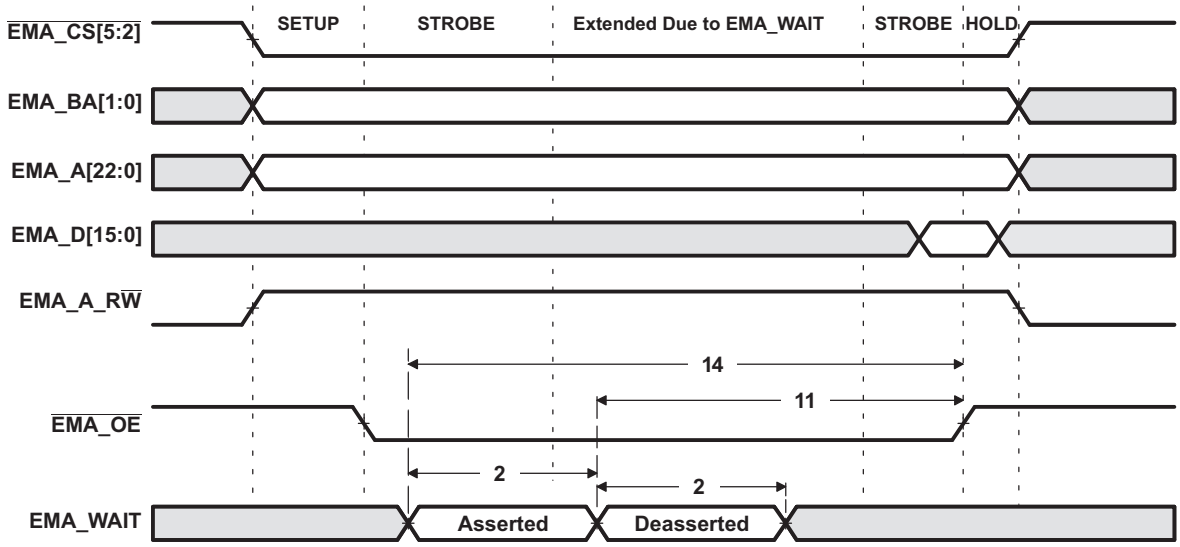


**Figure 5-16. EMA_WAIT Read Timing Requirements**

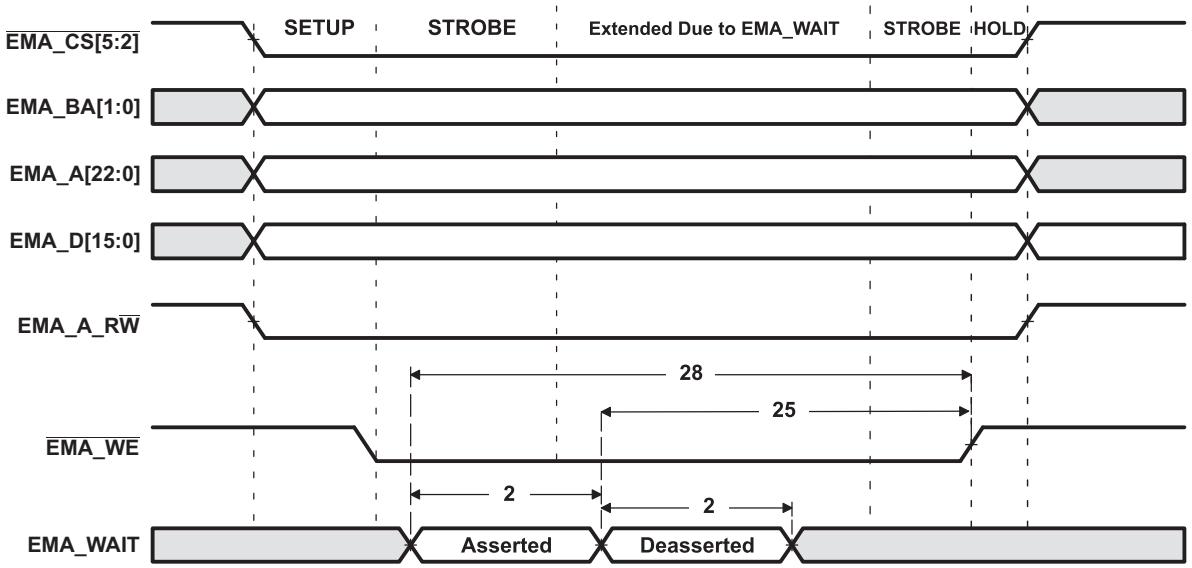


**Figure 5-17. EMA_WAIT Write Timing Requirements**


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## 5.11 DDR2/mDDR Controller

The DDR2/mDDR Memory Controller is a dedicated interface to DDR2/mDDR SDRAM. It supports JESD79-2A standard compliant DDR2 SDRAM devices and compliant Mobile DDR SDRAM devices.

The DDR2/mDDR Memory Controller support the following features:

- JESD79-2A standard compliant DDR2 SDRAM
- Mobile DDR SDRAM
- 512 MByte memory space for DDR2
- 256 MByte memory space for mDDR
- CAS latencies:
  - DDR2: 2, 3, 4 and 5
  - mDDR: 2 and 3
- Internal banks:
  - DDR2: 1, 2, 4 and 8
  - mDDR:1, 2 and 4
- Burst length: 8
- Burst type: sequential
- 1 chip select (CS) signal
- Page sizes: 256, 512, 1024 and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Partial array self-refresh (for mDDR)
- Power down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little endian

### *5.11.1 DDR2/mDDR Memory Controller Electrical Data/Timing*

**Table 5-25. Switching Characteristics Over Recommended Operating Conditions for DDR2/mDDR Memory Controller**

| No. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(DDR_CLK)}$ | Cycle time, DDR_CLKP / DDR_CLKN | DDR2 | 125 | 156 | 125 | 150 | —(1) | —(1) | MHz |
| | | | mDDR | 105 | 150 | 100 | 133 | 95 | 133 | |

(1) DDR2 is not supported at this voltage operating point.

### 5.11.2 DDR2/mDDR Controller Register Description(s)

**Table 5-26. DDR2/mDDR Controller Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0xB000 0000 | REVID | Revision ID Register |
| 0xB000 0004 | SDRSTAT | SDRAM Status Register |
| 0xB000 0008 | SDCR | SDRAM Configuration Register |
| 0xB000 000C | SDRCR | SDRAM Refresh Control Register |
| 0xB000 0010 | SDTIMR1 | SDRAM Timing Register 1 |
| 0xB000 0014 | SDTIMR2 | SDRAM Timing Register 2 |
| 0xB000 001C | SDCR2 | SDRAM Configuration Register 2 |
| 0xB000 0020 | PBBPR | Peripheral Bus Burst Priority Register |
| 0xB000 0040 | PC1 | Performance Counter 1 Registers |
| 0xB000 0044 | PC2 | Performance Counter 2 Register |
| 0xB000 0048 | PCC | Performance Counter Configuration Register |
| 0xB000 004C | PCMRS | Performance Counter Master Region Select Register |
| 0xB000 0050 | PCT | Performance Counter Time Register |
| 0xB000 00C0 | IRR | Interrupt Raw Register |
| 0xB000 00C4 | IMR | Interrupt Mask Register |
| 0xB000 00C8 | IMSR | Interrupt Mask Set Register |
| 0xB000 00CC | IMCR | Interrupt Mask Clear Register |
| 0xB000 00E4 | DRPYC1R | DDR PHY Control Register 1 |
| 0x01E2 C000 | VTPIO_CTL | VTP IO Control Register |

### 5.11.3 DDR2/mDDR Interface

This section provides the timing specification for the DDR2/mDDR interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2/mDDR memory system without the need for a complex timing closure process. For more information regarding guidelines for using this DDR2/mDDR specification, *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* (SPRAAV0).

#### 5.11.3.1 DDR2/mDDR Interface Schematic

Figure 5-18 shows the DDR2/mDDR interface schematic for a single-memory DDR2/mDDR system. The dual-memory system shown in Figure 5-19. Pin numbers for the device can be obtained from the pin description section.


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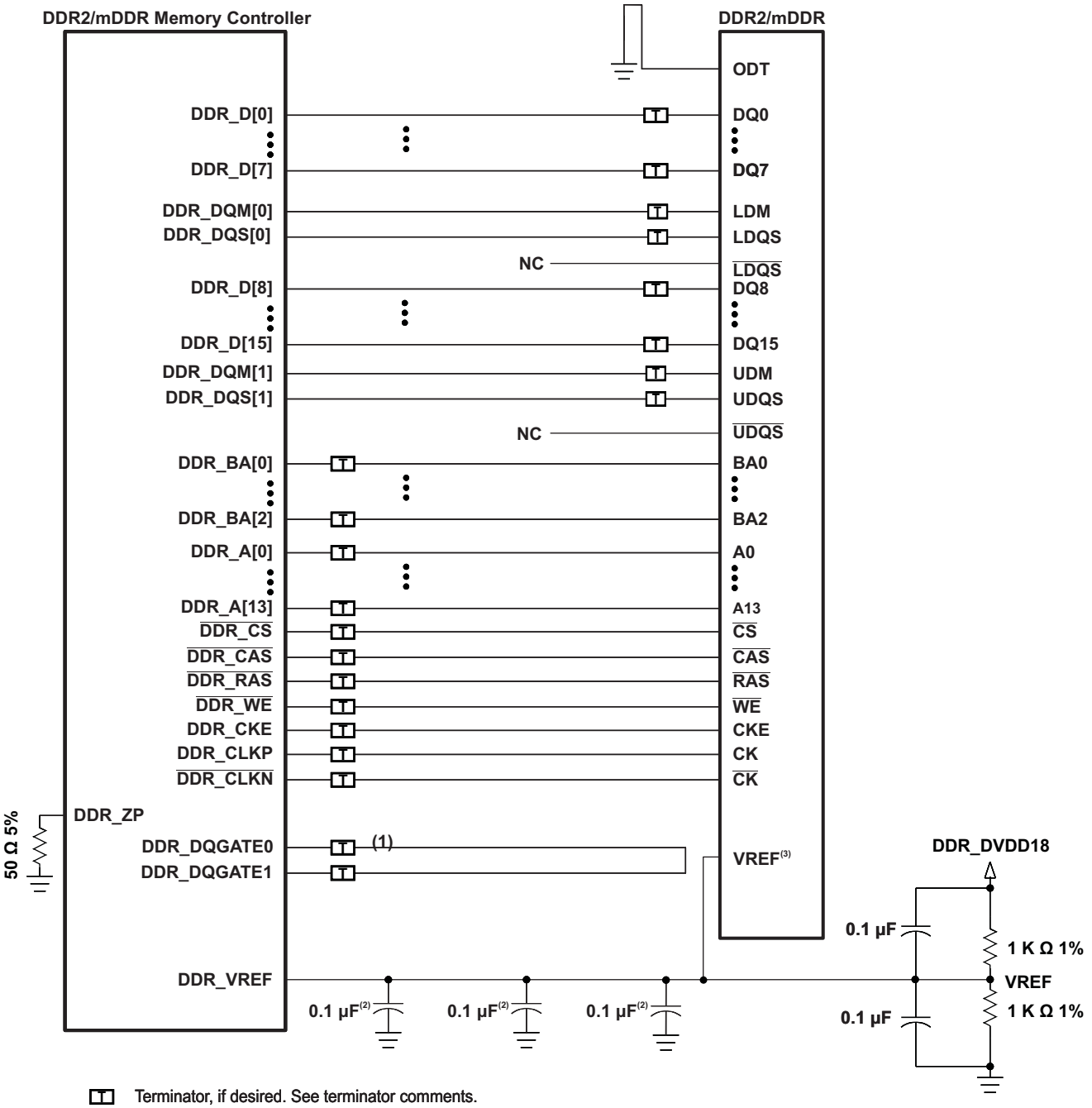
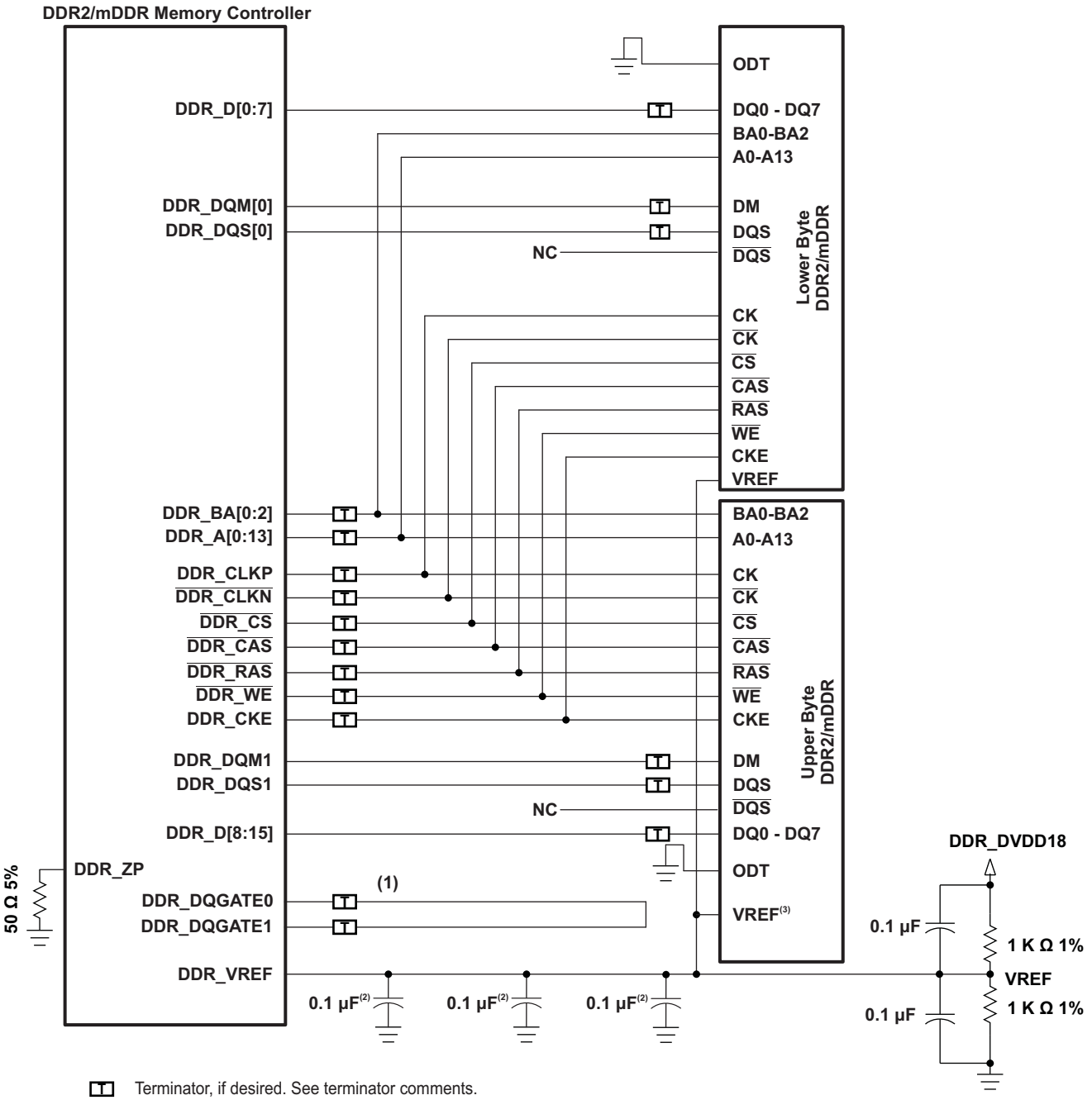



(1) See Figure 5-25 for DQGATE routing specifications.

(2) For DDR2, one of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin. For mDDR, these capacitors can be eliminated completely.

(3) VREF applies in the case of DDR2 memories. For mDDR, the DDR_VREF pin still needs to be connected to the divider circuit.

**Figure 5-18. DDR2/mDDR Single-Memory High Level Schematic**




(1) See Figure 5-25 for DQGATE routing specifications.

(2) For DDR2, one of these capacitors can be eliminated if the divider and its capacitors are placed near a device VREF pin. For mDDR, these capacitors can be eliminated completely.

(3) VREF applies in the case of DDR2 memories. For mDDR, the DDR_VREF pin still needs to be connected to the divider circuit.

**Figure 5-19. DDR2/mDDR Dual-Memory High Level Schematic**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#### 5.11.3.2 Compatible JEDEC DDR2/mDDR Devices

Table 5-27 shows the parameters of the JEDEC DDR2/mDDR devices that are compatible with this interface. Generally, the DDR2/mDDR interface is compatible with x16 DDR2/mDDR-400 speed grade DDR2/mDDR devices.

The device also supports JEDEC DDR2/mDDR x8 devices in the dual chip configuration. In this case, one chip supplies the upper byte and the second chip supplies the lower byte. Addresses and most control signals are shared just like regular dual chip memory configurations.

**Table 5-27. Compatible JEDEC DDR2/mDDR Devices**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | JEDEC DDR2/mDDR Device Speed Grade(1) | DDR2/mDDR-400 | | |
| 2 | JEDEC DDR2/mDDR Device Bit Width | x8 | x16 | Bits |
| 3 | JEDEC DDR2/mDDR Device Count(2) | 1 | 2 | Devices |

(1) Higher DDR2/mDDR speed grades are supported due to inherent JEDEC DDR2/mDDR backwards compatibility.
(2) Supported configurations are one 16-bit DDR2/mDDR memory or two 8-bit DDR2/mDDR memories

#### 5.11.3.3 PCB Stackup

The minimum stackup required for routing the device is a six layer stack as shown in Table 5-28. Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the PCB footprint.Complete stack up specifications are provided in Table 5-29.

**Table 5-28. Device Minimum PCB Stack Up**

| LAYER | TYPE | DESCRIPTION |
|---|---|---|
| 1 | Signal | Top Routing Mostly Horizontal |
| 2 | Plane | Ground |
| 3 | Plane | Power |
| 4 | Signal | Internal Routing |
| 5 | Plane | Ground |
| 6 | Signal | Bottom Routing Mostly Vertical |

**Table 5-29. PCB Stack Up Specifications**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | PCB Routing/Plane Layers | 6 | | | |
| 2 | Signal Routing Layers | 3 | | | |
| 3 | Full ground layers under DDR2/mDDR routing region | 2 | | | |
| 4 | Number of ground plane cuts allowed within DDR routing region | | | 0 | |
| 5 | Number of ground reference planes required for each DDR2/mDDR routing layer | 1 | | | |
| 6 | Number of layers between DDR2/mDDR routing layer and reference ground plane | | | 0 | |
| 7 | PCB Routing Feature Size | | 4 | | Mils |
| 8 | PCB Trace Width w | | 4 | | Mils |
| 8 | PCB BGA escape via pad size | | 18 | | Mils |
| 9 | PCB BGA escape via hole size | | 8 | | Mils |
| 10 | Device BGA pad size(1) | | | | |
| 11 | DDR2/mDDR Device BGA pad size(2) | | | | |
| 12 | Single Ended Impedance, Zo | 50 | | 75 | Ω |
| 13 | Impedance Control(3) | Z-5 | Z | Z+5 | Ω |

(1) Please refer to the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811) for device BGA pad size.
(2) Please refer to the DDR2/mDDR device manufacturer documentation for the DDR2/mDDR device BGA pad size.
(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

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### 5.11.3.4 Placement

Figure 5-19 shows the required placement for the device as well as the DDR2/mDDR devices. The dimensions for Figure 5-20 are defined in Table 5-30. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For single-memory DDR2/mDDR systems, the second DDR2/mDDR device is omitted from the placement.

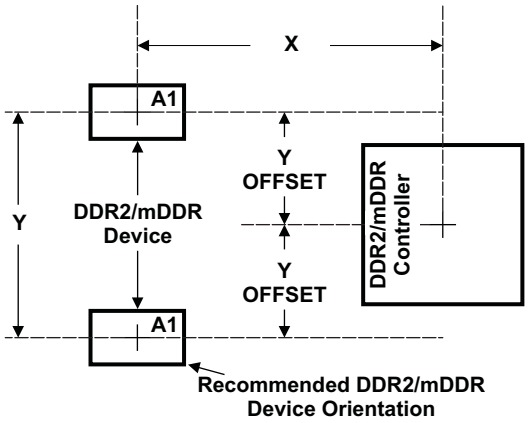


**Figure 5-20. OMAP-L138 and DDR2/mDDR Device Placement**

**Table 5-30. Placement Specifications(1)(2)**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | X | | 1750 | Mils |
| 2 | Y | | 1280 | Mils |
| 3 | Y Offset | | (3)650 | Mils |
| 4 | Clearance from non-DDR2/mDDR signal to DDR2/mDDR Keepout Region(4) | 4 | | w(5) |

(1) See Figure 5-20 for dimension definitions.
(2) Measurements from center of device to center of DDR2/mDDR device.
(3) For single memory systems it is recommended that Y Offset be as small as possible.
(4) Non-DDR2/mDDR signals allowed within DDR2/mDDR keepout region provided they are separated from DDR2/mDDR routing layers by a ground plane.
(5) w = PCB trace width as defined in Table 5-29.


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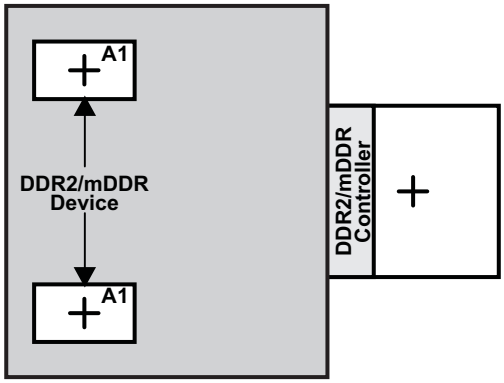
### 5.11.3.5 DDR2/mDDR Keep Out Region

The region of the PCB used for the DDR2/mDDR circuitry must be isolated from other signals. The DDR2/mDDR keep out region is defined for this purpose and is shown in Figure 5-21. The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are shown in Table 5-30.




**Region should encompass all DDR2/mDDR circuitry and varies depending on placement. Non-DDR2/mDDR signals should not be routed on the DDR signal layers within the DDR2/mDDR keep out region. Non-DDR2/mDDR signals may be routed in the region provided they are routed on layers separated from DDR2/mDDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.**

**Figure 5-21. DDR2/mDDR Keepout Region**

### 5.11.3.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2/mDDR and other circuitry. Table 5-31 contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the Soc and DDR2/mDDR interfaces. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 5-31. Bulk Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | DDR_DVDD18 Supply Bulk Bypass Capacitor Count(1) | 3 | | Devices |
| 2 | DDR_DVDD18 Supply Bulk Bypass Total Capacitance | 30 | | µF |
| 3 | DDR#1 Bulk Bypass Capacitor Count(1) | 1 | | Devices |
| 4 | DDR#1 Bulk Bypass Total Capacitance | 22 | | µF |
| 5 | DDR#2 Bulk Bypass Capacitor Count(1)(2) | 1 | | Devices |
| 6 | DDR#2 Bulk Bypass Total Capacitance(2) | 22 | | µF |

(1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.
(2) Only used on dual-memory systems.

### 5.11.3.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2/mDDR interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, Soc/DDR2/mDDR power, and Soc/DDR2/mDDR ground connections. Table 5-32 contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

**Table 5-32. High-Speed Bypass Capacitors**

| NO. | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| 1 | HS Bypass Capacitor Package Size(1) | | 0402 | 10 Mils |
| 2 | Distance from HS bypass capacitor to device being bypassed | | 250 | Mils |
| 3 | Number of connection vias for each HS bypass capacitor | 2(2) | | Vias |
| 4 | Trace length from bypass capacitor contact to connection via | 1 | 30 | Mils |
| 5 | Number of connection vias for each DDR2/mDDR device power or ground balls | 1 | | Vias |
| 6 | Trace length from DDR2/mDDR device power ball to connection via | | 35 | Mils |
| 7 | DDR_DVDD18 Supply HS Bypass Capacitor Count(3) | 10 | | Devices |
| 8 | DDR_DVDD18 Supply HS Bypass Capacitor Total Capacitance | 0.6 | | µF |
| 9 | DDR#1 HS Bypass Capacitor Count(3) | 8 | | Devices |
| 10 | DDR#1 HS Bypass Capacitor Total Capacitance | 0.4 | | µF |
| 11 | DDR#2 HS Bypass Capacitor Count(3)(4) | 8 | | Devices |
| 12 | DDR#2 HS Bypass Capacitor Total Capacitance(4) | 0.4 | | µF |

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor
(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.
(3) These devices should be placed as close as possible to the device being bypassed.
(4) Only used on dual-memory systems.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#### 5.11.3.8 Net Classes

Table 5-33 lists the clock net classes for the DDR2/mDDR interface. Table 5-34 lists the signal net classes, and associated clock net classes, for the signals in the DDR2/mDDR interface. These net classes are used for the termination and routing rules that follow.

**Table 5-33. Clock Net Class Definitions**

| CLOCK NET CLASS | Soc PIN NAMES |
|---|---|
| CK | DDR_CLKP / $\overline{\text{DDR_CLKN}}$ |
| DQS0 | DDR_DQS[0] |
| DQS1 | DDR_DQS[1] |

**Table 5-34. Signal Net Class Definitions**

| SIGNAL NET CLASS | ASSOCIATED CLOCK NET CLASS | Soc PIN NAMES |
|---|---|---|
| ADDR_CTRL | CK | DDR_BA[2:0], DDR_A[13:0], $\overline{\text{DDR_CS}}$, $\overline{\text{DDR_CAS}}$, $\overline{\text{DDR_RAS}}$, $\overline{\text{DDR_WE}}$, DDR_CKE |
| D0 | DQS0 | DDR_D[7:0], DDR_DQM0 |
| D1 | DQS1 | DDR_D[15:8], DDR_DQM1 |
| DQGATE | CK, DQS0, DQS1 | DDR_DQGATE0, DDR_DQGATE1 |

#### 5.11.3.9 DDR2/mDDR Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 5-35 shows the specifications for the series terminators.

**Table 5-35. DDR2/mDDR Signal Terminations(1)(2)(3)**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | CK Net Class | 0 | | 10 | Ω |
| 2 | ADDR_CTRL Net Class | 0 | 22 | Zo | Ω |
| 3 | Data Byte Net Classes (DQS[0], DQS[1], D0, D1)(4) | 0 | 22 | Zo | Ω |
| 4 | DQGATE Net Class (DQGATE) | 0 | 10 | Zo | Ω |

(1) Only series termination is permitted, parallel or SST specifically disallowed.
(2) Terminator values larger than typical only recommended to address EMI issues.
(3) Termination value should be uniform across net class.
(4) When no termination is used on data lines (0 Ω), the DDR2/mDDR devices must be programmed to operate in 60% strength mode.

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### 5.11.3.10 VREF Routing

VREF is used as a reference by the input buffers of the DDR2/mDDR memories as well as the OMAP-L138. VREF is intended to be half the DDR2/mDDR power supply voltage and should be created using a resistive divider as shown in Figure 5-18. Other methods of creating VREF are not recommended. Figure 5-22 shows the layout guidelines for VREF.

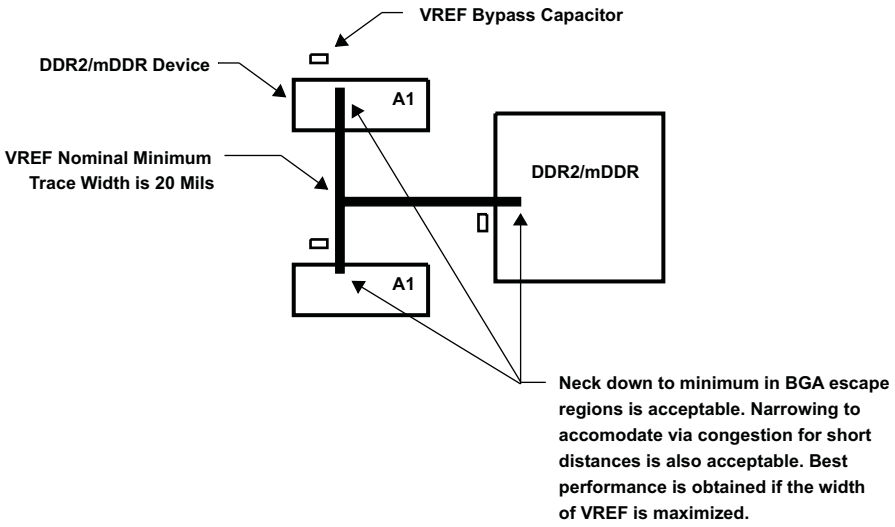


**Figure 5-22. VREF Routing and Topology**


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### 5.11.3.11 DDR2/mDDR CK and ADDR_CTRL Routing

Figure 5-23 shows the topology of the routing for the CK and ADDR_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

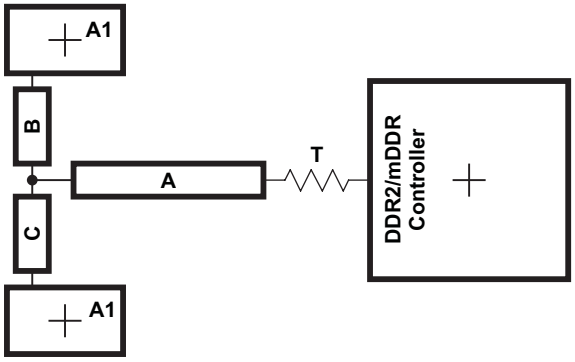


**Figure 5-23. CK and ADDR_CTRL Routing and Topology**

**Table 5-36. CK and ADDR_CTRL Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center to Center CK-CKN Spacing(1) | | | 2w(2) | |
| 2 | CK A to B/A to C Skew Length Mismatch(3) | | | 25 | Mils |
| 3 | CK B to C Skew Length Mismatch | | | 25 | Mils |
| 4 | Center to center CK to other DDR2/mDDR trace spacing(1) | 4w(2) | | | |
| 5 | CK/ADDR_CTRL nominal trace length(4) | CACLM-50 | CACLM | CACLM+50 | Mils |
| 6 | ADDR_CTRL to CK Skew Length Mismatch | | | 100 | Mils |
| 7 | ADDR_CTRL to ADDR_CTRL Skew Length Mismatch | | | 100 | Mils |
| 8 | Center to center ADDR_CTRL to other DDR2/mDDR trace spacing(1) | 4w(2) | | | |
| 9 | Center to center ADDR_CTRL to other ADDR_CTRL trace spacing(1) | 3w (2) | | | |
| 10 | ADDR_CTRL A to B/A to C Skew Length Mismatch(3) | | | 100 | Mils |
| 11 | ADDR_CTRL B to C Skew Length Mismatch | | | 100 | Mils |

(1) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) w = PCB trace width as defined in Table 5-29.
(3) Series terminator, if used, should be located closest to device.
(4) CACLM is the longest Manhattan distance of the CK and ADDR_CTRL net classes.

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Figure 5-24 shows the topology and routing for the DQS and D net class; the routes are point to point. Skew matching across bytes is not needed nor recommended.

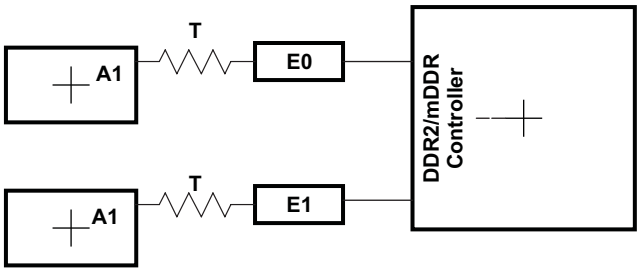


**Figure 5-24. DQS and D Routing and Topology**

**Table 5-37. DQS and D Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | Center to center DQS to other DDR2/mDDR trace spacing(1) | 4w(2) | | | |
| 2 | DQS/D nominal trace length(3)(4) | DQLM-50 | DQLM | DQLM+50 | Mils |
| 3 | D to DQS Skew Length Mismatch(4) | | | 100 | Mils |
| 4 | D to D Skew Length Mismatch(4) | | | 100 | Mils |
| 5 | Center to center D to other DDR2/mDDR trace spacing(1)(5) | 4w(2) | | | |
| 6 | Center to Center D to other D trace spacing(1)(6) | 3w(2) | | | |

(1) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
(2) w = PCB trace width as defined in Table 5-29.
(3) Series terminator, if used, should be located closest to DDR.
(4) There is no need and it is not recommended to skew match across data bytes, i.e., from DQS0 and data byte 0 to DQS1 and data byte 1.
(5) D's from other DQS domains are considered *other DDR2/mDDR trace*.
(6) DQLM is the longest Manhattan distance of each of the DQS and D net class.


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Figure 5-25 shows the routing for the DQGATE net class. Table 5-38 contains the routing specification.

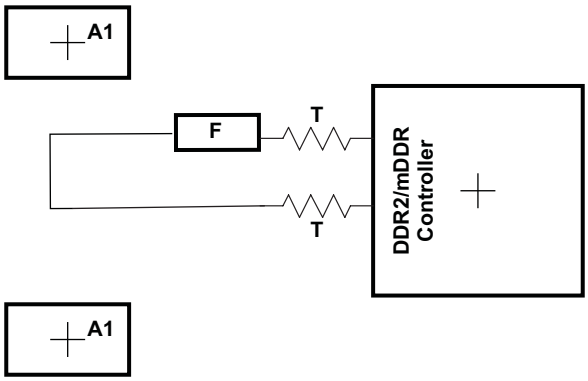


**Figure 5-25. DQGATE Routing**

**Table 5-38. DQGATE Routing Specification**

| NO. | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | DQGATE Length F | | CKB0B(1) | | |
| 2 | Center to center DQGATE to any other trace spacing | 4w(2) | | | |
| 3 | DQS/D nominal trace length | DQLM-50 | DQLM | DQLM+50 | Mils |
| 4 | DQGATE Skew(3) | | | 100 | Mils |

(1) CKB0B1 is the sum of the length of the CK net plus the average length of the DQS0 and DQS1 nets.
(2) w = PCB trace width as defined in Table 5-29.
(3) Skew from CKB0B1

### 5.11.3.12 MDDR/DDR2 Boundary Scan Limitations

Due to DDR implementation and timing restrictions, it was not possible to place boundary scan cells between core logic and the IO like boundary scan cells for other IO. Instead, the boundary scan cells are tapped-off to the DDR PHY and there is the equivalent of a multiplexer inside the DDR PHY which selects between functional and boundary scan paths.

The implication for boundary scan is that the DDR pins will not support the SAMPLE function of the output enable cells on the DDR pins and this is a violation of IEEE 1149.1. Full EXTEST and PRELOAD capability is still available.

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## 5.12 Memory Protection Units

The MPU performs memory protection checking. It receives requests from a bus master in the system and checks the address against the fixed and programmable regions to see if the access is allowed. If allowed, the transfer is passed unmodified to its output bus (to the targeted address). If the transfer is illegal (fails the protection check) then the MPU does not pass the transfer to the output bus but rather services the transfer internally back to the input bus (to prevent a hang) returning the fault status to the requestor as well as generating an interrupt about the fault. The following features are supported by the MPU:

- Provides memory protection for fixed and programmable address ranges.
- Supports multiple programmable address region.
- Supports secure and debug access privileges.
- Supports read, write, and execute access privileges.
- Supports privid(8) associations with ranges.
- Generates an interrupt when there is a protection violation, and saves violating transfer parameters.
- MMR access is also protected.

**Table 5-39. MPU1 Configuration Registers**

| MPU1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 4000 | REVID | Revision ID |
| 0x01E1 4004 | CONFIG | Configuration |
| 0x01E1 4010 | IRAWSTAT | Interrupt raw status/set |
| 0x01E1 4014 | IENSTAT | Interrupt enable status/clear |
| 0x01E1 4018 | IENSET | Interrupt enable |
| 0x01E1 401C | IENCLR | Interrupt enable clear |
| 0x01E1 4020 - 0x01E1 41FF | - | Reserved |
| 0x01E1 4200 | PROG1_MPSAR | Programmable range 1, start address |
| 0x01E1 4204 | PROG1_MPEAR | Programmable range 1, end address |
| 0x01E1 4208 | PROG1_MPPA | Programmable range 1, memory page protection attributes |
| 0x01E1 420C - 0x01E1 420F | - | Reserved |
| 0x01E1 4210 | PROG2_MPSAR | Programmable range 2, start address |
| 0x01E1 4214 | PROG2_MPEAR | Programmable range 2, end address |
| 0x01E1 4218 | PROG2_MPPA | Programmable range 2, memory page protection attributes |
| 0x01E1 421C - 0x01E1 421F | - | Reserved |
| 0x01E1 4220 | PROG3_MPSAR | Programmable range 3, start address |
| 0x01E1 4224 | PROG3_MPEAR | Programmable range 3, end address |
| 0x01E1 4228 | PROG3_MPPA | Programmable range 3, memory page protection attributes |
| 0x01E1 422C - 0x01E1 422F | - | Reserved |
| 0x01E1 4230 | PROG4_MPSAR | Programmable range 4, start address |
| 0x01E1 4234 | PROG4_MPEAR | Programmable range 4, end address |
| 0x01E1 4238 | PROG4_MPPA | Programmable range 4, memory page protection attributes |
| 0x01E1 423C - 0x01E1 423F | - | Reserved |
| 0x01E1 4240 | PROG5_MPSAR | Programmable range 5, start address |
| 0x01E1 4244 | PROG5_MPEAR | Programmable range 5, end address |
| 0x01E1 4248 | PROG5_MPPA | Programmable range 5, memory page protection attributes |
| 0x01E1 424C - 0x01E1 424F | - | Reserved |
| 0x01E1 4250 | PROG6_MPSAR | Programmable range 6, start address |
| 0x01E1 4254 | PROG6_MPEAR | Programmable range 6, end address |
| 0x01E1 4258 | PROG6_MPPA | Programmable range 6, memory page protection attributes |
| 0x01E1 425C - 0x01E1 42FF | - | Reserved |


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**Table 5-39. MPU1 Configuration Registers (continued)**

| MPU1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 4300 | FLTADDRR | Fault address |
| 0x01E1 4304 | FLTSTAT | Fault status |
| 0x01E1 4308 | FLTCLR | Fault clear |
| 0x01E1 430C - 0x01E1 4FFF | - | Reserved |

**Table 5-40. MPU2 Configuration Registers**

| MPU2 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 5000 | REVID | Revision ID |
| 0x01E1 5004 | CONFIG | Configuration |
| 0x01E1 5010 | IRAWSTAT | Interrupt raw status/set |
| 0x01E1 5014 | IENSTAT | Interrupt enable status/clear |
| 0x01E1 5018 | IENSET | Interrupt enable |
| 0x01E1 501C | IENCLR | Interrupt enable clear |
| 0x01E1 5020 - 0x01E1 51FF | - | Reserved |
| 0x01E1 5200 | PROG1_MPSAR | Programmable range 1, start address |
| 0x01E1 5204 | PROG1_MPEAR | Programmable range 1, end address |
| 0x01E1 5208 | PROG1_MPPA | Programmable range 1, memory page protection attributes |
| 0x01E1 520C - 0x01E1 520F | - | Reserved |
| 0x01E1 5210 | PROG2_MPSAR | Programmable range 2, start address |
| 0x01E1 5214 | PROG2_MPEAR | Programmable range 2, end address |
| 0x01E1 5218 | PROG2_MPPA | Programmable range 2, memory page protection attributes |
| 0x01E1 521C - 0x01E1 521F | - | Reserved |
| 0x01E1 5220 | PROG3_MPSAR | Programmable range 3, start address |
| 0x01E1 5224 | PROG3_MPEAR | Programmable range 3, end address |
| 0x01E1 5228 | PROG3_MPPA | Programmable range 3, memory page protection attributes |
| 0x01E1 522C - 0x01E1 522F | - | Reserved |
| 0x01E1 5230 | PROG4_MPSAR | Programmable range 4, start address |
| 0x01E1 5234 | PROG4_MPEAR | Programmable range 4, end address |
| 0x01E1 5238 | PROG4_MPPA | Programmable range 4, memory page protection attributes |
| 0x01E1 523C - 0x01E1 523F | - | Reserved |
| 0x01E1 5240 | PROG5_MPSAR | Programmable range 5, start address |
| 0x01E1 5244 | PROG5_MPEAR | Programmable range 5, end address |
| 0x01E1 5248 | PROG5_MPPA | Programmable range 5, memory page protection attributes |
| 0x01E1 524C - 0x01E1 524F | - | Reserved |
| 0x01E1 5250 | PROG6_MPSAR | Programmable range 6, start address |
| 0x01E1 5254 | PROG6_MPEAR | Programmable range 6, end address |
| 0x01E1 5258 | PROG6_MPPA | Programmable range 6, memory page protection attributes |
| 0x01E1 525C - 0x01E1 525F | - | Reserved |
| 0x01E1 5260 | PROG7_MPSAR | Programmable range 7, start address |
| 0x01E1 5264 | PROG7_MPEAR | Programmable range 7, end address |
| 0x01E1 5268 | PROG7_MPPA | Programmable range 7, memory page protection attributes |
| 0x01E1 526C - 0x01E1 526F | - | Reserved |
| 0x01E1 5270 | PROG8_MPSAR | Programmable range 8, start address |
| 0x01E1 5274 | PROG8_MPEAR | Programmable range 8, end address |
| 0x01E1 5278 | PROG8_MPPA | Programmable range 8, memory page protection attributes |
| 0x01E1 527C - 0x01E1 527F | - | Reserved |

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**Table 5-40. MPU2 Configuration Registers (continued)**

| MPU2 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 5280 | PROG9_MPSAR | Programmable range 9, start address |
| 0x01E1 5284 | PROG9_MPEAR | Programmable range 9, end address |
| 0x01E1 5288 | PROG9_MPPA | Programmable range 9, memory page protection attributes |
| 0x01E1 528C - 0x01E1 528F | - | Reserved |
| 0x01E1 5290 | PROG10_MPSAR | Programmable range 10, start address |
| 0x01E1 5294 | PROG10_MPEAR | Programmable range 10, end address |
| 0x01E1 5298 | PROG10_MPPA | Programmable range 10, memory page protection attributes |
| 0x01E1 529C - 0x01E1 529F | - | Reserved |
| 0x01E1 52A0 | PROG11_MPSAR | Programmable range 11, start address |
| 0x01E1 52A4 | PROG11_MPEAR | Programmable range 11, end address |
| 0x01E1 52A8 | PROG11_MPPA | Programmable range 11, memory page protection attributes |
| 0x01E1 52AC - 0x01E1 52AF | - | Reserved |
| 0x01E1 52B0 | PROG12_MPSAR | Programmable range 12, start address |
| 0x01E1 52B4 | PROG12_MPEAR | Programmable range 12, end address |
| 0x01E1 52B8 | PROG12_MPPA | Programmable range 12, memory page protection attributes |
| 0x01E1 52BC - 0x01E1 52FF | - | Reserved |
| 0x01E1 5300 | FLTADDRR | Fault address |
| 0x01E1 5304 | FLTSTAT | Fault status |
| 0x01E1 5308 | FLTCLR | Fault clear |
| 0x01E1 530C - 0x01E1 5FFF | - | Reserved |


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## 5.13 MMC / SD / SDIO (MMCSD0, MMCSD1)

### 5.13.1 MMCSD Peripheral Description

The device includes an two MMCSD controllers which are compliant with MMC V4.0, Secure Digital Part 1 Physical Layer Specification V1.1 and Secure Digital Input Output (SDIO) V2.0 specifications.

The MMC/SD Controller have following features:

- MultiMediaCard (MMC).
- Secure Digital (SD) Memory Card.
- MMC/SD protocol support.
- SDIO protocol support.
- Programmable clock frequency.
- 512 bit Read/Write FIFO to lower system overhead.
- Slave EDMA transfer capability.

The device MMC/SD Controller does not support SPI mode.

### 5.13.2 MMCSD Peripheral Register Description(s)

**Table 5-41. Multimedia Card/Secure Digital (MMC/SD) Card Controller Registers**

| MMCSD0 BYTE ADDRESS | MMCSD1 BYTE ADDRESS | ACRONYM | REGISTER DESCSRIPTION |
|---|---|---|---|
| 0x01C4 0000 | 0x01E1 B000 | MMCCTL | MMC Control Register |
| 0x01C4 0004 | 0x01E1 B004 | MMCCLK | MMC Memory Clock Control Register |
| 0x01C4 0008 | 0x01E1 B008 | MMCST0 | MMC Status Register 0 |
| 0x01C4 000C | 0x01E1 B00C | MMCST1 | MMC Status Register 1 |
| 0x01C4 0010 | 0x01E1 B010 | MMCIM | MMC Interrupt Mask Register |
| 0x01C4 0014 | 0x01E1 B014 | MMCTOR | MMC Response Time-Out Register |
| 0x01C4 0018 | 0x01E1 B018 | MMCTOD | MMC Data Read Time-Out Register |
| 0x01C4 001C | 0x01E1 B01C | MMCBLEN | MMC Block Length Register |
| 0x01C4 0020 | 0x01E1 B020 | MMCNBLK | MMC Number of Blocks Register |
| 0x01C4 0024 | 0x01E1 B024 | MMCNBLC | MMC Number of Blocks Counter Register |
| 0x01C4 0028 | 0x01E1 B028 | MMCDRR | MMC Data Receive Register |
| 0x01C4 002C | 0x01E1 B02C | MMCDXR | MMC Data Transmit Register |
| 0x01C4 0030 | 0x01E1 B030 | MMCCMD | MMC Command Register |
| 0x01C4 0034 | 0x01E1 B034 | MMCARGHL | MMC Argument Register |
| 0x01C4 0038 | 0x01E1 B038 | MMCRSP01 | MMC Response Register 0 and 1 |
| 0x01C4 003C | 0x01E1 B03C | MMCRSP23 | MMC Response Register 2 and 3 |
| 0x01C4 0040 | 0x01E1 B040 | MMCRSP45 | MMC Response Register 4 and 5 |
| 0x01C4 0044 | 0x01E1 B044 | MMCRSP67 | MMC Response Register 6 and 7 |
| 0x01C4 0048 | 0x01E1 B048 | MMCDRSP | MMC Data Response Register |
| 0x01C4 0050 | 0x01E1 B050 | MMCCIDX | MMC Command Index Register |
| 0x01C4 0064 | 0x01E1 B064 | SDIOCTL | SDIO Control Register |
| 0x01C4 0068 | 0x01E1 B068 | SDIOST0 | SDIO Status Register 0 |
| 0x01C4 006C | 0x01E1 B06C | SDIOIEN | SDIO Interrupt Enable Register |
| 0x01C4 0070 | 0x01E1 B070 | SDIOIST | SDIO Interrupt Status Register |
| 0x01C4 0074 | 0x01E1 B074 | MMCFIFOCTL | MMC FIFO Control Register |

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### 5.13.3 MMC/SD Electrical Data/Timing

Table 5-42 through Table 5-43 assume testing over recommended operating conditions.

**Table 5-42. Timing Requirements for MMC/SD (see Figure 5-27 and Figure 5-29)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(CMDV-CLKH)}$ | Setup time, MMCSD_CMD valid before MMCSD_CLK high | 4 | | 4 | | 6 | | ns |
| 2 | $t_{h(CLKH-CMDV)}$ | Hold time, MMCSD_CMD valid after MMCSD_CLK high | 2.5 | | 2.5 | | 2.5 | | ns |
| 3 | $t_{su(DATV-CLKH)}$ | Setup time, MMCSD_DATx valid before MMCSD_CLK high | 4.5 | | 5 | | 6 | | ns |
| 4 | $t_{h(CLKH-DATV)}$ | Hold time, MMCSD_DATx valid after MMCSD_CLK high | 2.5 | | 2.5 | | 2.5 | | ns |

**Table 5-43. Switching Characteristics for MMC/SD (see Figure 5-26 through Figure 5-29)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 7 | $f_{(CLK)}$ | Operating frequency, MMCSD_CLK | 0 | 52 | 0 | 50 | 0 | 25 | MHz |
| 8 | $f_{(CLK_ID)}$ | Identification mode frequency, MMCSD_CLK | 0 | 400 | 0 | 400 | 0 | 400 | KHz |
| 9 | $t_{W(CLKL)}$ | Pulse width, MMCSD_CLK low | 6.5 | | 6.5 | | 10 | | ns |
| 10 | $t_{W(CLKH)}$ | Pulse width, MMCSD_CLK high | 6.5 | | 6.5 | | 10 | | ns |
| 11 | $t_{r(CLK)}$ | Rise time, MMCSD_CLK | | 3 | | 3 | | 10 | ns |
| 12 | $t_{f(CLK)}$ | Fall time, MMCSD_CLK | | 3 | | 3 | | 10 | ns |
| 13 | $t_{d(CLKL-CMD)}$ | Delay time, MMCSD_CLK low to MMCSD_CMD transition | -4 | 2.5 | -4 | 3 | -4 | 4 | ns |
| 14 | $t_{d(CLKL-DAT)}$ | Delay time, MMCSD_CLK low to MMCSD_DATx transition | -4 | 3.3 | -4 | 3.5 | -4 | 4 | ns |


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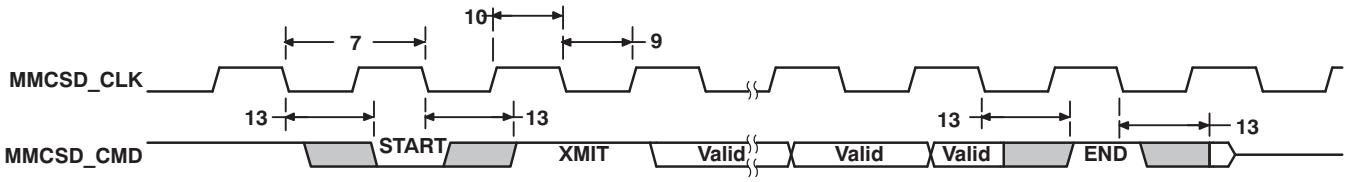


**Figure 5-26. MMC/SD Host Command Timing**

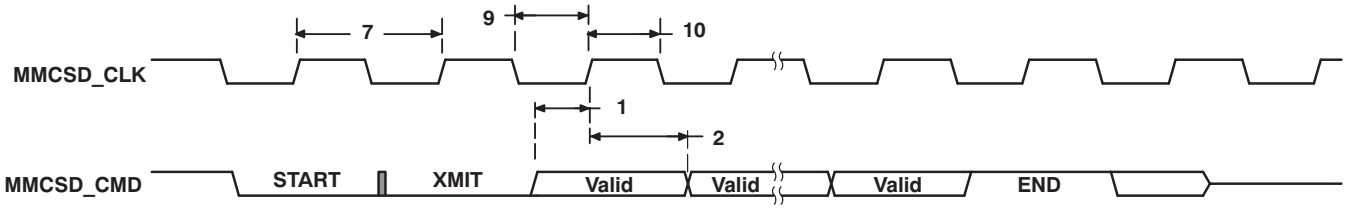


**Figure 5-27. MMC/SD Card Response Timing**

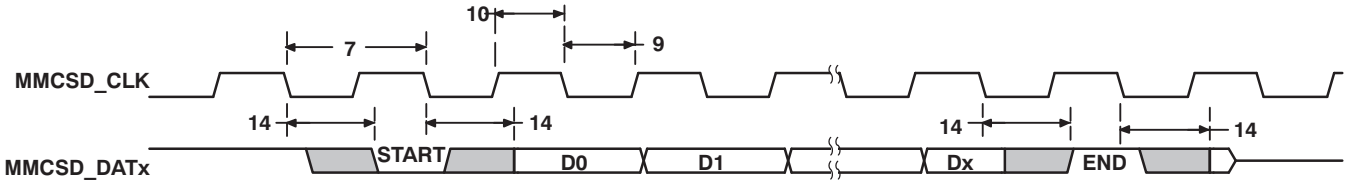


**Figure 5-28. MMC/SD Host Write Timing**

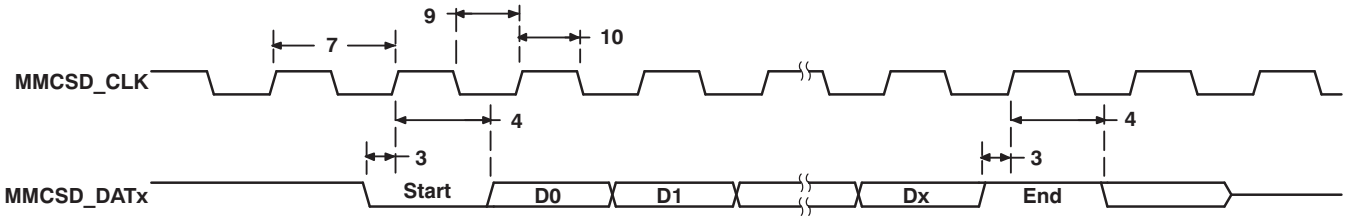


**Figure 5-29. MMC/SD Host Read and Card CRC Status Timing**

## 5.14 Serial ATA Controller (SATA)

The Serial ATA Controller (SATA) provides a single HBA port operating in AHCI mode and is used to interface to data storage devices at both 1.5 Gbits/second and 3.0 Gbits/second line speeds. AHCI describes a system memory structure that contains a generic area for control and status, and a table of entries describing a command list where each command list entry contains information necessary to program an SATA device, and a pointer to a descriptor table for transferring data between system memory and the device.

The SATA Controller supports the following features:

- Serial ATA 1.5 Gbps (Gen 1i) and 3 Gbps (Gen 2i) line speeds
- Support for the AHCI controller spec 1.1
- Integrated SERDES PHY
- Integrated Rx and Tx data buffers
- Supports all SATA power management features
- Internal DMA engine per port
- Hardware-assisted native command queuing (NCQ) for up to 32 entries
- 32-bit addressing
- Supports port multiplier with command-based switching
- Activity LED support
- Mechanical presence switch
- Cold presence detect

The SATA Controller support is dependent on the CPU voltage operating point:

- At CVDD = 1.3V, SATA Gen 2i (3.0 Gbps) and SATA Gen 1i (1.5 Gbps) are supported.
- At CVDD = 1.2V, SATA Gen 2i (3.0 Gbps) and SATA Gen 1i (1.5 Gbps) are supported.
- At CVDD = 1.1V, SATA Gen 1i (1.5 Gbps) only is supported.
- At CVDD = 1.0V, SATA is not supported.


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### 5.14.1 SATA Register Descriptions

Table 5-44 is a list of the SATA Controller registers.

**Table 5-44. SATA Controller Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 8000 | CAP | HBA Capabilities Register |
| 0x01E1 8004 | GHC | Global HBA Control Register |
| 0x01E1 8008 | IS | Interrupt Status Register |
| 0x01E1 800C | PI | Ports Implemented Register |
| 0x01E1 8010 | VS | AHCI Version Register |
| 0x01E1 8014 | CCC_CTL | Command Completion Coalescing Control Register |
| 0x01E1 8018 | CCC_PORTS | Command Completion Coalescing Ports Register |
| 0x01E1 80A0 | BISTAFR | BIST Active FIS Register |
| 0x01E1 80A4 | BISTCR | BIST Control Register |
| 0x01E1 80A8 | BISTFCTR | BIST FIS Count Register |
| 0x01E1 80AC | BISTSR | BIST Status Register |
| 0x01E1 80B0 | BISTDECR | BIST DWORD Error Count Register |
| 0x01E1 80E0 | TIMER1MS | BIST DWORD Error Count Register |
| 0x01E1 80E8 | GPARAM1R | Global Parameter 1 Register |
| 0x01E1 80EC | GPARAM2R | Global Parameter 2 Register |
| 0x01E1 80F0 | PPARAMR | Port Parameter Register |
| 0x01E1 80F4 | TESTR | Test Register |
| 0x01E1 80F8 | VERSIONR | Version Register |
| 0x01E1 80FC | IDR | ID Register |
| 0x01E1 8100 | P0CLB | Port Command List Base Address Register |
| 0x01E1 8108 | P0FB | Port FIS Base Address Register |
| 0x01E1 8110 | P0IS | Port Interrupt Status Register |
| 0x01E1 8114 | P0IE | Port Interrupt Enable Register |
| 0x01E1 8118 | P0CMD | Port Command Register |
| 0x01E1 8120 | P0TFD | Port Task File Data Register |
| 0x01E1 8124 | P0SIG | Port Signature Register |
| 0x01E1 8128 | P0SSTS | Port Serial ATA Status Register |
| 0x01E1 812C | P0SCTL | Port Serial ATA Control Register |
| 0x01E1 8130 | P0SERR | Port Serial ATA Error Register |
| 0x01E1 8134 | P0SACT | Port Serial ATA Active Register |
| 0x01E1 8138 | P0CI | Port Command Issue Register |
| 0x01E1 813C | P0SNTF | Port Serial ATA Notification Register |
| 0x01E1 8170 | P0DMACR | Port DMA Control Register |
| 0x01E1 8178 | P0PHYCR | Port PHY Control Register |
| 0x01E1 817C | P0PHYSR | Port PHY Status Register |

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### 5.14.2 1. SATA Interface

This section provides the timing specification for the SATA interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. TI has performed the simulation and system design work to ensure the SATA interface requirements are met.

#### 5.14.2.1 SATA Interface Schematic

Figure 5-30 shows the SATA interface schematic.

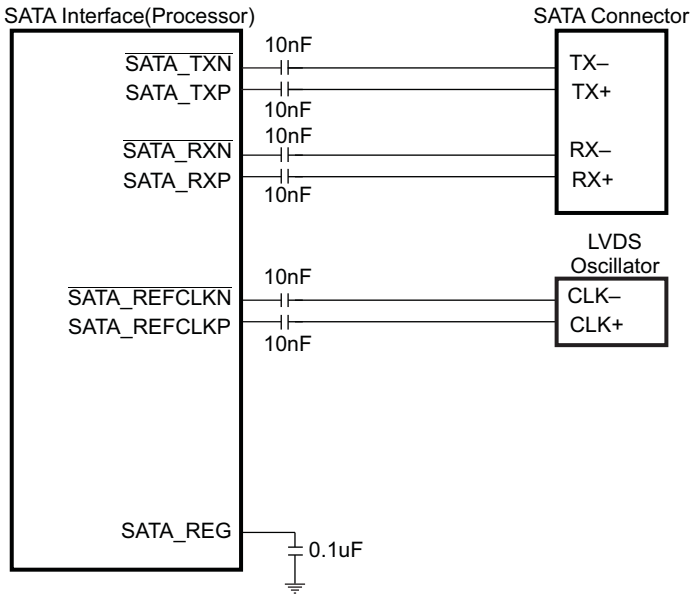


**Figure 5-30. SATA Interface High Level Schematic**

#### 5.14.2.2 Compatible SATA Components and Modes

Table 5-45 shows the compatible SATA components and supported modes. Note that the only supported configuration is an internal cable from the processor host to the SATA device.

**Table 5-45. SATA Supported Modes**

| PARAMETER | MIN | MAX | UNIT | SUPPORTED |
|---|---|---|---|---|
| Transfer Rates | 1.5 | 3.0 | Gbps | |
| eSATA | | | | No |
| xSATA | | | | No |
| Backplane | | | | No |
| Internal Cable | | | | Yes |


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#### 5.14.2.3 PCB Stackup Specifications

Table 5-46 shows the stackup and feature sizes required for SATA.

**Table 5-46. SATA PCB Stackup Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| PCB Routing/Plane Layers | 4 | 6 | | Layers |
| Signal Routing Layers | 2 | 3 | | Layers |
| Number of ground plane cuts allowed within SATA routing region | | | 0 | Layers |
| Number of layers between SATA routing region and reference ground plane | | | 0 | |
| PCB Routing Feature Size | 4 | | | Mils |
| PCB Trace Width w | 4 | | | Mils |
| PCB BGA escape via pad size | | 18 | | Mils |
| PCB BGA escape via hole size | | 8 | | Mils |
| Device BGA pad size (1) | | | | |

(1) Please refer to the Flip Chip Ball Grid Array Package Reference Guide (SPRU811) for device BGA pad size.

#### 5.14.2.4 Routing Specifications

The SATA data signal traces are edge-coupled and must be routed to achieve exactly 100 Ohms differential impedance. This is impacted by trace width, trace spacing, distance between planes, and dielectric material. Verify with a proper PCB manufacturing tool that the trace geometry for both data signal pairs results in exactly 100 ohms differential impedance traces. Table 5-47 shows the routing specifications for the data and REFCLK signals .

**Table 5-47. SATA Routing Specifications**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Device to SATA header trace length | | | 7000 | Mils |
| REFCLK trace length from oscillator to Device | | | 2000 | Mils |
| Number of stubs allowed on SATA traces | | | 0 | Stubs |
| TX/RX pair differential impedance | | 100 | | Ohms |
| Number of vias on each SATA trace | | | 3 | Vias (1) |
| SATA differential pair to any other trace spacing | 2*DS (2) | | | |

(1) Vias must be used in pairs with their distance minimized.
(2) DS is the differential spacing of the SATA traces.

#### 5.14.2.5 Coupling Capacitors

AC coupling capacitors are required on the receive data pair as well as the REFCLK pair. Table 5-48 shows the requirements for these capacitors.

**Table 5-48. SATA Bypass and Coupling Capacitors Requirements**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| SATA AC coupling capacitor value | 0.3 | 10 | 12 | nF |
| SATA AC coupling capacitor package size | | | 0603 | 10 Mils (1)(2) |

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor.
(2) The physical size of the capacitor should be as small as possible.

#### 5.14.2.6 SATA Interface Clock Source requirements

A high-quality, low-jitter differential clock source is required for the SATA PHY. The SATA interface requires a LVDS differential clock source to be provided at signals SATA_REFCLKP and SATA_REFCLKN. The clock source should be placed physically as close to the processor as possible.

Table 5-49 shows the requirements for the clock source.

**Table 5-49. SATA Input Clock Source Requirements**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Clock Frequency (1) | 75 | | 375 | MHz |
| Jitter | | | 50 | ps pk-pk |
| Duty Cycle | 40 | | 60 | % |
| Rise/Fall Time | | 700 | | ps |

(1) Discrete clock frequency points are supported based on the PLL multiplier used in the SATA PHY.

### 5.14.3 SATA Unused Signal Configuration

If the SATA interface is not used, the SATA signals should be configured as shown below.

**Table 5-50. Unused SATA Signal Configuration**

| SATA Signal Name | Configuration if SATA peripheral is not used |
|---|---|
| SATA_RXP | No Connect |
| $\overline{\text{SATA_RXN}}$ | No Connect |
| SATA_TXP | No Connect |
| $\overline{\text{SATA_TXN}}$ | No Connect |
| SATA_REFCLKP | No Connect |
| $\overline{\text{SATA_REFCLKN}}$ | No Connect |
| SATA_MPSWITCH | May be used as GPIO or other peripheral function |
| SATA_CP_DET | May be used as GPIO or other peripheral function |
| SATA_CP_POD | May be used as GPIO or other peripheral function |
| SATA_LED | May be used as GPIO or other peripheral function |
| SATA_REG | No Connect |
| SATA_VDDR | No Connect |
| SATA_VDD | Prior to silicon revision 2.0, this supply must be connected to a static 1.2V nominal supply. For silicon revision 2.0 and later, this supply may be left unconnected for additional power conservation. |
| SATA_VSS | Vss |


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## 5.15 Multichannel Audio Serial Port (McASP)

The McASP serial port is specifically designed for multichannel audio applications. Its key features are:

- Flexible clock and frame sync generation logic and on-chip dividers
- Up to sixteen transmit or receive data pins and serializers
- Large number of serial data format options, including:
  - TDM Frames with 2 to 32 time slots per frame (periodic) or 1 slot per frame (burst)
  - Time slots of 8,12,16, 20, 24, 28, and 32 bits
  - First bit delay 0, 1, or 2 clocks
  - MSB or LSB first bit order
  - Left- or right-aligned data words within time slots
- DIT Mode with 384-bit Channel Status and 384-bit User Data registers
- Extensive error checking and mute generation logic
- All unused pins GPIO-capable
- Transmit & Receive FIFO Buffers allow the McASP to operate at a higher sample rate by making it more tolerant to DMA latency.
- Dynamic Adjustment of Clock Dividers
  - Clock Divider Value may be changed without resetting the McASP

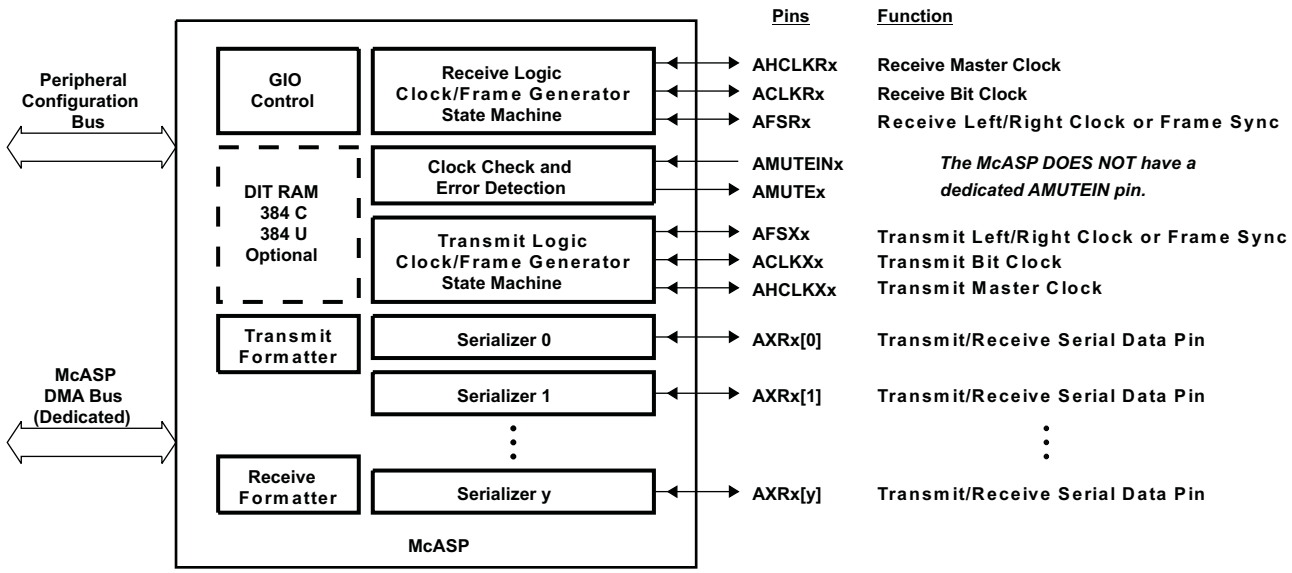


**Figure 5-31. McASP Block Diagram**

### 5.15.1 McASP Peripheral Registers Description(s)

Registers for the McASP are summarized in Table 5-51. The registers are accessed through the peripheral configuration port. The receive buffer registers (RBUF) and transmit buffer registers (XBUF) can also be accessed through the DMA port, as listed in Table 5-52

Registers for the McASP Audio FIFO (AFIFO) are summarized in Table 5-53. Note that the AFIFO Write FIFO (WFIFO) and Read FIFO (RFIFO) have independent control and status registers. The AFIFO control registers are accessed through the peripheral configuration port.

**Table 5-51. McASP Registers Accessed Through Peripheral Configuration Port**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 0000 | REV | Revision identification register |
| 0x01D0 0010 | PFUNC | Pin function register |
| 0x01D0 0014 | PDIR | Pin direction register |
| 0x01D0 0018 | PDOUT | Pin data output register |
| 0x01D0 001C | PDIN | Read returns: Pin data input register |
| 0x01D0 001C | PDSET | Writes affect: Pin data set register (alternate write address: PDOUT) |
| 0x01D0 0020 | PDCLR | Pin data clear register (alternate write address: PDOUT) |
| 0x01D0 0044 | GBLCTL | Global control register |
| 0x01D0 0048 | AMUTE | Audio mute control register |
| 0x01D0 004C | DLBCTL | Digital loopback control register |
| 0x01D0 0050 | DITCTL | DIT mode control register |
| 0x01D0 0060 | RGBLCTL | Receiver global control register: Alias of GBLCTL, only receive bits are affected - allows receiver to be reset independently from transmitter |
| 0x01D0 0064 | RMASK | Receive format unit bit mask register |
| 0x01D0 0068 | RFMT | Receive bit stream format register |
| 0x01D0 006C | AFSRCTL | Receive frame sync control register |
| 0x01D0 0070 | ACLKRCTL | Receive clock control register |
| 0x01D0 0074 | AHCLKRCTL | Receive high-frequency clock control register |
| 0x01D0 0078 | RTDM | Receive TDM time slot 0-31 register |
| 0x01D0 007C | RINTCTL | Receiver interrupt control register |
| 0x01D0 0080 | RSTAT | Receiver status register |
| 0x01D0 0084 | RSLOT | Current receive TDM time slot register |
| 0x01D0 0088 | RCLKCHK | Receive clock check control register |
| 0x01D0 008C | REVTCTL | Receiver DMA event control register |
| 0x01D0 00A0 | XGBLCTL | Transmitter global control register. Alias of GBLCTL, only transmit bits are affected - allows transmitter to be reset independently from receiver |
| 0x01D0 00A4 | XMASK | Transmit format unit bit mask register |
| 0x01D0 00A8 | XFMT | Transmit bit stream format register |
| 0x01D0 00AC | AFSXCTL | Transmit frame sync control register |
| 0x01D0 00B0 | ACLKXCTL | Transmit clock control register |
| 0x01D0 00B4 | AHCLKXCTL | Transmit high-frequency clock control register |
| 0x01D0 00B8 | XTDM | Transmit TDM time slot 0-31 register |
| 0x01D0 00BC | XINTCTL | Transmitter interrupt control register |
| 0x01D0 00C0 | XSTAT | Transmitter status register |
| 0x01D0 00C4 | XSLOT | Current transmit TDM time slot register |
| 0x01D0 00C8 | XCLKCHK | Transmit clock check control register |
| 0x01D0 00CC | XEVTCTL | Transmitter DMA event control register |
| 0x01D0 0100 | DITCSRA0 | Left (even TDM time slot) channel status register (DIT mode) 0 |
| 0x01D0 0104 | DITCSRA1 | Left (even TDM time slot) channel status register (DIT mode) 1 |
| 0x01D0 0108 | DITCSRA2 | Left (even TDM time slot) channel status register (DIT mode) 2 |


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**Table 5-51. McASP Registers Accessed Through Peripheral Configuration Port (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 010C | DITCSRA3 | Left (even TDM time slot) channel status register (DIT mode) 3 |
| 0x01D0 0110 | DITCSRA4 | Left (even TDM time slot) channel status register (DIT mode) 4 |
| 0x01D0 0114 | DITCSRA5 | Left (even TDM time slot) channel status register (DIT mode) 5 |
| 0x01D0 0118 | DITCSRB0 | Right (odd TDM time slot) channel status register (DIT mode) 0 |
| 0x01D0 011C | DITCSRB1 | Right (odd TDM time slot) channel status register (DIT mode) 1 |
| 0x01D0 0120 | DITCSRB2 | Right (odd TDM time slot) channel status register (DIT mode) 2 |
| 0x01D0 0124 | DITCSRB3 | Right (odd TDM time slot) channel status register (DIT mode) 3 |
| 0x01D0 0128 | DITCSRB4 | Right (odd TDM time slot) channel status register (DIT mode) 4 |
| 0x01D0 012C | DITCSRB5 | Right (odd TDM time slot) channel status register (DIT mode) 5 |
| 0x01D0 0130 | DITUDRA0 | Left (even TDM time slot) channel user data register (DIT mode) 0 |
| 0x01D0 0134 | DITUDRA1 | Left (even TDM time slot) channel user data register (DIT mode) 1 |
| 0x01D0 0138 | DITUDRA2 | Left (even TDM time slot) channel user data register (DIT mode) 2 |
| 0x01D0 013C | DITUDRA3 | Left (even TDM time slot) channel user data register (DIT mode) 3 |
| 0x01D0 0140 | DITUDRA4 | Left (even TDM time slot) channel user data register (DIT mode) 4 |
| 0x01D0 0144 | DITUDRA5 | Left (even TDM time slot) channel user data register (DIT mode) 5 |
| 0x01D0 0148 | DITUDRB0 | Right (odd TDM time slot) channel user data register (DIT mode) 0 |
| 0x01D0 014C | DITUDRB1 | Right (odd TDM time slot) channel user data register (DIT mode) 1 |
| 0x01D0 0150 | DITUDRB2 | Right (odd TDM time slot) channel user data register (DIT mode) 2 |
| 0x01D0 0154 | DITUDRB3 | Right (odd TDM time slot) channel user data register (DIT mode) 3 |
| 0x01D0 0158 | DITUDRB4 | Right (odd TDM time slot) channel user data register (DIT mode) 4 |
| 0x01D0 015C | DITUDRB5 | Right (odd TDM time slot) channel user data register (DIT mode) 5 |
| 0x01D0 0180 | SRCTL0 | Serializer control register 0 |
| 0x01D0 0184 | SRCTL1 | Serializer control register 1 |
| 0x01D0 0188 | SRCTL2 | Serializer control register 2 |
| 0x01D0 018C | SRCTL3 | Serializer control register 3 |
| 0x01D0 0190 | SRCTL4 | Serializer control register 4 |
| 0x01D0 0194 | SRCTL5 | Serializer control register 5 |
| 0x01D0 0198 | SRCTL6 | Serializer control register 6 |
| 0x01D0 019C | SRCTL7 | Serializer control register 7 |
| 0x01D0 01A0 | SRCTL8 | Serializer control register 8 |
| 0x01D0 01A4 | SRCTL9 | Serializer control register 9 |
| 0x01D0 01A8 | SRCTL10 | Serializer control register 10 |
| 0x01D0 01AC | SRCTL11 | Serializer control register 11 |
| 0x01D0 01B0 | SRCTL12 | Serializer control register 12 |
| 0x01D0 01B4 | SRCTL13 | Serializer control register 13 |
| 0x01D0 01B8 | SRCTL14 | Serializer control register 14 |
| 0x01D0 01BC | SRCTL15 | Serializer control register 15 |

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**Table 5-51. McASP Registers Accessed Through Peripheral Configuration Port (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 0200 | XBUF0(1) | Transmit buffer register for serializer 0 |
| 0x01D0 0204 | XBUF1(1) | Transmit buffer register for serializer 1 |
| 0x01D0 0208 | XBUF2(1) | Transmit buffer register for serializer 2 |
| 0x01D0 020C | XBUF3(1) | Transmit buffer register for serializer 3 |
| 0x01D0 0210 | XBUF4(1) | Transmit buffer register for serializer 4 |
| 0x01D0 0214 | XBUF5(1) | Transmit buffer register for serializer 5 |
| 0x01D0 0218 | XBUF6(1) | Transmit buffer register for serializer 6 |
| 0x01D0 021C | XBUF7(1) | Transmit buffer register for serializer 7 |
| 0x01D0 0220 | XBUF8(1) | Transmit buffer register for serializer 8 |
| 0x01D0 0224 | XBUF9(1) | Transmit buffer register for serializer 9 |
| 0x01D0 0228 | XBUF10(1) | Transmit buffer register for serializer 10 |
| 0x01D0 022C | XBUF11(1) | Transmit buffer register for serializer 11 |
| 0x01D0 0230 | XBUF12(1) | Transmit buffer register for serializer 12 |
| 0x01D0 0234 | XBUF13(1) | Transmit buffer register for serializer 13 |
| 0x01D0 0238 | XBUF14(1) | Transmit buffer register for serializer 14 |
| 0x01D0 023C | XBUF15(1) | Transmit buffer register for serializer 15 |
| 0x01D0 0280 | RBUF0(2) | Receive buffer register for serializer 0 |
| 0x01D0 0284 | RBUF1(2) | Receive buffer register for serializer 1 |
| 0x01D0 0288 | RBUF2(2) | Receive buffer register for serializer 2 |
| 0x01D0 028C | RBUF3(2) | Receive buffer register for serializer 3 |
| 0x01D0 0290 | RBUF4(2) | Receive buffer register for serializer 4 |
| 0x01D0 0294 | RBUF5(2) | Receive buffer register for serializer 5 |
| 0x01D0 0298 | RBUF6(2) | Receive buffer register for serializer 6 |
| 0x01D0 029C | RBUF7(2) | Receive buffer register for serializer 7 |
| 0x01D0 02A0 | RBUF8(2) | Receive buffer register for serializer 8 |
| 0x01D0 02A4 | RBUF9(2) | Receive buffer register for serializer 9 |
| 0x01D0 02A8 | RBUF10(2) | Receive buffer register for serializer 10 |
| 0x01D0 02AC | RBUF11(2) | Receive buffer register for serializer 11 |
| 0x01D0 02B0 | RBUF12(2) | Receive buffer register for serializer 12 |
| 0x01D0 02B4 | RBUF13(2) | Receive buffer register for serializer 13 |
| 0x01D0 02B8 | RBUF14(2) | Receive buffer register for serializer 14 |
| 0x01D0 02BC | RBUF15(2) | Receive buffer register for serializer 15 |

(1) Writes to XRBUF originate from peripheral configuration port only when XBUSEL = 1 in XFMT.
(2) Reads from XRBUF originate on peripheral configuration port only when RBUSEL = 1 in RFMT.

**Table 5-52. McASP Registers Accessed Through DMA Port**

| ACCESS TYPE | BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| Read Accesses | 0x01D0 2000 | RBUF | Receive buffer DMA port address. Cycles through receive serializers, skipping over transmit serializers and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Reads from DMA port only if XBUSEL = 0 in XFMT. |
| Write Accesses | 0x01D0 2000 | XBUF | Transmit buffer DMA port address. Cycles through transmit serializers, skipping over receive and inactive serializers. Starts at the lowest serializer at the beginning of each time slot. Writes to DMA port only if RBUSEL = 0 in RFMT. |


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**Table 5-53. McASP AFIFO Registers Accessed Through Peripheral Configuration Port**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01D0 1000 | AFIFOREV | AFIFO revision identification register |
| 0x01D0 1010 | WFIFOCTL | Write FIFO control register |
| 0x01D0 1014 | WFIFOSTS | Write FIFO status register |
| 0x01D0 1018 | RFIFOCTL | Read FIFO control register |
| 0x01D0 101C | RFIFOSTS | Read FIFO status register |

## *5.15.2 McASP Electrical Data/Timing*

### 5.15.2.1 Multichannel Audio Serial Port 0 (McASP0) Timing

Table 5-54 and Table 5-56 assume testing over recommended operating conditions (see Figure 5-32 and Figure 5-33).

**Table 5-54. Timing Requirements for McASP0 (1.3V, 1.2V, 1.1V)(1)(2)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 25 | | 28 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 12.5 | | 14 | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | AHCLKR/X ext | 25(3) | | 28(3) | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/W high or low | AHCLKR/X ext | 12.5 | | 14 | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, AFSR/X input to ACLKR/X(4) | AHCLKR/X int | 11.5 | | 12 | | ns |
| | | | AHCLKR/X ext input | 4 | | 5 | | ns |
| | | | AHCLKR/X ext output | 4 | | 5 | | ns |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, AFSR/X input after ACLKR/X(4) | AHCLKR/X int | -1 | | -2 | | ns |
| | | | AHCLKR/X ext input | 1 | | 1 | | ns |
| | | | AHCLKR/X ext output | 1 | | 1 | | ns |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, AXR0[n] input to ACLKR/X(4)(5) | AHCLKR/X int | 11.5 | | 12 | | ns |
| | | | AHCLKR/X ext | 4 | | 5 | | ns |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, AXR0[n] input after ACLKR/X(4)(5) | AHCLKR/X int | -1 | | -2 | | ns |
| | | | AHCLKR/X ext input | 3 | | 4 | | ns |
| | | | AHCLKR/X ext output | 3 | | 4 | | ns |

(1) ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) This timing is limited by the timing shown or 2P, whichever is greater.
(4) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0
(5) McASP0 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX0

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**Table 5-55. Timing Requirements for McASP0 (1.0V)(1)(2)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 35 | | ns |
| 2 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | 17.5 | | ns |
| 3 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | AHCLKR/X ext | 35(3) | | ns |
| 4 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/W high or low | AHCLKR/X ext | 17.5 | | ns |
| 5 | $t_{su(AFSRX-ACLKRX)}$ | Setup time, AFSR/X input to ACLKR/X(4) | AHCLKR/X int | 16 | | ns |
| | | | AHCLKR/X ext input | 5.5 | | ns |
| | | | AHCLKR/X ext output | 5.5 | | ns |
| 6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, AFSR/X input after ACLKR/X(4) | AHCLKR/X int | -2 | | ns |
| | | | AHCLKR/X ext input | 1 | | ns |
| | | | AHCLKR/X ext output | 1 | | ns |
| 7 | $t_{su(AXR-ACLKRX)}$ | Setup time, AXR0[n] input to ACLKR/X(4)(5) | AHCLKR/X int | 16 | | ns |
| | | | AHCLKR/X ext | 5.5 | | ns |
| 8 | $t_{h(ACLKRX-AXR)}$ | Hold time, AXR0[n] input after ACLKR/X(4)(5) | AHCLKR/X int | -2 | | ns |
| | | | AHCLKR/X ext input | 5 | | ns |
| | | | AHCLKR/X ext output | 5 | | ns |

(1) ACLKX0 internal – McASP0 ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKRCTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) P = SYSCLK2 period
(3) This timing is limited by the timing shown or 2P, whichever is greater.
(4) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0
(5) McASP0 ACLKXCTL.ASYNC=0: Receiver is clocked by transmitter's ACLKX0


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### Table 5-56. Switching Characteristics for McASP0 (1.3V, 1.2V, 1.1V)(1)

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 25 | | 28 | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | AH – 2.5(2) | | AH – 2.5(2) | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | ACLKR/X int | 25(3)(4) | | 28(3)(4) | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X int | A – 2.5(5) | | A – 2.5(5) | | ns |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid(6) | ACLKR/X int | -1 | 6 | -1 | 8 | ns |
| | | | ACLKR/X ext input | 2 | 13.5 | 2 | 14.5 | ns |
| | | | ACLKR/X ext output | 2 | 13.5 | 2 | 14.5 | ns |
| 14 | $t_{d(ACLKX-AXRV)}$ | Delay time, ACLKX transmit edge to AXR output valid | ACLKR/X int | -1 | 6 | -1 | 8 | ns |
| | | | ACLKR/X ext input | 2 | 13.5 | 2 | 15 | ns |
| | | | ACLKR/X ext output | 2 | 13.5 | 2 | 15 | ns |
| 15 | $t_{dis(ACLKX-AXRHZ)}$ | Disable time, ACLKR/X transmit edge to AXR high impedance following last data bit | ACLKR/X int | 0 | 6 | 0 | 8 | ns |
| | | | ACLKR/X ext | 2 | 13.5 | 2 | 15 | ns |

(1) McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKR0CTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(3) P = SYSCLK2 period
(4) This timing is limited by the timing shown or 2P, whichever is greater.
(5) A = (ACLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(6) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0

### Table 5-57. Switching Characteristics for McASP0 (1.0V)(1)

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 9 | $t_{c(AHCLKRX)}$ | Cycle time, AHCLKR/X | | 35 | | ns |
| 10 | $t_{w(AHCLKRX)}$ | Pulse duration, AHCLKR/X high or low | | AH – 2.5(2) | | ns |
| 11 | $t_{c(ACLKRX)}$ | Cycle time, ACLKR/X | ACLKR/X int | 35(3)(4) | | ns |
| 12 | $t_{w(ACLKRX)}$ | Pulse duration, ACLKR/X high or low | ACLKR/X int | A – 2.5(5) | | ns |
| 13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, ACLKR/X transmit edge to AFSX/R output valid(6) | ACLKR/X int | -0.5 | 10 | ns |
| | | | ACLKR/X ext input | 2 | 19 | ns |
| | | | ACLKR/X ext output | 2 | 19 | ns |
| 14 | $t_{d(ACLKX-AXRV)}$ | Delay time, ACLKX transmit edge to AXR output valid | ACLKR/X int | -0.5 | 10 | ns |
| | | | ACLKR/X ext input | 2 | 19 | ns |
| | | | ACLKR/X ext output | 2 | 19 | ns |
| 15 | $t_{dis(ACLKX-AXRHZ)}$ | Disable time, ACLKR/X transmit edge to AXR high impedance following last data bit | ACLKR/X int | 0 | 10 | ns |
| | | | ACLKR/X ext | 2 | 19 | ns |

(1) McASP0 ACLKX0 internal – ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX0 external input – McASP0 ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX0 external output – McASP0ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR0 internal – McASP0 ACLKR0CTL.CLKRM = 1, PDIR.ACLKR =1
ACLKR0 external input – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR0 external output – McASP0 ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1
(2) AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(3) P = SYSCLK2 period
(4) This timing is limited by the timing shown or 2P, whichever is greater.
(5) A = (ACLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.
(6) McASP0 ACLKXCTL.ASYNC=1: Receiver is clocked by its own ACLKR0

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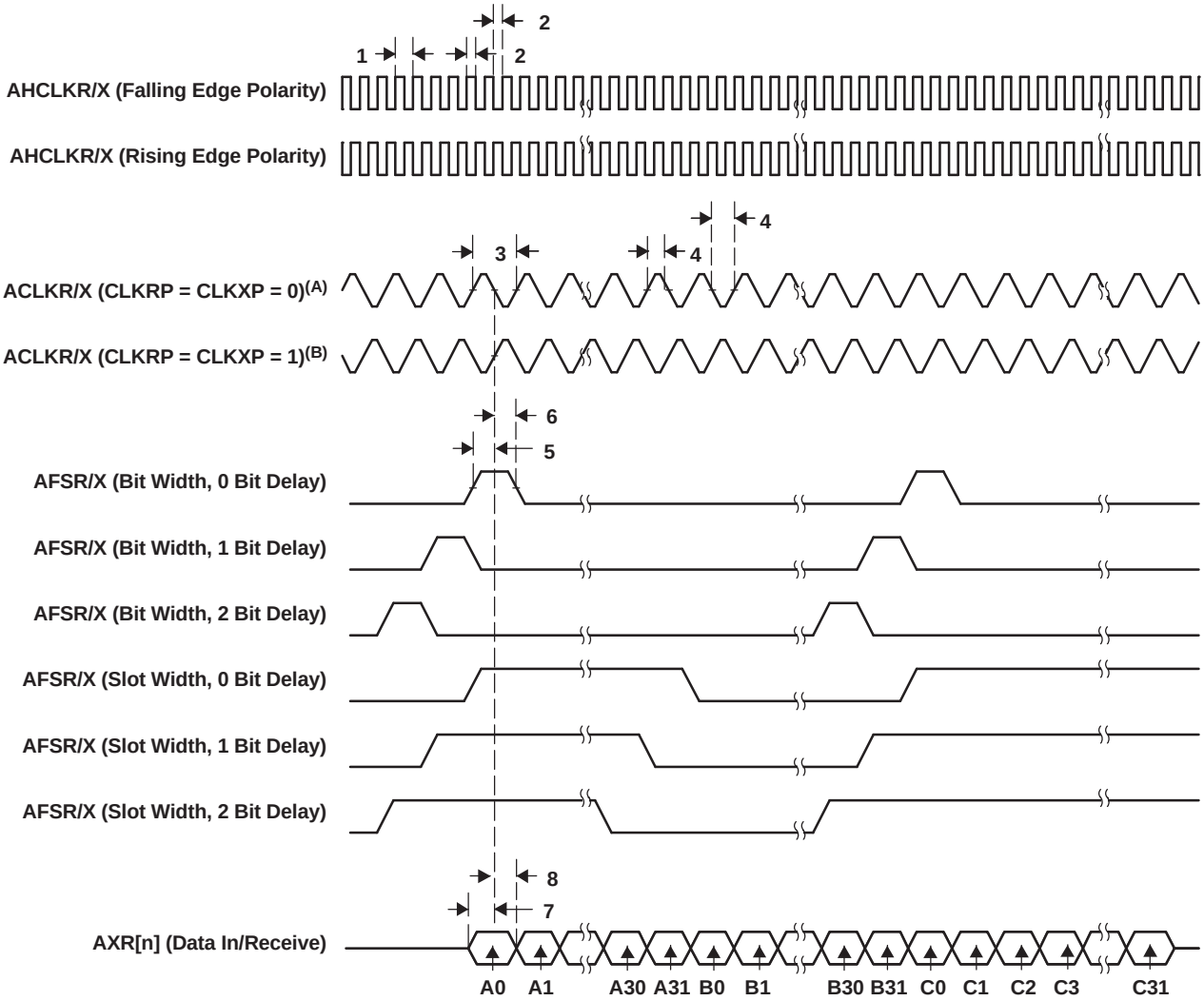


A. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

**Figure 5-32. McASP Input Timings**


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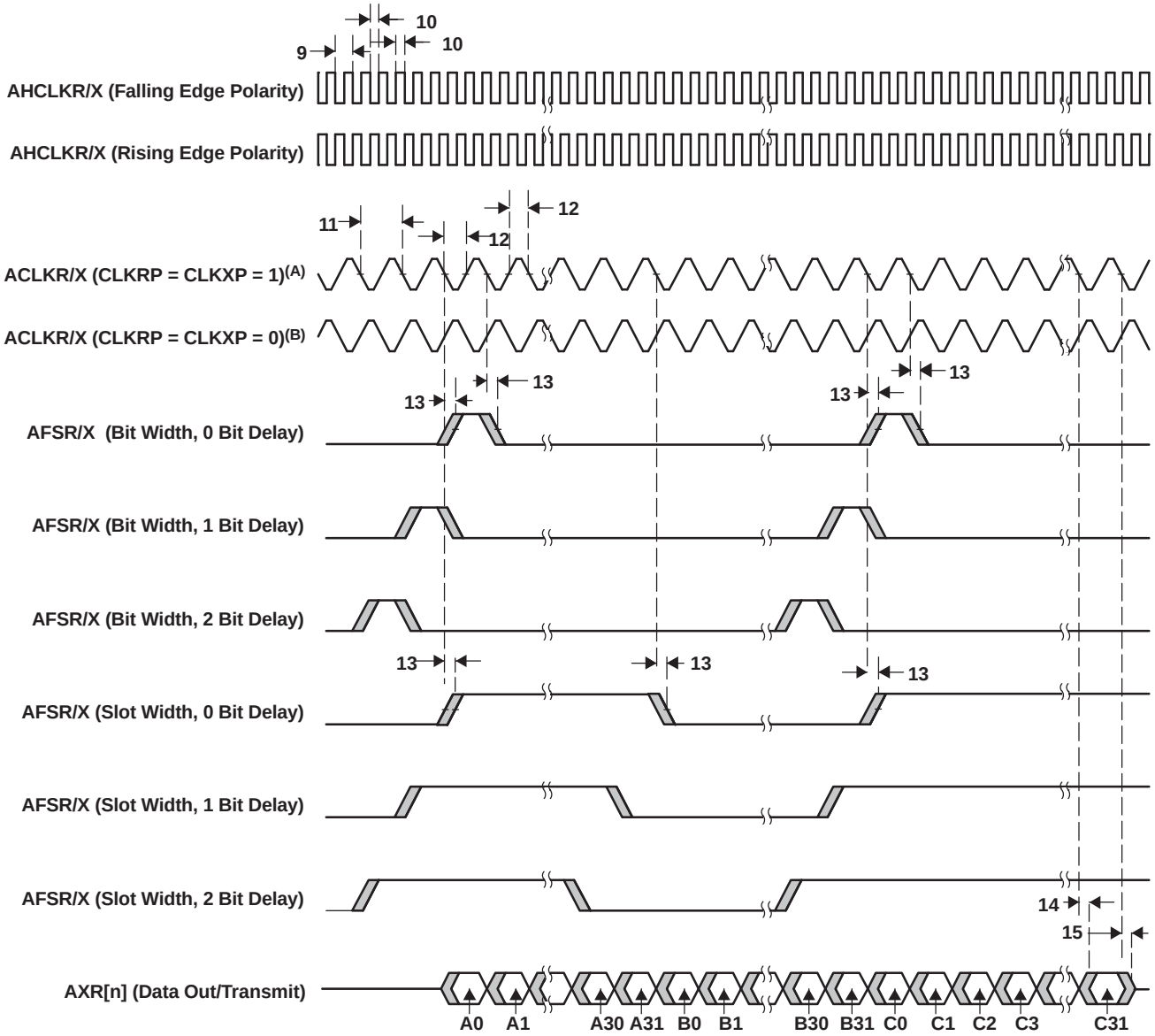


A. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

**Figure 5-33. McASP Output Timings**

## 5.16 Multichannel Buffered Serial Port (McBSP)

The McBSP provides these functions:

- Full-duplex communication
- Double-buffered data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit
- Direct interface to industry-standard codecs, analog interface chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- External shift clock or an internal, programmable frequency shift clock for data transfer
- Transmit & Receive FIFO Buffers allow the McBSP to operate at a higher sample rate by making it more tolerant to DMA latency

If internal clock source is used, the CLKGDV field of the Sample Rate Generator Register (SRGR) must always be set to a value of 1 or greater.

### *5.16.1 McBSP Peripheral Register Description(s)*

**Table 5-58. McBSP/FIFO Registers**

| McBSP0 BYTE ADDRESS | McBSP1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| **McBSP Registers** | | | |
| 0x01D1 0000 | 0x01D1 1000 | DRR | McBSP Data Receive Register (read-only) |
| 0x01D1 0004 | 0x01D1 1004 | DXR | McBSP Data Transmit Register |
| 0x01D1 0008 | 0x01D1 1008 | SPCR | McBSP Serial Port Control Register |
| 0x01D1 000C | 0x01D1 100C | RCR | McBSP Receive Control Register |
| 0x01D1 0010 | 0x01D1 1010 | XCR | McBSP Transmit Control Register |
| 0x01D1 0014 | 0x01D1 1014 | SRGR | McBSP Sample Rate Generator register |
| 0x01D1 0018 | 0x01D1 1018 | MCR | McBSP Multichannel Control Register |
| 0x01D1 001C | 0x01D1 101C | RCERE0 | McBSP Enhanced Receive Channel Enable Register 0 Partition A/B |
| 0x01D1 0020 | 0x01D1 1020 | XCERE0 | McBSP Enhanced Transmit Channel Enable Register 0 Partition A/B |
| 0x01D1 0024 | 0x01D1 1024 | PCR | McBSP Pin Control Register |
| 0x01D1 0028 | 0x01D1 1028 | RCERE1 | McBSP Enhanced Receive Channel Enable Register 1 Partition C/D |
| 0x01D1 002C | 0x01D1 102C | XCERE1 | McBSP Enhanced Transmit Channel Enable Register 1 Partition C/D |
| 0x01D1 0030 | 0x01D1 1030 | RCERE2 | McBSP Enhanced Receive Channel Enable Register 2 Partition E/F |
| 0x01D1 0034 | 0x01D1 1034 | XCERE2 | McBSP Enhanced Transmit Channel Enable Register 2 Partition E/F |
| 0x01D1 0038 | 0x01D1 1038 | RCERE3 | McBSP Enhanced Receive Channel Enable Register 3 Partition G/H |
| 0x01D1 003C | 0x01D1 103C | XCERE3 | McBSP Enhanced Transmit Channel Enable Register 3 Partition G/H |
| **McBSP FIFO Control and Status Registers** | | | |
| 0x01D1 0800 | 0x01D1 1800 | BFIFOREV | BFIFO Revision Identification Register |
| 0x01D1 0810 | 0x01D1 1810 | WFIFOCTL | Write FIFO Control Register |
| 0x01D1 0814 | 0x01D1 1814 | WFIFOSTS | Write FIFO Status Register |
| 0x01D1 0818 | 0x01D1 1818 | RFIFOCTL | Read FIFO Control Register |
| 0x01D1 081C | 0x01D1 181C | RFIFOSTS | Read FIFO Status Register |
| **McBSP FIFO Data Registers** | | | |
| 0x01F1 0000 | 0x01F1 1000 | RBUF | McBSP FIFO Receive Buffer |
| 0x01F1 0000 | 0x01F1 1000 | XBUF | McBSP FIFO Transmit Buffer |


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### 5.16.2 McBSP Electrical Data/Timing

The following assume testing over recommended operating conditions.

#### 5.16.2.1 Multichannel Buffered Serial Port (McBSP) Timing

**Table 5-59. Timing Requirements for McBSP0 [1.3V, 1.2V, 1.1V](1) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P or 20(2)(3) | | 2P or 25(2)(3) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P - 1(4) | | P - 1(4) | | ns |
| 5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 14 | | 15.5 | | ns |
| | | | CLKR ext | 4 | | 5 | | |
| 6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 6 | | 6 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| 7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 14 | | 15.5 | | ns |
| | | | CLKR ext | 4 | | 5 | | |
| 8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 3 | | 3 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| 10 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 14 | | 15.5 | | ns |
| | | | CLKX ext | 4 | | 5 | | |
| 11 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | 6 | | 6 | | ns |
| | | | CLKX ext | 3 | | 3 | | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

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**Table 5-60. Timing Requirements for McBSP0 [1.0V](1) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P or 26.6(2)(3) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P - 1(4) | | ns |
| 5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 20 | | ns |
| | | | CLKR ext | 5 | | |
| 6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 6 | | ns |
| | | | CLKR ext | 3 | | |
| 7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 20 | | ns |
| | | | CLKR ext | 5 | | |
| 8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 3 | | ns |
| | | | CLKR ext | 3 | | |
| 10 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 20 | | ns |
| | | | CLKX ext | 5 | | |
| 11 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | 6 | | ns |
| | | | CLKX ext | 3 | | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.


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**Table 5-61. Switching Characteristics for McBSP0 [1.3V, 1.2V, 1.1V](1)(2) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(CKSH-CKRXH)}$ | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | 2 | 14.5 | 2 | 16 | ns |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P or 20(3)(4)(5) | | 2P or 25(3)(4)(5) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C - 2(6) | C + 2(6) | C - 2(6) | C + 2(6) | ns |
| 4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | -4 | 5.5 | -4 | 5.5 | ns |
| | | | CLKR ext | 2 | 14.5 | 2 | 16 | |
| 9 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | -4 | 5.5 | -4 | 5.5 | ns |
| | | | CLKX ext | 2 | 14.5 | 2 | 16 | |
| 12 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | CLKX int | -4 | 7.5 | -5.5 | 7.5 | ns |
| | | | CLKX ext | -2 | 16 | -22 | 16 | |
| 13 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | CLKX int | -4 + D1(7) | 5.5 + D2(7) | -4 + D1(7) | 5.5 + D2(7) | ns |
| | | | CLKX ext | 2 + D1(7) | 14.5 + D2(7) | 2 + D1(7) | 16 + D2(7) | |
| 14 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid<br>ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX int | -4(8) | 5(8) | -4(8) | 5(8) | ns |
| | | | FSX ext | -2(8) | 14.5(8) | -2(8) | 16(8) | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

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**Table 5-62. Switching Characteristics for McBSP0 [1.0V](1) (2) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{d(CKSH-CKRXH)}$ | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | 3 | 21.5 | ns |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P or 26.6(3)(4)(5) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C - 2(6) | C + 2(6) | ns |
| 4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | -4 | 10 | ns |
| | | | CLKR ext | 2.5 | 21.5 | |
| 9 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | -4 | 10 | ns |
| | | | CLKX ext | 2.5 | 21.5 | |
| 12 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | CLKX int | -4 | 10 | ns |
| | | | CLKX ext | -2 | 21.5 | |
| 13 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | CLKX int | -4 + D1(7) | 10 + D2(7) | ns |
| | | | CLKX ext | 2.5 + D1(7) | 21.5 + D2(7) | |
| 14 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid | FSX int | -4(8) | 5(8) | ns |
| | | ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX ext | -2(8) | 21.5(8) | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P


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**Table 5-63. Timing Requirements for McBSP1 [1.3V, 1.2V, 1.1V](1) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P or 20(2)(3) | | 2P or 25(2) (4) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P - 1(5) | | P - 1(6) | | ns |
| 5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 15 | | 18 | | ns |
| | | | CLKR ext | 5 | | 5 | | |
| 6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 6 | | 6 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| 7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 15 | | 18 | | ns |
| | | | CLKR ext | 5 | | 5 | | |
| 8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 3 | | 3 | | ns |
| | | | CLKR ext | 3 | | 3 | | |
| 10 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 15 | | 18 | | ns |
| | | | CLKX ext | 5 | | 5 | | |
| 11 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | 6 | | 6 | | ns |
| | | | CLKX ext | 3 | | 3 | | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(5) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.
(6) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

**Table 5-64. Timing Requirements for McBSP1 [1.0V](1) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X ext | 2P or 26.6(2)(3) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X ext | P - 1(4) | | ns |
| 5 | $t_{su(FRH-CKRL)}$ | Setup time, external FSR high before CLKR low | CLKR int | 21 | | ns |
| | | | CLKR ext | 10 | | |
| 6 | $t_{h(CKRL-FRH)}$ | Hold time, external FSR high after CLKR low | CLKR int | 6 | | ns |
| | | | CLKR ext | 3 | | |
| 7 | $t_{su(DRV-CKRL)}$ | Setup time, DR valid before CLKR low | CLKR int | 21 | | ns |
| | | | CLKR ext | 10 | | |
| 8 | $t_{h(CKRL-DRV)}$ | Hold time, DR valid after CLKR low | CLKR int | 3 | | ns |
| | | | CLKR ext | 3 | | |
| 10 | $t_{su(FXH-CKXL)}$ | Setup time, external FSX high before CLKX low | CLKX int | 21 | | ns |
| | | | CLKX ext | 10 | | |
| 11 | $t_{h(CKXL-FXH)}$ | Hold time, external FSX high after CLKX low | CLKX int | 6 | | ns |
| | | | CLKX ext | 3 | | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(3) Use whichever value is greater. Minimum CLKR/X cycle times *must* be met, even when CLKR/X is generated by an internal clock source. The minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) This parameter applies to the maximum McBSP frequency. Operate serial clocks (CLKR/X) in the reasonable range of 40/60 duty cycle.

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**Table 5-65. Switching Characteristics for McBSP1 [1.3V, 1.2V, 1.1V](1) (2) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(CKSH-CKRXH)}$ | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | 0.5 | 16.5 | 1.5 | 18 | ns |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P or 20(3)(4)(5) | | 2P or 25(3)(4) (5) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C - 2(6) | C + 2(6) | C - 2(6) | C + 2(6) | ns |
| 4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | -4 | 6.5 | -4 | 13 | ns |
| | | | CLKR ext | 1 | 16.5 | 1 | 18 | |
| 9 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | -4 | 6.5 | -4 | 13 | ns |
| | | | CLKX ext | 1 | 16.5 | 1 | 18 | |
| 12 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | CLKX int | -4 | 6.5 | -4 | 13 | ns |
| | | | CLKX ext | -2 | 16.5 | -2 | 18 | |
| 13 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | CLKX int | -4 + D1(7) | 6.5 + D2(7) | -4 + D1(7) | 13 + D2(7) | ns |
| | | | CLKX ext | 1 + D1(7) | 16.5 + D2(7) | 1 + D1(7) | 18 + D2(7) | |
| 14 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid<br>ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX int | -4(8) | 6.5(8) | -4(8) | 13(8) | ns |
| | | | FSX ext | -2(8) | 16.5(8) | -2(8) | 18(9) | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(9) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P


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**Table 5-66. Switching Characteristics for McBSP1 [1.0V](1) (2) (see Figure 5-34)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 1 | $t_{d(CKSH-CKRXH)}$ | Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input | | 1.5 | 23 | ns |
| 2 | $t_{c(CKRX)}$ | Cycle time, CLKR/X | CLKR/X int | 2P or 26.6(3)(4)(5) | | ns |
| 3 | $t_{w(CKRX)}$ | Pulse duration, CLKR/X high or CLKR/X low | CLKR/X int | C - 2(6) | C + 2(6) | ns |
| 4 | $t_{d(CKRH-FRV)}$ | Delay time, CLKR high to internal FSR valid | CLKR int | -4 | 13 | ns |
| | | | CLKR ext | 2.5 | 23 | |
| 9 | $t_{d(CKXH-FXV)}$ | Delay time, CLKX high to internal FSX valid | CLKX int | -4 | 13 | ns |
| | | | CLKX ext | 1 | 23 | |
| 12 | $t_{dis(CKXH-DXHZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | CLKX int | -4 | 13 | ns |
| | | | CLKX ext | -2 | 23 | |
| 13 | $t_{d(CKXH-DXV)}$ | Delay time, CLKX high to DX valid | CLKX int | -4 + D1(7) | 13 + D2(8) | ns |
| | | | CLKX ext | 1 + D1(8) | 23 + D2(8) | |
| 14 | $t_{d(FXH-DXV)}$ | Delay time, FSX high to DX valid<br>ONLY applies when in data delay 0 (XDATDLY = 00b) mode | FSX int | -4(9) | 13(9) | ns |
| | | | FSX ext | -2(9) | 23(9) | |

(1) CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) Minimum delay times also represent minimum output hold times.
(3) Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLKR/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
(4) P = AYNC3 period in ns. For example, when the ASYNC clock domain is running at 100 MHz, use 10 ns.
(5) Use whichever value is greater.
(6) C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = ASYNC period)
S = sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see (4) above).
(7) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(8) Extra delay from CLKX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P
(9) Extra delay from FSX high to DX valid **applies *only* to the first data bit of a device**, if and only if DXENA = 1 in SPCR.
if DXENA = 0, then D1 = D2 = 0
if DXENA = 1, then D1 = 6P, D2 = 12P

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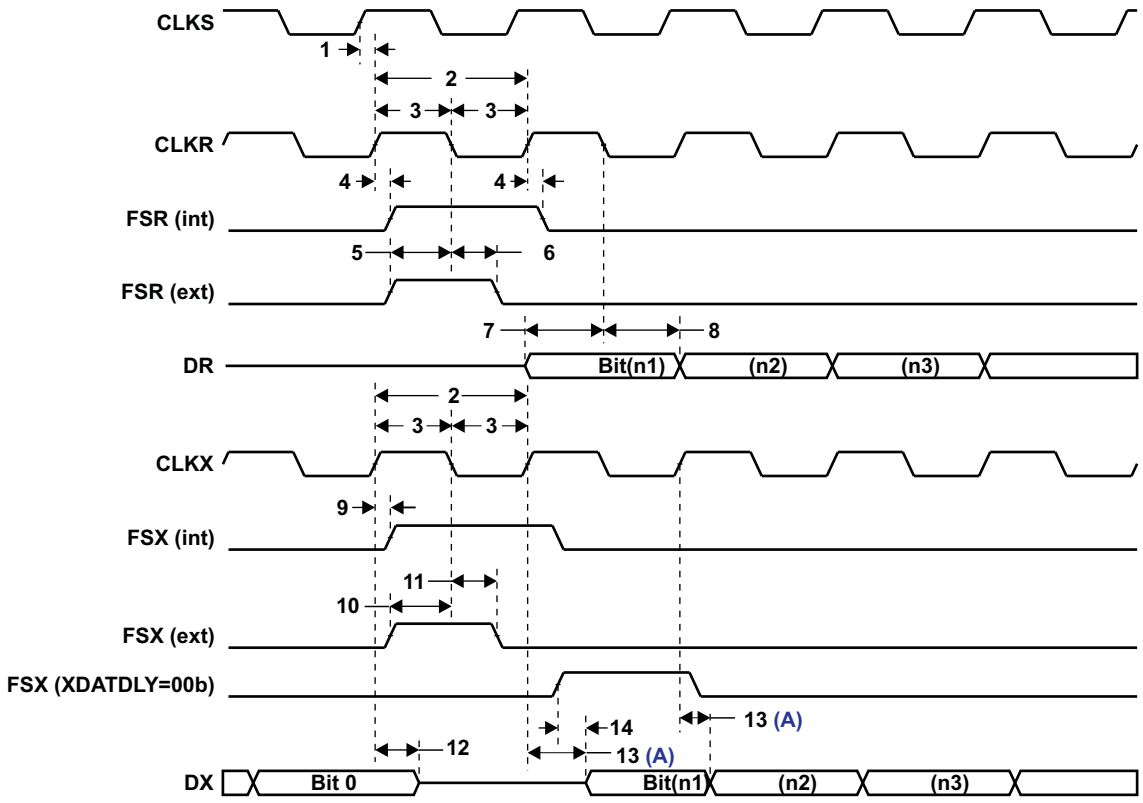


**Figure 5-34. McBSP Timing(B)**

**Table 5-67. Timing Requirements for McBSP0 FSR When GSYNC = 1 (see Figure 5-35)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(FRH-CKSH)}$ | Setup time, FSR high before CLKS high | 4 | | 4.5 | | 5 | | ns |
| 2 | $t_{h(CKSH-FRH)}$ | Hold time, FSR high after CLKS high | 4 | | 4 | | 4 | | ns |

**Table 5-68. Timing Requirements for McBSP1 FSR When GSYNC = 1 (see Figure 5-35)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(FRH-CKSH)}$ | Setup time, FSR high before CLKS high | 5 | | 5 | | 10 | | ns |
| 2 | $t_{h(CKSH-FRH)}$ | Hold time, FSR high after CLKS high | 4 | | 4 | | 4 | | ns |

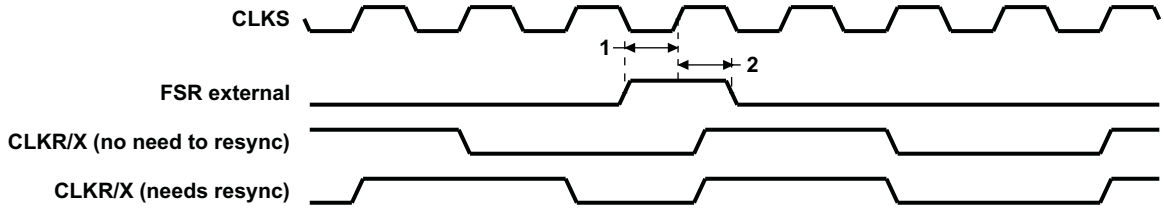


**Figure 5-35. FSR Timing When GSYNC = 1**


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## 5.17 Serial Peripheral Interface Ports (SPI0, SPI1)

Figure 5-36 is a block diagram of the SPI module, which is a simple shift register and buffer plus control logic. Data is written to the shift register before transmission occurs and is read from the buffer at the end of transmission. The SPI can operate either as a master, in which case, it initiates a transfer and drives the SPIx_CLK pin, or as a slave. Four clock phase and polarity options are supported as well as many data formatting options.

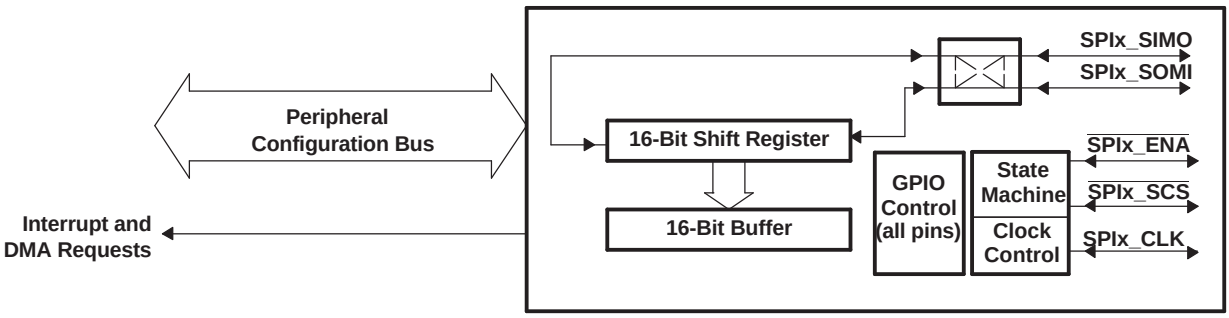


**Figure 5-36. Block Diagram of SPI Module**

The SPI supports 3-, 4-, and 5-pin operation with three basic pins (SPIx_CLK, SPIx_SIMO, and SPIx_SOMI) and two optional pins ($\overline{\text{SPIx_SCS}}$, $\overline{\text{SPIx_ENA}}$).

The optional $\overline{\text{SPIx_SCS}}$ (Slave Chip Select) pin is most useful to enable in slave mode when there are other slave devices on the same SPI port. The device will only shift data and drive the SPIx_SOMI pin when $\overline{\text{SPIx_SCS}}$ is held low.

In slave mode, $\overline{\text{SPIx_ENA}}$ is an optional output. The $\overline{\text{SPIx_ENA}}$ output provides the status of the internal transmit buffer (SPIDAT0/1 registers). In four-pin mode with the enable option, $\overline{\text{SPIx_ENA}}$ is asserted only when the transmit buffer is full, indicating that the slave is ready to begin another transfer. In five-pin mode, the $\overline{\text{SPIx_ENA}}$ is additionally qualified by $\overline{\text{SPIx_SCS}}$ being asserted. This allows a single handshake line to be shared by multiple slaves on the same SPI bus.

In master mode, the $\overline{\text{SPIx_ENA}}$ pin is an optional input and the master can be configured to delay the start of the next transfer until the slave asserts $\overline{\text{SPIx_ENA}}$. The addition of this handshake signal simplifies SPI communications and, on average, increases SPI bus throughput since the master does not need to delay each transfer long enough to allow for the worst-case latency of the slave device. Instead, each transfer can begin as soon as both the master and slave have actually serviced the previous SPI transfer.

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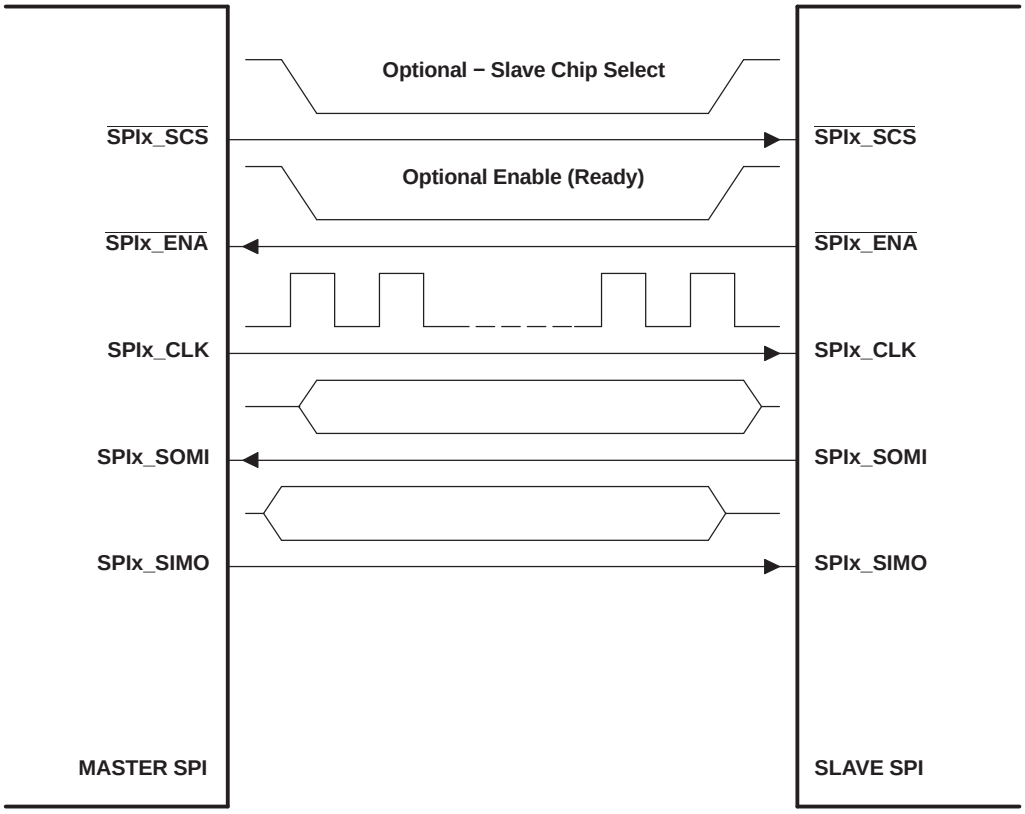


**Figure 5-37. Illustration of SPI Master-to-SPI Slave Connection**


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### 5.17.1 SPI Peripheral Registers Description(s)

Table 5-69 is a list of the SPI registers.

**Table 5-69. SPIx Configuration Registers**

| SPI0 BYTE ADDRESS | SPI1 BYTE ADDRESS | ACRONYM | DESCRIPTION |
|---|---|---|---|
| 0x01C4 1000 | 0x01F0 E000 | SPIGCR0 | Global Control Register 0 |
| 0x01C4 1004 | 0x01F0 E004 | SPIGCR1 | Global Control Register 1 |
| 0x01C4 1008 | 0x01F0 E008 | SPIINT0 | Interrupt Register |
| 0x01C4 100C | 0x01F0 E00C | SPILVL | Interrupt Level Register |
| 0x01C4 1010 | 0x01F0 E010 | SPIFLG | Flag Register |
| 0x01C4 1014 | 0x01F0 E014 | SPIPC0 | Pin Control Register 0 (Pin Function) |
| 0x01C4 1018 | 0x01F0 E018 | SPIPC1 | Pin Control Register 1 (Pin Direction) |
| 0x01C4 101C | 0x01F0 E01C | SPIPC2 | Pin Control Register 2 (Pin Data In) |
| 0x01C4 1020 | 0x01F0 E020 | SPIPC3 | Pin Control Register 3 (Pin Data Out) |
| 0x01C4 1024 | 0x01F0 E024 | SPIPC4 | Pin Control Register 4 (Pin Data Set) |
| 0x01C4 1028 | 0x01F0 E028 | SPIPC5 | Pin Control Register 5 (Pin Data Clear) |
| 0x01C4 102C | 0x01F0 E02C | Reserved | Reserved - Do not write to this register |
| 0x01C4 1030 | 0x01F0 E030 | Reserved | Reserved - Do not write to this register |
| 0x01C4 1034 | 0x01F0 E034 | Reserved | Reserved - Do not write to this register |
| 0x01C4 1038 | 0x01F0 E038 | SPIDAT0 | Shift Register 0 (without format select) |
| 0x01C4 103C | 0x01F0 E03C | SPIDAT1 | Shift Register 1 (with format select) |
| 0x01C4 1040 | 0x01F0 E040 | SPIBUF | Buffer Register |
| 0x01C4 1044 | 0x01F0 E044 | SPIEMU | Emulation Register |
| 0x01C4 1048 | 0x01F0 E048 | SPIDELAY | Delay Register |
| 0x01C4 104C | 0x01F0 E04C | SPIDEF | Default Chip Select Register |
| 0x01C4 1050 | 0x01F0 E050 | SPIFMT0 | Format Register 0 |
| 0x01C4 1054 | 0x01F0 E054 | SPIFMT1 | Format Register 1 |
| 0x01C4 1058 | 0x01F0 E058 | SPIFMT2 | Format Register 2 |
| 0x01C4 105C | 0x01F0 E05C | SPIFMT3 | Format Register 3 |
| 0x01C4 1060 | 0x01F0 E060 | INTVEC0 | Interrupt Vector for SPI INT0 |
| 0x01C4 1064 | 0x01F0 E064 | INTVEC1 | Interrupt Vector for SPI INT1 |

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## 5.17.2 SPI Electrical Data/Timing

### 5.17.2.1 Serial Peripheral Interface (SPI) Timing

Table 5-70 through Table 5-85 assume testing over recommended operating conditions (see Figure 5-38 through Figure 5-41).

**Table 5-70. General Timing Requirements for SPI0 Master Modes(1)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPC)M}$ | Cycle Time, SPI0_CLK, All Master Modes | | 20(2) | 256P | 30(2) | 256P | 40(2) | 256P | ns |
| 2 | $t_{w(SPCH)M}$ | Pulse Width High, SPI0_CLK, All Master Modes | | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | ns |
| 3 | $t_{w(SPCL)M}$ | Pulse Width Low, SPI0_CLK, All Master Modes | | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | ns |
| 4 | $t_{d(SIMO_SPC)M}$ | Delay, initial data bit valid on SPI0_SIMO after initial edge on SPI0_CLK(3) | Polarity = 0, Phase = 0, to SPI0_CLK rising | | 5 | | 5 | | 6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | | -0.5M+5 | | -0.5M+5 | | -0.5M+6 | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | | -0.5M+5 | | -0.5M+5 | | -0.5M+6 | |
| 5 | $t_{d(SPC_SIMO)M}$ | Delay, subsequent bits valid on SPI0_SIMO after transmit edge of SPI0_CLK | Polarity = 0, Phase = 0, from SPI0_CLK rising | | 5 | | 5 | | 6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK rising | | 5 | | 5 | | 6 | |
| 6 | $t_{oh(SPC_SIMO)M}$ | Output hold time, SPI0_SIMO valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0, from SPI0_CLK falling | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK rising | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK falling | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| 7 | $t_{su(SOMI_SPC)M}$ | Input Setup Time, SPI0_SOMI valid before receive edge of SPI0_CLK | Polarity = 0, Phase = 0, to SPI0_CLK falling | 1.5 | | 1.5 | | 1.5 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | 1.5 | | 1.5 | | 1.5 | | |
| 8 | $t_{ih(SPC_SOMI)M}$ | Input Hold Time, SPI0_SOMI valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0, from SPI0_CLK falling | 4 | | 4 | | 5 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK rising | 4 | | 4 | | 5 | | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 4 | | 4 | | 5 | | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK falling | 4 | | 4 | | 5 | | |

(1) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(2) This timing is limited by the timing shown or 3P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI0_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI0_SOMI.


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**Table 5-71. General Timing Requirements for SPI0 Slave Modes(1)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 9 | $t_{c(SPC)S}$ | Cycle Time, SPI0_CLK, All Slave Modes | | 40(2) | | 50(2) | | 60(2) | | ns |
| 10 | $t_{w(SPCH)S}$ | Pulse Width High, SPI0_CLK, All Slave Modes | | 18 | | 22 | | 27 | | ns |
| 11 | $t_{w(SPCL)S}$ | Pulse Width Low, SPI0_CLK, All Slave Modes | | 18 | | 22 | | 27 | | ns |
| 12 | $t_{su(SOMI_SPC)S}$ | Setup time, transmit data written to SPI before initial clock edge from master.(3) (4) | Polarity = 0, Phase = 0, to SPI0_CLK rising | 2P | | 2P | | 2P | | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | 2P | | 2P | | 2P | | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK falling | 2P | | 2P | | 2P | | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | 2P | | 2P | | 2P | | |
| 13 | $t_{d(SPC_SOMI)S}$ | Delay, subsequent bits valid on SPI0_SOMI after transmit edge of SPI0_CLK | Polarity = 0, Phase = 0, from SPI0_CLK rising | | 17 | | 20 | | 27 | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK falling | | 17 | | 20 | | 27 | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK falling | | 17 | | 20 | | 27 | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK rising | | 17 | | 20 | | 27 | |
| 14 | $t_{oh(SPC_SOMI)S}$ | Output hold time, SPI0_SOMI valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0, from SPI0_CLK falling | 0.5S-6 | | 0.5S-16 | | 0.5S-20 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK rising | 0.5S-6 | | 0.5S-16 | | 0.5S-20 | | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 0.5S-6 | | 0.5S-16 | | 0.5S-20 | | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK falling | 0.5S-6 | | 0.5S-16 | | 0.5S-20 | | |
| 15 | $t_{su(SIMO_SPC)S}$ | Input Setup Time, SPI0_SIMO valid before receive edge of SPI0_CLK | Polarity = 0, Phase = 0, to SPI0_CLK falling | 1.5 | | 1.5 | | 1.5 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | 1.5 | | 1.5 | | 1.5 | | |
| 16 | $t_{ih(SPC_SIMO)S}$ | Input Hold Time, SPI0_SIMO valid after receive edge of SPI0_CLK | Polarity = 0, Phase = 0, from SPI0_CLK falling | 4 | | 4 | | 5 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK rising | 4 | | 4 | | 5 | | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 4 | | 4 | | 5 | | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK falling | 4 | | 4 | | 5 | | |

(1) P = SYSCLK2 period; S = $t_{c(SPC)S}$ (SPI slave bit clock period)
(2) This timing is limited by the timing shown or 3P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI0_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI0_SIMO.
(4) Measured from the termination of the write of new data to the SPI module, In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by the CPU.

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**Table 5-72. Additional SPI0 Master Timings, 4-Pin Enable Option (1)(2)(3)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 17 | $t_{d(ENA_SPC)M}$ | Delay from slave assertion of $\overline{SPI0_ENA}$ active to first SPI0_CLK from master.(4) | Polarity = 0, Phase = 0, to SPI0_CLK rising | | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK falling | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| 18 | $t_{d(SPC_ENA)M}$ | Max delay for slave to deassert $\overline{SPI0_ENA}$ after final SPI0_CLK edge to ensure master does not begin the next transfer.(5) | Polarity = 0, Phase = 0, from SPI0_CLK falling | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK falling | | P+5 | | P+5 | | P+6 | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK rising | | P+5 | | P+5 | | P+6 | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-70).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before $\overline{SPI0_ENA}$ assertion.
(5) In the case where the master SPI is ready with new data before $\overline{SPI0_EN}$ A deassertion.

**Table 5-73. Additional SPI0 Master Timings, 4-Pin Chip Select Option (1)(2)(3)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 19 | $t_{d(SCS_SPC)M}$ | Delay from $\overline{SPI0_SCS}$ active to first SPI0_CLK(4) (5) | Polarity = 0, Phase = 0, to SPI0_CLK rising | 2P-1 | | 2P-2 | | 2P-3 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | 0.5M+2P-1 | | 0.5M+2P-2 | | 0.5M+2P-3 | | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK falling | 2P-1 | | 2P-2 | | 2P-3 | | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | 0.5M+2P-1 | | 0.5M+2P-2 | | 0.5M+2P-3 | | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-70).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before $\overline{SPI0_SCS}$ assertion.
(5) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].


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**Table 5-73. Additional SPI0 Master Timings, 4-Pin Chip Select Option (1)(2)(3) (continued)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 20 | $t_{d(SPC_SCS)M}$ | Delay from final SPI0_CLK edge to master deasserting SPI0_SCS (6) (7) | Polarity = 0, Phase = 0, from SPI0_CLK falling | 0.5M+P-1 | | 0.5M+P-2 | | 0.5M+P-3 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK falling | P-1 | | P-2 | | P-3 | | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 0.5M+P-1 | | 0.5M+P-2 | | 0.5M+P-3 | | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK rising | P-1 | | P-2 | | P-3 | | |

(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI0_SCS will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

**Table 5-74. Additional SPI0 Master Timings, 5-Pin Option (1)(2)(3)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 18 | $t_{d(SPC_ENA)M}$ | Max delay for slave to deassert SPI0_ENA after final SPI0_CLK edge to ensure master does not begin the next transfer. (4) | Polarity = 0, Phase = 0, from SPI0_CLK falling | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK falling | | P+5 | | P+5 | | P+6 | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK rising | | P+5 | | P+5 | | P+6 | |
| 20 | $t_{d(SPC_SCS)M}$ | Delay from final SPI0_CLK edge to master deasserting SPI0_SCS (5) (6) | Polarity = 0, Phase = 0, from SPI0_CLK falling | 0.5M+P-2 | | 0.5M+P-2 | | 0.5M+P-3 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK falling | P-2 | | P-2 | | P-3 | | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 0.5M+P-2 | | 0.5M+P-2 | | 0.5M+P-3 | | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK rising | P-2 | | P-2 | | P-3 | | |
| 21 | $t_{d(SCSL_ENAL)M}$ | Max delay for slave SPI to drive SPI0_ENA valid after master asserts SPI0_SCS to delay the master from beginning the next transfer, | | | C2TDELAY+P | | C2TDELAY+P | | C2TDELAY+P | ns |

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-71).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI0_ENA deassertion.
(5) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI0_SCS will remain asserted.
(6) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

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**Table 5-74. Additional SPI0 Master Timings, 5-Pin Option (1)(2)(3) (continued)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 22 | $t_{d(SCS_SPC)M}$ | Delay from SPI0_SCS active to first SPI0_CLK (7) (8) (9) | Polarity = 0, Phase = 0, to SPI0_CLK rising | 2P-2 | | 2P-2 | | 2P-3 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | 0.5M+2P-2 | | 0.5M+2P-2 | | 0.5M+2P-3 | | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK falling | 2P-2 | | 2P-2 | | 2P-3 | | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | 0.5M+2P-2 | | 0.5M+2P-2 | | 0.5M+2P-3 | | |
| 23 | $t_{d(ENA_SPC)M}$ | Delay from assertion of SPI0_ENA low to first SPI0_CLK edge. (10) | Polarity = 0, Phase = 0, to SPI0_CLK rising | | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI0_CLK rising | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| | | | Polarity = 1, Phase = 0, to SPI0_CLK falling | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | | Polarity = 1, Phase = 1, to SPI0_CLK falling | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |

(7) If SPI0_ENA is asserted immediately such that the transmission is not delayed by SPI0_ENA.
(8) In the case where the master SPI is ready with new data before SPI0_SCS assertion.
(9) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(10) If SPI0_ENA was initially deasserted high and SPI0_CLK is delayed.

**Table 5-75. Additional SPI0 Slave Timings, 4-Pin Enable Option (1)(2)(3)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 24 | $t_{d(SPC_ENAH)S}$ | Delay from final SPI0_CLK edge to slave deasserting SPI0_ENA. | Polarity = 0, Phase = 0, from SPI0_CLK falling | 1.5P-3 | 2.5P+17.5 | 1.5P-3 | 2.5P+20 | 1.5P-3 | 2.5P+27 | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK falling | – 0.5M+1.5P-3 | – 0.5M+2.5P+17.5 | – 0.5M+1.5P-3 | – 0.5M+2.5P+20 | – 0.5M+1.5P-3 | – 0.5M+2.5P+27 | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 1.5P-3 | 2.5P+17.5 | 1.5P-3 | 2.5P+20 | 1.5P-3 | 2.5P+27 | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK rising | – 0.5M+1.5P-3 | – 0.5+2.5P+17.5 | – 0.5M+1.5P-3 | – 0.5+2.5P+20 | – 0.5M+1.5P-3 | – 0.5+2.5P+27 | |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-71).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.


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### Table 5-76. Additional SPI0 Slave Timings, 4-Pin Chip Select Option (1)(2)(3)

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 25 | $t_{d(SCSL_SPC)S}$ | Required delay from $\overline{SPI0_SCS}$ asserted at slave to first SPI0_CLK edge at slave. | P + 1.5 | | P + 1.5 | | P + 1.5 | | ns |
| 26 | $t_{d(SPC_SCSH)S}$ | Required delay from final SPI0_CLK edge before $\overline{SPI0_SCS}$ is deasserted. Polarity = 0, Phase = 0, from SPI0_CLK falling | 0.5M+P+4 | | 0.5M+P+4 | | 0.5M+P+5 | | ns |
| | | Polarity = 0, Phase = 1, from SPI0_CLK falling | P+4 | | P+4 | | P+5 | | |
| | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 0.5M+P+4 | | 0.5M+P+4 | | 0.5M+P+5 | | |
| | | Polarity = 1, Phase = 1, from SPI0_CLK rising | P+4 | | P+4 | | P+5 | | |
| 27 | $t_{ena(SCSL_SOMI)S}$ | Delay from master asserting $\overline{SPI0_SCS}$ to slave driving SPI0_SOMI valid | | P+17.5 | | P+20 | | P+27 | ns |
| 28 | $t_{dis(SCSH_SOMI)S}$ | Delay from master deasserting $\overline{SPI0_SCS}$ to slave 3-stating SPI0_SOMI | | P+17.5 | | P+20 | | P+27 | ns |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-71).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

### Table 5-77. Additional SPI0 Slave Timings, 5-Pin Option (1)(2)(3)

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 25 | $t_{d(SCSL_SPC)S}$ | Required delay from $\overline{SPI0_SCS}$ asserted at slave to first SPI0_CLK edge at slave. | P + 1.5 | | P + 1.5 | | P + 1.5 | | ns |
| 26 | $t_{d(SPC_SCSH)S}$ | Required delay from final SPI0_CLK edge before $\overline{SPI0_SCS}$ is deasserted. Polarity = 0, Phase = 0, from SPI0_CLK falling | 0.5M+P+4 | | 0.5M+P+4 | | 0.5M+P+5 | | ns |
| | | Polarity = 0, Phase = 1, from SPI0_CLK falling | P+4 | | P+4 | | P+5 | | |
| | | Polarity = 1, Phase = 0, from SPI0_CLK rising | 0.5M+P+4 | | 0.5M+P+4 | | 0.5M+P+5 | | |
| | | Polarity = 1, Phase = 1, from SPI0_CLK rising | P+4 | | P+4 | | P+5 | | |
| 27 | $t_{ena(SCSL_SOMI)S}$ | Delay from master asserting $\overline{SPI0_SCS}$ to slave driving SPI0_SOMI valid | | P+17.5 | | P+20 | | P+27 | ns |
| 28 | $t_{dis(SCSH_SOMI)S}$ | Delay from master deasserting $\overline{SPI0_SCS}$ to slave 3-stating SPI0_SOMI | | P+17.5 | | P+20 | | P+27 | ns |
| 29 | $t_{ena(SCSL_ENA)S}$ | Delay from master deasserting $\overline{SPI0_SCS}$ to slave driving $\overline{SPI0_ENA}$ valid | | 17.5 | | 20 | | 27 | ns |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-71).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

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**Table 5-77. Additional SPI0 Slave Timings, 5-Pin Option (1)(2)(3) (continued)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 30 | $t_{dis(SPC_ENA)S}$ | Delay from final clock receive edge on SPI0_CLK to slave 3-stating or driving high $\overline{SPI0_ENA}$.(4) | Polarity = 0, Phase = 0, from SPI0_CLK falling | | 2.5P+17.5 | | 2.5P+20 | | 2.5P+27 | ns |
| | | | Polarity = 0, Phase = 1, from SPI0_CLK rising | | 2.5P+17.5 | | 2.5P+20 | | 2.5P+27 | |
| | | | Polarity = 1, Phase = 0, from SPI0_CLK rising | | 2.5P+17.5 | | 2.5P+20 | | 2.5P+27 | |
| | | | Polarity = 1, Phase = 1, from SPI0_CLK falling | | 2.5P+17.5 | | 2.5P+20 | | 2.5P+27 | |

(4) $\overline{SPI0_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.


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**Table 5-78. General Timing Requirements for SPI1 Master Modes(1)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SPC)M}$ | Cycle Time, SPI1_CLK, All Master Modes | | 20(2) | 256P | 30(2) | 256P | 40(2) | 256P | ns |
| 2 | $t_{w(SPCH)M}$ | Pulse Width High, SPI1_CLK, All Master Modes | | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | ns |
| 3 | $t_{w(SPCL)M}$ | Pulse Width Low, SPI1_CLK, All Master Modes | | 0.5M-1 | | 0.5M-1 | | 0.5M-1 | | ns |
| 4 | $t_{d(SIMO_SPC)M}$ | Delay, initial data bit valid on SPI1_SIMO to initial edge on SPI1_CLK(3) | Polarity = 0, Phase = 0, to SPI1_CLK rising | | 5 | | 5 | | 6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | | -0.5M+5 | | -0.5M+5 | | -0.5M+6 | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | | -0.5M+5 | | -0.5M+5 | | -0.5M+6 | |
| 5 | $t_{d(SPC_SIMO)M}$ | Delay, subsequent bits valid on SPI1_SIMO after transmit edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK rising | | 5 | | 5 | | 6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK falling | | 5 | | 5 | | 6 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | 5 | | 5 | | 6 | |
| 6 | $t_{oh(SPC_SIMO)M}$ | Output hold time, SPI1_SIMO valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 0.5M-3 | | 0.5M-3 | | 0.5M-3 | | |
| 7 | $t_{su(SOMI_SPC)M}$ | Input Setup Time, SPI1_SOMI valid before receive edge of SPI1_CLK | Polarity = 0, Phase = 0, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | |
| 8 | $t_{ih(SPC_SOMI)M}$ | Input Hold Time, SPI1_SOMI valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 4 | | 5 | | 6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 4 | | 5 | | 6 | | |

(1) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(2) This timing is limited by the timing shown or 3P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. MO(0) refers to first bit and MO(n) refers to last bit output on SPI1_SIMO. MI(0) refers to the first bit input and MI(n) refers to the last bit input on SPI1_SOMI.

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**Table 5-79. General Timing Requirements for SPI1 Slave Modes(1)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 9 | $t_{c(SPC)S}$ | Cycle Time, SPI1_CLK, All Slave Modes | | 40(2) | | 50(2) | | 60(2) | | ns |
| 10 | $t_{w(SPCH)S}$ | Pulse Width High, SPI1_CLK, All Slave Modes | | 18 | | 22 | | 27 | | ns |
| 11 | $t_{w(SPCL)S}$ | Pulse Width Low, SPI1_CLK, All Slave Modes | | 18 | | 22 | | 27 | | ns |
| 12 | $t_{su(SOMI_SPC)S}$ | Setup time, transmit data written to SPI before initial clock edge from master.(3)(4) | Polarity = 0, Phase = 0, to SPI1_CLK rising | 2P | | 2P | | 2P | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 2P | | 2P | | 2P | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | 2P | | 2P | | 2P | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 2P | | 2P | | 2P | | |
| 13 | $t_{d(SPC_SOMI)S}$ | Delay, subsequent bits valid on SPI1_SOMI after transmit edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK rising | | 15 | | 17 | | 19 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | 15 | | 17 | | 19 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK falling | | 15 | | 17 | | 19 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | 15 | | 17 | | 19 | |
| 14 | $t_{oh(SPC_SOMI)S}$ | Output hold time, SPI1_SOMI valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 0.5S-4 | | 0.5S-10 | | 0.5S-12 | | |
| 15 | $t_{su(SIMO_SPC)S}$ | Input Setup Time, SPI1_SIMO valid before receive edge of SPI1_CLK | Polarity = 0, Phase = 0, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK rising | 1.5 | | 1.5 | | 1.5 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 1.5 | | 1.5 | | 1.5 | | |
| 16 | $t_{ih(SPC_SIMO)S}$ | Input Hold Time, SPI1_SIMO valid after receive edge of SPI1_CLK | Polarity = 0, Phase = 0, from SPI1_CLK falling | 4 | | 5 | | 6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 4 | | 5 | | 6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK falling | 4 | | 5 | | 6 | | |

(1) P = SYSCLK2 period; S = $t_{c(SPC)S}$ (SPI slave bit clock period)
(2) This timing is limited by the timing shown or 3P, whichever is greater.
(3) First bit may be MSB or LSB depending upon SPI configuration. SO(0) refers to first bit and SO(n) refers to last bit output on SPI1_SOMI. SI(0) refers to the first bit input and SI(n) refers to the last bit input on SPI1_SIMO.
(4) Measured from the termination of the write of new data to the SPI module, In analyzing throughput requirements, additional internal bus cycles must be accounted for to allow data to be written to the SPI module by the CPU.


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**Table 5-80. Additional[1] SPI1 Master Timings, 4-Pin Enable Option[2][3]**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 17 | $t_{d(EN\ A_SPC)M}$ | Delay from slave assertion of SPI1_ENA active to first SPI1_CLK from master.[4] | Polarity = 0, Phase = 0, to SPI1_CLK rising | | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| 18 | $t_{d(SPC_ENA)M}$ | Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[5] | Polarity = 0, Phase = 0, from SPI1_CLK falling | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | P+5 | | P+5 | | P+6 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | P+5 | | P+5 | | P+6 | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-78).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_ENA assertion.
(5) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.

**Table 5-81. Additional[1] SPI1 Master Timings, 4-Pin Chip Select Option[2] [3]**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 19 | $t_{d(SCS_SPC)M}$ | Delay from SPI1_SCS active to first SPI1_CLK[4] [5] | Polarity = 0, Phase = 0, to SPI1_CLK rising | 2P-1 | | 2P-5 | | 2P-6 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | 2P-1 | | 2P-5 | | 2P-6 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |
| 20 | $t_{d(SPC_SCS)M}$ | Delay from final SPI1_CLK edge to master deasserting SPI1_SCS[6] [7] | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P-1 | | P-5 | | P-6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P-1 | | P-5 | | P-6 | | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-78).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_SCS assertion.
(5) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].
(6) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(7) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].

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**Table 5-82. Additional[1] SPI1 Master Timings, 5-Pin Option[2][3]**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 18 | $t_{d(SPC_ENA)M}$ | Max delay for slave to deassert SPI1_ENA after final SPI1_CLK edge to ensure master does not begin the next transfer.[4] | Polarity = 0, Phase = 0, from SPI1_CLK falling | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | | P+5 | | P+5 | | P+6 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | | 0.5M+P+5 | | 0.5M+P+5 | | 0.5M+P+6 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | | P+5 | | P+5 | | P+6 | |
| 20 | $t_{d(SPC_SCS)M}$ | Delay from final SPI1_CLK edge to master deasserting SPI1_SCS [5][6] | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P-1 | | P-5 | | P-6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P-1 | | 0.5M+P-5 | | 0.5M+P-6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P-1 | | P-5 | | P-6 | | |
| 21 | $t_{d(SCSL_ENAL)M}$ | Max delay for slave SPI to drive SPI1_ENA valid after master asserts SPI1_SCS to delay the master from beginning the next transfer, | | | C2TDELAY+P | | C2TDELAY+P | | C2TDELAY+P | ns |
| 22 | $t_{d(SCS_SPC)M}$ | Delay from SPI1_SCS active to first SPI1_CLK[7][8][9] | Polarity = 0, Phase = 0, to SPI1_CLK rising | 2P-1 | | 2P-5 | | 2P-6 | | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | 2P-1 | | 2P-5 | | 2P-6 | | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | 0.5M+2P-1 | | 0.5M+2P-5 | | 0.5M+2P-6 | | |

(1) These parameters are in addition to the general timings for SPI master modes (Table 5-79).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four master clocking modes.
(4) In the case where the master SPI is ready with new data before SPI1_ENA deassertion.
(5) Except for modes when SPIDAT1.CSHOLD is enabled and there is additional data to transmit. In this case, SPI1_SCS will remain asserted.
(6) This delay can be increased under software control by the register bit field SPIDELAY.T2CDELAY[4:0].
(7) If SPI1_ENA is asserted immediately such that the transmission is not delayed by SPI1_ENA.
(8) In the case where the master SPI is ready with new data before SPI1_SCS assertion.
(9) This delay can be increased under software control by the register bit field SPIDELAY.C2TDELAY[4:0].


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**Table 5-82. Additional[1] SPI1 Master Timings, 5-Pin Option[2][3] (continued)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 23 | $t_{d(ENA_SPC)M}$ | Delay from assertion of $\overline{SPI1_ENA}$ low to first SPI1_CLK edge.[10] | Polarity = 0, Phase = 0, to SPI1_CLK rising | | 3P+5 | | 3P+5 | | 3P+6 | ns |
| | | | Polarity = 0, Phase = 1, to SPI1_CLK rising | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |
| | | | Polarity = 1, Phase = 0, to SPI1_CLK falling | | 3P+5 | | 3P+5 | | 3P+6 | |
| | | | Polarity = 1, Phase = 1, to SPI1_CLK falling | | 0.5M+3P+5 | | 0.5M+3P+5 | | 0.5M+3P+6 | |

(10) If $\overline{SPI1_ENA}$ was initially deasserted high and SPI1_CLK is delayed.

**Table 5-83. Additional[1] SPI1 Slave Timings, 4-Pin Enable Option[2][3]**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 24 | $t_{d(SPC_ENAH)S}$ | Delay from final SPI1_CLK edge to slave deasserting $\overline{SPI1_ENA}$. | Polarity = 0, Phase = 0, from SPI1_CLK falling | 1.5P-3 | 2.5P+15 | 1.5P-10 | 2.5P+17 | 1.5P-12 | 2.5P+19 | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | –0.5M+1.5P-3 | –0.5M+2.5P+15 | –0.5M+1.5P-10 | –0.5M+2.5P+17 | –0.5M+1.5P-12 | –0.5M+2.5P+19 | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 1.5P-3 | 2.5P+15 | 1.5P-10 | 2.5P+17 | 1.5P-12 | 2.5P+19 | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | –0.5M+1.5P-3 | –0.5M+2.5P+15 | –0.5M+1.5P-10 | –0.5M+2.5P+17 | –0.5M+1.5P-12 | –0.5M+2.5P+19 | |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-79).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

**Table 5-84. Additional[1] SPI1 Slave Timings, 4-Pin Chip Select Option[2][3]**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 25 | $t_{d(SCSL_SPC)S}$ | Required delay from $\overline{SPI1_SCS}$ asserted at slave to first SPI1_CLK edge at slave. | P+1.5 | | P+1.5 | | P+1.5 | | ns |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-79).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.

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**Table 5-84. Additional[1] SPI1 Slave Timings, 4-Pin Chip Select Option[2][3] (continued)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 26 | $t_{d(SPC_SCSH)S}$ | Required delay from final SPI1_CLK edge before $\overline{SPI1_SCS}$ is deasserted. | Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | ns |
| | | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P+4 | | P+5 | | P+6 | | |
| | | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | |
| | | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P+4 | | P+5 | | P+6 | | |
| 27 | $t_{ena(SCSL_SOMI)S}$ | Delay from master asserting $\overline{SPI1_SCS}$ to slave driving SPI1_SOMI valid | | | P+15 | | P+17 | | P+19 | ns |
| 28 | $t_{dis(SCSH_SOMI)S}$ | Delay from master deasserting $\overline{SPI1_SCS}$ to slave 3-stating SPI1_SOMI | | | P+15 | | P+17 | | P+19 | ns |


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**Table 5-85. Additional[1] SPI1 Slave Timings, 5-Pin Option[2][3]**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 25 | $t_{d(SCSL_SPC)S}$ | Required delay from $\overline{SPI1_SCS}$ asserted at slave to first SPI1_CLK edge at slave. | P+1.5 | | P+1.5 | | P+1.5 | | ns |
| 26 | $t_{d(SPC_SCSH)S}$ | Required delay from final SPI1_CLK edge before $\overline{SPI1_SCS}$ is deasserted. Polarity = 0, Phase = 0, from SPI1_CLK falling | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | ns |
| | | Polarity = 0, Phase = 1, from SPI1_CLK falling | P+4 | | P+5 | | P+6 | | |
| | | Polarity = 1, Phase = 0, from SPI1_CLK rising | 0.5M+P+4 | | 0.5M+P+5 | | 0.5M+P+6 | | |
| | | Polarity = 1, Phase = 1, from SPI1_CLK rising | P+4 | | P+5 | | P+6 | | |
| 27 | $t_{ena(SCSL_SOMI)S}$ | Delay from master asserting $\overline{SPI1_SCS}$ to slave driving SPI1_SOMI valid | | P+15 | | P+17 | | P+19 | ns |
| 28 | $t_{dis(SCSH_SOMI)S}$ | Delay from master deasserting $\overline{SPI1_SCS}$ to slave 3-stating SPI1_SOMI | | P+15 | | P+17 | | P+19 | ns |
| 29 | $t_{ena(SCSL_ENA)S}$ | Delay from master deasserting $\overline{SPI1_SCS}$ to slave driving $\overline{SPI1_ENA}$ valid | | 15 | | 17 | | 19 | ns |
| 30 | $t_{dis(SPC_ENA)S}$ | Delay from final clock receive edge on SPI1_CLK to slave 3-stating or driving high $\overline{SPI1_ENA}$.[4] Polarity = 0, Phase = 0, from SPI1_CLK falling | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | ns |
| | | Polarity = 0, Phase = 1, from SPI1_CLK rising | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | |
| | | Polarity = 1, Phase = 0, from SPI1_CLK rising | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | |
| | | Polarity = 1, Phase = 1, from SPI1_CLK falling | | 2.5P+15 | | 2.5P+17 | | 2.5P+19 | |

(1) These parameters are in addition to the general timings for SPI slave modes (Table 5-79).
(2) P = SYSCLK2 period; M = $t_{c(SPC)M}$ (SPI master bit clock period)
(3) Figure shows only Polarity = 0, Phase = 0 as an example. Table gives parameters for all four slave clocking modes.
(4) $\overline{SPI1_ENA}$ is driven low after the transmission completes if the SPIINT0.ENABLE_HIGHZ bit is programmed to 0. Otherwise it is tri-stated. If tri-stated, an external pullup resistor should be used to provide a valid level to the master. This option is useful when tying several SPI slave devices to a single master.


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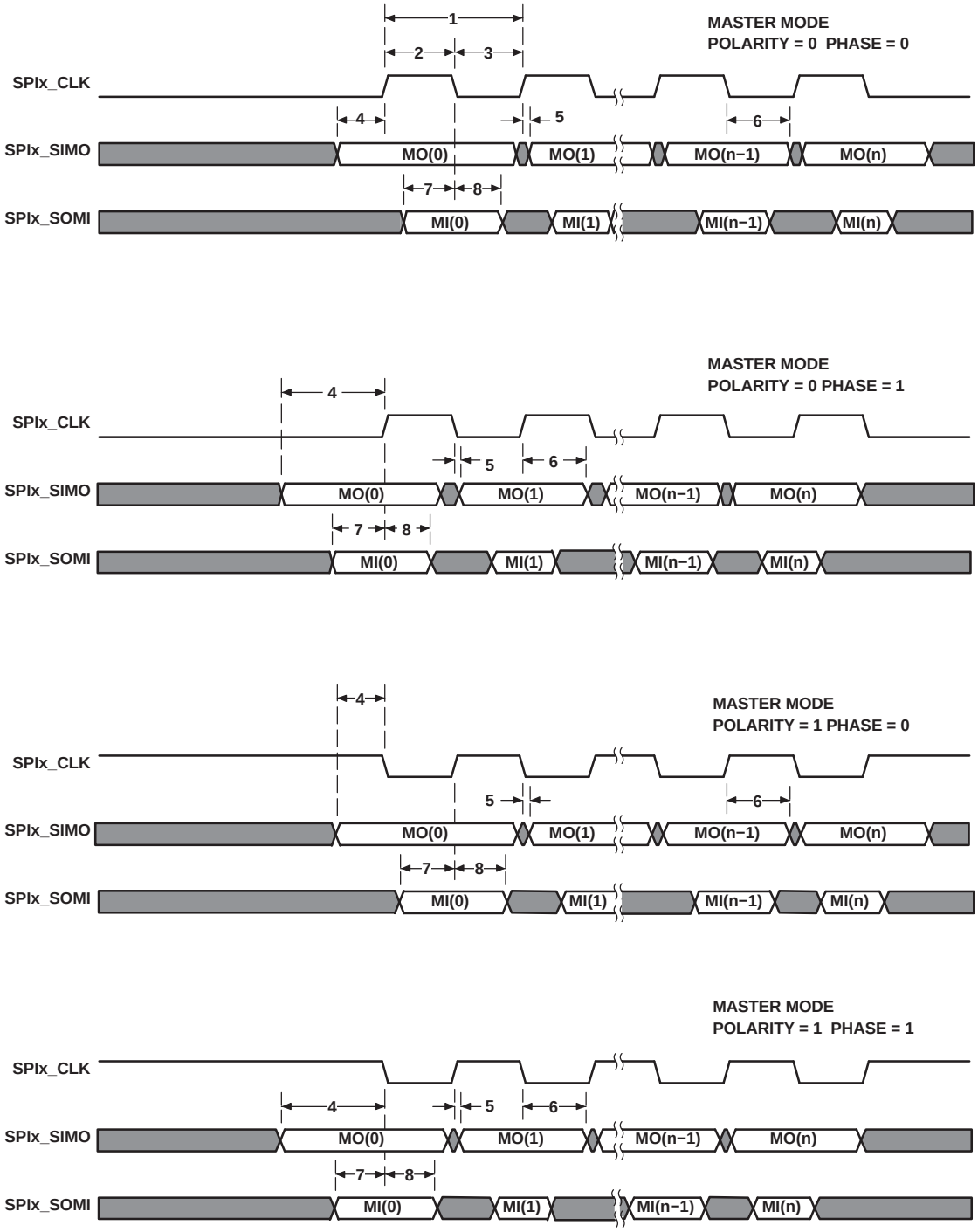


**Figure 5-38. SPI Timings—Master Mode**

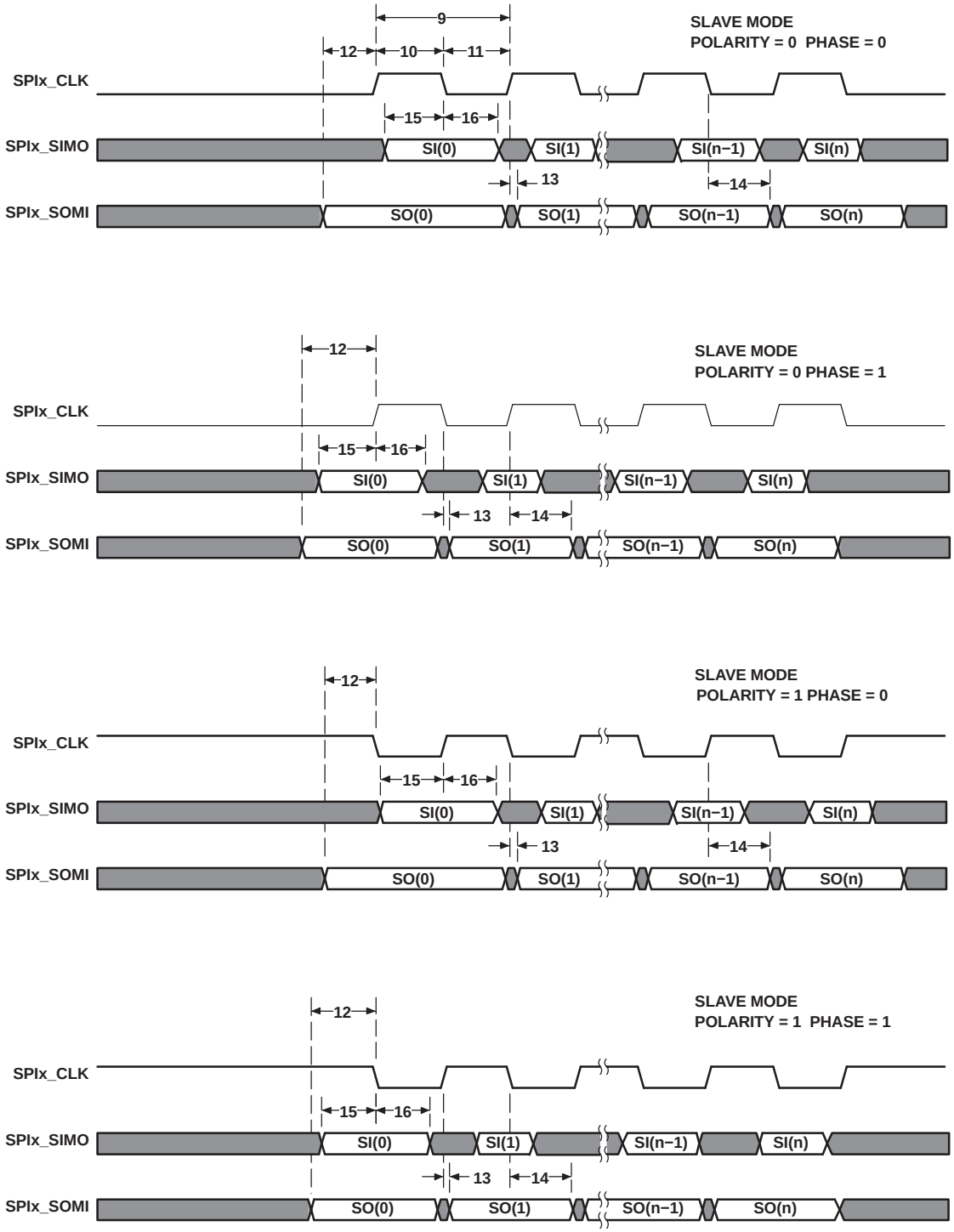


**Figure 5-39. SPI Timings—Slave Mode**


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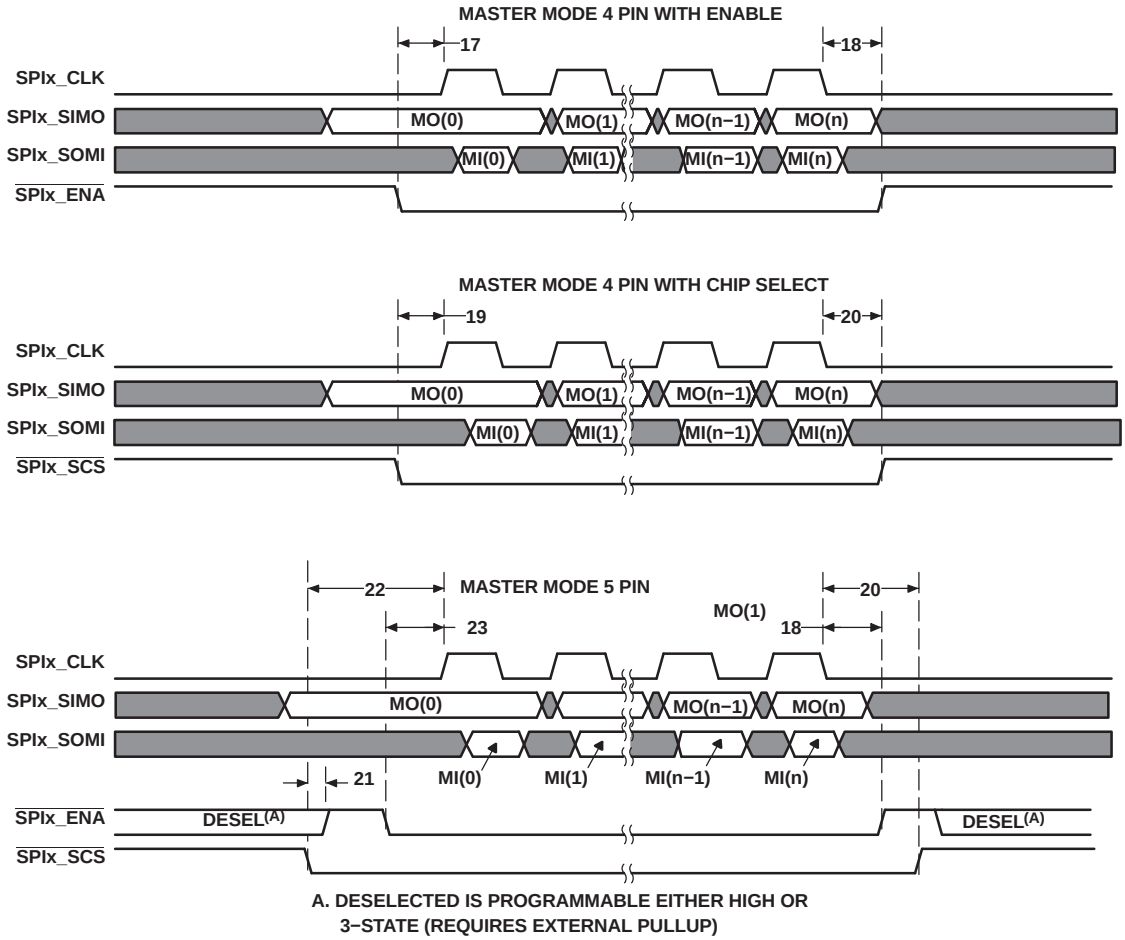


**Figure 5-40. SPI Timings—Master Mode (4-Pin and 5-Pin)**

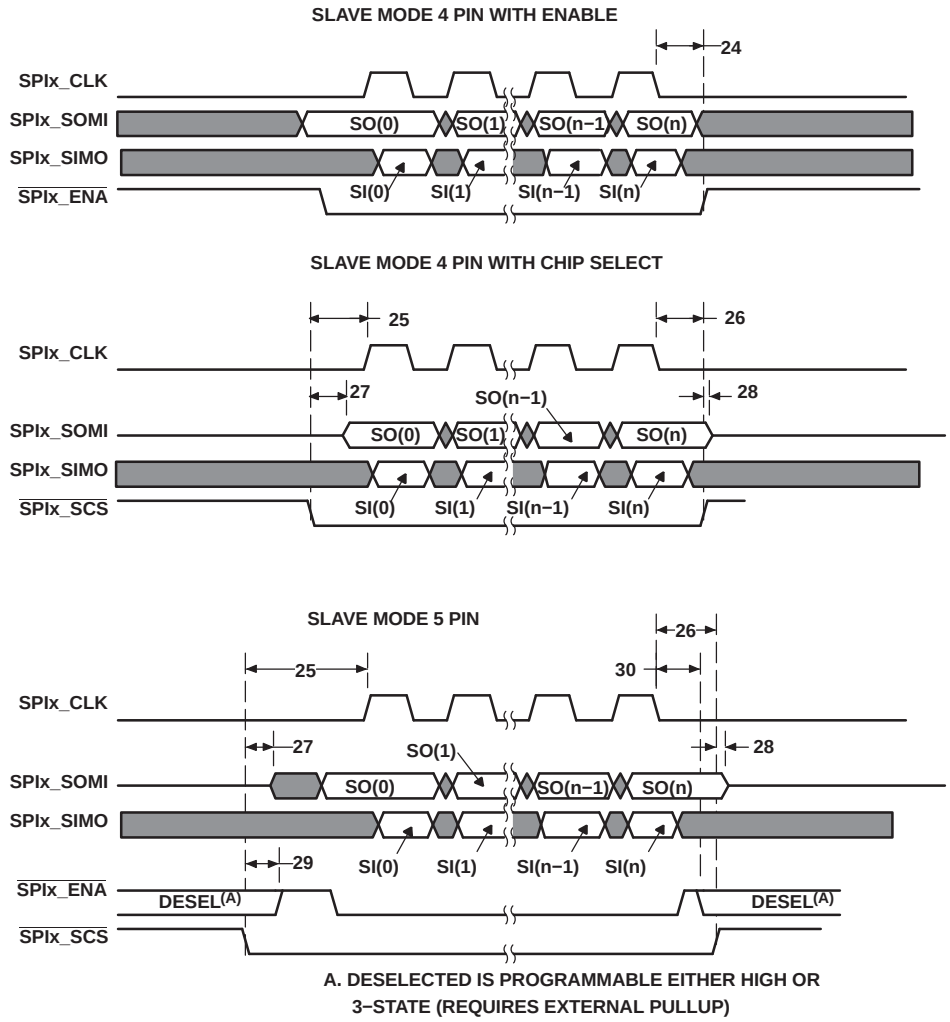


**Figure 5-41. SPI Timings—Slave Mode (4-Pin and 5-Pin)**


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## 5.18 Inter-Integrated Circuit Serial Ports (I2C)

### 5.18.1 I2C Device-Specific Information

Each I2C port supports:

- Compatible with Philips® I2C Specification Revision 2.1 (January 2000)
- Fast Mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise Filter to Remove Noise 50 ns or less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- Events: DMA, Interrupt, or Polling
- General-Purpose I/O Capability if not used as I2C

Figure 5-42 is block diagram of the device I2C Module.

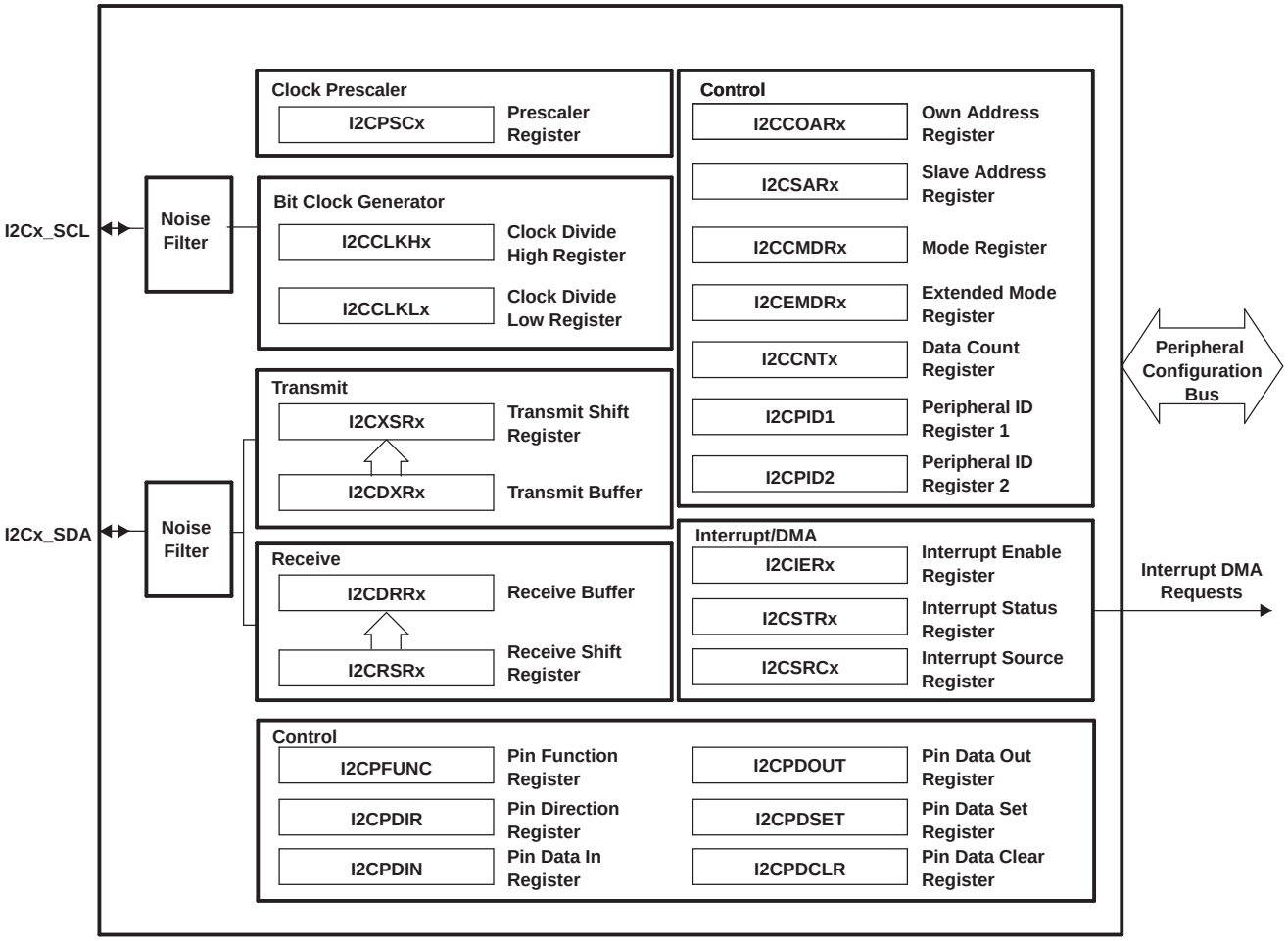


**Figure 5-42. I2C Module Block Diagram**

### 5.18.2 I2C Peripheral Registers Description(s)

Table 5-86 is the list of the I2C registers.

**Table 5-86. Inter-Integrated Circuit (I2C) Registers**

| I2C0 BYTE ADDRESS | I2C1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C2 2000 | 0x01E2 8000 | ICOAR | I2C Own Address Register |
| 0x01C2 2004 | 0x01E2 8004 | ICIMR | I2C Interrupt Mask Register |
| 0x01C2 2008 | 0x01E2 8008 | ICSTR | I2C Interrupt Status Register |
| 0x01C2 200C | 0x01E2 800C | ICCLKL | I2C Clock Low-Time Divider Register |
| 0x01C2 2010 | 0x01E2 8010 | ICCLKH | I2C Clock High-Time Divider Register |
| 0x01C2 2014 | 0x01E2 8014 | ICCNT | I2C Data Count Register |
| 0x01C2 2018 | 0x01E2 8018 | ICDRR | I2C Data Receive Register |
| 0x01C2 201C | 0x01E2 801C | ICSAR | I2C Slave Address Register |
| 0x01C2 2020 | 0x01E2 8020 | ICDXR | I2C Data Transmit Register |
| 0x01C2 2024 | 0x01E2 8024 | ICMDR | I2C Mode Register |
| 0x01C2 2028 | 0x01E2 8028 | ICIVR | I2C Interrupt Vector Register |
| 0x01C2 202C | 0x01E2 802C | ICEMDR | I2C Extended Mode Register |
| 0x01C2 2030 | 0x01E2 8030 | ICPSC | I2C Prescaler Register |
| 0x01C2 2034 | 0x01E2 8034 | REVID1 | I2C Revision Identification Register 1 |
| 0x01C2 2038 | 0x01E2 8038 | REVID2 | I2C Revision Identification Register 2 |
| 0x01C2 2048 | 0x01E2 8048 | ICPFUNC | I2C Pin Function Register |
| 0x01C2 204C | 0x01E2 804C | ICPDIR | I2C Pin Direction Register |
| 0x01C2 2050 | 0x01E2 8050 | ICPDIN | I2C Pin Data In Register |
| 0x01C2 2054 | 0x01E2 8054 | ICPDOUT | I2C Pin Data Out Register |
| 0x01C2 2058 | 0x01E2 8058 | ICPDSET | I2C Pin Data Set Register |
| 0x01C2 205C | 0x01E2 805C | ICPDCLR | I2C Pin Data Clear Register |


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## 5.18.3 I2C Electrical Data/Timing

### 5.18.3.1 Inter-Integrated Circuit (I2C) Timing

Table 5-87 and Table 5-88 assume testing over recommended operating conditions (see Figure 5-43 and Figure 5-44).

**Table 5-87. Timing Requirements for I2C Input**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(SCL)}$ | Cycle time, I2Cx_SCL | 10 | | 2.5 | | µs |
| 2 | $t_{su(SCLH-SDAL)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA low | 4.7 | | 0.6 | | µs |
| 3 | $t_{h(SCLL-SDAL)}$ | Hold time, I2Cx_SCL low after I2Cx_SDA low | 4 | | 0.6 | | µs |
| 4 | $t_{w(SCLL)}$ | Pulse duration, I2Cx_SCL low | 4.7 | | 1.3 | | µs |
| 5 | $t_{w(SCLH)}$ | Pulse duration, I2Cx_SCL high | 4 | | 0.6 | | µs |
| 6 | $t_{su(SDA-SCLH)}$ | Setup time, I2Cx_SDA before I2Cx_SCL high | 250 | | 100 | | ns |
| 7 | $t_{h(SDA-SCLL)}$ | Hold time, I2Cx_SDA after I2Cx_SCL low | 0 | | 0 | 0.9 | µs |
| 8 | $t_{w(SDAH)}$ | Pulse duration, I2Cx_SDA high | 4.7 | | 1.3 | | µs |
| 9 | $t_{r(SDA)}$ | Rise time, I2Cx_SDA | | 1000 | $20 + 0.1C_b$ | 300 | ns |
| 10 | $t_{r(SCL)}$ | Rise time, I2Cx_SCL | | 1000 | $20 + 0.1C_b$ | 300 | ns |
| 11 | $t_{f(SDA)}$ | Fall time, I2Cx_SDA | | 300 | $20 + 0.1C_b$ | 300 | ns |
| 12 | $t_{f(SCL)}$ | Fall time, I2Cx_SCL | | 300 | $20 + 0.1C_b$ | 300 | ns |
| 13 | $t_{su(SCLH-SDAH)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA high | 4 | | 0.6 | | µs |
| 14 | $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | N/A | | 0 | 50 | ns |
| 15 | $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

**Table 5-88. Switching Characteristics for I2C (1)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN | MAX | MIN | MAX | |
| 16 | $t_{c(SCL)}$ | Cycle time, I2Cx_SCL | 10 | | 2.5 | | µs |
| 17 | $t_{su(SCLH-SDAL)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA low | 4.7 | | 0.6 | | µs |
| 18 | $t_{h(SDAL-SCLL)}$ | Hold time, I2Cx_SCL low after I2Cx_SDA low | 4 | | 0.6 | | µs |
| 19 | $t_{w(SCLL)}$ | Pulse duration, I2Cx_SCL low | 4.7 | | 1.3 | | µs |
| 20 | $t_{w(SCLH)}$ | Pulse duration, I2Cx_SCL high | 4 | | 0.6 | | µs |
| 21 | $t_{su(SDAV-SCLH)}$ | Setup time, I2Cx_SDA valid before I2Cx_SCL high | 250 | | 100 | | ns |
| 22 | $t_{h(SCLL-SDAV)}$ | Hold time, I2Cx_SDA valid after I2Cx_SCL low | 0 | | 0 | 0.9 | µs |
| 23 | $t_{w(SDAH)}$ | Pulse duration, I2Cx_SDA high | 4.7 | | 1.3 | | µs |
| 28 | $t_{su(SCLH-SDAH)}$ | Setup time, I2Cx_SCL high before I2Cx_SDA high | 4 | | 0.6 | | µs |

(1) I2C must be configured correctly to meet the timings in Table 5-88.

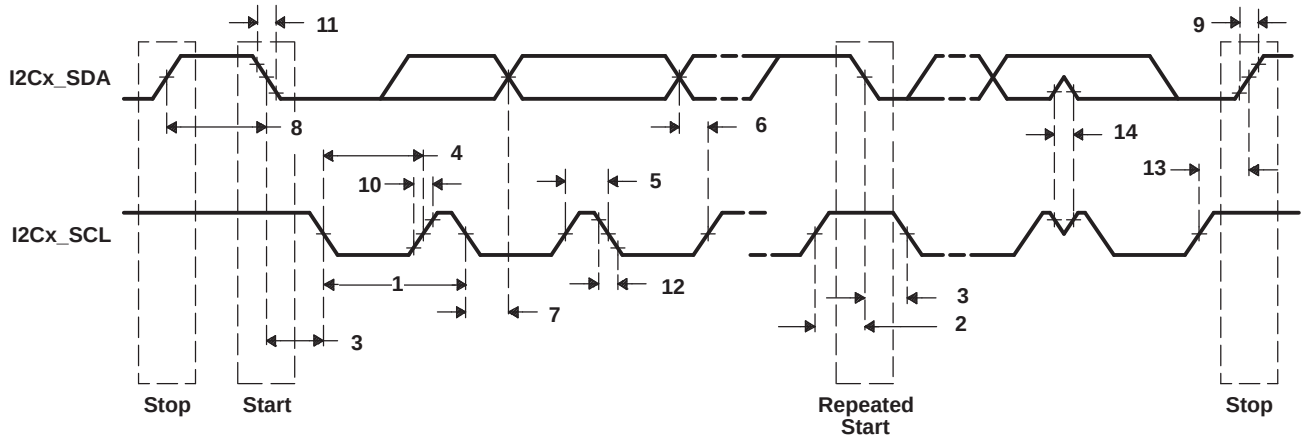


**Figure 5-43. I2C Receive Timings**

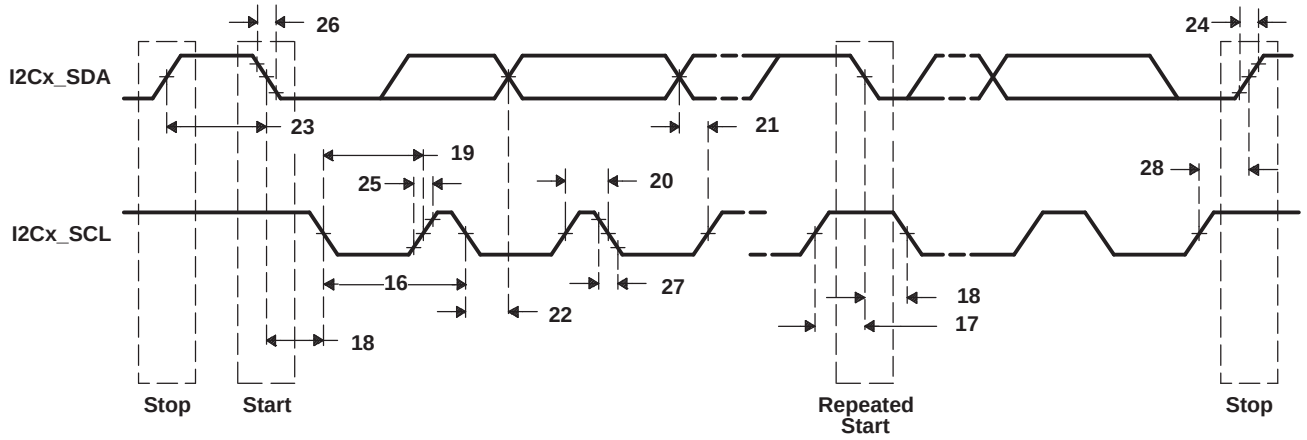


**Figure 5-44. I2C Transmit Timings**


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## 5.19 Universal Asynchronous Receiver/Transmitter (UART)

Each UART has the following features:

- 16-byte storage space for both the transmitter and receiver FIFOs
- 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- Programmable auto-rts and auto-cts for autoflow control
- Programmable Baud Rate up to 12 MBaud
- Programmable Oversampling Options of x13 and x16
- Frequency pre-scale values from 1 to 65,535 to generate appropriate baud rates
- Prioritized interrupts
- Programmable serial data formats
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no parity bit generation and detection
  - 1, 1.5, or 2 stop bit generation
- False start bit detection
- Line break generation and detection
- Internal diagnostic capabilities
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, and framing error simulation
- Modem control functions (CTS, RTS)

The UART registers are listed in Section 5.19.1

### *5.19.1 UART Peripheral Registers Description(s)*

Table 5-89 is the list of UART registers.

**Table 5-89. UART Registers**

| UART0 BYTE ADDRESS | UART1 BYTE ADDRESS | UART2 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|---|
| 0x01C4 2000 | 0x01D0 C000 | 0x01D0 D000 | RBR | Receiver Buffer Register (read only) |
| 0x01C4 2000 | 0x01D0 C000 | 0x01D0 D000 | THR | Transmitter Holding Register (write only) |
| 0x01C4 2004 | 0x01D0 C004 | 0x01D0 D004 | IER | Interrupt Enable Register |
| 0x01C4 2008 | 0x01D0 C008 | 0x01D0 D008 | IIR | Interrupt Identification Register (read only) |
| 0x01C4 2008 | 0x01D0 C008 | 0x01D0 D008 | FCR | FIFO Control Register (write only) |
| 0x01C4 200C | 0x01D0 C00C | 0x01D0 D00C | LCR | Line Control Register |
| 0x01C4 2010 | 0x01D0 C010 | 0x01D0 D010 | MCR | Modem Control Register |
| 0x01C4 2014 | 0x01D0 C014 | 0x01D0 D014 | LSR | Line Status Register |
| 0x01C4 2018 | 0x01D0 C018 | 0x01D0 D018 | MSR | Modem Status Register |
| 0x01C4 201C | 0x01D0 C01C | 0x01D0 D01C | SCR | Scratchpad Register |
| 0x01C4 2020 | 0x01D0 C020 | 0x01D0 D020 | DLL | Divisor LSB Latch |
| 0x01C4 2024 | 0x01D0 C024 | 0x01D0 D024 | DLH | Divisor MSB Latch |
| 0x01C4 2028 | 0x01D0 C028 | 0x01D0 D028 | REVID1 | Revision Identification Register 1 |
| 0x01C4 2030 | 0x01D0 C030 | 0x01D0 D030 | PWREMU_MGMT | Power and Emulation Management Register |
| 0x01C4 2034 | 0x01D0 C034 | 0x01D0 D034 | MDR | Mode Definition Register |

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### 5.19.2 UART Electrical Data/Timing

**Table 5-90. Timing Requirements for UART Receive(1) (see Figure 5-45)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 4 | $t_{w(URXDB)}$ | Pulse duration, receive data bit (RXDn) | 0.96U | 1.05U | ns |
| 5 | $t_{w(URXSB)}$ | Pulse duration, receive start bit | 0.96U | 1.05U | ns |

(1) U = UART baud time = 1/programmed baud rate.

**Table 5-91. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit(1) (see Figure 5-45)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $f_{(baud)}$ | Maximum programmable baud rate | | D/E (2) (3) | MBaud (4) |
| 2 | $t_{w(UTXDB)}$ | Pulse duration, transmit data bit (TXDn) | U - 2 | U + 2 | ns |
| 3 | $t_{w(UTXSB)}$ | Pulse duration, transmit start bit | U - 2 | U + 2 | ns |

(1) U = UART baud time = 1/programmed baud rate.
(2) D = UART input clock in MHz.
For UART0, the UART input clock is SYSCLK2.
For UART1 or UART2, the UART input clock is ASYNC3 (either PLL0_SYCLK2 or PLL1_SYSCLK2).
(3) E = UART divisor x UART sampling rate. The UART divisor is set through the UART divisor latch registers (DLL and DLH). The UART sampling rate is set through the over-sampling mode select bit (OSM_SEL) of the UART mode definition register (MDR).
(4) Baud rate is not indicative of data rate. Actual data rate will be limited by system factors such as EDMA loading, EMIF/DDR loading, system frequency, etc.

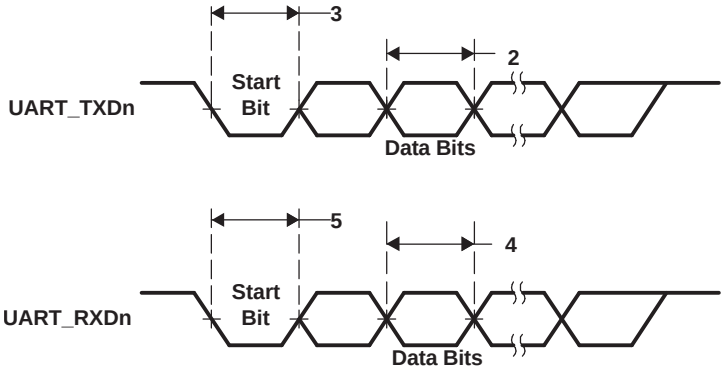


**Figure 5-45. UART Transmit/Receive Timing**


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## 5.20 Universal Serial Bus OTG Controller (USB0) [USB2.0 OTG]

The USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high speed (HS: 480 Mb/s) and full speed (FS: 12 Mb/s)
- USB 2.0 host at speeds HS, FS, and low speed (LS: 1.5 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous)
- 4 Transmit (TX) and 4 Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 4K endpoint
  - Programmable size
- Integrated USB 2.0 High Speed PHY
- Connects to a standard Charge Pump for VBUS 5 V generation
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

**Important Notice:** The USB0 controller module clock (PLL0_SYSCLK2) must be greater than 30 MHz for proper operation of the USB controller. A clock rate of 60 MHz or greater is recommended to avoid data throughput reduction.

Table 5-92 is the list of USB OTG registers.

**Table 5-92. Universal Serial Bus OTG (USB0) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E0 0000 | REVID | Revision Register |
| 0x01E0 0004 | CTRLR | Control Register |
| 0x01E0 0008 | STATR | Status Register |
| 0x01E0 000C | EMUR | Emulation Register |
| 0x01E0 0010 | MODE | Mode Register |
| 0x01E0 0014 | AUTOREQ | Autorequest Register |
| 0x01E0 0018 | SRPFIXTIME | SRP Fix Time Register |
| 0x01E0 001C | TEARDOWN | Teardown Register |
| 0x01E0 0020 | INTSRCR | USB Interrupt Source Register |
| 0x01E0 0024 | INTSETR | USB Interrupt Source Set Register |
| 0x01E0 0028 | INTCLRR | USB Interrupt Source Clear Register |
| 0x01E0 002C | INTMSKR | USB Interrupt Mask Register |
| 0x01E0 0030 | INTMSKSETR | USB Interrupt Mask Set Register |
| 0x01E0 0034 | INTMSKCLRR | USB Interrupt Mask Clear Register |
| 0x01E0 0038 | INTMASKEDR | USB Interrupt Source Masked Register |
| 0x01E0 003C | EOIR | USB End of Interrupt Register |
| 0x01E0 0040 | - | Reserved |
| 0x01E0 0050 | GENRNDISSZ1 | Generic RNDIS Size EP1 |
| 0x01E0 0054 | GENRNDISSZ2 | Generic RNDIS Size EP2 |
| 0x01E0 0058 | GENRNDISSZ3 | Generic RNDIS Size EP3 |
| 0x01E0 005C | GENRNDISSZ4 | Generic RNDIS Size EP4 |
| 0x01E0 0400 | FADDR | Function Address Register |
| 0x01E0 0401 | POWER | Power Management Register |
| 0x01E0 0402 | INTRTX | Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4 |
| 0x01E0 0404 | INTRRX | Interrupt Register for Receive Endpoints 1 to 4 |
| 0x01E0 0406 | INTRTXE | Interrupt enable register for INTRTX |
| 0x01E0 0408 | INTRRXE | Interrupt Enable Register for INTRRX |
| 0x01E0 040A | INTRUSB | Interrupt Register for Common USB Interrupts |
| 0x01E0 040B | INTRUSBE | Interrupt Enable Register for INTRUSB |

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**Table 5-92. Universal Serial Bus OTG (USB0) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E0 040C | FRAME | Frame Number Register |
| 0x01E0 040E | INDEX | Index Register for Selecting the Endpoint Status and Control Registers |
| 0x01E0 040F | TESTMODE | Register to Enable the USB 2.0 Test Modes |
| **Indexed Registers**<br>These registers operate on the endpoint selected by the INDEX register | | |
| 0x01E0 0410 | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint<br>(Index register set to select Endpoints 1-4 only) |
| 0x01E0 0412 | PERI_CSR0 | Control Status Register for Endpoint 0 in Peripheral Mode.<br>(Index register set to select Endpoint 0) |
| | HOST_CSR0 | Control Status Register for Endpoint 0 in Host Mode.<br>(Index register set to select Endpoint 0) |
| | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint.<br>(Index register set to select Endpoints 1-4) |
| | HOST_TXCSR | Control Status Register for Host Transmit Endpoint.<br>(Index register set to select Endpoints 1-4) |
| 0x01E0 0414 | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint<br>(Index register set to select Endpoints 1-4 only) |
| 0x01E0 0416 | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint.<br>(Index register set to select Endpoints 1-4) |
| | HOST_RXCSR | Control Status Register for Host Receive Endpoint.<br>(Index register set to select Endpoints 1-4) |
| 0x01E0 0418 | COUNT0 | Number of Received Bytes in Endpoint 0 FIFO.<br>(Index register set to select Endpoint 0) |
| | RXCOUNT | Number of Bytes in Host Receive Endpoint FIFO.<br>(Index register set to select Endpoints 1- 4) |
| 0x01E0 041A | HOST_TYPE0 | Defines the speed of Endpoint 0 |
| | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint. (Index register set to select Endpoints 1-4 only) |
| 0x01E0 041B | HOST_NAKLIMIT0 | Sets the NAK response timeout on Endpoint 0.<br>(Index register set to select Endpoint 0) |
| | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint. (Index register set to select Endpoints 1-4 only) |
| 0x01E0 041C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint. (Index register set to select Endpoints 1-4 only) |
| 0x01E0 041D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint. (Index register set to select Endpoints 1-4 only) |
| 0x01E0 041F | CONFIGDATA | Returns details of core configuration. (Index register set to select Endpoint 0) |
| **FIFO** | | |
| 0x01E0 0420 | FIFO0 | Transmit and Receive FIFO Register for Endpoint 0 |
| 0x01E0 0424 | FIFO1 | Transmit and Receive FIFO Register for Endpoint 1 |
| 0x01E0 0428 | FIFO2 | Transmit and Receive FIFO Register for Endpoint 2 |
| 0x01E0 042C | FIFO3 | Transmit and Receive FIFO Register for Endpoint 3 |
| 0x01E0 0430 | FIFO4 | Transmit and Receive FIFO Register for Endpoint 4 |
| **OTG Device Control** | | |
| 0x01E0 0460 | DEVCTL | Device Control Register |
| **Dynamic FIFO Control** | | |
| 0x01E0 0462 | TXFIFOSZ | Transmit Endpoint FIFO Size<br>(Index register set to select Endpoints 1-4 only) |
| 0x01E0 0463 | RXFIFOSZ | Receive Endpoint FIFO Size<br>(Index register set to select Endpoints 1-4 only) |
| 0x01E0 0464 | TXFIFOADDR | Transmit Endpoint FIFO Address<br>(Index register set to select Endpoints 1-4 only) |


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**Table 5-92. Universal Serial Bus OTG (USB0) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E0 0466 | RXFIFOADDR | Receive Endpoint FIFO Address<br>(Index register set to select Endpoints 1-4 only) |
| 0x01E0 046C | HWVERS | Hardware Version Register |
| **Target Endpoint 0 Control Registers, Valid Only in Host Mode** | | |
| 0x01E0 0480 | TXFUNCADDR | Address of the target function that has to be accessed through the associated Transmit Endpoint. |
| 0x01E0 0482 | TXHUBADDR | Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 0483 | TXHUBPORT | Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 0484 | RXFUNCADDR | Address of the target function that has to be accessed through the associated Receive Endpoint. |
| 0x01E0 0486 | RXHUBADDR | Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 0487 | RXHUBPORT | Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| **Target Endpoint 1 Control Registers, Valid Only in Host Mode** | | |
| 0x01E0 0488 | TXFUNCADDR | Address of the target function that has to be accessed through the associated Transmit Endpoint. |
| 0x01E0 048A | TXHUBADDR | Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 048B | TXHUBPORT | Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 048C | RXFUNCADDR | Address of the target function that has to be accessed through the associated Receive Endpoint. |
| 0x01E0 048E | RXHUBADDR | Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 048F | RXHUBPORT | Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| **Target Endpoint 2 Control Registers, Valid Only in Host Mode** | | |
| 0x01E0 0490 | TXFUNCADDR | Address of the target function that has to be accessed through the associated Transmit Endpoint. |
| 0x01E0 0492 | TXHUBADDR | Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 0493 | TXHUBPORT | Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 0494 | RXFUNCADDR | Address of the target function that has to be accessed through the associated Receive Endpoint. |
| 0x01E0 0496 | RXHUBADDR | Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 0497 | RXHUBPORT | Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| **Target Endpoint 3 Control Registers, Valid Only in Host Mode** | | |
| 0x01E0 0498 | TXFUNCADDR | Address of the target function that has to be accessed through the associated Transmit Endpoint. |

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**Table 5-92. Universal Serial Bus OTG (USB0) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E0 049A | TXHUBADDR | Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 049B | TXHUBPORT | Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 049C | RXFUNCADDR | Address of the target function that has to be accessed through the associated Receive Endpoint. |
| 0x01E0 049E | RXHUBADDR | Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 049F | RXHUBPORT | Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| **Target Endpoint 4 Control Registers, Valid Only in Host Mode** | | |
| 0x01E0 04A0 | TXFUNCADDR | Address of the target function that has to be accessed through the associated Transmit Endpoint. |
| 0x01E0 04A2 | TXHUBADDR | Address of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 04A3 | TXHUBPORT | Port of the hub that has to be accessed through the associated Transmit Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 04A4 | RXFUNCADDR | Address of the target function that has to be accessed through the associated Receive Endpoint. |
| 0x01E0 04A6 | RXHUBADDR | Address of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| 0x01E0 04A7 | RXHUBPORT | Port of the hub that has to be accessed through the associated Receive Endpoint. This is used only when full speed or low speed device is connected via a USB2.0 high-speed hub. |
| **Control and Status Register for Endpoint 0** | | |
| 0x01E0 0502 | PERI_CSR0 | Control Status Register for Endpoint 0 in Peripheral Mode |
| | HOST_CSR0 | Control Status Register for Endpoint 0 in Host Mode |
| 0x01E0 0508 | COUNT0 | Number of Received Bytes in Endpoint 0 FIFO |
| 0x01E0 050A | HOST_TYPE0 | Defines the Speed of Endpoint 0 |
| 0x01E0 050B | HOST_NAKLIMIT0 | Sets the NAK Response Timeout on Endpoint 0 |
| 0x01E0 050F | CONFIGDATA | Returns details of core configuration. |
| **Control and Status Register for Endpoint 1** | | |
| 0x01E0 0510 | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 0x01E0 0512 | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| | HOST_TXCSR | Control Status Register for Host Transmit Endpoint (host mode) |
| 0x01E0 0514 | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 0x01E0 0516 | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| | HOST_RXCSR | Control Status Register for Host Receive Endpoint (host mode) |
| 0x01E0 0518 | RXCOUNT | Number of Bytes in Host Receive endpoint FIFO |
| 0x01E0 051A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint. |
| 0x01E0 051B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint. |
| 0x01E0 051C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint. |
| 0x01E0 051D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint. |
| **Control and Status Register for Endpoint 2** | | |


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**Table 5-92. Universal Serial Bus OTG (USB0) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E0 0520 | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 0x01E0 0522 | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| | HOST_TXCSR | Control Status Register for Host Transmit Endpoint (host mode) |
| 0x01E0 0524 | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 0x01E0 0526 | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| | HOST_RXCSR | Control Status Register for Host Receive Endpoint (host mode) |
| 0x01E0 0528 | RXCOUNT | Number of Bytes in Host Receive endpoint FIFO |
| 0x01E0 052A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint. |
| 0x01E0 052B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint. |
| 0x01E0 052C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint. |
| 0x01E0 052D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint. |
| **Control and Status Register for Endpoint 3** | | |
| 0x01E0 0530 | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 0x01E0 0532 | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| | HOST_TXCSR | Control Status Register for Host Transmit Endpoint (host mode) |
| 0x01E0 0534 | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 0x01E0 0536 | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| | HOST_RXCSR | Control Status Register for Host Receive Endpoint (host mode) |
| 0x01E0 0538 | RXCOUNT | Number of Bytes in Host Receive endpoint FIFO |
| 0x01E0 053A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint. |
| 0x01E0 053B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint. |
| 0x01E0 053C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint. |
| 0x01E0 053D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint. |
| **Control and Status Register for Endpoint 4** | | |
| 0x01E0 0540 | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 0x01E0 0542 | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| | HOST_TXCSR | Control Status Register for Host Transmit Endpoint (host mode) |
| 0x01E0 0544 | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 0x01E0 0546 | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| | HOST_RXCSR | Control Status Register for Host Receive Endpoint (host mode) |
| 0x01E0 0548 | RXCOUNT | Number of Bytes in Host Receive endpoint FIFO |
| 0x01E0 054A | HOST_TXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Transmit endpoint. |
| 0x01E0 054B | HOST_TXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Transmit endpoint. |
| 0x01E0 054C | HOST_RXTYPE | Sets the operating speed, transaction protocol and peripheral endpoint number for the host Receive endpoint. |
| 0x01E0 054D | HOST_RXINTERVAL | Sets the polling interval for Interrupt/ISOC transactions or the NAK response timeout on Bulk transactions for host Receive endpoint. |
| **DMA Registers** | | |
| 0x01E0 1000 | DMAREVID | DMA Revision Register |
| 0x01E0 1004 | TDFDQ | DMA Teardown Free Descriptor Queue Control Register |
| 0x01E0 1008 | DMAEMU | DMA Emulation Control Register |

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**Table 5-92. Universal Serial Bus OTG (USB0) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E0 1800 | TXGCR[0] | Transmit Channel 0 Global Configuration Register |
| 0x01E0 1808 | RXGCR[0] | Receive Channel 0 Global Configuration Register |
| 0x01E0 180C | RXHPCRA[0] | Receive Channel 0 Host Packet Configuration Register A |
| 0x01E0 1810 | RXHPCRB[0] | Receive Channel 0 Host Packet Configuration Register B |
| 0x01E0 1820 | TXGCR[1] | Transmit Channel 1 Global Configuration Register |
| 0x01E0 1828 | RXGCR[1] | Receive Channel 1 Global Configuration Register |
| 0x01E0 182C | RXHPCRA[1] | Receive Channel 1 Host Packet Configuration Register A |
| 0x01E0 1830 | RXHPCRB[1] | Receive Channel 1 Host Packet Configuration Register B |
| 0x01E0 1840 | TXGCR[2] | Transmit Channel 2 Global Configuration Register |
| 0x01E0 1848 | RXGCR[2] | Receive Channel 2 Global Configuration Register |
| 0x01E0 184C | RXHPCRA[2] | Receive Channel 2 Host Packet Configuration Register A |
| 0x01E0 1850 | RXHPCRB[2] | Receive Channel 2 Host Packet Configuration Register B |
| 0x01E0 1860 | TXGCR[3] | Transmit Channel 3 Global Configuration Register |
| 0x01E0 1868 | RXGCR[3] | Receive Channel 3 Global Configuration Register |
| 0x01E0 186C | RXHPCRA[3] | Receive Channel 3 Host Packet Configuration Register A |
| 0x01E0 1870 | RXHPCRB[3] | Receive Channel 3 Host Packet Configuration Register B |
| 0x01E0 2000 | DMA_SCHED_CTRL | DMA Scheduler Control Register |
| 0x01E0 2800 | WORD[0] | DMA Scheduler Table Word 0 |
| 0x01E0 2804 | WORD[1] | DMA Scheduler Table Word 1 |
| . . . | . . . | . . . |
| 0x01E0 28FC | WORD[63] | DMA Scheduler Table Word 63 |
| **Queue Manager Registers** | | |
| 0x01E0 4000 | QMGRREVID | Queue Manager Revision Register |
| 0x01E0 4008 | DIVERSION | Queue Diversion Register |
| 0x01E0 4020 | FDBSC0 | Free Descriptor/Buffer Starvation Count Register 0 |
| 0x01E0 4024 | FDBSC1 | Free Descriptor/Buffer Starvation Count Register 1 |
| 0x01E0 4028 | FDBSC2 | Free Descriptor/Buffer Starvation Count Register 2 |
| 0x01E0 402C | FDBSC3 | Free Descriptor/Buffer Starvation Count Register 3 |
| 0x01E0 4080 | LRAM0BASE | Linking RAM Region 0 Base Address Register |
| 0x01E0 4084 | LRAM0SIZE | Linking RAM Region 0 Size Register |
| 0x01E0 4088 | LRAM1BASE | Linking RAM Region 1 Base Address Register |
| 0x01E0 4090 | PEND0 | Queue Pending Register 0 |
| 0x01E0 4094 | PEND1 | Queue Pending Register 1 |
| 0x01E0 5000 | QMEMRBASE[0] | Memory Region 0 Base Address Register |
| 0x01E0 5004 | QMEMRCTRL[0] | Memory Region 0 Control Register |
| 0x01E0 5010 | QMEMRBASE[1] | Memory Region 1 Base Address Register |
| 0x01E0 5014 | QMEMRCTRL[1] | Memory Region 1 Control Register |
| . . . | . . . | . . . |
| 0x01E0 50F0 | QMEMRBASE[15] | Memory Region 15 Base Address Register |
| 0x01E0 50F4 | QMEMRCTRL[15] | Memory Region 15 Control Register |
| 0x01E0 600C | CTRLD[0] | Queue Manager Queue 0 Control Register D |
| 0x01E0 601C | CTRLD[1] | Queue Manager Queue 1 Control Register D |
| . . . | . . . | . . . |
| 0x01E0 63FC | CTRLD[63] | Queue Manager Queue 63 Status Register D |
| 0x01E0 6800 | QSTATA[0] | Queue Manager Queue 0 Status Register A |
| 0x01E0 6804 | QSTATB[0] | Queue Manager Queue 0 Status Register B |
| 0x01E0 6808 | QSTATC[0] | Queue Manager Queue 0 Status Register C |


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**Table 5-92. Universal Serial Bus OTG (USB0) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E0 6810 | QSTATA[1] | Queue Manager Queue 1 Status Register A |
| 0x01E0 6814 | QSTATB[1] | Queue Manager Queue 1 Status Register B |
| 0x01E0 6818 | QSTATC[1] | Queue Manager Queue 1 Status Register C |
| . . . | . . . | . . . |
| 0x01E0 6BF0 | QSTATA[63] | Queue Manager Queue 63 Status Register A |
| 0x01E0 6BF4 | QSTATB[63] | Queue Manager Queue 63 Status Register B |
| 0x01E0 6BF8 | QSTATC[63] | Queue Manager Queue 63 Status Register C |

### 5.20.1 USB0 [USB2.0] Electrical Data/Timing

The USB PHY PLL can support input clock of the following frequencies: 12.0 MHz, 13.0 MHz, 19.2 MHz, 20.0 MHz, 24.0 MHz, 26.0 MHz, 38.4 MHz, 40.0 MHz or 48.0 MHz. USB_REFCLKIN jitter tolerance is 50 ppm (maximum).

**Table 5-93. Switching Characteristics Over Recommended Operating Conditions for USB0 [USB2.0] (see Figure 5-46)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | LOW SPEED 1.5 Mbps | | FULL SPEED 12 Mbps | | HIGH SPEED 480 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{r(D)}$ | Rise time, USB_DP and USB_DM signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 2 | $t_{f(D)}$ | Fall time, USB_DP and USB_DM signals(1) | 75 | 300 | 4 | 20 | 0.5 | | ns |
| 3 | $t_{rfM}$ | Rise/Fall time, matching(2) | 80 | 120 | 90 | 111 | – | – | % |
| 4 | $V_{CRS}$ | Output signal cross-over voltage(1) | 1.3 | 2 | 1.3 | 2 | – | – | V |
| 5 | $t_{jr(source)NT}$ | Source (Host) Driver jitter, next transition | | 2 | | 2 | | | (3)ns |
| | $t_{jr(FUNC)NT}$ | Function Driver jitter, next transition | | 25 | | 2 | | (3) | ns |
| 6 | $t_{jr(source)PT}$ | Source (Host) Driver jitter, paired transition(4) | | 1 | | 1 | | (3) | ns |
| | $t_{jr(FUNC)PT}$ | Function Driver jitter, paired transition | | 10 | | 1 | | (3) | ns |
| 7 | $t_{w(EOPT)}$ | Pulse duration, EOP transmitter | 1250 | 1500 | 160 | 175 | – | – | ns |
| 8 | $t_{w(EOPR)}$ | Pulse duration, EOP receiver | 670 | | 82 | | – | | ns |
| 9 | $t_{(DRATE)}$ | Data Rate | | 1.5 | | 12 | | 480 | Mb/s |
| 10 | $Z_{DRV}$ | Driver Output Resistance | – | – | 40.5 | 49.5 | 40.5 | 49.5 | Ω |
| 11 | $Z_{INP}$ | Receiver Input Impedance | 100k | | 100k | | - | - | Ω |

(1) Low Speed: $C_L$ = 200 pF, Full Speed: $C_L$ = 50 pF, High Speed: $C_L$ = 50 pF
(2) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]
(3) For more detailed information, see the Universal Serial Bus Specification Revision 2.0, Chapter 7. Electrical.
(4) $t_{jr} = t_{px(1)} - t_{px(0)}$

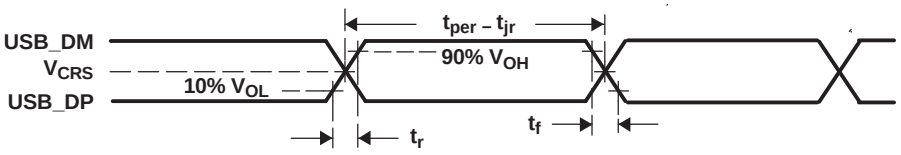


**Figure 5-46. USB2.0 Integrated Transceiver Interface Timing**

## 5.21 Universal Serial Bus Host Controller (USB1) [USB1.1 OHCI]

All the USB interfaces for this device are compliant with Universal Serial Bus Specifications, Revision 1.1.

Table 5-94 is the list of USB Host Controller registers.

**Table 5-94. USB Host Controller Registers**

| USB1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 5000 | HCREVISION | OHCI Revision Number Register |
| 0x01E2 5004 | HCCONTROL | HC Operating Mode Register |
| 0x01E2 5008 | HCCOMMANDSTATUS | HC Command and Status Register |
| 0x01E2 500C | HCINTERRUPTSTATUS | HC Interrupt and Status Register |
| 0x01E2 5010 | HCINTERRUPTENABLE | HC Interrupt Enable Register |
| 0x01E2 5014 | HCINTERRUPTDISABLE | HC Interrupt Disable Register |
| 0x01E2 5018 | HCHCCA | HC HCAA Address Register(1) |
| 0x01E2 501C | HCPERIODCURRENTED | HC Current Periodic Register(1) |
| 0x01E2 5020 | HCCONTROLHEADED | HC Head Control Register(1) |
| 0x01E2 5024 | HCCONTROLCURRENTED | HC Current Control Register(1) |
| 0x01E2 5028 | HCBULKHEADED | HC Head Bulk Register(1) |
| 0x01E2 502C | HCBULKCURRENTED | HC Current Bulk Register(1) |
| 0x01E2 5030 | HCDONEHEAD | HC Head Done Register(1) |
| 0x01E2 5034 | HCFMINTERVAL | HC Frame Interval Register |
| 0x01E2 5038 | HCFMREMAINING | HC Frame Remaining Register |
| 0x01E2 503C | HCFMNUMBER | HC Frame Number Register |
| 0x01E2 5040 | HCPERIODICSTART | HC Periodic Start Register |
| 0x01E2 5044 | HCLSTHRESHOLD | HC Low-Speed Threshold Register |
| 0x01E2 5048 | HCRHDESCRIPTORA | HC Root Hub A Register |
| 0x01E2 504C | HCRHDESCRIPTORB | HC Root Hub B Register |
| 0x01E2 5050 | HCRHSTATUS | HC Root Hub Status Register |
| 0x01E2 5054 | HCRHPORTSTATUS1 | HC Port 1 Status and Control Register(2) |
| 0x01E2 5058 | HCRHPORTSTATUS2 | HC Port 2 Status and Control Register(3) |

(1) Restrictions apply to the physical addresses used in these registers.
(2) Connected to the integrated USB1.1 phy pins (USB1_DM, USB1_DP).
(3) Although the controller implements two ports, the second port cannot be used.

**Table 5-95. Switching Characteristics Over Recommended Operating Conditions for USB1 [USB1.1]**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | LOW SPEED | | FULL SPEED | | |
| | | | MIN | MAX | MAX | MAX | |
| U1 | $t_r$ | Rise time, USB.DP and USB.DM signals(1) | 75(1) | 300(1) | 4(1) | 20(1) | ns |
| U2 | $t_f$ | Fall time, USB.DP and USB.DM signals(1) | 75(1) | 300(1) | 4(1) | 20(1) | ns |
| U3 | $t_{RFM}$ | Rise/Fall time matching(2) | 80(2) | 120(2) | 90(2) | 110(2) | % |
| U4 | $V_{CRS}$ | Output signal cross-over voltage(1) | 1.3(1) | 2(1) | 1.3(1) | 2(1) | V |
| U5 | $t_j$ | Differential propagation jitter(3) | -25(3) | 25(3) | -2(3) | 2(3) | ns |
| U6 | $f_{op}$ | Operating frequency(4) | | 1.5 | | 12 | MHz |

(1) Low Speed: $C_L$ = 200 pF. High Speed: $C_L$ = 50pF
(2) $t_{RFM}$ =( $t_r/t_f$ ) x 100
(3) $t_{jr} = t_{px(1)} - t_{px(0)}$
(4) $f_{op} = 1/t_{per}$


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## 5.22 Ethernet Media Access Controller (EMAC)

The Ethernet Media Access Controller (EMAC) provides an efficient interface between device and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The EMAC controls the flow of packet data from the device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts.

### *5.22.1 EMAC Peripheral Register Description(s)*

**Table 5-96. Ethernet Media Access Controller (EMAC) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 3000 | TXREV | Transmit Revision Register |
| 0x01E2 3004 | TXCONTROL | Transmit Control Register |
| 0x01E2 3008 | TXTEARDOWN | Transmit Teardown Register |
| 0x01E2 3010 | RXREV | Receive Revision Register |
| 0x01E2 3014 | RXCONTROL | Receive Control Register |
| 0x01E2 3018 | RXTEARDOWN | Receive Teardown Register |
| 0x01E2 3080 | TXINTSTATRAW | Transmit Interrupt Status (Unmasked) Register |
| 0x01E2 3084 | TXINTSTATMASKED | Transmit Interrupt Status (Masked) Register |
| 0x01E2 3088 | TXINTMASKSET | Transmit Interrupt Mask Set Register |
| 0x01E2 308C | TXINTMASKCLEAR | Transmit Interrupt Clear Register |
| 0x01E2 3090 | MACINVECTOR | MAC Input Vector Register |
| 0x01E2 3094 | MACEOIVECTOR | MAC End Of Interrupt Vector Register |
| 0x01E2 30A0 | RXINTSTATRAW | Receive Interrupt Status (Unmasked) Register |
| 0x01E2 30A4 | RXINTSTATMASKED | Receive Interrupt Status (Masked) Register |
| 0x01E2 30A8 | RXINTMASKSET | Receive Interrupt Mask Set Register |
| 0x01E2 30AC | RXINTMASKCLEAR | Receive Interrupt Mask Clear Register |
| 0x01E2 30B0 | MACINTSTATRAW | MAC Interrupt Status (Unmasked) Register |
| 0x01E2 30B4 | MACINTSTATMASKED | MAC Interrupt Status (Masked) Register |
| 0x01E2 30B8 | MACINTMASKSET | MAC Interrupt Mask Set Register |
| 0x01E2 30BC | MACINTMASKCLEAR | MAC Interrupt Mask Clear Register |
| 0x01E2 3100 | RXMBPENABLE | Receive Multicast/Broadcast/Promiscuous Channel Enable Register |
| 0x01E2 3104 | RXUNICASTSET | Receive Unicast Enable Set Register |
| 0x01E2 3108 | RXUNICASTCLEAR | Receive Unicast Clear Register |
| 0x01E2 310C | RXMAXLEN | Receive Maximum Length Register |
| 0x01E2 3110 | RXBUFFEROFFSET | Receive Buffer Offset Register |
| 0x01E2 3114 | RXFILTERLOWTHRESH | Receive Filter Low Priority Frame Threshold Register |
| 0x01E2 3120 | RX0FLOWTHRESH | Receive Channel 0 Flow Control Threshold Register |
| 0x01E2 3124 | RX1FLOWTHRESH | Receive Channel 1 Flow Control Threshold Register |
| 0x01E2 3128 | RX2FLOWTHRESH | Receive Channel 2 Flow Control Threshold Register |
| 0x01E2 312C | RX3FLOWTHRESH | Receive Channel 3 Flow Control Threshold Register |
| 0x01E2 3130 | RX4FLOWTHRESH | Receive Channel 4 Flow Control Threshold Register |
| 0x01E2 3134 | RX5FLOWTHRESH | Receive Channel 5 Flow Control Threshold Register |
| 0x01E2 3138 | RX6FLOWTHRESH | Receive Channel 6 Flow Control Threshold Register |
| 0x01E2 313C | RX7FLOWTHRESH | Receive Channel 7 Flow Control Threshold Register |

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**Table 5-96. Ethernet Media Access Controller (EMAC) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 3140 | RX0FREEBUFFER | Receive Channel 0 Free Buffer Count Register |
| 0x01E2 3144 | RX1FREEBUFFER | Receive Channel 1 Free Buffer Count Register |
| 0x01E2 3148 | RX2FREEBUFFER | Receive Channel 2 Free Buffer Count Register |
| 0x01E2 314C | RX3FREEBUFFER | Receive Channel 3 Free Buffer Count Register |
| 0x01E2 3150 | RX4FREEBUFFER | Receive Channel 4 Free Buffer Count Register |
| 0x01E2 3154 | RX5FREEBUFFER | Receive Channel 5 Free Buffer Count Register |
| 0x01E2 3158 | RX6FREEBUFFER | Receive Channel 6 Free Buffer Count Register |
| 0x01E2 315C | RX7FREEBUFFER | Receive Channel 7 Free Buffer Count Register |
| 0x01E2 3160 | MACCONTROL | MAC Control Register |
| 0x01E2 3164 | MACSTATUS | MAC Status Register |
| 0x01E2 3168 | EMCONTROL | Emulation Control Register |
| 0x01E2 316C | FIFOCONTROL | FIFO Control Register |
| 0x01E2 3170 | MACCONFIG | MAC Configuration Register |
| 0x01E2 3174 | SOFTRESET | Soft Reset Register |
| 0x01E2 31D0 | MACSRCADDRLO | MAC Source Address Low Bytes Register |
| 0x01E2 31D4 | MACSRCADDRHI | MAC Source Address High Bytes Register |
| 0x01E2 31D8 | MACHASH1 | MAC Hash Address Register 1 |
| 0x01E2 31DC | MACHASH2 | MAC Hash Address Register 2 |
| 0x01E2 31E0 | BOFFTEST | Back Off Test Register |
| 0x01E2 31E4 | TPACETEST | Transmit Pacing Algorithm Test Register |
| 0x01E2 31E8 | RXPAUSE | Receive Pause Timer Register |
| 0x01E2 31EC | TXPAUSE | Transmit Pause Timer Register |
| 0x01E2 3200 - 0x01E2 32FC | (see Table 5-97) | EMAC Statistics Registers |
| 0x01E2 3500 | MACADDRLO | MAC Address Low Bytes Register, Used in Receive Address Matching |
| 0x01E2 3504 | MACADDRHI | MAC Address High Bytes Register, Used in Receive Address Matching |
| 0x01E2 3508 | MACINDEX | MAC Index Register |
| 0x01E2 3600 | TX0HDP | Transmit Channel 0 DMA Head Descriptor Pointer Register |
| 0x01E2 3604 | TX1HDP | Transmit Channel 1 DMA Head Descriptor Pointer Register |
| 0x01E2 3608 | TX2HDP | Transmit Channel 2 DMA Head Descriptor Pointer Register |
| 0x01E2 360C | TX3HDP | Transmit Channel 3 DMA Head Descriptor Pointer Register |
| 0x01E2 3610 | TX4HDP | Transmit Channel 4 DMA Head Descriptor Pointer Register |
| 0x01E2 3614 | TX5HDP | Transmit Channel 5 DMA Head Descriptor Pointer Register |
| 0x01E2 3618 | TX6HDP | Transmit Channel 6 DMA Head Descriptor Pointer Register |
| 0x01E2 361C | TX7HDP | Transmit Channel 7 DMA Head Descriptor Pointer Register |
| 0x01E2 3620 | RX0HDP | Receive Channel 0 DMA Head Descriptor Pointer Register |
| 0x01E2 3624 | RX1HDP | Receive Channel 1 DMA Head Descriptor Pointer Register |
| 0x01E2 3628 | RX2HDP | Receive Channel 2 DMA Head Descriptor Pointer Register |
| 0x01E2 362C | RX3HDP | Receive Channel 3 DMA Head Descriptor Pointer Register |
| 0x01E2 3630 | RX4HDP | Receive Channel 4 DMA Head Descriptor Pointer Register |
| 0x01E2 3634 | RX5HDP | Receive Channel 5 DMA Head Descriptor Pointer Register |
| 0x01E2 3638 | RX6HDP | Receive Channel 6 DMA Head Descriptor Pointer Register |
| 0x01E2 363C | RX7HDP | Receive Channel 7 DMA Head Descriptor Pointer Register |
| 0x01E2 3640 | TX0CP | Transmit Channel 0 Completion Pointer Register |
| 0x01E2 3644 | TX1CP | Transmit Channel 1 Completion Pointer Register |
| 0x01E2 3648 | TX2CP | Transmit Channel 2 Completion Pointer Register |
| 0x01E2 364C | TX3CP | Transmit Channel 3 Completion Pointer Register |
| 0x01E2 3650 | TX4CP | Transmit Channel 4 Completion Pointer Register |


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**Table 5-96. Ethernet Media Access Controller (EMAC) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 3654 | TX5CP | Transmit Channel 5 Completion Pointer Register |
| 0x01E2 3658 | TX6CP | Transmit Channel 6 Completion Pointer Register |
| 0x01E2 365C | TX7CP | Transmit Channel 7 Completion Pointer Register |
| 0x01E2 3660 | RX0CP | Receive Channel 0 Completion Pointer Register |
| 0x01E2 3664 | RX1CP | Receive Channel 1 Completion Pointer Register |
| 0x01E2 3668 | RX2CP | Receive Channel 2 Completion Pointer Register |
| 0x01E2 366C | RX3CP | Receive Channel 3 Completion Pointer Register |
| 0x01E2 3670 | RX4CP | Receive Channel 4 Completion Pointer Register |
| 0x01E2 3674 | RX5CP | Receive Channel 5 Completion Pointer Register |
| 0x01E2 3678 | RX6CP | Receive Channel 6 Completion Pointer Register |
| 0x01E2 367C | RX7CP | Receive Channel 7 Completion Pointer Register |

**Table 5-97. EMAC Statistics Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 3200 | RXGOODFRAMES | Good Receive Frames Register |
| 0x01E2 3204 | RXBCASTFRAMES | Broadcast Receive Frames Register (Total number of good broadcast frames received) |
| 0x01E2 3208 | RXMCASTFRAMES | Multicast Receive Frames Register (Total number of good multicast frames received) |
| 0x01E2 320C | RXPAUSEFRAMES | Pause Receive Frames Register |
| 0x01E2 3210 | RXCRCERRORS | Receive CRC Errors Register (Total number of frames received with CRC errors) |
| 0x01E2 3214 | RXALIGNCODEERRORS | Receive Alignment/Code Errors Register (Total number of frames received with alignment/code errors) |
| 0x01E2 3218 | RXOVERSIZED | Receive Oversized Frames Register (Total number of oversized frames received) |
| 0x01E2 321C | RXJABBER | Receive Jabber Frames Register (Total number of jabber frames received) |
| 0x01E2 3220 | RXUNDERSIZED | Receive Undersized Frames Register (Total number of undersized frames received) |
| 0x01E2 3224 | RXFRAGMENTS | Receive Frame Fragments Register |
| 0x01E2 3228 | RXFILTERED | Filtered Receive Frames Register |
| 0x01E2 322C | RXQOSFILTERED | Received QOS Filtered Frames Register |
| 0x01E2 3230 | RXOCTETS | Receive Octet Frames Register (Total number of received bytes in good frames) |
| 0x01E2 3234 | TXGOODFRAMES | Good Transmit Frames Register (Total number of good frames transmitted) |
| 0x01E2 3238 | TXBCASTFRAMES | Broadcast Transmit Frames Register |
| 0x01E2 323C | TXMCASTFRAMES | Multicast Transmit Frames Register |
| 0x01E2 3240 | TXPAUSEFRAMES | Pause Transmit Frames Register |
| 0x01E2 3244 | TXDEFERRED | Deferred Transmit Frames Register |
| 0x01E2 3248 | TXCOLLISION | Transmit Collision Frames Register |
| 0x01E2 324C | TXSINGLECOLL | Transmit Single Collision Frames Register |
| 0x01E2 3250 | TXMULTICOLL | Transmit Multiple Collision Frames Register |
| 0x01E2 3254 | TXEXCESSIVECOLL | Transmit Excessive Collision Frames Register |
| 0x01E2 3258 | TXLATECOLL | Transmit Late Collision Frames Register |
| 0x01E2 325C | TXUNDERRUN | Transmit Underrun Error Register |
| 0x01E2 3260 | TXCARRIERSENSE | Transmit Carrier Sense Errors Register |
| 0x01E2 3264 | TXOCTETS | Transmit Octet Frames Register |
| 0x01E2 3268 | FRAME64 | Transmit and Receive 64 Octet Frames Register |

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**Table 5-97. EMAC Statistics Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 326C | FRAME65T127 | Transmit and Receive 65 to 127 Octet Frames Register |
| 0x01E2 3270 | FRAME128T255 | Transmit and Receive 128 to 255 Octet Frames Register |
| 0x01E2 3274 | FRAME256T511 | Transmit and Receive 256 to 511 Octet Frames Register |
| 0x01E2 3278 | FRAME512T1023 | Transmit and Receive 512 to 1023 Octet Frames Register |
| 0x01E2 327C | FRAME1024TUP | Transmit and Receive 1024 to 1518 Octet Frames Register |
| 0x01E2 3280 | NETOCTETS | Network Octet Frames Register |
| 0x01E2 3284 | RXSOFOVERRUNS | Receive FIFO or DMA Start of Frame Overruns Register |
| 0x01E2 3288 | RXMOFOVERRUNS | Receive FIFO or DMA Middle of Frame Overruns Register |
| 0x01E2 328C | RXDMAOVERRUNS | Receive DMA Start of Frame and Middle of Frame Overruns Register |

**Table 5-98. EMAC Control Module Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 2000 | REV | EMAC Control Module Revision Register |
| 0x01E2 2004 | SOFTRESET | EMAC Control Module Software Reset Register |
| 0x01E2 200C | INTCONTROL | EMAC Control Module Interrupt Control Register |
| 0x01E2 2010 | C0RXTHRESHEN | EMAC Control Module Interrupt Core 0 Receive Threshold Interrupt Enable Register |
| 0x01E2 2014 | C0RXEN | EMAC Control Module Interrupt Core 0 Receive Interrupt Enable Register |
| 0x01E2 2018 | C0TXEN | EMAC Control Module Interrupt Core 0 Transmit Interrupt Enable Register |
| 0x01E2 201C | C0MISCEN | EMAC Control Module Interrupt Core 0 Miscellaneous Interrupt Enable Register |
| 0x01E2 2020 | C1RXTHRESHEN | EMAC Control Module Interrupt Core 1 Receive Threshold Interrupt Enable Register |
| 0x01E2 2024 | C1RXEN | EMAC Control Module Interrupt Core 1 Receive Interrupt Enable Register |
| 0x01E2 2028 | C1TXEN | EMAC Control Module Interrupt Core 1 Transmit Interrupt Enable Register |
| 0x01E2 202C | C1MISCEN | EMAC Control Module Interrupt Core 1 Miscellaneous Interrupt Enable Register |
| 0x01E2 2030 | C2RXTHRESHEN | EMAC Control Module Interrupt Core 2 Receive Threshold Interrupt Enable Register |
| 0x01E2 2034 | C2RXEN | EMAC Control Module Interrupt Core 2 Receive Interrupt Enable Register |
| 0x01E2 2038 | C2TXEN | EMAC Control Module Interrupt Core 2 Transmit Interrupt Enable Register |
| 0x01E2 203C | C2MISCEN | EMAC Control Module Interrupt Core 2 Miscellaneous Interrupt Enable Register |
| 0x01E2 2040 | C0RXTHRESHSTAT | EMAC Control Module Interrupt Core 0 Receive Threshold Interrupt Status Register |
| 0x01E2 2044 | C0RXSTAT | EMAC Control Module Interrupt Core 0 Receive Interrupt Status Register |
| 0x01E2 2048 | C0TXSTAT | EMAC Control Module Interrupt Core 0 Transmit Interrupt Status Register |
| 0x01E2 204C | C0MISCSTAT | EMAC Control Module Interrupt Core 0 Miscellaneous Interrupt Status Register |
| 0x01E2 2050 | C1RXTHRESHSTAT | EMAC Control Module Interrupt Core 1 Receive Threshold Interrupt Status Register |
| 0x01E2 2054 | C1RXSTAT | EMAC Control Module Interrupt Core 1 Receive Interrupt Status Register |
| 0x01E2 2058 | C1TXSTAT | EMAC Control Module Interrupt Core 1 Transmit Interrupt Status Register |
| 0x01E2 205C | C1MISCSTAT | EMAC Control Module Interrupt Core 1 Miscellaneous Interrupt Status Register |
| 0x01E2 2060 | C2RXTHRESHSTAT | EMAC Control Module Interrupt Core 2 Receive Threshold Interrupt Status Register |
| 0x01E2 2064 | C2RXSTAT | EMAC Control Module Interrupt Core 2 Receive Interrupt Status Register |
| 0x01E2 2068 | C2TXSTAT | EMAC Control Module Interrupt Core 2 Transmit Interrupt Status Register |
| 0x01E2 206C | C2MISCSTAT | EMAC Control Module Interrupt Core 2 Miscellaneous Interrupt Status Register |
| 0x01E2 2070 | C0RXIMAX | EMAC Control Module Interrupt Core 0 Receive Interrupts Per Millisecond Register |
| 0x01E2 2074 | C0TXIMAX | EMAC Control Module Interrupt Core 0 Transmit Interrupts Per Millisecond Register |
| 0x01E2 2078 | C1RXIMAX | EMAC Control Module Interrupt Core 1 Receive Interrupts Per Millisecond Register |
| 0x01E2 207C | C1TXIMAX | EMAC Control Module Interrupt Core 1 Transmit Interrupts Per Millisecond Register |
| 0x01E2 2080 | C2RXIMAX | EMAC Control Module Interrupt Core 2 Receive Interrupts Per Millisecond Register |
| 0x01E2 2084 | C2TXIMAX | EMAC Control Module Interrupt Core 2 Transmit Interrupts Per Millisecond Register |


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**Table 5-99. EMAC Control Module RAM**

| BYTE ADDRESS | DESCRIPTION |
|---|---|
| 0x01E2 0000 - 0x01E2 1FFF | EMAC Local Buffer Descriptor Memory |

### 5.22.1.1 EMAC Electrical Data/Timing

**Table 5-100. Timing Requirements for MII_RXCLK (see Figure 5-47)**

| NO. | | | 1.3V, 1.2V, 1.1V | | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 10 Mbps | | 100 Mbps | | 10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(MII_RXCLK)}$ | Cycle time, MII_RXCLK | 400 | | 40 | | 400 | | ns |
| 2 | $t_{w(MII_RXCLKH)}$ | Pulse duration, MII_RXCLK high | 140 | | 14 | | 140 | | ns |
| 3 | $t_{w(MII_RXCLKL)}$ | Pulse duration, MII_RXCLK low | 140 | | 14 | | 140 | | ns |

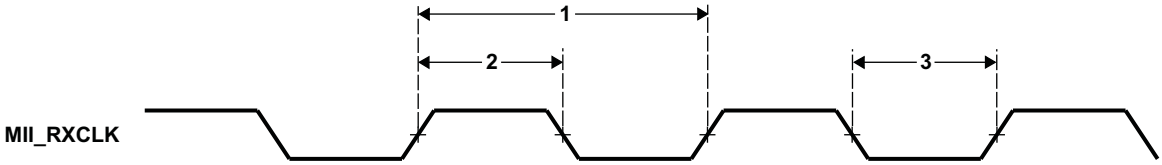


**Figure 5-47. MII_RXCLK Timing (EMAC - Receive)**

**Table 5-101. Timing Requirements for MII_TXCLK (see Figure 5-48)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V | | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | 10 Mbps | | 100 Mbps | | 10 Mbps | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(MII_TXCLK)}$ | Cycle time, MII_TXCLK | 400 | | 40 | | 400 | | ns |
| 2 | $t_{w(MII_TXCLKH)}$ | Pulse duration, MII_TXCLK high | 140 | | 14 | | 140 | | ns |
| 3 | $t_{w(MII_TXCLKL)}$ | Pulse duration, MII_TXCLK low | 140 | | 14 | | 140 | | ns |

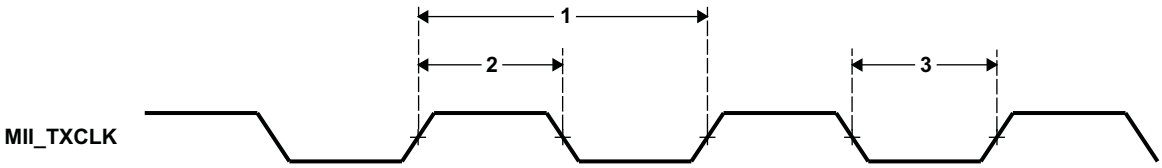


**Figure 5-48. MII_TXCLK Timing (EMAC - Transmit)**


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**Table 5-102. Timing Requirements for EMAC MII Receive 10/100 Mbit/s(1) (see Figure 5-49)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{su(MRXD-MII_RXCLKH)}$ | Setup time, receive selected signals valid before MII_RXCLK high | 8 | | ns |
| 2 | $t_{h(MII_RXCLKH-MRXD)}$ | Hold time, receive selected signals valid after MII_RXCLK high | 8 | | ns |

(1) Receive selected signals include: MII_RXD[3]-MII_RXD[0], MII_RXDV, and MII_RXER.

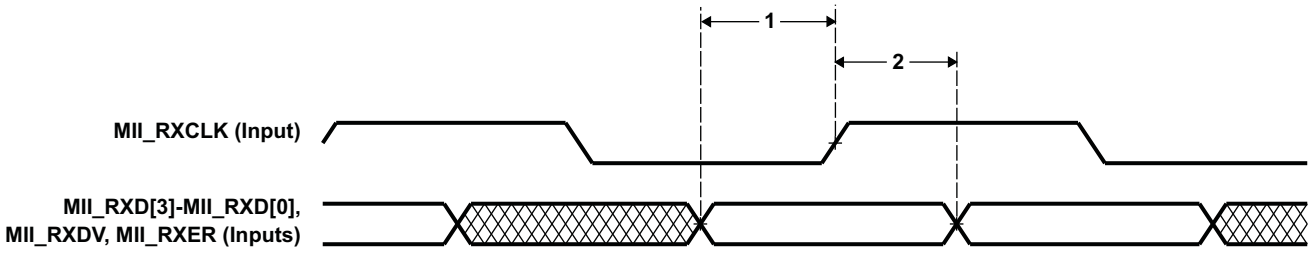


**Figure 5-49. EMAC Receive Interface Timing**

**Table 5-103. Switching Characteristics Over Recommended Operating Conditions for EMAC MII Transmit 10/100 Mbit/s(1) (see Figure 5-50)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{d(MII_TXCLKH-MTXD)}$ | Delay time, MII_TXCLK high to transmit selected signals valid | 2 | 25 | 2 | 32 | ns |

(1) Transmit selected signals include: MTXD3-MTXD0, and MII_TXEN.

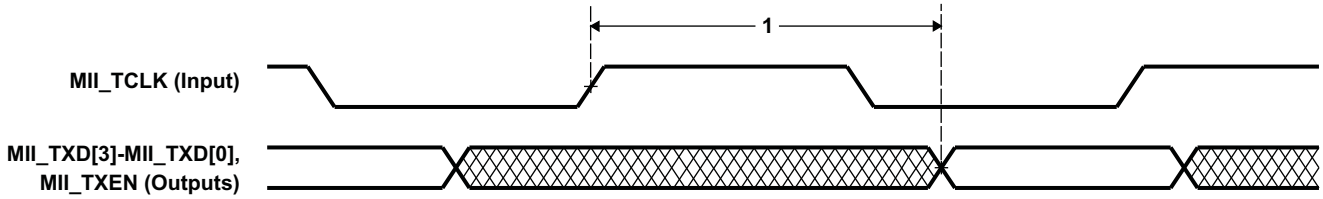


**Figure 5-50. EMAC Transmit Interface Timing**

**Table 5-104. Timing Requirements for EMAC RMII**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V(1) | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| 1 | tc(REFCLK) | Cycle Time, RMII_MHZ_50_CLK | | 20 | | ns |
| 2 | tw(REFCLKH) | Pulse Width, RMII_MHZ_50_CLK High | 7 | | 13 | ns |
| 3 | tw(REFCLKL) | Pulse Width, RMII_MHZ_50_CLK Low | 7 | | 13 | ns |
| 6 | tsu(RXD-REFCLK) | Input Setup Time, RXD Valid before RMII_MHZ_50_CLK High | 4 | | | ns |
| 7 | th(REFCLK-RXD) | Input Hold Time, RXD Valid after RMII_MHZ_50_CLK High | 2 | | | ns |
| 8 | tsu(CRSDV-REFCLK) | Input Setup Time, CRSDV Valid before RMII_MHZ_50_CLK High | 4 | | | ns |
| 9 | th(REFCLK-CRSDV) | Input Hold Time, CRSDV Valid after RMII_MHZ_50_CLK High | 2 | | | ns |
| 10 | tsu(RXER-REFCLK) | Input Setup Time, RXER Valid before RMII_MHZ_50_CLK High | 4 | | | ns |
| 11 | th(REFCLKR-RXER) | Input Hold Time, RXER Valid after RMII_MHZ_50_CLK High | 2 | | | ns |

(1) RMII is not supported at operating points below 1.1V nominal

**Note:** Per the RMII industry specification, the RMII reference clock (RMII_MHZ_50_CLK) must have jitter tolerance of 50 ppm or less.

**Table 5-105. Switching Characteristics Over Recommended Operating Conditions for EMAC RMII**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V(1) | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| 4 | td(REFCLK-TXD) | Output Delay Time, RMII_MHZ_50_CLK High to TXD Valid | 2.5 | | 13 | ns |
| 5 | td(REFCLK-TXEN) | Output Delay Time, RMII_MHZ_50_CLK High to TXEN Valid | 2.5 | | 13 | ns |

(1) RMII is not supported at operating points below 1.1V nominal.

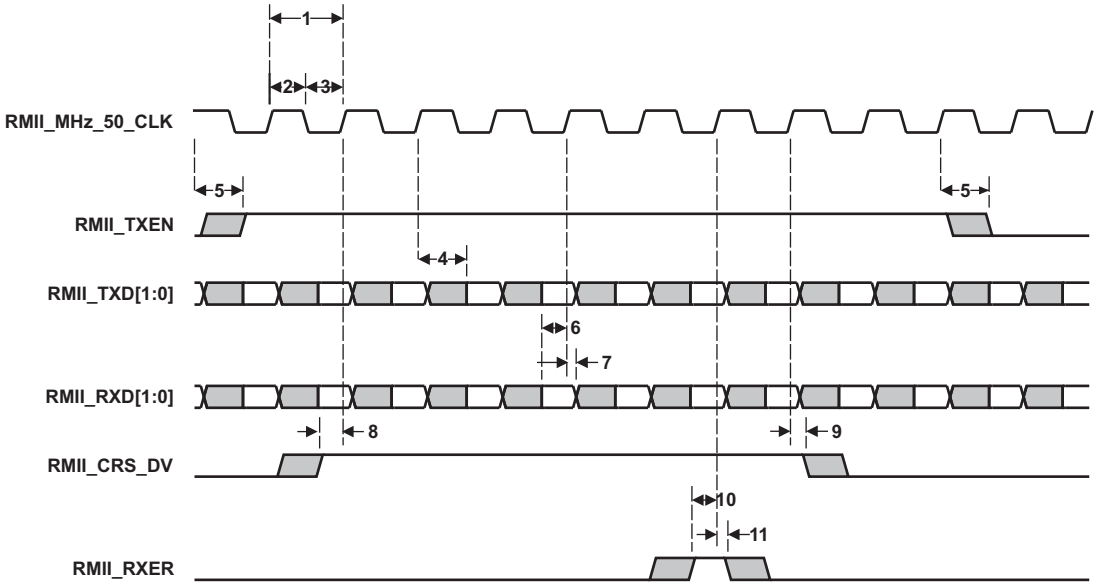


**Figure 5-51. RMII Timing Diagram**


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## 5.23 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and control Ethernet PHY(s) using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. Only one PHY may be connected at any given time.

### *5.23.1 MDIO Register Description(s)*

**Table 5-106. MDIO Register Memory Map**

| BYTE ADDRESS | ACRONYM | REGISTER NAME |
|---|---|---|
| 0x01E2 4000 | REV | Revision Identification Register |
| 0x01E2 4004 | CONTROL | MDIO Control Register |
| 0x01E2 4008 | ALIVE | MDIO PHY Alive Status Register |
| 0x01E2 400C | LINK | MDIO PHY Link Status Register |
| 0x01E2 4010 | LINKINTRAW | MDIO Link Status Change Interrupt (Unmasked) Register |
| 0x01E2 4014 | LINKINTMASKED | MDIO Link Status Change Interrupt (Masked) Register |
| 0x01E2 4018 | – | Reserved |
| 0x01E2 4020 | USERINTRAW | MDIO User Command Complete Interrupt (Unmasked) Register |
| 0x01E2 4024 | USERINTMASKED | MDIO User Command Complete Interrupt (Masked) Register |
| 0x01E2 4028 | USERINTMASKSET | MDIO User Command Complete Interrupt Mask Set Register |
| 0x01E2 402C | USERINTMASKCLEAR | MDIO User Command Complete Interrupt Mask Clear Register |
| 0x01E2 4030 - 0x01E2 407C | – | Reserved |
| 0x01E2 4080 | USERACCESS0 | MDIO User Access Register 0 |
| 0x01E2 4084 | USERPHYSEL0 | MDIO User PHY Select Register 0 |
| 0x01E2 4088 | USERACCESS1 | MDIO User Access Register 1 |
| 0x01E2 408C | USERPHYSEL1 | MDIO User PHY Select Register 1 |
| 0x01E2 4090 - 0x01E2 47FF | – | Reserved |

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### 5.23.2 Management Data Input/Output (MDIO) Electrical Data/Timing

**Table 5-107. Timing Requirements for MDIO Input (see Figure 5-52 and Figure 5-53)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(MDCLK)}$ | Cycle time, MDCLK | 400 | | 400 | | ns |
| 2 | $t_{w(MDCLK)}$ | Pulse duration, MDCLK high/low | 180 | | 180 | | ns |
| 3 | $t_{t(MDCLK)}$ | Transition time, MDCLK | | 5 | | 5 | ns |
| 4 | $t_{su(MDIO-MDCLKH)}$ | Setup time, MDIO data input valid before MDCLK high | 16 | | 21 | | ns |
| 5 | $t_{h(MDCLKH-MDIO)}$ | Hold time, MDIO data input valid after MDCLK high | 0 | | 0 | | ns |

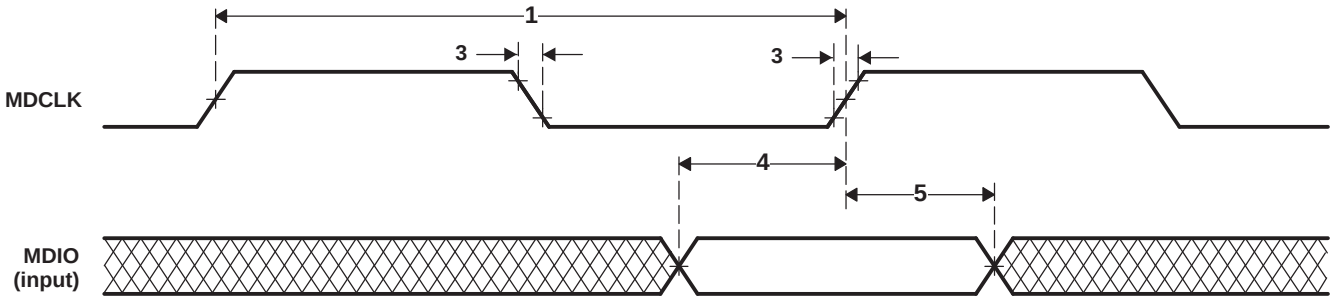


**Figure 5-52. MDIO Input Timing**

**Table 5-108. Switching Characteristics Over Recommended Operating Conditions for MDIO Output (see Figure 5-53)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 7 | $t_{d(MDCLKL-MDIO)}$ | Delay time, MDCLK low to MDIO data output valid | 0 | 100 | ns |

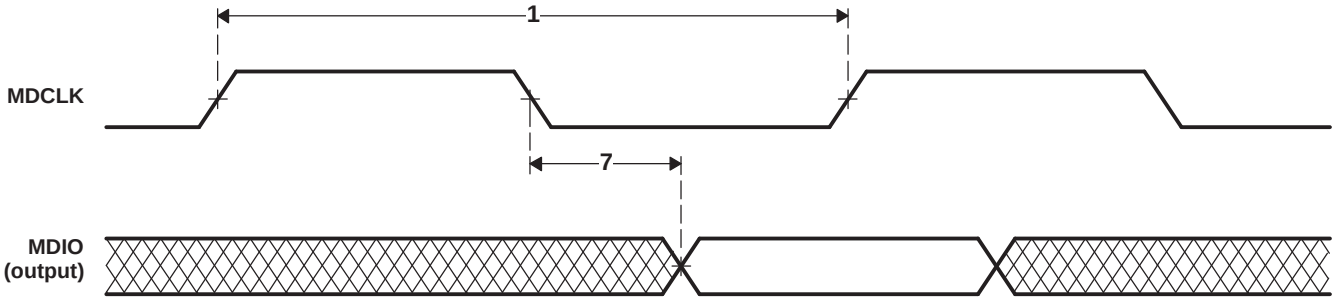


**Figure 5-53. MDIO Output Timing**


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## 5.24 LCD Controller (LCDC)

The LCD controller consists of two independent controllers, the Raster Controller and the LCD Interface Display Driver (LIDD) controller. Each controller operates independently from the other and only one of them is active at any given time.

- The Raster Controller handles the synchronous LCD interface. It provides timing and data for constant graphics refresh to a passive display. It supports a wide variety of monochrome and full-color display types and sizes by use of programmable timing controls, a built-in palette, and a gray-scale/serializer. Graphics data is processed and stored in frame buffers. A frame buffer is a contiguous memory block in the system. A built-in DMA engine supplies the graphics data to the Raster engine which, in turn, outputs to the external LCD device.
- The LIDD Controller supports the asynchronous LCD interface. It provides full-timing programmability of control signals (CS, WE, OE, ALE) and output data.

The maximum resolution for the LCD controller is 1024 x 1024 pixels. The maximum frame rate is determined by the image size in combination with the pixel clock rate. For details, see SPRAB93.

Table 5-109 lists the LCD Controller registers.

**Table 5-109. LCD Controller Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 3000 | REVID | LCD Revision Identification Register |
| 0x01E1 3004 | LCD_CTRL | LCD Control Register |
| 0x01E1 3008 | LCD_STAT | LCD Status Register |
| 0x01E1 300C | LIDD_CTRL | LCD LIDD Control Register |
| 0x01E1 3010 | LIDD_CS0_CONF | LCD LIDD CS0 Configuration Register |
| 0x01E1 3014 | LIDD_CS0_ADDR | LCD LIDD CS0 Address Read/Write Register |
| 0x01E1 3018 | LIDD_CS0_DATA | LCD LIDD CS0 Data Read/Write Register |
| 0x01E1 301C | LIDD_CS1_CONF | LCD LIDD CS1 Configuration Register |
| 0x01E1 3020 | LIDD_CS1_ADDR | LCD LIDD CS1 Address Read/Write Register |
| 0x01E1 3024 | LIDD_CS1_DATA | LCD LIDD CS1 Data Read/Write Register |
| 0x01E1 3028 | RASTER_CTRL | LCD Raster Control Register |
| 0x01E1 302C | RASTER_TIMING_0 | LCD Raster Timing 0 Register |
| 0x01E1 3030 | RASTER_TIMING_1 | LCD Raster Timing 1 Register |
| 0x01E1 3034 | RASTER_TIMING_2 | LCD Raster Timing 2 Register |
| 0x01E1 3038 | RASTER_SUBPANEL | LCD Raster Subpanel Display Register |
| 0x01E1 3040 | LCDDMA_CTRL | LCD DMA Control Register |
| 0x01E1 3044 | LCDDMA_FB0_BASE | LCD DMA Frame Buffer 0 Base Address Register |
| 0x01E1 3048 | LCDDMA_FB0_CEILING | LCD DMA Frame Buffer 0 Ceiling Address Register |
| 0x01E1 304C | LCDDMA_FB1_BASE | LCD DMA Frame Buffer 1 Base Address Register |
| 0x01E1 3050 | LCDDMA_FB1_CEILING | LCD DMA Frame Buffer 1 Ceiling Address Register |

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### 5.24.1 LCD Interface Display Driver (LIDD Mode)

**Table 5-110. Timing Requirements for LCD LIDD Mode**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 16 | $t_{su(LCD_D)}$ | Setup time, LCD_D[15:0] valid before LCD_CLK (SYSCLK2) high | 7 | | 8 | | ns |
| 17 | $t_{h(LCD_D)}$ | Hold time, LCD_D[15:0] valid after LCD_CLK (SYSCLK2) high | 0 | | 0 | | ns |

**Table 5-111. Switching Characteristics Over Recommended Operating Conditions for LCD LIDD Mode**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 4 | $t_{d(LCD_D_V)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] valid (write) | 0 | 7 | 0 | 9 | ns |
| 5 | $t_{d(LCD_D_I)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] invalid (write) | 0 | 7 | 0 | 9 | ns |
| 6 | $t_{d(LCD_E_A)}$ | Delay time, LCD_CLK (SYSCLK2) high to $\overline{\text{LCD_AC_ENB_CS}}$ low | 0 | 7 | 0 | 9 | ns |
| 7 | $t_{d(LCD_E_I)}$ | Delay time, LCD_CLK (SYSCLK2) high to $\overline{\text{LCD_AC_ENB_CS}}$ high | 0 | 7 | 0 | 9 | ns |
| 8 | $t_{d(LCD_A_A)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_VSYNC low | 0 | 7 | 0 | 9 | ns |
| 9 | $t_{d(LCD_A_I)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_VSYNC high | 0 | 7 | 0 | 9 | ns |
| 10 | $t_{d(LCD_W_A)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_HSYNC low | 0 | 7 | 0 | 9 | ns |
| 11 | $t_{d(LCD_W_I)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_HSYNC high | 0 | 7 | 0 | 9 | ns |
| 12 | $t_{d(LCD_STRB_A)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_PCLK active | 0 | 7 | 0 | 9 | ns |
| 13 | $t_{d(LCD_STRB_I)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_PCLK inactive | 0 | 7 | 0 | 9 | ns |
| 14 | $t_{d(LCD_D_Z)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] in 3-state | 0 | 7 | 0 | 9 | ns |
| 15 | $t_{d(Z_LCD_D)}$ | Delay time, LCD_CLK (SYSCLK2) high to LCD_D[15:0] (valid from 3-state) | 0 | 7 | 0 | 9 | ns |

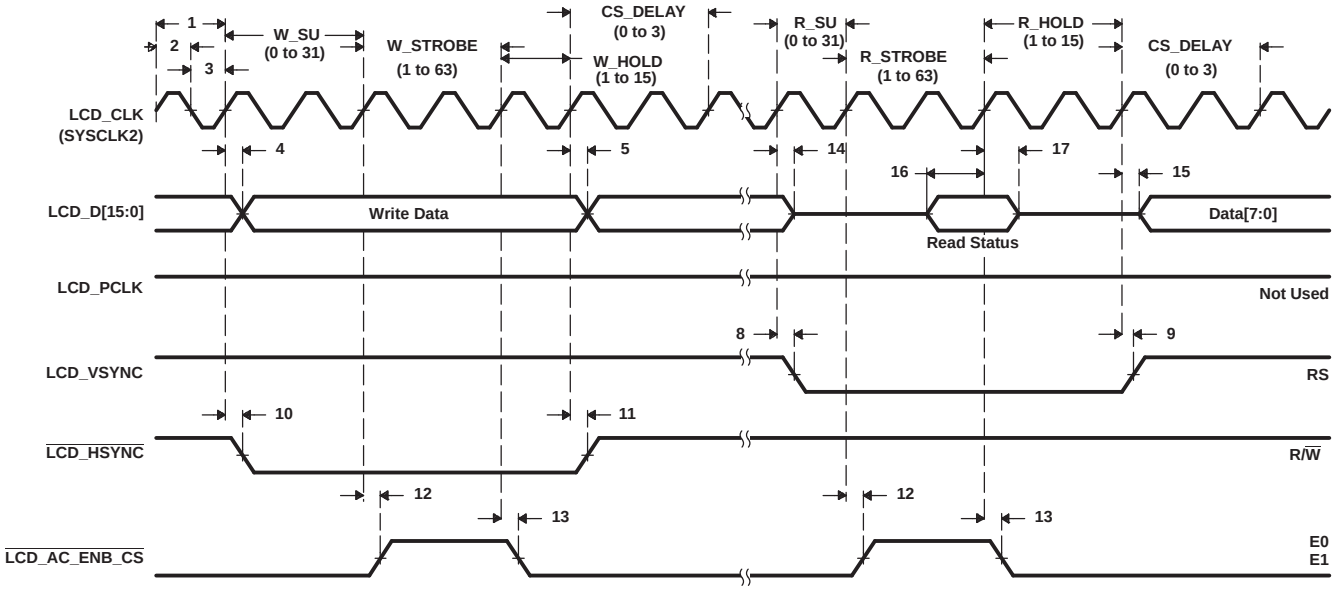


**Figure 5-54. Character Display HD44780 Write**


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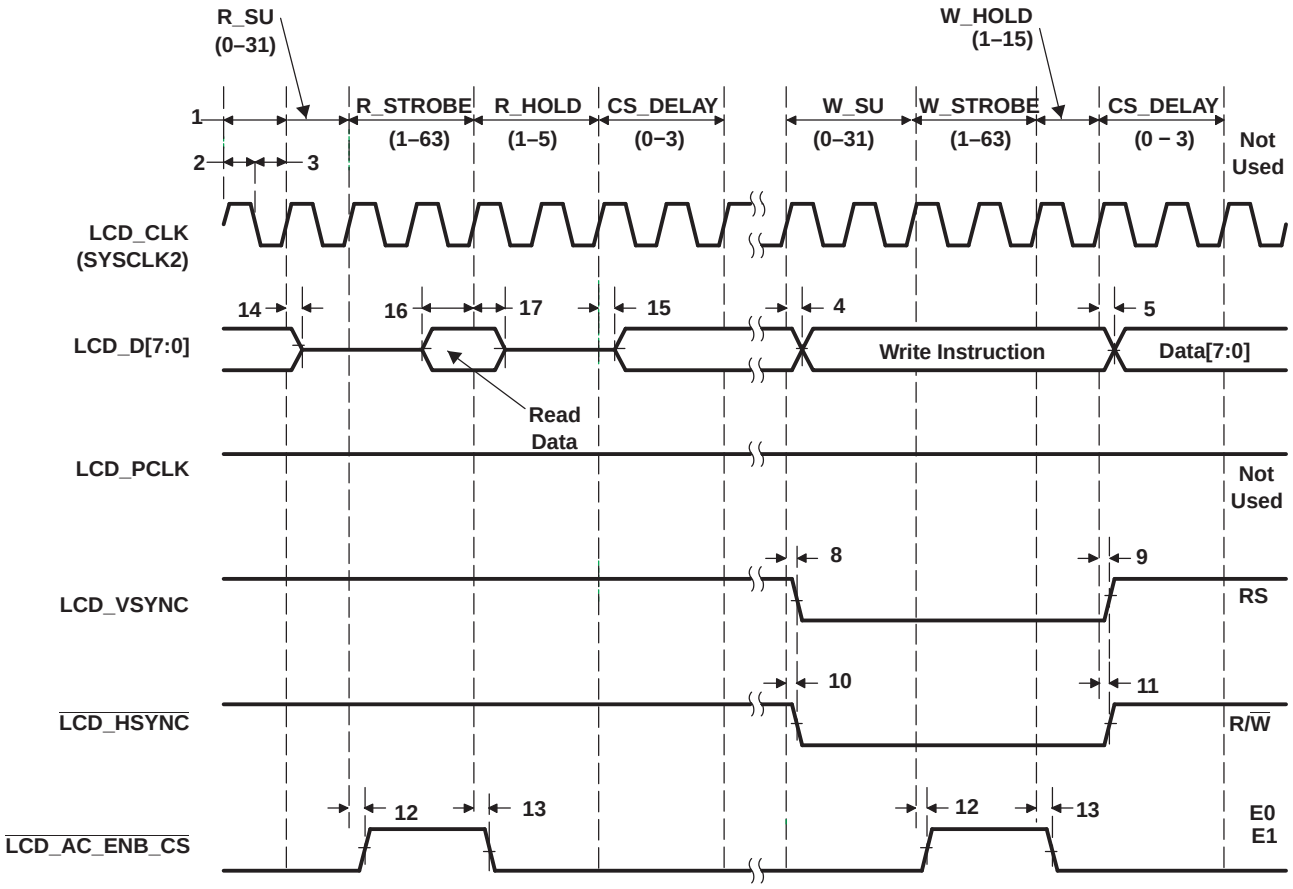


**Figure 5-55. Character Display HD44780 Read**

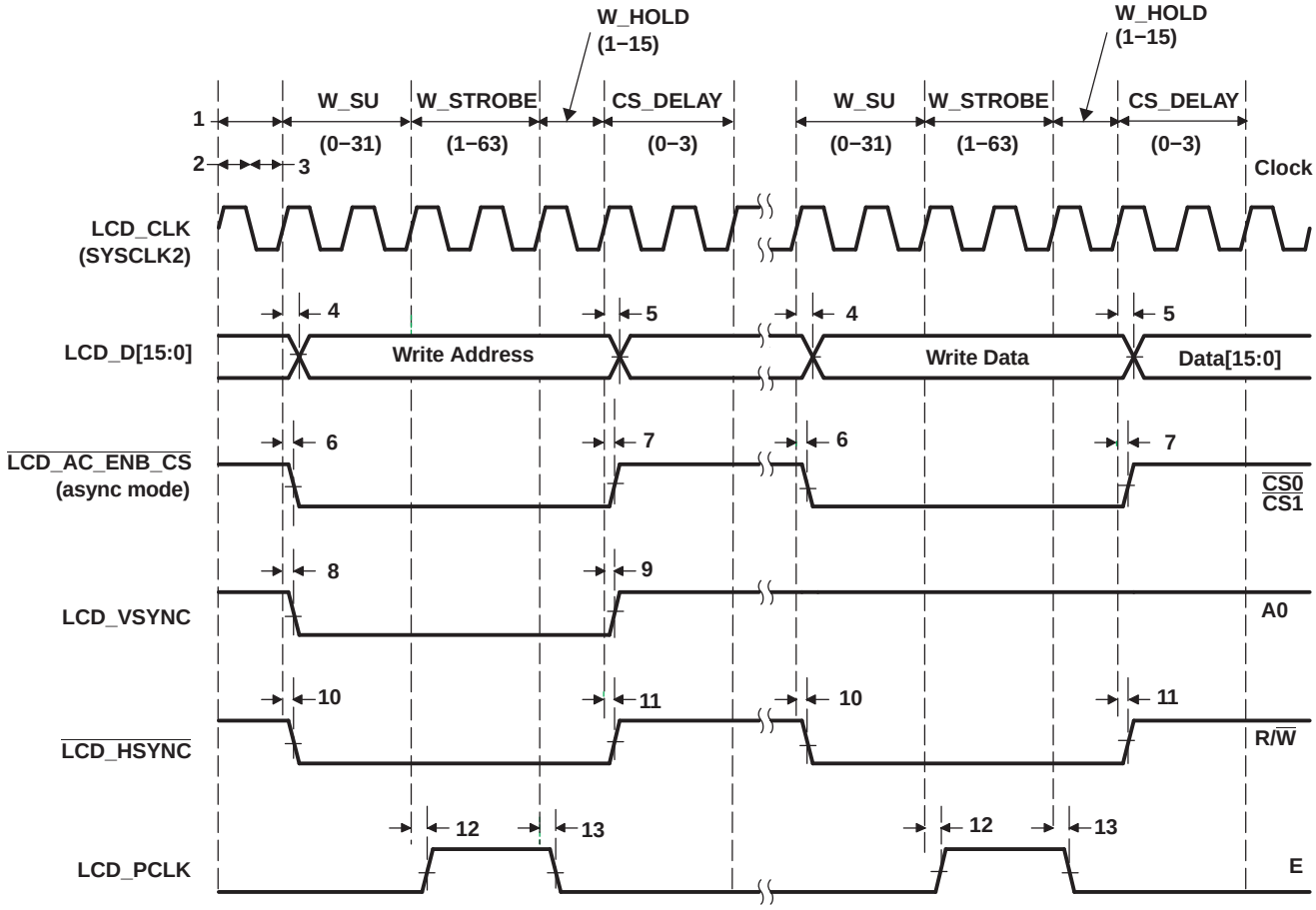


**Figure 5-56. Micro-Interface Graphic Display 6800 Write**


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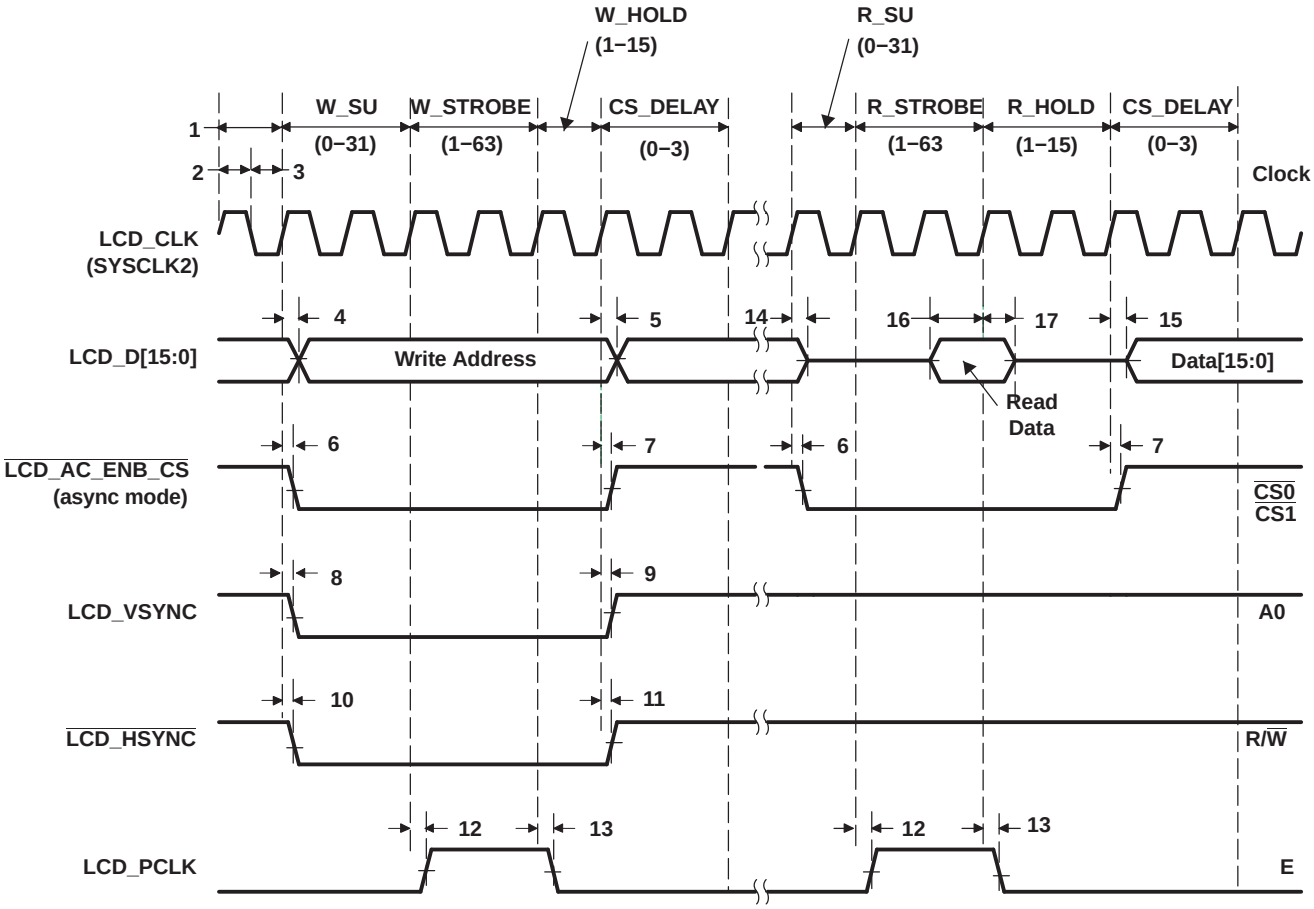


**Figure 5-57. Micro-Interface Graphic Display 6800 Read**

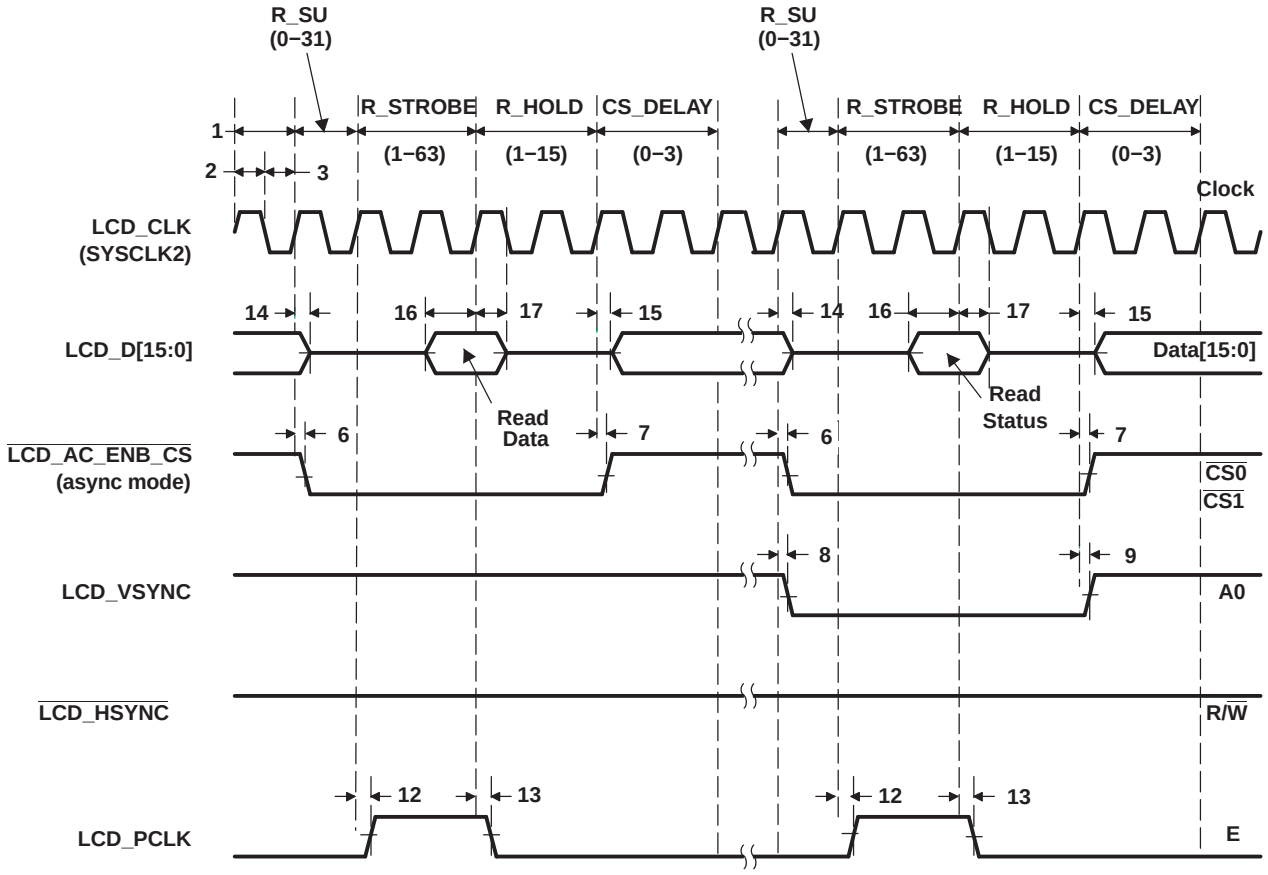


**Figure 5-58. Micro-Interface Graphic Display 6800 Status**


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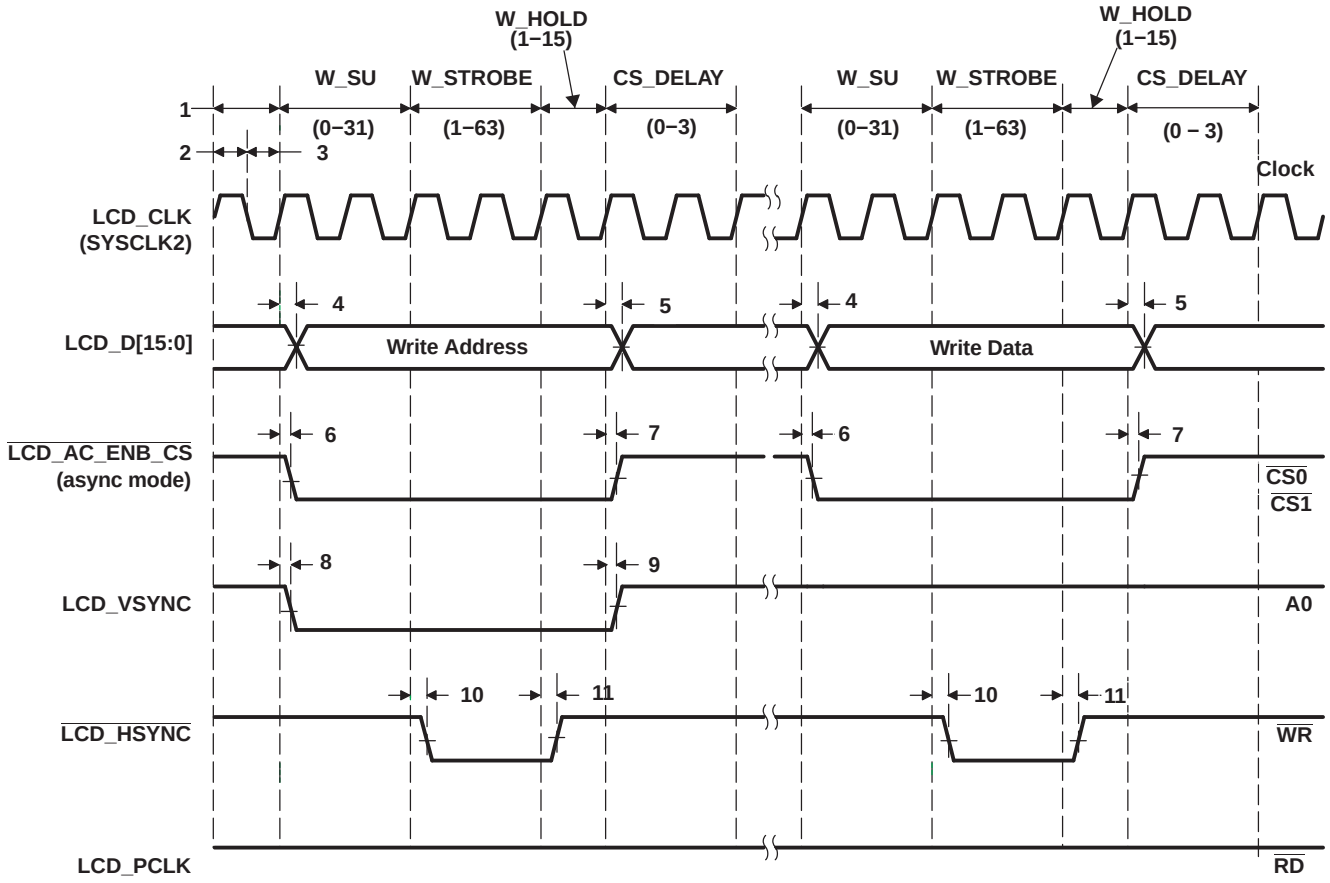


**Figure 5-59. Micro-Interface Graphic Display 8080 Write**

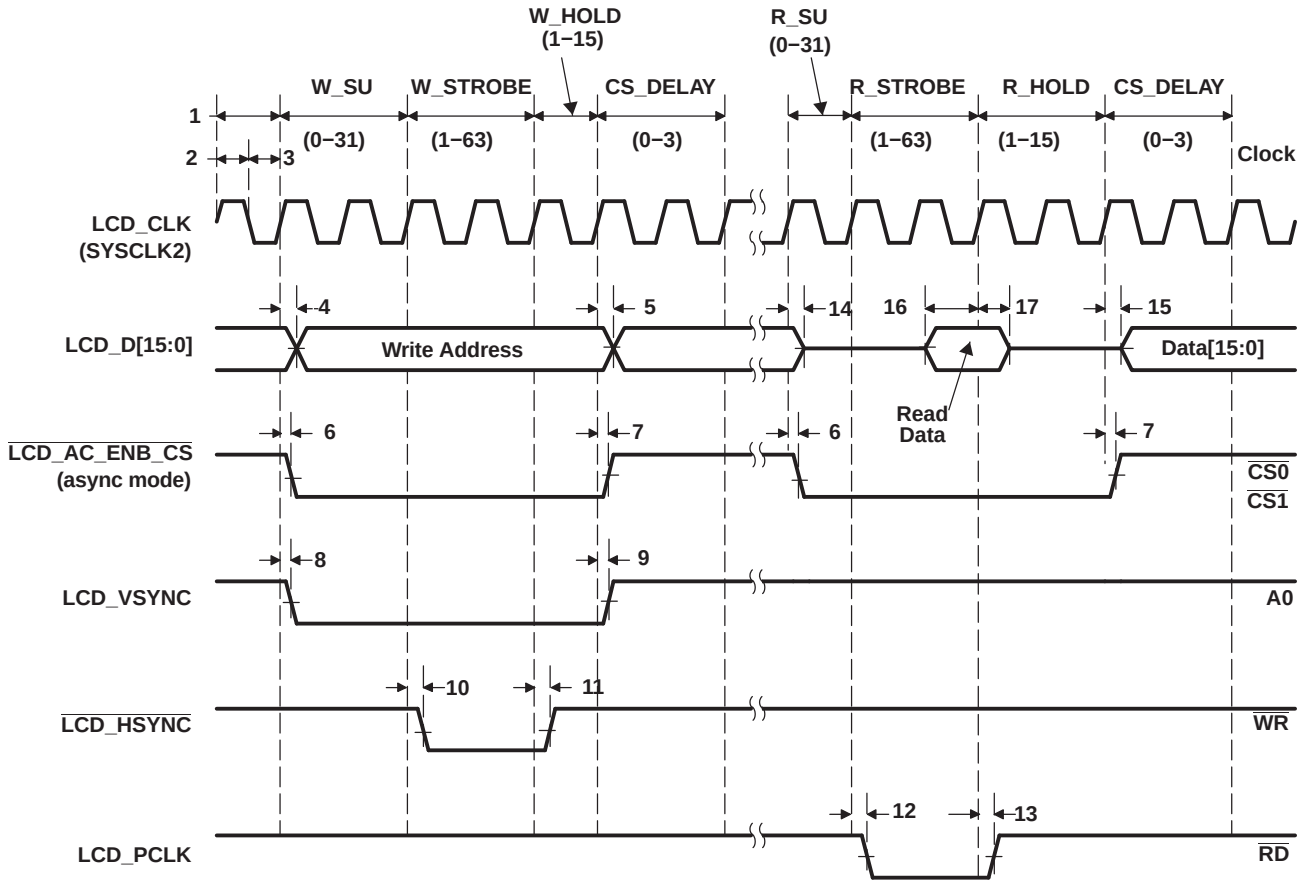


**Figure 5-60. Micro-Interface Graphic Display 8080 Read**


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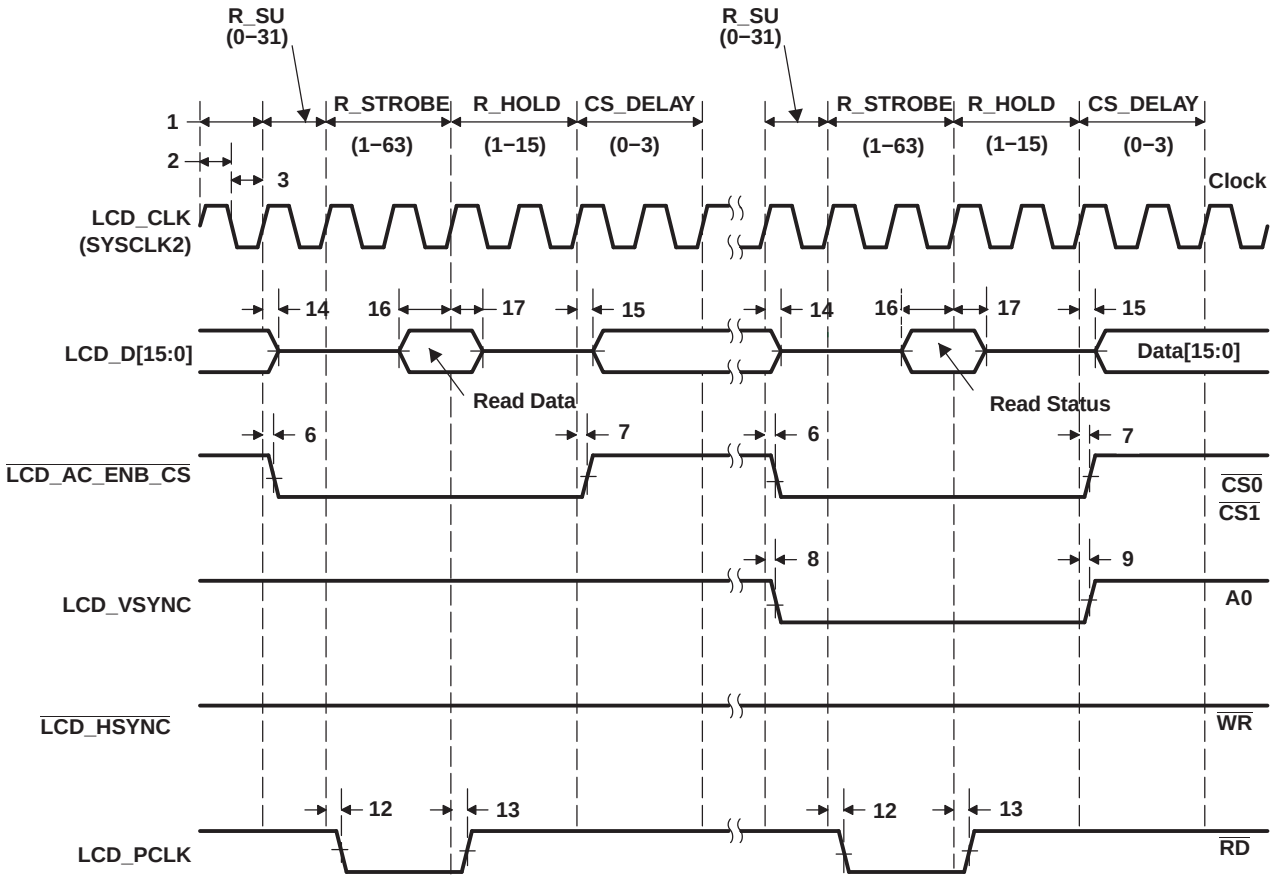


**Figure 5-61. Micro-Interface Graphic Display 8080 Status**

### 5.24.2 LCD Raster Mode

**Table 5-112. Switching Characteristics Over Recommended Operating Conditions for LCD Raster Mode**

See Figure 5-62 through Figure 5-66

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(PIXEL_CLK)}$ | Cycle time, pixel clock | 26.66 | | 33.33 | | ns |
| 2 | $t_{w(PIXEL_CLK_H)}$ | Pulse duration, pixel clock high | 10 | | 10 | | ns |
| 3 | $t_{w(PIXEL_CLK_L)}$ | Pulse duration, pixel clock low | 10 | | 10 | | ns |
| 4 | $t_{d(LCD_D_V)}$ | Delay time, LCD_PCLK high to LCD_D[15:0] valid (write) | 0 | 7 | 0 | 9 | ns |
| 5 | $t_{d(LCD_D_IV)}$ | Delay time, LCD_PCLK high to LCD_D[15:0] invalid (write) | 0 | 7 | 0 | 9 | ns |
| 6 | $t_{d(\overline{LCD_AC_ENB_CS_A})}$ | Delay time, LCD_PCLK low to $\overline{LCD_AC_ENB_CS}$ high | 0 | 7 | 0 | 9 | ns |
| 7 | $t_{d(\overline{LCD_AC_ENB_CS_I})}$ | Delay time, LCD_PCLK low to $\overline{LCD_AC_ENB_CS}$ low | 0 | 7 | 0 | 9 | ns |
| 8 | $t_{d(LCD_VSYNC_A)}$ | Delay time, LCD_PCLK low to LCD_VSYNC high | 0 | 7 | 0 | 9 | ns |
| 9 | $t_{d(LCD_VSYNC_I)}$ | Delay time, LCD_PCLK low to LCD_VSYNC low | 0 | 7 | 0 | 9 | ns |
| 10 | $t_{d(LCD_HSYNC_A)}$ | Delay time, LCD_PCLK high to LCD_HSYNC high | 0 | 7 | 0 | 9 | ns |
| 11 | $t_{d(LCD_HSYNC_I)}$ | Delay time, LCD_PCLK high to LCD_HSYNC low | 0 | 7 | 0 | 9 | ns |

Frame-to-frame timing is derived through the following parameters in the LCD (RASTER_TIMING_1) register:

- Vertical front porch (VFP)
- Vertical sync pulse width (VSW)
- Vertical back porch (VBP)
- Lines per panel (LPP)

Line-to-line timing is derived through the following parameters in the LCD (RASTER_TIMING_0) register:

- Horizontal front porch (HFP)
- Horizontal sync pulse width (HSW)
- Horizontal back porch (HBP)
- Pixels per panel (PPL)

$\overline{LCD_AC_ENB_CS}$ timing is derived through the following parameter in the LCD (RASTER_TIMING_2) register:

- AC bias frequency (ACB)

The display format produced in raster mode is shown in Figure 5-62. An entire frame is delivered one line at a time. The first line delivered starts at data pixel (1, 1) and ends at data pixel (P, 1). The last line delivered starts at data pixel (1, L) and ends at data pixel (P, L). The beginning of each new frame is denoted by the activation of I/O signal LCD_VSYNC. The beginning of each new line is denoted by the activation of I/O signal LCD_HSYNC.


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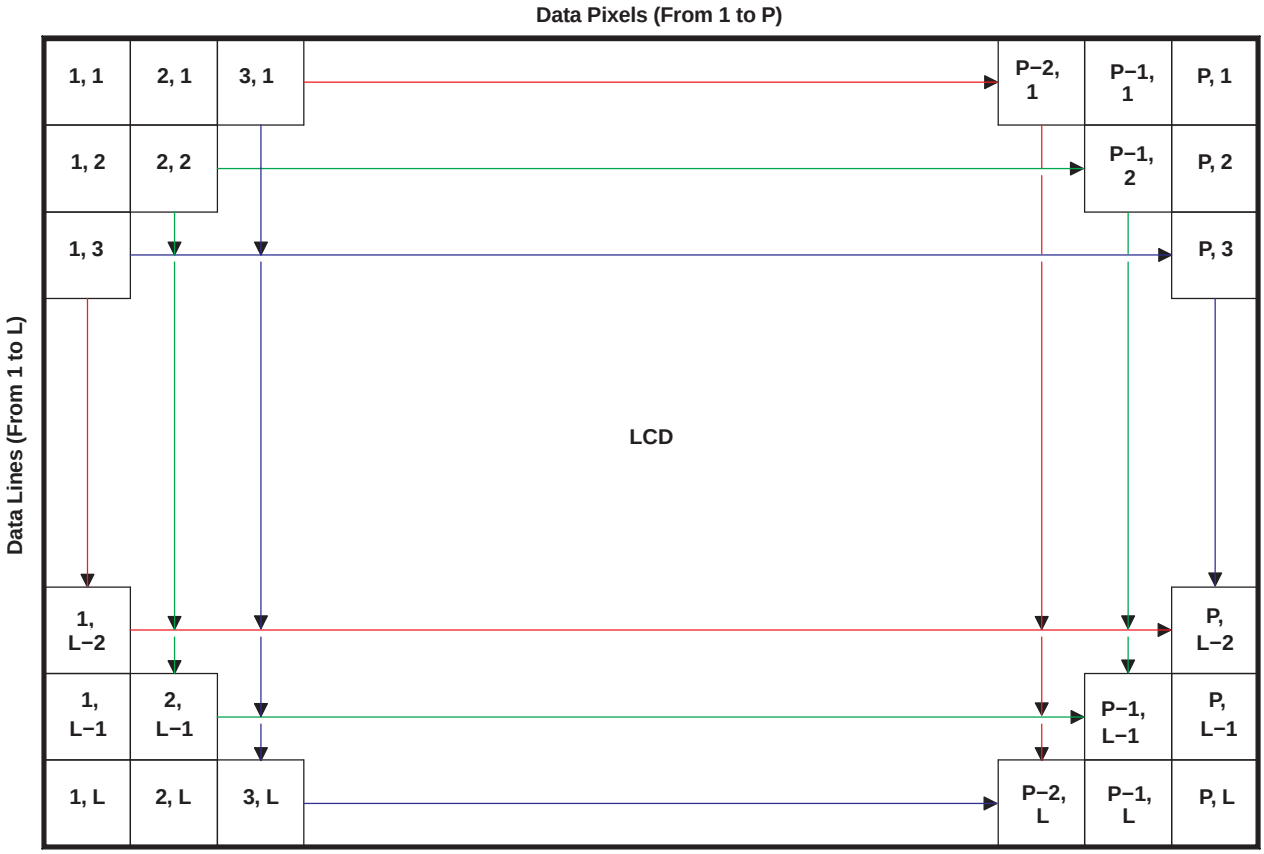


**Figure 5-62. LCD Raster-Mode Display Format**

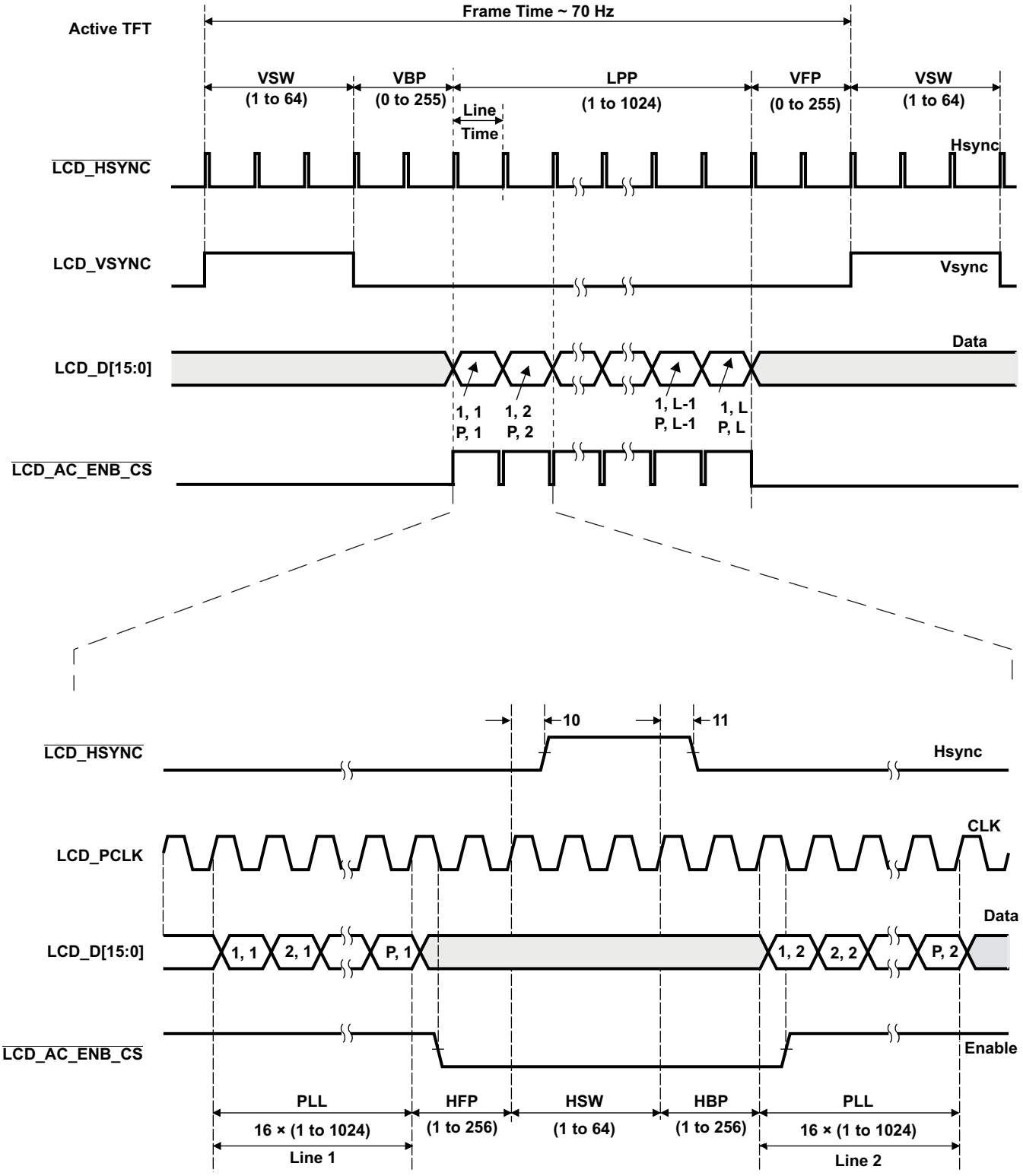


**Figure 5-63. LCD Raster-Mode Active**


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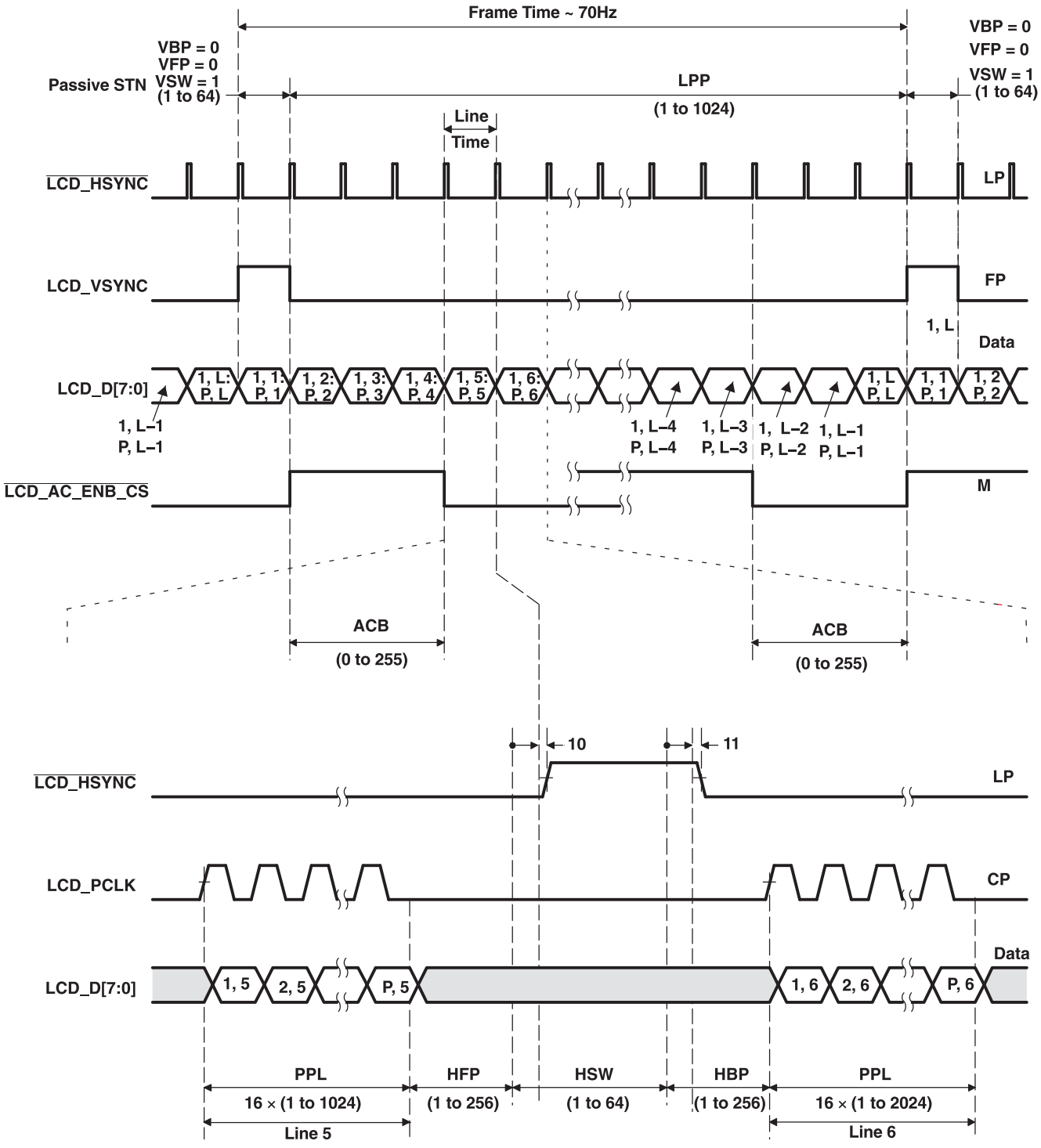


**Figure 5-64. LCD Raster-Mode Passive**

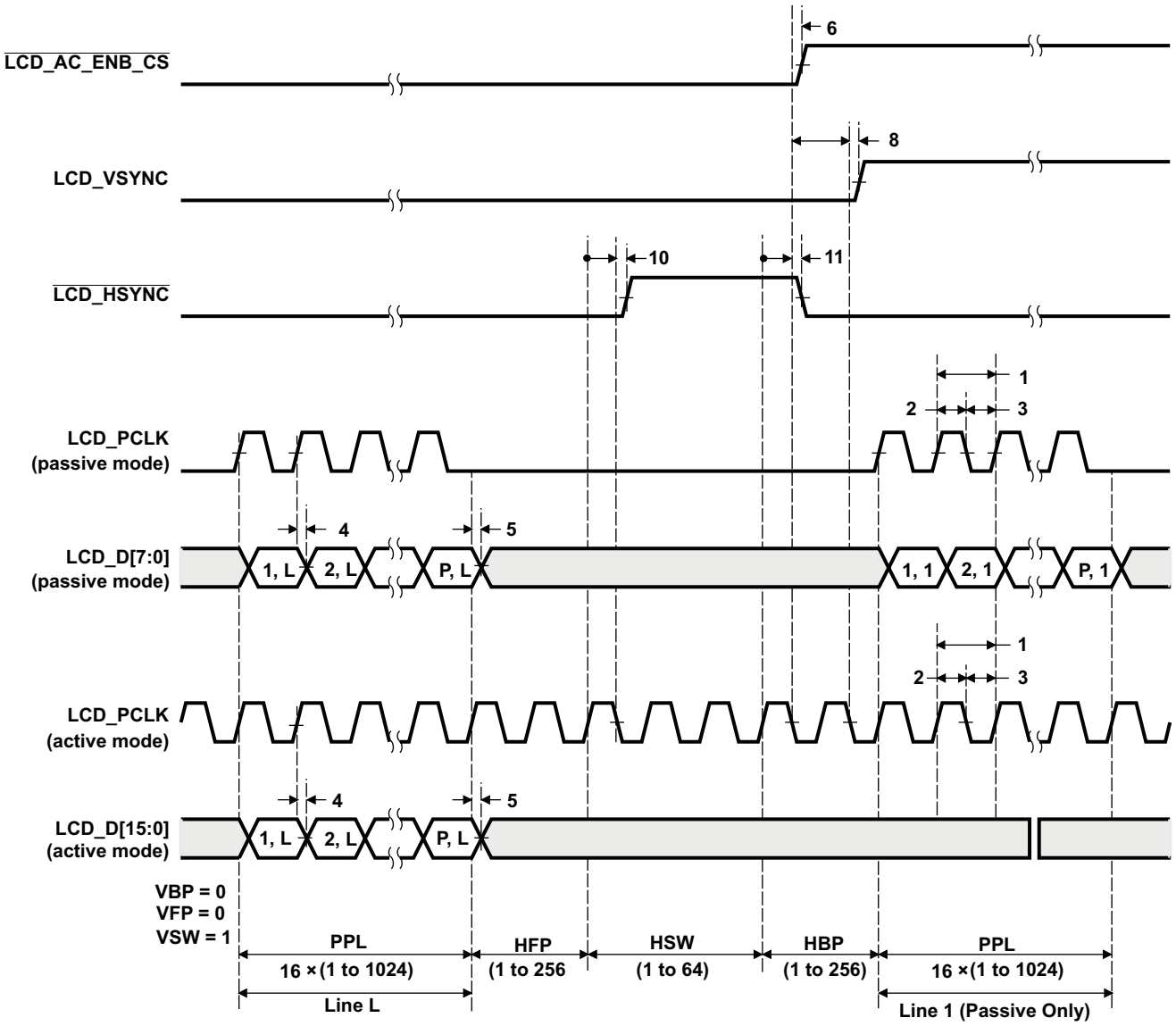


**Figure 5-65. LCD Raster-Mode Control Signal Activation**


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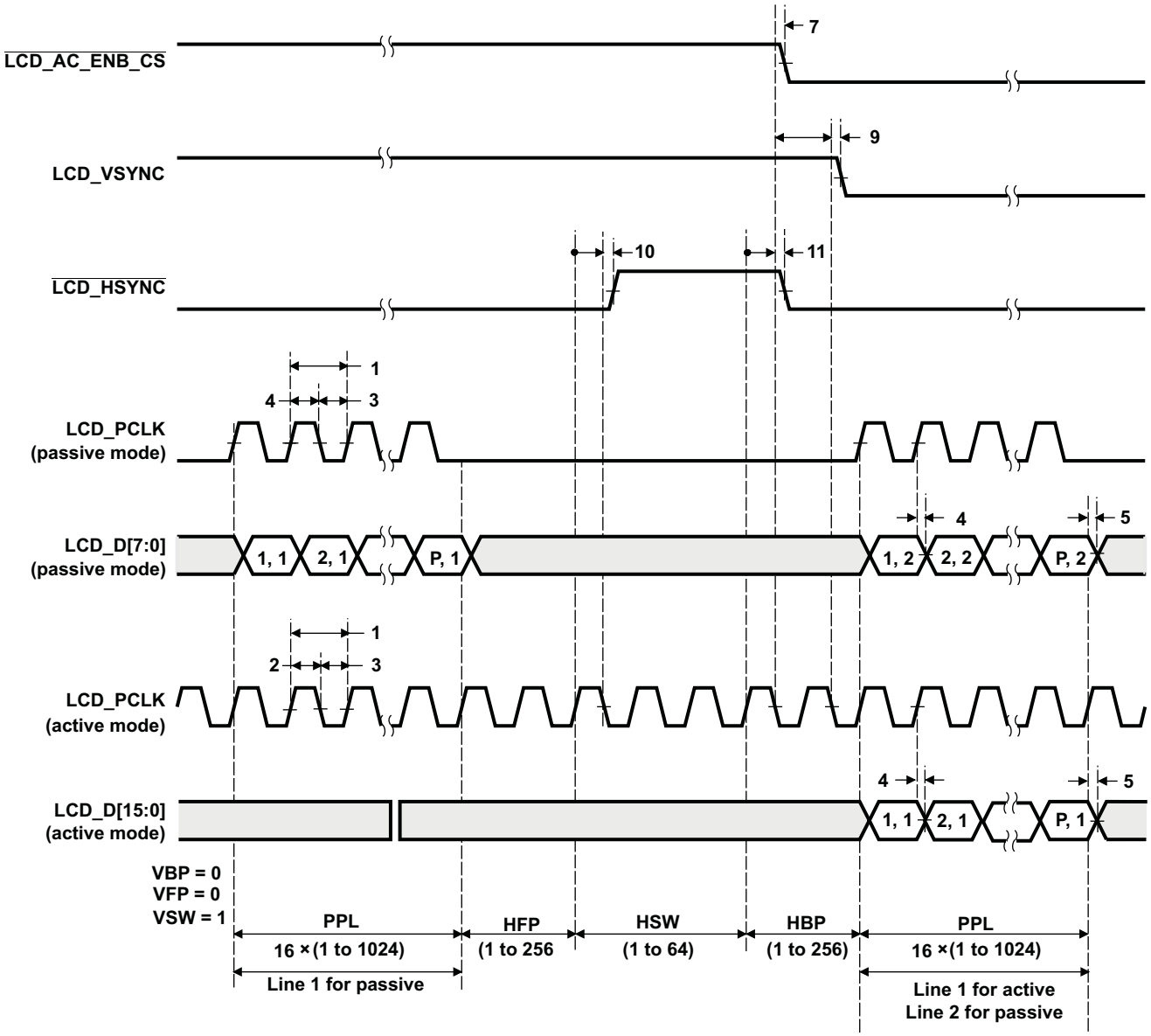


**Figure 5-66. LCD Raster-Mode Control Signal Deactivation**

## 5.25 Host-Port Interface (UHPI)

### 5.25.1 HPI Device-Specific Information

The device includes a user-configurable 16-bit Host-port interface (HPI16).

The host port interface (UHPI) provides a parallel port interface through which an external host processor can directly access the processor's resources (configuration and program/data memories). The external host device is asynchronous to the CPU clock and functions as a master to the HPI interface. The UHPI enables a host device and the processor to exchange information via internal or external memory. Dedicated address (HPIA) and data (HPID) registers within the UHPI provide the data path between the external host interface and the processor resources. A UHPI control register (HPIC) is available to the host and the CPU for various configuration and interrupt functions.

### 5.25.2 HPI Peripheral Register Description(s)

**Table 5-113. HPI Control Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | COMMENTS |
|---|---|---|---|
| 0x01E1 0000 | PID | Peripheral Identification Register | |
| 0x01E1 0004 | PWREMU_MGMT | HPI power and emulation management register | The CPU has read/write access to the PWREMU_MGMT register. |
| 0x01E1 0008 | - | Reserved | |
| 0x01E1 000C | GPIO_EN | General Purpose IO Enable Register | |
| 0x01E1 0010 | GPIO_DIR1 | General Purpose IO Direction Register 1 | |
| 0x01E1 0014 | GPIO_DAT1 | General Purpose IO Data Register 1 | |
| 0x01E1 0018 | GPIO_DIR2 | General Purpose IO Direction Register 2 | |
| 0x01E1 001C | GPIO_DAT2 | General Purpose IO Data Register 2 | |
| 0x01E1 0020 | GPIO_DIR3 | General Purpose IO Direction Register 3 | |
| 0x01E1 0024 | GPIO_DAT3 | General Purpose IO Data Register 3 | |
| 01E1 0028 | - | Reserved | |
| 01E1 002C | - | Reserved | |
| 01E1 0030 | HPIC | HPI control register | The Host and the CPU both have read/write access to the HPIC register. |
| 01E1 0034 | HPIA (HPIAW)(1) | HPI address register (Write) | The Host has read/write access to the HPIA registers. The CPU has only read access to the HPIA registers. |
| 01E1 0038 | HPIA (HPIAR)(1) | HPI address register (Read) | |
| 01E1 000C - 01E1 07FF | - | Reserved | |

(1) There are two 32-bit HPIA registers: HPIAR for read operations and HPIAW for write operations. The HPI can be configured such that HPIAR and HPIAW act as a single 32-bit HPIA (single-HPIA mode) or as two separate 32-bit HPIAs (dual-HPIA mode) from the perspective of the Host. The CPU can access HPIAW and HPIAR independently.


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### 5.25.3 HPI Electrical Data/Timing

**Table 5-114. Timing Requirements for Host-Port Interface [1.2V, 1.1V][1] [2]**

| NO. | | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{su(SELV-HSTBL)}$ | Setup time, select signals[3] valid before $\overline{\text{UHPI_HSTROBE}}$ low | 5 | | ns |
| 2 | $t_{h(HSTBL-SELV)}$ | Hold time, select signals[3] valid after $\overline{\text{UHPI_HSTROBE}}$ low | 2 | | ns |
| 3 | $t_{w(HSTBL)}$ | Pulse duration, $\overline{\text{UHPI_HSTROBE}}$ active low | 15 | | ns |
| 4 | $t_{w(HSTBH)}$ | Pulse duration, $\overline{\text{UHPI_HSTROBE}}$ inactive high between consecutive accesses | 2M | | ns |
| 9 | $t_{su(SELV-HASL)}$ | Setup time, selects signals valid before $\overline{\text{UHPI_HAS}}$ low | 5 | | ns |
| 10 | $t_{h(HASL-SELV)}$ | Hold time, select signals valid after $\overline{\text{UHPI_HAS}}$ low | 2 | | ns |
| 11 | $t_{su(HDV-HSTBH)}$ | Setup time, host data valid before $\overline{\text{UHPI_HSTROBE}}$ high | 5 | | ns |
| 12 | $t_{h(HSTBH-HDV)}$ | Hold time, host data valid after $\overline{\text{UHPI_HSTROBE}}$ high | 2 | | ns |
| 13 | $t_{h(HRDYL-HSTBH)}$ | Hold time, $\overline{\text{UHPI_HSTROBE}}$ high after $\overline{\text{UHPI_HRDY}}$ low. $\overline{\text{UHPI_HSTROBE}}$ should not be inactivated until $\overline{\text{UHPI_HRDY}}$ is active (low); otherwise, HPI writes will not complete properly. | 2 | | ns |
| 16 | $t_{su(HASL-HSTBL)}$ | Setup time, $\overline{\text{UHPI_HAS}}$ low before $\overline{\text{UHPI_HSTROBE}}$ low | 5 | | ns |
| 17 | $t_{h(HSTBL-HASH)}$ | Hold time, $\overline{\text{UHPI_HAS}}$ low after $\overline{\text{UHPI_HSTROBE}}$ low | 2 | | ns |

(1) $\overline{\text{UHPI_HSTROBE}}$ refers to the following logical operation on $\overline{\text{UHPI_HCS}}$, $\overline{\text{UHPI_HDS1}}$, and $\overline{\text{UHPI_HDS2}}$: [NOT($\overline{\text{UHPI_HDS1}}$ XOR $\overline{\text{UHPI_HDS2}}$)] OR $\overline{\text{UHPI_HCS}}$.
(2) M=SYSCLK2 period in ns.
(3) Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$ and HHWIL.

**Table 5-115. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface [1.3V, 1.2V, 1.1V](1) (2) (3)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| 5 | $t_{d(HSTBL-HRDYV)}$ | Delay time, HSTROBE low to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: Back-to-back HPIA writes (can be either first or second half-word)<br>*Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word)<br>*Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word)<br>*Case 4*: HPIA write and Write FIFO not empty<br><br>For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions:<br>*Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access)<br>*Case 2*: First half-word access of HPID Read without auto-increment<br>For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions:<br>*Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access)<br>*Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access)<br>*Case 3*: HPIC or HPIA read (applies to either half-word access) | | 15 | | 17 | ns |
| 5a | $t_{d(HASL-HRDYV)}$ | Delay time, HAS low to HRDY valid | | | 15 | | 17 | ns |
| 6 | $t_{en(HSTBL-HDLZ)}$ | Enable time, HD driven from HSTROBE low | | 1.5 | | 1.5 | | ns |
| 7 | $t_{d(HRDYL-HDV)}$ | Delay time, HRDY low to HD valid | | | 0 | | 0 | ns |
| 8 | $t_{oh(HSTBH-HDV)}$ | Output hold time, HD valid after HSTROBE high | | 1.5 | | 1.5 | | ns |
| 14 | $t_{dis(HSTBH-HDHZ)}$ | Disable time, HD high-impedance from HSTROBE high | | | 15 | | 17 | ns |
| 15 | $t_{d(HSTBL-HDV)}$ | Delay time, HSTROBE low to HD valid | For HPI Read. Applies to conditions where data is already residing in HPID/FIFO:<br>*Case 1*: HPIC or HPIA read<br>*Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO<br>*Case 3*: Second half-word of HPID read with or without auto-increment | | 15 | | 17 | ns |
| 18 | $t_{d(HSTBH-HRDYV)}$ | Delay time, HSTROBE high to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: HPID write when Write FIFO is full (can happen to either half-word)<br>*Case 2*: HPIA write (can happen to either half-word)<br>*Case 3*: HPID write without auto-increment (only happens to second half-word) | | 15 | | 17 | ns |

(1) M=SYSCLK2 period in ns.
(2) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(3) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).


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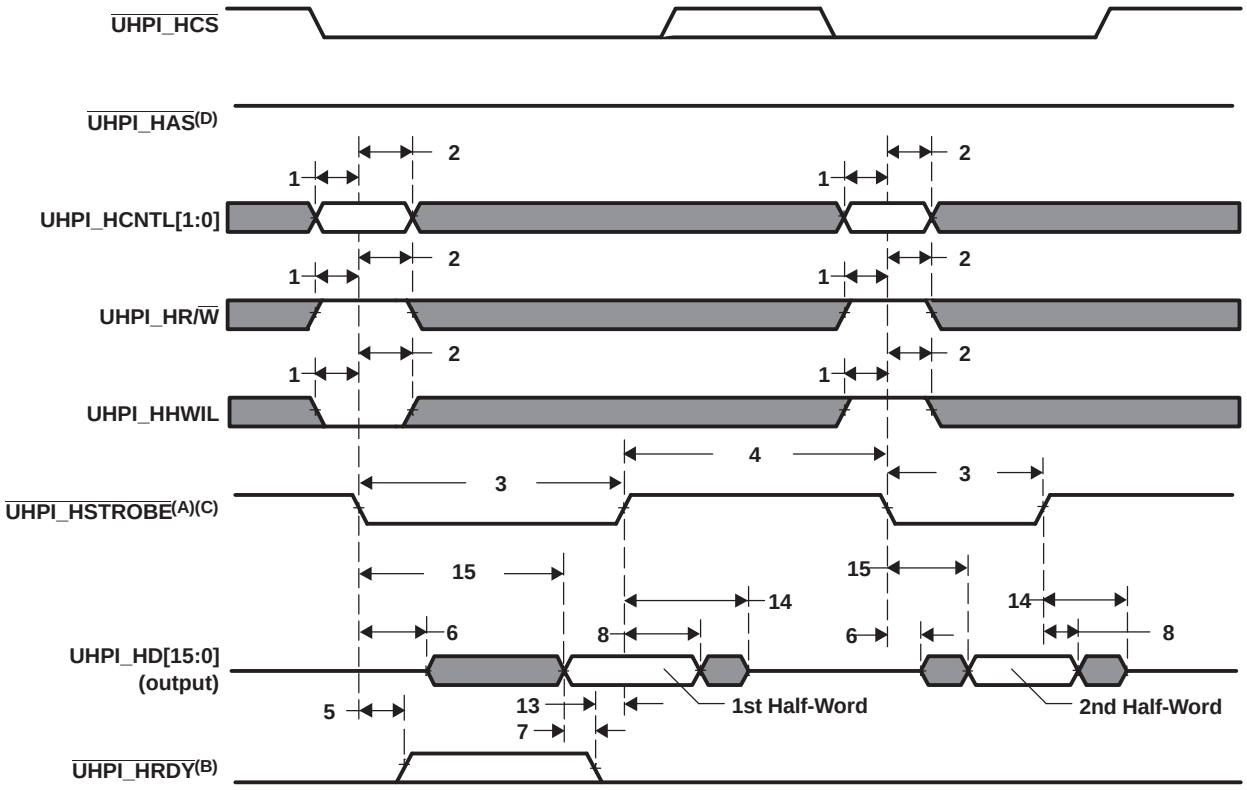
**Table 5-116. Switching Characteristics Over Recommended Operating Conditions for Host-Port Interface [1.0V](1) (2) (3)**

| NO. | PARAMETER | | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|
| | | | | MIN | MAX | |
| 5 | $t_{d(HSTBL-HRDYV)}$ | Delay time, HSTROBE low to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: Back-to-back HPIA writes (can be either first or second half-word)<br>*Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word)<br>*Case 3*: HPID write when FIFO is full or flushing (can be either first or second half-word)<br>*Case 4*: HPIA write and Write FIFO not empty<br><br>For HPI Read, HRDY can go high (*not ready*) for these HPI Read conditions:<br>*Case 1*: HPID read (with auto-increment) and data not in Read FIFO (can only happen to first half-word of HPID access)<br>*Case 2*: First half-word access of HPID Read without auto-increment<br>For HPI Read, HRDY stays low (*ready*) for these HPI Read conditions:<br>*Case 1*: HPID read with auto-increment and data is already in Read FIFO (applies to either half-word of HPID access)<br>*Case 2*: HPID read without auto-increment and data is already in Read FIFO (always applies to second half-word of HPID access)<br>*Case 3*: HPIC or HPIA read (applies to either half-word access) | | 22 | ns |
| 5a | $t_{d(HASL-HRDYV)}$ | Delay time, HAS low to HRDY valid | | | 22 | ns |
| 6 | $t_{en(HSTBL-HDLZ)}$ | Enable time, HD driven from HSTROBE low | | 1.5 | | ns |
| 7 | $t_{d(HRDYL-HDV)}$ | Delay time, HRDY low to HD valid | | | 0 | ns |
| 8 | $t_{oh(HSTBH-HDV)}$ | Output hold time, HD valid after HSTROBE high | | 1.5 | | ns |
| 14 | $t_{dis(HSTBH-HDHZ)}$ | Disable time, HD high-impedance from HSTROBE high | | | 22 | ns |
| 15 | $t_{d(HSTBL-HDV)}$ | Delay time, HSTROBE low to HD valid | For HPI Read. Applies to conditions where data is already residing in HPID/FIFO:<br>*Case 1*: HPIC or HPIA read<br>*Case 2*: First half-word of HPID read with auto-increment and data is already in Read FIFO<br>*Case 3*: Second half-word of HPID read with or without auto-increment | | 22 | ns |
| 18 | $t_{d(HSTBH-HRDYV)}$ | Delay time, HSTROBE high to HRDY valid | For HPI Write, HRDY can go high (*not ready*) for these HPI Write conditions; otherwise, HRDY stays low (*ready*):<br>*Case 1*: HPID write when Write FIFO is full (can happen to either half-word)<br>*Case 2*: HPIA write (can happen to either half-word)<br>*Case 3*: HPID write without auto-increment (only happens to second half-word) | | 22 | ns |

(1) M=SYSCLK2 period in ns.
(2) HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT(HDS1 XOR HDS2)] OR HCS.
(3) By design, whenever HCS is driven inactive (high), HPI will drive HRDY active (low).




A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing)and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.
C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE.
D The diagram above assumes UHPI_HAS has been pulled high.

**Figure 5-67. UHPI Read Timing (HAS Not Used, Tied High)**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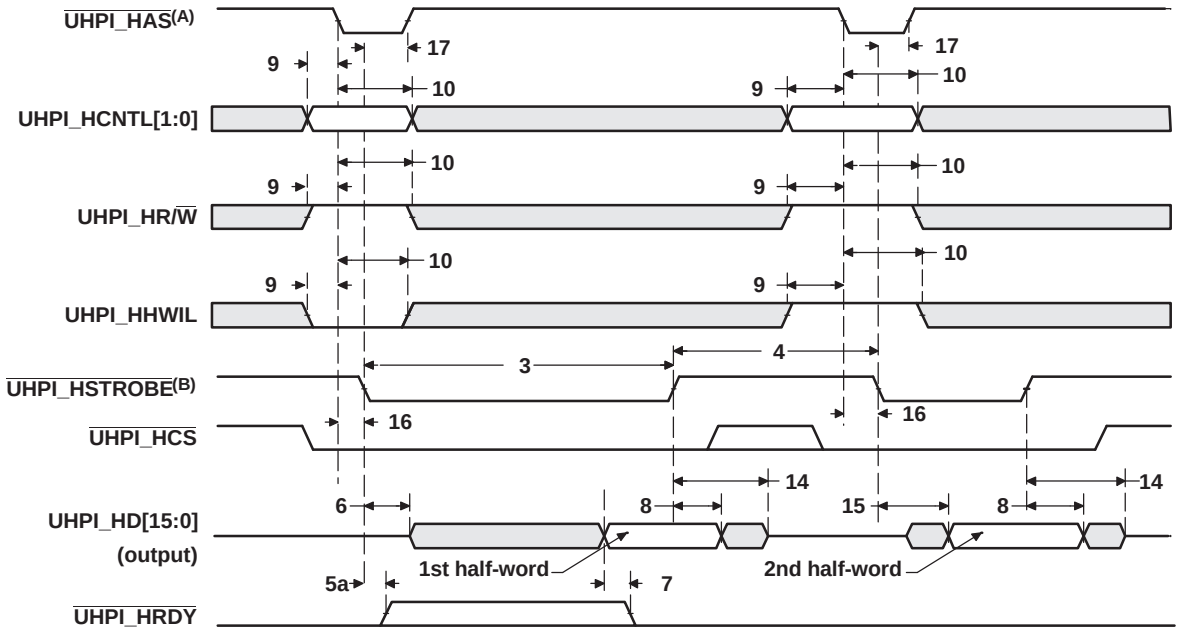
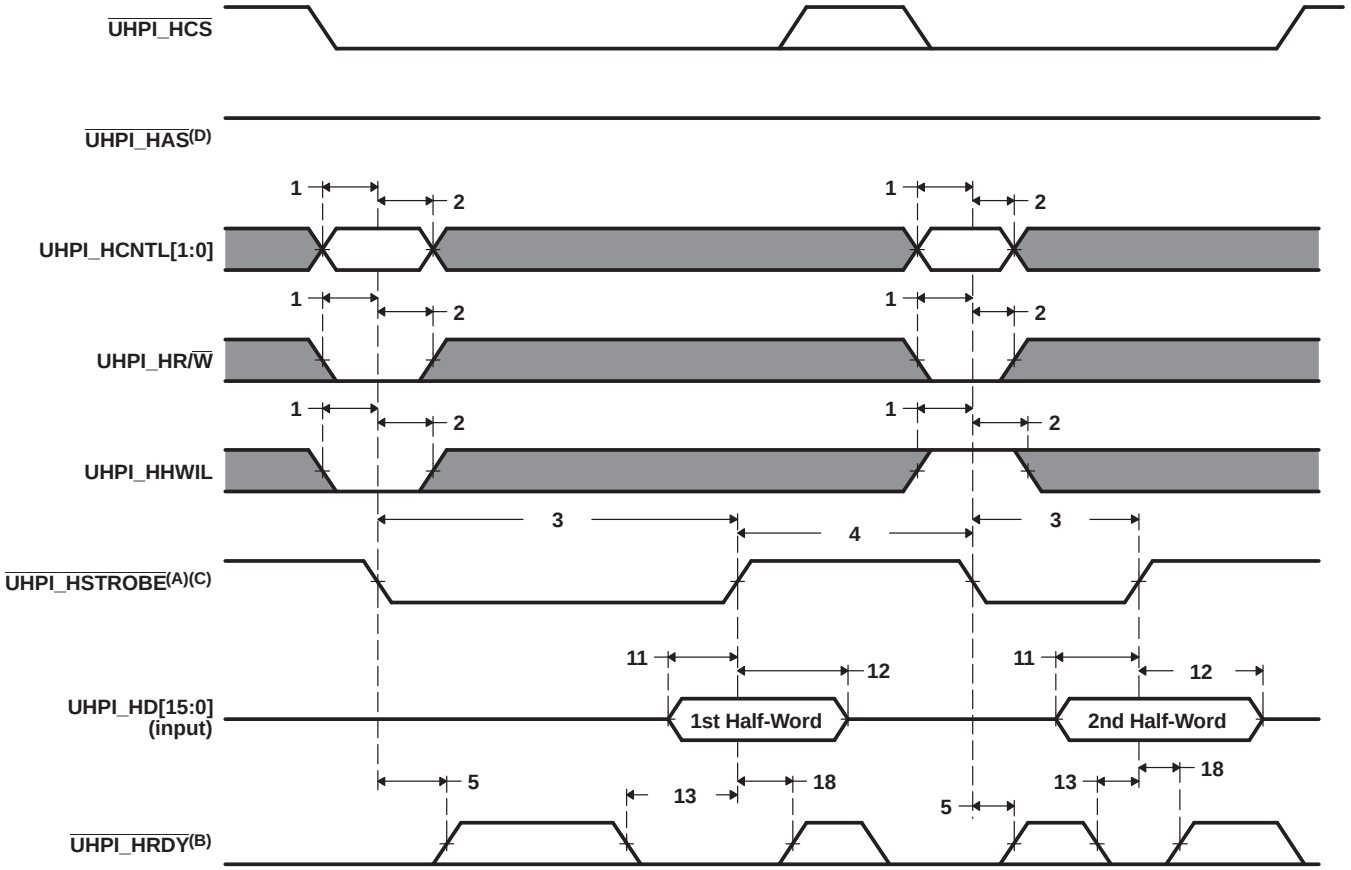



A. For correct operation, strobe the UHPI_HAS signal only once per UHPI_HSTROBE active cycle.

B. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(UHPI_HDS1 XOR UHPI_HDS2)] OR UHPI_HCS.

**Figure 5-68. UHPI Read Timing (HAS Used)**




A. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(HDS1 XOR HDS2)] OR UHPI_HCS.
B. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on UHPI_HRDY may or may not occur.
C. UHPI_HCS reflects typical UHPI_HCS behavior when UHPI_HSTROBE assertion is caused by UHPI_HDS1 or UHPI_HDS2. UHPI_HCS timing requirements are reflected by parameters for UHPI_HSTROBE.
D The diagram above assumes UHPI_HAS has been pulled high.

**Figure 5-69. UHPI Write Timing (HAS Not Used, Tied High)**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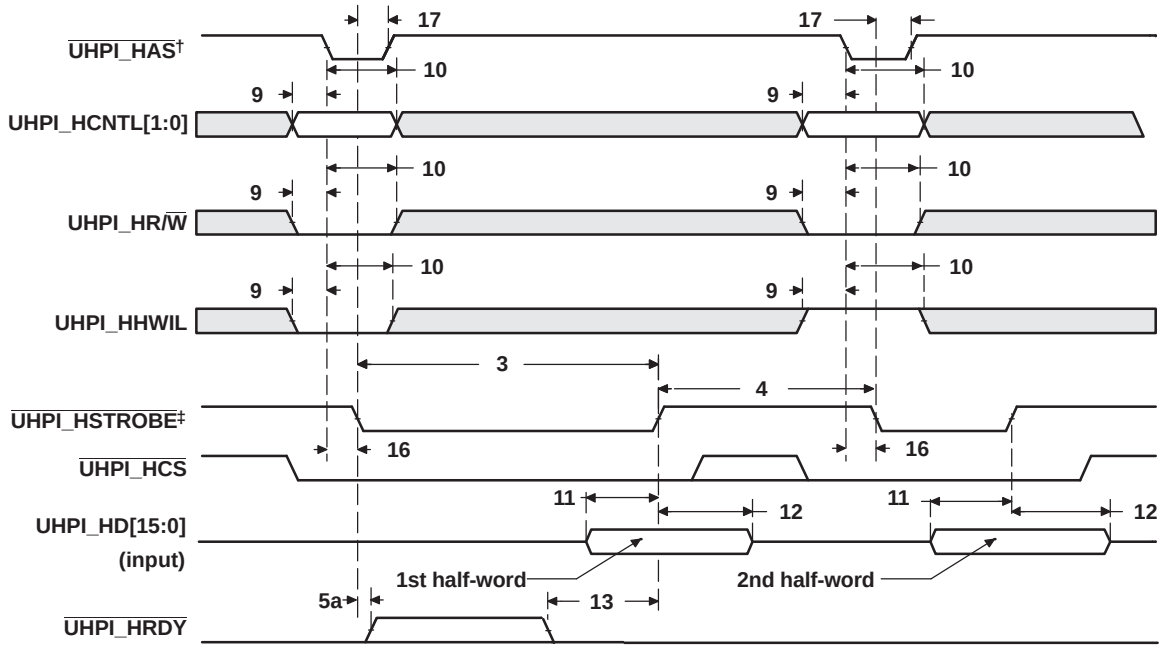


A. For correct operation, strobe the UHPI_HAS signal only once per UHPI_HSTROBE active cycle.
B. UHPI_HSTROBE refers to the following logical operation on UHPI_HCS, UHPI_HDS1, and UHPI_HDS2: [NOT(UHPI_HDS1 XOR UHPI_HDS2)] OR UHPI_HCS.

**Figure 5-70. UHPI Write Timing (HAS Used)**

## 5.26 Universal Parallel Port (uPP)

The Universal Parallel Port (uPP) peripheral is a multichannel, high-speed parallel interface with dedicated data lines and minimal control signals. It is designed to interface cleanly with high-speed analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) with up to 16-bit data width (per channel). It may also be interconnected with field-programmable gate arrays (FPGAs) or other uPP devices to achieve high-speed digital data transfer. It can operate in receive mode, transmit mode, or duplex mode, in which its individual channels operate in opposite directions.

The uPP peripheral includes an internal DMA controller to maximize throughput and minimize CPU overhead during high-speed data transmission. All uPP transactions use the internal DMA to provide data to or retrieve data from the I/O channels. The DMA controller includes two DMA channels, which typically service separate I/O channels. The uPP peripheral also supports data interleave mode, in which all DMA resources service a single I/O channel. In this mode, only one I/O channel may be used.

The features of the uPP include:

- Programmable data width per channel (from 8 to 16 bits inclusive)
- Programmable data justification
  - Right-justify with zero extend
  - Right-justify with sign extend
  - Left-justify with zero fill
- Supports multiplexing of interleaved data during SDR transmit
- Optional frame START signal with programmable polarity
- Optional data ENABLE signal with programmable polarity
- Optional synchronization WAIT signal with programmable polarity
- Single Data Rate (SDR) or Double data Rate (DDR, interleaved) interface
  - Supports multiplexing of interleaved data during SDR transmit
  - Supports demultiplexing and multiplexing of interleaved data during DDR transfers


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### 5.26.1 uPP Register Descriptions

**Table 5-117. Universal Parallel Port (uPP) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 6000 | UPPID | uPP Peripheral Identification Register |
| 0x01E1 6004 | UPPCR | uPP Peripheral Control Register |
| 0x01E1 6008 | UPDLB | uPP Digital Loopback Register |
| 0x01E1 6010 | UPCTL | uPP Channel Control Register |
| 0x01E1 6014 | UPICR | uPP Interface Configuration Register |
| 0x01E1 6018 | UPIVR | uPP Interface Idle Value Register |
| 0x01E1 601C | UPTCR | uPP Threshold Configuration Register |
| 0x01E1 6020 | UPISR | uPP Interrupt Raw Status Register |
| 0x01E1 6024 | UPIER | uPP Interrupt Enabled Status Register |
| 0x01E1 6028 | UPIES | uPP Interrupt Enable Set Register |
| 0x01E1 602C | UPIEC | uPP Interrupt Enable Clear Register |
| 0x01E1 6030 | UPEOI | uPP End-of-Interrupt Register |
| 0x01E1 6040 | UPID0 | uPP DMA Channel I Descriptor 0 Register |
| 0x01E1 6044 | UPID1 | uPP DMA Channel I Descriptor 1 Register |
| 0x01E1 6048 | UPID2 | uPP DMA Channel I Descriptor 2 Register |
| 0x01E1 6050 | UPIS0 | uPP DMA Channel I Status 0 Register |
| 0x01E1 6054 | UPIS1 | uPP DMA Channel I Status 1 Register |
| 0x01E1 6058 | UPIS2 | uPP DMA Channel I Status 2 Register |
| 0x01E1 6060 | UPQD0 | uPP DMA Channel Q Descriptor 0 Register |
| 0x01E1 6064 | UPQD1 | uPP DMA Channel Q Descriptor 1 Register |
| 0x01E1 6068 | UPQD2 | uPP DMA Channel Q Descriptor 2 Register |
| 0x01E1 6070 | UPQS0 | uPP DMA Channel Q Status 0 Register |
| 0x01E1 6074 | UPQS1 | uPP DMA Channel Q Status 1 Register |
| 0x01E1 6078 | UPQS2 | uPP DMA Channel Q Status 2 Register |

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### 5.26.2 uPP Electrical Data/Timing

**Table 5-118. Timing Requirements for uPP (see Figure 5-71, Figure 5-72, Figure 5-73, Figure 5-74)**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(INCLK)}$ | Cycle time, CH*n*_CLK | SDR mode | 13.33 | | 20 | | 26.66 | | ns |
| | | | DDR mode | 26.66 | | 40 | | 53.33 | | |
| 2 | $t_{w(INCLKH)}$ | Pulse width, CH*n*_CLK high | SDR mode | 5 | | 8 | | 10 | | ns |
| | | | DDR mode | 10 | | 16 | | 20 | | |
| 3 | $t_{w(INCLKL)}$ | Pulse width, CH*n*_CLK low | SDR mode | 5 | | 8 | | 10 | | ns |
| | | | DDR mode | 10 | | 16 | | 20 | | |
| 4 | $t_{su(STV-INCLKH)}$ | Setup time, CH*n*_START valid before CH*n*_CLK high | | 4 | | 5.5 | | 6.5 | | ns |
| 5 | $t_{h(INCLKH-STV)}$ | Hold time, CH*n*_START valid after CH*n*_CLK high | | 0.8 | | 0.8 | | 0.8 | | ns |
| 6 | $t_{su(ENV-INCLKH)}$ | Setup time, CH*n*_ENABLE valid before CH*n*_CLK high | | 4 | | 5.5 | | 6.5 | | ns |
| 7 | $t_{h(INCLKH-ENV)}$ | Hold time, CH*n*_ENABLE valid after CH*n*_CLK high | | 0.8 | | 0.8 | | 0.8 | | ns |
| 8 | $t_{su(DV-INCLKH)}$ | Setup time, CH*n*_DATA/XDATA valid before CH*n*_CLK high | | 4 | | 5.5 | | 6.5 | | ns |
| 9 | $t_{h(INCLKH-DV)}$ | Hold time, CH*n*_DATA/XDATA valid after CH*n*_CLK high | | 0.8 | | 0.8 | | 0.8 | | ns |
| 10 | $t_{su(DV-INCLKL)}$ | Setup time, CH*n*_DATA/XDATA valid before CH*n*_CLK low | | 4 | | 5.5 | | 6.5 | | ns |
| 11 | $t_{h(INCLKL-DV)}$ | Hold time, CH*n*_DATA/XDATA valid after CH*n*_CLK low | | 0.8 | | 0.8 | | 0.8 | | ns |
| 19 | $t_{su(WTV-INCLKL)}$ | Setup time, CH*n*_WAIT valid before CH*n*_CLK high | | 10 | | 12 | | 14 | | ns |
| 20 | $t_{h(INCLKL-WTV)}$ | Hold time, CH*n*_WAIT valid after CH*n*_CLK high | | 0.8 | | 0.8 | | 0.8 | | ns |
| 21 | $t_{c(2xTXCLK)}$ | Cycle time, 2xTXCLK input clock(1) | | 6.66 | | 10 | | 13.33 | | ns |

(1) 2xTXCLK is an alternate transmit clock source that must be at least 2 times the required uPP transmit clock rate (as it is is divided down by 2 inside the uPP). 2xTXCLK has no specified skew relationship to the CH*n*_CLOCK and therefore is not shown in the timing diagram.

**Table 5-119. Switching Characteristics Over Recommended Operating Conditions for uPP**

| NO. | PARAMETER | | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 12 | $t_{c(OUTCLK)}$ | Cycle time, CH*n*_CLK | SDR mode | 13.33 | | 20 | | 26.66 | | ns |
| | | | DDR mode | 26.66 | | 40 | | 53.33 | | |
| 13 | $t_{w(OUTCLKH)}$ | Pulse width, CH*n*_CLK high | SDR mode | 5 | | 8 | | 10 | | ns |
| | | | DDR mode | 10 | | 16 | | 20 | | |
| 14 | $t_{w(OUTCLKL)}$ | Pulse width, CH*n*_CLK low | SDR mode | 5 | | 8 | | 10 | | ns |
| | | | DDR mode | 10 | | 16 | | 20 | | |
| 15 | $t_{d(OUTCLKH-STV)}$ | Delay time, CH*n*_START valid after CH*n*_CLK high | | 2 | 11 | 2 | 15 | 2 | 21 | ns |
| 16 | $t_{d(OUTCLKH-ENV)}$ | Delay time, CH*n*_ENABLE valid after CH*n*_CLK high | | 2 | 11 | 2 | 15 | 2 | 21 | ns |
| 17 | $t_{d(OUTCLKH-DV)}$ | Delay time, CH*n*_DATA/XDATA valid after CH*n*_CLK high | | 2 | 11 | 2 | 15 | 2 | 21 | ns |
| 18 | $t_{d(OUTCLKL-DV)}$ | Delay time, CH*n*_DATA/XDATA valid after CH*n*_CLK low | | 2 | 11 | 2 | 15 | 2 | 21 | ns |


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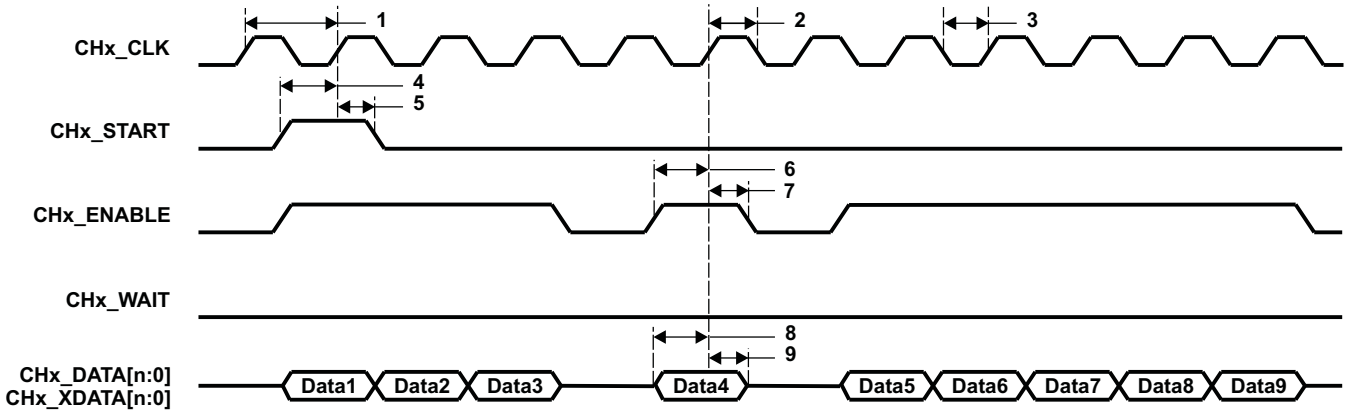


**Figure 5-71. uPP Single Data Rate (SDR) Receive Timing**

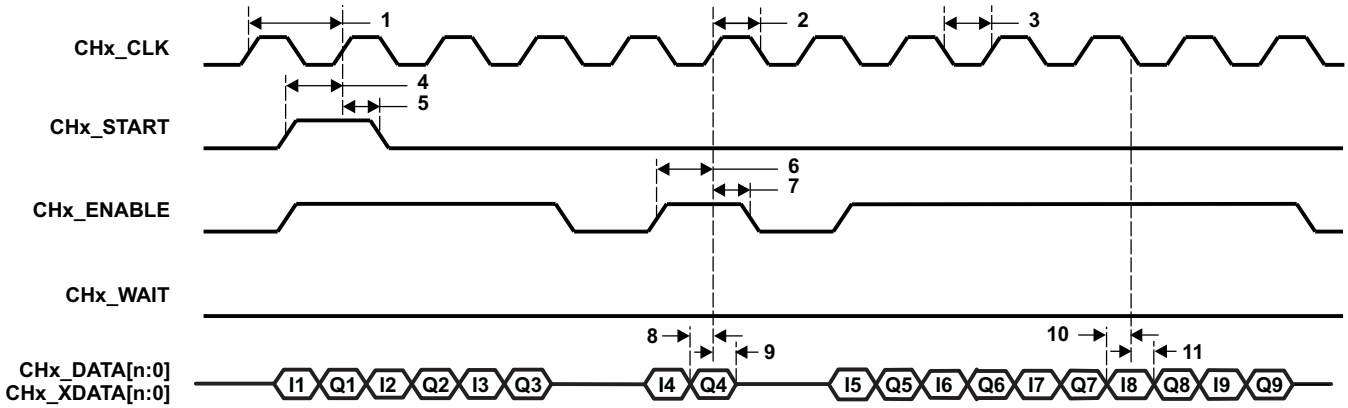


**Figure 5-72. uPP Double Data Rate (DDR) Receive Timing**

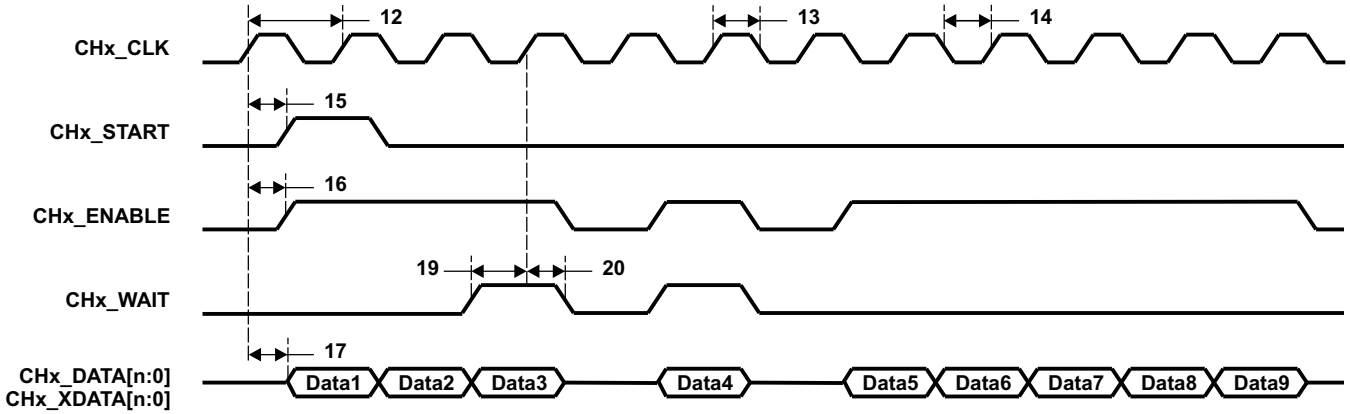


**Figure 5-73. uPP Single Data Rate (SDR) Transmit Timing**

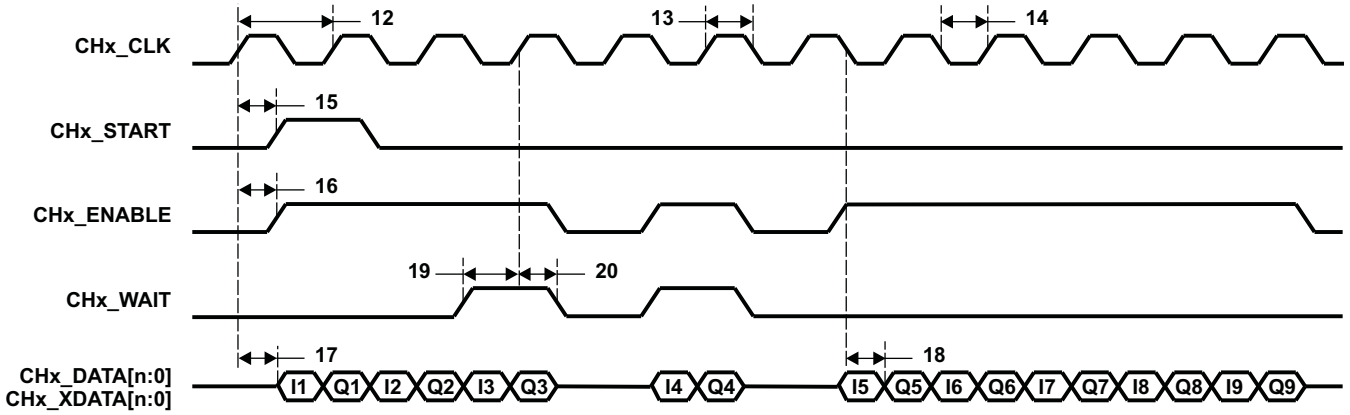


**Figure 5-74. uPP Double Data Rate (DDR) Transmit Timing**


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## 5.27 Video Port Interface (VPIF)

The Video Port Interface (VPIF) allows the capture and display of digital video streams. Features include:

- Up to 2 Video Capture Channels (Channel 0 and Channel 1)
  - Two 8-bit Standard-Definition (SD) Video with embedded timing codes (BT.656)
  - Single 16-bit High-Definition (HD) Video with embedded timing codes (BT.1120)
  - Single Raw Video (8-/10-/12-bit)
- Up to 2 Video Display Channels (Channel 2 and Channel 3)
  - Two 8-bit SD Video Display with embedded timing codes (BT.656)
  - Single 16-bit HD Video Display with embedded timing codes (BT.1120)

The VPIF capture channel input data format is selectable based on the settings of the specific Channel Control Register (Channels 0–3). The VPIF Raw Video data-bus width is selectable based on the settings of the Channel 0 Control Register.

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### 5.27.1 VPIF Register Descriptions

Table 5-120 shows the VPIF registers.

**Table 5-120. Video Port Interface (VPIF) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 7000 | PID | Peripheral identification register |
| 0x01E1 7004 | CH0_CTRL | Channel 0 control register |
| 0x01E1 7008 | CH1_CTRL | Channel 1 control register |
| 0x01E1 700C | CH2_CTRL | Channel 2 control register |
| 0x01E1 7010 | CH3_CTRL | Channel 3 control register |
| 0x01E1 7014 - 0x01E1 701F | - | Reserved |
| 0x01E1 7020 | INTEN | Interrupt enable |
| 0x01E1 7024 | INTENSET | Interrupt enable set |
| 0x01E1 7028 | INTENCLR | Interrupt enable clear |
| 0x01E1 702C | INTSTAT | Interrupt status |
| 0x01E1 7030 | INTSTATCLR | Interrupt status clear |
| 0x01E1 7034 | EMU_CTRL | Emulation control |
| 0x01E1 7038 | DMA_SIZE | DMA size control |
| 0x01E1 703C - 0x01E1 703F | - | Reserved |
| **CAPTURE CHANNEL 0 REGISTERS** | | |
| 0x01E1 7040 | CH0_TY_STRTADR | Channel 0 Top Field luma buffer start address |
| 0x01E1 7044 | CH0_BY_STRTADR | Channel 0 Bottom Field luma buffer start address |
| 0x01E1 7048 | CH0_TC_STRTADR | Channel 0 Top Field chroma buffer start address |
| 0x01E1 704C | CH0_BC_STRTADR | Channel 0 Bottom Field chroma buffer start address |
| 0x01E1 7050 | CH0_THA_STRTADR | Channel 0 Top Field horizontal ancillary data buffer start address |
| 0x01E1 7054 | CH0_BHA_STRTADR | Channel 0 Bottom Field horizontal ancillary data buffer start address |
| 0x01E1 7058 | CH0_TVA_STRTADR | Channel 0 Top Field vertical ancillary data buffer start address |
| 0x01E1 705C | CH0_BVA_STRTADR | Channel 0 Bottom Field vertical ancillary data buffer start address |
| 0x01E1 7060 | CH0_SUBPIC_CFG | Channel 0 sub-picture configuration |
| 0x01E1 7064 | CH0_IMG_ADD_OFST | Channel 0 image data address offset |
| 0x01E1 7068 | CH0_HA_ADD_OFST | Channel 0 horizontal ancillary data address offset |
| 0x01E1 706C | CH0_HSIZE_CFG | Channel 0 horizontal data size configuration |
| 0x01E1 7070 | CH0_VSIZE_CFG0 | Channel 0 vertical data size configuration (0) |
| 0x01E1 7074 | CH0_VSIZE_CFG1 | Channel 0 vertical data size configuration (1) |
| 0x01E1 7078 | CH0_VSIZE_CFG2 | Channel 0 vertical data size configuration (2) |
| 0x01E1 707C | CH0_VSIZE | Channel 0 vertical image size |
| **CAPTURE CHANNEL 1 REGISTERS** | | |
| 0x01E1 7080 | CH1_TY_STRTADR | Channel 1 Top Field luma buffer start address |
| 0x01E1 7084 | CH1_BY_STRTADR | Channel 1 Bottom Field luma buffer start address |
| 0x01E1 7088 | CH1_TC_STRTADR | Channel 1 Top Field chroma buffer start address |
| 0x01E1 708C | CH1_BC_STRTADR | Channel 1 Bottom Field chroma buffer start address |
| 0x01E1 7090 | CH1_THA_STRTADR | Channel 1 Top Field horizontal ancillary data buffer start address |
| 0x01E1 7094 | CH1_BHA_STRTADR | Channel 1 Bottom Field horizontal ancillary data buffer start address |
| 0x01E1 7098 | CH1_TVA_STRTADR | Channel 1 Top Field vertical ancillary data buffer start address |
| 0x01E1 709C | CH1_BVA_STRTADR | Channel 1 Bottom Field vertical ancillary data buffer start address |
| 0x01E1 70A0 | CH1_SUBPIC_CFG | Channel 1 sub-picture configuration |
| 0x01E1 70A4 | CH1_IMG_ADD_OFST | Channel 1 image data address offset |
| 0x01E1 70A8 | CH1_HA_ADD_OFST | Channel 1 horizontal ancillary data address offset |
| 0x01E1 70AC | CH1_HSIZE_CFG | Channel 1 horizontal data size configuration |


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**Table 5-120. Video Port Interface (VPIF) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 70B0 | CH1_VSIZE_CFG0 | Channel 1 vertical data size configuration (0) |
| 0x01E1 70B4 | CH1_VSIZE_CFG1 | Channel 1 vertical data size configuration (1) |
| 0x01E1 70B8 | CH1_VSIZE_CFG2 | Channel 1 vertical data size configuration (2) |
| 0x01E1 70BC | CH1_VSIZE | Channel 1 vertical image size |
| **DISPLAY CHANNEL 2 REGISTERS** | | |
| 0x01E1 70C0 | CH2_TY_STRTADR | Channel 2 Top Field luma buffer start address |
| 0x01E1 70C4 | CH2_BY_STRTADR | Channel 2 Bottom Field luma buffer start address |
| 0x01E1 70C8 | CH2_TC_STRTADR | Channel 2 Top Field chroma buffer start address |
| 0x01E1 70CC | CH2_BC_STRTADR | Channel 2 Bottom Field chroma buffer start address |
| 0x01E1 70D0 | CH2_THA_STRTADR | Channel 2 Top Field horizontal ancillary data buffer start address |
| 0x01E1 70D4 | CH2_BHA_STRTADR | Channel 2 Bottom Field horizontal ancillary data buffer start address |
| 0x01E1 70D8 | CH2_TVA_STRTADR | Channel 2 Top Field vertical ancillary data buffer start address |
| 0x01E1 70DC | CH2_BVA_STRTADR | Channel 2 Bottom Field vertical ancillary data buffer start address |
| 0x01E1 70E0 | CH2_SUBPIC_CFG | Channel 2 sub-picture configuration |
| 0x01E1 70E4 | CH2_IMG_ADD_OFST | Channel 2 image data address offset |
| 0x01E1 70E8 | CH2_HA_ADD_OFST | Channel 2 horizontal ancillary data address offset |
| 0x01E1 70EC | CH2_HSIZE_CFG | Channel 2 horizontal data size configuration |
| 0x01E1 70F0 | CH2_VSIZE_CFG0 | Channel 2 vertical data size configuration (0) |
| 0x01E1 70F4 | CH2_VSIZE_CFG1 | Channel 2 vertical data size configuration (1) |
| 0x01E1 70F8 | CH2_VSIZE_CFG2 | Channel 2 vertical data size configuration (2) |
| 0x01E1 70FC | CH2_VSIZE | Channel 2 vertical image size |
| 0x01E1 7100 | CH2_THA_STRTPOS | Channel 2 Top Field horizontal ancillary data insertion start position |
| 0x01E1 7104 | CH2_THA_SIZE | Channel 2 Top Field horizontal ancillary data size |
| 0x01E1 7108 | CH2_BHA_STRTPOS | Channel 2 Bottom Field horizontal ancillary data insertion start position |
| 0x01E1 710C | CH2_BHA_SIZE | Channel 2 Bottom Field horizontal ancillary data size |
| 0x01E1 7110 | CH2_TVA_STRTPOS | Channel 2 Top Field vertical ancillary data insertion start position |
| 0x01E1 7114 | CH2_TVA_SIZE | Channel 2 Top Field vertical ancillary data size |
| 0x01E1 7118 | CH2_BVA_STRTPOS | Channel 2 Bottom Field vertical ancillary data insertion start position |
| 0x01E1 711C | CH2_BVA_SIZE | Channel 2 Bottom Field vertical ancillary data size |
| 0x01E1 7120 - 0x01E1 713F | - | Reserved |
| **DISPLAY CHANNEL 3 REGISTERS** | | |
| 0x01E1 7140 | CH3_TY_STRTADR | Channel 3 Field 0 luma buffer start address |
| 0x01E1 7144 | CH3_BY_STRTADR | Channel 3 Field 1 luma buffer start address |
| 0x01E1 7148 | CH3_TC_STRTADR | Channel 3 Field 0 chroma buffer start address |
| 0x01E1 714C | CH3_BC_STRTADR | Channel 3 Field 1 chroma buffer start address |
| 0x01E1 7150 | CH3_THA_STRTADR | Channel 3 Field 0 horizontal ancillary data buffer start address |
| 0x01E1 7154 | CH3_BHA_STRTADR | Channel 3 Field 1 horizontal ancillary data buffer start address |
| 0x01E1 7158 | CH3_TVA_STRTADR | Channel 3 Field 0 vertical ancillary data buffer start address |
| 0x01E1 715C | CH3_BVA_STRTADR | Channel 3 Field 1 vertical ancillary data buffer start address |
| 0x01E1 7160 | CH3_SUBPIC_CFG | Channel 3 sub-picture configuration |
| 0x01E1 7164 | CH3_IMG_ADD_OFST | Channel 3 image data address offset |
| 0x01E1 7168 | CH3_HA_ADD_OFST | Channel 3 horizontal ancillary data address offset |
| 0x01E1 716C | CH3_HSIZE_CFG | Channel 3 horizontal data size configuration |
| 0x01E1 7170 | CH3_VSIZE_CFG0 | Channel 3 vertical data size configuration (0) |
| 0x01E1 7174 | CH3_VSIZE_CFG1 | Channel 3 vertical data size configuration (1) |
| 0x01E1 7178 | CH3_VSIZE_CFG2 | Channel 3 vertical data size configuration (2) |
| 0x01E1 717C | CH3_VSIZE | Channel 3 vertical image size |

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**Table 5-120. Video Port Interface (VPIF) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E1 7180 | CH3_THA_STRTPOS | Channel 3 Top Field horizontal ancillary data insertion start position |
| 0x01E1 7184 | CH3_THA_SIZE | Channel 3 Top Field horizontal ancillary data size |
| 0x01E1 7188 | CH3_BHA_STRTPOS | Channel 3 Bottom Field horizontal ancillary data insertion start position |
| 0x01E1 718C | CH3_BHA_SIZE | Channel 3 Bottom Field horizontal ancillary data size |
| 0x01E1 7190 | CH3_TVA_STRTPOS | Channel 3 Top Field vertical ancillary data insertion start position |
| 0x01E1 7194 | CH3_TVA_SIZE | Channel 3 Top Field vertical ancillary data size |
| 0x01E1 7198 | CH3_BVA_STRTPOS | Channel 3 Bottom Field vertical ancillary data insertion start position |
| 0x01E1 719C | CH3_BVA_SIZE | Channel 3 Bottom Field vertical ancillary data size |
| 0x01E1 71A0 - 0x01E1 71FF | - | Reserved |


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### 5.27.2 VPIF Electrical Data/Timing

**Table 5-121. Timing Requirements for VPIF VP_CLKINx Inputs[1] (see Figure 5-75)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(VKI)}$ | Cycle time, VP_CLKIN0 | 13.3 | | 20 | | 37 | | ns |
| | | Cycle time, VP_CLKIN1/2/3 | 13.3 | | 20 | | 37 | | ns |
| 2 | $t_{w(VKIH)}$ | Pulse duration, VP_CLKINx high | 0.4C | | 0.4C | | 0.4C | | ns |
| 3 | $t_{w(VKIL)}$ | Pulse duration, VP_CLKINx low | 0.4C | | 0.4C | | 0.4C | | ns |
| 4 | $t_{t(VKI)}$ | Transition time, VP_CLKINx | | 5 | | 5 | | 5 | ns |

(1) C = VP_CLKINx period in ns.

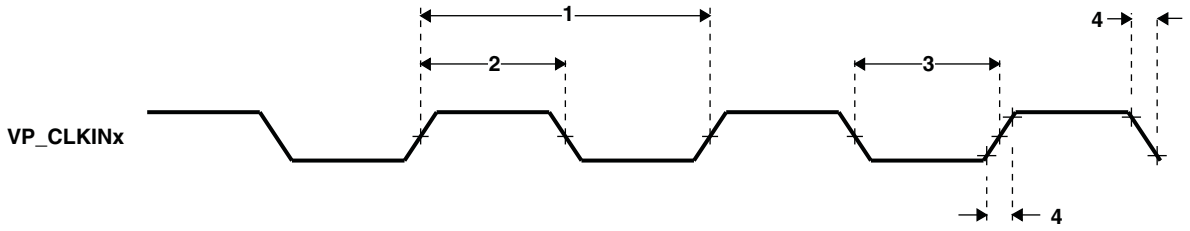


**Figure 5-75. Video Port Capture VP_CLKINx Timing**

**Table 5-122. Timing Requirements for VPIF Channels 0/1 Video Capture Data and Control Inputs (see Figure 5-76)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{su(VDINV-VKIH)}$ | Setup time, VP_DINx valid before VP_OSCIN0/1 high | 4 | | 6 | | 7 | | ns |
| 2 | $t_{h(VKIH-VDINV)}$ | Hold time, VP_DINx valid after VP_CLKIN0/1 high | 0 | | 0 | | 0 | | ns |

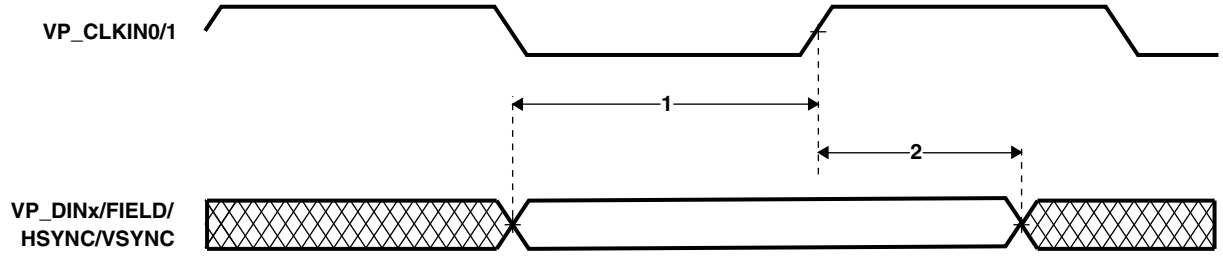


**Figure 5-76. VPIF Channels 0/1 Video Capture Data and Control Input Timing**

**Table 5-123. Switching Characteristics Over Recommended Operating Conditions for Video Data Shown With Respect to VP_CLKOUT2/3 (1) (see Figure 5-77)**

| NO. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(VKO)}$ | Cycle time, VP_CLKOUT2/3 | 13.3 | | 20 | | 37 | | ns |
| 2 | $t_{w(VKOH)}$ | Pulse duration, VP_CLKOUT2/3 high | 0.4C | | 0.4C | | 0.4C | | ns |
| 3 | $t_{w(VKOL)}$ | Pulse duration, VP_CLKOUT2/3 low | 0.4C | | 0.4C | | 0.4C | | ns |
| 4 | $t_{t(VKO)}$ | Transition time, VP_CLKOUT2/3 | | 5 | | 5 | | 5 | ns |
| 11 | $t_{d(VKOH-VPDOUTV)}$ | Delay time, VP_CLKOUT2/3 high to VP_DOUTx valid | | 8.5 | | 12 | | 17 | ns |
| 12 | $t_{d(VCLKOH-VPDOUTIV)}$ | Delay time, VP_CLKOUT2/3 high to VP_DOUTx invalid | 1.5 | | 1.5 | | 1.5 | | ns |

(1) C = VP_CLKO2/3 period in ns.

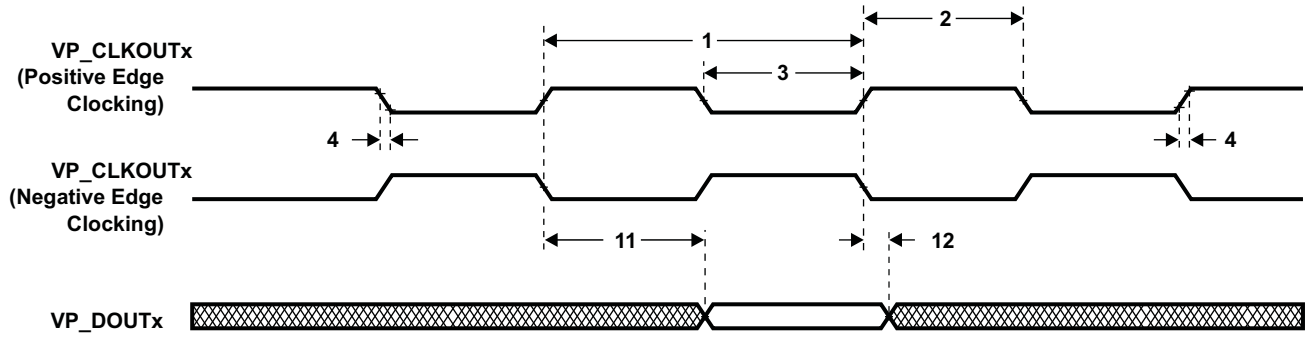


**Figure 5-77. VPIF Channels 2/3 Video Display Data Output Timing With Respect to VP_CLKOUT2/3**


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## 5.28 Enhanced Capture (eCAP) Peripheral

The device contains up to three enhanced capture (eCAP) modules. Figure 5-78 shows a functional block diagram of a module.

Uses for ECAP include:

- Speed measurements of rotating machinery (e.g. toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor triggers
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The ECAP module described in this specification includes the following features:

- 32 bit time base
- 4 event time-stamp registers (each 32 bits)
- Edge polarity selection for up to 4 sequenced time-stamp capture events
- Interrupt on either of the 4 events
- Single shot capture of up to 4 event time-stamps
- Continuous mode capture of time-stamps in a 4 deep circular buffer
- Absolute time-stamp capture
- Difference mode time-stamp capture
- All the above resources are dedicated to a single input pin

The eCAP modules are clocked at the ASYNC3 clock domain rate.

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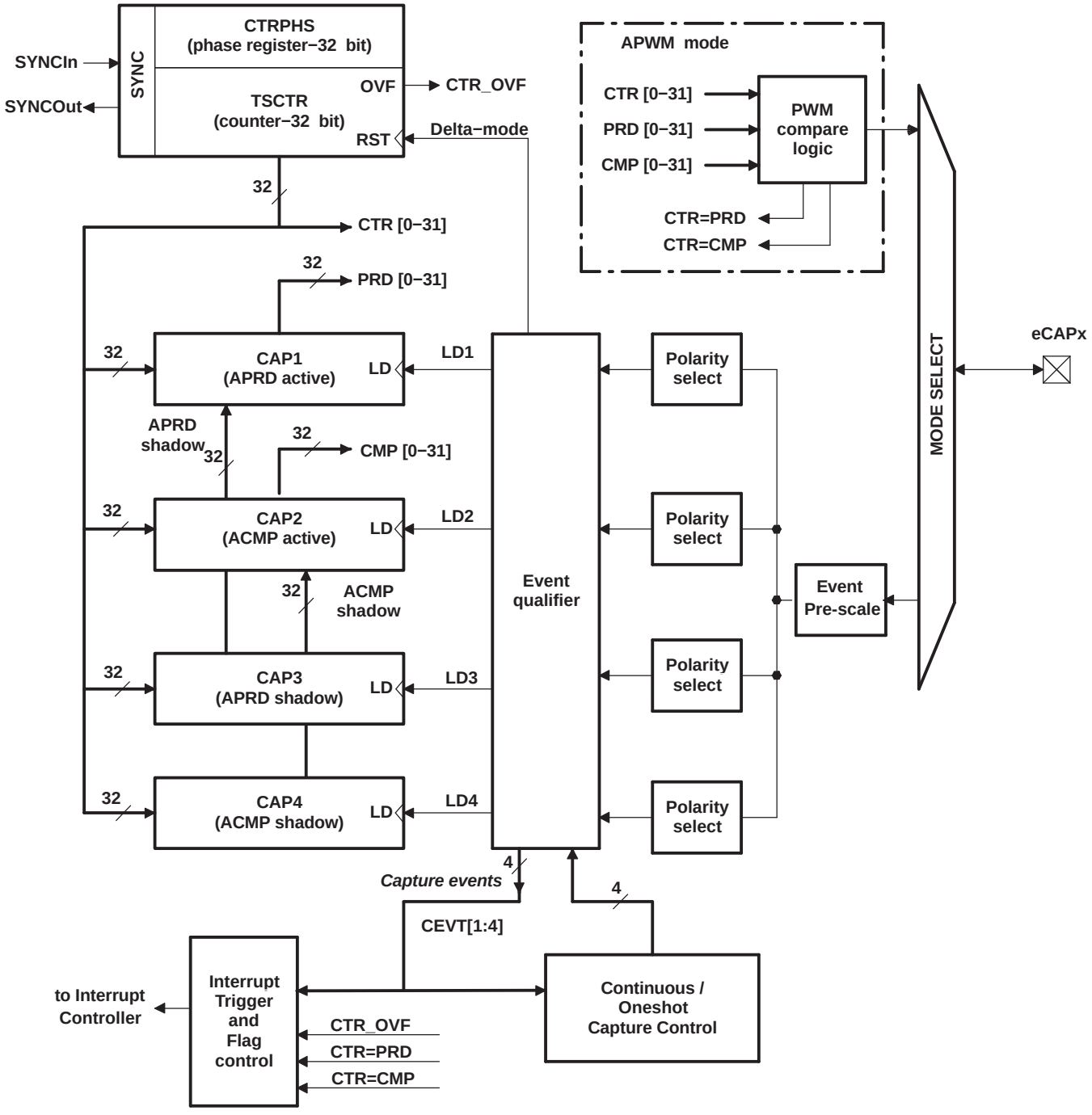


**Figure 5-78. eCAP Functional Block Diagram**


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Table 5-124 is the list of the ECAP registers.

**Table 5-124. ECAPx Configuration Registers**

| ECAP0 BYTE ADDRESS | ECAP1 BYTE ADDRESS | ECAP2 BYTE ADDRESS | ACRONYM | DESCRIPTION |
|---|---|---|---|---|
| 0x01F0 6000 | 0x01F0 7000 | 0x01F0 8000 | TSCTR | Time-Stamp Counter |
| 0x01F0 6004 | 0x01F0 7004 | 0x01F0 8004 | CTRPHS | Counter Phase Offset Value Register |
| 0x01F0 6008 | 0x01F0 7008 | 0x01F0 8008 | CAP1 | Capture 1 Register |
| 0x01F0 600C | 0x01F0 700C | 0x01F0 800C | CAP2 | Capture 2 Register |
| 0x01F0 6010 | 0x01F0 7010 | 0x01F0 8010 | CAP3 | Capture 3 Register |
| 0x01F0 6014 | 0x01F0 7014 | 0x01F0 8014 | CAP4 | Capture 4 Register |
| 0x01F0 6028 | 0x01F0 7028 | 0x01F0 8028 | ECCTL1 | Capture Control Register 1 |
| 0x01F0 602A | 0x01F0 702A | 0x01F0 802A | ECCTL2 | Capture Control Register 2 |
| 0x01F0 602C | 0x01F0 702C | 0x01F0 802C | ECEINT | Capture Interrupt Enable Register |
| 0x01F0 602E | 0x01F0 702E | 0x01F0 802E | ECFLG | Capture Interrupt Flag Register |
| 0x01F0 6030 | 0x01F0 7030 | 0x01F0 8030 | ECCLR | Capture Interrupt Clear Register |
| 0x01F0 6032 | 0x01F0 7032 | 0x01F0 8032 | ECFRC | Capture Interrupt Force Register |
| 0x01F0 605C | 0x01F0 705C | 0x01F0 805C | REVID | Revision ID |

Table 5-125 shows the eCAP timing requirement and Table 5-126 shows the eCAP switching characteristics.

**Table 5-125. Timing Requirements for Enhanced Capture (eCAP)**

| PARAMETER | | TEST CONDITIONS | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{w(CAP)}$ | Capture input pulse width | Asynchronous | $2t_{c(SCO)}$ | | cycles |
| | | Synchronous | $2t_{c(SCO)}$ | | cycles |

**Table 5-126. Switching Characteristics Over Recommended Operating Conditions for eCAP**

| PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{w(APWM)}$ | Pulse duration, APWMx output high/low | 20 | | 20 | | 20 | | ns |

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## 5.29 Enhanced High-Resolution Pulse-Width Modulator (eHRPWM)

The device contains two enhanced PWM Modules (eHRPWM). Figure 5-79 shows a block diagram of multiple eHRPWM modules. Figure 5-79 shows the signal interconnections with the eHRPWM.

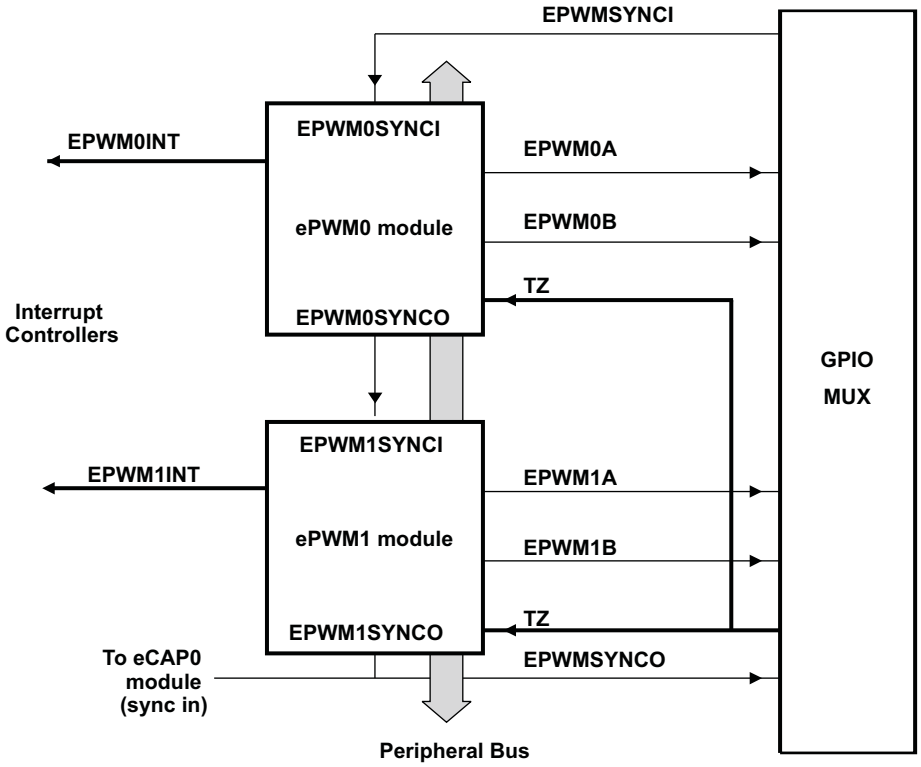


**Figure 5-79. Multiple PWM Modules in a OMAP-L138 System**


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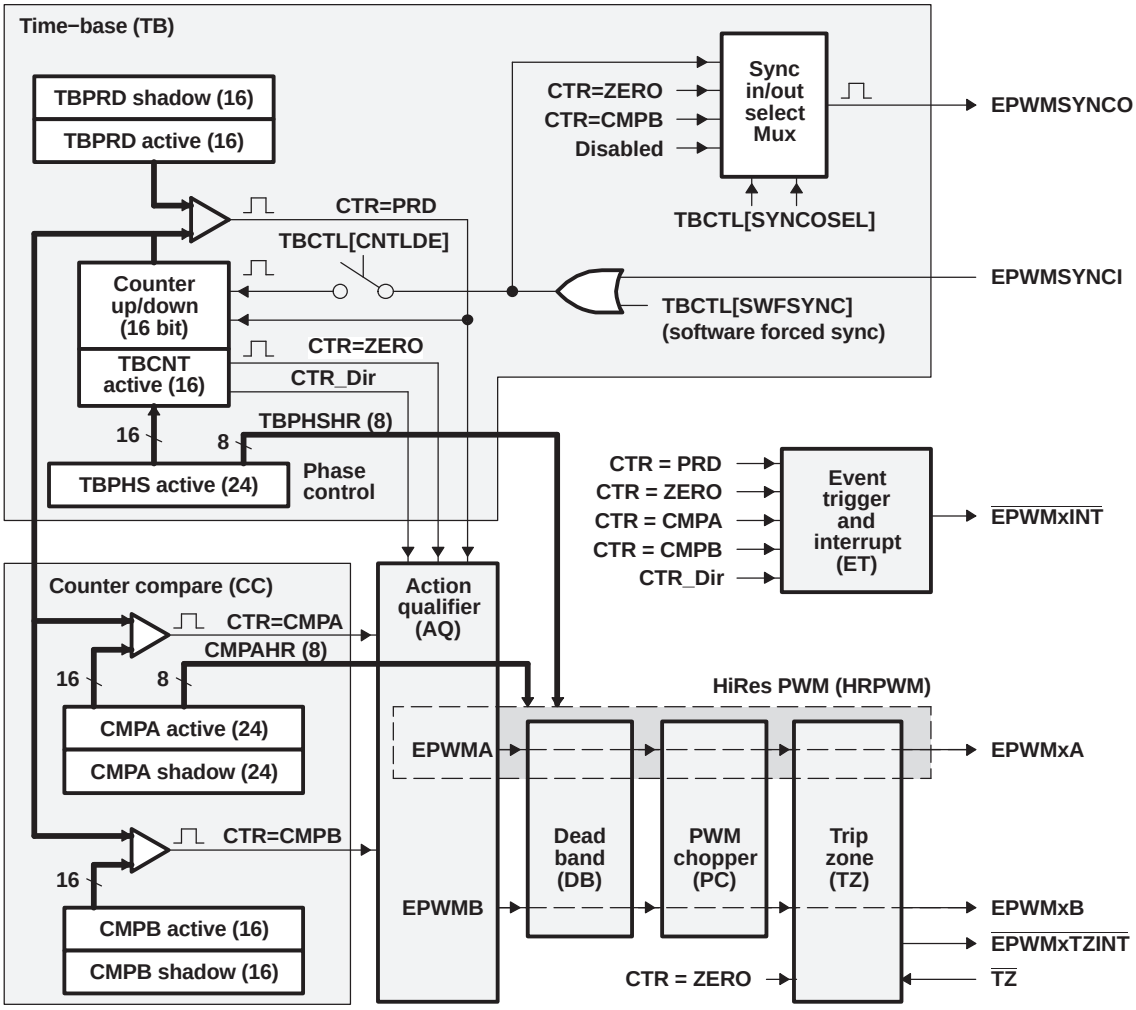


**Figure 5-80. eHRPWM Sub-Modules Showing Critical Internal Signal Interconnections**

**Table 5-127. eHRPWM Module Control and Status Registers Grouped by Submodule**

| eHRPWM0 BYTE ADDRESS | eHRPWM1 BYTE ADDRESS | ACRONYM | SHADOW | REGISTER DESCRIPTION |
|---|---|---|---|---|
| **Time-Base Submodule Registers** | | | | |
| 0x01F0 0000 | 0x01F0 2000 | TBCTL | No | Time-Base Control Register |
| 0x01F0 0002 | 0x01F0 2002 | TBSTS | No | Time-Base Status Register |
| 0x01F0 0004 | 0x01F0 2004 | TBPHSHR | No | Extension for HRPWM Phase Register(1) |
| 0x01F0 0006 | 0x01F0 2006 | TBPHS | No | Time-Base Phase Register |
| 0x01F0 0008 | 0x01F0 2008 | TBCNT | No | Time-Base Counter Register |
| 0x01F0 000A | 0x01F0 200A | TBPRD | Yes | Time-Base Period Register |
| **Counter-Compare Submodule Registers** | | | | |
| 0x01F0 000E | 0x01F0 200E | CMPCTL | No | Counter-Compare Control Register |
| 0x01F0 0010 | 0x01F0 2010 | CMPAHR | No | Extension for HRPWM Counter-Compare A Register(1) |
| 0x01F0 0012 | 0x01F0 2012 | CMPA | Yes | Counter-Compare A Register |
| 0x01F0 0014 | 0x01F0 2014 | CMPB | Yes | Counter-Compare B Register |
| **Action-Qualifier Submodule Registers** | | | | |
| 0x01F0 0016 | 0x01F0 2016 | AQCTLA | No | Action-Qualifier Control Register for Output A (eHRPWMxA) |
| 0x01F0 0018 | 0x01F0 2018 | AQCTLB | No | Action-Qualifier Control Register for Output B (eHRPWMxB) |
| 0x01F0 001A | 0x01F0 201A | AQSFRC | No | Action-Qualifier Software Force Register |
| 0x01F0 001C | 0x01F0 201C | AQCSFRC | Yes | Action-Qualifier Continuous S/W Force Register Set |
| **Dead-Band Generator Submodule Registers** | | | | |
| 0x01F0 001E | 0x01F0 201E | DBCTL | No | Dead-Band Generator Control Register |
| 0x01F0 0020 | 0x01F0 2020 | DBRED | No | Dead-Band Generator Rising Edge Delay Count Register |
| 0x01F0 0022 | 0x01F0 2022 | DBFED | No | Dead-Band Generator Falling Edge Delay Count Register |
| **PWM-Chopper Submodule Registers** | | | | |
| 0x01F0 003C | 0x01F0 203C | PCCTL | No | PWM-Chopper Control Register |
| **Trip-Zone Submodule Registers** | | | | |
| 0x01F0 0024 | 0x01F0 2024 | TZSEL | No | Trip-Zone Select Register |
| 0x01F0 0028 | 0x01F0 2028 | TZCTL | No | Trip-Zone Control Register |
| 0x01F0 002A | 0x01F0 202A | TZEINT | No | Trip-Zone Enable Interrupt Register |
| 0x01F0 002C | 0x01F0 202C | TZFLG | No | Trip-Zone Flag Register |
| 0x01F0 002E | 0x01F0 202E | TZCLR | No | Trip-Zone Clear Register |
| 0x01F0 0030 | 0x01F0 2030 | TZFRC | No | Trip-Zone Force Register |
| **Event-Trigger Submodule Registers** | | | | |
| 0x01F0 0032 | 0x01F0 2032 | ETSEL | No | Event-Trigger Selection Register |
| 0x01F0 0034 | 0x01F0 2034 | ETPS | No | Event-Trigger Pre-Scale Register |
| 0x01F0 0036 | 0x01F0 2036 | ETFLG | No | Event-Trigger Flag Register |
| 0x01F0 0038 | 0x01F0 2038 | ETCLR | No | Event-Trigger Clear Register |
| 0x01F0 003A | 0x01F0 203A | ETFRC | No | Event-Trigger Force Register |
| **High-Resolution PWM (HRPWM) Submodule Registers** | | | | |
| 0x01F0 1040 | 0x01F0 3040 | HRCNFG | No | HRPWM Configuration Register (1) |

(1) These registers are only available on eHRPWM instances that include the high-resolution PWM (HRPWM) extension; otherwise, these locations are reserved.


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### 5.29.1 Enhanced Pulse Width Modulator (eHRPWM) Timing

PWM refers to PWM outputs on eHRPWM1-6. Table 5-128 shows the PWM timing requirements and Table 5-129, switching characteristics.

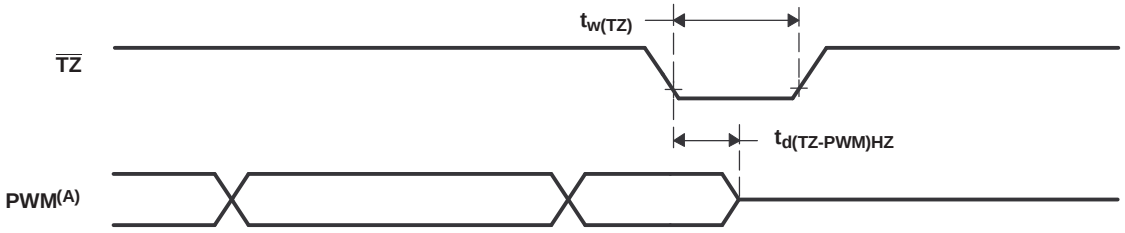
**Table 5-128. Timing Requirements for eHRPWM**

| PARAMETER | | TEST CONDITIONS | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{w(SYNCIN)}$ | Sync input pulse width | Asynchronous | $2t_{c(SCO)}$ | | cycles |
| | | Synchronous | $2t_{c(SCO)}$ | | cycles |

**Table 5-129. Switching Characteristics Over Recommended Operating Conditions for eHRPWM**

| PARAMETER | | TEST CONDITIONS | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{w(PWM)}$ | Pulse duration, PWMx output high/low | | 20 | | 20 | | 26.6 | | ns |
| $t_{w(SYNCOUT)}$ | Sync output pulse width | | $8t_{c(SCO)}$ | | $8t_{c(SCO)}$ | | $8t_{c(SCO)}$ | | cycles |
| $t_{d(PWM)TZA}$ | Delay time, trip input active to PWM forced high<br>Delay time, trip input active to PWM forced low | no pin load; no additional programmable delay | | 25 | | 25 | | 25 | ns |
| $t_{d(TZ-PWM)HZ}$ | Delay time, trip input active to PWM Hi-Z | no additional programmable delay | | 20 | | 20 | | 20 | ns |

### 5.29.2 Trip-Zone Input Timing




A. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

**Figure 5-81. PWM Hi-Z Characteristics**

**Table 5-130. Trip-Zone input Timing Requirements**

| PARAMETER | | TEST CONDITIONS | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{w(TZ)}$ | Pulse duration, $\overline{TZ}$x input low | Asynchronous | $1t_{c(SCO)}$ | | cycles |
| | | Synchronous | $2t_{c(SCO)}$ | | cycles |

Table 5-131 shows the high-resolution PWM switching characteristics.

**Table 5-131. High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)**

| PARAMETER | 1.3V, 1.2V | | | 1.1V | | | 1.0V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Micro Edge Positioning (MEP) step size(1) | | 200 | | | 200 | | | 200 | | ps |

(1) MEP step size will increase with low voltage and high temperature and decrease with high voltage and cold temperature.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## 5.30 Timers

The timers support the following features:

- Configurable as single 64-bit timer or two 32-bit timers
- Period timeouts generate interrupts, DMA events or external pin events
- 8 32-bit compare registers
- Compare matches generate interrupt events
- Capture capability
- 64-bit Watchdog capability (Timer64P1 only)

Table 5-132 lists the timer registers.

**Table 5-132. Timer Registers**

| TIMER64P 0 BYTE ADDRESS | TIMER64P 1 BYTE ADDRESS | TIMER64P 2 BYTE ADDRESS | TIMER64P 3 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|---|---|
| 0x01C2 0000 | 0x01C2 1000 | 0x01F0 C000 | 0x01F0 D000 | REV | Revision Register |
| 0x01C2 0004 | 0x01C2 1004 | 0x01F0 C004 | 0x01F0 D004 | EMUMGT | Emulation Management Register |
| 0x01C2 0008 | 0x01C2 1008 | 0x01F0 C008 | 0x01F0 D008 | GPINTGPEN | GPIO Interrupt and GPIO Enable Register |
| 0x01C2 000C | 0x01C2 100C | 0x01F0 C00C | 0x01F0 D00C | GPDATGPDIR | GPIO Data and GPIO Direction Register |
| 0x01C2 0010 | 0x01C2 1010 | 0x01F0 C010 | 0x01F0 D010 | TIM12 | Timer Counter Register 12 |
| 0x01C2 0014 | 0x01C2 1014 | 0x01F0 C014 | 0x01F0 D014 | TIM34 | Timer Counter Register 34 |
| 0x01C2 0018 | 0x01C2 1018 | 0x01F0 C018 | 0x01F0 D018 | PRD12 | Timer Period Register 12 |
| 0x01C2 001C | 0x01C2 101C | 0x01F0 C01C | 0x01F0 D01C | PRD34 | Timer Period Register 34 |
| 0x01C2 0020 | 0x01C2 1020 | 0x01F0 C020 | 0x01F0 D020 | TCR | Timer Control Register |
| 0x01C2 0024 | 0x01C2 1024 | 0x01F0 C024 | 0x01F0 D024 | TGCR | Timer Global Control Register |
| 0x01C2 0028 | 0x01C2 1028 | 0x01F0 C028 | 0x01F0 D028 | WDTCR | Watchdog Timer Control Register |
| 0x01C2 0034 | 0x01C2 1034 | 0x01F0 C034 | 0x01F0 D034 | REL12 | Timer Reload Register 12 |
| 0x01C2 0038 | 0x01C2 1038 | 0x01F0 C038 | 0x01F0 D038 | REL34 | Timer Reload Register 34 |
| 0x01C2 003C | 0x01C2 103C | 0x01F0 C03C | 0x01F0 D03C | CAP12 | Timer Capture Register 12 |
| 0x01C2 0040 | 0x01C2 1040 | 0x01F0 C040 | 0x01F0 D040 | CAP34 | Timer Capture Register 34 |
| 0x01C2 0044 | 0x01C2 1044 | 0x01F0 C044 | 0x01F0 D044 | INTCTLSTAT | Timer Interrupt Control and Status Register |
| 0x01C2 0060 | 0x01C2 1060 | 0x01F0 C060 | 0x01F0 D060 | CMP0 | Compare Register 0 |
| 0x01C2 0064 | 0x01C2 1064 | 0x01F0 C064 | 0x01F0 D064 | CMP1 | Compare Register 1 |
| 0x01C2 0068 | 0x01C2 1068 | 0x01F0 C068 | 0x01F0 D068 | CMP2 | Compare Register 2 |
| 0x01C2 006C | 0x01C2 106C | 0x01F0 C06C | 0x01F0 D06C | CMP3 | Compare Register 3 |
| 0x01C2 0070 | 0x01C2 1070 | 0x01F0 C070 | 0x01F0 D070 | CMP4 | Compare Register 4 |
| 0x01C2 0074 | 0x01C2 1074 | 0x01F0 C074 | 0x01F0 D074 | CMP5 | Compare Register 5 |
| 0x01C2 0078 | 0x01C2 1078 | 0x01F0 C078 | 0x01F0 D078 | CMP6 | Compare Register 6 |
| 0x01C2 007C | 0x01C2 107C | 0x01F0 C07C | 0x01F0 D07C | CMP7 | Compare Register 7 |

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### 5.30.1 Timer Electrical Data/Timing

**Table 5-133. Timing Requirements for Timer Input(1) (2) (see Figure 5-82)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{c(TM64Px_IN12)}$ | Cycle time, TM64Px_IN12 | 4P | | ns |
| 2 | $t_{w(TINPH)}$ | Pulse duration, TM64Px_IN12 high | 0.45C | 0.55C | ns |
| 3 | $t_{w(TINPL)}$ | Pulse duration, TM64Px_IN12 low | 0.45C | 0.55C | ns |
| 4 | $t_{t(TM64Px_IN12)}$ | Transition time, TM64Px_IN12 | | 0.25P or 10 (3) | ns |

(1) P = OSCIN cycle time in ns.
(2) C = TM64P0_IN12 cycle time in ns.
(3) Whichever is smaller. P = the period of the applied signal. Maintaining transition times as fast as possible is recommended to improve noise immunity on input signals.

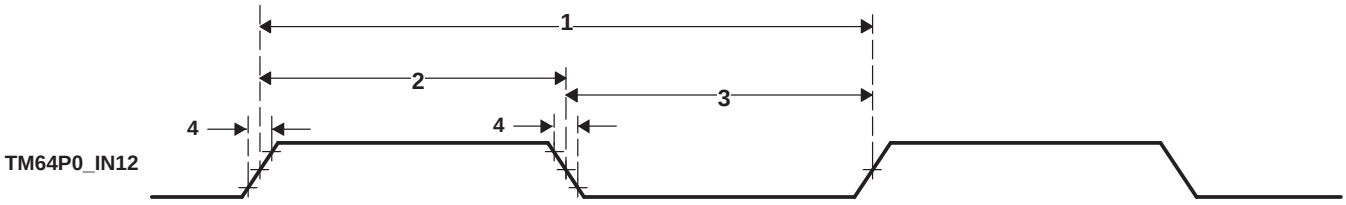


**Figure 5-82. Timer Timing**

**Table 5-134. Switching Characteristics Over Recommended Operating Conditions for Timer Output (1)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 5 | $t_{w(TOUTH)}$ | Pulse duration, TM64P0_OUT12 high | 4P | | ns |
| 6 | $t_{w(TOUTL)}$ | Pulse duration, TM64P0_OUT12 low | 4P | | ns |

(1) P = OSCIN cycle time in ns. For example, when OSCIN frequency is 27 MHz, use P = 37.0$\overline{37}$ ns.

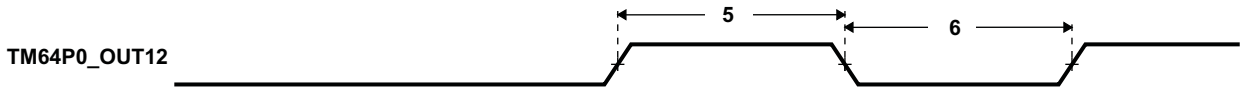


**Figure 5-83. Timer Timing**


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## 5.31 Real Time Clock (RTC)

The RTC provides a time reference to an application running on the device. The current date and time is tracked in a set of counter registers that update once per second. The time can be represented in 12-hour or 24-hour mode. The calendar and time registers are buffered during reads and writes so that updates do not interfere with the accuracy of the time and date.

Alarms are available to interrupt the CPU at a particular time, or at periodic time intervals, such as once per minute or once per day. In addition, the RTC can interrupt the CPU every time the calendar and time registers are updated, or at programmable periodic intervals.

The real-time clock (RTC) provides the following features:

- 100-year calendar (xx00 to xx99)
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 12-hour clock mode (with AM and PM) or 24-hour clock mode
- Alarm interrupt
- Periodic interrupt
- Single interrupt to the CPU
- Supports external 32.768-kHz crystal or external clock source of the same frequency
- Separate isolated power supply

Figure 5-84 shows a block diagram of the RTC.

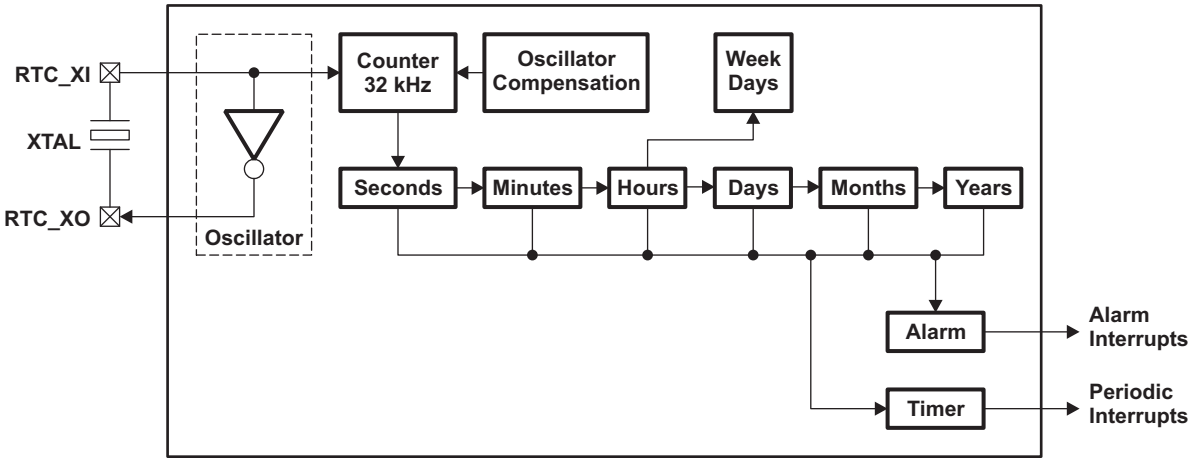


**Figure 5-84. Real-Time Clock Block Diagram**

### 5.31.1 Clock Source

The clock reference for the RTC is an external 32.768-kHz crystal or an external clock source of the same frequency. The RTC also has a separate power supply that is isolated from the rest of the system. When the CPU and other peripherals are without power, the RTC can remain powered to preserve the current time and calendar information. Even if the RTC is not used, it must remain powered when the rest of the device is powered.

The source for the RTC reference clock may be provided by a crystal or by an external clock source. The RTC has an internal oscillator buffer to support direct operation with a crystal. The crystal is connected between pins RTC_XI and RTC_XO. RTC_XI is the input to the on-chip oscillator and RTC_XO is the output from the oscillator back to the crystal.

An external 32.768-kHz clock source may be used instead of a crystal. In such a case, the clock source is connected to RTC_XI, and RTC_XO is left unconnected.

If the RTC is not used, the RTC_XI pin should be held either low or high, RTC_XO should be left unconnected, RTC_CVDD should be connected to the device CVDD and RTC_VSS should remain grounded.

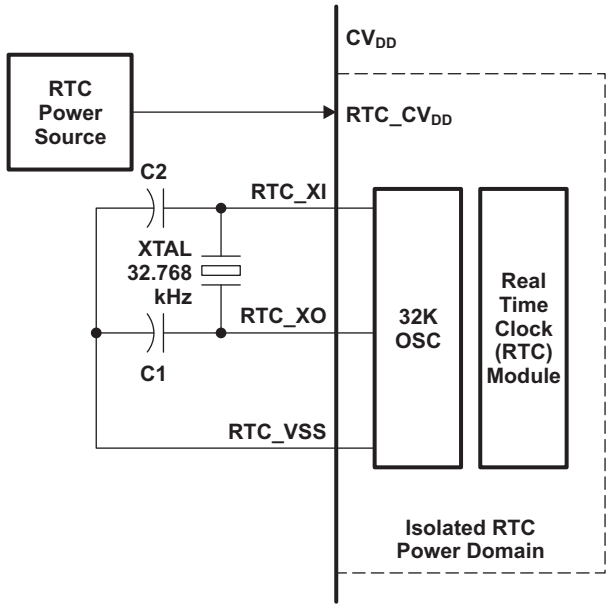


**Figure 5-85. Clock Source**


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### 5.31.2 Real-Time Clock Register Descriptions

**Table 5-135. Real-Time Clock (RTC) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01C2 3000 | SECOND | Seconds Register |
| 0x01C2 3004 | MINUTE | Minutes Register |
| 0x01C2 3008 | HOUR | Hours Register |
| 0x01C2 300C | DAY | Day of the Month Register |
| 0x01C2 3010 | MONTH | Month Register |
| 0x01C2 3014 | YEAR | Year Register |
| 0x01C2 3018 | DOTW | Day of the Week Register |
| 0x01C2 3020 | ALARMSECOND | Alarm Seconds Register |
| 0x01C2 3024 | ALARMMINUTE | Alarm Minutes Register |
| 0x01C2 3028 | ALARMHOUR | Alarm Hours Register |
| 0x01C2 302C | ALARMDAY | Alarm Days Register |
| 0x01C2 3030 | ALARMMONTH | Alarm Months Register |
| 0x01C2 3034 | ALARMYEAR | Alarm Years Register |
| 0x01C2 3040 | CTRL | Control Register |
| 0x01C2 3044 | STATUS | Status Register |
| 0x01C2 3048 | INTERRUPT | Interrupt Enable Register |
| 0x01C2 304C | COMPLSB | Compensation (LSB) Register |
| 0x01C2 3050 | COMPMSB | Compensation (MSB) Register |
| 0x01C2 3054 | OSC | Oscillator Register |
| 0x01C2 3060 | SCRATCH0 | Scratch 0 (General-Purpose) Register |
| 0x01C2 3064 | SCRATCH1 | Scratch 1 (General-Purpose) Register |
| 0x01C2 3068 | SCRATCH2 | Scratch 2 (General-Purpose) Register |
| 0x01C2 306C | KICK0 | Kick 0 (Write Protect) Register |
| 0x01C2 3070 | KICK1 | Kick 1 (Write Protect) Register |

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## 5.32 General-Purpose Input/Output (GPIO)

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, a write to an internal register can control the state driven on the output pin. When configured as an input, the state of the input is detectable by reading the state of an internal register. In addition, the GPIO peripheral can produce CPU interrupts and EDMA events in different interrupt/event generation modes. The GPIO peripheral provides generic connections to external devices. The GPIO pins are grouped into banks of 16 pins per bank (i.e., bank 0 consists of GPIO [0:15]).

The device GPIO peripheral supports the following:

- Up to 144 Pins configurable as GPIO
- External Interrupt and DMA request Capability
  - Every GPIO pin may be configured to generate an interrupt request on detection of rising and/or falling edges on the pin.
  - The interrupt requests within each bank are combined (logical or) to create eight unique bank level interrupt requests.
  - The bank level interrupt service routine may poll the INTSTATx register for its bank to determine which pin(s) have triggered the interrupt.
  - GPIO Banks 0, 1, 2, 3, 4, 5, 6, 7, and 8 Interrupts assigned to ARM INTC Interrupt Requests 42, 43, 44, 45, 46, 47, 48, 49, and 50 respectively
  - GPIO Banks 0, 1, 2, 3, 4, 5, 6, 7, and 8 Interrupts assigned to DSP Events 65, 41, 49, 52, 54, 59, 62, 72, and 75 respectively
  - GPIO Banks 0, 1, 2, 3, 4, and 5 are assigned to EDMA events 6, 7, 22, 23, 28, 29, and 29 respectively on Channel Controller 0 and GPIO Banks 6, 7, and 8 are assigned to EDMA events 16, 17, and 18 respectively on Channel Controller 1.
- Set/clear functionality: Firmware writes 1 to corresponding bit position(s) to set or to clear GPIO signal(s). This allows multiple firmware processes to toggle GPIO output signals without critical section protection (disable interrupts, program GPIO, re-enable interrupts, to prevent context switching to anther process during GPIO programming).
- Separate Input/Output registers
- Output register in addition to set/clear so that, if preferred by firmware, some GPIO output signals can be toggled by direct write to the output register(s).
- Output register, when read, reflects output drive status. This, in addition to the input register reflecting pin status and open-drain I/O cell, allows wired logic be implemented.

The memory map for the GPIO registers is shown in Table 5-136.


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### 5.32.1 GPIO Register Description(s)

**Table 5-136. GPIO Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01E2 6000 | REV | Peripheral Revision Register |
| 0x01E2 6004 | RESERVED | Reserved |
| 0x01E2 6008 | BINTEN | GPIO Interrupt Per-Bank Enable Register |
| **GPIO Banks 0 and 1** | | |
| 0x01E2 6010 | DIR01 | GPIO Banks 0 and 1 Direction Register |
| 0x01E2 6014 | OUT_DATA01 | GPIO Banks 0 and 1 Output Data Register |
| 0x01E2 6018 | SET_DATA01 | GPIO Banks 0 and 1 Set Data Register |
| 0x01E2 601C | CLR_DATA01 | GPIO Banks 0 and 1 Clear Data Register |
| 0x01E2 6020 | IN_DATA01 | GPIO Banks 0 and 1 Input Data Register |
| 0x01E2 6024 | SET_RIS_TRIG01 | GPIO Banks 0 and 1 Set Rising Edge Interrupt Register |
| 0x01E2 6028 | CLR_RIS_TRIG01 | GPIO Banks 0 and 1 Clear Rising Edge Interrupt Register |
| 0x01E2 602C | SET_FAL_TRIG01 | GPIO Banks 0 and 1 Set Falling Edge Interrupt Register |
| 0x01E2 6030 | CLR_FAL_TRIG01 | GPIO Banks 0 and 1 Clear Falling Edge Interrupt Register |
| 0x01E2 6034 | INTSTAT01 | GPIO Banks 0 and 1 Interrupt Status Register |
| **GPIO Banks 2 and 3** | | |
| 0x01E2 6038 | DIR23 | GPIO Banks 2 and 3 Direction Register |
| 0x01E2 603C | OUT_DATA23 | GPIO Banks 2 and 3 Output Data Register |
| 0x01E2 6040 | SET_DATA23 | GPIO Banks 2 and 3 Set Data Register |
| 0x01E2 6044 | CLR_DATA23 | GPIO Banks 2 and 3 Clear Data Register |
| 0x01E2 6048 | IN_DATA23 | GPIO Banks 2 and 3 Input Data Register |
| 0x01E2 604C | SET_RIS_TRIG23 | GPIO Banks 2 and 3 Set Rising Edge Interrupt Register |
| 0x01E2 6050 | CLR_RIS_TRIG23 | GPIO Banks 2 and 3 Clear Rising Edge Interrupt Register |
| 0x01E2 6054 | SET_FAL_TRIG23 | GPIO Banks 2 and 3 Set Falling Edge Interrupt Register |
| 0x01E2 6058 | CLR_FAL_TRIG23 | GPIO Banks 2 and 3 Clear Falling Edge Interrupt Register |
| 0x01E2 605C | INTSTAT23 | GPIO Banks 2 and 3 Interrupt Status Register |
| **GPIO Banks 4 and 5** | | |
| 0x01E2 6060 | DIR45 | GPIO Banks 4 and 5 Direction Register |
| 0x01E2 6064 | OUT_DATA45 | GPIO Banks 4 and 5 Output Data Register |
| 0x01E2 6068 | SET_DATA45 | GPIO Banks 4 and 5 Set Data Register |
| 0x01E2 606C | CLR_DATA45 | GPIO Banks 4 and 5 Clear Data Register |
| 0x01E2 6070 | IN_DATA45 | GPIO Banks 4 and 5 Input Data Register |
| 0x01E2 6074 | SET_RIS_TRIG45 | GPIO Banks 4 and 5 Set Rising Edge Interrupt Register |
| 0x01E2 6078 | CLR_RIS_TRIG45 | GPIO Banks 4 and 5 Clear Rising Edge Interrupt Register |
| 0x01E2 607C | SET_FAL_TRIG45 | GPIO Banks 4 and 5 Set Falling Edge Interrupt Register |
| 0x01E2 6080 | CLR_FAL_TRIG45 | GPIO Banks 4 and 5 Clear Falling Edge Interrupt Register |
| 0x01E2 6084 | INTSTAT45 | GPIO Banks 4 and 5 Interrupt Status Register |

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**Table 5-136. GPIO Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| **GPIO Banks 6 and 7** | | |
| 0x01E2 6088 | DIR67 | GPIO Banks 6 and 7 Direction Register |
| 0x01E2 608C | OUT_DATA67 | GPIO Banks 6 and 7 Output Data Register |
| 0x01E2 6090 | SET_DATA67 | GPIO Banks 6 and 7 Set Data Register |
| 0x01E2 6094 | CLR_DATA67 | GPIO Banks 6 and 7 Clear Data Register |
| 0x01E2 6098 | IN_DATA67 | GPIO Banks 6 and 7 Input Data Register |
| 0x01E2 609C | SET_RIS_TRIG67 | GPIO Banks 6 and 7 Set Rising Edge Interrupt Register |
| 0x01E2 60A0 | CLR_RIS_TRIG67 | GPIO Banks 6 and 7 Clear Rising Edge Interrupt Register |
| 0x01E2 60A4 | SET_FAL_TRIG67 | GPIO Banks 6 and 7 Set Falling Edge Interrupt Register |
| 0x01E2 60A8 | CLR_FAL_TRIG67 | GPIO Banks 6 and 7 Clear Falling Edge Interrupt Register |
| 0x01E2 60AC | INTSTAT67 | GPIO Banks 6 and 7 Interrupt Status Register |
| **GPIO Bank 8** | | |
| 0x01E2 60B0 | DIR8 | GPIO Bank 8 Direction Register |
| 0x01E2 60B4 | OUT_DATA8 | GPIO Bank 8 Output Data Register |
| 0x01E2 60B8 | SET_DATA8 | GPIO Bank 8 Set Data Register |
| 0x01E2 60BC | CLR_DATA8 | GPIO Bank 8 Clear Data Register |
| 0x01E2 60C0 | IN_DATA8 | GPIO Bank 8 Input Data Register |
| 0x01E2 60C4 | SET_RIS_TRIG8 | GPIO Bank 8 Set Rising Edge Interrupt Register |
| 0x01E2 60C8 | CLR_RIS_TRIG8 | GPIO Bank 8 Clear Rising Edge Interrupt Register |
| 0x01E2 60CC | SET_FAL_TRIG8 | GPIO Bank 8 Set Falling Edge Interrupt Register |
| 0x01E2 60D0 | CLR_FAL_TRIG8 | GPIO Bank 8 Clear Falling Edge Interrupt Register |
| 0x01E2 60D4 | INTSTAT8 | GPIO Bank 8 Interrupt Status Register |


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### 5.32.2 GPIO Peripheral Input/Output Electrical Data/Timing

**Table 5-137. Timing Requirements for GPIO Inputs(1) (see Figure 5-86)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(GPIH)}$ | Pulse duration, GP*n*[*m*] as input high | 2C(1) (2) | | ns |
| 2 | $t_{w(GPIL)}$ | Pulse duration, GP*n*[*m*] as input low | 2C(1) (2) | | ns |

(1) The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIx changes through software polling of the GPIO register, the GPIx duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns.

**Table 5-138. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-86)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 3 | $t_{w(GPOH)}$ | Pulse duration, GP*n*[*m*] as output high | 2C(1) (2) | | ns |
| 4 | $t_{w(GPOL)}$ | Pulse duration, GP*n*[*m*] as output low | 2C(1) (2) | | ns |

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
(2) C=SYSCLK4 period in ns.

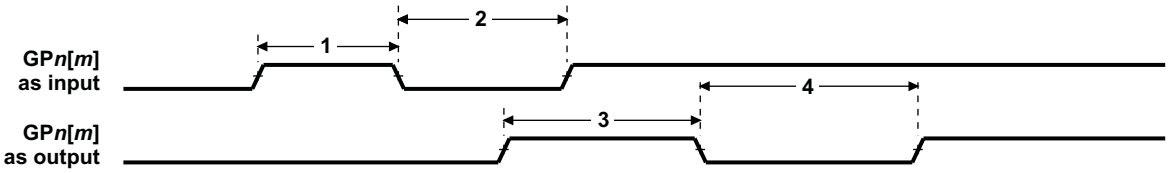


**Figure 5-86. GPIO Port Timing**

### 5.32.3 GPIO Peripheral External Interrupts Electrical Data/Timing

**Table 5-139. Timing Requirements for External Interrupts(1) (see Figure 5-87)**

| NO. | PARAMETER | | 1.3V, 1.2V, 1.1V, 1.0V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| 1 | $t_{w(ILOW)}$ | Width of the external interrupt pulse low | 2C(1) (2) | | ns |
| 2 | $t_{w(IHIGH)}$ | Width of the external interrupt pulse high | 2C(1) (2) | | ns |

(1) The pulse width given is sufficient to generate an interrupt or an EDMA event. However, if a user wants to have the device recognize the GPIO changes through software polling of the GPIO register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.
(2) C=SYSCLK4 period in ns.

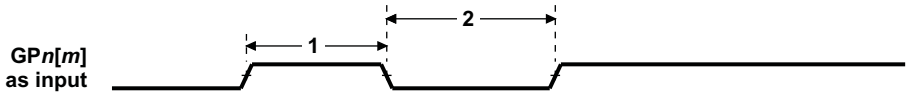


**Figure 5-87. GPIO External Interrupt Timing**

## 5.33 Programmable Real-Time Unit Subsystem (PRUSS)

The Programmable Real-Time Unit Subsystem (PRUSS) consists of

- Two Programmable Real-Time Units (PRU0 and PRU1) and their associated memories
- An Interrupt Controller (INTC) for handling system interrupt events. The INTC also supports posting events back to the device level host CPU.
- A Switched Central Resource (SCR) for connecting the various internal and external masters to the resources inside the PRUSS.

The two PRUs can operate completely independently or in coordination with each other. The PRUs can also work in coordination with the device level host CPU. This is determined by the nature of the program which is loaded into the PRUs instruction memory. Several different signaling mechanisms are available between the two PRUs and the device level host CPU.

The PRUs are optimized for performing embedded tasks that require manipulation of packed memory mapped data structures, handling of system events that have tight realtime constraints and interfacing with systems external to the device.

The PRUSS comprises various distinct addressable regions. Externally the subsystem presents a single 64Kbyte range of addresses. The internal interconnect bus (also called switched central resource, or SCR) of the PRUSS decodes accesses for each of the individual regions. The PRUSS memory map is documented in Table 5-140 and in Table 5-141. Note that these two memory maps are implemented inside the PRUSS and are local to the components of the PRUSS.

**Table 5-140. Programmable Real-Time Unit Subsystem (PRUSS) Local Instruction Space Memory Map**

| BYTE ADDRESS | PRU0 | PRU1 |
|---|---|---|
| 0x0000 0000 - 0x0000 0FFF | PRU0 Instruction RAM | PRU1 Instruction RAM |

**Table 5-141. Programmable Real-Time Unit Subsystem (PRUSS) Local Data Space Memory Map**

| BYTE ADDRESS | PRU0 | PRU1 |
|---|---|---|
| 0x0000 0000 - 0x0000 01FF | Data RAM 0 (1) | Data RAM 1 (1) |
| 0x0000 0200 - 0x0000 1FFF | Reserved | Reserved |
| 0x0000 2000 - 0x0000 21FF | Data RAM 1 (1) | Data RAM 0 (1) |
| 0x0000 2200 - 0x0000 3FFF | Reserved | Reserved |
| 0x0000 4000 - 0x0000 6FFF | INTC Registers | INTC Registers |
| 0x0000 7000 - 0x0000 73FF | PRU0 Control Registers | PRU0 Control Registers |
| 0x0000 7400 - 0x0000 77FF | Reserved | Reserved |
| 0x0000 7800 - 0x0000 7BFF | PRU1 Control Registers | PRU1 Control Registers |
| 0x0000 7C00 - 0xFFFF FFFF | Reserved | Reserved |

(1) Note that PRU0 accesses Data RAM**0** at address 0x0000 0000, also PRU1 accesses Data RAM**1** at address 0x0000 0000. Data RAM0 is intended to be the primary data memory for PRU0 and Data RAM1 is intended to be the primary data memory for PRU1. However for passing information between PRUs, each PRU can access the data ram of the 'other' PRU through address 0x0000 2000.

The global view of the PRUSS internal memories and control ports is documented in Table 5-142. The offset addresses of each region are implemented inside the PRUSS but the global device memory mapping places the PRUSS slave port in the address range 0x01C3 0000-0x01C3 FFFF. The PRU0 and PRU1 can use either the local or global addresses to access their internal memories, but using the local addresses will provide access time several cycles faster than using the global addresses. This is because when accessing via the global address the access needs to be routed through the switch fabric outside PRUSS and back in through the PRUSS slave port.


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**Table 5-142. Programmable Real-Time Unit Subsystem (PRUSS) Global Memory Map**

| BYTE ADDRESS | REGION |
|---|---|
| 0x01C3 0000 - 0x01C3 01FF | Data RAM 0 |
| 0x01C3 0200 - 0x01C3 1FFF | Reserved |
| 0x01C3 2000 - 0x01C3 21FF | Data RAM 1 |
| 0x01C3 2200 - 0x01C3 3FFF | Reserved |
| 0x01C3 4000 - 0x01C3 6FFF | INTC Registers |
| 0x01C3 7000 - 0x01C3 73FF | PRU0 Control Registers |
| 0x01C3 7400 - 0x01C3 77FF | PRU0 Debug Registers |
| 0x01C3 7800 - 0x01C3 7BFF | PRU1 Control Registers |
| 0x01C3 7C00 - 0x01C3 7FFF | PRU1 Debug Registers |
| 0x01C3 8000 - 0x01C3 8FFF | PRU0 Instruction RAM |
| 0x01C3 9000 - 0x01C3 BFFF | Reserved |
| 0x01C3 C000 - 0x01C3 CFFF | PRU1 Instruction RAM |
| 0x01C3 D000 - 0x01C3 FFFF | Reserved |

Each of the PRUs can access the rest of the device memory (including memory mapped peripheral and configuration registers) using the global memory space addresses

### *5.33.1 PRUSS Register Descriptions*

**Table 5-143. Programmable Real-Time Unit Subsystem (PRUSS) Control / Status Registers**

| PRU0 BYTE ADDRESS | PRU1 BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|---|
| 0x01C3 7000 | 0x01C3 7800 | CONTROL | PRU Control Register |
| 0x01C3 7004 | 0x01C3 7804 | STATUS | PRU Status Register |
| 0x01C3 7008 | 0x01C3 7808 | WAKEUP | PRU Wakeup Enable Register |
| 0x01C3 700C | 0x01C3 780C | CYCLCNT | PRU Cycle Count |
| 0x01C3 7010 | 0x01C3 7810 | STALLCNT | PRU Stall Count |
| 0x01C3 7020 | 0x01C3 7820 | CONTABBLKIDX0 | PRU Constant Table Block Index Register 0 |
| 0x01C3 7028 | 0x01C3 7828 | CONTABPROPTR0 | PRU Constant Table Programmable Pointer Register 0 |
| 0x01C3 702C | 0x01C3 782C | CONTABPROPTR1 | PRU Constant Table Programmable Pointer Register 1 |
| 0x01C37400 - 0x01C3747C | 0x01C3 7C00 - 0x01C3 7C7C | INTGPR0 – INTGPR31 | PRU Internal General Purpose Register 0 (for Debug) |
| 0x01C37480 - 0x01C374FC | 0x01C3 7C80 - 0x01C3 7CFC | INTCTER0 – INTCTER31 | PRU Internal General Purpose Register 0 (for Debug) |

**Table 5-144. Programmable Real-Time Unit Subsystem Interrupt Controller (PRUSS INTC) Registers**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01C3 4000 | REVID | Revision ID Register |
| 0x01C3 4004 | CONTROL | Control Register |
| 0x01C3 4010 | GLBLEN | Global Enable Register |
| 0x01C3 401C | GLBLNSTLVL | Global Nesting Level Register |
| 0x01C3 4020 | STATIDXSET | System Interrupt Status Indexed Set Register |
| 0x01C3 4024 | STATIDXCLR | System Interrupt Status Indexed Clear Register |
| 0x01C3 4028 | ENIDXSET | System Interrupt Enable Indexed Set Register |
| 0x01C3 402C | ENIDXCLR | System Interrupt Enable Indexed Clear Register |
| 0x01C3 4034 | HSTINTENIDXSET | Host Interrupt Enable Indexed Set Register |
| 0x01C3 4038 | HSTINTENIDXCLR | Host Interrupt Enable Indexed Clear Register |
| 0x01C3 4080 | GLBLPRIIDX | Global Prioritized Index Register |
| 0x01C3 4200 | STATSETINT0 | System Interrupt Status Raw/Set Register 0 |

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**Table 5-144. Programmable Real-Time Unit Subsystem Interrupt Controller (PRUSS INTC) Registers (continued)**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|---|---|
| 0x01C3 4204 | STATSETINT1 | System Interrupt Status Raw/Set Register 1 |
| 0x01C3 4280 | STATCLRINT0 | System Interrupt Status Enabled/Clear Register 0 |
| 0x01C3 4284 | STATCLRINT1 | System Interrupt Status Enabled/Clear Register 1 |
| 0x01C3 4300 | ENABLESET0 | System Interrupt Enable Set Register 0 |
| 0x01C3 4304 | ENABLESET1 | System Interrupt Enable Set Register 1 |
| 0x01C3 4380 | ENABLECLR0 | System Interrupt Enable Clear Register 0 |
| 0x01C3 4384 | ENABLECLR1 | System Interrupt Enable Clear Register 1 |
| 0x01C3 4400 - 0x01C3 4440 | CHANMAP0 - CHANMAP15 | Channel Map Registers 0-15 |
| 0x01C3 4800 - 0x01C3 4808 | HOSTMAP0 - HOSTMAP2 | Host Map Register 0-2 |
| 0x01C3 4900 - 0x01C3 4928 | HOSTINTPRIIDX0 - HOSTINTPRIIDX9 | Host Interrupt Prioritized Index Registers 0-9 |
| 0x01C3 4D00 | POLARITY0 | System Interrupt Polarity Register 0 |
| 0x01C3 4D04 | POLARITY1 | System Interrupt Polarity Register 1 |
| 0x01C3 4D80 | TYPE0 | System Interrupt Type Register 0 |
| 0x01C3 4D84 | TYPE1 | System Interrupt Type Register 1 |
| 0x01C3 5100 - 0x01C3 5128 | HOSTINTNSTLVL0- HOSTINTNSTLVL9 | Host Interrupt Nesting Level Registers 0-9 |
| 0x01C3 5500 | HOSTINTEN | Host Interrupt Enable Register |


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## 5.34 Emulation Logic

This section describes the steps to use a third party debugger on the ARM926EJ-S within the device. The debug capabilities and features for DSP and ARM are as shown below.

**DSP:**

- Basic Debug
  - Execution Control
  - System Visibility
- Real-Time Debug
  - Interrupts serviced while halted
  - Low/non-intrusive system visibility while running
- Advanced Debug
  - Global Start
  - Global Stop
  - Specify targeted memory level(s) during memory accesses
  - HSRTDX (High Speed Real Time Data eXchange)
- Advanced System Control
  - Subsystem reset via debug
  - Peripheral notification of debug events
  - Cache-coherent debug accesses
- Analysis Actions
  - Stop program execution
  - Generate debug interrupt
  - Benchmarking with counters
  - External trigger generation
  - Debug state machine state transition
  - Combinational and Sequential event generation
- Analysis Events
  - Program event detection
  - Data event detection
  - External trigger Detection
  - System event detection (i.e. cache miss)
  - Debug state machine state detection
- Analysis Configuration
  - Application access
  - Debugger access

**Table 5-145. DSP Debug Features**

| Category | Hardware Feature | Availability |
|---|---|---|
| Basic Debug | Software breakpoint | Unlimited |
| | Hardware breakpoint | Up to 10 HWBPs, including:<br>4 precise(1) HWBPs inside DSP core and one of them is associated with a counter.<br>2 imprecise(1) HWBPs from AET.<br>4 imprecise(1) HWBPs from AET which are shared for watch point. |

(1) Precise hardware breakpoints will halt the processor immediately prior to the execution of the selected instruction. Imprecise breakpoints will halt the processor some number of cycles after the selected instruction depending on device conditions.

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**Table 5-145. DSP Debug Features (continued)**

| Category | Hardware Feature | Availability |
|---|---|---|
| Analysis | Watch point | Up to 4 watch points, which are shared with HWBPs, and can also be used as 2 watch points with data (32 bits) |
| | Watch point with Data | Up to 2, Which can also be used as 4 watch points. |
| | Counters/timers | 1x64-bits (cycle only) + 2x32-bits (water mark counters) |
| | External Event Trigger In | 1 |
| | External Event Trigger Out | 1 |

**ARM:**

- Basic Debug
  - Execution Control
  - System Visibility
- Advanced Debug
  - Global Start
  - Global Stop
- Advanced System Control
  - Subsystem reset via debug
  - Peripheral notification of debug events
  - Cache-coherent debug accesses
- Program Trace
  - Program flow corruption
  - Code coverage
  - Path coverage
  - Thread/interrupt synchronization problems
- Data Trace
  - Memory corruption
- Timing Trace
  - Profiling
- Analysis Actions
  - Stop program execution
  - Control trace streams
  - Generate debug interrupt
  - Benchmarking with counters
  - External trigger generation
  - Debug state machine state transition
  - Combinational and Sequential event generation
- Analysis Events
  - Program event detection
  - Data event detection
  - External trigger Detection
  - System event detection (i.e. cache miss)
  - Debug state machine state detection
- Analysis Configuration
  - Application access
  - Debugger access


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**Table 5-146. ARM Debug Features**

| Category | Hardware Feature | Availability |
|---|---|---|
| Basic Debug | Software breakpoint | Unlimited |
| | Hardware breakpoint | Up to 14 HWBPs, including:<br>2 precise(1) HWBP inside ARM core which are shared with watch points.<br>8 imprecise(1) HWBPs from ETM's address comparators, which are shared with trace function, and can be used as watch points.<br>4 imprecise(1) HWBPs from ICECrusher. |
| Analysis | Watch point | Up to 6 watch points, including:<br>2 from ARM core which is shared with HWBPs and can be associated with a data.<br>8 from ETM's address comparators, which are shared with trace function, and HWBPs. |
| | Watch point with Data | 2 from ARM core which is shared with HWBPs.<br>8 watch points from ETM can be associated with a data comparator, and ETM has total 4 data comparators. |
| | Counters/timers | 3x32-bit (1 cycle ; 2 event) |
| | External Event Trigger In | 1 |
| | External Event Trigger Out | 1 |
| | Internal Cross-Triggering Signals | One between ARM and DSP |
| Trace Control | Address range for trace | 4 |
| | Data qualification for trace | 2 |
| | System events for trace control | 20 |
| | Counters/Timers for trace control | 2x16-bit |
| | State Machines/Sequencers | 1x3-State State Machine |
| | Context/Thread ID Comparator | 1 |
| | Independent trigger control units | 12 |
| On-chip Trace Capture | Capture depth PC | 4k bytes ETB |
| | Capture depth PC + Timing | 4k bytes ETB |
| | Application accessible | Y |

(1) Precise hardware breakpoints will halt the processor immediately prior to the execution of the selected instruction. Imprecise breakpoints will halt the processor some number of cycles after the selected instruction depending on device conditions.

### 5.34.1 JTAG Port Description

The device target debug interface uses the five standard IEEE 1149.1(JTAG) signals ($\overline{\text{TRST}}$, TCK, TMS, TDI, and TDO), a return clock (RTCK) due to the clocking requirements of the ARM926EJ-S and emulation signals EMU0 and EMU1.

TRST holds the debug and boundary scan logic in reset (normal DSP operation) when pulled low (its default state). Since TRST has an internal pull-down resistor, this ensures that at power up the device functions in its normal (non-test) operation mode if TRST is not connected. Otherwise, TRST should be driven inactive by the emulator or boundary scan controller. Boundary scan test cannot be performed while the TRST pin is pulled low.

**Table 5-147. JTAG Port Description**

| PIN | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| $\overline{\text{TRST}}$ | I | Test Logic Reset | When asserted (active low) causes all test and debug logic in the device to be reset along with the IEEE 1149.1 interface |
| TCK | I | Test Clock | This is the test clock used to drive an IEEE 1149.1 TAP state machine and logic.Depending on the emulator attached to , this is a free running clock or a gated clock depending on RTCK monitoring. |
| RTCK | O | Returned Test Clock | Synchronized TCK. Depending on the emulator attached to, the JTAG signals are clocked from RTCK or RTCK is monitored by the emulator to gate TCK. |
| TMS | I | Test Mode Select | Directs the next state of the IEEE 1149.1 test access port state machine |

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**Table 5-147. JTAG Port Description (continued)**

| PIN | TYPE | NAME | DESCRIPTION |
|---|---|---|---|
| TDI | I | Test Data Input | Scan data input to the device |
| TDO | O | Test Data Output | Scan data output of the device |
| EMU0 | I/O | Emulation 0 | Channel 0 trigger + HSRTDX |
| EMU1 | I/O | Emulation 1 | Channel 1 trigger + HSRTDX |

### 5.34.2 Scan Chain Configuration Parameters

Table 5-148 shows the TAP configuration details required to configure the router/emulator for this device.

**Table 5-148. JTAG Port Description**

| Router Port ID | Default TAP | TAP Name | Tap IR Length |
|---|---|---|---|
| 17 | No | C674x | 38 |
| 18 | No | ARM926 | 4 |
| 19 | No | ETB | 4 |

The router is revision C and has a 6-bit IR length.

### 5.34.3 Initial Scan Chain Configuration

The first level of debug interface that sees the scan controller is the TAP router module. The debugger can configure the TAP router for serially linking up to 16 TAP controllers or individually scanning one of the TAP controllers without disrupting the IR state of the other TAPs.

#### 5.34.3.1 Adding TAPS to the Scan Chain

The TAP router must be programmed to add additional TAPs to the scan chain. The following JTAG scans must be completed to add the ARM926EJ-S to the scan chain.

A Power-On Reset (POR) or the JTAG Test-Logic Reset state configures the TAP router to contain only the router's TAP.

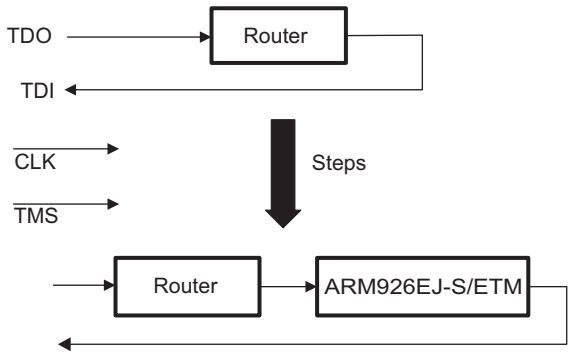


**Figure 5-88. Adding ARM926EJ-S to the scan chain**

**Pre-amble**: The device whose data reaches the emulator first is listed first in the board configuration file. This device is a pre-amble for all the other devices. This device has the lowest device ID.

**Post-amble**: The device whose data reaches the emulator last is listed last in the board configuration file. This device is a post-amble for all the other devices. This device has the highest device ID.


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- Function : Update the JTAG preamble and post-amble counts.
  - Parameter : The IR pre-amble count is '0'.
  - Parameter : The IR post-amble count is '0'.
  - Parameter : The DR pre-amble count is '0'.
  - Parameter : The DR post-amble count is '0'.
  - Parameter : The IR main count is '6'.
  - Parameter : The DR main count is '1'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000007'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '8'.
  - Parameter : The send data value is '0x00000089'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000002'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Embed the port address in next command.
  - Parameter : The port address field is '0x0f000000'.
  - Parameter : The port address value is '3'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '32'.
  - Parameter : The send data value is '0xa2002108'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only all-ones JTAG IR/DR scan.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'run-test/idle'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is 'all-ones'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Wait for a minimum number of TCLK pulses.
  - Parameter : The count of TCLK pulses is '10'.

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- Function : Update the JTAG preamble and post-amble counts.
  - Parameter : The IR pre-amble count is '0'.
  - Parameter : The IR post-amble count is '6'.
  - Parameter : The DR pre-amble count is '0'.
  - Parameter : The DR post-amble count is '1'.
  - Parameter : The IR main count is '4'.
  - Parameter : The DR main count is '1'.

The initial scan chain contains only the TAP router module. The following steps must be completed in order to add ETB TAP to the scan chain.

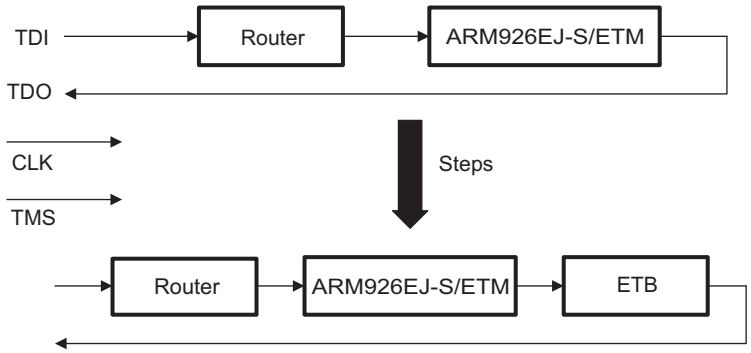


**Figure 5-89. Adding ETB to the scan chain**

- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000007'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '8'.
  - Parameter : The send data value is '0x00000089'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'pause-ir'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is '0x00000002'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Embed the port address in next command.
  - Parameter : The port address field is '0x0f000000'.
  - Parameter : The port address value is '3'.


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- Function : Do a send-only JTAG IR/DR scan.
  - Parameter : The route to JTAG shift state is 'shortest transition'.
  - Parameter : The JTAG shift state is 'shift-dr'.
  - Parameter : The JTAG destination state is 'pause-dr'.
  - Parameter : The bit length of the command is '32'.
  - Parameter : The send data value is '0xa3302108'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Do a send-only all-ones JTAG IR/DR scan.
  - Parameter : The JTAG shift state is 'shift-ir'.
  - Parameter : The JTAG destination state is 'run-test/idle'.
  - Parameter : The bit length of the command is '6'.
  - Parameter : The send data value is 'all-ones'.
  - Parameter : The actual receive data is 'discarded'.
- Function : Wait for a minimum number of TCLK pulses.
  - Parameter : The count of TCLK pulses is '10'.
- Function : Update the JTAG preamble and post-amble counts.
  - Parameter : The IR pre-amble count is '0'.
  - Parameter : The IR post-amble count is '6 + 4'.
  - Parameter : The DR pre-amble count is '0'.
  - Parameter : The DR post-amble count is '1 + 1'.
  - Parameter : The IR main count is '4'.
  - Parameter : The DR main count is '1'.

### 5.34.4 IEEE 1149.1 JTAG

The JTAG(1) interface is used for BSDL testing and emulation of the device.

The device requires that both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ be asserted upon power up to be properly initialized. While $\overline{\text{RESET}}$ initializes the device, $\overline{\text{TRST}}$ initializes the device's emulation logic. Both resets are required for proper operation.

While both $\overline{\text{TRST}}$ and $\overline{\text{RESET}}$ need to be asserted upon power up, only $\overline{\text{RESET}}$ needs to be released for the device to boot properly. $\overline{\text{TRST}}$ may be asserted indefinitely for normal operation, keeping the JTAG port interface and device's emulation logic in the reset state.

$\overline{\text{TRST}}$ only needs to be released when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality. Note: $\overline{\text{TRST}}$ is synchronous and ***must*** be clocked by TCK; otherwise, the boundary scan logic may not respond as expected after $\overline{\text{TRST}}$ is asserted.

$\overline{\text{RESET}}$ must be released only in order for boundary-scan JTAG to read the variant field of IDCODE correctly. Other boundary-scan instructions work correctly independent of current state of $\overline{\text{RESET}}$.

For maximum reliability, the device includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the device's internal emulation logic will always be properly initialized.

JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a pullup resistor on $\overline{\text{TRST}}$.

When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary scan operations.

(1) IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

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### 5.34.4.1 JTAG Peripheral Register Description(s) – JTAG ID Register (DEVIDR0)

**Table 5-149. DEVIDR0 Register**

| BYTE ADDRESS | ACRONYM | REGISTER DESCRIPTION | COMMENTS |
|---|---|---|---|
| 0x01C1 4018 | DEVIDR0 | JTAG Identification Register | Read-only. Provides 32-bit JTAG ID of the device. |

The JTAG ID register is a read-only register that identifies the JTAG/Device ID. For the device, the JTAG ID register resides at address location 0x01C1 4018. The register hex value for each silicon revision is:

- 0x0B7D 102F for silicon revision 1.0
- 0x0B7D 102F for silicon revision 1.1
- 0x1B7D 102F for silicon revision 2.0

For the actual register bit names and their associated bit field descriptions, see Figure 5-90 and Table 5-150.

| 31-28 | 27-12 | 11-1 | 0 |
|---|---|---|---|
| VARIANT (4-Bit) | PART NUMBER (16-Bit) | MANUFACTURER (11-Bit) | LSB |
| R-xxxx | R-1011 0111 1101 0001 | R-0000 0010 111 | R-1 |

LEGEND: R = Read, W = Write, n = value at reset

**Figure 5-90. JTAG ID (DEVIDR0) Register Description - Register Value**

**Table 5-150. JTAG ID Register Selection Bit Descriptions**

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 31:28 | VARIANT | Variant (4-Bit) value |
| 27:12 | PART NUMBER | Part Number (16-Bit) value |
| 11-1 | MANUFACTURER | Manufacturer (11-Bit) value |
| 0 | LSB | LSB. This bit is read as a "1". |


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### 5.34.4.2 JTAG Test-Port Electrical Data/Timing

**Table 5-151. Timing Requirements for JTAG Test Port (see Figure 5-91)**

| No. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | $t_{c(TCK)}$ | Cycle time, TCK | 40 | | 50 | | 66.6 | | ns |
| 2 | $t_{w(TCKH)}$ | Pulse duration, TCK high | 16 | | 20 | | 26.6 | | ns |
| 3 | $t_{w(TCKL)}$ | Pulse duration, TCK low | 16 | | 20 | | 26.6 | | ns |
| 4 | $t_{c(RTCK)}$ | Cycle time, RTCK | 40 | | 50 | | 66.6 | | ns |
| 5 | $t_{w(RTCKH)}$ | Pulse duration, RTCK high | 16 | | 20 | | 26.6 | | ns |
| 6 | $t_{w(RTCKL)}$ | Pulse duration, RTCK low | 16 | | 20 | | 26.6 | | ns |
| 7 | $t_{su(TDIV-RTCKH)}$ | Setup time, TDI/TMS/$\overline{TRST}$ valid before RTCK high | 4 | | 4 | | 4 | | ns |
| 8 | $t_{h(RTCKH-TDIV)}$ | Hold time, TDI/TMS/$\overline{TRST}$ valid after RTCK high | 4 | | 6 | | 8 | | ns |

**Table 5-152. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 5-91)**

| No. | PARAMETER | | 1.3V, 1.2V | | 1.1V | | 1.0V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| 9 | $t_{d(RTCKL-TDOV)}$ | Delay time, RTCK low to TDO valid | | 18 | | 23 | | 31 | ns |

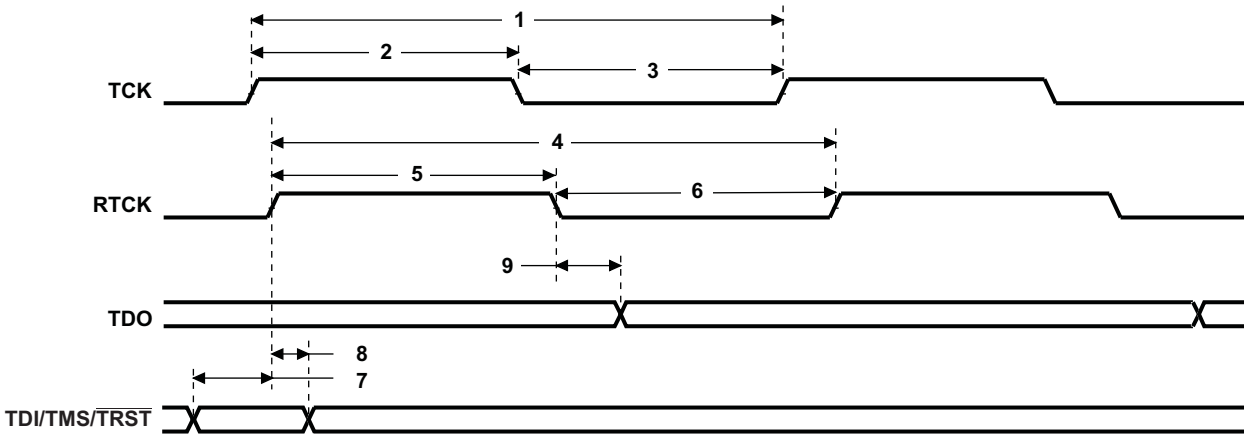


**Figure 5-91. JTAG Test-Port Timing**

### *5.34.5 JTAG 1149.1 Boundary Scan Considerations*

To use boundary scan, the following sequence should be followed:

- Execute a valid reset sequence and exit reset
- Wait at least 6000 OSCIN clock cycles
- Enter boundary scan mode using the JTAG pins

No specific value is required on the EMU0 and EMU1 pins for boundary scan testing. If TRST is not driven by the boundary scan tool or tester, TRST should be externally pulled high during boundary scan testing.

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# 6 Device and Documentation Support

## 6.1 Device Support

### 6.1.1 Development Support

TI offers an extensive line of development tools for the device platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the device applications:

**Software Development Tools:**

Code Composer Studio™ Integrated Development Environment (IDE): including Editor

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any application.

**Hardware Development Tools:**

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the device, visit the Texas Instruments web site on the Worldwide Web at http://www.ti.com uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### 6.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: X, P or NULL (e.g., OMAP-L138). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications.

**P** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

**NULL** Fully-qualified production device.

Support tool development evolutionary flow:

**TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Null devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.


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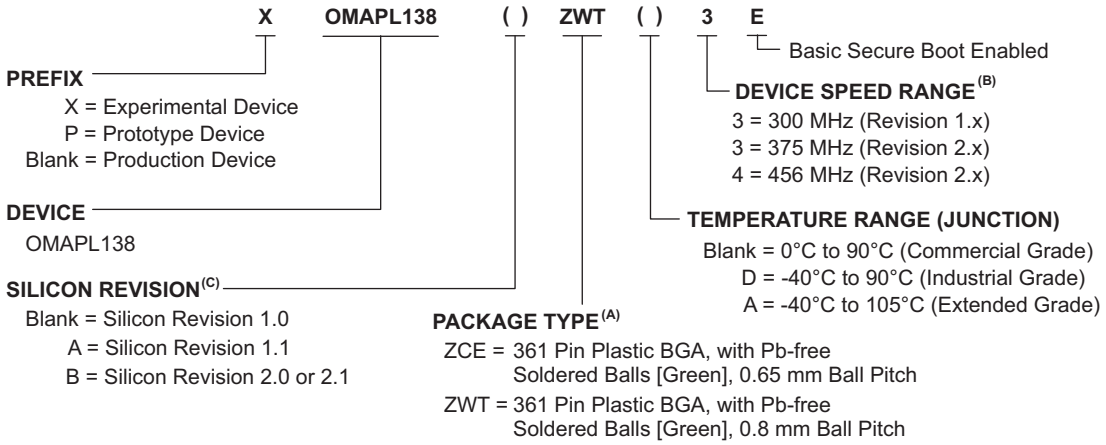
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZWT), the temperature range (for example, "Blank" is the commercial temperature range), and the device speed range in megahertz (for example, "Blank" is the default).

Figure 6-1 provides a legend for reading the complete device.




A. BGA = Ball Grid Array

B. The device speed range symbolization indicates the maximum CPU frequency when the core voltage $CV_{DD}$ is set to 1.2 V.

C. Parts marked revision B are silicon revision 2.1 if '2.1' is marked on the package, and silicon revision 2.0 if there is no '2.1' marking.

**Figure 6-1. Device Nomenclature**

## 6.2 Documentation Support

The following documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box.

**DSP Reference Guides**

**SPRUG82** ***TMS320C674x DSP Cache User's Guide.*** Explains the fundamentals of memory caches and describes how the two-level cache-based internal memory architecture in the TMS320C674x digital signal processor (DSP) can be efficiently used in DSP applications. Shows how to maintain coherence with external memory, how to use DMA to reduce memory latencies, and how to optimize your code to improve cache efficiency. The internal memory architecture in the C674x DSP is organized in a two-level hierarchy consisting of a dedicated program cache (L1P) and a dedicated data cache (L1D) on the first level. Accesses by the CPU to the these first level caches can complete without CPU pipeline stalls. If the data requested by the CPU is not contained in cache, it is fetched from the next lower memory level, L2 or external memory.

**SPRUFE8** ***TMS320C674x DSP CPU and Instruction Set Reference Guide.*** Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C674x digital signal processors (DSPs). The C674x DSP is an enhancement of the C64x+ and C67x+ DSPs with added functionality and an expanded instruction set.

**SPRUFK5** ***TMS320C674x DSP Megamodule Reference Guide.*** Describes the TMS320C674x digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

**SPRUFK9** ***TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the device.

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**SPRUGM7** ***OMAP-L138 Applications Processor System Reference Guide.*** Describes the System-on-Chip (SoC) system. The SoC system includes TI's standard TMS320C674x Megamodule and several blocks of internal memory (L1P, L1D, and L2).

**SPRUGQ9** ***TMS320C674x/OMAP-L1x Processor Security User's Guide***. Provides an overview of the security concepts implemented on TI Basic Secure Boot devices.

## 6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.


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# 7 Mechanical Packaging and Orderable Information

This section describes the orderable part numbers, packaging options, materials, thermal and mechanical parameters.

## 7.1 Thermal Data for ZCE Package

The following table(s) show the thermal resistance characteristics for the PBGA–ZCE mechanical package.

**Table 7-1. Thermal Resistance Characteristics (PBGA Package) [ZCE]**

| NO. | | | °C/W(1) | AIR FLOW (m/s)(2) |
|---|---|---|---|---|
| 1 | $R\Theta_{JC}$ | Junction-to-case | 7.6 | N/A |
| 2 | $R\Theta_{JB}$ | Junction-to-board | 11.3 | N /A |
| 3 | $R\Theta_{JA}$ | Junction-to-free air | 23.9 | 0.00 |
| 4 | $R\Theta_{JMA}$ | Junction-to-moving air | 21.2 | 0.50 |
| 5 | | | 20.3 | 1.00 |
| 6 | | | 19.5 | 2.00 |
| 7 | | | 18.6 | 4.00 |
| 8 | $Psi_{JT}$ | Junction-to-package top | 0.2 | 0.00 |
| 9 | | | 0.3 | 0.50 |
| 10 | | | 0.3 | 1.00 |
| 11 | | | 0.4 | 2.00 |
| 12 | | | 0.5 | 4.00 |
| 13 | $Psi_{JB}$ | Junction-to-board | 11.2 | 0.00 |
| 14 | | | 11.1 | 0.50 |
| 15 | | | 11.1 | 1.00 |
| 16 | | | 11.0 | 2.00 |
| 17 | | | 10.9 | 4.00 |

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. Power dissipation of 500 mW and ambient temp of 70C assumed. PCB with 2oz (70um) top and bottom copper thickness and 1.5oz (50um) inner copper thickness

(2) m/s = meters per second

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## 7.2 Thermal Data for ZWT Package

The following table(s) show the thermal resistance characteristics for the PBGA–ZWT mechanical package.

**Table 7-2. Thermal Resistance Characteristics (PBGA Package) [ZWT]**

| NO. | | | °C/W(1) | AIR FLOW (m/s)(2) |
|---|---|---|---|---|
| 1 | $R\Theta_{JC}$ | Junction-to-case | 7.3 | N/A |
| 2 | $R\Theta_{JB}$ | Junction-to-board | 12.4 | N /A |
| 3 | $R\Theta_{JA}$ | Junction-to-free air | 23.7 | 0.00 |
| 4 | $R\Theta_{JMA}$ | Junction-to-moving air | 21.0 | 0.50 |
| 5 | | | 20.1 | 1.00 |
| 6 | | | 19.3 | 2.00 |
| 7 | | | 18.4 | 4.00 |
| 8 | $Psi_{JT}$ | Junction-to-package top | 0.2 | 0.00 |
| 9 | | | 0.3 | 0.50 |
| 10 | | | 0.3 | 1.00 |
| 11 | | | 0.4 | 2.00 |
| 12 | | | 0.5 | 4.00 |
| 13 | $Psi_{JB}$ | Junction-to-board | 12.3 | 0.00 |
| 14 | | | 12.2 | 0.50 |
| 15 | | | 12.1 | 1.00 |
| 16 | | | 12.0 | 2.00 |
| 17 | | | 11.9 | 4.00 |

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. Power dissipation of 1W and ambient temp of 70C assumed. PCB with 2oz (70um) top and bottom copper thickness and 1.5oz (50um) inner copper thickness

(2) m/s = meters per second


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| OMAPL138BZCE3 | ACTIVE | NFBGA | ZCE | 361 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZCE4 | ACTIVE | NFBGA | ZCE | 361 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZCEA3 | ACTIVE | NFBGA | ZCE | 361 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZCEA3E | ACTIVE | NFBGA | ZCE | 361 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZCED4 | ACTIVE | NFBGA | ZCE | 361 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZCED4E | ACTIVE | NFBGA | ZCE | 361 | | TBD | Call TI | Call TI | |
| OMAPL138BZWT3 | ACTIVE | NFBGA | ZWT | 361 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZWT4 | ACTIVE | NFBGA | ZWT | 361 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZWTA3 | ACTIVE | NFBGA | ZWT | 361 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZWTA3E | ACTIVE | NFBGA | ZWT | 361 | | TBD | Call TI | Call TI | |
| OMAPL138BZWTD4 | ACTIVE | NFBGA | ZWT | 361 | 1 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |
| OMAPL138BZWTD4E | ACTIVE | NFBGA | ZWT | 361 | 90 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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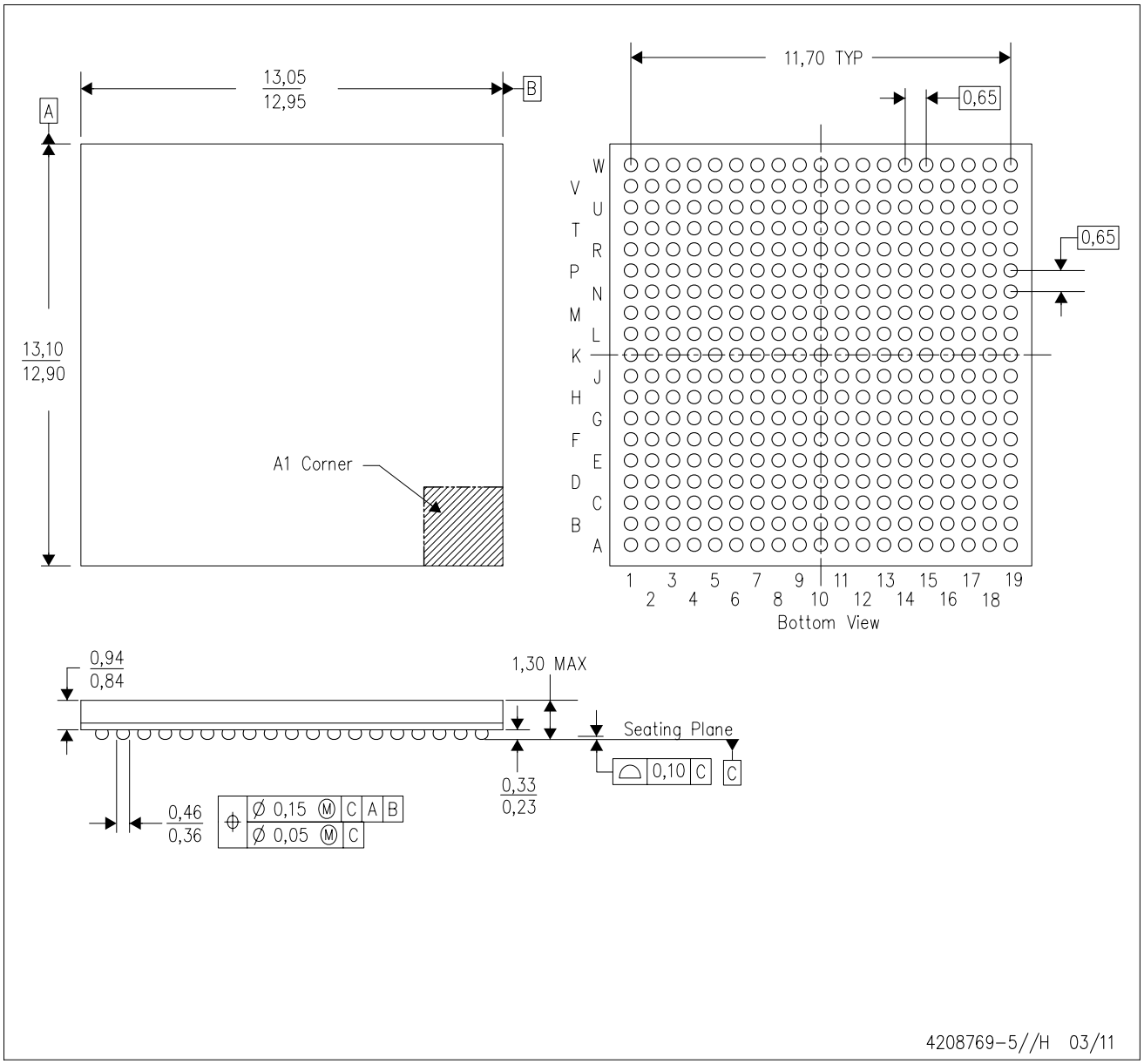
ZCE (S–PBGA–N361) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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