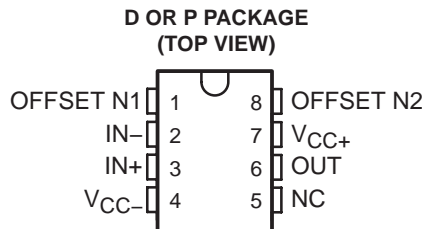


- **Low Noise**
- **No External Components Required**
- **Replace Chopper Amplifiers at a Lower Cost**
- **Wide Input-Voltage Range**
... 0 to ± 14 V Typ
- **Wide Supply-Voltage Range**
... ± 3 V to ± 18 V



NC – No internal connection

description/ordering information

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

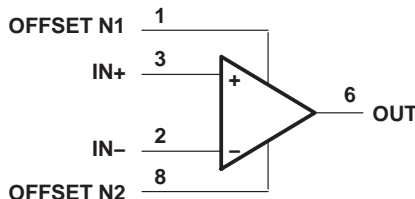
These devices are characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	OP07CP	OP07CP
		Tube of 50	OP07DP	OP07DP
	SOIC (D)	Tube of 75	OP07CD	OP07C
		Reel of 2500	OP07CDR	
		Tube of 75	OP07DD	OP07D
		Reel of 2500	OP07DDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

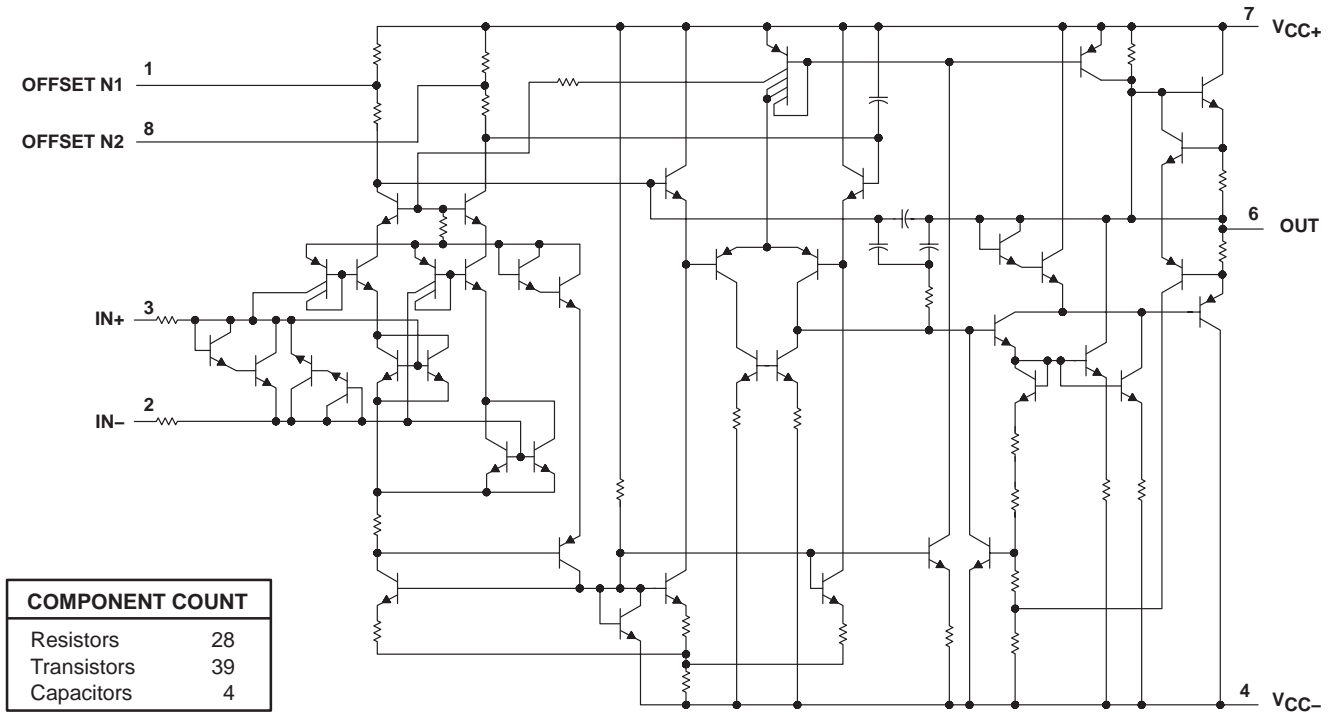
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OP07C, OP07D PRECISION OPERATIONAL AMPLIFIERS

SLOS099E – OCTOBER 1983 – REVISED MAY 2004

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1)	22 V
V_{CC-} (see Note 1)	-22 V
Differential input voltage (see Note 2)	± 30 V
Input voltage, V_I (either input, see Note 3)	± 22 V
Duration of output short circuit (see Note 4)	Unlimited
Package thermal impedance, θ_{JA} (see Notes 5 and 6): D package	97°C/W
P package	85°C/W
Operating virtual junction temperature, T_J	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .

2. Differential voltages are at $IN+$ with respect to $IN-$.

3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.

4. The output may be shorted to ground or to either power supply.

5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.

6. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		± 3	± 18	V
V_{IC}	Common-mode input voltage	$V_{CC\pm} = \pm 15$ V	-13	13	V
T_A	Operating free-air temperature		0	70	°C

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electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITION†	TA	OP07C			OP07D			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	25°C	60	150		60	150	μV	
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	0°C to 70°C	85	250		85	250	$\mu\text{V}/^\circ\text{C}$	
Long-term drift of input offset voltage	See Note 6	0°C to 70°C	0.5	1.8		0.7	2.5	$\mu\text{V}/^\circ\text{C}$	
Offset adjustment range	$R_S = 20\ \text{k}\Omega$, See Figure 1	25°C	±4			±4			mV
I_{IO} Input offset current		25°C	0.8	6		0.8	6	nA	
α_{IIO} Temperature coefficient of input offset current		0°C to 70°C	1.6	8		1.6	8	nA	
I_{IB} Input bias current		0°C to 70°C	12	50		12	50	pA/°C	
α_{IIB} Temperature coefficient of input bias current		25°C	±1.8	±7		±2	±12	nA	
V_{ICR} Common-mode input voltage range		0°C to 70°C	±2.2	±9		±3	±14	pA/°C	
V_{OM} Peak output voltage		0°C to 70°C	18	50		18	50	pA/°C	
		25°C	±13	±14		±13	±14	V	
		0°C to 70°C	±13	±13.5		±13	±13.5	V	
		25°C	±12	±13		±12	±13	V	
A_{VD} Large-signal differential voltage amplification		25°C	±11.5	±12.8		±11.5	±12.8	V	
		0°C to 70°C	±12			±12		V	
		25°C	±11.5	±12.8		±11.5	±12.8	V	
		0°C to 70°C	±11	±12.6		±11	±12.6	V	
B_1 Unity-gain bandwidth	$V_{CC\pm} = \pm 3\text{ V}$, $V_O = \pm 0.5\text{ V}$, $R_L \geq 500\ \text{k}\Omega$	25°C	100	400		400		V/mV	
	$V_O = \pm 10\text{ V}$, $R_L = 2\ \text{k}\Omega$	25°C	120	400		120	400	V/mV	
		0°C to 70°C	100	400		100	400	V/mV	
r_i Input resistance		25°C	0.4	0.6		0.4	0.6	MHz	
CMRR Common-mode rejection ratio		25°C	8	33		7	31	MΩ	
		0°C to 70°C	100	120		94	110	dB	
kSVS Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)		25°C	97	120		94	106	dB	
		0°C to 70°C	7	32		7	32	dB	
PD Power dissipation	$V_{CC\pm} = \pm 3\text{ V}$ to $\pm 18\text{ V}$, $R_S = 50\ \Omega$	25°C	10	51		10	51	$\mu\text{V}/\text{V}$	
	$V_O = 0$, No load	0°C to 70°C	80	150		80	150	mW	
	$V_{CC\pm} = \pm 3\text{ V}$, $V_O = 0$, No load	25°C	4	8		4	8	mW	

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

NOTE 7: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.



operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITION [†]	OP07C	OP07D	UNIT
		TYP	TYP	
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	10.5	10.5	$\text{nV}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$	10.2	10.3	
	$f = 1\text{ kHz}$	9.8	9.8	
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }10\text{ Hz}$	0.38	0.38	μV
I_n Equivalent input noise current	$f = 10\text{ Hz}$	0.35	0.35	$\text{pA}/\sqrt{\text{Hz}}$
	$f = 100\text{ Hz}$	0.15	0.15	
	$f = 1\text{ kHz}$	0.13	0.13	
$I_{N(PP)}$ Peak-to-peak equivalent input noise current	$f = 0.1\text{ Hz to }10\text{ Hz}$	15	15	pA
SR Slew rate	$R_L \geq 2\text{ k}\Omega$	0.3	0.3	$\text{V}/\mu\text{s}$

[†] All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

APPLICATION INFORMATION

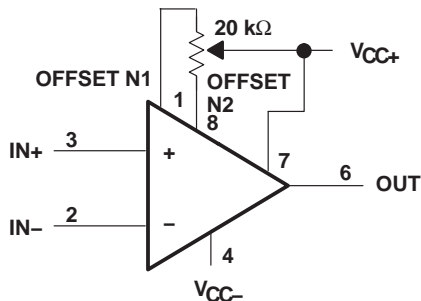


Figure 1. Input Offset-Voltage Null Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
OP-07DPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP-07DPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP-07DPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
OP07CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
OP07DD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07DDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07DDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07DDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07DDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07DDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OP07DP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
OP07DPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OP-07DPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
OP07CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OP07DDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

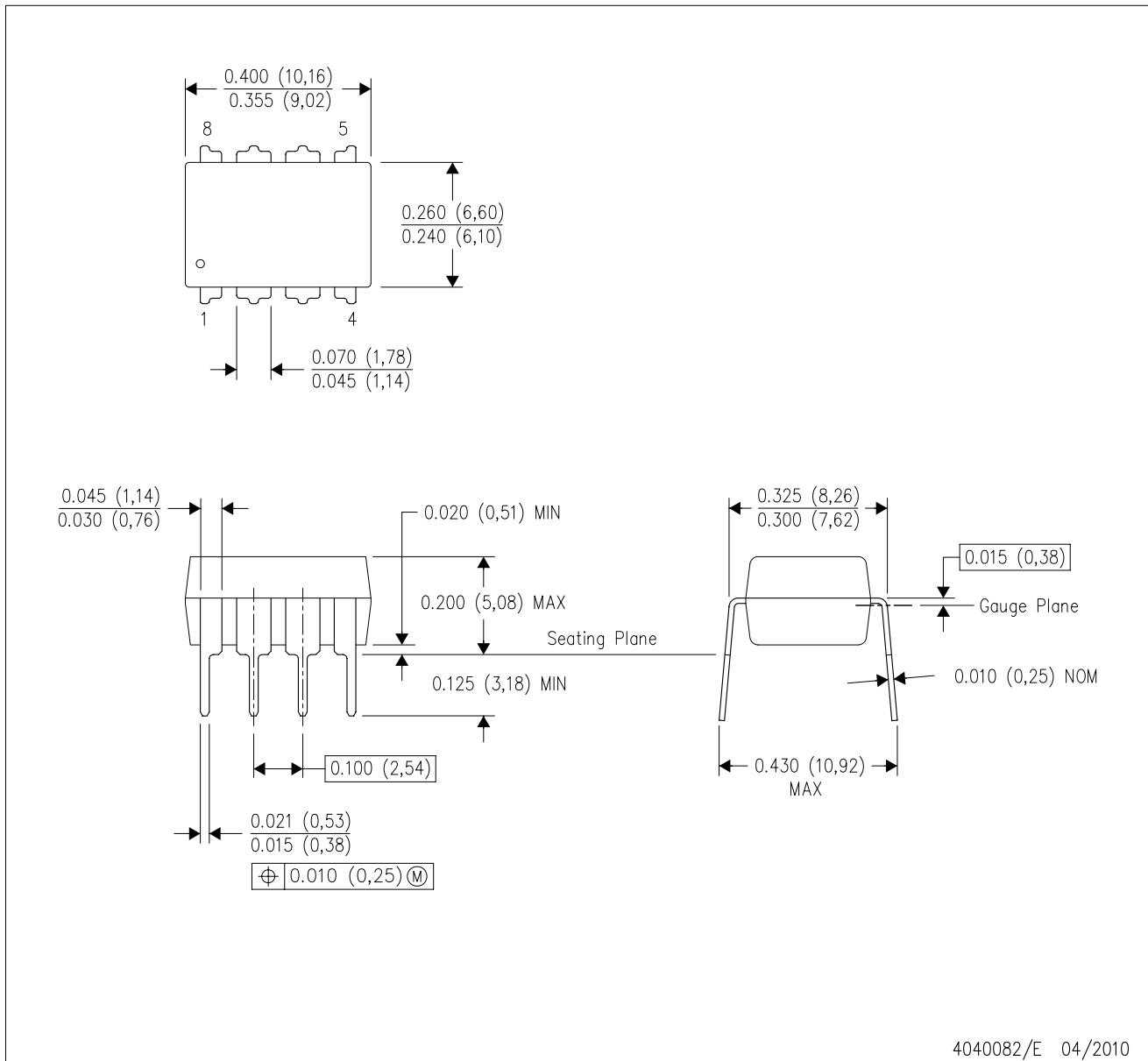
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OP-07DPSR	SO	PS	8	2000	346.0	346.0	33.0
OP07CDR	SOIC	D	8	2500	340.5	338.1	20.6
OP07DDR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

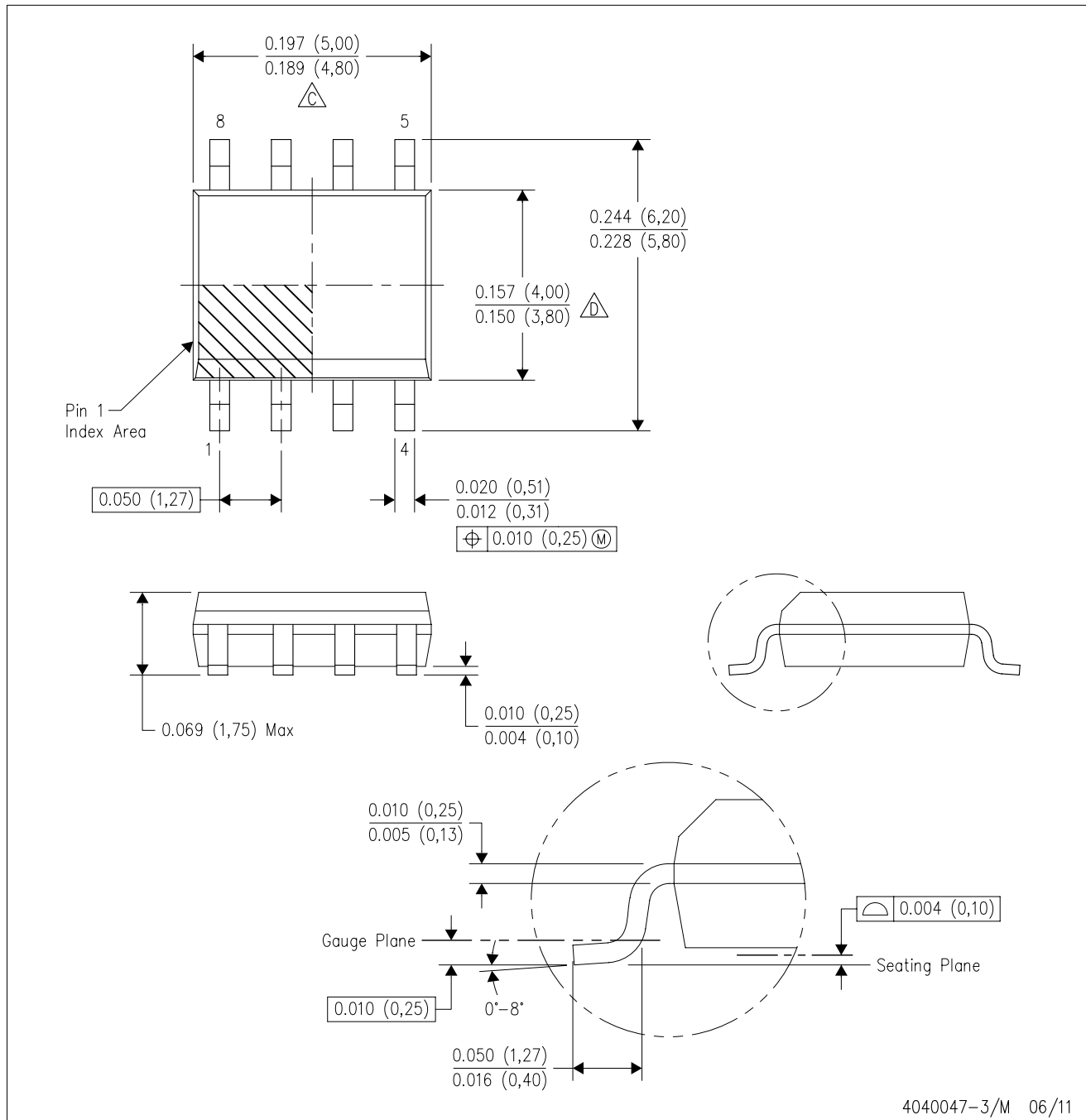
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

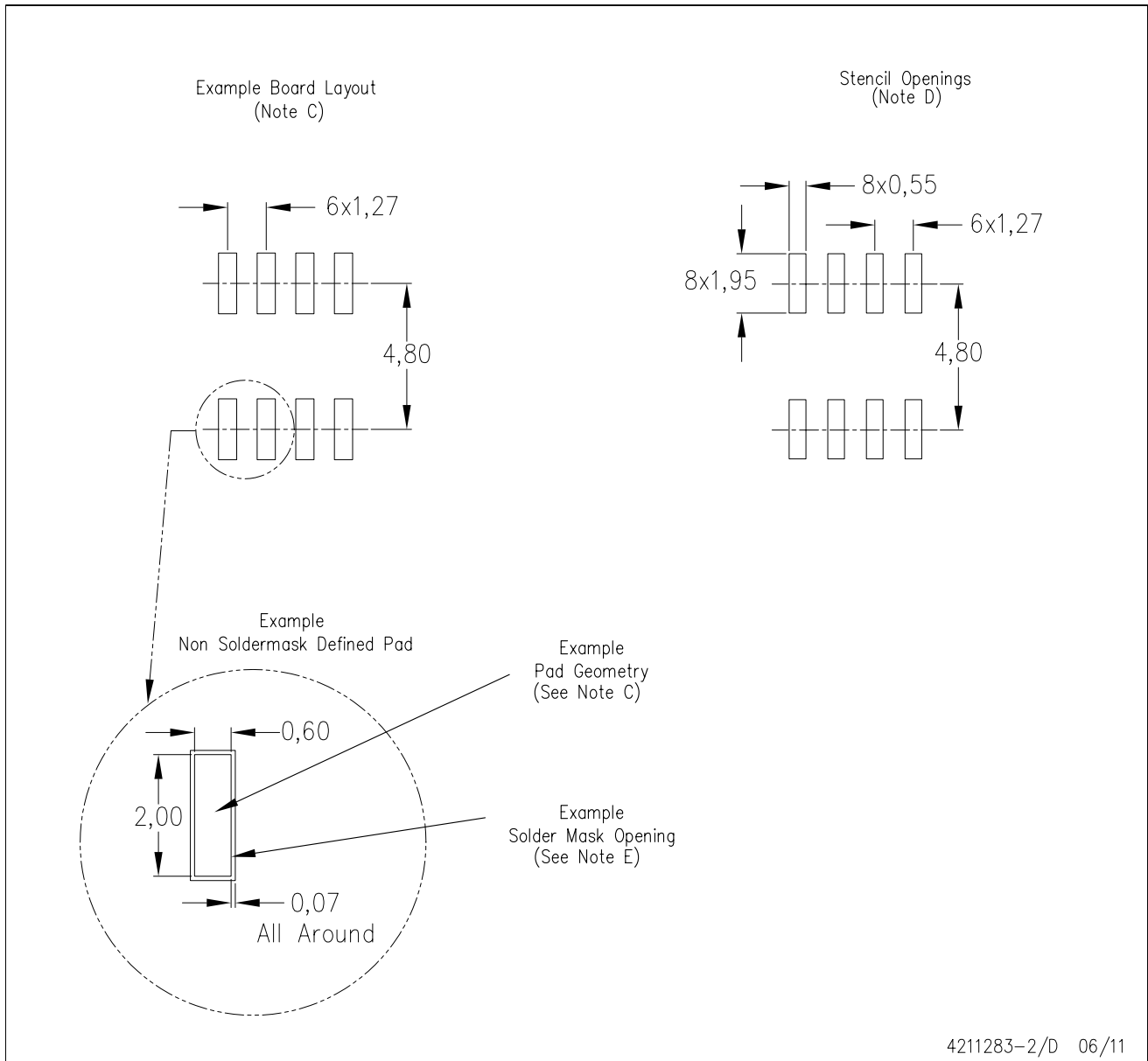
PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

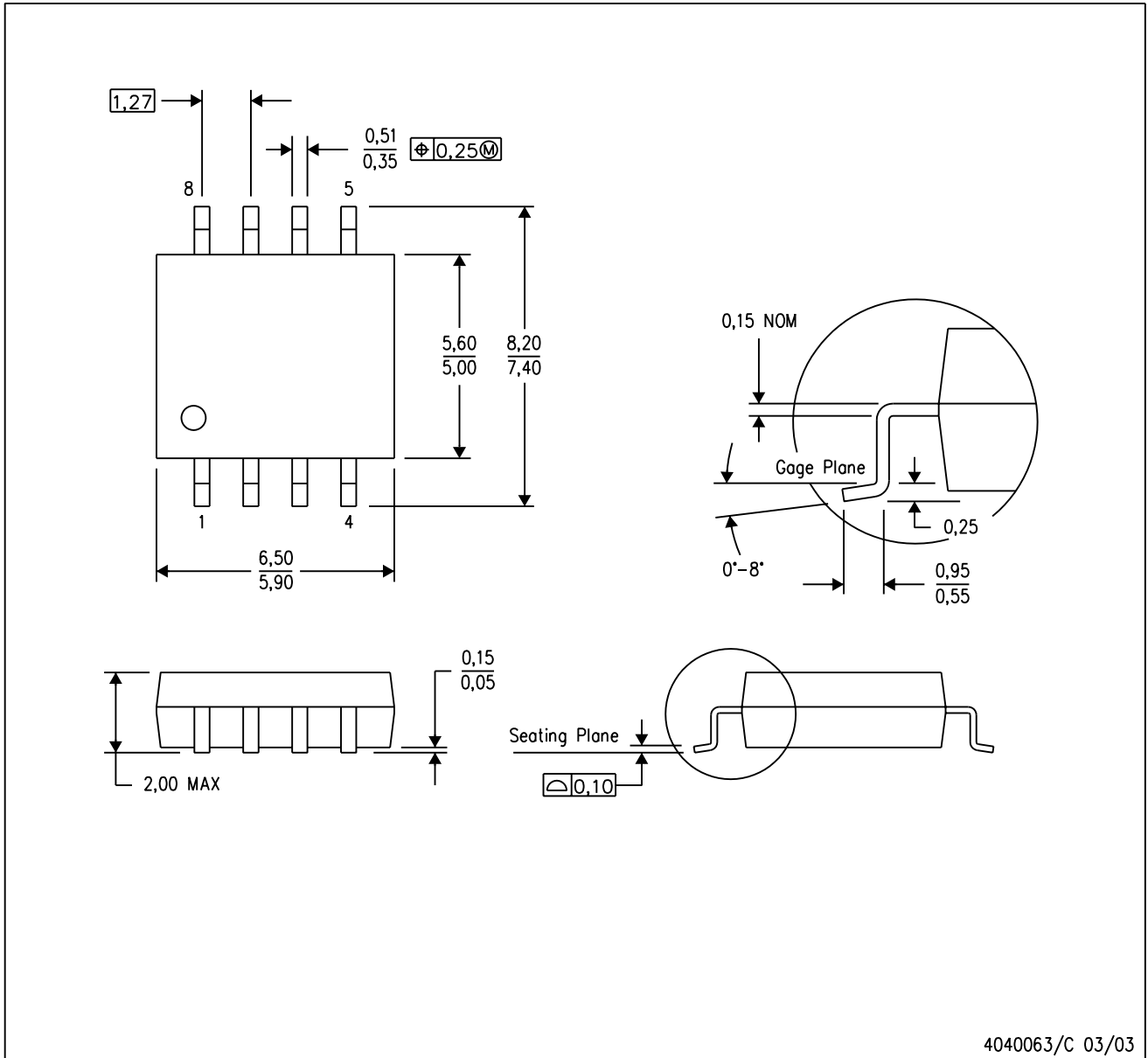


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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