



### Features

- 60A Output Current
- Multi-Phase Topology
- +5V Input
- 5-bit Programmable:  
1.3V to 3.5V  
1.075V to 1.850V
- High Efficiency
- Differential Remote Sense
- Short Circuit Protection
- Output Tracking Feature
- Over-Temp Shutdown
- Power Good & OV Flag
- Low-Profile Package
- Solderable Copper Case
- “Current Booster”  
Compatible

### Ordering Information

PT8001□ = 1.3 to 3.5 Volts  
PT8002□ = 1.075 to 1.850 Volts

### PT Series Suffix (PT1234X)

#### Case/Pin Configuration

Vertical Through-Hole	<b>N</b>
Horizontal Through-Hole	<b>A</b>
Horizontal Surface Mount	<b>C</b>

For dimensions and PC board layout, see  
Package Styles 1600, 1610 and 1615

### Description

The PT8000 series is a 60 A high-performance, Integrated Switching Regulator (ISR) housed in a single low-profile 44-pin SIP package. Operating from an input voltage of +5V, the PT8000 series offers a state-of-the-art “Plug-in Power” solution for highly-integrated digital systems that demand high power supply currents at low voltages.

The output voltage from these modules is programmable over a preset range via a 5-bit input. The PT8001 may be set from 1.3V to 3.5V, which is compatible with Intel’s Pentium Pro®  $\mu$ -processors. The output voltage of the PT8002 is programmable from 1.075V to 1.85V.

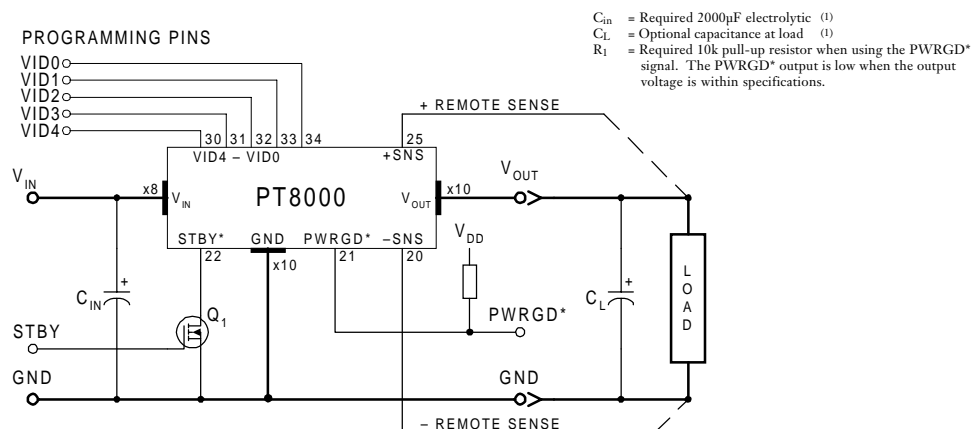
The PT8000 series incorporates many features to facilitate system

integration. Output short-circuit protection and over-temperature shutdown enables these modules to survive any load fault. Two self-diagnostic signals, “Power Good” (PWRGD\*) and “Over-Voltage Flag” (OVF\*) are provided. And a unique tracking feature allows the output to be synchronized to a master ramp voltage during power-up.

Other features include a standby input, and a differential remote sense to compensate for voltage drop between the ISR and load.

A low ESR capacitance of 2000 $\mu$ F is required at the input for proper operation.

### Standard Application



### Pin-Out Information

Pin	Function	PinFunction
1	V <sub>out</sub>	16 GND
2	V <sub>in</sub>	17 GND
3	V <sub>in</sub>	18 GND
4	GND	19 V <sub>out</sub>
5	GND	20 Remote Sense Gnd
6	V <sub>in</sub>	21 PWRGD*
7	V <sub>in</sub>	22 STBY*
8	V <sub>out</sub>	23 OVF*
9	V <sub>out</sub>	24 Track
10	V <sub>out</sub>	25 Remote Sense V <sub>out</sub>
11	Synch 1	26 V <sub>out</sub>
12	Synch 2	27 GND
13	Synch 3	28 GND
14	Synch 4	29 GND
15	Do Not Connect	30 VID4

For STBY\* pin; Open = output enabled  
Gnd = output disabled.

PinFunction
31 VID3
32 VID2
33 VID1
34 VID0
35 V <sub>out</sub>
36 V <sub>out</sub>
37 V <sub>out</sub>
38 V <sub>in</sub>
39 V <sub>in</sub>
40 GND
41 GND
42 V <sub>in</sub>
43 V <sub>in</sub>
44 V <sub>out</sub>

### Programming Information

					PT8001		PT8002	
					VID4=1	VID4=0	VID4=1	VID4=0
VID3	VID2	VID1	VID0	V <sub>o</sub>	V <sub>o</sub>	V <sub>o</sub>	V <sub>o</sub>	
1	1	1	1	2.0V	1.30V	1.075V	1.475V	
1	1	1	0	2.1V	1.35V	1.100V	1.500V	
1	1	0	1	2.2V	1.40V	1.125V	1.525V	
1	1	0	0	2.3V	1.45V	1.150V	1.550V	
1	0	1	1	2.4V	1.50V	1.175V	1.575V	
1	0	1	0	2.5V	1.55V	1.200V	1.600V	
1	0	0	1	2.6V	1.60V	1.225V	1.625V	
1	0	0	0	2.7V	1.65V	1.250V	1.650V	
0	1	1	1	2.8V	1.70V	1.275V	1.675V	
0	1	1	0	2.9V	1.75V	1.300V	1.700V	
0	1	0	1	3.0V	1.80V	1.325V	1.725V	
0	1	0	0	3.1V	1.85V	1.350V	1.750V	
0	0	1	1	3.2V	1.90V	1.375V	1.775V	
0	0	1	0	3.3V	1.95V	1.400V	1.800V	
0	0	0	1	3.4V	2.00V	1.425V	1.825V	
0	0	0	0	3.5V	2.05V	1.450V	1.850V	

Logic 0 = Pin 20 potential (remote sense gnd)  
Logic 1 = Open circuit (no pull-up resistors)  
VID3 and VID4 may not be changed while the unit is operating.

### Specifications

Characteristics (T <sub>a</sub> = 25°C unless noted)	Symbols	Conditions	PT8000 SERIES			
			Min	Typ	Max	Units
Output Current	I <sub>o</sub>	T <sub>a</sub> = +50°C, 400 LFM, pkg N T <sub>a</sub> = +25°C, natural convection	0.1 (1) 0.1 (1)	—	60 (2) 30 (2)	A
Input Voltage Range	V <sub>in</sub>	0.1A ≤ I <sub>o</sub> ≤ 60A	4.5	—	5.5	V
Output Voltage Tolerance	ΔV <sub>o</sub>	Over V <sub>in</sub> range, I <sub>o</sub> = I <sub>o,max</sub> 0°C ≤ T <sub>a</sub> ≤ +60°C	V <sub>o</sub> -0.03	—	V <sub>o</sub> +0.03	V
Line Regulation	Reg <sub>line</sub>	Over V <sub>in</sub> range, I <sub>o</sub> = I <sub>max</sub>	—	±1.0	±10	mV
Load Regulation	Reg <sub>load</sub>	V <sub>in</sub> = 5V, 0.1 ≤ I <sub>o</sub> ≤ I <sub>o,max</sub>	—	±1.0	±10	mV
V <sub>o</sub> Ripple/Noise pk-pk	V <sub>n</sub>	V <sub>in</sub> = 5V, I <sub>o</sub> = 60A	—	50	—	mV
Transient Response (no external capacitance)	t <sub>tr</sub> V <sub>os</sub>	I <sub>o</sub> step from 30A to 60A in 6μs V <sub>o</sub> over/undershoot	— —	50 100	— —	μs mV
Efficiency	η	V <sub>in</sub> = +5V, I <sub>o</sub> = 30A, V <sub>o</sub> = 3.3V V <sub>o</sub> = 1.8V	— —	92 86	— —	%
Switching Frequency	f <sub>o</sub>	Over V <sub>in</sub> and I <sub>o</sub> ranges	1.3	—	1.5	MHz
STBY* (pin 22)	Off On		0 Note (2)	—	0.8	V
PWRGD* (pin 21)	On Off	85% < V <sub>out</sub> < 115% of VID set point V <sub>out</sub> < 85%, or V <sub>out</sub> > 125% of VID set point	— —	500 500	— —	Ω kΩ
OVF* (pin 23)	On Off	V <sub>out</sub> > 125% of VID set point V <sub>out</sub> < 115% of VID set point	— —	500 500	— —	Ω kΩ
Over-temperature Shutdown Point	O <sub>TP</sub>	Case temperature -Auto reset	—	105	—	°C
Absolute Maximum Operating Temperature Range	T <sub>a</sub>	—	-40	—	+85 (3)	°C
Storage Temperature	T <sub>s</sub>	—	-40	—	+125	°C
Weight	—	Vertical/Horizontal	—	110	—	grams

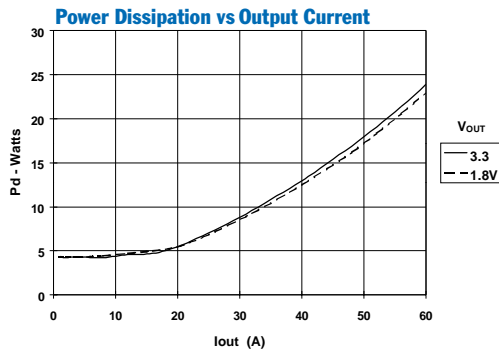
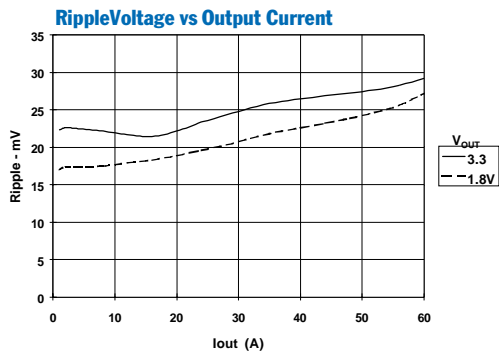
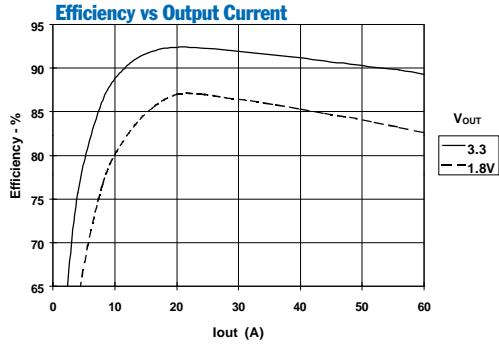
**Notes:** (1) The ISR will operate down to no load with reduced specifications.

(2) Specified as “Open-Circuit.” Either an “open-collector” bipolar transistor, or “open-drain” MOSFET is recommended for controlling this input.

(3) See Safe Operating Area curves or contact the factory to determine the appropriate derating.

**Input Filter:** To facilitate the high output fast transient performance, a high quality 2,000μF input capacitor(s) is required for the PT8000 series. Use either tantalum or Oscon® type capacitors with a maximum ESR (equivalent series resistance) of 20mΩ.

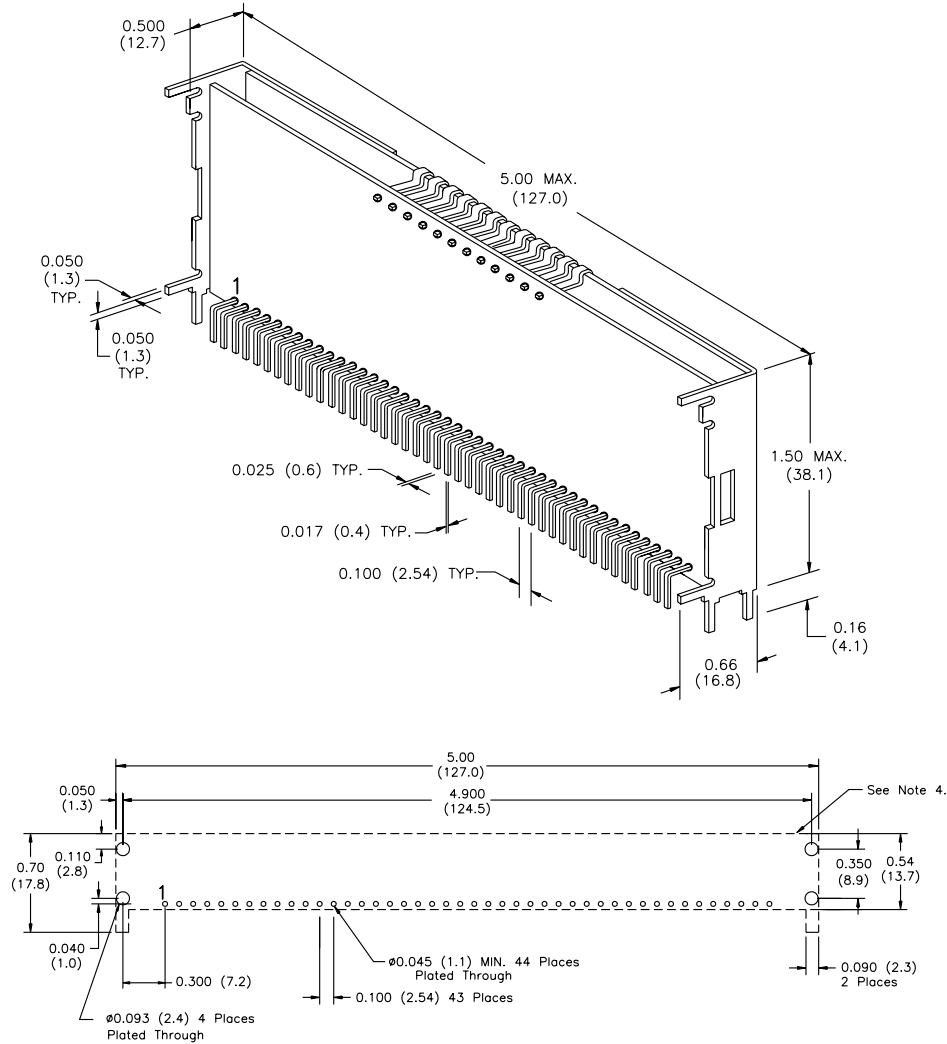
Performance Characteristics,  $V_{in} = 5.0V$  (See Note A)



**Note A:** Characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the regulator.  
**Note B:** Safe Operating Area curves represent conditions at which internal components are at or below manufacturer's rated operating temperatures.

## PACKAGE INFORMATION AND DIMENSIONS

Vertical Through-Hole Mount (Suffix N)



PC Layout

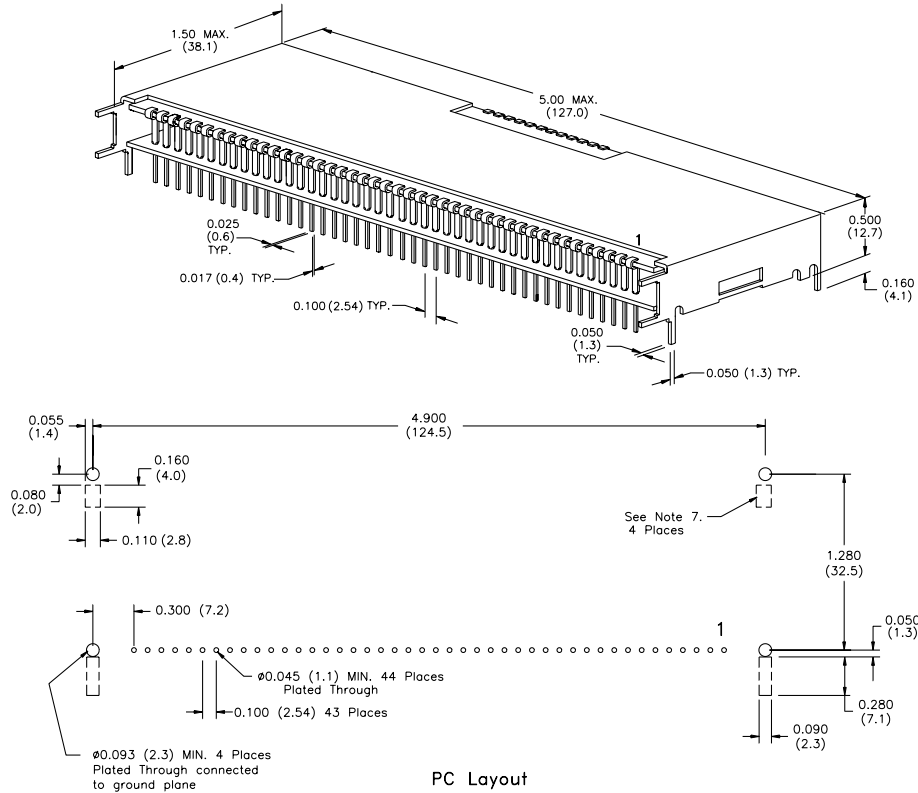
Notes: (Rev. A)

- 1: All dimensions are in inches (mm).
- 2: 2 place decimals are  $\pm 0.030$  ( $\pm 0.8$ mm).
- 3: 3 place decimals are  $\pm 0.010$  ( $\pm 0.3$ mm).
- 4: Recommended mechanical keep out area (dotted line).

**Power Trends proprietary package design.  
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### PACKAGE INFORMATION AND DIMENSIONS

#### Horizontal Through-Hole Mount (Suffix A)



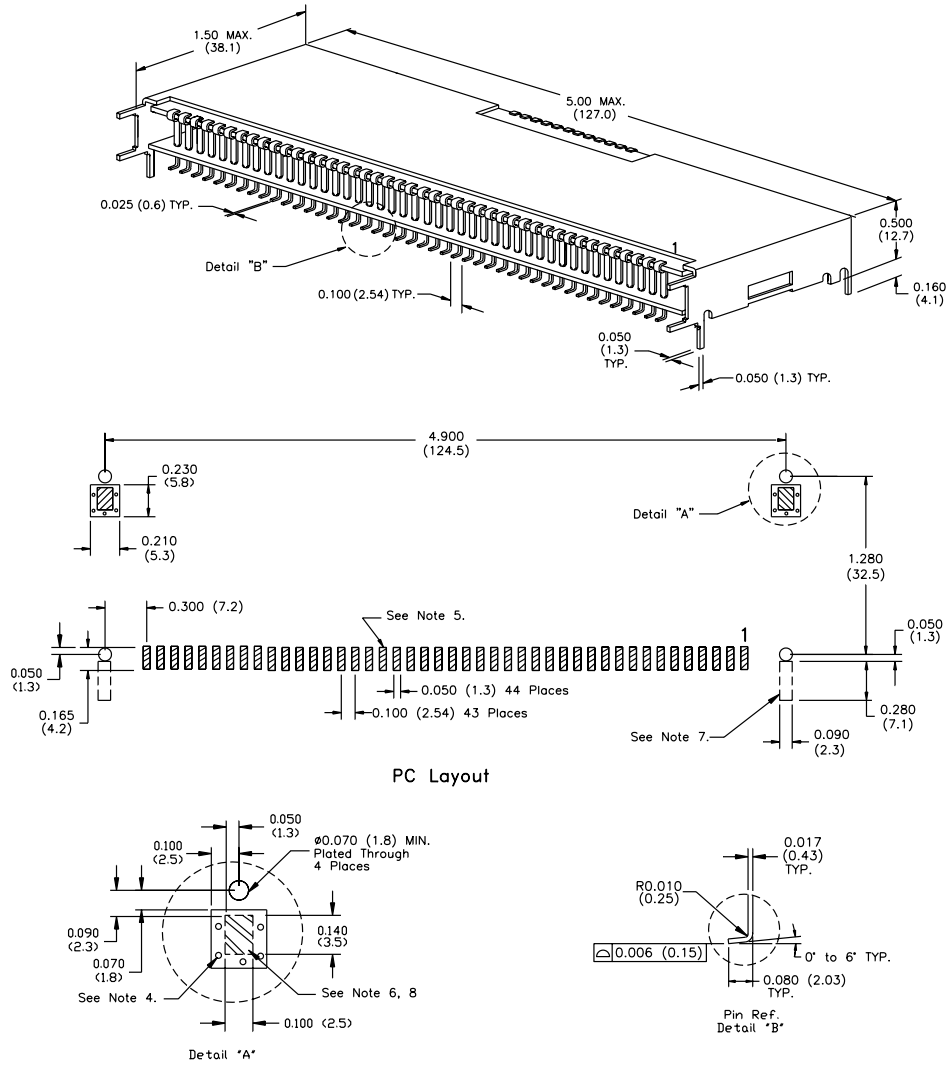
#### Notes: (Rev. A)

- 1: All dimensions are in inches (mm).
- 2: 2 place decimals are  $\pm 0.030$  ( $\pm 0.8$ mm).
- 3: 3 place decimals are  $\pm 0.010$  ( $\pm 0.3$ mm).
- 4: Recommended mechanical keep out area (dotted lines).

**Power Trends proprietary package design.  
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### PACKAGE INFORMATION AND DIMENSIONS

#### Horizontal Surface Mount (Suffix C)



#### Notes: (Rev. B)

- 1: All dimensions are in inches (mm).
- 2: 2 place decimals are  $\pm 0.030$  ( $\pm 0.8\text{mm}$ ).
- 3: 3 place decimals are  $\pm 0.010$  ( $\pm 0.3\text{mm}$ ).
- 4: Vias are recommended to improve copper adhesion.
- 5: Power pin connections should utilize two or more vias per input, ground and output pin.
- 6: Solder mask openings to copper island for solder joints to mechanical pins.
- 7: Recommended mechanical keep out area (dotted lines).
- 8: Electrically connected case to ground plane.

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PT8001A	NRND	SIP MOD ULE	ERA	44	4	TBD	Call TI	Level-1-215C-UNLIM
PT8001C	NRND	SIP MOD ULE	ERC	44	4	TBD	Call TI	Level-1-215C-UNLIM
PT8001N	NRND	SIP MOD ULE	ERD	44	4	TBD	Call TI	Level-1-215C-UNLIM
PT8002A	NRND	SIP MOD ULE	ERA	44		TBD	Call TI	Call TI
PT8002C	NRND	SIP MOD ULE	ERC	44		TBD	Call TI	Call TI
PT8002N	NRND	SIP MOD ULE	ERD	44		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

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