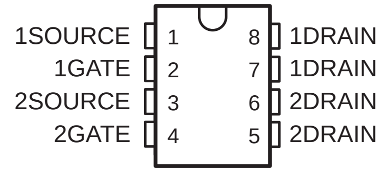
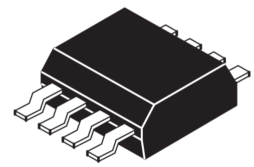
Jameco Part Number 827729

- **Low $r_{DS(on)}$ . . . 0.18 Ω at V_{GS} = –10 V**
- **3-V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = –1.5 V Max**
- **ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015**

D PACKAGE
(TOP VIEW)





description

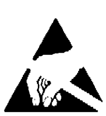
The TPS1120 incorporates two independent p-channel enhancement-mode MOSFETs that have been optimized, by means of the Texas Instruments LinBiCMOS™ process, for 3-V or 5-V power distribution in battery-powered systems. With a maximum $V_{GS(th)}$ of –1.5 V and an I_{DSS} of only 0.5 µA, the TPS1120 is the ideal high-side switch for low-voltage portable battery-management systems, where maximizing battery life is a primary concern. Because portable equipment is potentially subject to electrostatic discharge (ESD), the MOSFETs have built-in circuitry for 2-kV ESD protection. End equipment for the TPS1120 includes notebook computers, personal digital assistants (PDAs), cellular telephones, bar-code scanners, and PCMCIA cards. For existing designs, the TPS1120D has a pinout common with other p-channel MOSFETs in small-outline integrated circuit SOIC packages.

The TPS1120 is characterized for an operating junction temperature range, T_J, from –40°C to 150°C.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES† SMALL OUTLINE (D)	CHIP FORM (Y)
–40°C to 150°C	TPS1120D	TPS1120Y

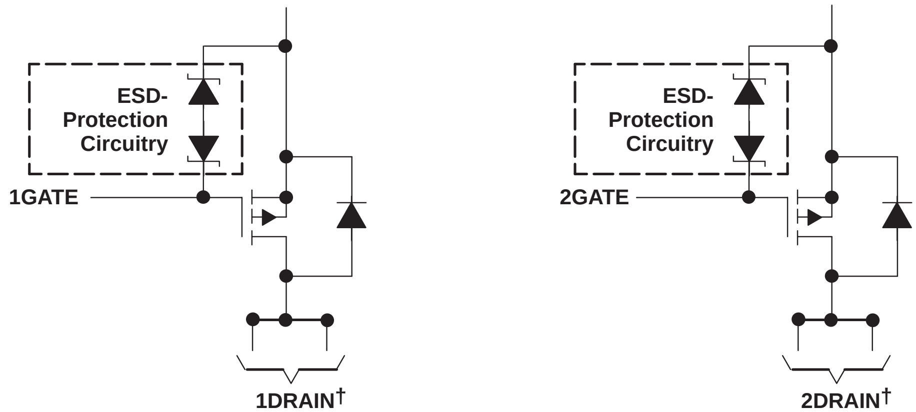
† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1120DR). The chip form is tested at 25°C.



Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMS is a trademark of Texas Instruments Incorporated.

schematic

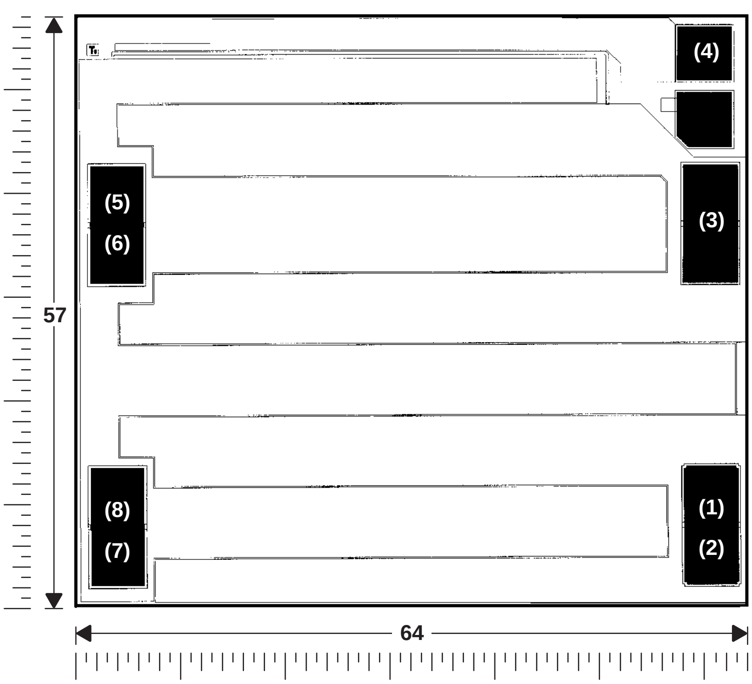


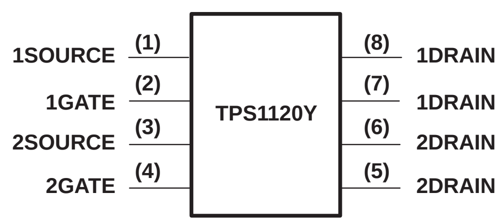
† For all applications, both drain pins for each device should be connected.

TPS1120Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1120C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

				UNIT
Drain-to-source voltage, V_{DS}			–15	V
Gate-to-source voltage, V_{GS}			2 or –15	V
Continuous drain current, each device (T_J = 150°C), I_D	V_{GS} = –2.7 V	T_A = 25°C	±0.39	A
		T_A = 125°C	±0.21	
	V_{GS} = –3 V	T_A = 25°C	±0.5	
		T_A = 125°C	±0.25	
	V_{GS} = –4.5 V	T_A = 25°C	±0.74	
		T_A = 125°C	±0.34	
	V_{GS} = –10 V	T_A = 25°C	±1.17	
		T_A = 125°C	±0.53	
Pulse drain current, I_D		T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S		T_A = 25°C	–1	A
Continuous total power dissipation			See Dissipation Rating Table	
Storage temperature range, T_{stg}			–55 to 150	°C
Operating junction temperature range, T_J			–40 to 150	°C
Operating free-air temperature range, T_A			–40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	840 mW	6.71 mW/°C	538 mW	437 mW	169 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 149°C/W for the package. These devices are mounted on an FR4 board with no special thermal considerations.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS		TPS1120			UNIT
				MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	I_D = –250 µA	–1	–1.25	–1.50	V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	I_S = –1 A,	V_{GS} = 0 V		–0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	V_{DS} = 0 V,	V_{GS} = –12 V			±100	nA
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = –12 V, V_{GS} = 0 V	T_J = 25°C			–0.5	µA
			T_J = 125°C			–10	
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = –10 V	I_D = –1.5 A		180		mΩ
		V_{GS} = –4.5 V	I_D = –0.5 A		291	400	
		V_{GS} = –3 V	I_D = –0.2 A		476	700	
		V_{GS} = –2.7 V			606	850	
g_{fs}	Forward transconductance†	V_{DS} = –10 V,	I_D = –2 A		2.5		S

† Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%

static

PARAMETER		TEST CONDITIONS		TPS1120Y			UNIT
				MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	I_D = –250 µA		–1.25		V
V_{SD}	Source-to-drain voltage (diode forward voltage)†	I_S = –1 A,	V_{GS} = 0 V		–0.9		V
$r_{DS(on)}$	Static drain-to-source on-state resistance†	V_{GS} = –10 V	I_D = –1.5 A		180		mΩ
		V_{GS} = –4.5 V	I_D = –0.5 A		291		
		V_{GS} = –3 V	I_D = –0.2 A		476		
		V_{GS} = –2.7 V			606		
g_{fs}	Forward transconductance†	V_{DS} = –10 V,	I_D = –2 A		2.5		S

† Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			TPS1120, TPS1120Y			UNIT
					MIN	TYP	MAX	
Q_g	Total gate charge	V_{DS} = –10 V,	V_{GS} = –10 V,	I_D = –1 A		5.45		nC
Q_{gs}	Gate-to-source charge					0.87		
Q_{gd}	Gate-to-drain charge					1.4		
$t_{d(on)}$	Turn-on delay time	V_{DD} = –10 V, R_G = 6 Ω,	R_L = 10 Ω, See Figures 1 and 2	I_D = –1 A,		4.5		ns
$t_{d(off)}$	Turn-off delay time					13		ns
t_r	Rise time					10		ns
t_f	Fall time					2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	I_F = 5.3 A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

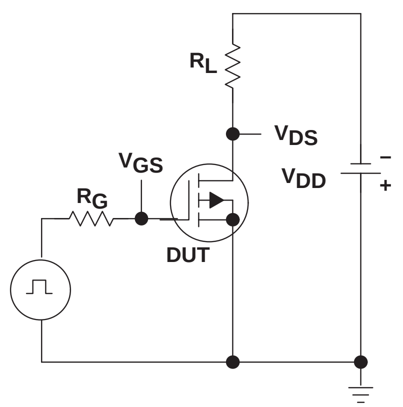


Figure 1. Switching-Time Test Circuit

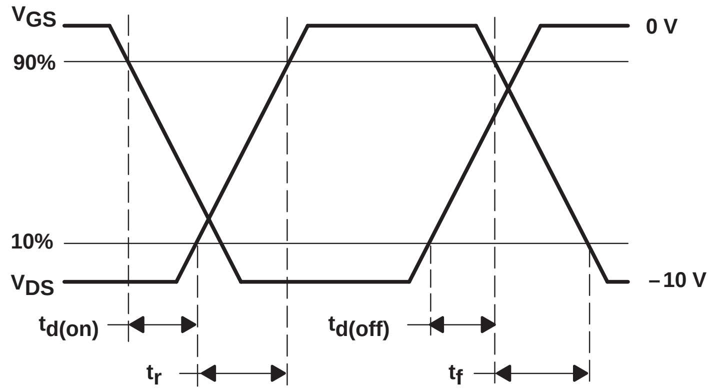


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS†

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

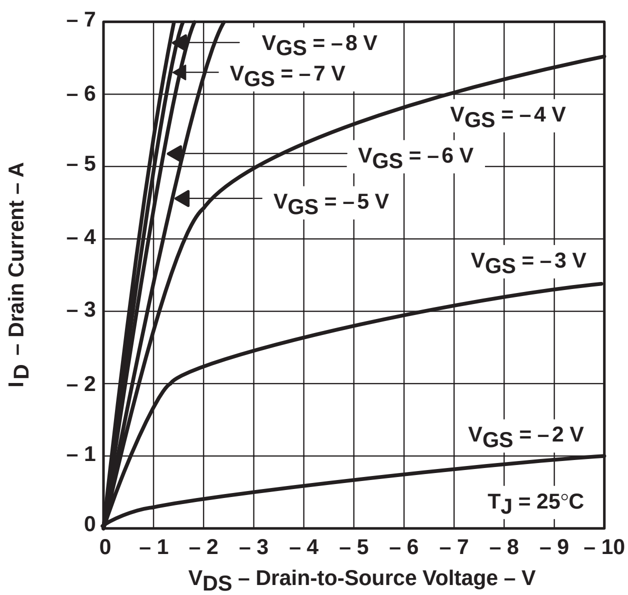


Figure 3

DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

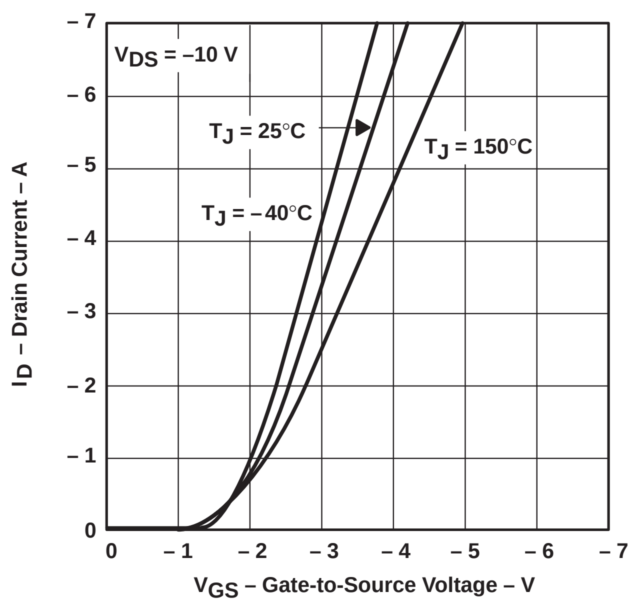


Figure 4

† All characteristics data applies for each independent MOSFET incorporated on the TPS1120.

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

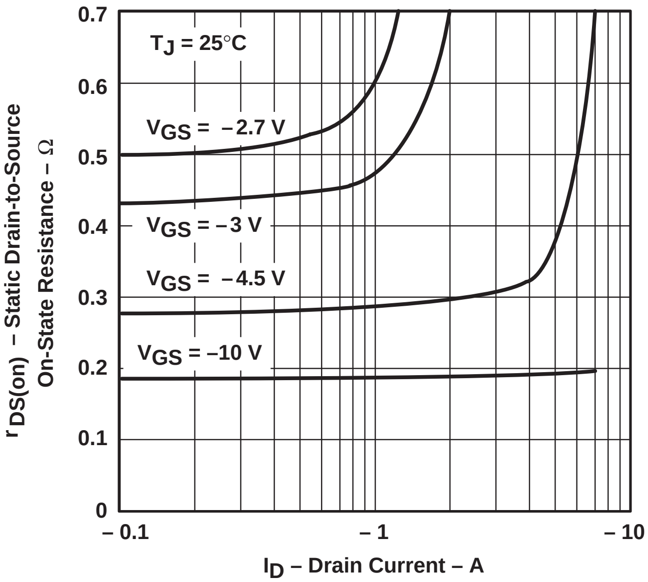
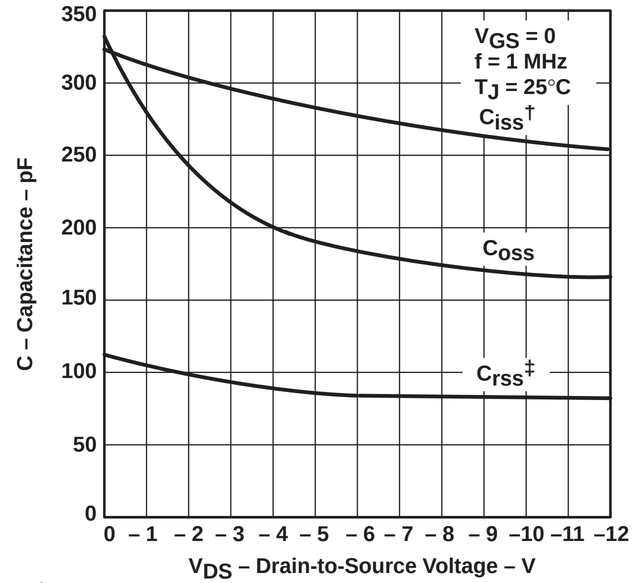


Figure 5

CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}, \; C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}, \; C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED) vs JUNCTION TEMPERATURE

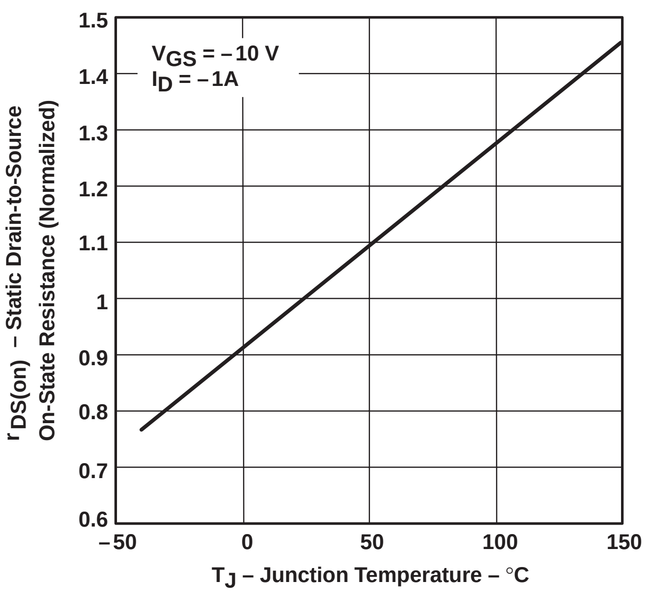


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

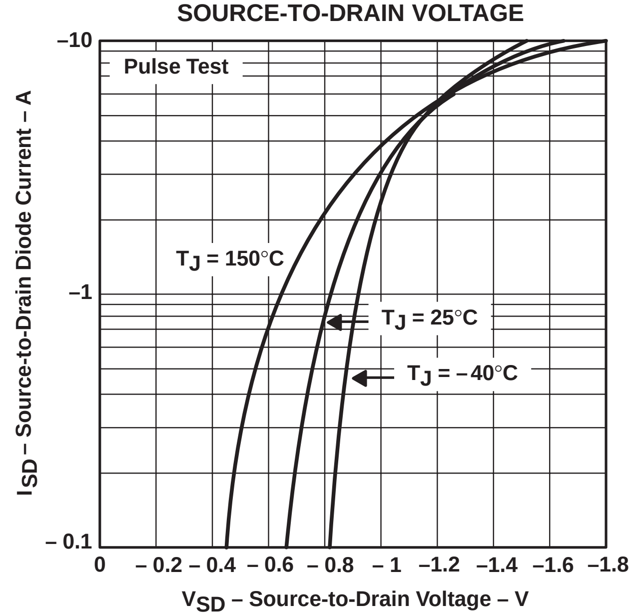


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
GATE-TO-SOURCE VOLTAGE

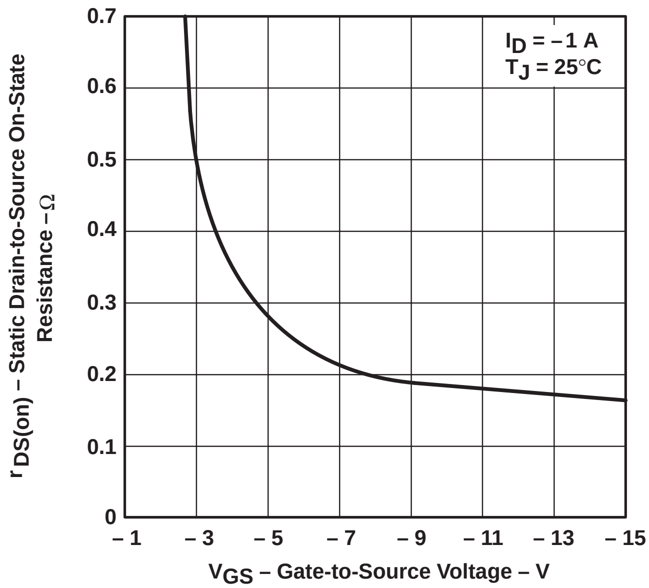


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

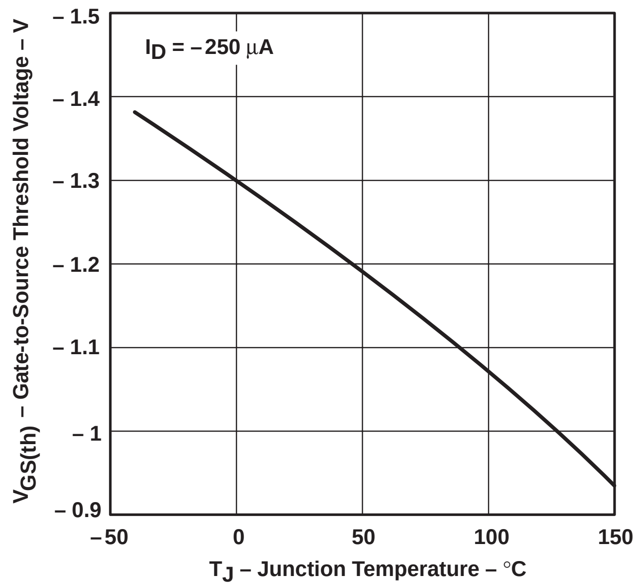


Figure 10

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

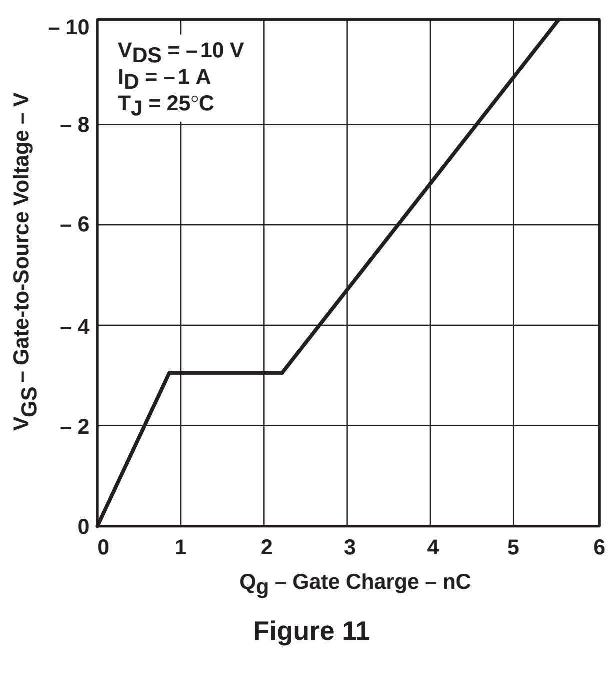
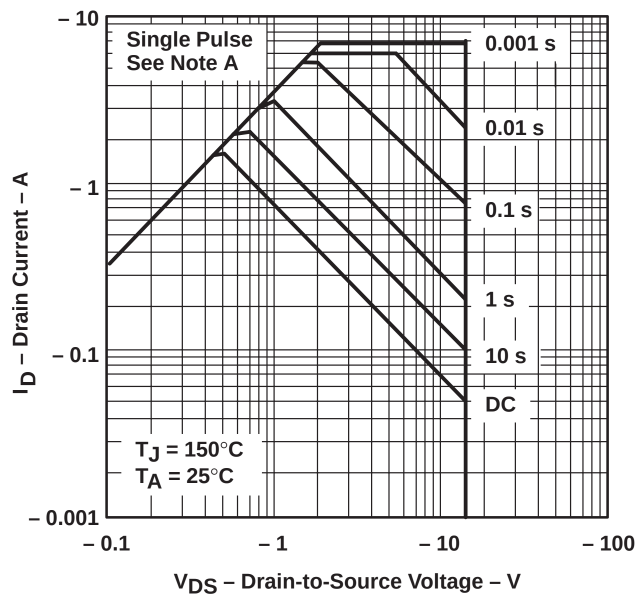


Figure 11

THERMAL INFORMATION

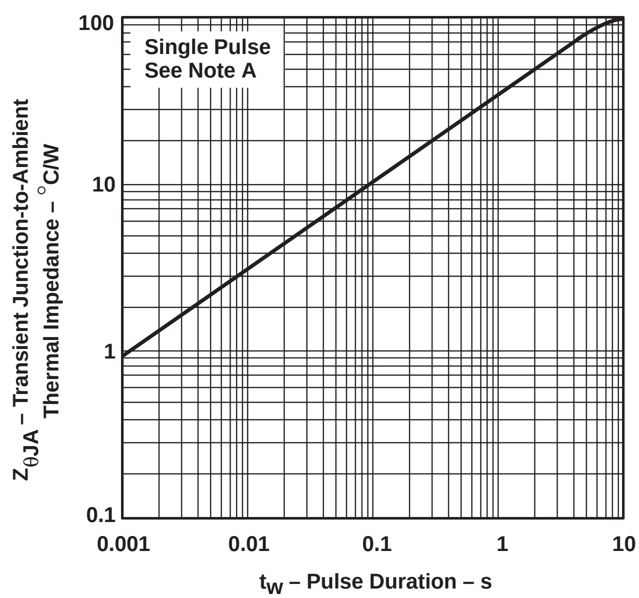
**DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE**



NOTE A: FR4-board-mounted only

Figure 12

**TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION**



NOTE A: FR4-board-mounted only

Figure 13

THERMAL INFORMATION

The profile of the heat sinks used for thermal measurements is shown in Figure 14. Board type is FR4 with 1-oz copper and 1-oz tin/lead (63/37) plate. Use of vias or through-holes to enhance thermal conduction was avoided.

Figure 15 shows a family of $R_{\theta JA}$ curves. The $R_{\theta JA}$ was obtained for various areas of heat sinks while subject to air flow. Power remained fixed at 0.25 W per device or 0.50 W per package. This testing was done at 25°C.

As Figure 14 illustrates, there are two separated heat sinks for each package. Each heat sink is coupled to the lead that is internally tied to a single MOSFET source and is half the total area, as shown in Figure 15. For example, if the total area shown in Figure 15 is 4 cm^2, each heat sink is 2 cm^2.

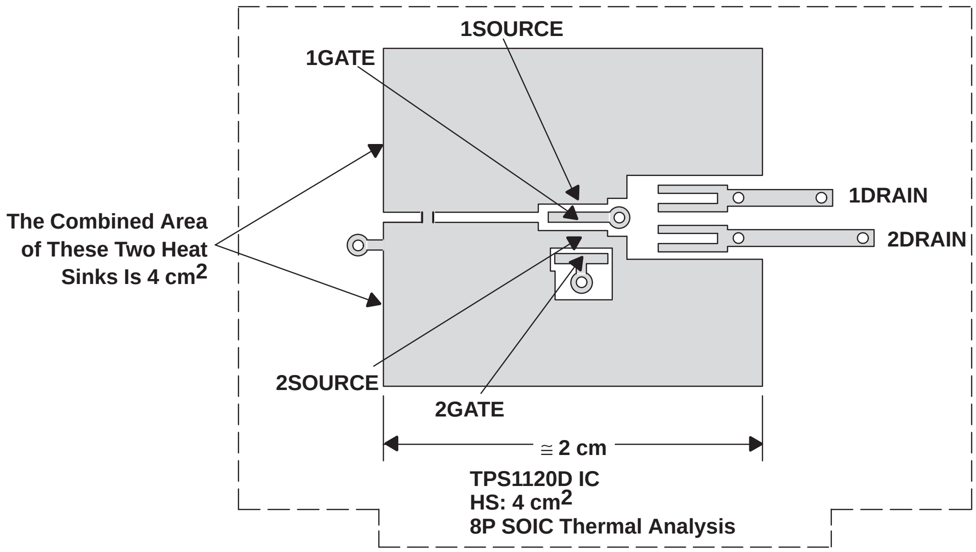


Figure 14. Profile of Heat Sinks

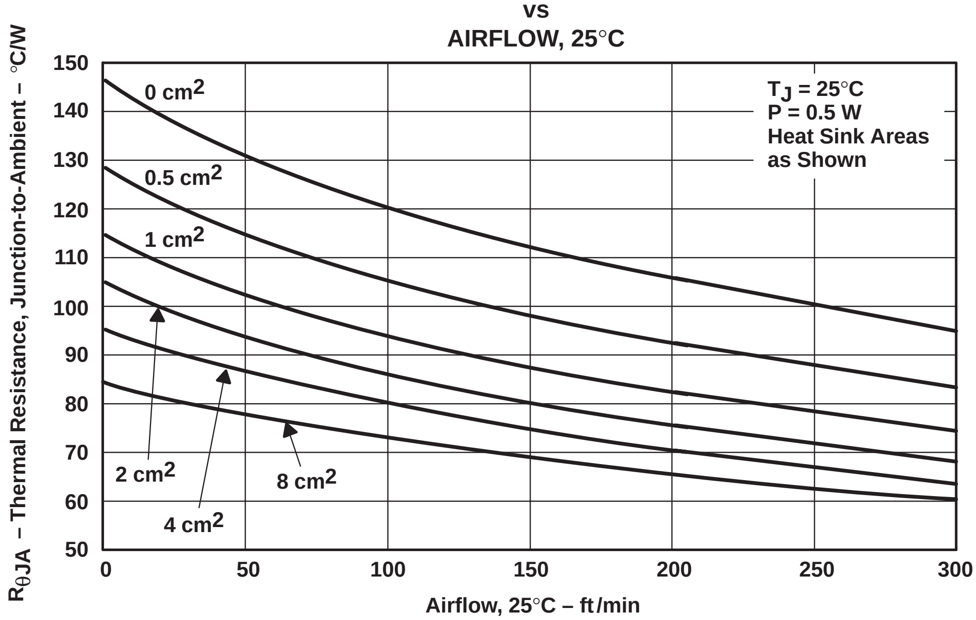


Figure 15

THERMAL INFORMATION

Figure 16 illustrates the thermally enhanced (SO) lead frame. Attaching the two MOSFET dies directly to the source terminals allows maximum heat transfer into a power plane.

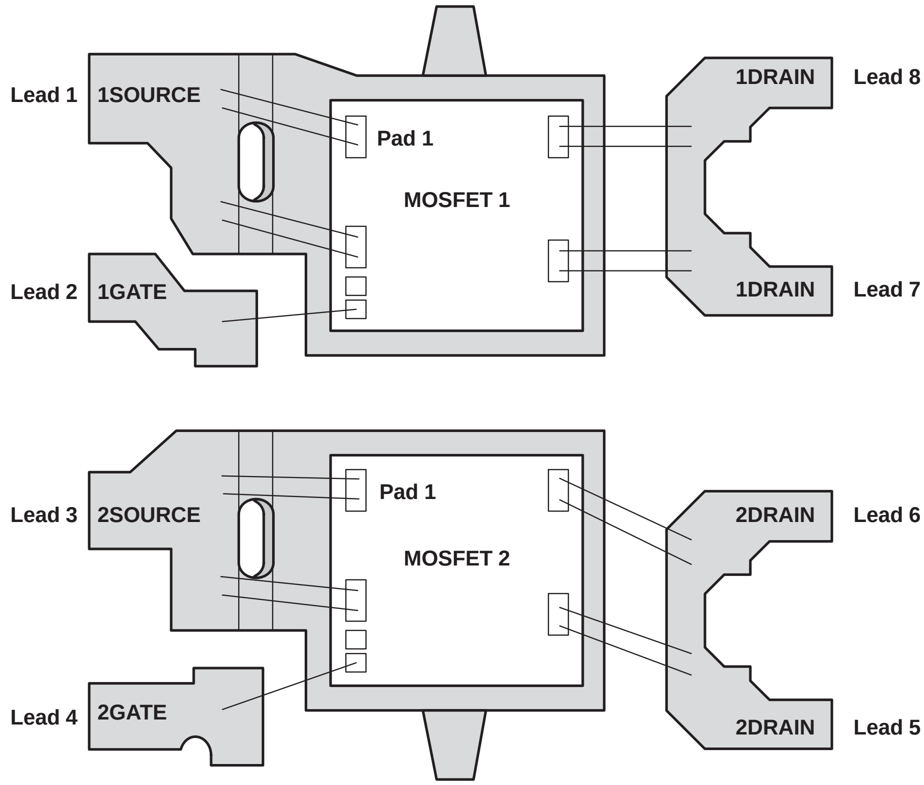


Figure 16. TPS1120 Dual MOSFET SO-8 Lead Frame

APPLICATION INFORMATION

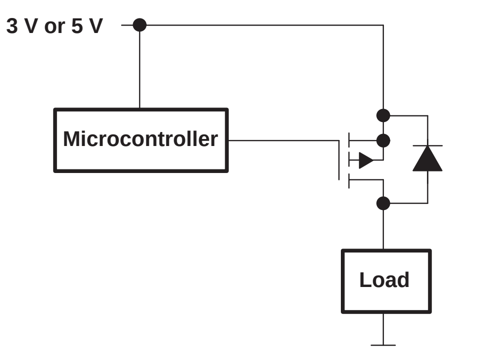


Figure 17. Notebook Load Management

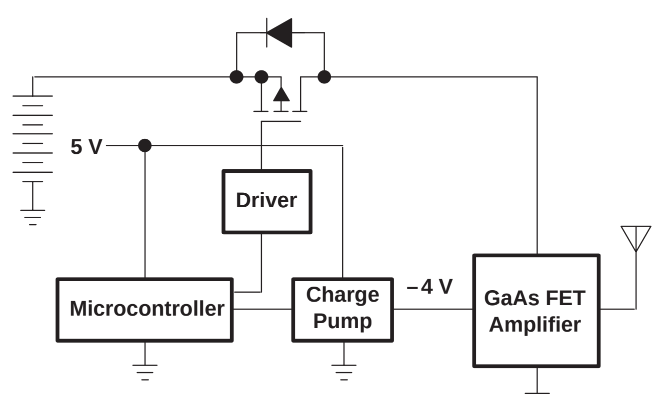


Figure 18. Cellular Phone Output Drive

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS1120D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1120DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1120DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1120DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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