



Quad Complementary CMOS Analog Switch

FEATURES

- $\pm 22\text{-V}$ Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$: $45\ \Omega$
- Low Leakage— $I_{D(on)}$: $20\ \text{pA}$
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— t_{ON} : $85\ \text{ns}$

BENEFITS

- Low Charge Injection— Q : $1\ \text{pC}$
- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Low Cost

APPLICATIONS

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

DESCRIPTION

The versatile DG213 analog switch has two NC and two NO switches. It can be used in various configurations, including four single-pole single-throw (SPST), two single-pole double-throw (SPDT), one "T" switch, one DPDT, etc. This device is fabricated in a Vishay Siliconix' proprietary high-voltage silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

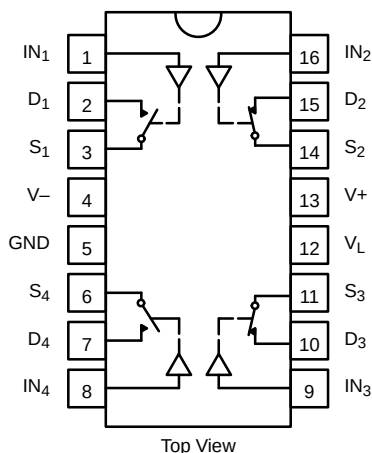
This analog switch was designed for a wide variety of general purpose applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge

injection compensation design minimizes switching transients. These switches can handle up to $\pm 22\ \text{V}$, and have an improved continuous current rating of $30\ \text{mA}$. An epitaxial layer prevents latchup.

All switches feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

For additional information, please refer to Application Note AN208 (FaxBack document #70606).

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	SW ₁ , SW ₄	SW ₂ , SW ₃
0	OFF	ON
1	ON	OFF

Logic "0" $\leq 0.8\ \text{V}$
Logic "1" $\geq 2.4\ \text{V}$

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG213DJ
	16-Pin Narrow SOIC	DG213DY
	16-Pin TSSOP	DG213DQ

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ 44 V

GND 25 V

Digital Inputs^a V_S, V_D (V–) –2 V to (V+) +2 V
or 30 mA, whichever occurs first

Current, Any Terminal 30 mA

Peak Current, S or D

(Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature –65 to 125°C

Power Dissipation (Package)^b16-Pin Plastic DIP^c 470 mW16-Pin Narrow SOIC^d 640 mW16-Pin TSSOP^d 500 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 6.5 mW/°C above 75°C

d. Derate 7.6 mW/°C above 75°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V VL = 5 V, VIN = 2.4 V, 0.8 V ^e	Temp ^a	D Suffix −40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	V−		V+	V
Drain-Source On-Resistance	r _{DS(on)}	VD = ±10 V, IS = 1 mA	Room Full		45	60 85	Ω
r _{DS(on)} Match	Δr _{DS(on)}		Room		1	2	
Source Off Leakage Current	IS(off)	VS = ±14 V, VD = ∓14 V	Room Full	−0.5 −5	±0.01	0.5 5	nA
Drain Off Leakage Current	ID(off)	VD = ±14 V, VS = ∓14 V	Room Full	−0.5 −5	±0.01	0.5 5	
Drain On Leakage Current	ID(on)	VS = VD = 14 V	Room Full	−0.5 −10	±0.02	0.5 10	
Digital Control							
Input Voltage High	V _{INH}		Full	2.4			V
Input Voltage Low	V _{INL}		Full			0.8	
Input Current	I _{INH} or I _{INL}	V _{INH} or V _{INL}	Full	−1		1	μA
Input Capacitance	C _{IN}		Room		5		pF
Dynamic Characteristics							
Turn-On Time	t _{ON}	VS = 10 V See Figure 2	Room		85	130	ns
Turn-Off Time	t _{OFF}		Room		55	100	
Break-Before-Make Time Delay	t _D	VS = 10 V, See Figure 3	Room	15	25		
Charge Injection	Q	CL = 1000 pF, Vg = 0 V, Rg = 0 Ω	Room		1		pC
Source-Off Capacitance	CS(off)	VS = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	CD(off)		Room		5		
Channel On Capacitance	CD(on)	VD = VS = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	CL = 15 pF, RL = 50 Ω VS = 1 VRMS, f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	XTALK		Room		95		

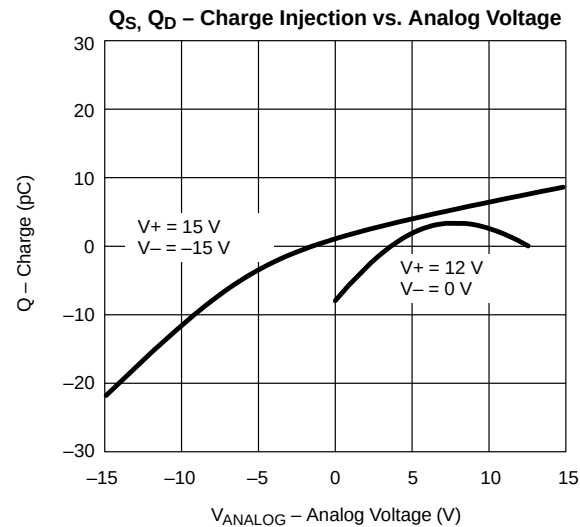
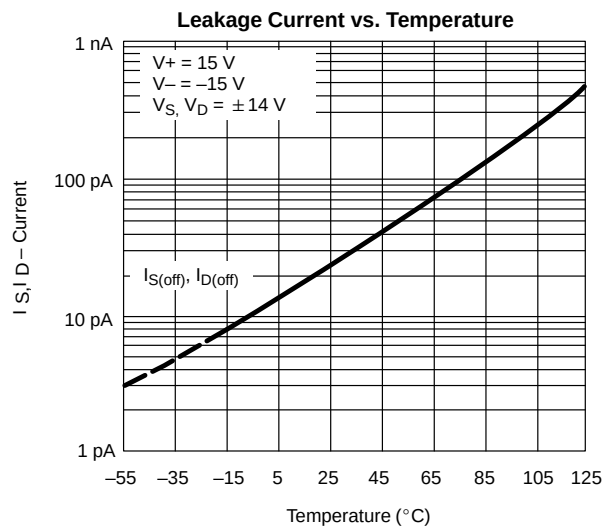
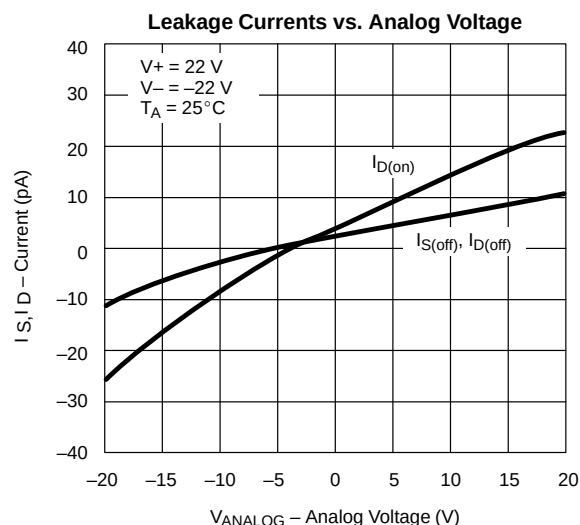
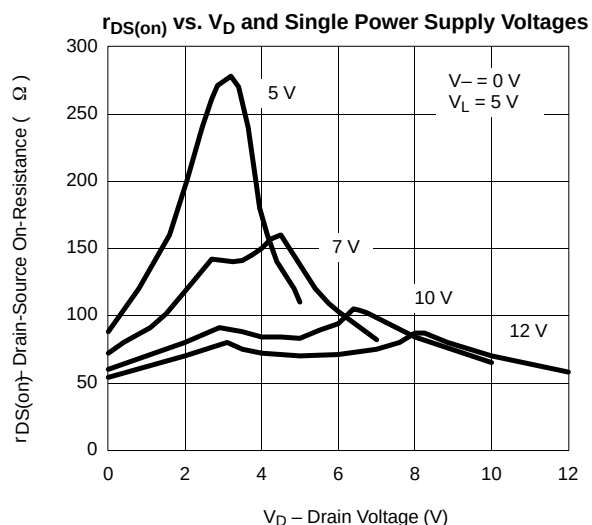
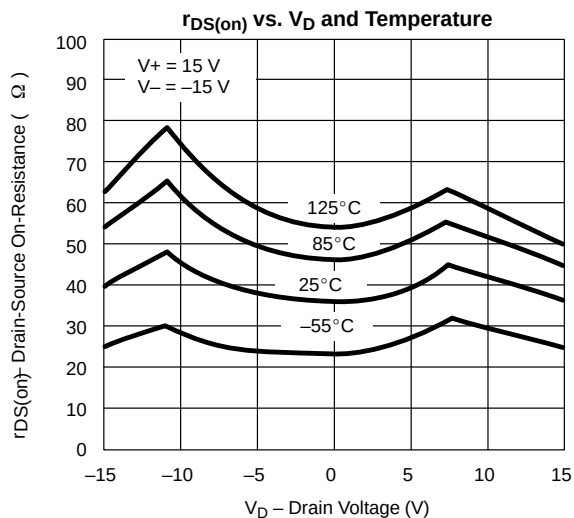
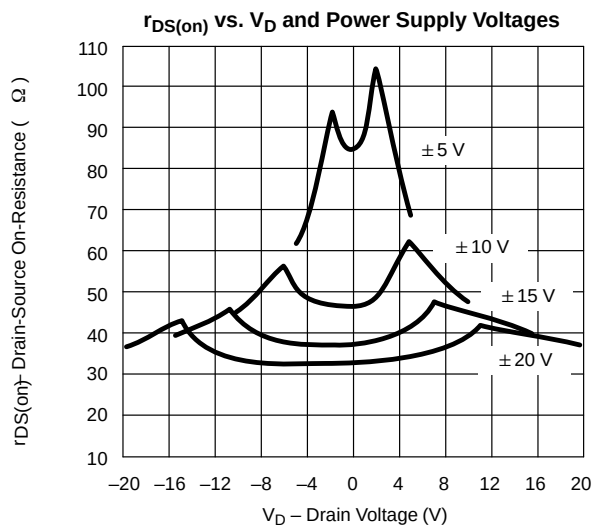


SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V VL = 5 V, VIN = 2.4 V, 0.8 V ^e	Temp ^a	D Suffix −40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Power Supply							
Positive Supply Current	I+	VIN = 0 or 5 V	Room Full			1 5	μA
Negative Supply Current	I−		Room Full	−1 −5			
Logic Supply Current	IL		Room Full			1 5	
Power Supply Range for Continuous Operation	VOP		Full	±3		±22	V

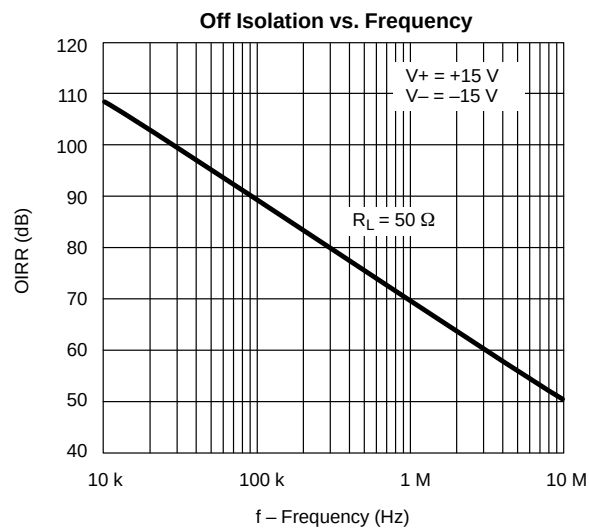
SPECIFICATIONS FOR UNIPOLAR SUPPLY							
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V VL = 5 V, VIN = 2.4 V, 0.8 V ^e	Temp ^a	D Suffix −40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	V−		V+	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = 3 V, 8 V, I _S = 1 mA	Room Full		90	110 140	Ω
Dynamic Characteristics							
Turn-On Time	t _{ON}	See Figure 2	Room		125	200	ns
Turn-Off Time	t _{OFF}		Room		45	100	
Break-Before-Make Time Delay	t _D	V _S = 8 V, See Figure 3	Room	50	80		
Charge Injection	Q	C _L = 1 nF, V _{gen} = 6 V, R _{gen} = 0 Ω	Room		4		pC
Power Supply							
Positive Supply Current	I+	VIN = 0 or 5 V	Room Full			1 5	μA
Negative Supply Current	I−		Room Full	−1 −5			
Logic Supply Current	IL		Room Full			1 5	
Power Supply Range for Continuous Operation	VOP		Full	+ 3		+ 40	V

Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

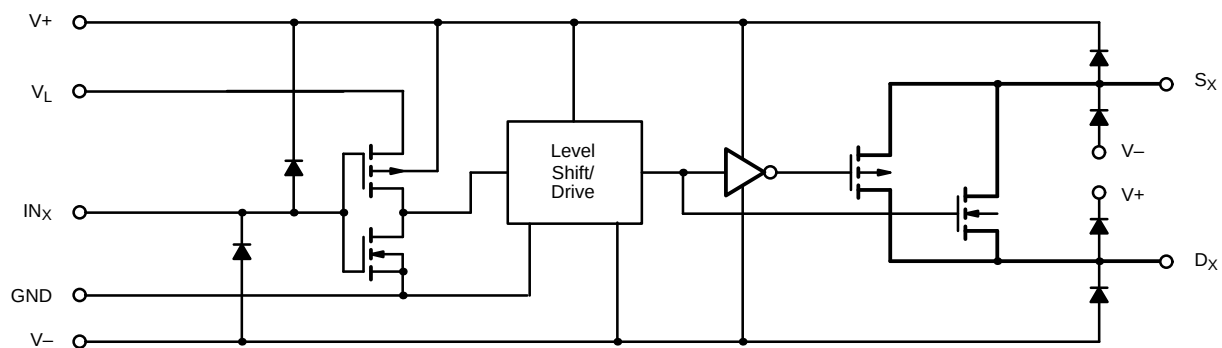


FIGURE 1.

TEST CIRCUITS

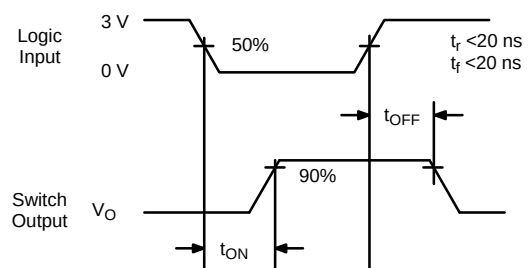
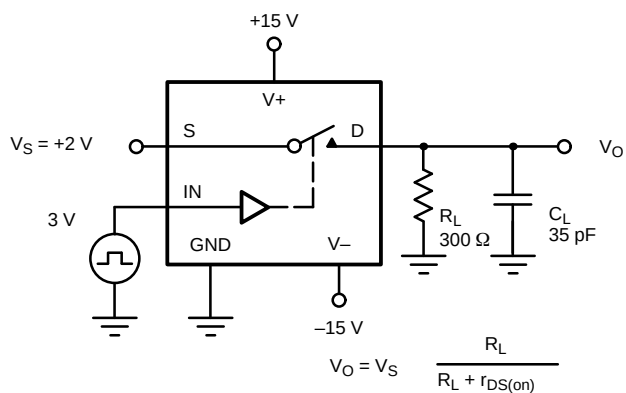


FIGURE 2. Switching Time

TEST CIRCUITS

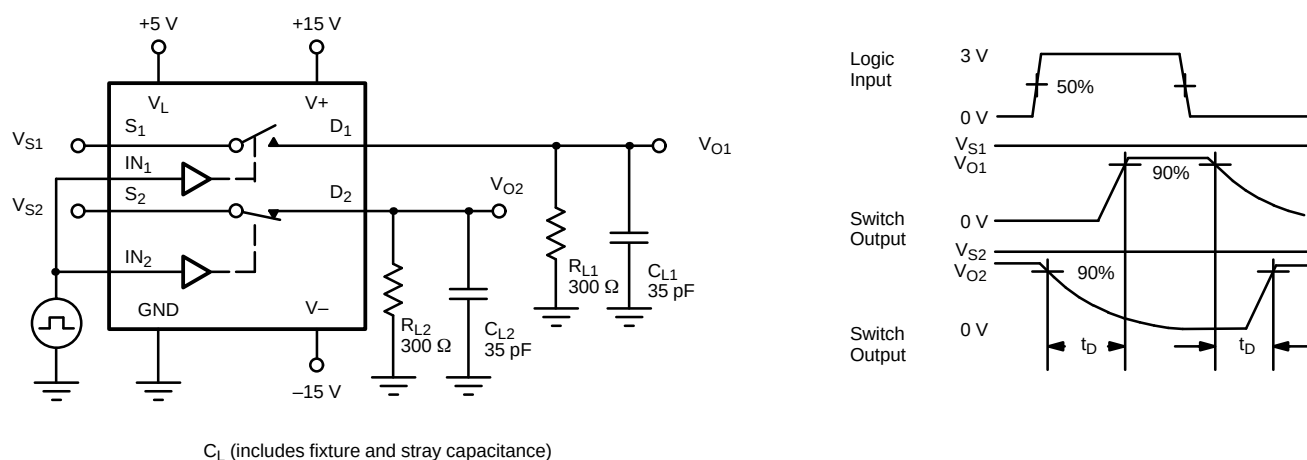


FIGURE 3. Break-Before-Make

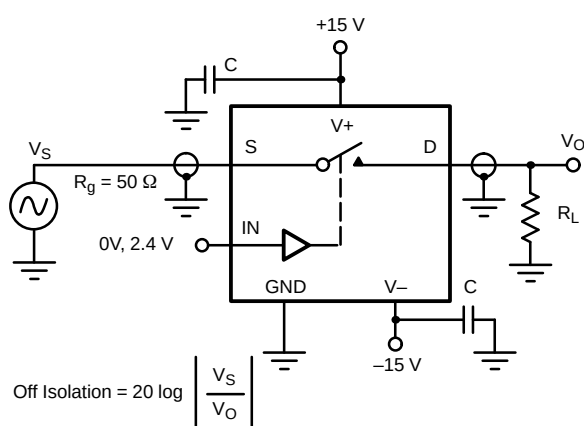


FIGURE 4. Off Isolation

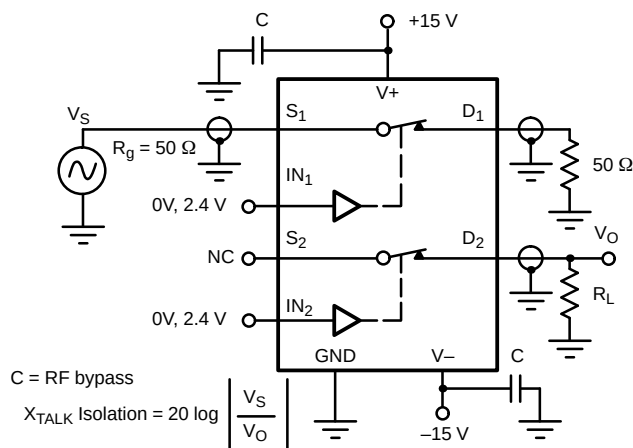


FIGURE 5. Channel-to-Channel Crosstalk

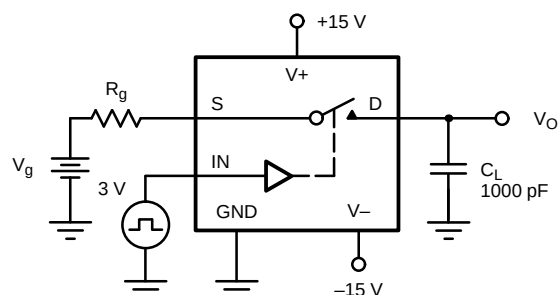


FIGURE 6. Charge Injection

APPLICATIONS

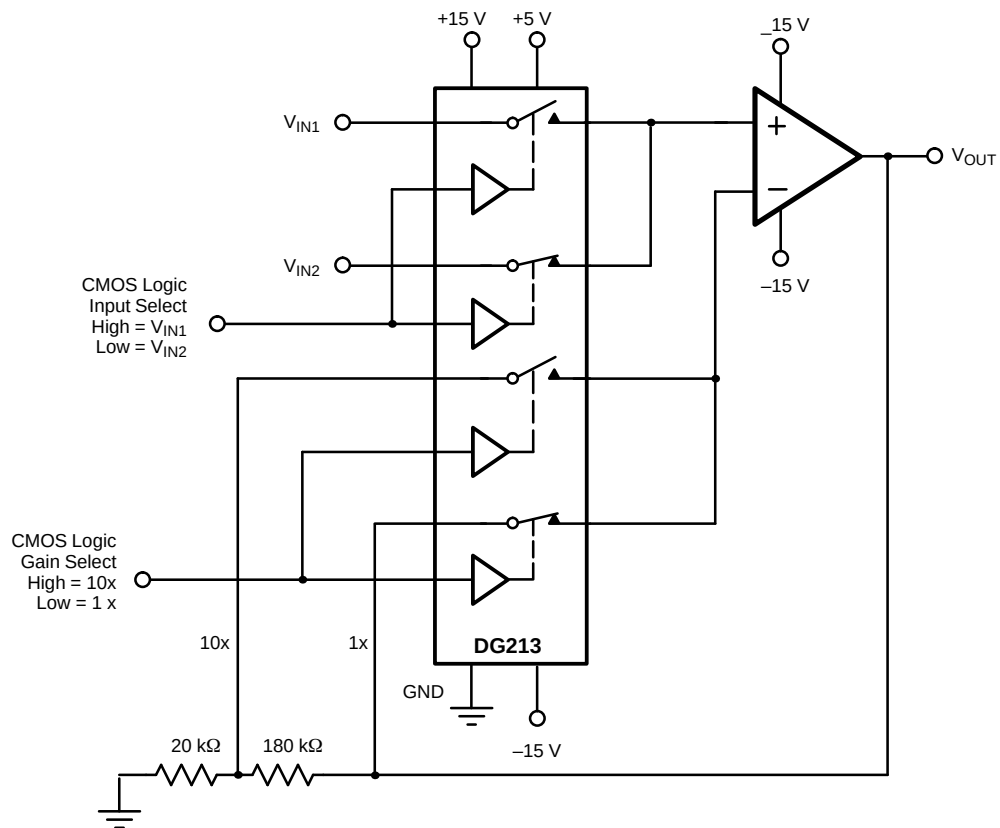


FIGURE 7. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain



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