

DDR5 SDRAM

Product Core Data Sheet

Features

- $V_{DD} = V_{DDQ} = 1.1V$ (nom)
- $V_{PP} = 1.8V$ (nom)
- On-die, internal, adjustable V_{REF} generation for DQ, CA, CS
- 1.1V pseudo open-drain I/O
- TC maximum up to 95°C
 - 32ms, 8192-cycle refresh up to 85°C
 - 16ms, 8192-cycle refresh at >85°C to 95°C
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- 16n-bit prefetch architecture
- 1 cycle/2 cycle command structure
- 2N mode
- All bank and same bank refresh
- Multi-purpose command (MPC)
- CS/CA training mode
- On-die ECC
- ECC transparency and error scrub
- Decision feedback equalization (DFE)
- Loopback mode
- Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination (ODT)
- sPPR and hPPR capability
- Write/read cyclic redundancy check (CRC)
- Per-DRAM addressability (PDA)
- DQ VREF training
- Duty cycle adjuster
- Mode register read/write
- Write leveling training
- Programmable preamble/postamble
- Data mask (DM)
- Refresh management (RFM)
- Per row activation counting (PRAC)
- Same bank precharge
- Maximum power saving mode (MPSM)
- JEDEC JESD79-5C compliant

Options¹

- Configuration
 - Refer to the DDR5 Die Revision-specific data sheet
- FBGA package (Pb-free) — x4, x8
 - Refer to the DDR5 Die Revision-specific data sheet
- FBGA package (Pb-free) — x16
 - Refer to the DDR5 Die Revision-specific data sheet
- Timing – cycle time
 - Refer to the DDR5 Die Revision-specific data sheet
- Operating temperature
 - Refer to the DDR5 Die Revision-specific data sheet

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on micron.com for available offerings.

General Specification Details

This document serves as the core data sheet specification for the DDR5 family of Micron DRAM products. Along with this core document, each DDR5 die revision has a specific data sheet specification (for example, 16Gb DDR5 SDRAM Die Revision A Data Sheet Addendum).

Where discrepancies may exist, content in the die-revision specific DDR5 data sheet addendum will supersede content defined in this core DDR5 specification.

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Important Notes and Warnings

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Basic Functionality

DDR5 is a high-speed dynamic random-access memory. The 8Gb density is internally configured as:

- x4/x8 devices: 16 banks (8 bank group with 2 banks for each bank group)
- x16 devices: 8 banks (4 bank group with 2 banks for each bank group)

With higher densities (greater than or equal to 16Gb), the bank resources double, enabling the device to be internally configured as:

- x4/x8 devices: 32 banks (8 bank group with 4 banks for each bank group)
- x16 devices: 16 banks (4 bank group with 4 banks for each bank group)

DDR5 uses a 16n pre-fetch architecture to achieve high-speed operation. The 16n pre-fetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation consists of a single 16n-bit wide, eight clock data transfer at the internal core and 16 corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

READ and WRITE operations are burst-oriented, start at a selected location, and continue for a burst length of 16 (BL16) or a chopped burst of eight (BC8) in a programmed sequence. Operation begins with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered with the ACTIVATE command are used to select the bank and row to be activated (see [DDR5 Addressing](#) for specific requirements). The address bits registered with the READ or WRITE command select the starting column location for the burst operation, determine if the AUTO PRECHARGE command is to be issued, and select BC8 on-the-fly (OTF), fixed BL16, fixed BL32 (optional), or BL32 OTF (optional) mode if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

This simplified state diagram is intended to provide an overview of the possible state transitions and the commands to control them. Some events are not captured in full detail; in particular, situations involving more than one bank and the enabling or disabling of on-die termination.

Figure 1: State transition diagram of the memory controller. The diagram illustrates the various states and transitions of the memory controller, including Power-On, Reset procedure, Connectivity test, Write leveling, PODTM, Self refreshing, Refresh Management, Refreshing, Maximum power saving mode, Read Training Pattern, VREFCA/VREFCS Training, Read Preamble Training, CS training mode, CA training mode, hPPR/mPPR/sPPR, ZQ calibration idle, MBIST, ZQ calibration active, Mode register read, Mode register write, Activating, PDA Select ID Mode, PDA enumeration mode, Pre-charged power-down, Active power-down, Awaiting dummy write, Bank active, Awaiting dummy read, Writing, and Reading. The legend defines the line styles: solid for 'A and B and C', dashed for 'A or B or C', dotted for 'Pin asserted', and dash-dot for 'Automatic sequence'. Solid lines with arrows represent command sequences.

Table 1: State Diagram Command Definitions

Abbreviation	Function
ACT	Activate
MPC	Multi-purpose command
MRR	Mode register read
MRW	Mode register write
NOP	No operation
PDE	Power-down entry mode
PDX (NOP)	Power-down exit mode
PREab	Precharge all banks
PREpb	Precharge per bank
PREsb	Precharge same bank
RD	Read
RDA	Read auto precharge
REFab	Refresh all banks
REFsb	Refresh same bank
RFMab	Refresh management all banks
RFMsb	Refresh management same bank
RFU	Reserved for future use
RESET_n	Start reset procedure
SRE	Self-refresh entry mode
SRX (NOP)	Self-refresh exit mode
SREF	Self refresh entry with frequency change
VREFCA	VREFCA command
VREFCS	VREFCS command
WR	Write
WRA	Write auto precharge
WRP	Write pattern
WRPA	Write pattern auto precharge

DDR5 Pinout Assignments

Table 2: Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All command/address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CS_n, CS1_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code and is used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode, the CS_n input buffer operates with the same ODT and V _{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh mode, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V _{DDQ} .
DM_n, DMU_n, DML_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM_n is not supported on x4 devices. For x8 devices, the function of DM_n is enabled by the mode register. For x16 devices, the function of DMU_n/DML_n is enabled by the mode register.
CA[13:0]	Input	Command/Address Inputs: Command/Address (CA) signals provide the command and address inputs according to the Command Truth Table. Because some commands are multicycle, the pins may not be interchanged between devices on the same bus.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V _{DDQ} .
DQ	Input/Output	Data Input/Output: Bidirectional data bus. If CRC is enabled via the mode register, CRC code is added at the end of a data burst.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/Output	Data Strobe: Output with read data, input with write data, edge-aligned with read data, centered in write data. For x16 devices, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. The device supports differential data strobe only, not single-ended.
TDQS_t, TDQS_c	Input	Termination Data Strobe: Applicable to x8 devices only. When enabled via the mode register, the device enables the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via the mode register, DM/TDQS provides the data mask function depending on the MR setting; TDQS_c is not used. x4/x16 devices must disable the TDQS function via the mode register.
ALERT_n	Input/Output	Alert: If there is an error in CRC, ALERT_n drives LOW for the period time interval and returns HIGH. During the connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In cases where this pin is not connected, ALERT_n must be bonded to V _{DDQ} on the system board.
TEN	Input	Connectivity Test Mode Enable: A HIGH on this pin enables CONNECTIVITY TEST MODE operation along with other pins. It is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of V _{DDQ} . Usage of this signal is system-dependent. This pin is pulled LOW internally with a weak pulldown resistor to V _{SS} .

Table 2: Pinout Description (Continued)

Symbol	Type	Function
MIR	Input	Mirror: Used to inform the system that this device is being run in mirrored mode instead of standard mode. With the MIR pin connected (strapped) to V_{DDQ} , the device internally swaps even-numbered CA with the next higher odd-number CA. The MIR pin must be tied to V_{SS} if no CA mirror is required. Mirror pair examples: CA2 with CA3 (not CA1) CA4 with CA5 (not CA3). Note: the CA[13] function is only relevant for certain densities (including stacking). In the case that CA[13] is not used, its ball location, considering whether MIR is used or not, should be connected (strapped) to V_{DDQ} . No active signaling requirements required.
CAI	Input	Command and Address Inversion: With this pin connected (strapped) to V_{DDQ} , the device internally inverts the logic level present on all CA signals. The CAI pin must be connected to V_{SS} if no CA inversion is required. No active signaling requirements required.
CA_ODT	Input	ODT for Command and Address: Apply Group A settings if the pin is connected (strapped) to V_{SS} ; apply Group B settings if the pin is connected (strapped) to V_{DDQ} . See the mode register defaults table for details. No active signaling requirements required.
LBDQ	Output	Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
LBDQS	Output	Loopback Data Strobe Output: A single-ended strobe with the rising edged aligned with loopback data edge, falling edge aligned with data center. When loopback is enabled, it is in driver mode using the default RON described in the Loopback function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
RFU	Input/Output	Reserved for future use.
DNU		Do not use.
NF		No function: Internal connection is present but has no function.
V_{DDQ}	Supply	DQ power supply; 1.1V nominal.
V_{DD}	Supply	Power supply; 1.1V nominal.
V_{SS}	Supply	Ground
V_{PP}	Supply	Activating power supply; 1.8V nominal.
ZQ, ZQ1	Reference	Reference pin for ZQ calibration. This ball is tied to an external 240 ohm resistor (RZQ), which is tied to V_{SS} .

DDR5 Addressing

Table 3: 8Gb Addressing

Configuration		2Gb x4	1Gb x8	512Mb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 2 / 16	8 / 2 / 16	4 / 2 / 8
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0	BA0	BA0
Row address		R0-R15	R0-R15	R0-R15
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Table 4: 16Gb Addressing

Configuration		4Gb x4	2Gb x8	1Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address		R0-R15	R0-R15	R0-R15
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Table 5: 24Gb Addressing

Configuration		6Gb x4	3Gb x8	1.5Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address ¹		R0-R16	R0-R16	R0-R16
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Note: 1. For non-binary memory densities, a quarter of the row address space is invalid. When the MSB address bit is HIGH, the MSB-1 address bit must be LOW.

Table 6: 32Gb Addressing

Configuration		8Gb x4	4Gb x8	2Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address		R0-R16	R0-R16	R0-R16
Column address		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-3 / 16H	CID0-3 / 16H	CID0-3 / 16H

Table 7: 64Gb Addressing

Configuration		16Gb x4	8Gb x8	4Gb x16
Bank address	Number of bank groups/number of banks per bank group/number of banks	8 / 4 / 32	8 / 4 / 32	4 / 4 / 16
	Bank group address	BG0-BG2	BG0-BG2	BG0-BG1
	Bank address in a bank group	BA0-BA1	BA0-BA1	BA0-BA1
Row address		R0-R17	R0-R17	R0-R17
Column address ¹		C0-C10	C0-C9	C0-C9
Page size		1KB	1KB	2KB
Chip IDs/maximum stack height		CID0-2 / 8H	CID0-2 / 8H	CID0-2 / 8H

Note: 1. While the column addressing rows indicate the LSB is C0, in fact, C0 and C1 are controlled internally by the burst logic. As shown in the Command Truth Table, C0 and C1 states are not selectable by any column access burst command such that the burst would be reordered.

Reset and Initialization Procedure

The table below defines the default values of the mode registers. Mode registers not shown in this table have a default value of zero (0).

Table 8: Mode Registers with Default States

Item	MR	Op-code(s)	Default Setting	Description
Burst Length	0	[1:0]	00b	BL16
CAS Latency (CL)	0	[6:2]	00010b	CL = 26 @3200
CAS Write Latency (CWL)	N/A	N/A	CWL = CL-2	Fixed; based on CL setting
PDA Enumerate ID	1	[3:0]	1111b	PDA enumerate ID
PDA Select ID	1	[7:4]	1111b	PDA select ID
Write Recovery	6	[3:0]	0000b	$t_{WR} = 48CK @3200^1$
Read to Precharge Delay	6	[7:4]	0000b	$t_{RTP} = 12CK @3200^1$
Write Preamble	8	[4:3]	01b	2 t_{CK}
V _{refDQ} Value	10	[7:0]	00101101b	V _{refDQ} Range: 75% of V _{DDQ}
V _{refCA} Value	11	[6:0]	0101101b	V _{refCA} Range: 75% of V _{DDQ}
V _{refCS} Value	12	[6:0]	0101101b	V _{refCS} Range: 75% of V _{DDQ}
ECS Error Threshold Count (ETC)	15	[2:0]	011b	256
Read Training Data0	26	[7:0]	Register value = 0x5A	
Read Training Data1	27	[7:0]	Register value = 0x3C	
Read LFSR	30	[7:0]	Register value = 0xFE	
CK ODT	32	[2:0]	Based on strap value	Group A = RTT_OFF = 000b Group B = 40 ohms = 111b
CS ODT	32	[5:3]	Based on strap value	Group A = RTT_OFF = 000b Group B = 40 ohms = 111b
CA ODT	33	[2:0]	Based on strap value	Group A = RTT_OFF = 000b Group B = 80 ohms = 100b
RTT_WR	34	[5:3]	001b	240 ohms
RTT_NOM_WR	35	[2:0]	011b	80 ohms
RTT_NOM_RD	35	[5:3]	011b	80 ohms
ODTLon_WR_Offset	37	[2:0]	100b	-1 clocks
ODTLoff_WR_Offset	37	[5:3]	101b	0 clocks
ODTLon_WR_NT_Offset	38	[2:0]	100b	-1 clocks
ODTLoff_WR_NT_Offset	38	[5:3]	101b	0 clocks
ODTLon_RD_NT_Offset	39	[2:0]	100b	-1 clocks
ODTLong_RD_NT_Offset	39	[5:3]	101b	0 clocks
RFM	58	[0]	See DDR5 Die Revision specific Datasheet	Refresh management required/not required
RFM RAAIMT	58	[4:1]	See DDR5 Die Revision specific Datasheet	Rolling accumulated ACT initial management threshold
RFM RAAMMT	58	[7:5]	See DDR5 Die Revision specific Datasheet	Rolling accumulated ACT maximum management threshold

Table 8: Mode Registers with Default States (Continued)

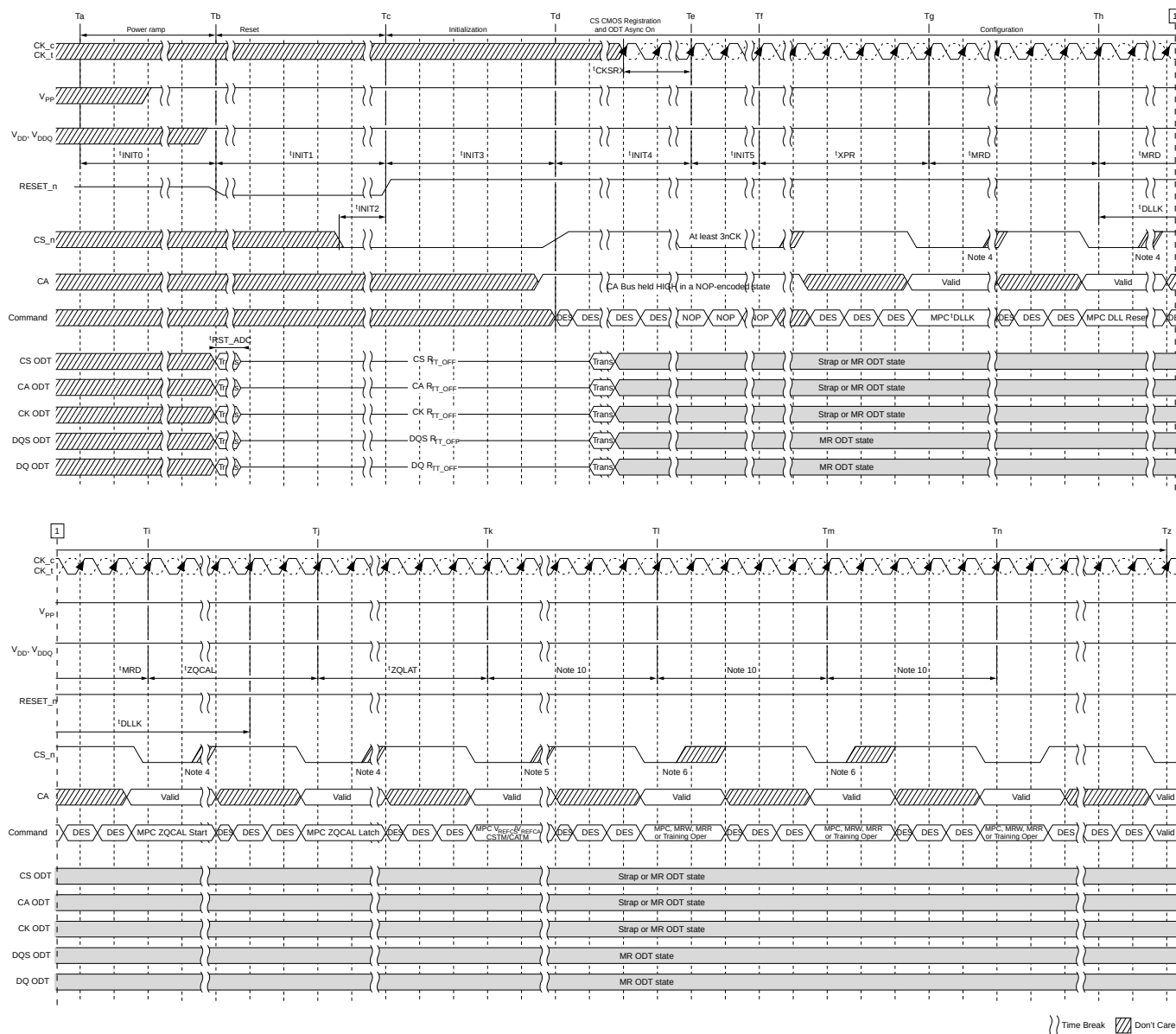
Item	MR	Op-code(s)	Default Setting	Description
RFM RAA Counter	59	[7:6]	See DDR5 Die Revision specific Datasheet	Rolling accumulated ACT counter decrement per REF command

Note: 1. See the Timing by Speed Grade Table for the timing parameter.

Power-up and Initialization

The following sequence and conditions are required for power-up and initialization, as shown in the figure below.

Figure 2: Reset and Initialization Sequence at Power-on Ramping



Notes: 1. From (Td) until (Te), the CA bus must be held HIGH in a NOP encoded state.

2. From (Te) until (Tf), NOP commands must be applied on the CA bus.

3. From (Tf) until (Tk), DES commands must be applied between legal commands (MRR, MRW, MPC, VREFCS, and VREFCA). MRR and MRW commands while legal, may not execute properly until CS and CA training routines are completed.
4. Prior to ZQcal completion at (Tk), MPC commands will be multicycle as described in the MPC Command Timing section.
5. From time point (Tk) until (Tl) all MPC, VREFCS and VREFCA commands prior to CS and CA training successfully completing, must be multicycle (MR2:OP[4] = 0) as described in the MPC, VREFCS, and VREFCA timing sections.
6. At time point (Tl), with successful completion of CS and CA training, an MRW command setting MR2:OP[4] = 1 is recommended and enables MPC, VREFCS, VREFCA commands to be single-cycle, improving training duration.
7. From time point (Tk) until (Tz), DES commands will be applied between legal commands (MRR, MRW, MPC, VREFCS and VREFCA).
8. Starting at (Tl), MRW commands must be issued to all mode registers that require non-default settings.
9. Default ODT tolerances are wider prior to ZQ calibration.
10. All MPC/MRW/MRR to MPC/MRW/MRR commands must meet the timing restrictions required.
11. From time point (Tk) until (Tz), the SRX/NOP clock-sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, the host shall issue an SRE/SRX pair to ensure that the clock-sync is in effect during DCA training. It is also applied for CS gear-down initialization sequence (for example, after power-up and initialization, CSTM, MPC (CS gear-down enable), sync pulse, CATM, MRW (SRX/NOP clock-sync enable), the host shall issue an SRE/SRX pair). The host (including RCD and clock driver) is responsible for ensuring the phases of the system clock during DCA training.

Table 9: Voltage Ramp Conditions

After	Application Conditions
Ta is reached	V _{PP} must be greater than V _{DD}

Notes: 1. Ta is the point when any power supply first reaches 300mV.

2. Voltage ramp conditions apply between Ta and power-off (controlled or uncontrolled).

3. Tb is the point at which all supply and reference voltages are within their defined ranges.

4. Power ramp duration (Tb-Ta) must not exceed t_{INIT0}.

Power-up Initialization Sequence

1. While applying power (after Ta), RESET_n must be LOW ($\leq 0.2 \times V_{DDQ}$) while all other inputs may be undefined. The device outputs remain disabled while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the Input Voltage Power-up and Power-down Sequence section that follows. During power up and power down, |V_{DDQ}-V_{DD}| must be equal to or less than 200mV, and V_{PP} must always be equal to or greater than V_{DDQ}.
2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DQS_t, DQS_c, CS_n, CK_t, CK_c and CA input levels must be between V_{SS} and V_{DDQ} to avoid latch-up.
3. Beginning at Tb, RESET_n must be maintained LOW for a minimum of t_{INIT1} (Tb to Tc), after which RESET_n may be de-asserted to HIGH (Tc). At least t_{INIT2} (10ns) before RESET_n deassertion, CS_n must be set LOW. All other input signals are don't care. The device supports the ability for RESET_n to be held LOW indefinitely.
4. After RESET_n is de-asserted (Tc), wait at least t_{INIT3} before driving CS_n HIGH.
5. After CS_n deasserts HIGH (Td), wait a minimum of t_{INIT4} to enable the CS_n, CK and CA, DQ, and DQS ODT to go to the defined strap initial state (Te). Clock (CK_t, CK_c) is required to be started and stabilized for t_{CKSRX} before exit of t_{INIT4} (Te). Upon the completion of (Te), all ODT states (CA, CS_n, CK, DQ and DQS ODT) should be valid. The CS receiver should no longer be in its CMOS-based mode. ODT termination states remain uncalibrated until completion of ZQcal at (Tj).
6. Upon (Te), NOP commands must be issued for a minimum of t_{INIT5} to conclude exit of initialization process and start t_{XPR} timer at (Tf). The system must wait at least t_{XPR} before issuing any legal configuration commands (Tg). During early configuration steps (Tg to Tk), only MRR,

MRW, MPC, VREFCS and VREFCA commands are legal. MRR and MRW command while legal, may not execute properly until CS and CA training routines are completed.

7. Between (Tg) and (Tj), the following initial configuration modes must be completed prior to other training modes:
 - a) MPC for setting MR13 ($t_{\text{CCD}}/t_{\text{DLLK}}/t_{\text{CCD\_L\_WR}}/t_{\text{CCD\_L\_WR2}}$) must be issued before the MPC command to reset the DLL.
 - b) MPC to execute DLL RESET must be issued before ZQCal Start.
 - c) MPC to execute ZQCal Start followed by ZQCal Latch must be issued before any other training modes such as V_{REFCS} , V_{REFCA} , CS and CA Training.
8. Between (Tk to Tz), any number of legal configuration commands are allowed. Many training-based commands are optional and may be done at the system architect's discretion and may vary depending on the system, though proper setting of certain registers, such as those related to write leveling training, is required. The host must follow multicycle MPC timing requirements in cases where the alignment between CS_n, CA and CK is unknown, (that is, prior to successfully completing VREFCS, VREFCA, CS and CA training commands or host-provided successful training solutions). MRW and MRR commands can be used after the alignment between CS_n, CA and CK are known. Single-cycle CS_n assertions are allowed after setting MR2:OP[4] = 1.
9. Between (Tk to Tz), the SRX/NOP clock-sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/ CATM prior to DCA training, the host shall issue an SRE/SRX pair to ensure that the clock-sync is in effect during DCA training. It is also applied for CS geardown initialization sequence (for example, after power-up and initialization, CSTM, MPC (CS geardown enable), Sync Pulse, CATM, MRW (SRX/NOP clock-sync enable), the host shall issue an SRE/SRX pair). The host (including RCD and clock driver) is responsible for ensuring the phases of the system clock during DCA training to make the DCA training effective with the consistent phases of system and DRAM internal clocks.
10. After (Tz), and the completion of any training or calibration timing parameters (t_{ZQLAT}) is satisfied, the device is ready for normal operation and is able to accept any valid command. Any additional mode registers that have not previously been set up for normal operation should be written at this time. If the host uses writeback suppression mode, it should be set after the initial write process to prevent aliasing to a 2-bit error.
11. After all mode registers have been programmed for normal operation, optional MBIST mode can be entered by writing MR23:OP[4] to HIGH, followed by subsequent MR24 PPR guard keys. The device then drives ALERT_n to LOW for a maximum of t_{SELFTEST} time. The device drives ALERT_N to HIGH to indicate the operation is complete. After ALERT_n is driven HIGH, the device is immediately ready to receive valid commands. The MBIST/mPPR transparency status must subsequently be checked in MR22:OP[2:0] to determine whether mPPR should be performed. See the [MBIST/mPPR](#) section for more detailed operation procedures.

Table 10: Initialization Timing Parameters

Parameter	Value		Unit	Comment
	MIN	MAX		
t_{INIT0}	–	20	ms	Maximum voltage ramp time
t_{INIT1}	200	–	μs	Minimum RESET_n LOW time after completion of voltage ramp
t_{INIT2}	10	–	ns	Minimum CS_n LOW time before RESET_n HIGH
t_{INIT3}	4	–	ms	Minimum CS_n LOW time after RESET_n HIGH
t_{INIT4}	2	–	μs	Minimum time for the device to register EXIT on CS with CMOS and assert the device default ODT values
t_{INIT5}	3	–	nCK	Minimum NOP cycles required after CS_n HIGH to exit RESET
t_{XPR}	t_{XS}	–	ns	Minimum time from exit RESET to first valid configuration command

Table 10: Initialization Timing Parameters (Continued)

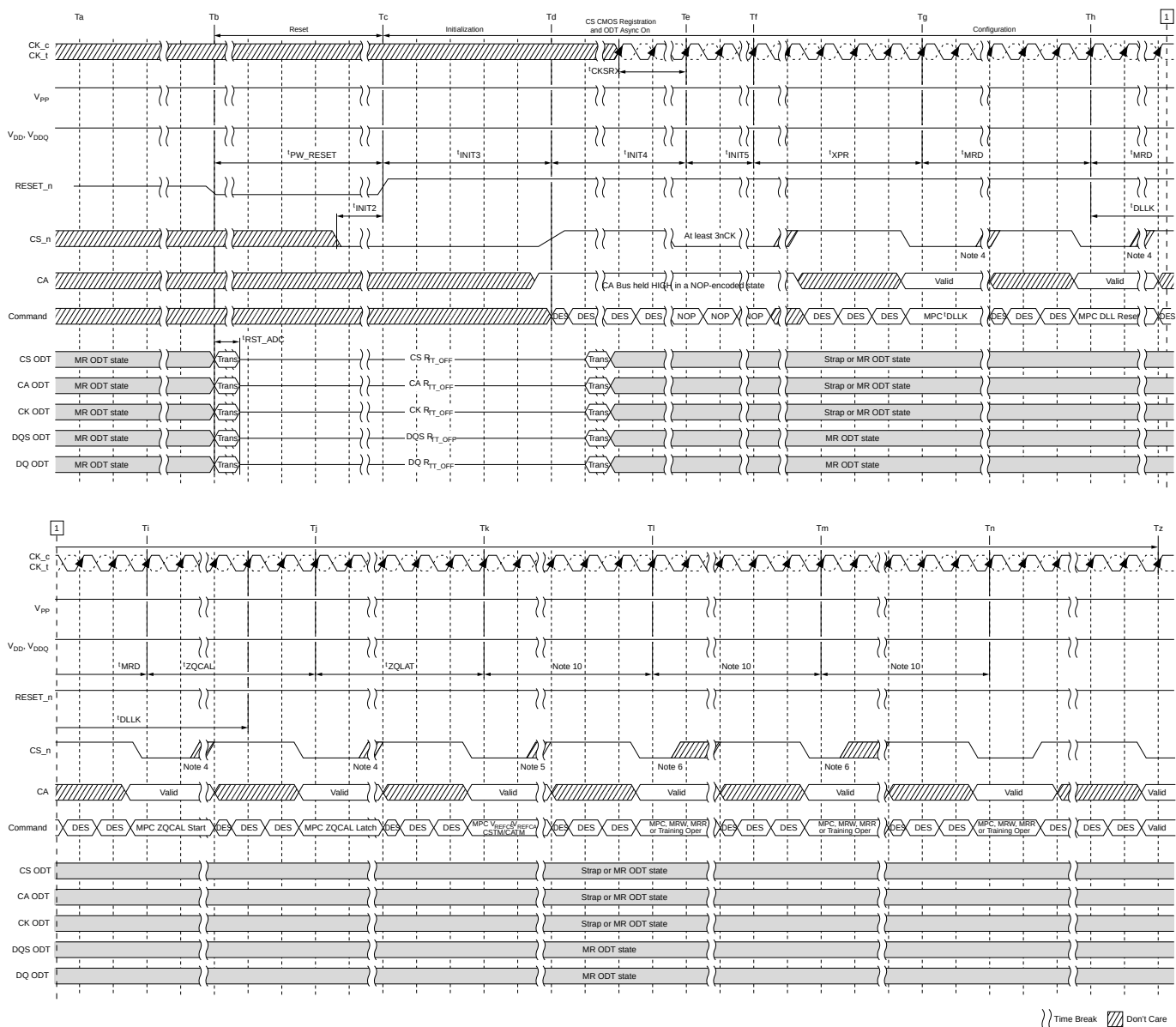
Parameter	Value		Unit	Comment
	MIN	MAX		
t_{CKSRX}	See Self-Refresh Timing Table		–	Minimum stable clock time

Reset Initialization with Stable Power

The following sequence is required for RESET with no power interruption in order to provide proper initialization of the device as shown in the figure below.

1. Assert RESET_n below $0.2 \times V_{DDQ}$ any time when reset is required. RESET_n must be maintained for a minimum time of t_{PW_RESET} . CS_n must be held LOW at least t_{INIT2} before deasserting RESET_n.
2. Repeat steps 4 through 11 in the [Power-up Initialization Sequence](#) section.

Figure 3: Reset Procedure with Stable Power



- Notes: 1. From time point (Td) until (Te), the CA bus must be held HIGH in a NOP encoded state.
2. From time point (Te) until (Tf), NOP commands must be applied on the CA bus.
3. From time point (Tf) until (Tk), DES commands must be applied between legal commands (MRR, MRW, MPC, VREFCS, and VREFCA) and MRR/MRW is legal if the timing alignment for a 2-cycle command is configured properly.
4. Prior to ZQcal completion at (Tk), MPC commands shall be multi-cycle as described in the MPC command timings section.
5. From time point (Tk) until (Ti) all MPC, VREFCS and VREFCA commands prior to CS and CA training successfully completing, will be multicycle (MR2:OP[4] = 0) as described in the MPC, VREFCS, and VREFCA timing sections.
6. At time point (Ti), with successful completion of CS and CA training, an MRW command setting MR2:OP[4] = 1 is recommended and enables MPC, VREFCS, VREFCA commands to be single-cycle, improving training duration.
7. From time point (Tk) until (Tz), DES commands will be applied between legal commands (MRR, MRW, MPC, VREFCS and VREFCA).
8. Starting at (Ti), MRW Commands must be issued to all mode registers that require nondefault settings.
9. Default ODT tolerances are wider prior to ZQ calibration.

10. All MPC/MRW/MRR to MPC/MRW/MRR commands must meet the timing restrictions required.
11. MRR is legal after DLL_reset.
12. From time point (Tk) until (Tz), the SRX/NOP clock-sync feature can be enabled through an MRW command by programming MR13:OP[5]=1. When it is enabled, after CSTM/CATM prior to DCA training, the host shall issue an SRE/SRX pair to ensure that the clock-sync is in effect during DCA training. It is also applied for CS geardown Initialization sequence (for example, after power-up and initialization, CSTM, MPC (CS geardown enable), sync pulse, CATM, MRW (SRX/NOP clock-sync enable), the host shall issue an SRE/SRX pair). The host (including RCD and clock driver) is responsible for ensuring the phases of the system clock during DCA training.

Input Voltage Power-up and Power-down Sequence

Once V_{DD} and V_{DDQ} reach nominal operating conditions, $|V_{DDQ} - V_{DD}| < 66\text{mV}$.

Figure 4: Requirement for Voltage Ramp Control

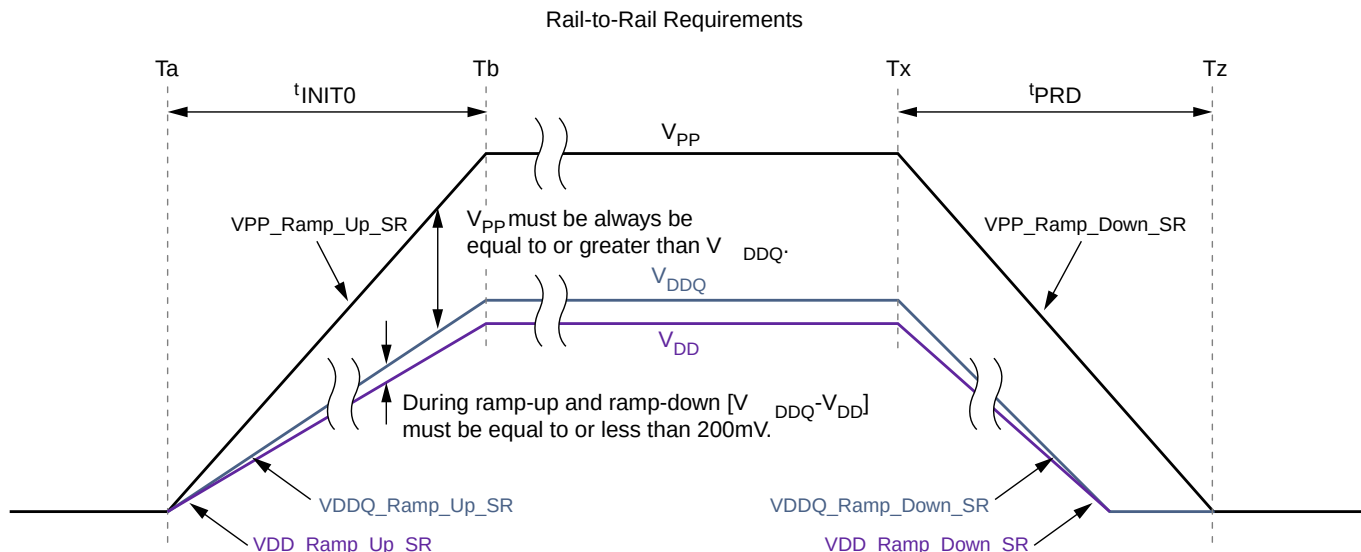


Table 11: Input Voltage Slew Rates and Power Ramp Down Time

Description	Symbol	MIN	MAX	Units	Notes
V_{PP} Rail	$V_{PP\_Ramp\_Up\_SR}$	0.2	5	V/ms	1, 2, 3
	$V_{PP\_Ramp\_Down\_SR}$	0.1	4.5	V/ms	1, 2, 3
V_{DD} Rail	$V_{DD\_Ramp\_Up\_SR}$	0.1	4.5	V/ms	1, 2, 3
	$V_{DD\_Ramp\_Down\_SR}$	0.1	4.5	V/ms	1, 2, 3
V_{DDQ} Rail	$V_{DDQ\_Ramp\_Up\_SR}$	0.1	4.5	V/ms	1, 2, 3
	$V_{DDQ\_Ramp\_Down\_SR}$	0.1	4.5	V/ms	1, 2, 3
Power Ramp Down Time	t_{PRD}	-	19.08	ms	

Notes: 1. All supply measurements made between 10% and 90% nominal voltage.

2. 1 MHz bandwidth limited measurement.

3. V_{PP} must be equal to or greater than V_{DD}/V_{DDQ} at all times.

4. During ramp up and ramp down $|V_{DDQ} - V_{DD}|$ must shall be equal or less than 200mV.

5. After t_{INIT0} , all supplies must be within their specified tolerance, as defined in the DC Operating tables.

Mode Registers

Note: Mode Register assignments (MRs and OP codes) for DDR5 are defined in this section and supersede any assignments found elsewhere in this document.

For application flexibility, various functions, features, and modes are programmable in up to 256 byte-wide mode registers. The mode registers are selectable by eight address bits (MRAs) provided as part of the MODE REGISTER WRITE (MRW) and MODE REGISTER READ (MRR) access commands.

The mode registers are divided into various fields depending on functionality and/or modes. As not all mode registers (MR#) have default values defined, contents of mode registers must be initialized and/or re-initialized (i. e., written) after power up and/or reset for proper operation. Additionally, the contents of the mode registers can be altered using the MRW command during normal operation.

When programming the mode registers, all address fields within the accessed mode register must be redefined when the MRW command is issued—even if only a subset of the MRW Op Code fields is modified. The MRW command does not directly affect array contents, which means this command can be executed any time after power-up without affecting the array contents.

MODE REGISTER READ

The MODE REGISTER READ (MRR) command reads configuration and status data from the device mode registers. The MRR command is initiated with CS_n and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[7:0]) enable selection of one of 256 registers. The mode register contents are available on the second 8 UIs of the burst and are repeated across all DQs after the CL following the MRR command. To avoid a potentially worst-case pattern, every odd DQ bit has its contents inverted (represented with an !). Data in the burst (UI 0-7) is either 0 or 1, with 1 indicating the content of the later UI's (UI 8-15) is inverted.

MRR commands require all banks to be idle on the DRAM. For 3DS, MRR commands require all banks to be idle on all logical ranks. The 3DS base die (CID[3:0] = 0x0) is the targeted logical rank for most MRR commands, however the CID setting of MR14:OP[3:0] designates the targeted logical rank for MRR commands to MR14–MR20, MR22 and MR54–MR57, and still requires all banks to be idle not only on the targeted logical rank but also on all other logical ranks.

DQS is toggled for the duration of the MRR burst. The MRR has a command burst length of 16, regardless of the MR0 setting, the training mode, or the mode register address. MRR termination control and ODT timings are the same as for the READ command. The MRR operation must not be interrupted.

Non-target ODT encoding is available for MRR, similar to a normal READ operation. MRR NT ODT termination control and ODT timings are the same as for the READ NT command.

When Read CRC is enabled, the MRR output will come with BL18 (BL16 plus 2 CRC-bit), but the host has the option to consider the 17th and 18th bits don't care for MRR handling. Regardless if the host uses the 17th and 18th bits while Read CRC is enabled, the strobe toggles for BL18.

Figure 5: Mode Register Read Timing

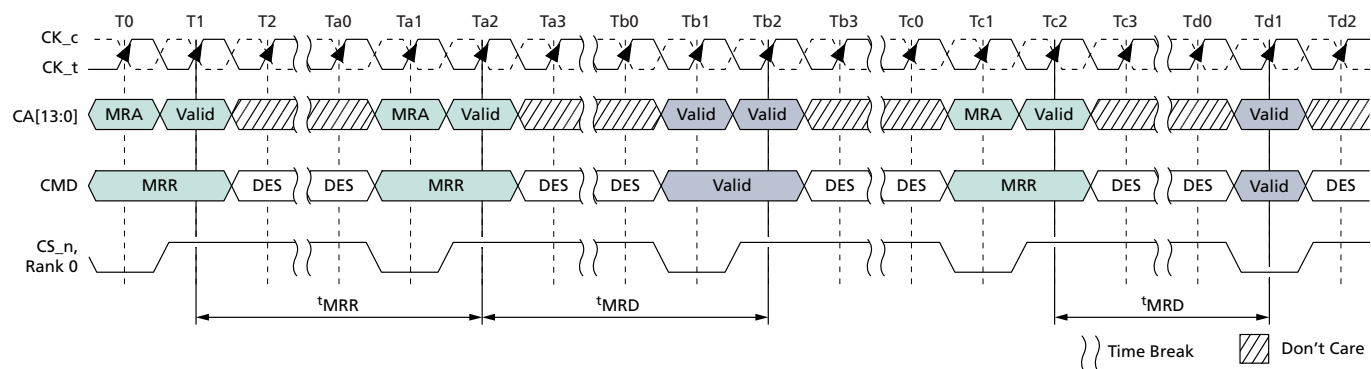


Table 12: DQ Output Mapping for x4 Devices

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Note: 1. The MRR's read preamble and postamble are the same as a normal READ command.

Table 13: DQ Output Mapping for x8 Devices

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Note: 1. The MRR's read preamble and postamble are the same as a normal READ command.

Table 14: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Registers Excluded)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

**Table 14: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Registers Excluded)
(Continued)**

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

- Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.
2. Mode register data output is only duplicated and inverted across the lower byte DQs of a x16 device. The host should treat the upper byte DQs as don't care values.
3. Output map excludes per-bit DFE, DCA, and VREFDQ mode registers (MR103–MR255).

Table 15: DQ Output Mapping for x16 Devices (MR46-47)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

- Notes: 1. The read preamble and postamble are the same as a normal READ command.
2. Output map excludes per-bit DFE, DCA, and VREFDQ mode registers (MR103–MR255).

Table 16: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Lower Byte – DQ[7:0], DML)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ8	Don't Care								
DQ9									
DQ10									
DQ11									
DQ12									
DQ13									
DQ14									
DQ15									

- Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.
2. Mode register data output is only duplicated and inverted across the lower byte DQs of a x16 device when reading from a per-bit DFE register associated with a lower byte DQ or DML. The host should treat the upper byte DQs as don't care values.
3. Output map is for per-bit DFE, DCA, and VREFDQ mode registers (MR103-MR255) only.

Table 17: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Upper Byte – DQ[15:8], DMU)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ0	Don't Care								
DQ1									
DQ2									
DQ3									
DQ4									
DQ5									
DQ6									
DQ7									
DQ8	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ9	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ10	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ11	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ12	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7

Table 17: DQ Output Mapping for x16 Devices (per-bit DFE, DCA and VREFDQ Upper Byte – DQ[15:8], DMU) (Continued)

	UI								
	0-7	8	9	10	11	12	13	14	15
DQ13	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ14	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ15	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

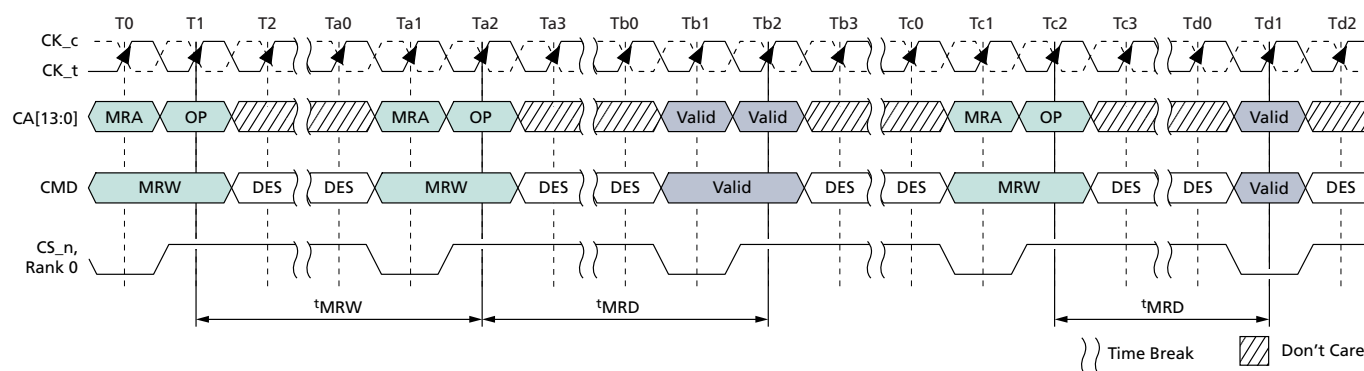
- Notes: 1. The MRR's read preamble and postamble are the same as a normal READ command.
2. Mode register data output is only duplicated and inverted across the upper byte DQs of a x16 device when reading from a per-bit DFE register associated with a upper byte DQ or DMU. The host should treat the lower byte DQs as don't care values.
3. Output map is for per-bit DFE, DCA, and VREFDQ mode registers (MR103-MR255) only.

MODE REGISTER WRITE

The MODE REGISTER WRITE (MRW) command writes configuration data to the device mode registers. The MRW command is initiated with CS and CA[13:0] in the proper state as defined by the Command Truth Table. The mode register address and the data written to the mode registers is contained in CA[13:0] according to the Command Truth Table. The MRW command period is defined by t_{MRW} . Mode register writes to read-only registers have no impact on device functionality.

MRW commands require all banks to be idle on the DRAM. For 3DS, MRW commands are broadcast across all logical ranks, requiring all banks to be idle on all logical ranks. For 3DS, MBIST Enable (MR23:OP[4] = 1) is only enabled on the target logical rank designated by CID[3:0] and programmed by MRW via MR14:OP[3:0], but still requires all banks to be idle on all logical ranks.

Figure 6: Mode Register Write Timing



DFE Mode Register Write Update Timing

This mode register update timing parameter applies for MR112 (MA[7:0]=70H) through MR254 (MA[7:0]=F8H) — mode registers for DFE including DFE Gain Bias, DFE Tap-1, DFE Tap-2, DFE Tap-3, DFE Tap-4 mode registers

Figure 7: DFE Update Setting

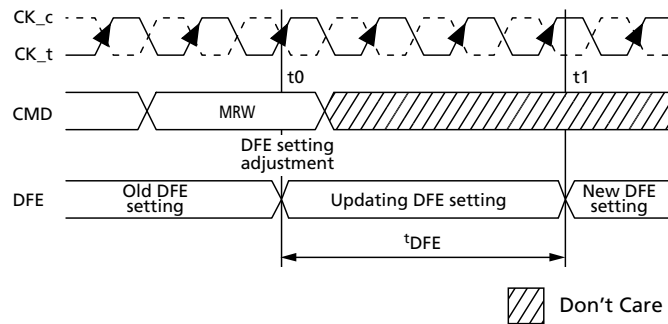


Figure 8: Example MRR to MRW Timing Diagram for Same Physical Rank

)) Time Break Don't Care

- Table 18: MRR and MRW Truth Table**

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Mode Register Reading (all banks idle)	All banks idle
All banks idle	MRW	Mode Register Writing (all banks idle)	All banks idle

Note: 1. For 3DS, MRR commands and MRW commands require all banks to be idle on all logical ranks.

Table 19: MRR/MRW Timing Constraints

From Command	To Command	Minimum Delay Between From Command and To Command	Unit	Notes
MRR	MRR	t_{MRR}/t_{MRR_p}	–	2, 4
	MRW	$CL + BL/2 + \text{MAX}[1, \text{ODTLoff\_RD\_NT\_Offset}]$	t_{CK}	2, 3
	MPC	$CL + BL/2 + \text{MAX}[1, \text{ODTLoff\_RD\_NT\_Offset}]$	t_{CK}	2, 3
	VREFCA/VREFCS	$CL + BL/2 + \text{MAX}[1, \text{ODTLoff\_RD\_NT\_Offset}]$	t_{CK}	2, 3
	Any other valid command	t_{MRD}	–	1, 2
MRW	MRW	t_{MRW}	–	
	Any other valid command	t_{MRD}	–	
RDA	MRR	$t_{RTP} + t_{RP}$	–	
	MRW	$t_{RTP} + t_{RP}$		
WRA	MRR	$CWL + BL/2 + t_{WR} + t_{RP}$	–	
	MRW	$CWL + BL/2 + t_{WR} + t_{RP}$	–	
PRE	MRR	t_{RP}	–	
	MRW	t_{RP}	–	
REF	MRR	t_{RFC}	–	
	MRW	t_{RFC}	–	

Notes: 1. All data bursts in progress must be completed before entry into self refresh or power-down mode.
 2. MRR can refer to both TARGET ODT MRR and NON-TARGET ODT MRR.
 3. Minimum delay is 1 clock after the burst or until the ODT offset requirements for DQS/DQ are met.
 4. During Read Training, MRR to MRR command spacing can be t_{MRR_p} .

Mode Register Definitions

DDR5 devices support up to 8 mode register address (MRA) bits, each with a byte-wide payload, enabling up to 256 byte-wide registers.

The MRA and payload placed in op-codes (OP[7:0]) are all packeted in the command/address (CA[13:0]) bus encoding method. For more information, refer to the Command Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW) command protocols.

The DDR5 Mode Register Assignments table summarizes the mode registers for DDR5.

- The default state (at power-up or after reset) of each mode register (MR) bit is zero (0), except as listed in the [Mode Registers with Default States](#) table in the RESET and Initialization Procedure section.
- A MODE REGISTER READ (MRR) command reads a mode register. A MODE REGISTER WRITE (MRW) command writes a mode register.
- Each bit in a register byte (MR#) is denoted as R if it can be read but not written, W if it can be written only, and R/W if it can be read and written. MR reads to write-only (W) registers always produce a zero (0) for those specific bits. Additionally, a DRAM read-only bit combined with a host write-only bit is denoted as a SR/W bit. This bit allows the DRAM to return a defined status during a read of that bit (SR = status read), independent of what the host may have written to the bit.
- A defined register byte (MR#) is any MR# that has at least one defined bit. When a defined register byte (MR#) contains an RFU bit, the host must write a zero (0) for those specific bits, and the DRAM does not guarantee any operation of those specific RFU bits. When the host issues an MRR to a defined register (MR#) that contains RFU bits in it, those specific bits will always produce a zero (0).
- If an entire MR# is marked RFU, it is considered undefined and all bits from the device are “Don't Care” for reads or writes. These undefined mode registers (completely empty bytes, not individual bits of an MR) may not be supported in the device.
- In cases where a mode register is specific to a particular device configuration (x4 ,x8, x16) and/or density (8Gb, 16Gb, 32Gb), the following rules apply:
 - With a DRAM configured as a x4/x8 device, an entire MR# used only for a x16 device is considered RFU. These bits are don't care for reads and writes, and they may be unsupported.
 - When a bit field within a register is used by a different configuration or density than a given device, the host may write/read programmed values to these fields, but device operation will not be affected.

Table 20: DDR5 Mode Register Assignments

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	CAS Latency (CL)						Burst Length	
1	PDA Select ID				PDA Enumerate ID			
2	Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	WL Training	Read Preamble Training
3	Write Leveling Internal Cycle Alignment – Upper Byte				Write Leveling Internal Cycle Alignment – Lower Byte			
4	TUF	RFU	Wide Range	Refresh ^t RFC Mode	Refresh Interval Rate Indicator	Refresh Rate		
5	Pull-down Output Driver Impedance		DM Enable	TDQS Enable	PODTM Support	Pull-up Output Driver Impedance		Data Output Disable
6	^t RTP				Write Recovery Time			
7	RFU						(Optional) Write Leveling Internal + 0.5 ^t CK Alignment Offset - Upper Byte	(Optional) Write Leveling Internal + 0.5 ^t CK Alignment Offset - Lower Byte
8	Write Postamble Settings	Read Postamble Settings	RFU	Write Preamble Settings		Read Preamble Settings		
9	TM	RFU						
10	V _{REFDQ} Calibration Settings							
11	Valid	V _{REFCA} Calibration Settings						
12	Valid	V _{REFCS} Calibration Settings						
13	RFU		SRX/NOP Clock-Sync Support and Enable/Disable at Next SRX (optional)	CS Geardown Enable/Disable at Next SREF	^t CCD_L/ ^t CCD_L_WR/ ^t CCD_L_WR2/ ^t DLLK			
14	ECS Mode	Reset ECS Counters	Row Mode/Code Word Mode	RFU	CID3	CID2	CID1	CID0
15	x4 Writes	ECS Writeback	RFU		Automatic ECS in Self Refresh	Transparency – ECS Threshold per Gb of Memory Cells		
16	Transparency – Address of Row with Max Errors 1							
17	Transparency – Address of Row with Max Errors 2							
18	RFU	Transparency – Address of Row with Max Errors 3						
19	PASR	RFU	Transparency – Max Row Errors					

Table 20: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
20	Transparency – Error Count of Rows or Code Words with Errors							
21	RFU					Rx DQS CTLE Control (optional)		
22	Rx CS_n CTLE Control (optional)		Rx CA CTLE Control (optional)		Rx CTLE Support	MBIST/mPPR Transparency (optional)		
23	RFU			MBIST (optional)	mPPR (optional)	sPPR enable		hPPR
24	PPR Guard Key							
25	RFU				Continuous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format
26	Read Training Pattern Data0/LFSR0 Seed							
27	Read Training Pattern Data1/LFSR1 Seed							
28	Read Training Pattern Invert DQL7:0 (DQ7:0)							
29	Read Training Pattern Invert DQU7:0 (DQ15:8)							
30	LFSR Assignment DQL7/DQU7	LFSR Assignment DQL6/DQU6	LFSR Assignment DQL5/DQU5	LFSR Assignment DQL4/DQU4	LFSR Assignment DQL3/DQU3	LFSR Assignment DQL2/DQU2	LFSR Assignment DQL1/DQU1	LFSR Assignment DQL0/DQU0
31	Read Training Pattern Address							
32	RFU	CA_ODT Strap Value	CS ODT			CK ODT		
33	RFU		DQS_RTT_PARK			CA ODT		
34	RFU		RTT_WR			RTT_PARK		
35	RFU		RTT_NOM_RD			RTT_NOM_WR		
36	RFU					RTT_Loopback		
37	RFU		ODTLoff_WR_offset			ODTLon_WR_offset		
38	RFU		ODTLoff_WR_NT_offset			ODTLon_WR_NT_offset		
39	RFU		ODTLoff_RD_NT_offset			ODTLon_RD_NT_offset		
40	RFU					Read DQS Offset Timing		
41	RFU							
42	DCA Training Assist Mode II (optional)				DCA Training Assist Mode I		DCA Types Supported	
43	Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clocks			Sign Bit for OP[2:0]	DCA for single/two-phase clock(s) or QCKL in 4-phase clocks		
44	RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		
45	DQS Interval Timer Run Time							
46	DQS Oscillator Count – LSB							
47	DQS Oscillator Count – MSB							
48	Write Pattern Mode							
49	RFU							

Table 20: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
50	RFU		Write CRC Auto-Disable Status	Write CRC Auto-Disable Enable	Write CRC Error Status	Write CRC Enable Upper Nibble	Write CRC Enable	Read CRC Enable
51	RFU	Write CRC Auto-Disable Threshold						
52	RFU	Write CRC Auto-Disable Window						
53	Loopback Output Mode	Loopback Select Phase		Loopback Output Select				
54	hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0
55	hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0
56	hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0
57	hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0
58	RAAMMT[2:0]			RAAIMT[3:0]				RFM Required
59	RFM RAA Counter		ARFM		BRC Support Level	Bounded Refresh Configuration		DRFM Enable
60	PASR Segment Mask							
61	Reserved			Package Output Driver Test Mode				
62	Vendor Specified							
63	DRAM Scratch Pad							
64	Reserved for Paging Pointer							
65	Serial Number 1							
66	Serial Number 2							
67	Serial Number 3							
68	Serial Number 4							
69	Serial Number 5							
70	ALERT_n Verification	ALERT_n Verification Support (optional)	ABO Flag	RFU	ACT Counter Initialization Complete	ACT Counter Initialization	PRAC and ABO Enable/Disable	PRAC and ABO Support (optional)
71	RFU	PRAC Testing Initialization	PRAC Testing Enable/Disable	PRAC Testing Support (optional)	Adaptive PRAC		ABO_RFM and ABO_Delay	
72	RFU						Counter Address Report Flag	Counter RAS Event Flag
73	Activation Counter Error Row Address R[7:0]							

Table 20: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
74	Activation Counter Error Row Address R[15:8]							
75	RFU	Activation Counter Error Row Bank Group BG[2:0]			Activation Counter Error Row Bank Address BA[1:0]		Activation Counter Error Row Address R[17:16]	
76-102	RFU							
103	DQSL_t IBCLK Sign	RFU	DQSL_t DCA for IBCLK		DQSL_t QCLK Sign	RFU	DQSL_t DCA for QCLK	
104	RFU				DQSL_t QBCLK Sign	RFU	DQSL_t DCA for QBCLK	
105	DQSL_c IBCLK Sign	RFU	DQSL_c DCA for IBCLK		DQSL_c QCLK Sign	RFU	DQSL_c DCA for QCLK	
106	RFU				DQSL_c QBCLK Sign	RFU	DQSL_c DCA for QBCLK	
107	DQSU_t IBCLK Sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK Sign	RFU	DQSU_t DCA for QCLK	
108	RFU				DQSU_t QBCLK Sign	RFU	DQSU_t DCA for QBCLK	
109	DQSU_c IBCLK Sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK Sign	RFU	DQSU_c DCA for QCLK	
110	RFU				DQSU_c QBCLK Sign	RFU	DQSU_c DCA for QBCLK	
111	RFU			Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE Gain Enable
112	RFU				DML DFE Gain Bias			
113	DML DFE Tap-1 Bias							
114	DML DFE Tap-2 Bias							
115	DML DFE Tap-3 Bias							
116	DML DFE Tap-4 Bias							
117	RFU							
118	DML V _{REFDQ} Sign	DML V _{REFDQ} Offset			RFU			
119	RFU							
120	RFU				DMU DFE Gain Bias			
121	DMU DFE Tap-1 Bias							
122	DMU DFE Tap-2 Bias							
123	DMU DFE Tap-3 Bias							
124	DMU DFE Tap-4 Bias							
125	RFU							
126	DMU V _{REFDQ} Sign	DMU V _{REFDQ} Offset			RFU			
127	RFU							
128	RFU				DQL0 DFE Gain Bias			
129	DQL0 DFE Tap-1 Bias							
130	DQL0 DFE Tap-2 Bias							

Table 20: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
131	DQL0 DFE Tap-3 Bias							
132	DQL0 DFE Tap-4 Bias							
133	DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK		DQL0 QCLK Sign	RFU	DQL0 DCA for QCLK	
134	DQL0 V _{REFDQ} Sign	DQL0 V _{REFDQ} Offset			DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK	
135	RFU							
136	RFU				DQL1 DFE Gain Bias			
137	DQL1 DFE Tap-1 Bias							
138	DQL1 DFE Tap-2 Bias							
139	DQL1 DFE Tap-3 Bias							
140	DQL1 DFE Tap-4 Bias							
141	DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK		DQL1 QCLK Sign	RFU	DQL1 DCA for QCLK	
142	DQL1 V _{REFDQ} Sign	DQL1 V _{REFDQ} Offset			DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK	
143	RFU							
144	RFU				DQL2 DFE Gain Bias			
145	DQL2 DFE Tap-1 Bias							
146	DQL2 DFE Tap-2 Bias							
147	DQL2 DFE Tap-3 Bias							
148	DQL2 DFE Tap-4 Bias							
149	DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK		DQL2 QCLK Sign	RFU	DQL2 DCA for QCLK	
150	DQL2 V _{REFDQ} Sign	DQL2 V _{REFDQ} Offset			DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK	
151	RFU							
152	RFU				DQL3 DFE Gain Bias			
153	DQL3 DFE Tap-1 Bias							
154	DQL3 DFE Tap-2 Bias							
155	DQL3 DFE Tap-3 Bias							
156	DQL3 DFE Tap-4 Bias							
157	DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK		DQL3 QCLK Sign	RFU	DQL3 DCA for QCLK	
158	DQL3 V _{REFDQ} Sign	DQL3 V _{REFDQ} Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	
159	RFU							
160	RFU				DQL4 DFE Gain Bias			
161	DQL4 DFE Tap-1 Bias							
162	DQL4 DFE Tap-2 Bias							
163	DQL4 DFE Tap-3 Bias							
164	DQL4 DFE Tap-4 Bias							

Table 20: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
165	DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK		DQL4 QCLK Sign	RFU	DQL4 DCA for QCLK	
166	DQL4 V _{REFDQ} Sign	DQL4 V _{REFDQ} Offset			DQL4 QBCLK Sign	RFU	DQL4 DCA for QBCLK	
167	RFU							
168	RFU				DQL5 DFE Gain Bias			
169	DQL5 DFE Tap-1 Bias							
170	DQL5 DFE Tap-2 Bias							
171	DQL5 DFE Tap-3 Bias							
172	DQL5 DFE Tap-4 Bias							
173	DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK		DQL5 QCLK Sign	RFU	DQL5 DCA for QCLK	
174	DQL5 V _{REFDQ} Sign	DQL5 V _{REFDQ} Offset			DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK	
175	RFU							
176	RFU				DQL6 DFE Gain Bias			
177	DQL6 DFE Tap-1 Bias							
178	DQL6 DFE Tap-2 Bias							
179	DQL6 DFE Tap-3 Bias							
180	DQL6 DFE Tap-4 Bias							
181	DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL6 QCLK Sign	RFU	DQL6 DCA for QCLK	
182	DQL6 V _{REFDQ} Sign	DQL6 V _{REFDQ} Offset			DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK	
183	RFU							
184	RFU				DQL7 DFE Gain Bias			
185	DQL7 DFE Tap-1 Bias							
186	DQL7 DFE Tap-2 Bias							
187	DQL7 DFE Tap-3 Bias							
188	DQL7 DFE Tap-4 Bias							
189	DQL7 IBCLK Sign	RFU	DQL7 DCA for IBCLK		DQL7 QCLK Sign	RFU	DQL7 DCA for QCLK	
190	DQL7 V _{REFDQ} Sign	DQL7 V _{REFDQ} Offset			DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK	
191	RFU							
192	RFU				DQU0 DFE Gain Bias			
193	DQU0 DFE Tap-1 Bias							
194	DQU0 DFE Tap-2 Bias							
195	DQU0 DFE Tap-3 Bias							
196	DQU0 DFE Tap-4 Bias							
197	DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK		DQU0 QCLK Sign	RFU	DQU0 DCA for QCLK	

Table 20: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
198	DQU0 V _{REFDQ} Sign	DQU0 V _{REFDQ} Offset			DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK	
199	RFU							
200	RFU				DQU1 DFE Gain Bias			
201	DQU1 DFE Tap-1 Bias							
202	DQU1 DFE Tap-2 Bias							
203	DQU1 DFE Tap-3 Bias							
204	DQU1 DFE Tap-4 Bias							
205	DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK		DQU1 QCLK Sign	RFU	DQU1 DCA for QCLK	
206	DQU1 V _{REFDQ} Sign	DQU1 V _{REFDQ} Offset			DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK	
207	RFU							
208	RFU				DQU2 DFE Gain Bias			
209	DQU2 DFE Tap-1 Bias							
210	DQU2 DFE Tap-2 Bias							
211	DQU2 DFE Tap-3 Bias							
212	DQU2 DFE Tap-4 Bias							
213	DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK		DQU2 QCLK Sign	RFU	DQU2 DCA for QCLK	
214	DQU2 V _{REFDQ} Sign	DQU2 V _{REFDQ} Offset			DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK	
215	RFU							
216	RFU				DQU3 DFE Gain Bias			
217	DQU3 DFE Tap-1 Bias							
218	DQU3 DFE Tap-2 Bias							
219	DQU3 DFE Tap-3 Bias							
220	DQU3 DFE Tap-4 Bias							
221	DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK		DQU3 QCLK Sign	RFU	DQU3 DCA for QCLK	
222	DQU3 V _{REFDQ} Sign	DQU3 V _{REFDQ} Offset			DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK	
223	RFU							
224	RFU				DQU4 DFE Gain Bias			
225	DQU4 DFE Tap-1 Bias							
226	DQU4 DFE Tap-2 Bias							
227	DQU4 DFE Tap-3 Bias							
228	DQU4 DFE Tap-4 Bias							
229	DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK		DQU4 QCLK Sign	RFU	DQU4 DCA for QCLK	
230	DQU4 V _{REFDQ} Sign	DQU4 V _{REFDQ} Offset			DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK	
231	RFU							

Table 20: DDR5 Mode Register Assignments (Continued)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
232	RFU				DQU5 DFE Gain Bias			
233	DQU5 DFE Tap-1 Bias							
234	DQU5 DFE Tap-2 Bias							
235	DQU5 DFE Tap-3 Bias							
236	DQU5 DFE Tap-4 Bias							
237	DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK		DQU5 QCLK Sign	RFU	DQU5 DCA for QCLK	
238	DQU5 V _{REFDQ} Sign	DQU5 V _{REFDQ} Offset			DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK	
239	RFU							
240	RFU				DQU6 DFE Gain Bias			
241	DQU6 DFE Tap-1 Bias							
242	DQU6 DFE Tap-2 Bias							
243	DQU6 DFE Tap-3 Bias							
244	DQU6 DFE Tap-4 Bias							
245	DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK		DQU6 QCLK Sign	RFU	DQU6 DCA for QCLK	
246	DQU6 V _{REFDQ} Sign	DQU6 V _{REFDQ} Offset			DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK	
247	RFU							
248	RFU				DQU7 DFE Gain Bias			
249	DQU7 DFE Tap-1 Bias							
250	DQU7 DFE Tap-2 Bias							
251	DQU7 DFE Tap-3 Bias							
252	DQU7 DFE Tap-4 Bias							
253	DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK		DQU7 QCLK Sign	RFU	DQU7 DCA for QCLK	
254	DQU7 V _{REFDQ} Sign	DQU7 V _{REFDQ} Offset			DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK	
255	RFU							

MR0-MR31

MR0 Burst Length, CAS Latency

Table 21: MR0 Register and OP-Code Bit Definitions (MA[7:0] = 00h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CAS Latency (CL)						Burst Length	

Function	Type	OP	Description/Data	Notes
Burst Length	R/W	OP[1:0]	00b=BL16, 01b=BC8 OTF, 10b=BL32, 11b=BL32 OTF	
CAS Latency	R/W	OP[7:2]	000000b=22, 000001b=24, 000010b=26, 000011b=28, 000100b=30, 000101b=32, 000110b=34, 000111b=36, 001000b=38, 001001b=40, 001010b=42, 001011b=44, 001100b=46, 001101b=48, 001110b=50, 001111b=52, 010000b=54, 010001b=56, 010010b=58, 010011b=60, 010100b=62, 010101b=64, 010110b=66, 010111b=68, 011000b=70, 011001b=72, 011010b=74, 011011b=76, 011100b=78, 011101b=80, 011110b=82, 011111b=84, 100000b=86, 100001b=88, 100010b=90, 100011b=92, 100100b-111111b=RFU	1, 2

Notes: 1. Range covers both monolithic and 3DS devices up to 8800, plus margin for CRC latency adder of 2.
2. CWL = CL-2.

MR1 PDA Mode Details

Table 22: MR1 Register and OP-Code Bit Definitions (MA[7:0] = 01h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PDA Select ID				PDA Enumerate ID			

Function	Type	OP	Description/Data	Notes
PDA Enumerate ID	R	OP[3:0]	This is a read-only MR field, which is only programmed through an MPC command with the PDA enumerate ID opcode. xxxxb encoding is set with MPC command with the PDA enumerate ID opcode. This can only be set when PDA enumerate programming mode is enabled and the associated DRAM's DQ0 is asserted LOW. The PDA enumerate ID opcode includes 4 bits for this encoding. The default setting is 1111b.	
PDA Select ID	R	OP[7:4]	This is a read-only MR field, which is only programmed through an MPC command with the PDA select ID opcode. xxxxb encoding is set with MPC command with the PDA select ID opcode. The PDA select ID opcode includes 4 bits for this encoding. 1111b = all DRAMs execute MRW, MPC, VREFCA, and VREFCS commands. For all other encodings, DRAMs execute MRW, MPC, VREFCS, and VREFCA commands only if PDA select ID[3:0] = PDA enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA select ID. The default setting is 1111b.	

MR2 Functional Modes

Table 23: MR2 Register and OP-Code Bit Definitions (MA[7:0] = 02h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Internal Write Timing	Reserved	Device 15 MPSM	CS Assertion Duration (MPC)	Max Power Saving Mode (MPSM)	2N Mode	Write Leveling Training	Read Preamble Training

Function	Type	OP	Description/Data	Notes
Read Preamble Enable	R/W	OP[0]	0b=normal mode (default), 1b=read preamble training	
Write Leveling Training	R/W	OP[1]	0b=normal mode (default), 1b=write leveling	1,2,3
2N Mode	R	OP[2]	0b=2N mode (default), 1b=1N mode	4
Max Power Saving Mode (MPSM)	R/W	OP[3]	0b=disable (default), 1b=enable	
CS Assertion Duration (MPC)	R/W	OP[4]	0b=only multiple cycles of CS assertion available for MPC, VREFCA, and VREFCS commands (default), 1b=only a single cycle of CS assertion available for MPC, VREFCA, and VREFCS commands.	
Device 15 MPSM	R/W	OP[5]	0b=disable (default), 1b=enable	
Reserved	Reserved	OP[6]	Reserved	
Internal Write Timing	R/W	OP[7]	0b=disabled (default), 1b=enabled	5,6

- Notes: 1. To enter WL training mode, the MR field must be programmed to 1. WL training mode is used when internal write timing mode = 0 (external WL training) and when internal write timing mode = 1 (internal WL training).
2. To exit WL training mode, the MR field must be programmed to 0.
3. MRRs are not supported during write leveling.
4. This MR bit is programmed via an explicit MPC command only.
5. Internal write timing is disabled at the beginning of external write leveling mode and re-enabled at the start of write leveling internal cycle alignment. See the Write Leveling Training Mode section for details.
6. Device implementation may optionally have the same behavior when the internal Write timing mode is enabled instead of disabled. This means the CK and DQS timing paths remain matched internally. The WL internal cycle alignment mode setting must still support pulling the internal WL pulse earlier so that the same WL training flow produces the correct results.

MR3 Write Leveling Internal Cycle Alignment Settings

Table 24: MR3 Register and OP-Code Bit Definitions (MA[7:0] = 03h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Leveling Internal Cycle Alignment - Upper Byte				Write Leveling Internal Cycle Alignment - Lower Byte			

Function	Type	OP	Description/Data	Notes
Write Leveling Internal Cycle Alignment - Lower Byte	R/W	OP[3:0]	0000b=0 ^t CK (default) 0001b= -1 ^t CK 0010b= -2 ^t CK ... (optional opcodes: 0111b through 1111b) ^t CK; 1101b= -13 ^t CK 1110b= -14 ^t CK 1111b= -15 ^t CK	1,2,3,5

Function	Type	OP	Description/Data	Notes
Write Leveling Internal Cycle Alignment - Upper Byte	R/W	OP[7:4]	0000b=0 ^t CK (default) 0001b= -1 ^t CK 0010b= -2 ^t CK ... (optional opcodes: 0111b through 1111b) ^t CK; 1101b= -13 1110b= -14 ^t CK 1111b= -15 ^t CK	1,2,4,5

- Notes: 1. This is set during WL training, after the host DQS has been aligned to the ideal external WL timings. The internal write timing is enabled and the WL internal timing alignment is set to ensure the internal write enable aligns within ^tDQS2CK of the external WL trained location. When internal write timing is disabled, the WL internal cycle alignment setting does not change the behavior of the write timings.
2. Device implementation may optionally have the same behavior when the internal write timing is enabled instead of disabled. This would mean that the CK and DQS timing paths remain matched internally. The WL internal cycle alignment setting must still support pulling the internal WL pulse earlier so that the same WL training flow will produce the correct result.
3. Lower byte WL internal cycle alignment is intended for x4, x8 and x16 configurations.
4. Upper byte WL internal cycle alignment is intended for x16 configurations only. Although training of the lower and upper bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.
5. Optional opcodes (0111b-1111b) may be needed for certain speed bins.

MR4 Refresh Settings

Table 25: MR4 Register and OP-Code Bit Definitions (MA[7:0] = 04h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU	Wide Range (optional)	Refresh ^t RFC Mode	Refresh Interval Rate Indicator	Refresh Rate		

Function	Type	OP	Description/Data	Notes
Refresh Rate	R	OP[2:0]	If Wide Range is not supported (OP[5]=0): 000b=RFU; 001b= ^t REFI x1 (1x Ref Rate), <80°C nominal; 010b= ^t REFI x1 (1x Ref Rate), 80-85°C nominal; 011b= ^t REFI /2 (2x Ref Rate), 85-90°C nominal; 100b= ^t REFI /2 (2x Ref Rate), 90-95°C nominal; 101b= ^t REFI /2 (2x Ref Rate), >95°C nominal; 110b=RFU, 111b=RFU If Wide Range is supported (OP[5]=1): 000b= ^t REFI x1 (1x Ref Rate), <75°C nominal; 001b= ^t REFI x1 (1x Ref Rate), 75-80°C nominal; 010b= ^t REFI x1 (1x Ref Rate), 80-85°C nominal; 011b= ^t REFI /2 (2x Ref Rate), 85-90°C nominal; 100b= ^t REFI /2 (2x Ref Rate), 90-95°C nominal; 101b= ^t REFI /2 (2x Ref Rate), 95-100°C nominal; 110b= ^t REFI /2 (2x Ref Rate), >100°C nominal; 111b=RFU	1,2,3,4,5, 6,7,8
Refresh Interval Rate Indicator	SR/W	OP[3]	DRAM status read (SR): 0=not implemented, 1=implemented Host write (W): 0b=disabled (default); 1b=enabled	
Refresh ^t RFC Mode	R/W	OP[4]	0b=normal (^t RFC1); 1b=fine granularity refresh mode (^t RFC2)	
Wide Range (optional)	R	OP[5]	0b=wide range is not supported; 1b=wide range is supported	8
RFU	RFU	RFU	RFU	
TUF (Temperature Update Flag)	R	OP[7]	0b=no change in OP[2:0] since last MR4 read (default); 1b=change in OP[2:0] since last MR4 read	

- Notes: 1. The minimum required refresh rate for each OP[2:0] setting applies to t_{REFI1} and t_{REFI2} . OP[2:0] settings specify a nominal temperature range. The ranges defined by OP[2:0] are determined by temperature thresholds used by the system for proper operation.
2. When OP[5]=0, the four temperature thresholds are nominally at 80°C, 85°C, 90°C and 95°C. The <80°C threshold has no minimum value specified and the >95°C threshold has no maximum temperature value specified. When OP[5]=1, the six temperature thresholds are nominally at 75°C, 80°C, 85°C, 90°C, 95°C, and 100°C. The <75°C threshold has no minimum value specified and the >100°C threshold has no maximum temperature value specified.
3. DRAM vendors report all possible settings over the operating temperature range of the device. Each vendor guarantees their device will work at any temperature within the range when the system refresh interval follows these guidelines:
- Threshold $\leq 85^{\circ}\text{C}$ $t_{REFI} \times 1$ (1x Ref Rate) or faster may be used
 - Threshold $> 85^{\circ}\text{C}$ $t_{REFI}/2$ (2x Ref Rate) or faster is required
4. The 2X refresh rate must be provided by the system before the device T_j has gone up by more than 2°C (temperature margin) since the first report out of OP[2:0]=011b. This condition is reset when OP[2:0] is equal to 010b.
5. The device may not operate properly when OP[2:0]=101b, if T_j has gone up by more than 2°C (temperature margin) since the first report out of OP[2:0]=101b. This condition is reset when OP[2:0] is equal to 100b. OP[2:0]=101b must be a temporary condition of the device, to be addressed by immediately reducing the T_j of the device by throttling its power, and/or the power of nearby devices.
6. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence (Te).
7. See the Temperature Sensor section for information on the recommended frequency of reading MR4.
8. Support for wide range temperature sensing does not indicate the device may operate properly at temperature ranges above 95°C. Side effects may include loss of data integrity.
9. OP[3] for optional functionality; RFU is not supported by the device.

MR5 I/O Settings

Table 26: MR5 Register and OP-Code Bit Definitions (MA[7:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Pull-down Output Driver Impedance		DM Enable	TDQS Enable	Package Output Driver Test Mode Supported	Pull-up Output Driver Impedance		Data Output Disable

Function	Type	OP	Description/Data	Notes
Data Output Disable	W	OP[0]	0b=normal (default), 1b=outputs disabled	
Pull-up Output Driver Impedance	R/W	OP[2:1]	00b=RZQ/7 (34 ohm), 01b= RZQ/6 (40 ohm), 10b=RZQ/5 (48 ohm), 11b=RFU	
Package Output Driver Test Mode Supported	R	OP[3]	0b=function not supported, 1b=function supported	
TDQS Enable	R/W	OP[4]	0b=disable (default), 1b=enable	
DM Enable	R/W	OP[5]	0b=disable (default), 1b=enable	
Pull-down Output Driver Impedance	R/W	OP[7:6]	00b=RZQ/7 (34 ohm), 01b=RZQ/6 (40 ohm), 10b=RZQ/5 (48 ohm), 11b=RFU	

MR6 Write Recovery Time (t_{WR}) and Read to Precharge Time (t_{RTP})

Table 27: MR6 Register and OP-Code Bit Definitions (MA[7:0] = 06h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read to Precharge Time (t_{RTP})				Write Recovery Time (t_{WR})			

Function	Type	OP	Description/Data	Notes
Write Recovery Time (t_{WR}) Legacy / PRAC	R/W	OP[3:0]	0000b=48CK (Legacy) / 16CK (PRAC), 001b=54CK (Legacy) / 18CK (PRAC), 0010b=60CK (Legacy) / 20CK (PRAC), 0011b=66CK (Legacy) / 22CK (PRAC), 0100b=72CK (Legacy) / 24CK (PRAC), 0101b=78CK (Legacy) / 26CK (PRAC), 0110b=84CK (Legacy) / 28CK (PRAC), 0111b=90CK (Legacy) / 30CK (PRAC), 1000b=96CK (Legacy) / 32CK (PRAC), 1001b=102CK (Legacy) / 34CK (PRAC), 1010b=108CK (Legacy) / 36CK (PRAC), 1011b=114CK (Legacy) / 38CK (PRAC), 1100b=120CK (Legacy) / 40CK (PRAC), 1101b=126CK (Legacy) / 42CK (PRAC), 1110b=132CK (Legacy) / 44CK (PRAC), 1111b = RFU	1
Read to Precharge Time (t_{WR}) Legacy / PRAC	R/W	OP[7:4]	0000b=12CK (Legacy) / 8CK (PRAC), 0001b=14CK (Legacy) / 9CK (PRAC), 0010b=15CK (Legacy) / 10CK (PRAC), 0011b=17CK (Legacy) / 11CK (PRAC), 0100b=18CK (Legacy) / 12CK (PRAC), 0101b=20CK (Legacy) / 13CK (PRAC), 0110b=21CK (Legacy) / 14CK (PRAC), 0111b=23CK (Legacy) / 15CK (PRAC), 1000b=24CK (Legacy) / 16CK (PRAC), 1001b=26CK (Legacy) / 17CK (PRAC), 1010b=27CK (Legacy) / 18CK (PRAC), 1011b=29CK (Legacy) / 19CK (PRAC), 1100b=30CK (Legacy) / 20CK (PRAC), 1101b=32CK (Legacy) / 21CK (PRAC), 1110b=33CK (Legacy) / 22CK (PRAC), 1111b=RFU	2

- Notes: 1. t_{WR} (MIN) is defined in the Timing By Speed Bin tables. The host must operate with MR settings resulting in t_{CK} * MR6:OP [3:0] $\geq t_{WR}$ (MIN).
2. t_{RTP} (MIN) is defined in the Timing By Speed Bin tables. The host must operate with MR settings resulting in t_{CK} * MR6:OP [7:4] $\geq t_{RTP}$ (MIN).
3. All nCK conversions require rounding algorithm considerations.

MR7 RFU

Table 28: MR7 Register and OP-Code Bit Definitions (MA[7:0] = 07h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU						Write Leveling Internal Upper Byte (optional)	Write Leveling Internal Lower Byte (optional)

Function	Type	OP	Description/Data	Notes
(Optional) Write Leveling Internal + 0.5 t_{CK} Alignment Offset - Lower Byte	R/W	0	0b: disabled (default); 1b: 0.5 t_{CK}	1,2,4

Function	Type	OP	Description/Data	Notes
(Optional) Write Leveling Internal + 0.5 ^t CK Alignment Offset - Upper Byte	R/W	1	0b: disabled (default); 1b: 0.5 ^t CK	1,3,4
RFU	RFU	OP[7:0]	RFU	

- Notes: 1. The WICA 0.5 ^tCK offset is a positive adjustment to the target WICA value. (Example: MR3:OP[3:0] = -3 ^tCK (0011b) and MR7:OP[0] = 1, WICA + WICAhalfCycle = -3 ^tCK + 0.5 ^tCK = -2.5 ^tCK)
2. Lower byte WL internal cycle alignment is intended for x4, x8, and x16 configurations.
3. Upper byte WL internal cycle alignment is intended for x16 configuration only. Although training of the lower and upper bytes is independent, contact the DRAM vendor regarding recommendations for setting the WICA values to the same offset.
4. When operating at 1980-2100 MT/s (CL=22), the host must not apply the WICA 0.5^tCK offset.

MR8 Preamble/Postamble

Table 29: MR8 Register and OP-Code Bit Definitions (MA[7:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Postamble Settings	Read Postamble Settings	RFU	Write Preamble Settings		Read Preamble Settings		

Function	Type	OP	Description/Data	Notes
Read Preamble Settings	R/W	OP[2:0]	000b=1 ^t CK - 10 pattern, 001b=2 ^t CK - 0010 pattern, 010b=2 ^t CK - 1110 pattern, 011b=3 ^t CK - 000010 pattern, 100b=4 ^t CK - 00001010 pattern, all other encodings RFU	1
Write Preamble Settings	R/W	OP[4:3]	00b=reserved, 01b=2 ^t CK - 0010 pattern (default), 10b=3 ^t CK - 000010 pattern, 11b=4 ^t CK - 00001010 pattern	
RFU	RFU	RFU	RFU	
Read Postamble Settings	R/W	OP[6]	0b=0.5 ^t CK - 0 pattern, 1b=1.5 ^t CK - 010 pattern	
Write Postamble Settings	R/W	OP[7]	0b=0.5 ^t CK - 0 pattern, 1b=1.5 ^t CK - 000 pattern	

Note: 1. Refer to the Preamble section for details on read preamble modes and patterns.

MR9 Test Mode Enable

Table 30: MR9 Register and OP-Code Bit Definitions (MA[7:0] = 09h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Test Mode (TM)	RFU						

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[6:0]	RFU	
Test Mode (TM)	W	OP[7]	0b=normal (default), 1b=test mode	1

MR10 V_{refDQ} Calibration Settings

Table 31: MR10 Register and OP-Code Bit Definitions (MA[7:0] = 0Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
V _{refDQ} Cal Settings							

Function	Type	OP	Description/Data	Notes
V _{refDQ} Cal Value	R/W	OP[7:0]	0000 0000b = 97.5% 0000 0001b = 97.0%... 0111 1100b = 35.5% 0111 1101b = 35.0% All other encodings RFU	

Note: 1. Default setting 00101101b (75% of V_{DDQ}).

MR11 V_{refCA} Calibration Settings (Read-Only)

Table 32: MR11 Register and OP-Code Bit Definitions (MA[7:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid	V _{refCA} Calibration Settings (read-only)						

Function	Type	OP	Description/Data	Notes
V _{refCA} Cal Value	R	OP[6:0]	000 0000b = 97.5% 000 0001b = 97.0%... 111 1100b = 35.5% 111 1101b = 35.0% All other encodings RFU	1,2,3
Valid	R	OP[7]	Valid (V)	

Notes: 1. Default setting 0101101b (75% of V_{DDQ}).

- Because V_{REFCA} calibration setting has an explicit command (VREFCA command), it can only be programmed via that command; and therefore, its mode register is read-only.
- Because the state of CA12 is used to differentiate the VREFCA vs. VREFCS command, VREFCA OP[7] should always be equal to 0; the MR11/12 OP[7] value is defined as valid.

MR12 V_{refCS} Calibration Settings (Read-Only)

Table 33: MR12 Register and OP-Code Bit Definitions (MA[7:0] = 0Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid	V _{refCS} Calibration Settings (read-only)						

Function	Type	OP	Description/Data	Notes
V _{refCS} Cal Value	R	OP[6:0]	000 0000b = 97.5% 000 0001b = 97.0%... 111 1100b = 35.5% 111 1101b = 35.0% All other encodings RFU	1,2,3
Valid	R	OP[7]	Valid (V)	

Notes: 1. Default setting 0101101b (75% of V_{DDQ}).

- Because V_{REFCS} calibration setting has an explicit command (VREFCS command), it can only be programmed via that command; and therefore, its mode register is read-only.
- Because the state of CA12 is used to differentiate the VREFCA vs. VREFCS command, VREFCA OP[7] should always be equal to 0; the MR11/12 OP[7] value is defined as valid.

MR13 CS Geardown/ t_{CCD_L} / $t_{CCD\_L\_WR}$ / $t_{CCD\_L\_WR2}$ / t_{DLLK}

Table 34: MR13 Register and OP-Code Bit Definitions (MA[7:0] = 0Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		SRX/NOP Clock-Sync Support and Enable/ Disable at next SRX (Optional) ⁴	CS Geardown enable/ disable at next SREF	t_{CCD_L} / $t_{CCD\_L\_WR}$ / $t_{CCD\_L\_WR2}$ / t_{DLLK}			

Function	Type	OP	Description/Data	Notes
t_{CCD_L} $t_{CCD\_L\_WR}$ $t_{CCD\_L\_WR2}$ t_{DLLK}	R	OP[3:0]	See table below	1, 2, 3
CS geardown enable/ disable at next SREF	R/W	OP[4]	0b: CS geardown is disabled at next SREF (default) 1b: CS geardown is enabled at next SRE	
SRX/NOP Clock-Sync Support and Enable/ Disable at next SRX (Optional) ⁴	SR/W	OP[5]	DRAM Status Read (SR): 0b=SRX/NOP clock-sync not supported 1b=SRX/NOP clock-sync supported Host Write (W): 0b=Disable SRX/NOP clock-sync (default) 1b=Enable SRX/NOP clock-sync	4
RFU	RFU	OP[7:6]	RFU	

- Notes: 1. The t_{CCD_L} / $t_{CCD\_L\_WR}$ / $t_{CCD\_L\_WR2}$ / t_{DLLK} should be programmed according to the value defined in the AC parametric table per operating frequency.
2. The register type is R (read only) because MR13 is set by the CONFIGURE t_{DLLK} / $t_{CCD\_L\_WR}$ / $t_{CCD\_L\_WR2}$ / t_{CCD_L} MPC command.
3. Data rate ranges align with Speed Bin Table definitions.
4. If needed, the host shall program MR13:OP[5]=1 via MRW command to enable/disable the SRX/NOP Clock-Sync feature at the next SRX. During the next self refresh, the DRAM will automatically apply the update to the function.

MR13 OP[3:0]	t_{CCD_L} MIN (nCK) $t_{CCD\_L\_WR}$ MIN (nCK) $t_{CCD\_L\_WR2}$ MIN (nCK)	t_{DDLK} MIN (nCK)	Details
0000	8, 16, 32	1024	1980 MT/s ≤ data rate ≤ 2100 MT/s and 2933 MT/s ≤ data rate ≤ 3200 MT/s
0001	9, 18, 36	1024	3200 MT/s < data rate ≤ 3600 MT/s
0010	10, 20, 40	1280	3600 MT/s < data rate ≤ 4000 MT/s
0011	11, 22, 44	1280	4000 MT/s < data rate ≤ 4400 MT/s
0100	12, 24, 48	1536	4400 MT/s < data rate ≤ 4800 MT/s
0101	13, 26, 52	1536	4800 MT/s < data rate ≤ 5200 MT/s
0110	14, 28, 56	1792	5200 MT/s < data rate ≤ 5600 MT/s
0111	15, 30, 60	1792	5600 MT/s < data rate ≤ 6000 MT/s
1000	16, 32, 64	2048	6000 MT/s < data rate ≤ 6400 MT/s
1001	17, 34, 68	2048	6400MT/s ≤ Data Rate ≤ 6800MT/s
1010	18, 36, 72	2304	6800MT/s ≤ Data Rate ≤ 7200MT/s

MR13 OP[3:0]	$t_{CCD\_L\ MIN} (nCK)$ $t_{CCD\_L\_WR\ MIN} (nCK)$ $t_{CCD\_L\_WR2\ MIN} (nCK)$	$t_{DDLK\ MIN} (nCK)$	Details
1011	19, 38, 76	2304	7200MT/s ≤ Data Rate ≤ 7600MT/s
1100	20, 40, 80	2560	7600MT/s ≤ Data Rate ≤ 8000MT/s
1101	21, 42, 84	2560	8000MT/s ≤ Data Rate ≤ 8400MT/s
1110	22, 44, 88	2816	8400MT/s ≤ Data Rate ≤ 8800MT/s
1111	Reserved		

MR14 Transparency — Error Check Scrub (ECS) Configuration

Table 35: MR14 Register and OP-Code Bit Definitions (MA[7:0] = 0Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ECS Mode	ECS Reset Counters	Row Mode/Code Word Mode	RFU	ECS Error Register Index/MBIST Rank Select			

Function	Type	OP	Description/Data	Notes
ECS Error Register Index/MBIST Rank Select	R/W	OP[3:0]	CID[3:0]	1,2,3,4
RFU	RFU	OP[4]	RFU	
Row Mode/Code Word Mode	R/W	OP[5]	0b=ECS counts rows with errors, 1b=ECS counts code words with errors	1
ECS Reset Counters	W	OP[6]	0b=normal (default), 1b=reset ECS counters	1,4
ECS Mode	R/W	OP[7]	0b=automatic ECS mode (default), 1b=manual ECS mode	1,4

- Notes: 1. OP[3:0] must be set by MRW to indicate which slice in the 3DS stack is referenced by the MRR for MR14–MR20 ECS transparency data, MR22 MBIST transparency data, and MR54–MR57 hPPR resource availability. On 3DS devices that support optional MBIST/mPPR prior to MBIST initialization via MR23:OP[4] followed by guard keys, MR14:OP[3:0] must be programmed by MRW according to the logical rank that is desired to perform MBIST.
2. CID[3:0] encoding is based on the stack height of the device and varies depending on the number of dice in the stack.
3. For monolithic devices, CID[3:0] should be set to 0.
4. ECS stands for Error Check and Scrub operation.

MR15 Transparency — Transparency ECS Threshold and Automatic ECS in Self Refresh

Table 36: MR15 Register and OP-Code Bit Definitions (MA[7:0] = 0Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
x4 Writes	ECS Writeback	RFU		Automatic ECS in Self Refresh	ECS Error Threshold Count		

Function	Type	OP	Description/Data	Notes
ECS Error Threshold Count (ETC)	R/W	OP[2:0]	000b=RFU, 001b=RFU, 010b=RFU, 011b=256 (default), 100b=1024, 101b=4096, 110–111b=RFU	1
Automatic ECS in Self Refresh	W	OP[3]	0b=automatic ECS disabled in self refresh in manual ECS mode (default); 1b=automatic ECS enabled in self refresh in manual ECS mode	2,3
RFU	RFU	OP[5:4]	RFU	

Function	Type	OP	Description/Data	Notes
ECS Writeback	R/W	OP[6]	0b=do not suppress writeback of data and ECC check bits (default); 1b=suppress writeback of data and ECC check bits (optional)	4
x4 Writes	R/W	OP[7]	0b=do not suppress writeback of data during RMW (default); 1b=suppress writeback of data during RMW (optional)	4

- Notes: 1. MR15 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.
2. The device performs automatic ECS operation while in self refresh mode by either enabling MR15 OP[3]=1b (automatic ECS in self refresh enable) or disabling MR14 OP[7]=0b (automatic ECS mode enable).
3. If automatic ECS in self refresh is enabled, updated transparency mode registers cannot be controlled by the number of manual ECS operation MPC commands since the ECS counter is increased by both the manual ECS command and the auto ECS operation in self refresh mode.
4. DDR5 SPD byte 14 bits [2:1] indicate if feature is supported; also indicates that the device uses MR15 for enabling the modes.

MR16 Address of Row with Max Errors 1

Table 37: MR16 Register and OP-Code Bit Definitions (MA[7:0] = 10h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Transparency - Address of Row with Max Errors 1							

Function	Type	OP	Description/Data	Notes
Max Row Error Address R[7:0]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count.	1

- Note: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR17 Address of Row with Max Errors 2

Table 38: MR17 Register and OP-Code Bit Definitions (MA[7:0] = 11h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Transparency - Address of Row with Max Errors 2							

Function	Type	OP	Description/Data	Notes
Max Row Error Address R[15:8]	R	OP[7:0]	Contains 8 bits of the row address with the highest error count.	

- Note: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR18 Address of Row with Max Errors 3

Table 39: MR18 Register and OP-Code Bit Definitions (MA[7:0] = 12h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Transparency - Address of Row with Max Errors 3						

Function	Type	OP	Description/Data	Notes
Max Row Error Address BG[2:0],BA[1:0],R[17,16]	R	OP[6:0]	Contains 7 bits of the row address with the highest error count.	1,2,3,4,5
RFU	RFU	OP[7]	RFU	

Notes: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.
 2. BG2 is don't care for x16.
 3. BA1 is don't care for 8Gb.
 4. R16 is don't care for 8Gb and 16Gb.
 5. R17 is don't care for 8Gb, 16Gb, 24Gb, and 32Gb.

MR19 Max Row Errors/PASR

Table 40: MR19 Register and OP-Code Bit Definitions (MA[7:0] = 13h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR	RFU	Transparency - Max Row Error Count (REC)					

Function	Type	OP	Description/Data	Notes
Max Row Error Count (REC)	R	OP[5:0]	Contains number of errors within the row with the most errors.	1
RFU	RFU	OP[6]	RFU	
PASR	R	OP[7]	0b=PASR not supported; 1b=PASR supported	2

Notes: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.
 2. Support of PASR has been deprecated.

MR20 Error Count

Table 41: MR20 Register and OP-Code Bit Definitions (MA[7:0] = 14h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Error Count (EC) bits 7 to 0							

Function	Type	OP	Description/Data	Notes
Error Count (EC) bits 7 to 0	R	OP[7:0]	Contains the error count range data.	1

Note: 1. MR14 OP[3:0] applies to CID[3:0] for 3DS and must be set to indicate in which slice in the 3DS stack the transparency data resides for MR14 through MR20.

MR21 RFU Rx CTLE Control Setting (DQS)

Table 42: MR21 Register and OP-Code Bit Definitions (MA[7:0] = 15h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					Rx DQS CTLE Control(optional)		

Function	Type	OP	Description/Data	Notes
Rx DQS CTLE Control (optional)	W	OP[2:0]	000b: Vendor-optimized setting (default), 001b: Vendor-defined, 010b: Vendor-defined, 011b: Vendor-defined, 100b: Vendor-defined, 101b: Vendor-defined, 110b: Vendor-defined, 111b: Vendor-defined	1.2.3.4
RFU	RFU	OP[7:3]	RFU	

Notes: 1. Rx CTLE is an optional feature on DDR5. It may be needed for DRAMs that operate at ≥6000 Mb/s; MR22:OP[3] indicates host whether or not Rx CTLE is supported.
 2. Because CTLE circuits cannot be typically bypassed, a disable option is not provided. Instead, a vendor-optimized setting is given. It should be noted that the settings are not specifically linear in relationship to the vendor-optimized setting; therefore, the host may opt to instead walk through all provided options and use the setting that works best in their environment.

3. The host can step through all possible combinations of MR bit allocation and choose the settings that are best optimized for the system based on the performance metric of interest.
4. MR21:OP[2:0] controls both upper and lower DQS (U/LDQS) for x16 DRAMs.

MR22 MBIST/mPPR Transparency (Optional), Rx CTLE Control Setting (Support Indicator, CA, and CS_n)

Table 43: MR22 Register and OP-Code Bit Definitions (MA[7:0] = 16h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Rx CS_n CTLE Control (Optional)		Rx CA CTLE Control (Optional)		Rx CTLE Support	MBIST/mPPR Transparency (optional)		

Function	Type	OP	Description/Data	Notes
MBIST/mPPR Transparency (optional)	R	OP[2:0]	000b: MBIST has not run since INIT or no fails remain after most recent run (default); 001b = Fails remain; 010b = Unrepairable fails remain; 011b = MBIST should be run again; 100b-111b = Reserved	1,2
Rx CTLE Support	R	OP[3]	0: Rx CTLE not supported; 1: Rx CTLE supported	3
Rx CA CTLE Control (optional)	R/W	OP[5:4]	00: Vendor-optimized setting (default); 01: Vendor-defined; 10: Vendor-defined; 11: Vendor-defined	3,4,5
Rx CS_n CTLE Control(optional)	R/W	OP[7:6]	00B: Vendor-optimized setting (default); 01: Vendor-defined; 10B: Vendor-defined; 11: Vendor defined	3,4,5

- Notes: 1. The host should track whether or not MBIST has run since INIT. If MBIST runs and no fails are found, this transparency state remains set to 000.
2. MR14:OP[3:0] must be programmed by MRW to indicate which slice in the 3DS-DDR5 stack is referenced by the MRR for reading MR22 MBIST transparency data.
3. Rx CTLE is an optional feature on DDR5. It may be needed for DRAMs that operate at ≥ 6000 Mbps. MR22:OP[3] indicates to the host whether or not Rx CTLE is supported.
4. Because CTLE circuits cannot be typically bypassed, a disable option is not provided. Instead, a vendor-optimized setting is given. It should be noted that the settings are not specifically linear in relationship to the vendor optimized setting, so the host may opt instead to walk through all provided options and use the setting that works best in their environment.
5. The host can step through all possible combinations of MR bit allocation and choose the settings that are best optimized for the system based on the performance metric of interest.

MR23 MBIST/PPR Settings

Table 44: MR23 Register and OP-Code Bit Definitions (MA[7:0] = 17h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			MBIST	mPPR	sPPR		hPPR

Function	Type	OP	Description/Data	Notes
hPPR	R/W	OP[0]	0=disable, 1=enable	1
sPPR	R/W	OP[1]	0=disable, 1=enable (see OP[2] definition with sPPR Undo/Lock implemented)	
	SR/W	OP[2]	DRAM Status Read (SR): 0b=not implemented; 1b=sPPR undo/lock implemented Host Write (W) for OP[2:1]: 00b=disabled (normal operation); 01b=sPPR enabled; 10b=sPPR undo enabled; 11b=sPPR lock enabled	1
mPPR	W	OP[3]	0=disable; 1=enable (optional)	1

Function	Type	OP	Description/Data	Notes
MBIST	SR/W	OP[4]	DRAM Status Read (SR): 0b=no MBIST/mPPR support; 1b=supports MBIST/mPPR (optional) Host Write: 0b=MBIST disabled; 1b=MBIST enabled	1,2,3
RFU	RFU	OP[7:5]	RFU	

- Notes: 1. Only one of these op-code bits may be programmed by the host to 1 at any given time. If any one of these op-code bits are enabled, the remaining bits must be programmed to 0.
2. The device automatically writes to 0 when MBIST completes; therefore, the host is not required to program to 0 before performing MBIST again.
3. For 3DS-DDR5 devices, MBIST Enable (MR23:OP[4]=1) is only enabled on the target logical rank designated by CID[3:0] and programmed by MRW via MR14:OP[3:0].

MR24 PPR Guard Key

Table 45: MR24 Register and OP-Code Bit Definitions (MA[7:0] = 18h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PPR Guard Key							

Function	Type	OP	Description/Data	Notes
PPR Guard Key	W	OP[7:0]	See the Post Package Repair (PPR) section for sequence	

MR25 Read Training Mode

Table 46: MR25 Register and OP-Code Bit Definitions (MA[7:0] = 19h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Continuous Burst Mode	LFSR1 Pattern Option	LFSR0 Pattern Option	Read Training Pattern Format

Function	Type	OP	Description/Data	Notes
Read Training Pattern Format	R/W	OP[0]	0b=serial, 1b=LFSR	
LFSR0 Pattern Option	R/W	OP[1]	0b=LFSR, 1b=clock	
LFSR1 Pattern Option	R/W	OP[2]	0b=LFSR, 1b=clock	
Continuous Burst Mode	R/W	OP[3]	0b=MRR command-based (default), 1b=continuous burst option	
RFU	RFU	OP[7:4]	RFU	

MR26 Read Training Pattern Data0/LFSR0 Seed

Table 47: MR26 Register and OP-Code Bit Definitions (MA[7:0] = 1Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Data0/LFSR0 Seed							

Function	Type	OP	Description/Data	Notes
Read Pattern/LFSR Seed UI0	R/W	OP[0]	UI<7:0> data for serial mode, LFSR0 seed for LFSR mode	1
Read Pattern/LFSR Seed UI1	R/W	OP[1]		
Read Pattern/LFSR Seed UI2	R/W	OP[2]		
Read Pattern/LFSR Seed UI3	R/W	OP[3]		
Read Pattern/LFSR Seed UI4	R/W	OP[4]		
Read Pattern/LFSR Seed UI5	R/W	OP[5]		
Read Pattern/LFSR Seed UI6	R/W	OP[6]		
Read Pattern/LFSR Seed UI7	R/W	OP[7]		

Note: 1. Default = 0x5A

MR27 Read Training Pattern Data1/LFSR1 Seed

Table 48: MR27 Register and OP-Code Bit Definitions (MA[7:0] = 1Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Data1/LFSR1 Seed							

Function	Type	OP	Description/Data	Notes
Read Pattern/LFSR Seed UI8	R/W	OP[0]	UI<15:8> data for serial mode, LFSR1 seed for LFSR mode	1
Read Pattern/LFSR Seed UI9	R/W	OP[1]		
Read Pattern/LFSR Seed UI10	R/W	OP[2]		
Read Pattern/LFSR Seed UI11	R/W	OP[3]		
Read Pattern/LFSR Seed UI12	R/W	OP[4]		
Read Pattern/LFSR Seed UI13	R/W	OP[5]		
Read Pattern/LFSR Seed UI14	R/W	OP[6]		
Read Pattern/LFSR Seed UI15	R/W	OP[7]		

Note: 1. Default = 0x3C

MR28 Read Training Pattern Invert Lower Byte DQs

Table 49: MR28 Register and OP-Code Bit Definitions (MA[7:0] = 1Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Invert Lower Byte DQs							

Function	Type	OP	Description/Data	Notes
DQ invert (lower DQ bits)	R/W	OP[0]	DQL0 (DQ0): 0b=normal, 1b=invert	1
	R/W	OP[1]	DQL1 (DQ1): 0b=normal, 1b=invert	
	R/W	OP[2]	DQL2 (DQ2): 0b=normal, 1b=invert	
	R/W	OP[3]	DQL3 (DQ3): 0b=normal, 1b=invert	
	R/W	OP[4]	DQL4 (DQ4): 0b=normal, 1b=invert	
	R/W	OP[5]	DQL5 (DQ5): 0b=normal, 1b=invert	
	R/W	OP[6]	DQL6 (DQ6): 0b=normal, 1b=invert	
	R/W	OP[7]	DQL7 (DQ7): 0b=normal, 1b=invert	

Note: 1. Default = 0x00

MR29 Read Training Pattern Invert Upper Byte DQs

Table 50: MR29 Register and OP-Code Bit Definitions (MA[7:0] = 1Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Invert Upper Byte DQs							

Function	Type	OP	Description/Data	Notes
DQ invert (upper DQ bits)	R/W	OP[0]	DQU0 (DQ8): 0b=normal, 1b=invert	1
	R/W	OP[1]	DQU1 (DQ9): 0b=normal, 1b=invert	
	R/W	OP[2]	DQU2 (DQ10): 0b=normal, 1b=invert	
	R/W	OP[3]	DQU3 (DQ11): 0b=normal, 1b=invert	
	R/W	OP[4]	DQU4 (DQ12): 0b=normal, 1b=invert	
	R/W	OP[5]	DQU5 (DQ13): 0b=normal, 1b=invert	
	R/W	OP[6]	DQU6 (DQ14): 0b=normal, 1b=invert	
	R/W	OP[7]	DQU7 (DQ15): 0b=normal, 1b=invert	

Note: 1. Default = 0x00

MR30 Read LFSR Assignments

Table 51: MR30 Register and OP-Code Bit Definitions (MA[7:0] = 1Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read LFSR Assignments							

Function	Type	OP	Description/Data	Notes
LFSR Assignment DQ0/DQ8 (DQL0/DQU0)	R/W	OP[0]	0b = read pattern data0/LFSR0, 1b = read pattern data1/LFSR1	1
LFSR Assignment DQ1/DQ9 (DQL1/DQU1)	R/W	OP[1]		
LFSR Assignment DQ2/DQ10 (DQL2/DQU2)	R/W	OP[2]		
LFSR Assignment DQ3/DQ11 (DQL3/DQU3)	R/W	OP[3]		
LFSR Assignment DQ4/DQ12 (DQL4/DQU4)	R/W	OP[4]		
LFSR Assignment DQ5/DQ13 (DQL5/DQU5)	R/W	OP[5]		
LFSR Assignment DQ6/DQ14 (DQL6/DQU6)	R/W	OP[6]		
LFSR Assignment DQ7/DQ15 (DQL7/DQU7)	R/W	OP[7]		

Note: 1. Default = 0xFE

MR31 Read Training Pattern Address

Table 52: MR31 Register and OP-Code Bit Definitions (MA[7:0] = 1Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Read Training Pattern Address							

Function	Type	OP	Description/Data	Notes
Read Training Pattern Address	R	OP[7:0]	Reserved. No specific register fields are associated with this address. In response to the MRR to this address, the device sends the BL16 read training pattern. All 8 bits associated with this MR address are reserved.	

MR32-MR102

MR32 CK ODT, CS ODT, CA ODT Strap

Table 53: MR32 Register and OP-Code Bit Definitions (MA[7:0] = 20h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

Function	Type	OP	Description/Data	Notes
CK ODT	R	OP[2:0]	000b=RTT_OFF (disable), 001b=R _{ZQ} /0.5 (480 ohm), 010b=R _{ZQ} /1 (240 ohm), 011b=R _{ZQ} /2 (120 ohm), 100b=R _{ZQ} /3 (80 ohm), 101b=R _{ZQ} /4 (60 ohm), 110b=RFU, 111b=R _{ZQ} /6 (40 ohm); Group A default=000b, Group B default=111b	1, 2
CS ODT	R	OP[5:3]	000b=RTT_OFF (disable), 001b=R _{ZQ} /0.5 (480 ohm), 010b=R _{ZQ} /1 (240 ohm), 011b=R _{ZQ} /2 (120 ohm), 100b=R _{ZQ} /3 (80 ohm), 101b=R _{ZQ} /4 (60 ohm), 110b=RFU, 111b=R _{ZQ} /6 (40 ohm); Group A default =000b, Group B default=111b	1, 2
CA_ODT Strap Value	R	OP[6]	0b=group A, 1b=group B	3
RFU	RFU	OP[7]	RFU	

Notes: 1. This mode register is programmed via an explicit MPC command only.
 2. CK ODT $R_{ZQ}/2$ (120 ohm) and CS ODT $R_{ZQ}/2$ (120 ohm) are only supported at >5200 MT/s data rates.
 3. Strapping for ODT on Command and Address. The device applies Group A settings if the CA_ODT pin is connected to V_{SS} and Group B settings if the CA_ODT pin is connected to V_{DD} . This MR is used to confirm the device's setting for that configuration.

MR33 CA ODT, DQS_RTT_PARK

Table 54: MR33 Register and OP-Code Bit Definitions (MA[7:0] = 21h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		DQS_RTT_PARK			CA ODT		

Function	Type	OP	Description/Data	Notes
CA ODT	R	OP[2:0]	000b=RTT_OFF (default), 001b= $R_{ZQ}/0.5$ (480 ohm), 010b= $R_{ZQ}/1$ (240 ohm), 011b= $R_{ZQ}/2$ (120 ohm), 100b= $R_{ZQ}/3$ (80 ohm), 101b= $R_{ZQ}/4$ (60 ohm), 110b=RFU, 111b= $R_{ZQ}/6$ (40 ohm); Group A default =000b, Group B default=0x100b	1, 2
DQS_RTT_PARK	R	OP[5:3]	000b=RTT_OFF (default), 001b= R_{ZQ} (240 ohm), 010b= $R_{ZQ}/2$ (120 ohm), 011b= $R_{ZQ}/3$ (80 ohm), 100b= $R_{ZQ}/4$ (60 ohm), 101b= $R_{ZQ}/5$ (48 ohm), 110b= $R_{ZQ}/6$ (40 ohm); 111b= $R_{ZQ}/7$ (34 ohm)	1
RFU	RFU	OP[7:6]	RFU	

Notes: 1. This mode register is programmed via an explicit MPC command only.
 2. CA ODT $R_{ZQ}/2$ (120 ohm) is only supported at >5200 MT/s data rates.

MR34 RTT_PARK and RTT_WR

Table 55: MR34 Register and OP-Code Bit Definitions (MA[7:0] = 22h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		RTT_WR			RTT_PARK		

Function	Type	OP	Description/Data	Notes
RTT_PARK	R	OP[2:0]	000b=RTT_OFF (default), 001b= R_{ZQ} (240 ohm), 010b= $R_{ZQ}/2$ (120 ohm), 011b= $R_{ZQ}/3$ (80 ohm), 100b= $R_{ZQ}/4$ (60 ohm), 101b= $R_{ZQ}/5$ (48 ohm), 110b= $R_{ZQ}/6$ (40 ohm), 111b= $R_{ZQ}/7$ (34 ohm)	1
RTT_WR	R/W	OP[5:3]	000b=RTT_OFF, 001b= R_{ZQ} (240 ohm) (default), 010b= $R_{ZQ}/2$ (120 ohm), 011b= $R_{ZQ}/3$ (80 ohm), 100b= $R_{ZQ}/4$ (60 ohm), 101b= $R_{ZQ}/5$ (48 ohm), 110b= $R_{ZQ}/6$ (40 ohm), 111b= $R_{ZQ}/7$ (34 ohm)	
RFU	RFU	OP[7:6]	RFU	

Note: 1. This mode register is programmed via an explicit MPC command only.

MR35 RTT_NOM_WR and RTT_NOM_RD

Table 56: MR35 Register and OP-Code Bit Definitions (MA[7:0] = 23h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		RTT_NOM_RD			RTT_NOM_WR		

Function	Type	OP	Description/Data	Notes
RTT_NOM_WR	R/W	OP[2:0]	000b=OFF, 001b= R_{ZQ} (240 ohm), 010b= $R_{ZQ}/2$ (120 ohm), 011b= $R_{ZQ}/3$ (80 ohm) (default), 100b= $R_{ZQ}/4$ (60 ohm), 101b= $R_{ZQ}/5$ (48 ohm), 110b= $R_{ZQ}/6$ (40 ohm), 111b= $R_{ZQ}/7$ (34 ohm)	

Function	Type	OP	Description/Data	Notes
RTT_NOM_RD	R/W	OP[5:3]	000b=OFF, 001b=R _{ZQ} (240 ohm), 010b=R _{ZQ} /2 (120 ohm), 011b=R _{ZQ} /3 (80 ohm) (default), 100b=R _{ZQ} /4 (60 ohm), 101b=R _{ZQ} /5 (48 ohm), 110b=R _{ZQ} /6 (40 ohm), 111b=R _{ZQ} /7 (34 ohm)	
RFU	RFU	OP[7:6]	RFU	

MR36 RTT_Loopback

Table 57: MR36 Register and OP-Code Bit Definitions (MA[7:0] = 24h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					RTT_Loopback		

Function	Type	OP	Description/Data	Notes
RTT_Loopback	R/W	OP[2:0]	000b=RTT_OFF (default), 001-100b=RFU, 101b=R _{ZQ} /5 (48 ohm), 110-111b=RFU	1
RFU	RFU	OP[7:3]	RFU	

Note: 1. When Loopback is disabled, both LBDQS and LBDQ pins are either at High-Z or termination mode. When Loopback is enabled, it is in driver mode.

MR37 ODT Write Control Offset

Table 58: MR37 Register and OP-Code Bit Definitions (MA[7:0] = 25h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTLoff_WR_Offset			ODTLon_WR_Offset		

Function	Type	OP	Description/Data	Notes
ODTLon_WR_Offset	R/W	OP[2:0]	000b=RFU, 001b=-4 clocks, 010b=-3 clocks, 011b=-2 clocks, 100b=-1 clocks (default), 101b=0 clocks, 110b=+1 clock, 111b=+2 clocks	
ODTLoff_WR_Offset	R/W	OP[5:3]	000b=RFU, 001b=+4 clocks, 010b=+3 clocks, 011b=+2 clocks, 100b=+1 clocks, 101b=0 clocks (default), 110b=-1 clock, 111b=-2 clocks	
RFU	RFU	OP[7:6]	RFU	

Note: 1. The Write ODTLon -4 offset and Write ODTLoff +4 offset is not allowed for 1980–2100 data rates.

MR38 ODTL Write NT Control Offset

Table 59: MR38 Register and OP-Code Bit Definitions (MA[7:0] = 26h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTLoff_WR_NT_Offset			ODTLon_WR_NT_Offset		

Function	Type	OP	Description/Data	Notes
ODTLon_WR_NT_Offset	R/W	OP[2:0]	000b=RFU, 001b=-4 clocks, 010b=-3 clocks, 011b=-2 clocks, 100b=-1 clocks (default), 101b=0 clocks, 110b=+1 clock, 111b=+2 clocks	
ODTLoff_WR_NT_Offset	R/W	OP[5:3]	000b=RFU, 001b=+4 clocks, 010b=+3 clocks, 011b=+2 clocks, 100b=+1 clocks, 101b=0 clocks (default), 110b=-1 clock, 111b=-2 clocks	
RFU	RFU	OP[7:6]	RFU	

Note: 1. The Write NT ODTLon -4 offset and Write NT ODTLoff +4 offset is not allowed for 1980–2100 data rates.

MR39 ODT RD NT Control Offset

Table 60: MR39 Register and OP-Code Bit Definitions (MA[7:0] = 27h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		ODTLoff_RD_NT_Offset			ODTLon_RD_NT_Offset		

Function	Type	OP	Description/Data	Notes
ODTLon_RD_NT_Offset	R/W	OP[2:0]	000b=RFU, 001b=RFU, 010b=-3 clocks, 011b=-2 clocks, 100b=-1 clocks (default), 101b=0 clocks, 110b=+1 clock, 111b=RFU	
ODTLoff_RD_NT_Offset	R/W	OP[5:3]	000b=RFU, 001b=RFU, 010b=+3 clocks, 011b=+2 clocks, 100b=+1 clocks, 101b=0 clocks (default), 110b=-1 clock, 111b=RFU	
RFU	RFU	OP[7:6]	RFU	

MR40 Read DQS Offset Timing

Table 61: MR40 Register and OP-Code Bit Definitions (MA[7:0] = 28h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU					Read DQS Offset Timing		

Function	Type	OP	Description/Data	Notes
Read DQS Offset Timing	R/W	OP[2:0]	000=0 clocks (default), 001b=1 clock, 010b=2 clocks, 011b=3 clocks, 100-111b=RFU	1
RFU	RFU	OP[7:3]	RFU	

Note: 1. When operating at low speed (CL ≤30), ^tRPRE + Read DQS offset ≥5 clocks cannot be supported.

MR41 RFU

Table 62: MR41 Register and OP-Code Bit Definitions (MA[7:0] = 29h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[7:0]	RFU	

MR42 DCA Types Supported

Table 63: MR42 Register and OP-Code Bit Definitions (MA[7:0] = 2Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DCA Training Assist Mode II (optional)				DCA Training Assist Mode I		DCA Types Supported	

Function	Type	OP	Description/Data	Notes
DCA Types Supported	R	OP[1:0]	00b=device does not support DCA, 01b=device supports DCA for single/two-phase internal clock(s), 10b=device supports DCA for four-phase internal clocks, 11b=RFU	

Function	Type	OP	Description/Data	Notes
DCA Training Assist Mode I	R/W	OP[3:2]	00b=disable (default), 01b=MRR (or Read) synchronized with IBCLK is blocked, 10b=MRR (or Read) synchronized with ICLK is blocked, 11b=RFU	1,2,3,4,5,6
DCA Training Assist Mode II	R/W	OP[6:4]	00b=disable (default), 001b=DQ fires 0001 data pattern, 010b=DQ fires 0011 data pattern, 011b=DQ fires 0111 data pattern, 100b=DQ fires 1000 data pattern, 101b=DQ fires 1100 data pattern, 110b=DQ fires 1110 data pattern, 111b=RFU	3,4,5,7,8,9,10,11
	SR/W	OP[7]	DRAM Status Read (SR) 0b: DCA Training Assist Mode II is not supported 1b: DCA Training Assist Mode II is supported Host Write (W) 0b: MRR-based (default) 1b: Continuous burst output	

- Notes: 1. When “MRR (or Read) synchronized with IBCLK is blocked” is set by MR42 OP[3:2]=01b, DQs caused by MRR (or Read) synchronized with IBCLK are driven HIGH.
2. When “MRR (or Read) synchronized with ICLK is blocked” is set by MR42 OP[3:2]=10b, DQs caused by MRR (or Read) synchronized with ICLK are driven HIGH.
3. DQS_t/DQS_c output normal toggling waveforms meaning that DQS_t/DQS_c are not affected by the settings of DCA Assist Mode MR42 OP[3:2].
4. The CRC function is not supported during DCA Training Assist mode.
5. DCA Training Assist mode is only supported by DRAMs with DCAs that have 4-phase internal clocks.
6. If MR42: OP[3:2] is set to either 01b or 10b, odd-gap READ or odd-gap MODE REGISTER READ PATTERN commands should follow the ^tMRR timing specification.
7. The MRR-based mode of DCA Training Assist Mode II is enabled when the host sets MR42:OP[6:4]≠000b and MR42:OP[7]=0b. The DRAM will provide the selected predefined pattern when the host issues an MRR command to MR42. Issuing any MRR other than to MR42 is invalid and may result in unexpected DQ behavior, requiring the host to issue a reset to exit MRR-based mode and restart the training with an MRR to MR42. The returned data will be a predefined pattern instead of the contents of a mode register. The timing of the read data return is the same as for an MRR command, including the operation of the strobes (DQS_t, DQS_c). The host can issue an MRW to MR42:OP[6:4]≠000b to change data pattern during MRR-based mode. The host needs to issue MRW to MR42:OP[6:4]=000b to exit the MRR-based mode.
8. Continuous burst output mode is available for DCA Training Assist Mode II and is enabled with an MRW to MR42:OP[6:4]≠000b and MR42:OP[7]=1. After this mode is enabled, an MRR to MR42 will start the pattern output and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or issuing an MRW MR42:OP[7]=0b command that reverts it to the MRR based (Default) mode. Issuing any MRR other than to MR42 is invalid and may result in unexpected DQ behavior, requiring the host to issue a reset to exit continuous burst output mode and restart the training with an MRR to MR42. After the MR42:OP[7]=0b MRR based (Default) is registered by the DRAM, it will stop all pattern traffic by ^tCont_Exit. Because there is no MIN time for ^tCont_Exit, the DRAM may stop the pattern prior to ^tCont_Exit, potentially truncating any current burst pattern. To ensure that the DRAM's state-machine doesn't get into some metastability while turning off the output pattern, the host must issue a second MR42:OP[7]=0b MRR based (Default) after waiting ^tMRR, which will then start ^tCont_Exit_delay. After ^tCont_Exit_delay has expired, any other valid command is then legal. Issuing any MRW other than MRW to MR42:OP[7]=0 during continuous burst mode after predefined pattern output started is invalid and may result in unexpected DQ behavior, requiring the host to issue a reset to exit continuous burst output mode and restart the training with an MRR to MR42.
9. The DCA Training Assist Mode I and II can not be enabled at the same time by the host. That is, while the DCA Training Assist Mode II is enabled, the DCA Training Assist Mode I must be disabled by the host and vice versa.
10. Depending on relationship of internal clocks and MRR command, DRAM may start outputting from the 3rd bit of data pattern. The data pattern is defined with ICLK bases (1st=ICLK, 2nd=QCLK, 3rd=IBCLK and 4th=QBCLK), but MRR burst may start from IBCLK.
11. In DCA assist mode II, MRR to MR42 outputs the repetitive data pattern through all DQ bits for a 16-bit burs. For example, if MR42:OP[6:4]=0010b and issues MRR to MR42 is issued, all DQs output the same 0011001100110011 data pattern.

MR43 DCA Settings 1

Table 64: MR43 Register and OP-Code Bit Definitions (MA[7:0] = 2Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Sign Bit for OP[6:4]	DCA for IBCLK in 4-phase clock			Sign Bit for OP[2:0]	DCA for single/2-phase clock(s) or QCLK in 4-phase clocks		

Function	Type	OP	Description/Data	Notes
DCA for single/2-phase clock(s) or QCLK in 4-phase clocks	W	OP[2:0]	000b=DCA step +0 (default), 001b=DCA step +1, 010b=DCA step +2, 011b=DCA step +3, 100b=DCA step +4, 101b=DCA step +5, 110b=DCA step +6, 111b=DCA step +7	1
Sign Bit for OP[2:0]	W	OP[3]	0b=positive offset (default), 1b=negative offset	1
DCA for IBCLK in 4-phase clocks	W	OP[6:4]	000b=DCA step +0 (default), 001b=DCA step +1, 010b=DCA step +2, 011b=DCA step +3, 100b=DCA step +4, 101b=DCA step +5, 110b=DCA step +6, 111b=DCA step +7	2
Sign Bit for OP[6:4]	W	OP[7]	0b=positive offset (default), 1b=negative offset	2

Notes: 1. These settings can be applied only if MR42[1:0] = 01b or 10b.

2. These settings can be applied only if MR42[1:0] = 10b.

MR44 DCA Settings 2

Table 65: MR44 Register and OP-Code Bit Definitions (MA[7:0] = 2Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Sign Bit for QBCLK in 4-phase clocks	DCA for QBCLK in 4-phase clocks		

Function	Type	OP	Description/Data	Notes
DCA for QBCLK in 4-phase clocks	W	OP[2:0]	000b=DCA step +0 (default), 001b=DCA step +1, 010b=DCA step +2, 011b=DCA step +3, 100b=DCA step +4, 101b=DCA step +5, 110b=DCA step +6, 111b=DCA step +7	1
Sign Bit for QBCLK in 4-phase clocks	W	OP[3]	0b=positive offset (default), 1b=negative offset	1
RFU	RFU	OP[7:4]	RFU	

Note: 1. These settings can be applied only if MR42[1:0] = 10b.

MR45 DQS Interval Control

Table 66: MR45 Register and OP-Code Bit Definitions (MA[7:0] = 2Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Interval Timer Run Time							

Function	Type	OP	Description/Data	Notes
DQS Interval Timer Run Time	W	OP[7:0]	0000 0000b: DQS interval timer stop via MPC command (default) 0000 0001b: DQS timer stops at 16th clocks after timer start 0000 0010b: DQS timer stops at 32nd clocks after timer start 0000 0011b: DQS timer stops at 48th clocks after timer start 0000 0100b: DQS timer stops at 64th clocks after timer start ----- thru ----- 0011 1111b: DQS timer stops at (63X16)th clocks after timer start 01XX XXXXb: DQS timer stops at 2048th clocks after timer start 10XX XXXXb: DQS timer stops at 4096th clocks after timer start 11XX XXXXb: DQS timer stops at 8192nd clocks after timer start	1,2

- Notes: 1. MPC command with OP[7:0]=0000 0110b (STOP DQS INTERVAL OSCILLATOR) stops DQS interval timer in case of MR45:OP[7:0] = 00000000b.
 2. MPC command with OP[7:0]=0000 0110b (STOP DQS INTERVAL OSCILLATOR) is illegal with non-zero values in MR45:OP[7:0].

MR46 DQS Interval Oscillator Count — LSB

Table 67: MR46 Register and OP-Code Bit Definitions (MA[7:0] = 2Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Interval Osc Count - LSB							

Function	Type	OP	Description/Data	Notes
DQS Interval Osc Count - LSB	R	OP[7:0]	0-255 LSB	1,2,3

- Notes: 1. MR46 reports the LSB bits of the DQS Oscillator count. The DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
 2. Both MR46 and MR47 must be read (MRR) and combined to obtain the value of the DQS Oscillator count.
 3. A new MPC (START DQS OSCILLATOR) should be issued to reset the contents of MR46/MR47.

MR47 DQS Interval Oscillator Count — MSB

Table 68: MR47 Register and OP-Code Bit Definitions (MA[7:0] = 2Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Interval Osc Count - MSB							

Function	Type	OP	Description/Data	Notes
DQS Interval Osc Count - MSB	R	OP[7:0]	0-255 MSB	1,2,3

- Notes: 1. MR47 reports the MSB bits of the DQS Oscillator count. The DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
 2. Both MR46 and MR47 must be read (MRR) and combined to obtain the value of the DQS Oscillator count.
 3. A new MPC (START DQS OSCILLATOR) should be issued to reset the contents of MR46/MR47.

MR48 Write Pattern Data

Table 69: MR48 Register and OP-Code Bit Definitions (MA[7:0] = 30h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Pattern DQ7/ DQ15	Write Pattern DQ6/ DQ14	Write Pattern DQ5/ DQ13	Write Pattern DQ4/ DQ12	Write Pattern DQ3/ DQ11	Write Pattern DQ2/ DQ10	Write Pattern DQ1/DQ9	Write Pattern DQ0/DQ8

Function	Type	OP	Description/Data	Notes
Write Pattern DQ0/DQ8 (DQL0/DQU0)	R/W	OP[0]	Data for DQ0/DQ8 (DQL0/DQU0)	1,2,3
Write Pattern DQ1/DQ9 (DQL1/DQU1)	R/W	OP[1]	Data for DQ1/DQ9 (DQL1/DQU1)	
Write Pattern DQ2/DQ10 (DQL2/DQU2)	R/W	OP[2]	Data for DQ2/DQ10 (DQL2/DQU2)	
Write Pattern DQ3/DQ11 (DQL3/DQU3)	R/W	OP[3]	Data for DQ3/DQ11 (DQL3/DQU3)	
Write Pattern DQ4/DQ12 (DQL4/DQU4)	R/W	OP[4]	Data for DQ4/DQ12 (DQL4/DQU4)	
Write Pattern DQ5/DQ13 (DQL5/DQU5)	R/W	OP[5]	Data for DQ5/DQ13 (DQL5/DQU5)	
Write Pattern DQ6/DQ14 (DQL6/DQU6)	R/W	OP[6]	Data for DQ6/DQ14 (DQL6/DQU6)	
Write Pattern DQ7/DQ15 (DQL7/DQU7)	R/W	OP[7]	Data for DQ7/DQ15 (DQL7/DQU7)	

Notes: 1. OP[7:0] can be independently programmed with either 0 or 1.
 2. Default 0x00.
 3. If CRC enabled, ALERT_n will not be issued from the device during Write Pattern mode.

MR49 RFU

Table 70: MR49 Register and OP-Code Bit Definitions (MA[7:0] = 31h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[7:0]	RFU	

MR50 CRC Settings

Table 71: MR50 Register and OP-Code Bit Definitions (MA[7:0] = 32h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		Write CRC Auto-Disable Status	Write CRC Auto-Disable Enable	Write CRC Error Status	Write CRC Enable Upper Nibble	Write CRC Enable Lower Nibble	Read CRC Enable

Function	Type	OP	Description/Data	Notes
Read CRC Enable	R/W	OP[0]	0b=disable (default), 1b=enable	

Function	Type	OP	Description/Data	Notes
Write CRC Enable Lower Nibble	R/W	OP[1]	0b=disable (default), 1b=enable	1
Write CRC Enable Upper Nibble	R/W	OP[2]	0b=disable (default), 1b=enable	1
Write CRC Error Status	R/W	OP[3]	0b=clear, 1b=error (MRW can only set to 0 (clear); it cannot set to 1 (error))	
Write CRC Auto-Disable Enable	R/W	OP[4]	0b=disable (default), 1b=enable	
Write CRC Auto-Disable Status	R/W	OP[5]	0b=not triggered, 1b= triggered (MRW can only set to 0 (not triggered); it cannot set to 1 (triggered))	
RFU	RFU	OP[7:6]	RFU	

Notes: 1. When at least one of the two write CRC enable bits is set to 1 in x8, the timing of Write CRC Enable mode is applied to the entire device (that is, both nibbles). When Write CRC is enabled in one nibble and disabled in the other nibble in x8, the device does not check CRC errors on the disabled nibble, and therefore, the ALERT_n signal and any internal status bit related to CRC error is not impacted by the disabled nibble.

2. The host must disable Write CRC, if enabled, prior to entering Write Leveling Training mode.

MR51 Write CRC Auto-Disable Threshold

Table 72: MR51 Register and OP-Code Bit Definitions (MA[7:0] = 33h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Write CRC Auto-Disable Threshold						

Function	Type	OP	Description/Data	Notes
Write CRC Auto-Disable Threshold	R/W	OP[6:0]	0000000b=0...1111111b=127 OP[6:0] corresponds to threshold bits [:0]	
RFU	RFU	OP[7]	RFU	

MR52 Write CRC Auto-Disable Window

Table 73: MR52 Register and OP-Code Bit Definitions (MA[7:0] = 34h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Write CRC Auto-Disable Window						

Function	Type	OP	Description/Data	Notes
Write CRC Auto-Disable Window	R/W	OP[6:0]	0000000b=0, 1111111b=127 OP[6:0] corresponds to threshold bits [:0]	
RFU	RFU	OP[7]	RFU	

MR53 Loopback

Table 74: MR53 Register and OP-Code Bit Definitions (MA[7:0] = 35h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Loopback Output Mode	Loopback Select Phase		Loopback Output Select				

Function	Type	OP	Description/Data	Notes
Loopback Output Select	R/W	OP[4:0]	00000b=loopback disabled (default), 00001b=loopback DM(L) (x8 and x16 only), 00010b=loopback DMU (X16 only), 00011b=vendor-specific, 00100b=vendor-specific, 00101b=01111b=RFU, 10000b=loopback DQL0, 10001b=loopback DQL1, 10010b=loopback DQL2, 10011b=loopback DQL3, 10100b=loopback DQL4 (X8 and X16 only), 10101b=loopback DQL5 (X8 and X16 only), 10110b=loopback DQL6 (X8 and X16 only), 10111b=loopback DQL7 (X8 and X16 only), 11000b=loopback DQU0 (X16 only), 11001b=loopback DQU1 (X16 only), 11010b=loopback DQU2 (X16 only), 11011b=loopback DQU3 (X16 only), 11100b=loopback DQU4 (X16 only), 11101b=loopback DQU5 (X16 only), 11110b=loopback DQU6 (X16 only), 11111b=loopback DQU7 (X16 only)	1,2
Loopback Select Phase	R/W	OP[6:5]	00b=loopback select phase A, 01b=loopback select phase B (4-way and 2-way interleave only), 10b=loopback select phase C (4-way interleave only), 11b=loopback select phase D (4-way interleave only)	3
Loopback Output Mode	R/W	OP[7]	0b=normal output (Default), 1b=write burst output	4

- Notes: 1. When loopback is disabled, both LBDQS and LBDQ pins are either at Hi-Z or termination mode per MR36:OP[2:0]. Loopback termination default value is RTT_OFF.
2. When loopback is enabled, both LBDQS and LBDQ pins are in driver mode using default R_{ON} of 34 ohm.
3. Phase A through D determines which bit in the multiplexer is being selected for loopback output.
4. This configures the loopback output to either send data out every time the DQS toggles in normal output mode, or to send data out only when enabled by the WRITE command, so that only write burst data is sent out via loopback.
5. The DM function shall be enabled (MR5:OP[5] = 1) when loopback output from the DML or DMU pin is selected for loopback measurement (MR53:OP[4:0] = 00001b or 00010b).

MR54 hPPR Resources 1

Table 75: MR54 Register and OP-Code Bit Definitions (MA[7:0] = 36h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG1 Bank 3	hPPR Resource BG1 Bank 2	hPPR Resource BG1 Bank 1	hPPR Resource BG1 Bank 0	hPPR Resource BG0 Bank 3	hPPR Resource BG0 Bank 2	hPPR Resource BG0 Bank 1	hPPR Resource BG0 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG0 Bank 0	R	OP[0]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG0 Bank 1	R	OP[1]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG0 Bank 2	R	OP[2]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3
hPPR Resource BG0 Bank 3	R	OP[3]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3
hPPR Resource BG1 Bank 0	R	OP[4]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG1 Bank 1	R	OP[5]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG1 Bank 2	R	OP[6]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3

Function	Type	OP	Description/Data	Notes
hPPR Resource BG1 Bank 3	R	OP[7]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3

Notes: 1. Don't care for 8Gb.
2. Don't care for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR55 hPPR Resources 2

Table 76: MR55 Register and OP-Code Bit Definitions (MA[7:0] = 37h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG3 Bank 3	hPPR Resource BG3 Bank 2	hPPR Resource BG3 Bank 1	hPPR Resource BG3 Bank 0	hPPR Resource BG2 Bank 3	hPPR Resource BG2 Bank 2	hPPR Resource BG2 Bank 1	hPPR Resource BG2 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG2 Bank 0	R	OP[0]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG2 Bank 1	R	OP[1]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG2 Bank 2	R	OP[2]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3
hPPR Resource BG2 Bank 3	R	OP[3]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3
hPPR Resource BG3 Bank 0	R	OP[4]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG3 Bank 1	R	OP[5]	0b=hPPR Resource not available, 1b=hPPR Resource available	3
hPPR Resource BG3 Bank 2	R	OP[6]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3
hPPR Resource BG3 Bank 3	R	OP[7]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,3

Notes: 1. Don't care for 8Gb.
2. Don't care for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR56 hPPR Resources 3

Table 77: MR56 Register and OP-Code Bit Definitions (MA[7:0] = 38h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG5 Bank 3	hPPR Resource BG5 Bank 2	hPPR Resource BG5 Bank 1	hPPR Resource BG5 Bank 0	hPPR Resource BG4 Bank 3	hPPR Resource BG4 Bank 2	hPPR Resource BG4 Bank 1	hPPR Resource BG4 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG4 Bank 0	R	OP[0]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3
hPPR Resource BG4 Bank 1	R	OP[1]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3

Function	Type	OP	Description/Data	Notes
hPPR Resource BG4 Bank 2	R	OP[2]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3
hPPR Resource BG4 Bank 3	R	OP[3]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3
hPPR Resource BG5 Bank 0	R	OP[4]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3
hPPR Resource BG5 Bank 1	R	OP[5]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3
hPPR Resource BG5 Bank 2	R	OP[6]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3
hPPR Resource BG5 Bank 3	R	OP[7]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3

Notes: 1. Don't care for 8Gb.
2. Don't care for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR57 hPPR Resources 4

Table 78: MR57 Register and OP-Code Bit Definitions (MA[7:0] = 39h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
hPPR Resource BG7 Bank 3	hPPR Resource BG7 Bank 2	hPPR Resource BG7 Bank 1	hPPR Resource BG7 Bank 0	hPPR Resource BG6 Bank 3	hPPR Resource BG6 Bank 2	hPPR Resource BG6 Bank 1	hPPR Resource BG6 Bank 0

Function	Type	OP	Description/Data	Notes
hPPR Resource BG6 Bank 0	R	OP[0]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3
hPPR Resource BG6 Bank 1	R	OP[1]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3
hPPR Resource BG6 Bank 2	R	OP[2]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3
hPPR Resource BG6 Bank 3	R	OP[3]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3
hPPR Resource BG7 Bank 0	R	OP[4]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3
hPPR Resource BG7 Bank 1	R	OP[5]	0b=hPPR Resource not available, 1b=hPPR Resource available	2,3
hPPR Resource BG7 Bank 2	R	OP[6]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3
hPPR Resource BG7 Bank 3	R	OP[7]	0b=hPPR Resource not available, 1b=hPPR Resource available	1,2,3

Notes: 1. Don't care for 8Gb.
2. Don't care for x16 devices.
3. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be configured to indicate which slice in the 3DS stack is referenced in the MR54-MR57 hPPR resource information.

MR58 RFM Configuration

Table 79: MR58 Register and OP-Code Bit Definitions (MA[7:0] = 3Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Rolling Accumulated ACT Maximum Management Threshold (RAAMMT)			Rolling Accumulated ACT Initial Management Threshold (RAAIMT)			RFM Required	

Function	Type	OP	Description/Data	Notes
RFM Required	R	OP[0]	0b=refresh management not required; 1b=refresh management required	1,3
Rolling Accumulated ACT Initial Management Threshold (RAAIMT)	R	OP[4:1]	0000-0011b=RFU (normal), RFU (FGR); 0100b=32 (normal), 16 (FGR); 0101b=40 (normal), 20 (FGR); ... 1001b=72 (normal), 36 (FGR); 1010b=80 (normal), 40 (FGR); 1011-1111b=RFU (normal), RFU (FGR)	1,2
Rolling Accumulated ACT Maximum Management Threshold (RAAMMT)	R	OP[7:5]	000-010b=RFU (normal), RFU (FGR); 011b=3x (normal), 6x (FGR); 100b=4x (normal), 8x (FGR); 101b=5x (normal), 10x (FGR); 110b=6x (normal), 12x (FGR); 111b=RFU (normal), RFU (FGR)	1,2

- Notes: 1. Refresh management settings are vendor-specific by the MR settings.
2. Only applicable if the refresh management required bit is set to 1 (MR58:OP[0] = 1b) or ARFM is set to level A, B, or C.
3. Specific attempts to by-pass the on-die circuitry designed to protect data integrity may result in data disturb.

MR59 DRFM, ARFM, RFM RAA Counter

Table 80: MR59 Register and OP-Code Bit Definitions (MA[7:0] = 3Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RAA Counter Decrement per REF Command		Adaptive RFM (ARFM)		BRC Support Level	Bounded Refresh Configuration (BRC)		DRFM Enable (DRFE)

Function	Type	OP	Description/Data	Notes
DRFM Enable (DRFE)	SR/W	OP[0]	DRAM Status Read (SR): 0b: DRFM not implemented (default); 1b: DRFM implemented Host Write (W): 0b: DRFM disabled (default); 1b: DRFM enabled	3
Bounded Refresh Configuration (BRC)	R/W	OP[2:1]	00b: BRC 2 (Default); 01b: BRC 3; 10b: BRC 4; 11b: RFU	3
BRC Support Level	R	OP[3]	0b: BRC2,3,4 (default); 1b: BRC2 only	3
Adaptive RFM (ARFM)	R/W	OP[5:4]	00b=default (RAAIMT, RAAMMT, RAADEC); 01b=level A (RAAIMT-A, RAAMMT-A, RAADEC-A); 10b=level B (RAAIMT-B, RAAMMT-B, RAADEC-B); 11b=level C (RAAIMT-C, RAAMMT-C, RAADEC-C)	1
RAA Counter Decrement per REF Command	R	OP[7:6]	00b=RAAIMT, 01b=RAAIMT*0.5, 10b=RFU, 11b=RFU	1, 2

- Notes: 1. Refresh management settings are vendor-specific by the MR settings.
2. Only applicable if the refresh management required bit is set to 1 (MR58:OP[0] = 1b) or ARFM is set to level A, B, or C.
3. Only applicable if the DRFM function is supported (Status Read MR59:OP[0]=1b).

MR60 PASR Segment Mask

Support for PASR has been deprecated. Details shown are for devices that support the feature.

Table 81: MR60 Register and OP-Code Bit Definitions (MA[7:0] = 3Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment 7 (111)	Segment 6 (110)	Segment 5 (101)	Segment 4 (100)	Segment 3 (011)	Segment 2 (010)	Segment 1 (001)	Segment 0 (000)

Function	Type	OP	Description/Data	Notes
Segment 0 (000)	W	OP[0]	0b = normal; 1b = masked	1,2
Segment 1 (001)	W	OP[1]		1,2
Segment 2 (010)	W	OP[2]		1,2
Segment 3 (011)	W	OP[3]		1,2
Segment 4 (100)	W	OP[4]		1,2
Segment 5 (101)	W	OP[5]		1,2
Segment 6 (110)	W	OP[6]		1,2
Segment 7 (111)	W	OP[7]		1,2

Notes: 1. Must be 0 for 24Gb devices.

2. Bit will behave as RFU on devices that do not support PASR.

MR61 Package Output Driver Test Mode

Table 82: MR61 Register and OP-Code Bit Definitions (MA[7:0] = 3Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			Package Output Driver Test Mode				

Function	Type	OP	Description/Data	Notes
Package Output Driver Test Mode	W	OP[4:0]	00000b=package test disabled (default); 00001b=package test DML; 00010b=package test DMU (x16 only); 00011b=RFU; 00100b=RFU; 00101b=RFU ... thru ... 01111b=RFU; 10000b=package test DQL0; 10001b=package test DQL1; 10010b=package test DQL2; 10011b=package test DQL3; 10100b=package test DQL4 (X8 and X16 only); 10101b=package test DQL5 (x8 and x16 only); 10110b=package test DQL6 (x8 and x16 only); 10111b=package test DQL7 (x8 and x16 only); 11000b=package test DQU0 (x16 only); 11001b=package test DQU1 (x16 only); 11010b=package test DQU2 (x16 only); 11011b=package test DQU3 (x16 only); 11100b=package test DQU4 (x16 only); 11101b=package test DQU5 (x16 only); 11110b=package test DQU6 (x16 only); 11111b=package test DQU7 (x16 only)	
RFU	W	OP[7:5]	Must be programmed to 000b	

MR62 Vendor-Specified

Table 83: MR62 Register and OP-Code Bit Definitions (MA[7:0] = 3Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specified							

Function	Type	OP	Description/Data	Notes
Vendor-specified	R/W	OP[7:0]	Vendor-specified	

MR63 Scratch Pad

Table 84: MR63 Register and OP-Code Bit Definitions (MA[7:0] = 3Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DRAM Scratch Pad							
Function	Type	OP	Description/Data	Notes			
DRAM Scratch Pad	R/W	OP[7:0]	Any value is valid.	1,2			

Notes: 1. The contents of this register can be written via MRW and read via MRR but have no function in the device.
2. Details for this function can be found in the DDR5 RCD01 specification.

MR64 Reserved for Paging Pointer

Table 85: MR64 Register and OP-Code Bit Definitions (MA[7:0] = 40h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved for Paging Pointer							
Function	Type	OP	Description/Data	Notes			
Reserved for Paging Pointer	RFU	RFU	RFU				

MR65 Serial Number 1

Table 86: MR65 Register and OP-Code Bit Definitions (MA[7:0] = 41h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 1							
Function	Type	OP	Description/Data	Notes			
Serial Number 1	R	OP[7:0]	Any value is valid.				

MR66 Serial Number 2

Table 87: MR66 Register and OP-Code Bit Definitions (MA[7:0] = 42h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 2							
Function	Type	OP	Description/Data	Notes			
Serial Number 2	R	OP[7:0]	Any value is valid.				

MR67 Serial Number 3

Table 88: MR67 Register and OP-Code Bit Definitions (MA[7:0] = 43h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 3							

Function	Type	OP	Description/Data	Notes
Serial Number 3	R	OP[7:0]	Any value is valid.	

MR68 Serial Number 4

Table 89: MR68 Register and OP-Code Bit Definitions (MA[7:0] = 44h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 4							

Function	Type	OP	Description/Data	Notes
Serial Number 4	R	OP[7:0]	Any value is valid.	

MR69 Serial Number 5

Table 90: MR69 Register and OP-Code Bit Definitions (MA[7:0] = 45h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Serial Number 5							

Function	Type	OP	Description/Data	Notes
Serial Number 5	R	OP[7:0]	Any value is valid.	

MR70 PRAC, ABO

Table 91: MR70 Register and OP-Code Bit Definitions (MA[7:0] = 46h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ALERT_n Verification	ALERT_n Verification Support (optional)	Alert Back-Off Flag	RFU	Activation Counter Initialization Complete	Activation Counter Initialization	Per Row Activation Counting and Alert Back-Off Enable/Disable	Per Row Activation Counting and Alert Back-Off Support (Optional)

Function	Type	OP	Description/Data	Notes
Per Row Activation Counting and Alert Back-Off Support (Optional)	R	OP[0]	0b: PRAC and ABO not supported; 1b: PRAC and ABO supported	
Per Row Activation Counting and Alert Back-Off Enable/Disable	R/W	OP[1]	0b: Disable PRAC and ABO (default); 1b: Enable PRAC and ABO	2
Activation Counter Initialization	R/W	OP[2]	0b: Normal operating mode (default); 1b: Initialization mode	2
Activation Counter Initialization Complete	R	OP[3]	0b: Initialization not completed; 1b: Initialization completed	2
RFU	RFU	OP[4]	RFU	
Alert Back-Off Flag	R	OP[5]	0b: Clear; 1b: Source of ALERT_n	1
ALERT_n Verification Support (optional)	R	OP[6]	0b: ALERT_n verification not supported; 1b ALERT_n verification supported	

Function	Type	OP	Description/Data	Notes
ALERT_n Verification	R/W	OP[7]	0b: ALERT_n verification disabled (default); 1b ALERT_n verification trigger	

- Notes: 1. MR14:OP[3:0] applies to CID[3:0] for 3DS devices and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR70:OP[5] Alert Back-Off Flag source.
2. When PRAC is disabled, MR70:OP[1]=0b, both MR70:OP[2] and MR70:OP[3] are reset to the default 0b by the device. Likewise, when ACI is enabled, MR70:OP[2]=01b, MR70:OP[3] is reset to 0b by the device.

MR71 PRAC, ABO

Table 92: MR71 Register and OP-Code Bit Definitions (MA[7:0] = 47h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	PRAC Testing Initialization	PRAC Testing Enable/Disable	PRAC Testing Support (Optional)	Adaptive Per-Row Activation Counting		Min RFMab Commands During Recovery Period (ABO_RFM) and Min ACT commands during Alert Back-Off Delay (ABO_Delay)	

Function	Type	OP	Description/Data	Notes
Min RFMab Commands during Recovery Period (ABO_RFM) and min ACT commands during Alert Back-Off Delay (ABO_Delay)	R/W	OP[1:0]	00b: 4 (default); 01b: 2; 10b: 1; 11b: RFU	
Adaptive Per-Row Activation Counting	R/W	OP[3:2]	00b: Default mitigation threshold (default); 01b: Mitigation threshold level A; 10b: Mitigation threshold level B; 11b: Mitigation threshold level C	
PRAC Testing Support (Optional)	R	OP[4]	0b: PRAC testing not supported; 1b: PRAC testing supported	
PRAC Testing Enable/Disable	R/W	OP[5]	0b: Disable PRAC testing (default); 1b: Enable PRAC testing	
PRAC Testing Initialization	R/W	OP[6]	0b: Disable PRAC testing initialization (default); 1b: Enable PRAC testing	
RFU	RFU	OP[7]	RFU	

MR72 Counter Address/Counter Error Flag

Table 93: MR72 Register and OP-Code Bit Definitions (MA[7:0] = 48h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU						Counter Address Report Flag	Counter Error Flag

Function	Type	OP	Description/Data	Notes
Counter Error Flag	R/W	OP[0]	0b: Clear; 1b: Counter error detected	
Counter Address Report Flag	R/W	OP[1]	0b: Clear; 1b: Failing row address available in MR73-MR75	
RFU	RFU	OP[7:2]	RFU	

MR73 Activation Counter Error Row Address [7:0]

Table 94: MR73 Register and OP-Code Bit Definitions (MA[7:0] = 49h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Activation Counter Error Row Address R[7:0]							

Function	Type	OP	Description/Data	Notes
8 bits of the row address	R	OP[7:0]	Activation counter error row address	1

Note: 1. MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR73 through MR75 Activation Counter Error address data.

MR74 Activation Counter Error Row Address [15:0]

Table 95: MR74 Register and OP-Code Bit Definitions (MA[7:0] = 4ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Activation Counter Error Row Address R[15:8]							

Function	Type	OP	Description/Data	Notes
8 bits of the row address	R	OP[7:0]	Activation counter error row address	1

Note: 1. MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR73 through MR75 Activation Counter Error address data.

MR75 Activation Counter Error

Table 96: MR75 Register and OP-Code Bit Definitions (MA[7:0] = 4bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	Activation Counter Error Row Bank Group BG[2:0]			Activation Counter Error Row Bank Address BA[1:0]		Activation Counter Error Row Address R[17:16]	

Function	Type	OP	Description/Data	Notes
2 bits of the row address	R	OP[1:0]	Activation counter error row address R[17:16]	1
2 bits of the bank address	R	OP[3:2]	Activation counter error row bank address BA[1:0]	1
3 bits of the bank group	R	OP[6:4]	Activation counter error row bank group BG[2:0]	1
RFU	RFU	OP[7]	RFU	

Note: 1. MR14:OP[3:0] applies to CID[3:0] for 3DS-DDR5 and must be setup to indicate which slice in the 3DS-DDR5 stack is referenced in the MR73 through MR75 Activation Counter Error address data.

MR76–102 RFU

Mode registers between M76 and MR102 are undefined.

Mode Register Definitions for Decision Feedback Equalization

The following mode registers are used to configure the Decision Feedback Equalization (DFE), Per Bit Duty Cycle Adjuster, and Per Bit VREFDQ feature. These mode registers (MA[7:0]=70-FFh) are organized in a way such that those used for programming DFE, DCA and VREFDQ configuration per DQ or DM are grouped together. For example:

DQL0 starts at MA[7:0]=80h,

DQL1 starts at MA[7:0]=88h,

...

DQU6 starts at MA[7:0]=F0h,

DQU7 starts at MA[7:0]=F8h

Looking further into the 8-bit binary encoding, MA[6:3] is defined as a direct mapping for DQL0 to DQU7. For example:

MA[7:0]=1000:0XXXb for DQ0,

MA[7:0]=1000:1XXXb for DQ1,

...

MA[7:0]=1111:0XXXb for DQU6

MA[7:0]=1111:1XXXb for DQU7

Additional notes for MR112–MR116:

1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values and range are speed-dependent.

Table 97: Visual Representation of DFE, Per Bit DCA and Per Bit VREFDQ Mode Register Mapping

MRW Address, Binary	Function	MRW Address Bits [2:0]							
		000b	001b	010b	011b	100b	101b	110b	111b
0111 0XXX	DML	Gain	Tap1	Tap2	Tap3	Tap4	MR address space not currently used		
0111 1XXX	DMU								
1000 0XXX	DQL0								
1000 1XXX	DQL1								
1001 0XXX	DQL2								
1001 1XXX	DQL3								
1010 0XXX	DQL4								
1010 1XXX	DQL5								
1011 0XXX	DQL6								
1011 1XXX	DQL7								
1100 0XXX	DQU0								
1100 1XXX	DQU1								
1101 0XXX	DQU2								
1101 1XXX	DQU3								
1110 0XXX	DQU4								
1110 1XXX	DQU5								
1111 0XXX	DQU6								
1111 1XXX	DQU7								

MR103-MR254

MR103 DQSL_t DCA for IBCLK and QCLK

Table 98: MR103 Register and OP-Code Bit Definitions (MA[7:0] = 67h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSL_t IBCLK sign	RFU	DQSL_t DCA for IBCLK		DQSL_ t QCLK sign	RFU	DQSL_t DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSL_t DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL_t QCLK sign	W	OP[3]	0b=positive (default), 1b=negative	1
DQSL_t DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQSL_t IBCLK sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR104 DQSL_t DCA for QBCLK

Table 99: MR104 Register and OP-Code Bit Definitions (MA[7:0] = 68h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSL _t QBCLK sign	RFU	DQSL _t DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSL _t DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL _t QBCLK sign	W	OP[3]	0b=positive (default), 1b=negative	
RFU	RFU	OP[7:4]	RFU	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR105 DQSL_c DCA fro IBCLK and QCLK

Table 100: MR105 Register and OP-Code Bit Definitions (MA[7:0] = 69h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSL _c IBCLK sign	RFU	DQSL _c DCA for IBCLK		DQSL _c QCLK sign	RFU	DQSL _c DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSL _c DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL _c QCLK sign	W	OP[3]	0b=positive (default), 1b=negative	
DQSL _c DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQSL _c IBCLK sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR106 DQSL_c DCA for QBCLK

Table 101: MR106 Register and OP-Code Bit Definitions (MA[7:0] = 6Ah)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSL _c QBCLK sign	RFU	DQSL _c DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSL _c DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSL _c QBCLK sign	W	OP[3]	0b=positive (default), 1b=negative	
RFU	RFU	OP[7:4]	RFU	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR107 DQSU_t DCA for IBCLK and QCLK

Table 102: MR107 Register and OP-Code Bit Definitions (MA[7:0] = 6Bh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSU_t IBCLK sign	RFU	DQSU_t DCA for IBCLK		DQSU_t QCLK sign	RFU	DQSU_t DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSU_t DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_t QCLK sign	W	OP[3]	0b=positive (default), 1b=negative	1
DQSU_t DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQSU_t IBCLK sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR108 DQSU_t DCA for QBCLK

Table 103: MR108 Register and OP-Code Bit Definitions (MA[7:0] = 6Ch)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSU_t QBCLK sign	RFU	DQSU_t DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSU_t DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_t QBCLK sign	W	OP[3]	0b=positive (default), 1b=negative	1
RFU	RFU	OP[7:4]	RFU	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR109 DQSU_c DCA for IBCLK and QCLK

Table 104: MR108 Register and OP-Code Bit Definitions (MA[7:0] = 6Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQSU_c IBCLK sign	RFU	DQSU_c DCA for IBCLK		DQSU_c QCLK sign	RFU	DQSU_c DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQSU_c DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_c QCLK sign	W	OP[3]	0b=positive (default), 1b=negative	1
DQSU_c DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	
RFU	RFU	OP[6]	RFU	

Function	Type	OP	Description/Data	Notes
DQSU_c IBCK sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR110 DQSU_c DCA for QBCLK

Table 105: MR110 Register and OP-Code Bit Definitions (MA[7:0] = 6Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DQSU_c QBCLK sign	RFU	DQSU_c DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQSU_c DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQSU_c QBCLK sign	W	OP[3]	0b=positive (default), 1b=negative	
RFU	RFU	OP[7:4]	RFU	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR111 Global DFE Enable

Table 106: MR111 Register and OP-Code Bit Definitions (MA[7:0] = 6Fh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			Global DFE Tap-4 Enable	Global DFE Tap-3 Enable	Global DFE Tap-2 Enable	Global DFE Tap-1 Enable	Global DFE Gain Enable

Function	Type	OP	Description/Data	Notes
Global DFE Gain Enable	R/W	OP[0]	0b=DFE Gain Enable (default), 1b=DFE Gain Disable	1
Global DFE Tap-1 Enable	R/W	OP[1]	0b=DFE Tap-1 Enable (default), 1b=DFE Tap-1 Disable	1
Global DFE Tap-2 Enable	R/W	OP[2]	0b=DFE Tap-2 Enable (default), 1b=DFE Tap-2 Disable	1
Global DFE Tap-3 Enable	R/W	OP[3]	0b=DFE Tap-3 Enable (default), 1b=DFE Tap-3 Disable	1
Global DFE Tap-4 Enable	R/W	OP[4]	0b=DFE Tap-4 Enable (default), 1b=DFE Tap-4 Disable	1
RFU	RFU	OP[7:5]	RFU	

Notes: 1. This bit applies to all DM and DQ pins.
2. Setting MR111: OP[4:0]=11111b disables the DFE.

MR112 DML DFE Gain Bias

The MR112 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Gain Bias. Additional MRs for DFE Gain Bias are positioned every 8 MRs (MR112, MR120, MR128, etc.) until all pins are covered.

Table 107: MR112 Register and OP-Code Bit Definitions (MA[7:0] = 70h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Sign Bit Gain Bias	DFE Gain Bias		

Function	Type	OP	Description/Data	Notes
DFE Gain Bias	R/W	OP[2:0]	000b: DFE Gain Bias step 0 (default), 001b: DFE Gain Bias step 1, 010b: DFE Gain Bias step 2, 011b: DFE Gain Bias step 3, 100b–111b=RFU	1,2,3
Sign Bit Gain Bias	R/W	OP[3]	0b: positive DFE Gain Bias (default), 1b: negative DFE Gain Bias	
RFU	RFU	OP[7:4]	RFU	

Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.

2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.

3. The number of step size, step values, and range are speed-dependent.

4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR113 DML DFE Tap-1 Bias

The MR113 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-1.

Additional MRs for DFE Tap-1 settings are positioned every 8 MRs (MR113, MR121, MR129, etc.) until all pins are covered.

Table 108: MR113 Register and OP-Code Bit Definitions (MA[7:0] = 71h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 1 Bias	Sign Bit DFE Tap 1 Bias	DFE Tap 1 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 1 Bias	R/W	OP[5:0]	000000b=DFE Tap-1 Bias Step +0 (default), 000001b=DFE Tap-1 Bias Step +1, 000010b=DFE Tap-1 Bias Step +2, 000011b=DFE Tap-1 Bias Step +3, 000100b=DFE Tap-1 Bias Step +4, 000101b=DFE Tap-1 Bias Step +5, ... 100101b=DFE Tap-1 Bias Step +38, 100110b=DFE Tap-1 Bias Step +39, 101000b=DFE Tap-1 Bias Step +40, 101001b–111111b=RFU	
Sign Bit DFE Tap 1 Bias	R/W	OP[6]	0b=positive DFE Tap-1 Bias (default), 1b=negative DFE Tap-1 Bias	
Enable/Disable DFE Tap 1 Bias	R/W	OP[7]	0b=DFE Tap-1 disable (default), 1b=DFE Tap-1 enable	

Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.

2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.

3. The number of step size, step values, and range are speed-dependent.

4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR114 DML DFE Tap-2 Bias

The MR114 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-2.

Additional MRs for DFE Tap-2 settings are positioned every eight MRs (MR114, MR122, MR130, etc) until all pins are covered.

Table 109: MR114 Register and OP-Code Bit Definitions (MA[7:0] = 72h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 2 Bias	Sign Bit DFE Tap 2 Bias	DFE Tap 2 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 2 Bias	R/W	OP[5:0]	000000b=DFE Tap-2 Bias Step +0 (default), 000001b=DFE Tap-2 Bias Step +1, 000010b=DFE Tap-2 Bias Step +2, 000011b=DFE Tap-2 Bias Step +3, 000100b=DFE Tap-2 Bias Step +4, 000101b=DFE Tap-2 Bias Step +5, ... 001011b=DFE Tap-2 Bias Step +13, 001110b=DFE Tap-2 Bias Step +14, 001111b=DFE Tap-2 Bias Step +15, 0100000b-111111b=RFU	
Sign Bit DFE Tap 2 Bias	R/W	OP[6]	0b=positive DFE Tap-2 Bias (default), 1b=negative DFE Tap-2 Bias	
Enable/Disable DFE Tap 2 Bias	R/W	OP[7]	0b=DFE Tap-2 disable (default), 1b=DFE Tap-2 enable	

- Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.
2. The number of step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values, and range are speed-dependent.
4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR115 DML DFE Tap-3 Bias

The MR115 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-3. Additional MRs for DFE TAP-3 settings are positioned every eight MRs (MR115, MR123, MR131, etc) until all pins are covered.

Table 110: MR115 Register and OP-Code Bit Definitions (MA[7:0] = 73h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 3 Bias	Sign Bit DFE Tap 3 Bias	DFE Tap 3 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 3 Bias	R/W	OP[5:0]	000000b=DFE Tap-3 Bias Step +0 (default), 000001b=DFE Tap-3 Bias Step +1, 000010b=DFE Tap-3 Bias Step +2, 000011b=DFE Tap-3 Bias Step +3, 000100b=DFE Tap-3 Bias Step +4, 000101b=DFE Tap-3 Bias Step +5, ... 001010b=DFE Tap-3 Bias Step +10, 001011b=DFE Tap-3 Bias Step +11, 001100b=DFE Tap-3 Bias Step +12, 001101b-111111b=RFU	1,2,3
Sign Bit DFE Tap 3 Bias	R/W	OP[6]	0b=positive DFE Tap-3 Bias (default), 1b=negative DFE Tap-3 Bias	
Enable/Disable DFE Tap 3 Bias	R/W	OP[7]	0b=DFE Tap-3 disable (default), 1b=DFE Tap-3 enable	

- Notes: 1. Refer to the DDR5 DFE specification for information on step size, step size tolerance and range values.
2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.
3. The number of step size, step values, and range are speed-dependent.

4. Setting all DFE gain bias bits (in MR112, MR120, MR128, ... MR248 OP[3:0]=0000b and MR113-MR116, MR121-MR124, MR129-MR132, ... MR249-MR152 OP[8:0]=00000000b) disables the DFE.

MR116 DML DFE Tap-4 Bias

The MR116 definition covers registers for DML, DMU, DQL[7:0], and DQU[7:0] for DFE Tap-4. Additional MRs for DFE TAP-4 settings are positioned every eight MRs (MR116, MR124, MR132, etc) until all pins are covered.

Table 111: MR116 Register and OP-Code Bit Definitions (MA[7:0] = 74h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Enable/ Disable DFE Tap 4 Bias	Sign Bit DFE Tap 4 Bias	DFE Tap 4 Bias					

Function	Type	OP	Description/Data	Notes
DFE Tap 4 Bias	R/W	OP[5:0]	000000b=DFE Tap-4 Bias Step +0 (default), 000001b=DFE Tap-4 Bias Step +1, 000010b=DFE Tap-4 Bias Step +2, 000011b=DFE Tap-4 Bias Step +3, 000100b=DFE Tap-4 Bias Step +4, 000101b=DFE Tap-4 Bias Step +5, 000110b=DFE Tap-4 Bias Step +6, 000111b=DFE Tap-4 Bias Step +7, 001000b=DFE Tap-4 Bias Step +8, 001001b=DFE Tap-4 Bias Step+9, 001010b-111111b=RFU	1,2,3
Sign Bit DFE Tap 4 Bias	R/W	OP[6]	0b=positive DFE Tap-4 Bias (default), 1b=negative DFE Tap-4 Bias	
Enable/Disable DFE Tap 4 Bias	R/W	OP[7]	0b=DFE Tap-4 disable (default), 1b=DFE Tap-4 enable	

Notes: 1. Refer to the DFE specification for information on step size, step size tolerance and range values.

2. The step size and step values are related to the min/max ranges specified in the DFE Gain Adjustment and Tap Coefficient tables.

3. The number of step size, step values and range are speed-dependent.

MR118 DML V_{REFDQ} Offset

Table 112: MR118 Register and OP-Code Bit Definitions (MA[7:0] = 76h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DML V_{REFDQ} Sign	DML V_{REFDQ} Offset			RFU			

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[3:0]	RFU	
DML V_{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 001b=step+1, 010b=step+2, 011b=step+3, 100b-111b=RFU	1
DML V_{REFDQ} sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR126 DMU V_{REFDQ} Offset

Table 113: MR126 Register and OP-Code Bit Definitions (MA[7:0] = 7Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DMU V_{REFDQ} Sign	DMU V_{REFDQ} Offset			RFU			

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[3:0]	RFU	
DMU V_{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 001b=step+1, 010b=step+2, 011b=step+3, 100b-111b=RFU	1
DMU V_{REFDQ} sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR133 DQL0 DCA for IBCLK and QCLK

Table 114: MR133 Register and OP-Code Bit Definitions (MA[7:0] = 85h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL0 IBCLK Sign	RFU	DQL0 DCA for IBCLK		DQL0 QCLK Sign	RFU	DQL0 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL0 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL0 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL0 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQL0 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR134 DQL0 DCA for QBCLK and DQL0 V_{REFDQ} Offset

Table 115: MR134 Register and OP-Code Bit Definitions (MA[7:0] = 86h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL0 V_{REFDQ} Sign	DQL0 V_{REFDQ} Offset			DQL0 QBCLK Sign	RFU	DQL0 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL0 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL0 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL0 V_{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
DQL0 V_{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR141 DQL1 DCA for IBCLK and QCLK

Table 116: MR141 Register and OP-Code Bit Definitions (MA[7:0] = 8Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL1 IBCLK Sign	RFU	DQL1 DCA for IBCLK		DQL1 QCLK Sign	RFU	DQL1 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL1 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQL1 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL1 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQL1 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR142 DQL1 DCA for QBCLK and DQL1 V_{REFDQ} Offset

Table 117: MR142 Register and OP-Code Bit Definitions (MA[7:0] = 8Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL1 V _{REFDQ} Sign	DQL1 V _{REFDQ} Offset			DQL1 QBCLK Sign	RFU	DQL1 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL1 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQL1 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL1 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
DQL1 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR149 DQL2 DCA for IBCLK and QCLK

Table 118: MR149 Register and OP-Code Bit Definitions (MA[7:0] = 95h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL2 IBCLK Sign	RFU	DQL2 DCA for IBCLK		DQL2 QCLK Sign	RFU	DQL2 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL2 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQL2 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL2 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQL2 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR150 DQL2 DCA for QBCLK and DQL2 V_{REFDQ} Offset

Table 119: MR150 Register and OP-Code Bit Definitions (MA[7:0] = 96h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL2 V_{REFDQ} Sign	DQL2 V_{REFDQ} Offset			DQL2 QBCLK Sign	RFU	DQL2 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL2 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL2 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL2 V_{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
DQL2 V_{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR157 DQL3 DCA for IBCLK and QCLK

Table 120: MR157 Register and OP-Code Bit Definitions (MA[7:0] = 9Dh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL3 IBCLK Sign	RFU	DQL3 DCA for IBCLK		DQL3 QCLK Sign	RFU	DQL3 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL3 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL3 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL3 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQL3 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR158 DQL3 DCA for QBCLK and DQL3 V_{REFDQ} Offset

Table 121: MR158 Register and OP-Code Bit Definitions (MA[7:0] = 9Eh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL3 V_{REFDQ} Sign	DQL3 V_{REFDQ} Offset			DQL3 QBCLK Sign	RFU	DQL3 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL3 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL3 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL3 V_{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1

Function	Type	OP	Description/Data	Notes
DQL3 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR165 DQL4 DCA for IBCLK and QCLK

Table 122: MR165 Register and OP-Code Bit Definitions (MA[7:0] = A5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL4 IBCLK Sign	RFU	DQL4 DCA for IBCLK		DQL4 QCLK Sign	RFU	DQL4 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL4 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL4 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL4 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQL4 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR166 DQL4 DCA for QBCLK and DQL4 V_{REFDQ} Offset

Table 123: MR166 Register and OP-Code Bit Definitions (MA[7:0] = A6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL4 V _{REFDQ} Sign	DQL4 V _{REFDQ} Offset			DQL4 QBCLK Sign	RFU	DQL4 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL4 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL4 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL4 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
DQL4 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR173 DQL5 DCA for IBCLK and QCLK

Table 124: MR173 Register and OP-Code Bit Definitions (MA[7:0] = ADh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL5 IBCLK Sign	RFU	DQL5 DCA for IBCLK		DQL5 QCLK Sign	RFU	DQL5 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL5 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[2]	RFU	
DQL5 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL5 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQL5 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR174 DQL5 DCA for QBCLK and DQL5 V_{REFDQ} Offset

Table 125: MR174 Register and OP-Code Bit Definitions (MA[7:0] = AEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL5 V _{REFDQ} Sign	DQL5 V _{REFDQ} Offset			DQL5 QBCLK Sign	RFU	DQL5 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL5 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQL5 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL5 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3, 100b-111b=RFU	1
DQL5 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR181 DQL6 DCA for IBCLK and QCLK

Table 126: MR181 Register and OP-Code Bit Definitions (MA[7:0] = B5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL6 IBCLK Sign	RFU	DQL6 DCA for IBCLK		DQL6 QCLK Sign	RFU	DQL6 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL6 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQL6 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL6 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQL6 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR182 DQL6 DCA for QBCLK and DQL6 V_{REFDQ} Offset

Table 127: MR182 Register and OP-Code Bit Definitions (MA[7:0] = B6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL6 V _{REFDQ} Sign	DQL6 V _{REFDQ} Offset			DQL6 QBCLK Sign	RFU	DQL6 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL6 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL6 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL6 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1
DQL6 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR189 DQL7 DCA for IBCLK and QCLK

Table 128: MR189 Register and OP-Code Bit Definitions (MA[7:0] = BDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL7 IBCLK Sign	RFU	DQL7 DCA for IBCLK		DQL7 QCLK Sign	RFU	DQL7 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQL7 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL7 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL7 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQL7 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR190 DQL7 DCA for QBCLK and DQL7 V_{REFDQ} Offset

Table 129: MR190 Register and OP-Code Bit Definitions (MA[7:0] = BEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQL7 V _{REFDQ} Sign	DQL7 V _{REFDQ} Offset			DQL7 QBCLK Sign	RFU	DQL7 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQL7 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQL7 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQL7 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1

Function	Type	OP	Description/Data	Notes
DQL7 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR197 DQU0 DCA for IBCLK and QCLK

Table 130: MR197 Register and OP-Code Bit Definitions (MA[7:0] = C5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU0 IBCLK Sign	RFU	DQU0 DCA for IBCLK		DQU0 QCLK Sign	RFU	DQU0 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU0 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU0 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU0 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQU0 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR198 DQU0 DCA for QBCLK and DQU0 V_{REFDQ} Offset

Table 131: MR198 Register and OP-Code Bit Definitions (MA[7:0] = C6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU0 V _{REFDQ} Sign	DQU0 V _{REFDQ} Offset			DQU0 QBCLK Sign	RFU	DQU0 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU0 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU0 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU0 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1
DQU0 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR205 DQU1 DCA for IBCLK and QCLK

Table 132: MR205 Register and OP-Code Bit Definitions (MA[7:0] = CDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU1 IBCLK Sign	RFU	DQU1 DCA for IBCLK		DQU1 QCLK Sign	RFU	DQU1 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU1 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[2]	RFU	
DQU1 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU1 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQU1 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR206 DQU1 DCA for QBCLK and DQU1 V_{REFDQ} Offset

Table 133: MR206 Register and OP-Code Bit Definitions (MA[7:0] = CEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU1 V _{REFDQ} Sign	DQU1 V _{REFDQ} Offset			DQU1 QBCLK Sign	RFU	DQU1 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU1 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQU1 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU1 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3, 100b-111b=RFU	1
DQU1 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR213 DQU2 DCA for IBCLK and QCLK

Table 134: MR213 Register and OP-Code Bit Definitions (MA[7:0] = D5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU2 IBCLK Sign	RFU	DQU2 DCA for IBCLK		DQU2 QCLK Sign	RFU	DQU2 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU2 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQU2 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU2 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQU2 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR214 DQU2 DCA for QBCLK and DQU2 V_{REFDQ} Offset

Table 135: MR214 Register and OP-Code Bit Definitions (MA[7:0] = D6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU2 V _{REFDQ} Sign	DQU2 V _{REFDQ} Offset			DQU2 QBCLK Sign	RFU	DQU2 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU2 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU2 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU2 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1
DQU2 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR221 DQU3 DCA for IBCLK and QCLK

Table 136: MR221 Register and OP-Code Bit Definitions (MA[7:0] = DDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU3 IBCLK Sign	RFU	DQU3 DCA for IBCLK		DQU3 QCLK Sign	RFU	DQU3 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU3 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU3 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU3 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQU3 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR222 DQU3 DCA for QBCLK and DQU3 V_{REFDQ} Offset

Table 137: MR222 Register and OP-Code Bit Definitions (MA[7:0] = DEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU3 V _{REFDQ} Sign	DQU3 V _{REFDQ} Offset			DQU3 QBCLK Sign	RFU	DQU3 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU3 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU3 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU3 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1

Function	Type	OP	Description/Data	Notes
DQU3 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR229 DQU4 DCA for IBCLK and QCLK

Table 138: MR229 Register and OP-Code Bit Definitions (MA[7:0] = E5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU4 IBCLK Sign	RFU	DQU4 DCA for IBCLK		DQU4 QCLK Sign	RFU	DQU4 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU4 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU4 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU4 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQU4 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR230 DQU4 DCA for QBCLK and DQU4 V_{REFDQ} Offset

Table 139: MR230 Register and OP-Code Bit Definitions (MA[7:0] = E6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU4 V _{REFDQ} Sign	DQU4 V _{REFDQ} Offset			DQU4 QBCLK Sign	RFU	DQU4 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU4 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU4 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU4 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1
DQU4 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR237 DQU5 DCA for IBCLK and QCLK

Table 140: MR237 Register and OP-Code Bit Definitions (MA[7:0] = EDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU5 IBCLK Sign	RFU	DQU5 DCA for IBCLK		DQU5 QCLK Sign	RFU	DQU5 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU5 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1

Function	Type	OP	Description/Data	Notes
RFU	RFU	OP[2]	RFU	
DQU5 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU5 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQU5 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR238 DQU5 DCA for QBCLK and DQU5 V_{REFDQ} Offset

Table 141: MR238 Register and OP-Code Bit Definitions (MA[7:0] = EEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU5 V _{REFDQ} Sign	DQU5 V _{REFDQ} Offset			DQU5 QBCLK Sign	RFU	DQU5 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU5 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQU5 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU5 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3, 100b-111b=RFU	1
DQU5 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR245 DQU6 DCA for IBCLK and QCLK

Table 142: MR245 Register and OP-Code Bit Definitions (MA[7:0] = F5h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU6 IBCLK Sign	RFU	DQU6 DCA for IBCLK		DQU6 QCLK Sign	RFU	DQU6 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU6 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[2]	RFU	
DQU6 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU6 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step +3	1
RFU	RFU	OP[6]	RFU	
DQU6 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR246 DQU6 DCA for QBCLK and DQU6 V_{REFDQ} Offset

Table 143: MR246 Register and OP-Code Bit Definitions (MA[7:0] = F6h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU6 V _{REFDQ} Sign	DQU6 V _{REFDQ} Offset			DQU6 QBCLK Sign	RFU	DQU6 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU6 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU6 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU6 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1
DQU6 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR253 DQU7 DCA for IBCLK and QCLK

Table 144: MR253 Register and OP-Code Bit Definitions (MA[7:0] = FDh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU7 IBCLK Sign	RFU	DQU7 DCA for IBCLK		DQU7 QCLK Sign	RFU	DQU7 DCA for QCLK	

Function	Type	OP	Description/Data	Notes
DQU7 DCA for QCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU7 QCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU7 DCA for IBCLK	W	OP[5:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[6]	RFU	
DQU7 IBCLK Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

MR254 DQU7 DCA for QBCLK and DQU7 V_{REFDQ} Offset

Table 145: MR254 Register and OP-Code Bit Definitions (MA[7:0] = FEh)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQU7 V _{REFDQ} Sign	DQU7 V _{REFDQ} Offset			DQU7 QBCLK Sign	RFU	DQU7 DCA for QBCLK	

Function	Type	OP	Description/Data	Notes
DQU7 DCA for QBCLK	W	OP[1:0]	00b=disable (default), 01b=step+1, 10b=step+2, 11b=step+3	1
RFU	RFU	OP[2]	RFU	
DQU7 QBCLK Sign	W	OP[3]	0b=positive (default), 1b=negative	
DQU7 V _{REFDQ} Offset	W	OP[6:4]	00b=disable (default), 01b=step +1, 10b=step+2, 11b=step+3, 100b-111b=RFU	1

Function	Type	OP	Description/Data	Notes
DQU7 V _{REFDQ} Sign	W	OP[7]	0b=positive (default), 1b=negative	

Note: 1. Range: -3 ~ +3 LSB codes; step size: 1LSB.

Command Description and Operation

Notes 1, 2, and 14 apply to the entire table.

To improve command decode time, the table has been optimized to orient all 1-cycle commands together and all 2-cycle commands together; enabling CA1 to be used to identify the difference between a 1-cycle and a 2-cycle command.

Table 146: Command Truth Table

Function	Abv.	CS	CA Pins														Note
			CA 0	CA 1	CA 2	CA 3	CA 4	CA 5	CA 6	CA 7	CA 8	CA 9	CA 10	CA 11	CA 12	CA 13	
Activate	ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,17,20
		H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/R17	
Reserved	REXT	L	L	H	Reserved												
		H	Reserved														
RFU	RFU	L	H	L	L	L	L	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
RFU	RFU	L	H	L	L	L	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Write Pattern (Zero)	WRP	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,15,18,19,20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP=H	H	V	CID3	
Write Pattern w/Auto Precharge	WRPA	L	H	L	L	H	L	H	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	11,15,18,19,20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	AP=L	H	V	CID3	
RFU	RFU	L	H	L	L	H	H	V	V	V	V	V	V	V	V	V	
		H	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Mode Register Write	MRW	L	H	L	H	L	L	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	11,13
		H	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V	V	CW	V	V	V	
Mode Register Read	MRR	L	H	L	H	L	H	MRA0	MRA1	MRA2	MRA3	MRA4	MRA5	MRA6	MRA7	V	8,13,21,22
		H	L	L	V	V	V	V	V	V	V	V	CW	V	V	V	
Mode Register Read NT	MRR-NT	L	H	L	H	L	H	V	V	V	V	V	V	V	V	V	8,21,22
		L	L	L	V	V	V	V	V	V	V	V	V	V	V	V	
Write	WR	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,12,15,19,20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	H	WR_P=L	V	CID3	
Write Auto Precharge	WRA	L	H	L	H	H	L	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,12,15,19,20
		H	V	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	L	WR_P=L	V	CID3	
Write NT	WR-NT	L	H	L	H	H	L	BL*=L	V	V	V	V	V	V	V	V	8,12,15,19
		L	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Read	RD	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,15,19,20
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	V	V	CID3	

Table 146: Command Truth Table (Continued)

Function	Abv.	CS	CA Pins														Note	
			CA 0	CA 1	CA 2	CA 3	CA 4	CA 5	CA 6	CA 7	CA 8	CA 9	CA 10	CA 11	CA 12	CA 13		
Read Auto Precharge	RDA	L	H	L	H	H	H	BL*=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	8,15, 19,20	
		H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V or DRFM=L	L	V	V	CID3		
Read NT	RD-NT	L	H	L	H	H	H	BL*=L	V	V	V	V	V	V	V	V	V	8,15, 19
		L	V	V	V	V	V	V	V	V	V	V	V	V	V	V		
VREF CA command	VrefCA	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7=L	V		
VREF CS command	VreCS	L	H	H	L	L	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7=H	V		
Refresh All	REFab	L	H	H	L	L	H	CID3	V	V	V or RIR	V or H	L	CID0	CID1	CID2	3,20, 23,24	
Refresh Managem ent All	RFMab	L	H	H	L	L	H	CID3 or DRFM-L	V	V	V	L	L	CID0	CID1	CID2	3,20, 23	
Refresh Same Bank	REFsb	L	H	H	L	L	H	CID3	BA0	BA1	V or RIR	V or H	H	CID0	CID1	CID2	4,20, 23,24	
Refresh Managem ent Same Bank	RFMsb	L	H	H	L	L	H	CID3 or DRFM=L	B A	BA1	V	L	H	CID0	CID1	CID2	4,20, 23	
Precharge All Banks	PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2	5,20	
Precharge Same Bank	PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2	6,20	
Precharge	PREpb	L	H	H	L	H	H	CID3 or DRFM=L	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2	7,20	
Reserved Future Use	RFU	L	H	H	H	L	L	V	V	V	V	V	V	V	V	V		
Self Refresh Entry	SRE	L	H	H	H	L	H	V	V	V	V	H	L	V	V	V	9	
Self Refresh Entry w/ Frequency Change	SREF	L	H	H	H	L	H	V	V	V	V	L	L	V	V	V	9	
Power-Down Entry	PDE	L	H	H	H	L	H	V	V	V	V	V	H	ODT=L	V	V	10,16	
Multi Purpose Command	MPC	L	H	H	H	H	L	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	V		
No Operation	NOP	L	H	H	H	H	H	V	V	V	V	V	V	V	V	V	26	

Table 146: Command Truth Table (Continued)

Func- tion	Abv.	CS	CA Pins														Note
			CA 0	CA 1	CA 2	CA 3	CA 4	CA 5	CA 6	CA 7	CA 8	CA 9	CA 10	CA 11	CA 12	CA 13	
Deselect	DES	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

- Notes: 1. V=valid logic level HIGH or LOW. X=don't care, in which case the signal may be floated. BG=bank group address. BA=bank address. R=row address. C=column address. BL=burst length. MRA=mode register address. OP=op code. CID=chip ID. CW=control word. NT = non-target rank. RIR = refresh interval rate (if enabled, H state = 1X REF, L state = 2X REF).
- Bank group addresses BG[2:0] and bank addresses BA[1:0] determine which bank is to be operated upon in a specific bank group.
 - The REFRESH ALL and REFRESH MANAGEMENT ALL commands are applied to all banks in all bank groups. CA6, CA7 and CA8 are required to be valid (V). The bank addresses and bank group addresses are don't care.
 - The REFRESH SAME BANK and REFRESH MANAGEMENT SAME BANK commands refresh the same bank in all bank group bits. The bank bits, BA0 and BA1 on CA6 and CA7, respectively, specify the bank within each bank group.
 - The PRECHARGE ALL command applies to all open banks in all bank groups.
 - The PRECHARGE SAME BANK command applies to the same bank in all bank groups. The bank bits specify the bank within each bank group.
 - The PRECHARGE command applies to a single bank as specified by bank address and bank group bits.
 - CS=LOW during the second cycle of on-die terminating two-cycle WR, RD and MRR commands.
 - The SRE command places the device in self-refresh state.
 - The PDE command places the device in power-down state.
 - For two-cycle commands with no ODT control (ACT, MRW, WRP [Zero]), the command is not executed if the device receives CS as LOW on the second cycle (a command cancel).
 - WR command with WR_partial=LOW indicates a partial WRITE command. This is to help the device start an internal read for read modify writes.
 - If CW=LOW during the MRW command, the device executes the command and the mode register is written. If CW=HIGH, the device ignores the MRW command and the mode register is not changed. If CW=LOW, the device executes the MRR command. If CW=HIGH, the device may not execute the MRR command.
 - CID0-3 bits used for 3DS stacking die selection up to 16 high stacking support.
 - If CA5:BL*=LOW, device is placed into alternate burst mode (described in MR0:OP[1:0]) instead of the default burst length.
 - ODT=LOW is defined to enable ODT to persist when the device is in power-down mode.
 - CID[3]/R17 is a multimode pin enabling either 16-high 3DS with CID[3] bit usage or R17 for high-density monolithic usage. These usages are mutually exclusive.
 - The WRITE PATTERN and WRITE PATTERN WITH AUTO PRECHARGE commands support BL16 and BL32 (non-OTF) only.
 - When CID3 is not used, its CA decode is VALID.
 - In the case of a device where the density or stacking doesn't require CA[13], the ball location for that function (considering the state of MIR) must be connected to V_{DDQ}, and the device must decode CA[13]=L so that the proper selection of die and RA is provided.
 - CA0, CA1 encoded as LOW on second pulse to meet MRR requirements that only BL16 sequential burst order is supported for MRR command.
 - When the host issues MRR with CRC enabled, data is returned with CRC bit.
 - If the refresh management required bit is 0 (MR58:OP[0]=0), CA9 is only required to be valid (V) for a REF command, and the device will treat a RFM command as a REF command. If MR58:OP[0]=1, a REF command requires CA9=H.
 - If the refresh interval rate indicator bit is disabled (MR4:OP[3]=0) by the host, CA8 is only required to be valid (V). If the refresh interval rate indicator bit is enabled (MR4:OP[3]=1) by the host, the host is required to set CA8=H for REF commands issued at the 1X refresh interval rate and CA8=L for REF commands issued at the 2X refresh interval rate. If the host issues 2X REF commands with CA8=L while MR4:OP[3]=1, but the refresh rate requirement is 1X as determined internally by the device, the device may internally align to the 1X refresh rate.

25. For command truth table bits such as BG2, BA1, R16, R17, C10 and CID[3:0], which are unused based on a device's density, configuration width, and stacking options, the CA decode is defined as VALID when in these unused states.
26. Unlike DES, NOP is considered a valid command, and timing from a preceding valid command must satisfy any associated command timings.

2-Cycle Command Cancel

ACT, WRP, WRPA and MRW are 2-cycle commands without associated ODT control requirements. The device does not execute these 2-cycle commands if CS_n is LOW on the second cycle (command cancel).

If the RCD detects a parity error on the second cycle of 2-cycle command, the CS_n will remain LOW for both the first and second cycle of the command. If the command is either READ, WRITE, or MRR, it will be converted to non-target ODT in the DRAM. If the command is either ACT, WRP, WRPA, or MRW, the command will be canceled in the DRAM. COMMAND CANCEL is a result of CA parity error detected by the RCD, and is not issued by the host. The relationship between COMMAND CANCEL and the next valid command shall not be illegal. For example, MRR cannot be issued after a canceled ACT, even with $t_{\text{CMD\_cancel}}$ satisfied. In that case, the host is supposed to issue PRE before issuing MRR.

Figure 9: Command Cancel Timing Diagram

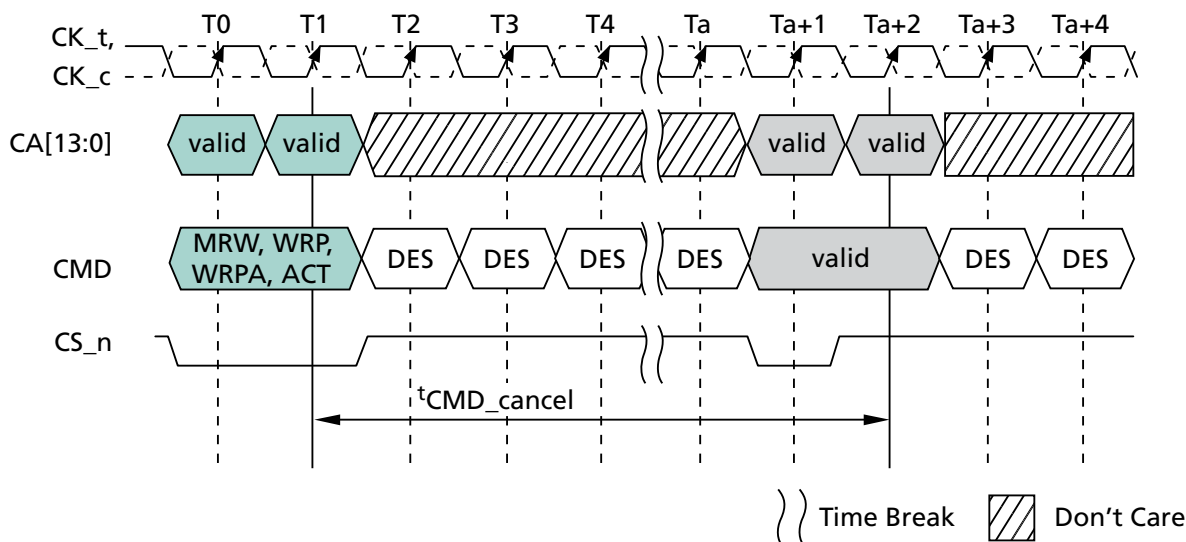


Table 147: Command Cancel Timing Parameters

Parameter	Symbol	3200-8800		Unit
		MIN	MAX	
Command cancel timing for ACT, WRP, WRPA, MRW when CS_n is LOW on second cycle	$t_{\text{CMD\_cancel}}$	8	-	nCK

CS_n Truth Table

This table outlines the CS_n status while the device is in power-down mode and self refresh mode and trying to exit. It is assumed that after the device enters self refresh mode, the driver switches to CMOS to conserve power while the device switches into a lower power receiver mode. When the device is coming out of reset either at power-up initialization or during a reset with stable power, there are important requirements on the CS_n signal (both prior to, and after, applying a stable clock); refer to the Power-up and Initialization section and the Reset Initialization with Stable Power section for details.

CS_n is ACTIVE LOW.

For more details of all signals, see the command truth table and corresponding sections for Power-down and Self Refresh Operation.

Table 148: CS_n Truth Table

Current State	CS_n			Command (N)	Next Command (N+1)	Action (N)	Note
	Previous Cycle (N-1) ¹	Current Cycle (N) ¹	Next Cycle (N+1) ¹				
Power-down	H	H	H	X	X	Maintain power-down mode	
	H	L	H	PDX (NOP)	DES	Power-down mode exit	2
Self refresh	L	L	L	X	X	Maintain self refresh mode	3
	See footnote and refer to Self Refresh Operation section for details					Self refresh mode exit	4
Reset	X	X	X	X	X	Maintain reset	5
	L	L	H	NOP	DES	Exit reset	6

Notes: 1. CS_n (N) is the logic state of CS_n at clock edge N; CS_n (N-1) is the state of CS_n at the previous clock edge, CS_n (N+1) is the logic state of CS_n at the next clock edge N+1.

- A single NOP cycle exits power-down mode; additional time is required after the exit before normal operation can resume.
- To maintain self refresh, CS_n must remain LOW.
- Self refresh exit is defined by the transition of CS_n LOW to HIGH with a defined pulse width ^tCSH_SRExit, followed by three or more NOP commands (^tCSL_SRExit) to ensure DRAM stability in recognizing the exit. See Self Refresh Operation section for more details.
- RESET_n is used exclusively for maintaining the device in RESET. CS only is needed to properly exit.
- Exiting RESET requires a stable clock and that ^tINIT5 is met with CS LOW and NOP on the CA bus followed by CS transitioning HIGH with NOP on the CA bus. CS remains HIGH for ^tCSH to allow the device CMOS receiver enough time to register the command.

MULTI-PURPOSE Command (MPC)

The MULTI-PURPOSE command (MPC) is used to issue commands associated with interface initialization, training, and periodic calibration. The MPC command is initiated with CS_n and CA[4:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has eight operands (OP[7:0] = CA[12:5]) that are decoded to execute specific commands.

The MPC command uses an encoding that includes the command encoding and the op-code payload in a single clock cycle. This enables the host to extend the setup and hold for the CA signals beyond the single cycle when the chip select asserts. In addition, the MPC command supports multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensure the device captures the MPC command during at least one rising CK_t/CK_c edge.

MPC Op-Codes

Table 149: MPC Function Definition for OP[7:0]

Function	MPC Mode	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Notes
Exit CS Training Mode	CSTMX	0	0	0	0	0	0	0	0	1,2,10
Enter CS Training Mode	CSTMN	0	0	0	0	0	0	0	1	1,2,10
DLL Reset	DLL RESET	0	0	0	0	0	0	1	0	1,10
Enter CA Training Mode	CATM	0	0	0	0	0	0	1	1	1,3,10
ZQCal Latch	ZQCLH	0	0	0	0	0	1	0	0	1,4,10
ZQCal Start	ZQCST	0	0	0	0	0	1	0	1	1,4,10
Stop DQS Interval Osc	DQSOSCSP	0	0	0	0	0	1	1	0	1,5,10
Start DQS Interval Osc	DQSOSCST	0	0	0	0	0	1	1	1	1,5,10
Set 2N Command Timing (default)	SET2N	0	0	0	0	1	0	0	0	1,10
Set 1N Command Timing	SET1N	0	0	0	0	1	0	0	1	1,10
Exit PDA Enumerate Program Mode	PDAENPX	0	0	0	0	1	0	1	0	1,6,10
Enter PDA Enumerate Program Mode	PDAENPE	0	0	0	0	1	0	1	1	1,6,10
Manual ECS Operation	ECS	0	0	0	0	1	1	0	0	1,10
RFU	RFU	0	0	0	0	1	1	0	1	1,10
RFU	RFU	0	0	0	0	1	1	1	0	1,10
Apply VREFCA, VREFCS and RTT_CA/CS/CK	REFRTTAP	0	0	0	1	1	1	1	1	1,8,10
Set Group A RTT_CK = xxx	RTTCKA	0	0	1	0	0	x	x	x	1,7,10
Set Group B RTT_CK = xxx	RTTCKB	0	0	1	0	1	x	x	x	1,7,10
Set Group A RTT_CS = xxx	RTTCSA	0	0	1	1	0	x	x	x	1,7,10
Set Group B RTT_CS = xxx	RTTCSB	0	0	1	1	1	x	x	x	1,7,10
Set Group A RTT_CA = xxx	RTTCAA	0	1	0	0	0	x	x	x	1,7,10
Set Group B RTT_CA = xxx	RTTCAB	0	1	0	0	1	x	x	x	1,7,10
Set DQS_RTT_PARK = xxx	DQSRTTPARK	0	1	0	1	0	x	x	x	1,10
Set RTT_PARK = xxx	RTTPARK	0	1	0	1	1	x	x	x	1,10
PDA Enumerate ID	PDAENID	0	1	1	0	x	x	x	x	1,9,10

Table 149: MPC Function Definition for OP[7:0] (Continued)

Function	MPC Mode	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Notes
PDA Select ID	PDASLID	0	1	1	1	x	x	x	x	1,9,10
Configure ^t DLLK/ ^t CCD_L	DLLKCCDL	1	0	0	0	x	x	x	x	1,10,11
CS Geardown Enable	CSGRDWNE	1	0	0	1	0	0	0	1	1,10
All Others Reserved	-	-	-	-	-	-	-	-	-	1,10

- Notes: 1. For more information on the MPC commands, see the Command Truth Table.
2. See the CS Training Mode section for more information regarding CS training mode entry and exit.
3. See the CA Training Mode section for more information regarding the CA training mode entry.
4. See the ZQ Calibration section for information regarding ZQCal Start and ZQCal Latch.
5. See the DQS Interval Oscillator section for more information regarding Start DQS Oscillator and Stop DQS Oscillator.
6. See the Per DRAM Addressability section for more information regarding Enter PDA and Exit PDA modes.
7. Refer to CA ODT Strap Operation for more information regarding Group A and Group B configurations for Set RTT_CA, Set RTT_CS, and Set RTT_CK.
8. APPLY VREFCA or VREFCS and RTT_CA/CS/CK applies the settings previously sent with the VREFCA or VREFCS command and MPC SET RTT_CA/CS/CK. Until this MPC APPLY VREFCA, VREFCS and RTT_CA/CS/CK command is sent, the values are in a shadow register. Any MRR to the VREFCA, VREFCS and RTT_CA/CS/CK settings should return only the applied value. The shadow register must retain the previously set value so that any time the MPC APPLY VREFCA, VREFCS and RTT_CA/CS/CK command is sent, there is no change in the applied value unless a new VREFCA, VREFCS or RTT_CA/CS/CK value was sent to the shadow register since the previous MPC APPLY VREFCA, VREFCS and RTT_CA/CS/CK command.
9. The PDA Enumerate ID and PDA Select ID op-codes include a 4-bit value, designated by xxxxb in the table. This is the value that is programmed into the MR for these fields. The PDA Enumerate ID can only be changed while in PDA Enumerate Programming mode.
10. For any MPC command that is associated with a mode register, the only way to program (write to) that mode register is via the MPC. Those mode registers are, therefore, read only and do not support MRW commands.
11. See MR13:OP[3:0] for encoding. The MPC ^tDLLK/^tCCD_L command sends the settings to the MR13:OP[3:0] shadow register and applies the settings to MR13 when the device encounters the DLL RESET command or SREF with CA9=L.
12. The MPC function DLL RESET requires ^tMPC_delay to all commands that do not require a locked DLL. ^tDLLK_min shall be satisfied prior to issuing any commands that require a locked DLL. REFab/REFsb/ RFMab/RFMsb must not be issued during ^tRFC1 after issuing the MPC DLL RESET function. See the Self Refresh Operation section for the full list of commands that require or do not require a locked DLL.

Table 150: PDA Enumerate ID and PDA Select ID Encoding

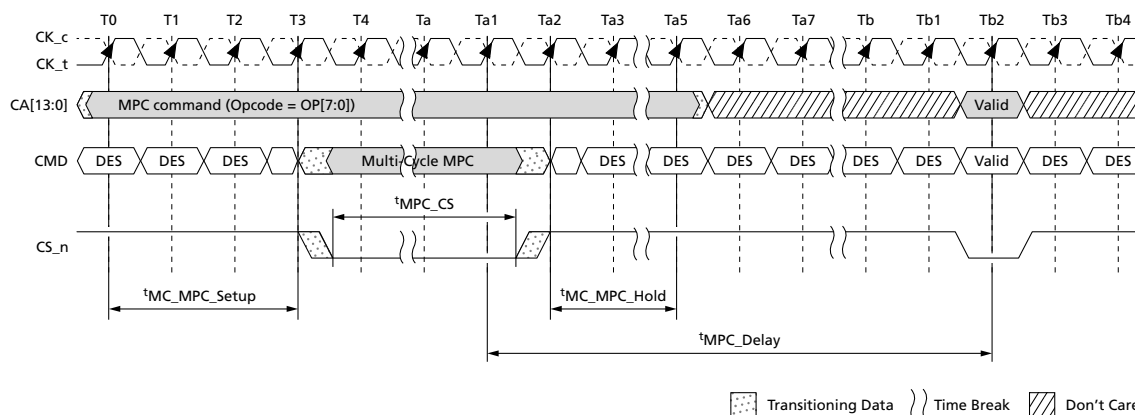
MPC Function	OP[7:4]	OP[3:0]	Notes
PDA Enumerate ID	0110	0000b: ID 0 0001b: ID 1 0010b: ID 2 0011b: ID 3 0100b: ID 4 0101b: ID 5 0110b: ID 6 0111b: ID 7 1000b: ID 8 1001b: ID 9 1010b: ID 10 1011b: ID 11 1100b: ID 12 1101b: ID 13 1110b: ID 14 1111b: ID 15 - default	
PDA Select ID	0111	0000b: ID 0 0001b: ID 1 0010b: ID 2 0011b: ID 3 0100b: ID 4 0101b: ID 5 0110b: ID 6 0111b: ID 7 1000b: ID 8 1001b: ID 9 1010b: ID 10 1011b: ID 11 1100b: ID 12 1101b: ID 13 1110b: ID 14 1111b: ID 15	1

Note: 1. PDA SELECT ID 15 selects all devices regardless of their enumerate ID.

MPC Function Timing

As shown in the following figure, the MPC CMD timings are extended when multicycle CS assertion duration mode (MR2:OP[4]) is set to zero. The CS_n is also asserted for multiple consecutive cycles, limited by ^tMPC_CS. All timings are relative to the final rising CK_t/CK_c within the CS_n assertion window. The MIN delay from when the MPC is captured to the next valid command is specified as ^tMPC_Delay. Prior to VREFCS, VREFCA, CS, and CA Training completing successfully, CA is driven with additional setup and hold beyond the CS_n assertion. For the device to latch the MPC in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state and provide at least three cycles of setup prior to CS_n transitioning from HIGH to LOW, CS_n must remain LOW for ^tMPC_CS, and CA must remain in the proper command state and provide at least three cycles of hold after CS_n transitions from LOW to HIGH. This additional setup and hold is only needed when MR2:OP[4] is set to 0 (multicycle CS assertion duration mode).

Figure 10: MPC Function Timing



The device supports an MR setting to indicate when a multicycle CS assertion may be used for MPC, VREFCA and VREFCS commands. MR2:OP[4] defaults to 0 upon a reset. After MR2:OP[4] = 1 (single-cycle CS_n assertion) has been set, the host is required to change MR2:OP[4]=0 if any multicycle CS_n timings are used.

Figure 11: MPC Function Timing to 2-Cycle Command

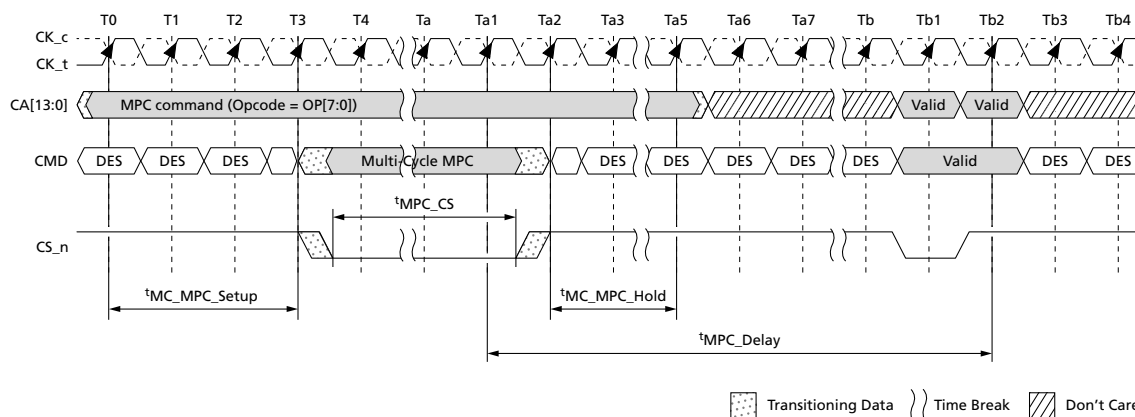


Table 151: MPC, VREFCA and VREFCS Assertion Duration

MR Address	Operating Mode	Description
MR2:OP[4]	CS Assertion Duration	0 = Multiple cycles of CS assertion supported for MPC, VREFCA and VREFCS. 1 = Only a single cycle of CS assertion supported for MPC, VREFCA and VREFCS.

Default value for the CS assertion duration is 0, which enables multicycle CS assertions during training.

Some MPC functions require all banks to be in an Idle state, while other MPC functions can occur regardless if all banks are Idle or if some or all banks are Active. Regardless of the initial bank state requirement for an MPC function, the MPC function itself will not change the bank state between active or idle.

MPC functions that require all banks to be Idle when the MPC is issued will complete in an all banks Idle state.

MPC functions that can occur regardless of the bank state will not change the state of the bank, but other commands simultaneously executing within the duration of the MPC function may result in a

change of states. For example, a Precharge command to an Active bank can change the state from Active to Idle while the MPC function is executing.

Table 152: MPC Functions Requiring All Banks Idle State

MPC Functions
CSTM (Enter/Exit)
DLL RESET
CATM (Enter)
PDA Enumerate Programming (Enter/Exit)
Manual ECS Operation
Apply VrefCA, VrefCS and RTT_CA/CS/CK
Set DQS_RTT_PARK
Set RTT_PARK
PDA Enumerate/Select ID
CS Geardown Enable

Note: 1. For 3DS, MPC commands for All Banks Idle cases require all banks to be idle on all logical ranks.

Table 153: MPC Functions Independent of Bank State

MPC Functions	Notes
ZQCAL (Latch/Start)	1
DQS Interval Oscillator (Start/Stop)	
Set 1N/2N Command	
Configure Group A/B RTT_CA/CS/CK	
Configure t_{DLLK}/t_{CCD_L}	

Note: 1. The host can issue MPC ZQCAL Start command with the timing delay specified in the PRE Timing Constraints Related to ZQCAL Start table.

Table 154: PRE Timing Constraints Related to ZQCAL START

From Command	To Command	Minimum Delay Between From Command and To Command	Unit
PREab/sb/pb	ZQCAL START	1	t_{CK}

Table 155: RD/WR Timing Constraints Related to MPC, VREFCS and VREFCA for All Banks Idle Cases

From Command	To Command	Minimum Delay between From Command and To Command	Unit
RDA	MPC	$t_{RTP} + t_{RP}$	t_{CK}
	VREFCA/VREFCS	$t_{RTP} + t_{RP}$	t_{CK}
WRA	MPC	$CWL + BL/2 + t_{WR} + t_{RP}$	t_{CK}
	VREFCA/VREFCS	$CWL + BL/2 + t_{WR} + t_{RP}$	t_{CK}

Notes: 1. RD/WR can refer to both target ODT RD/WR and nontarget ODT RD/WR.
2. Selected MPC functions require all banks to be idle. This includes all banks within 3DS logical ranks.
3. Nontarget rank commands are required to meet the minimum ODT requirements for DQ/DQS.

2N Mode

2N mode enables the system to provide more setup and hold on the CA bus. 2N mode is enabled by default on the device, and an MPC is used to change between 2N and 1N modes. MR2:OP[2] enables the state of the 2N mode to be read.

The device has defined two-cycle commands, which require the device to capture the command differently between 1N and 2N modes. In both modes, the first half of the command is sampled on the clock that the chip select is active. In 1N mode, the second half of the command is sampled on the next clock edge. In 2N mode, the second half of the command is sampled two clocks after the first half.

NT ODT signaling (on the chip select) is also delayed by a clock in 2N mode.

One-cycle commands operate the same in 1N and 2N mode, with the command sampled on the same clock where the chip select is active.

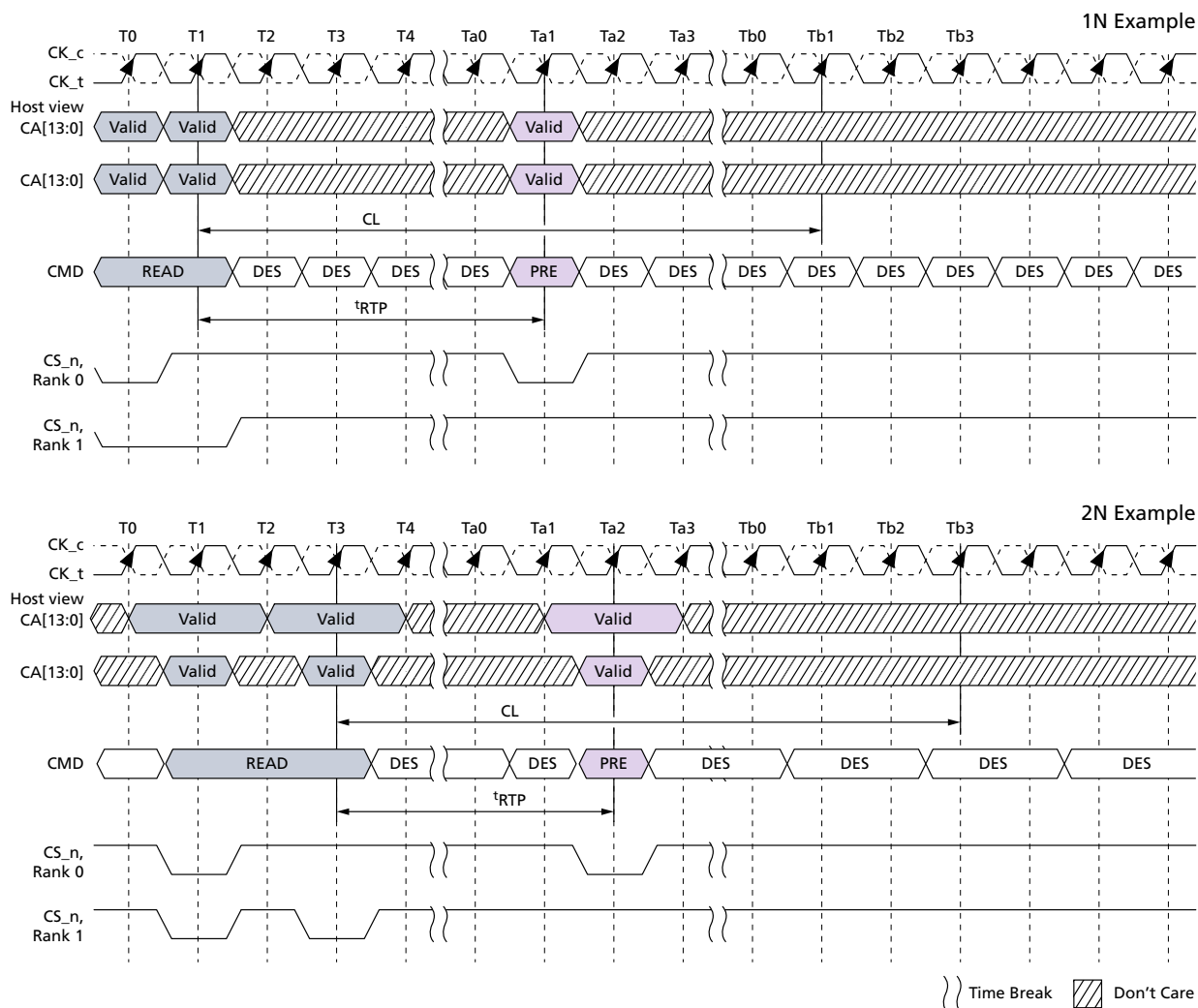
A two-cycle or one-cycle command can start on any clock (unlike gear-down mode). The following figure shows the differences between standard 1N mode with a two-cycle READ command followed by a one-cycle PRECHARGE command, along with comparable timing when operated in 2N mode with the same commands. In 2N mode, the host never sends two consecutive chip selects except during explicit cases such as exiting CATM mode.

Table 156: 2N Mode Register Configuration

Function	Register Type	Operand	Data	Notes
2N mode	R	MR2:OP[2]	0b: 2N mode (default) 1b: 1N mode	1,2

- Notes: 1. To ensure training modes can be enabled and run appropriately, the default (power-on) mode for the device is 2N mode. After CA training, the user can configure this bit to put the device into either 1N mode or 2N mode.
2. Since 2N mode setting is an MPC-based command, it can only be programmed via that command and its mode register is therefore read-only.

Figure 12: Example of 1N vs. 2N Mode - Reference Only



- Notes: 1. The host view CA[13:0] is shown for clarification, while CA[13:0] is what the device should expect.
2. CS_n Rank 1 is shown for READ NT ODT clarification.
3. tRTP can be launched on odd or even clocks.

1N/2N Mode Clarifications

Several DDR5 device features require specific CS_n and CA bus behavior to function correctly in 1N and 2N modes. The following shows these behaviors, with additional details in the respective sections of the data sheet.

Table 157: CS_n and CA Bus Required Behaviors

Behavior	CS Assertion Duration	CS_n Required Behavior for 1N or 2N	CA Bus Required Behavior for Multicycle CS Assertion/2N
Cold or warm reset exit	Multi (default)	N/A	Static NOP for 3+ nCK
MPC (includes CSTM exit)	Single	Single low pulse	Single MPC
	Multi	Static multicycle low	Static MPC surrounding CS_n low by tMC_MPC_*

Table 157: CS_n and CA Bus Required Behaviors (Continued)

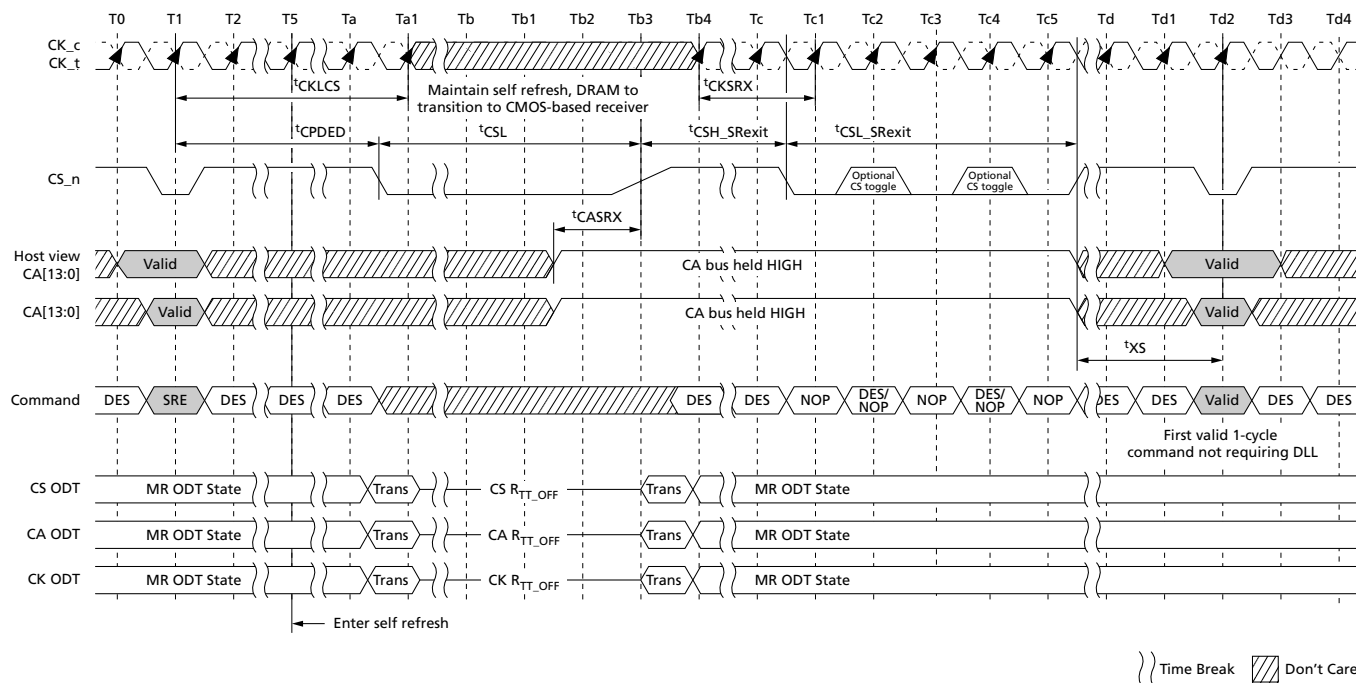
Behavior	CS Assertion Duration	CS_n Required Behavior for 1N or 2N	CA Bus Required Behavior for Multicycle CS Assertion/2N
VREFCS/VREFCA	Single	Single low pulse	Single VREFCS/VREFCA
	Multi	Static multicycle low	Static VREFCS/VREFCA surrounding CS_n low by $t_{MC\_VREFCS\_*} / t_{MC\_VREFCA\_*}$
CATM exit (NOP Command)	Don't care	Static low for 2+ nCK	Static NOP for the duration of $t_{CATM\_CS\_Exit}$
Power Down Mode Exit (NOP)	Don't care	Single low pulse	Single NOP
Self Refresh Mode Exit (3 x NOPs)	Don't care	Static low for 3+ nCK	Static NOP for 3+ nCK if CS_n held static low
		Pulsing low 3+ cycles (...0, 1, 0, 1, 0...)	Static NOP for 5+ nCK if CS_n is pulsed low

Note: 1. The MR2:OP[4] CS assertion duration setting only applies to the MPC, VREFCA, and VREFCS commands.

Self Refresh in 2N Mode

The following figure shows details for self refresh entry/exit in 2N mode. Only exiting self refresh (3 x NOPs) with a pulsing CS_n (NOP-DES-NOP-DES-NOP) during t_{CSL_SRExit} to a one-cycle command is shown, but behavior is similar for exiting self refresh (3 x NOPs) to a two-cycle command. Behavior is similar for frequency change during self refresh with or without V_{REF} and/or ODT changes. Pulsing CS_n during t_{CSL_SRExit} is not required for self refresh exit (for example, CS_n may be held LOW for the full t_{CSL_SRExit} duration).

Figure 13: Self Refresh Entry/Exit Timing in 2N Mode with One-Cycle Exit Command



Notes: 1. If t_{CSH_SRExit} timing is not met after CS_n transition from LOW to HIGH or if three or more NOPs are not issued to satisfy t_{CSL_SRExit} as defined in the specification, device operation cannot be guaranteed.

- When $t_{CSH\_SExit,min}$ expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at t_{c+1} , the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters.

CS Geardown Mode

DDR5 geardown mode for CS enables CS operation to 2N mode at conditions where 1N mode is not viable due to the system configuration and speed of operation. CS geardown is enabled with an MPC during power-up. Upon exit from self refresh with frequency change, CS geardown mode is enabled or disabled based on the setting of MR13:OP[4].

CS geardown mode is supported only on DRAMs that support MAX data rates of 7200 and faster. These DRAMs support CS geardown mode at all supported operating frequencies. The DRAM must also be capable of operating at 7200 MT/s and above with geardown mode disabled. The commands must not be issued at odd gap clocks from where clock sync occurred for proper functioning.

The system must complete CSTM and CATM after any power-on initialization.

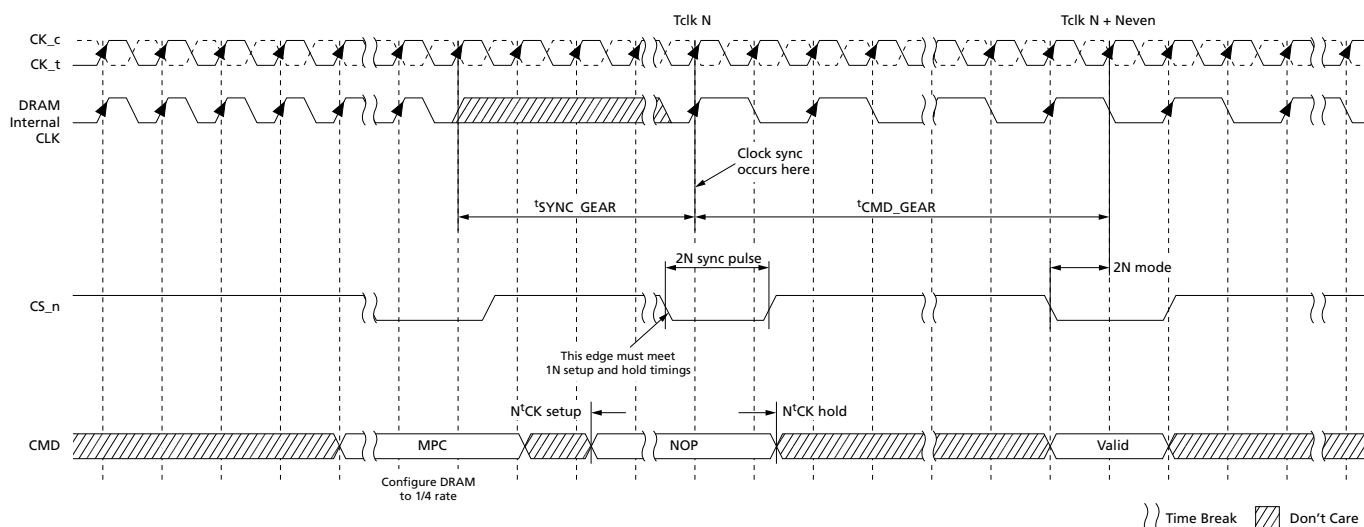
Geardown INIT sequence:

- Power-up initialization
- CSTM (1N CS pulse)
- MPC (CS geardown enable)
- Sync pulse (2N)
 - Only DSEL commands are allowed during t_{SYNC_GEAR} (between MPC and sync pulse).
 - 2N sync pulse is 2 clocks wide. The falling edge of the pulse must meet 1N setup and hold timings. It must meet the hold time from the previous rising edge of the clock where it is sampled HIGH, and meet the setup time of the next rising edge of the clock where it is sampled LOW.
- CATM (in geardown)

Note that in geardown mode, the exit from CATM is achieved with two consecutive geardown NOPs (CS sampled active on two consecutive even numbered clocks).

For the CS geardown MPC, MR13:OP[4] Opcode, defined in the MPC Command Definition for OP[7:0] table, should be applied. The MPC command will not affect MR13:OP[4]. The host controller is expected to set this mode register if CS geardown is to be used following self refresh.

Figure 14: CS Geardown During Initialization



- Notes:
1. During initialization, CSTM must be run before entering CS geardown mode.
 2. CSTM must be run in 1N mode in order to meet the 1N setup and hold window for the CS geardown sync, which is sent when the bus is quiet. After entering CS geardown mode, the CS is sampled only on even numbered clocks, which provides the additional setup and hold times required for normal operation when other signals are toggling.
 3. For the sync pulse, only the first falling edge of CS is used by the DRAM to determine the clock phase. The rising edge of the CS is not used for synchronization and has no timing constraints.
 4. The NOP encoding on the CA bus may be longer than the CS pulse used for synchronization.

Table 158: CS Geardown Parameters

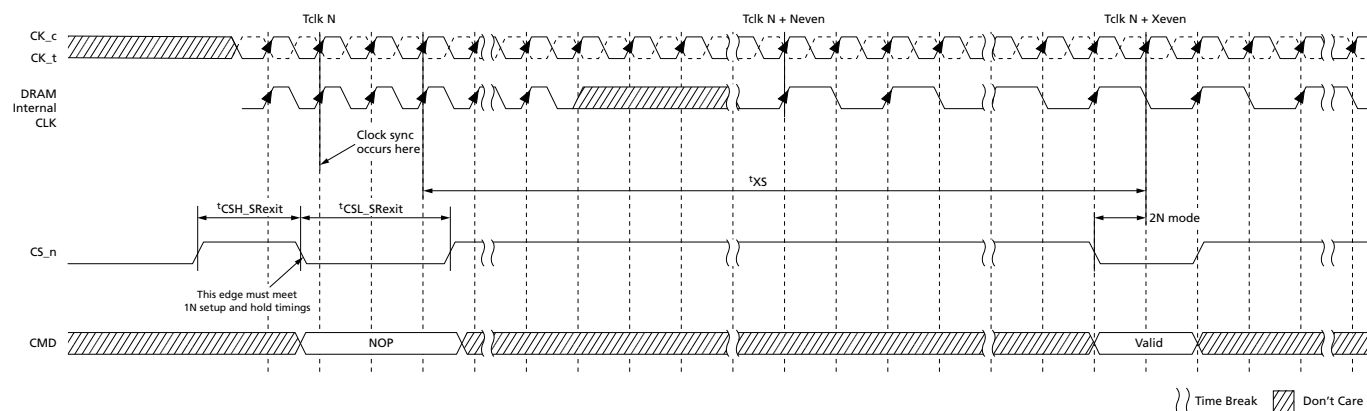
Symbol	Value
$t_{\text{Sync\_Gear}}$	$\max(14\text{ns}, 16\text{nCK})$
$t_{\text{CMD\_Gear}}$	$\max(14\text{ns}, 16\text{nCK})$

Upon self refresh exit, the geardown clock phase must be re-established. CS geardown may also be switched on or off upon self refresh exit due to a frequency change. MR13:OP[4] determines whether the DRAM will enable geardown mode upon the next exit of self refresh with frequency change. If switching between CS geardown on and off modes, the host controller must write MR13:OP[4] to the appropriate value any time prior to the self refresh entry with frequency change (SREF) command. The required MR13:OP[4] change is defined in the Mode Register Assignment and Definition MR0-MR63 table. Note that an SRE command (without frequency change) will remain in the previous mode and will NOT change based on a change in MR13:OP[4].

When CS geardown is enabled, during a self refresh exit the DRAM will sample the proper clock edge during $t_{\text{CSL\_SRExit}}$. After t_{XS} , the host can drive CS at 2N.

CS geardown must be used only with the CA bus in 2N mode. It is the host controller's responsibility to have the CA bus in 2N mode with an explicit MPC command when operating in CS geardown mode before any 2-cycle commands are sent.

Figure 15: CS Geardown Enabled During SRX



- Notes:
1. For the sync pulse, only the first falling edge of CS is used by the DRAM to determine the clock phase. The rising edge of the CS is not used for synchronization and has no timing constraints.
 2. CS must remain static LOW during $t_{\text{CSL\_SRExit}}$.
 3. The NOP encoding on the CA bus may be longer than the CS pulse used for synchronization.

ACTIVATE Command

The ACTIVATE command opens (activates) a row in a particular bank for subsequent access. The values on BG[2:0] in x4 and x8 devices and BG[1:0] in x16 devices select the bank group; BA[1:0] (BA[0] only for 8Gb) selects the bank within the bank group. The address provided on the appropriate CA pins for R[17:0] selects the row. In case of a 3DS device, CID[3:0] is also selected to identify the correct die in the stack. This row remains active (open) for accesses until a PRECHARGE command is issued to that bank or a PRECHARGE ALL command is issued. A bank must be precharged before opening a different row in the same bank.

Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. t_{RRD_S} (short) is used for timing between banks located in different bank groups. t_{RRD_L} (long) is used for timing between banks located in the same bank group.

Consecutive ACTIVATE commands, which are allowed to be issued at t_{RRDmin} , are restricted to a maximum of four within the time period t_{FAW} (four activate window).

Non-Binary Density Considerations

An ACT command with row address inputs which violate this restriction must follow all timing and protocol rules as though the ACT were valid.

Any RD or RDA command to a bank following an invalid ACT to that same bank must drive the DQS strobes with normal timing, but must not expose information that can be used to learn about data stored in cells with valid addresses. Data being sent that coincidentally matches cell array data is permissible (for example, always sending all 1s and cell data sometimes being all 1s). Consistently exposing data from a previous READ or previous ACTIVATE would not be permissible.

Any WR, WRA, WRP or WRPA command to a bank following an invalid ACT to that same bank must not result in new data being written anywhere within the device.

The device operates normally for READ and WRITE commands to banks that have pages open to valid rows.

PRECHARGE Command

The PRECHARGE command deactivates the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time ('RP) after the PRECHARGE command is issued. After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. The precharge period is determined by the last PRECHARGE command issued to the bank.

If CA10 is LOW for the second half of a READ or WRITE command, the auto-precharge function engages. This feature enables the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS latency), thus improving system performance for random data access. The RAS lockout circuit internally delays the precharge operation until the array restore operation completes ('RAS satisfied) so that the AUTO PRECHARGE command may be issued with any read. Auto-precharge is also implemented during WRITE commands. The precharge operation engaged by the AUTO PRECHARGE command does not begin until the last data of the burst write sequence is properly stored in the memory array. The bank is available for a subsequent row activation at a specified time ('RP) after the hidden PRECHARGE command (AUTO PRECHARGE) is issued to that bank. The precharge-to-precharge delay is defined by 'PPD in the core timing tables. 'PPD applies to any combination of precharge commands (PREab, PREsb, PREpb). 'PPD also applies to any combination of precharge commands to a different die in a 3DS device.

PRECHARGE Command Modes

Three different types of precharge commands are supported:

- PRECHARGE (PREpb): applies precharge to a specific bank defined by BA[1:0] (if applicable) in a specific bank group defined by BG[2:0].
- PRECHARGE ALL (PREab): applies precharge to all banks in all bank groups.
- PRECHARGE SAME BANK (PREsb): applies precharge to a specific bank defined by BA[1:0] in all bank groups.

With a 3DS device, CID[3:0] is also selected to identify the target die.

The different encodings for PREsb, PREab, and PREpb are shown in the [Command Truth table](#).

Burst Length, Type, and Order

Accesses within a given burst are sequential only; interleaved is not supported. The ordering of accesses within a burst is determined by the burst length and the starting column address, as shown in the tables below. The burst length is defined by MR0:OP[1:0]. Burst length options include BC8 OTF, BL16, BL32 (optional), and BL32 OTF (optional).

BL16 Mode

Table 159: Burst Type and Order — READ

Burst Length	Burst Type	C3	C2	READ Burst Cycle and Burst Address Sequence															
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BC8 OTF	Sequential	0	0	0	1	2	3	4	5	6	7	T	T	T	T	T	T	T	T
		0	1	4	5	6	7	0	1	2	3	T	T	T	T	T	T	T	T
		1	0	8	9	A	B	C	D	E	F	T	T	T	T	T	T	T	T
		1	1	C	D	E	F	8	9	A	B	T	T	T	T	T	T	T	T
16	Sequential	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0	1	4	5	6	7	0	1	2	3	C	D	E	F	8	9	A	B
		1	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	C	D	E	F	8	9	A	B	4	5	6	7	0	1	2	3

Notes: 1. T: Output driver for data and strobes are in RTT_PARK.

2. V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

3. X: Don't Care.

Table 160: Burst Type and Order — WRITE

Burst Length	Burst Type	C3	C2	WRITE Burst Cycle and Burst Address Sequence															
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BC8 OTF	Sequential	0	V	0	1	2	3	4	5	6	7	X	X	X	X	X	X	X	X
		1	V	8	9	A	B	C	D	E	F	X	X	X	X	X	X	X	X
16	Sequential	V	V	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

BL32 Mode

If supported, BL32 (optional) and BL32 OTF (optional) are for x4 devices only.

Table 161: Burst Type and Order — READ

Burst Length	Burst Type	C10	C3	C2	READ Burst Cycle and Burst Address Sequence							
					1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32
BL32	Sequential	0	0	0	0-3	4-7	8-B	C-F	10-13	14-17	18-1B	1C-1F
		0	0	1	4-7	0-3	C-F	8-B	14-17	10-13	1C-1F	18-1B
		0	1	0	8-B	C-F	0-3	4-7	18-1B	1C-1F	10-13	14-17
		0	1	1	C-F	8-B	4-7	0-3	1C-1F	18-1B	14-17	10-13
		1	0	0	10-13	14-17	18-1B	1C-1F	0-3	4-7	8-B	C-F
		1	0	1	14-17	10-13	1C-1F	18-1B	4-7	0-3	C-F	8-B
		1	1	0	18-1B	1C-1F	10-13	14-17	8-B	C-F	0-3	4-7
		1	1	1	1C-1F	18-1B	14-17	10-13	C-F	8-B	4-7	0-3
BL16 in BL32 OTF	Sequential	0	0	0	0-3	4-7	8-B	C-F	X	X	X	X
		0	0	1	4-7	0-3	C-F	8-B	X	X	X	X
		0	1	0	8-B	C-F	0-3	4-7	X	X	X	X
		0	1	1	C-F	8-B	4-7	0-3	X	X	X	X
		1	0	0	10-13	14-17	18-1B	1C-1F	X	X	X	X
		1	0	1	14-17	10-13	1C-1F	18-1B	X	X	X	X
		1	1	0	18-1B	1C-1F	10-13	14-17	X	X	X	X
		1	1	1	1C-1F	18-1B	14-17	10-13	X	X	X	X

Table 162: Burst Type and Order — WRITE

Burst Length	Burst Type	C10	C3	C2	WRITE Burst Cycle and Burst Address Sequence			
					1-8	0-16	17-24	25-32
BL32	Sequential	0	V	V	0-7	8-F	10-17	18-1F
BL16 in BL32 OTF	Sequential	0	V	V	0-7	8-F	X	X
		1	V	V	10-17	18-1F	X	X

- Notes: 1. In case of BL16 in BL32 OTF mode by setting MR0:OP[1:0]=11, the internal write operation starts eight cycles earlier than for BL32 mode. This means that the starting point for t_{WR} and $t_{CCD\_*_WTR}$ must be pulled in by eight clocks.
2. T: Output driver for data and strobes are in RTT_PARK.
3. V: A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
4. X: Don't Care.

IO Features and Modes

Output Disable

Device outputs can be disabled using the data output disable mode register (MR5:OP[0]). For normal operation, set MR5:OP[0]=0b (default). To disable device outputs, set MR5:OP[0]=1b. Disabling the data outputs also disables on-die termination (ODT) for those pins. Write and non-target (NT) commands to devices with the data outputs disabled may not function correctly.

TDQS/DM

The x8 configuration has a package ball that is shared between TDQS_t and DM_n. The Write Data Mask (DM) function is dependent upon Termination Data Strobe (TDQS). If TDQS is enabled, DM is disabled. If TDQS is disabled, DM may be enabled or disabled via mode register setting, as noted in the table below.

TDQS

One pair of Termination Data Strobe (TDQS) pins, TDQS_t/TDQS_c, is supported for the x8 configuration. The TDQS function is programmable via MR5:OP[4]. The x8 is the only configuration that supports the TDQS function. The x4 and x16 configurations do not support this function; therefore, for these configurations, the TDQS MR setting must be disabled (MR5:OP[4] = 0 (default)). When TDQS is enabled (MR5:OP[4] = 1), the same termination resistance function is applied to the TDQS_t/TDQS_c pins that is applied to DQS_t/DQS_c pins, except during READ commands where TDQS does not output any data and remains at RTT_DQS_PARK.

DM

See the Write Data Mask section for data mask functionality.

TDQS/DM Enable

When the TDQS is disabled (MR5:OP[4] = 0), the MR5:OP[5] bit may be used to enable or disable the DM_n pin function.

When both TDQS and DM functions are disabled, termination is turned off and the pins drive Hi-Z. The DM_n pin input receiver will be turned-off and does not expect any valid logic level.

Table 163: x8 TDQS Function Matrix

TDQS (MR5:OP[4])	DM
0: Disabled (default)	MR5:OP[5]
1: Enabled	Disabled

Programmable Preamble and Postamble

The device supports programmable read and write preambles and postambles.

Read Preamble and Postamble

The read preamble (t_{RPRE}) is configured as 1 t_{CK} , 2 t_{CK} (two unique modes), 3 t_{CK} , and 4 t_{CK} via MR8:OP[2:0]. The read postamble is configured as 0.5 t_{CK} or 1.5 t_{CK} via MR8:OP[6].

DQS has an option to drive early by $x \cdot t_{\text{CK}}$ to accommodate different host receiver design as controlled by the read DQS offset in MR40:OP[2:0].

When operating at low speed ($\text{CL} \leq 30$), $t_{\text{RPRE}} + \text{Read DQS Offset} \geq 5$ Clocks cannot be supported, as shown in the table below.

Table 164: Valid t_{RPRE} + Read DQS Offset Combinations for $\text{CL} \leq 30$

	t_{RPRE} (nCK)	Read DQS Offset (nCK)			
		0	1	2	3
When $\text{CL} \leq 30$	1	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Invalid
	3	Valid	Valid	Invalid	Invalid
	4	Valid	Invalid	Invalid	Invalid

Figure 16: Example Read Preamble Modes (Default) with 0.5 t_{CK} Postamble

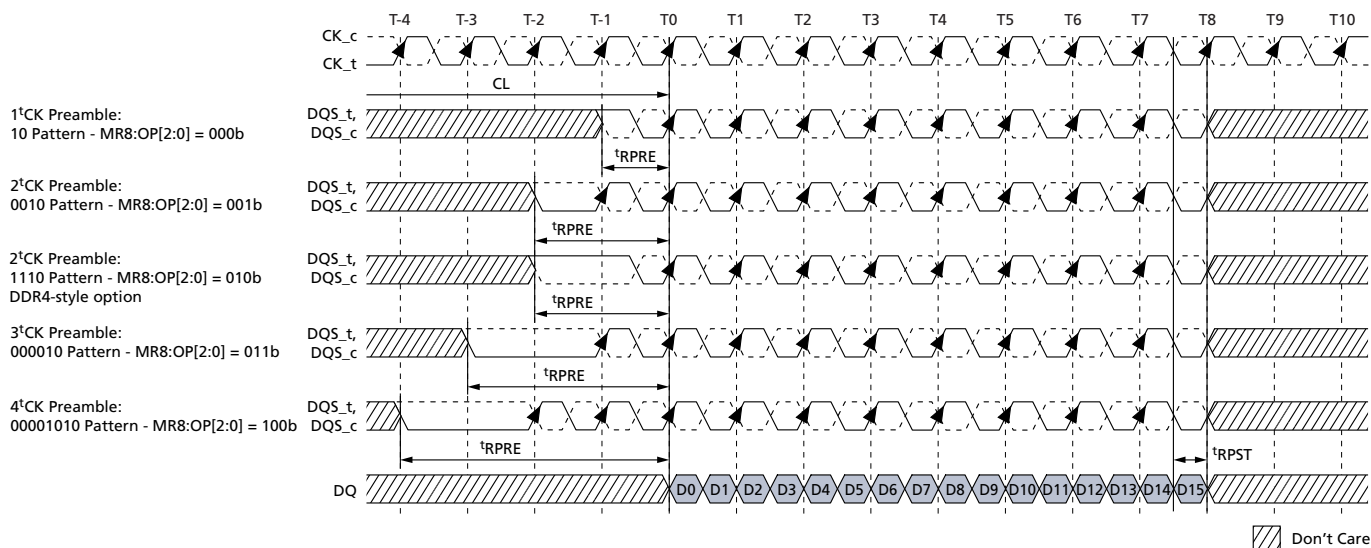


Figure 17: Example Read Preamble Modes (Default) with 1.5 t^*CK Postamble

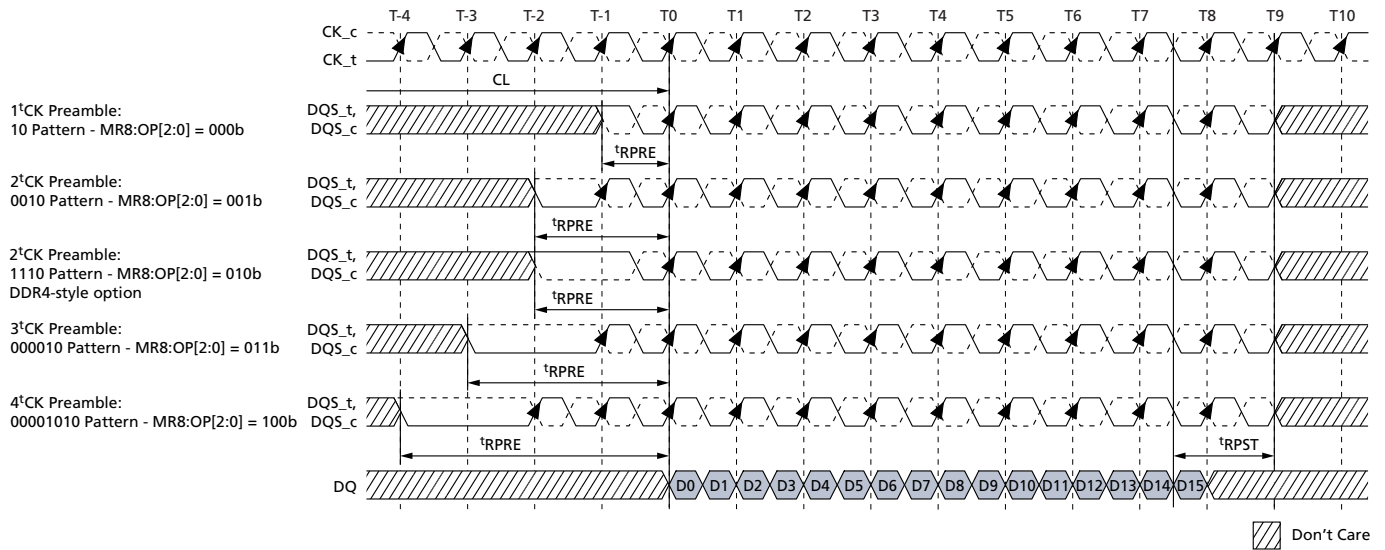
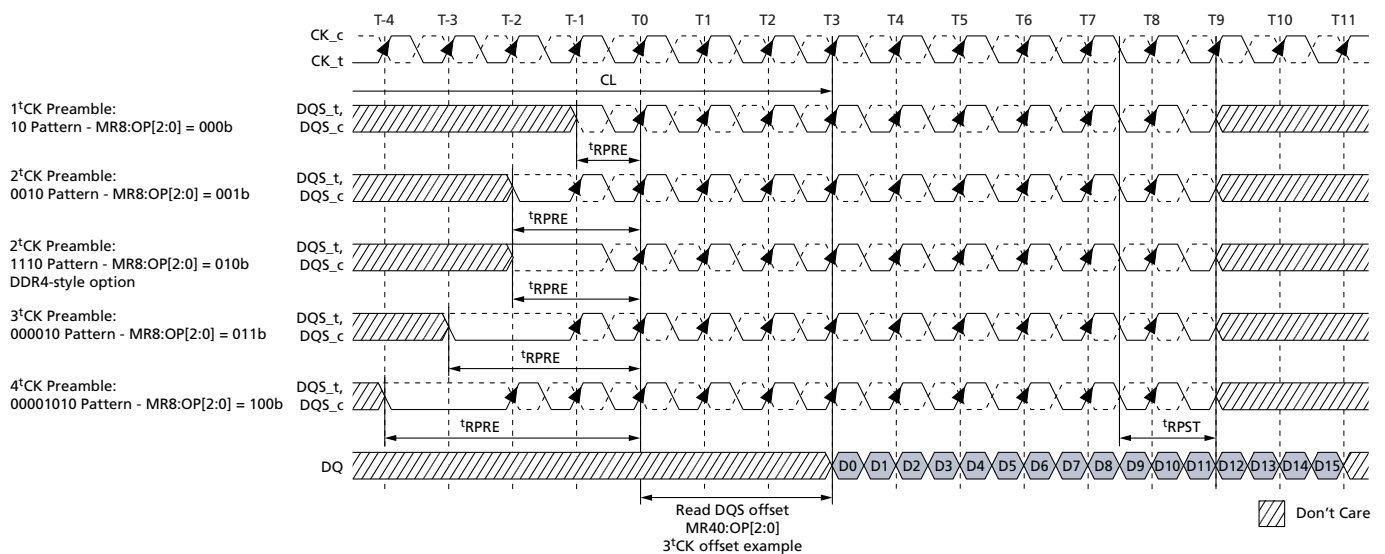


Figure 18: Example Read Preamble Modes (Default) with 3 t^*CK DQS Offset and with 1.5 t^*CK Postamble



Write Preamble and Postamble

The device supports a programmable write preamble and postamble. The write preamble is configured as 2 t_{CK} , 3 t_{CK} , and 4 t_{CK} via MR8:OP[4:3]. The write postamble is configured as 0.5 t_{CK} or 1.5 t_{CK} via MR8:OP[7].

Figure 19: Example Write Preamble Modes (Default) with 0.5 t_{CK} Postamble

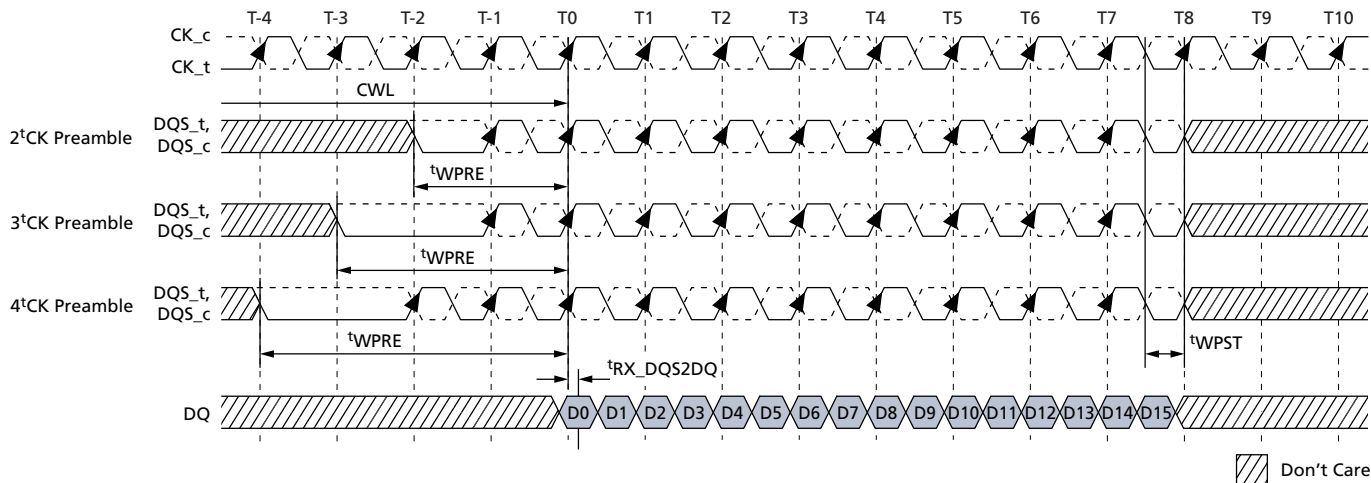
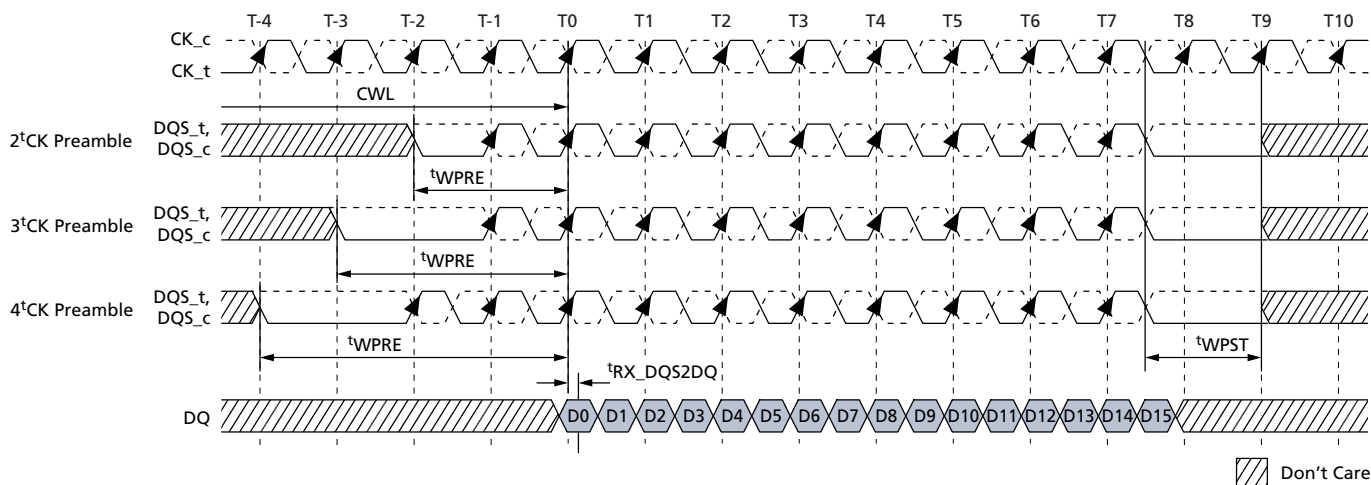


Figure 20: Example: Write Preamble Modes (Default) with 1.5 t_{CK} Postamble



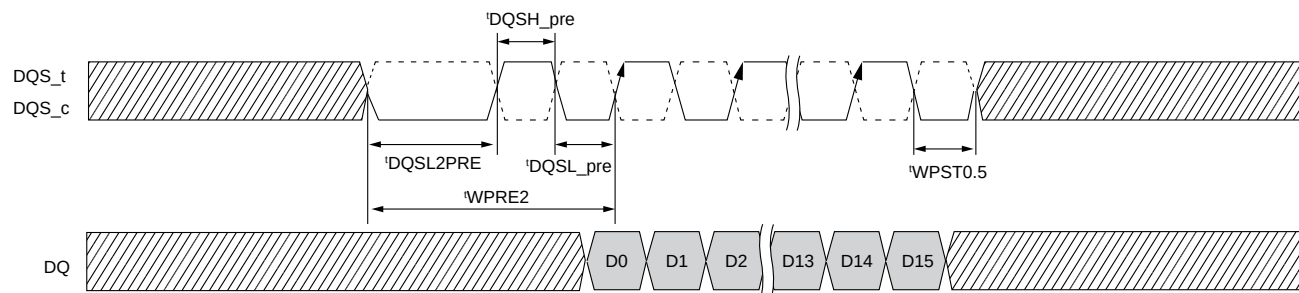
Write and Read Preamble & Postamble Timings

During WRITE and READ operations, the input and output receiver strobes, respectively, must be aligned with the DQ according to the preamble and postamble settings. Additionally, the strobes must meet the specified timing requirements to guarantee enough timing margin by setting the window for the strobes during the preamble and postamble time frames. When the DFE is enabled, the DQs shall be high for a minimum of 4UI prior to the first write data bit to ensure proper DFE synchronization.

Write preamble is set by MR8:OP[4:3] and read preamble is set by MR8:OP[2:0].

Write postamble is set by MR8:OP[7] and read postamble is set by MR8:OP[6].

Figure 21: Example: DQS Timing with 2 t^*CK Write Preamble and 0.5 t^*CK Write Postamble

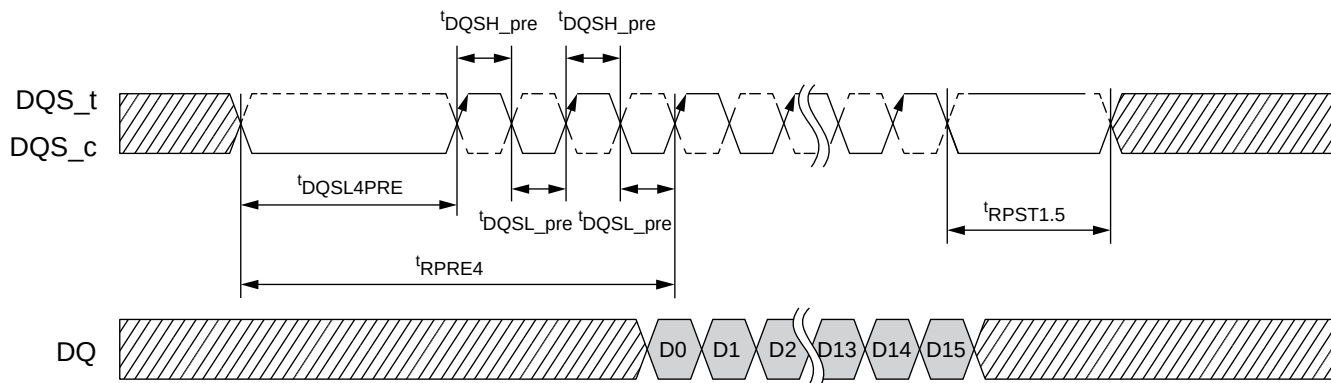


Notes: 1. BL=16

2. t^{DQSH_pre} and t^{DQSL_pre} are shown and apply to all toggles during the preamble.

3. Second preamble during WRITE to WRITE operation must follow same the requirements.

Figure 22: Example: DQS Timing with 4 t^*CK Write Preamble and 1.5 t^*CK Write Postamble

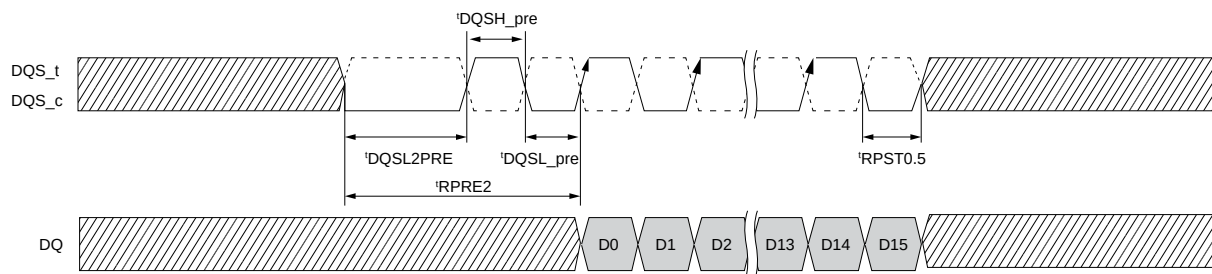


Notes: 1. BL=16

2. t^{DQSH_pre} and t^{DQSL_pre} are shown and apply to all toggles during the preamble.

3. Second preamble during WRITE to WRITE operation must follow same the requirements.

Figure 23: DQS Timing with 2 t^*CK Read Preamble and 0.5 t^*CK Read Postamble

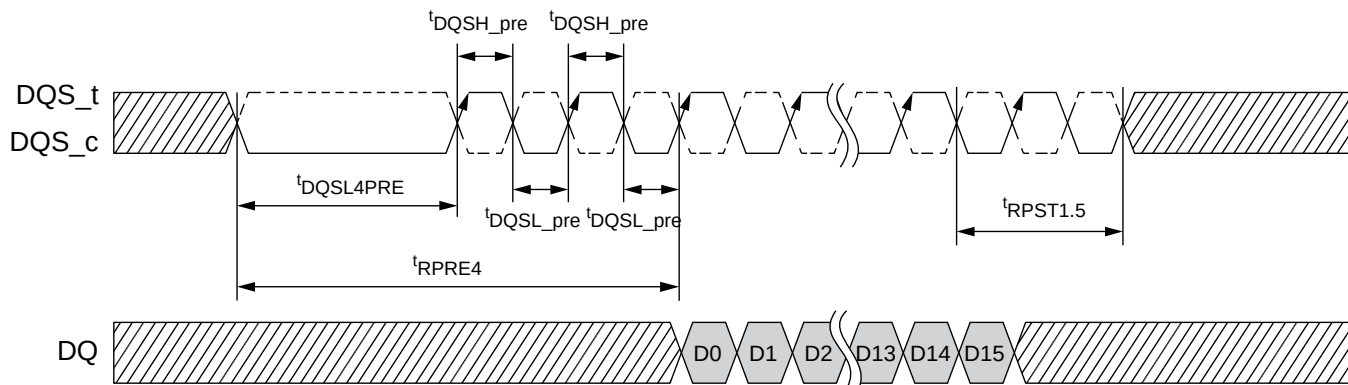


Notes: 1. BL=16

2. t^{DQSH_pre} and t^{DQSL_pre} are shown and apply to all toggles during the preamble.

3. Second preamble during READ to READ operation must follow same the requirements.

Figure 24: DQS Timing with 4 t_{CK} Read Preamble and 1.5 t_{CK} Read Postamble



- Notes:
1. BL=16
 2. t_{DQSH_pre} and t_{DQSL_pre} are shown and apply to all toggles during the preamble.
 3. Second preamble during READ to READ operation must follow same the requirements.

t_{WPRE} and t_{RPRE} Measurement

t_{WPRE} and t_{RPRE} are measured from a starting point at VswM HIGH or LOW (as defined in the table below) to the differential crossing point of DQS_t/DQS_c corresponding to the first burst bit of data as the ending point. The method is applicable for all programmable preamble durations.

Examples of the method for measuring the duration of t_{WPRE} and t_{RPRE} are shown in the figure below.

Figure 25: Method for Measuring Preamble Start and End Points

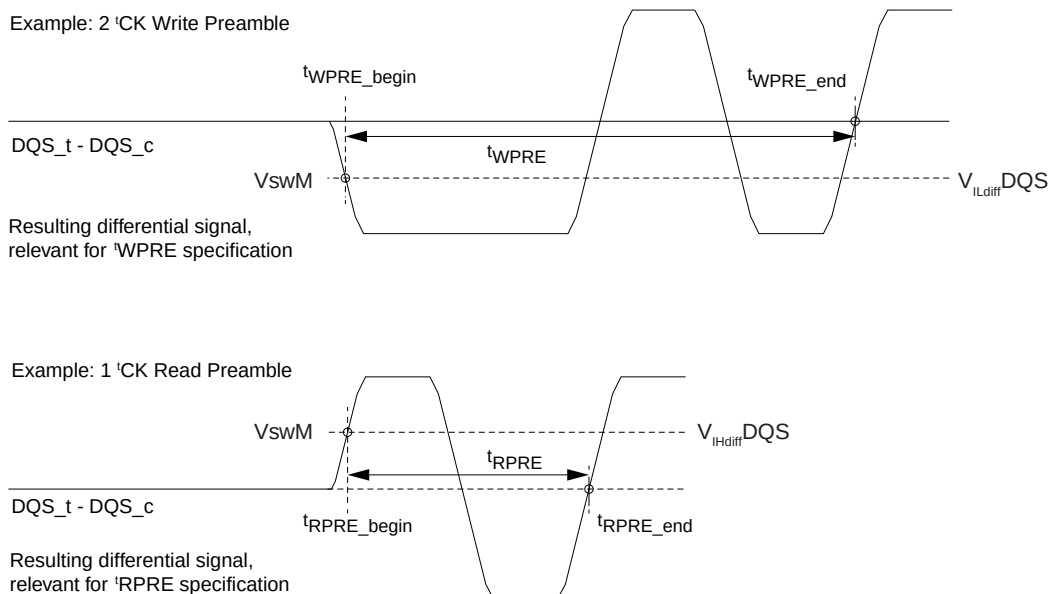


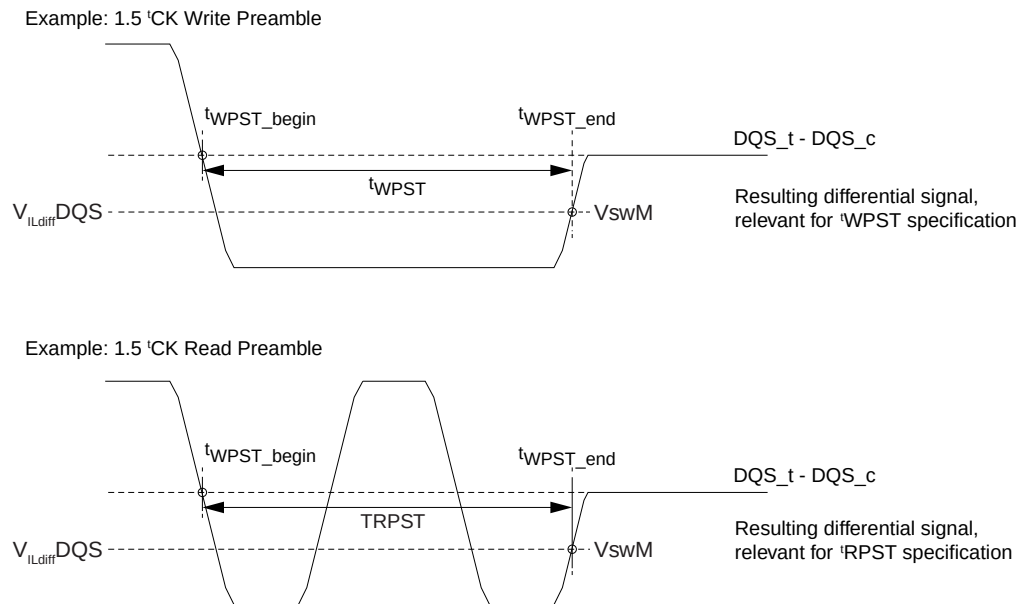
Table 165: VswM Reference Voltages for Preamble and Postamble Timing Measurements

Measured Parameter	Reference	Unit
VswM HIGH	$V_{IHdiff}DQS$	mV
VswM LOW	$V_{ILdiff}DQS$	mV

t_{WPST} and t_{RPST} Measurement

t_{WPST} and t_{RPST} are measured from a starting point at the differential crossing point of DQS_t / DQS_c corresponding to the last burst bit of data to the V_{swM} LOW ending point. The method is applicable for all programmable postamble durations. Examples of the method for measuring the duration of t_{WPST} and t_{RPST} are shown in the figure below.

Figure 26: Method for Measuring Postamble Start and End Points



Interamble

The DQS strobe requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid) and a postamble after the last latching edge. The preamble and postamble options are set via MRW commands. Additionally, the postamble- and preamble-configured size does not force the host to add command gaps in the command interval just to satisfy postamble or preamble settings (that is, preamble = 4 t_{CK} + postamble = 1.5 t_{CK} does not force $t_{CCD} + 5$).

Read Interamble Timing Diagrams

In READ-to-READ operations with $t_{CCD} = BL/2$, postamble for the first command and preamble for the second command disappear to create consecutive DQS latching edges for seamless burst operations. In the case of READ-to-READ operations with a command interval of $t_{CCD} + 1$, $t_{CCD} + 2$, etc., the toggles take precedence over static preambles if the postamble and preambles overlap.

Figure 27: Example: Seamless READ Operation: $t_{CCD} = \text{MIN}$

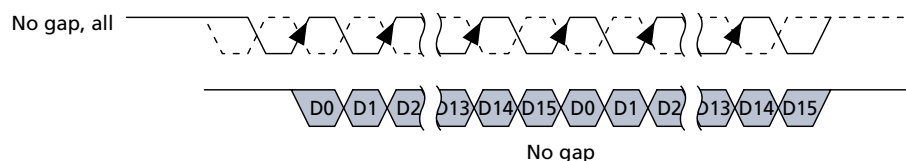


Figure 28: Example: Consecutive READ Operation: $t_{CCD} = \text{MIN} + 1$

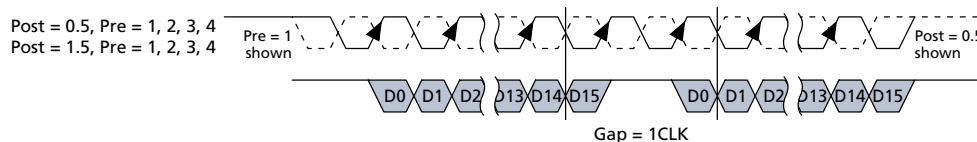


Figure 29: Example: Consecutive READ Operation: $t_{CCD} = \text{MIN} + 2$

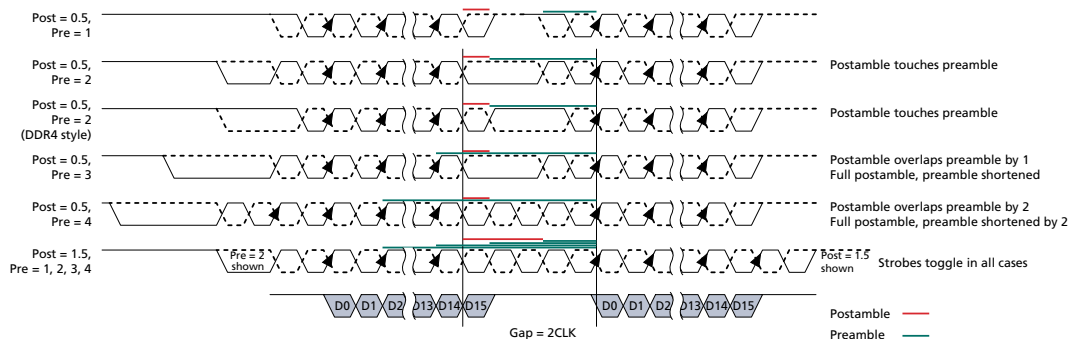


Figure 30: Example: Consecutive READ Operation: $t_{CCD} = \text{MIN} + 3$

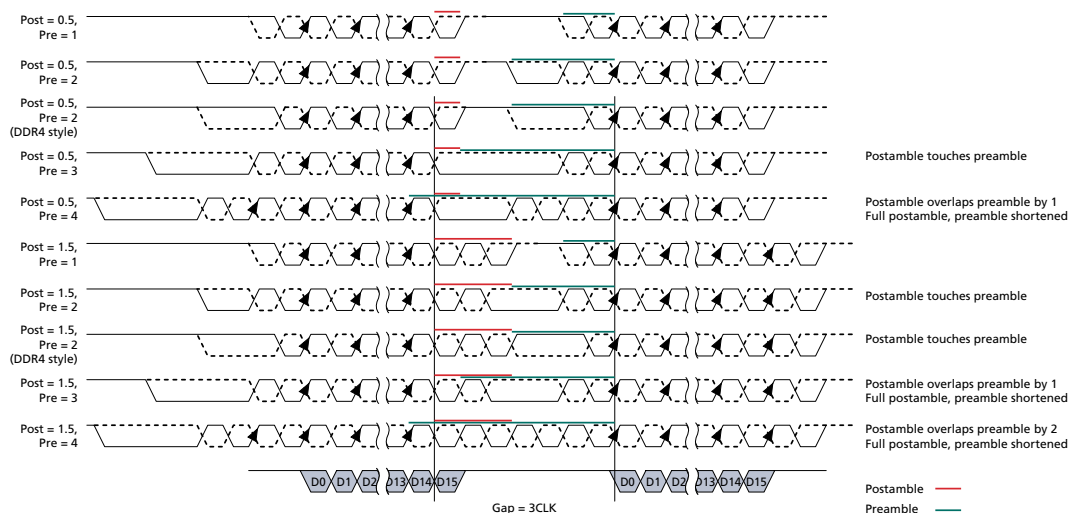


Figure 31: Example: Consecutive READ Operation: $t_{CCD} = \text{MIN} + 4$

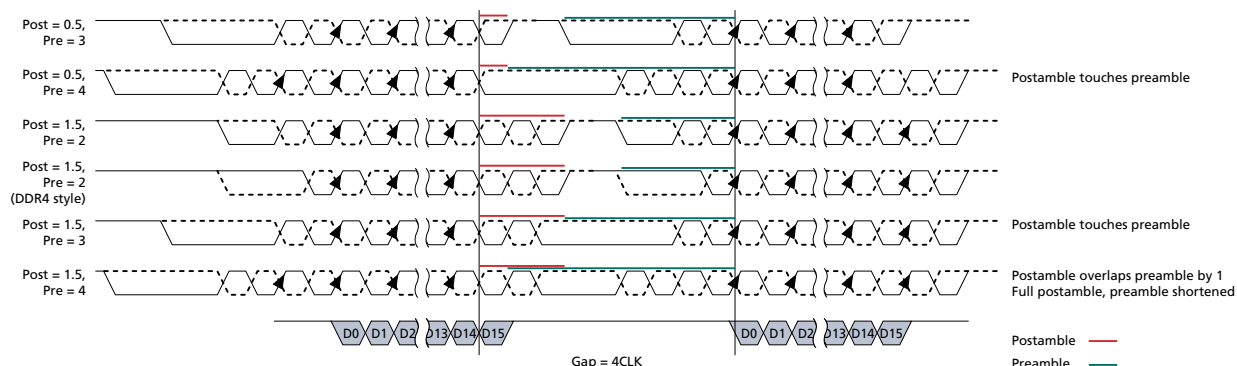
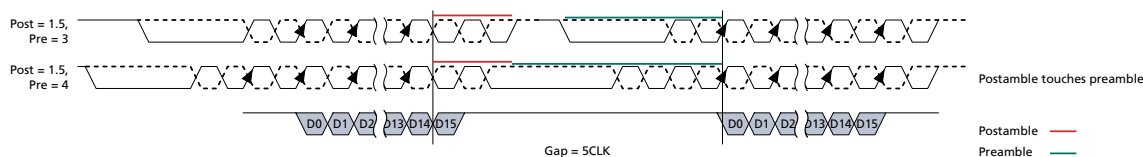


Figure 32: Example: Consecutive READ Operation: $t_{CCD} = \text{MIN} + 5$



Write Interamble Timing Diagrams

In WRITE-to-WRITE operations with $t_{CCD} = \text{BL}/2$, postamble for the first command and preamble for the second command disappear to create consecutive DQS latching edges for seamless burst operations. In the case of WRITE-to-WRITE operations with a command interval of $t_{CCD} + 1$, $t_{CCD} + 2$, etc., the toggles take precedence over static preambles if the postamble and preambles overlap.

When the DFE is enabled, the DQs shall be high during the interamble for a minimum of 4UI prior to the first write data bit of the second WRITE command. If there are 4UI or less and the DFE is enabled, the host shall drive the DQs high during the full write interamble period.

Figure 33: Example: Seamless WRITE Operation: $t_{CCD} = \text{MIN}$

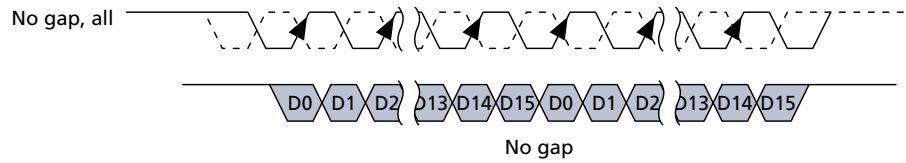


Figure 34: Example: Consecutive WRITE Operation: $t_{CCD} = \text{MIN} + 1$

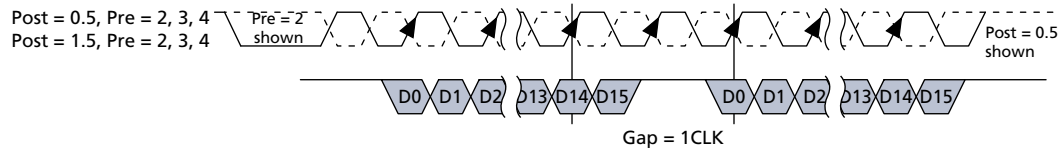


Figure 35: Example: Consecutive WRITE Operation: $t_{CCD} = \text{MIN} + 2$

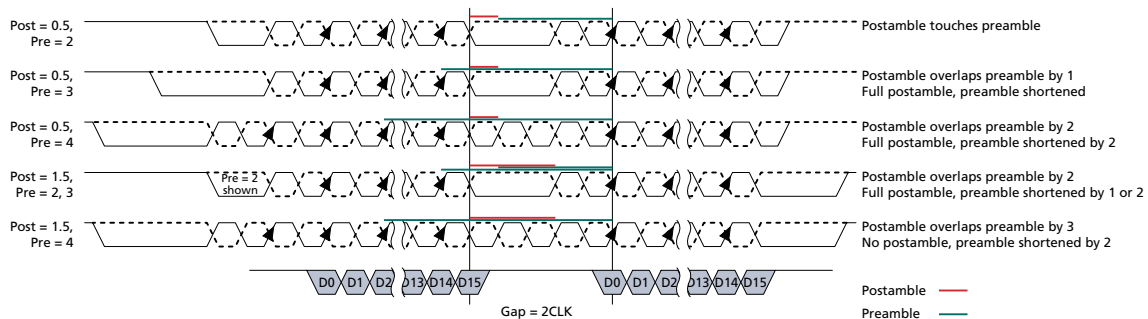


Figure 36: Example: Consecutive WRITE Operation: $t_{CCD} = \text{MIN} + 3$

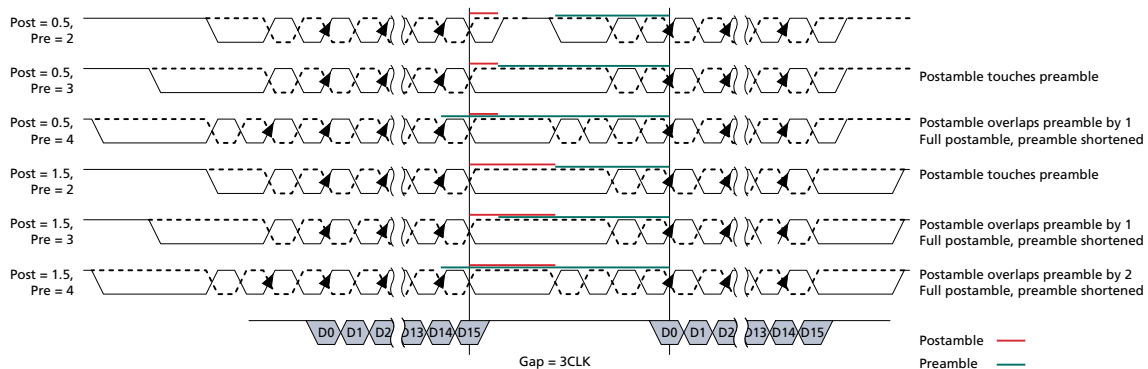


Figure 37: Example: Consecutive WRITE Operation: $t_{CCD} = \text{MIN} + 4$

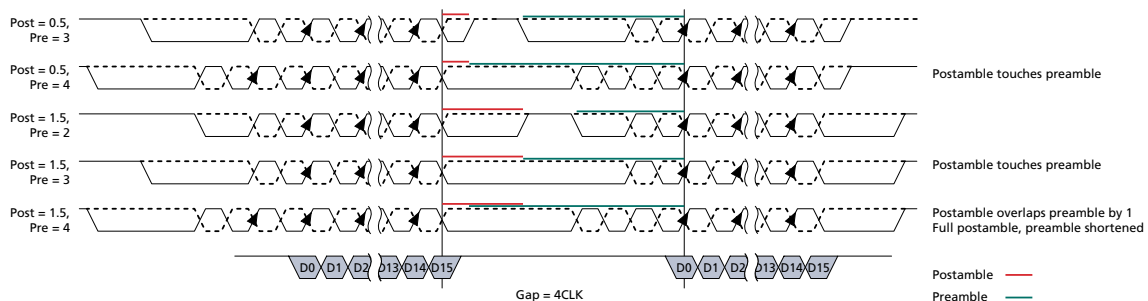
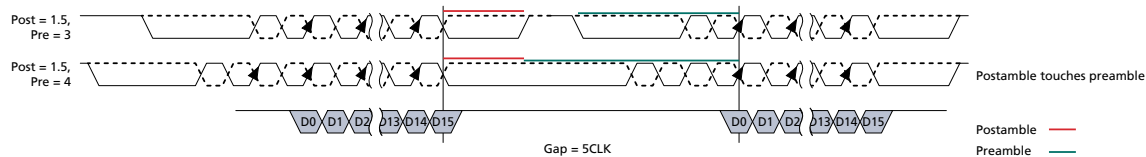


Figure 38: Example: Consecutive WRITE Operation: $t_{CCD} = \text{MIN} + 5$



On-Die ECC

Single error correction (SEC) ECC is required to improve the data integrity within the device. The device uses 128 data bits to compute the ECC code of 8 ECC check bits.

For a x4 device, internal prefetch for on-die ECC is 128 bits, even though a x4 is a 64-bit prefetch device. For each read or write transaction in a x4 device, an additional section of the device array is accessed internally to provide the required additional 64 bits used in the 128-bit ECC computation. In other words, in a x4 device, each 8-bit ECC check bit word is tied to two 64-bit sections of the device. In the case of a x8 device, no extra prefetch is required because the prefetch is the same as the external transfer size. For a x16 device, two 128-bit data words and their corresponding 8 check bits are fetched from different internal banks (same external bank address).

Each 128 data bits and the corresponding 8 check bits are checked separately and in parallel.

On reads, the device corrects any single bit errors before returning the data to the memory controller. The device must not write the corrected data back to the array during a READ cycle.

On writes, the device computes ECC and writes data and ECC bits to the array. If the external data transfer size is smaller than the 128 data bit code word (x4 devices), the device will have to perform an internal READ-MODIFY-WRITE operation. The device will correct any single bit errors that result from the internal read before merging the incoming write data and then re-compute 8 ECC check bits before writing data and ECC bits to the array. In the case of a x8 and x16 device, no internal read is required.

For a x16 device, two 136-bit code words are read from two internal banks (same external bank address); one code word is mapped to DQ[0:7] and the other code word is mapped to DQ[8:15].

SEC Overview

The ECC blocks shown in the following figure are the ECC check bit generator, syndrome generator, and syndrome decode and correction. The check bit generator and syndrome generator blocks are fully specified by the H matrix.

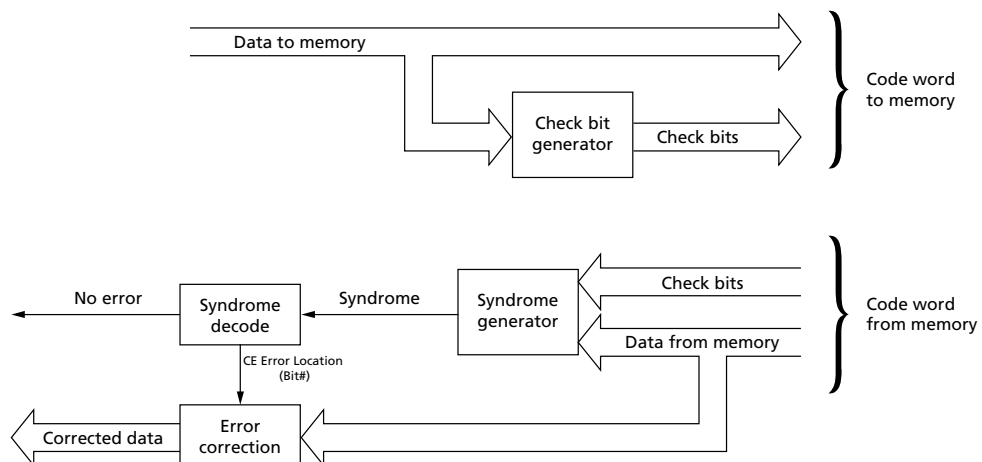
The syndrome decode block executes the following function:

- Zero syndrome => No error
- Non-zero syndrome matches one of the columns of the H matrix => Flip corresponding bit
- Non-zero syndrome that does not match any of the columns in the H matrix => DUE

Where:

- DUE: Detected uncorrected

Figure 39: On-Die ECC Block Diagram



Reliability Design Guidelines

These reliability design guidelines aim to bound bits impacted by certain device failures. This limits the number of failure patterns seen by the memory controller such that correction of many failures can be reliably performed in DIMMs with one ECC device.

Many internal device failures may impact only a portion of the data from a fetch. The likelihood of a specific component failing may also vary between process generations and DRAM vendors.

These guidelines can be used by devices to bound failures from the components most likely to fail. These design guidelines can only address failures that impact a portion of the data from a 128-bit fetch. Failures that impact all the data in a 128-bit fetch from a device (for example, device failure, bank failure) cannot be bounded as described here.

x8 Device Guidelines

In a x8 device, bounded failures are defined by the following qualities:

- A bounded failure must not impact more than 32 bits of data in a 128-bit fetch.
- The data bits impacted by a bounded failure are confined to at most two DQs (that is, the failures are DQ-aligned).
- The DQs transmitting data impacted by the failure must both be in either the first nibble or the second nibble of a burst. That is, the impacted DQs will both be in the set of the first four DQs (DQ0, DQ1, DQ2, DQ3) or the last four DQs (DQ4, DQ5, DQ6, DQ7).

The figure below shows examples of failure boundaries for x8 devices. The device on the left has a bounded failure in lanes DQ0 and DQ1 in the first nibble. The device on the right has a bounded failure in lanes DQ4 and DQ6 in the second nibble.

Figure 40: Examples of x8 Failure Boundaries



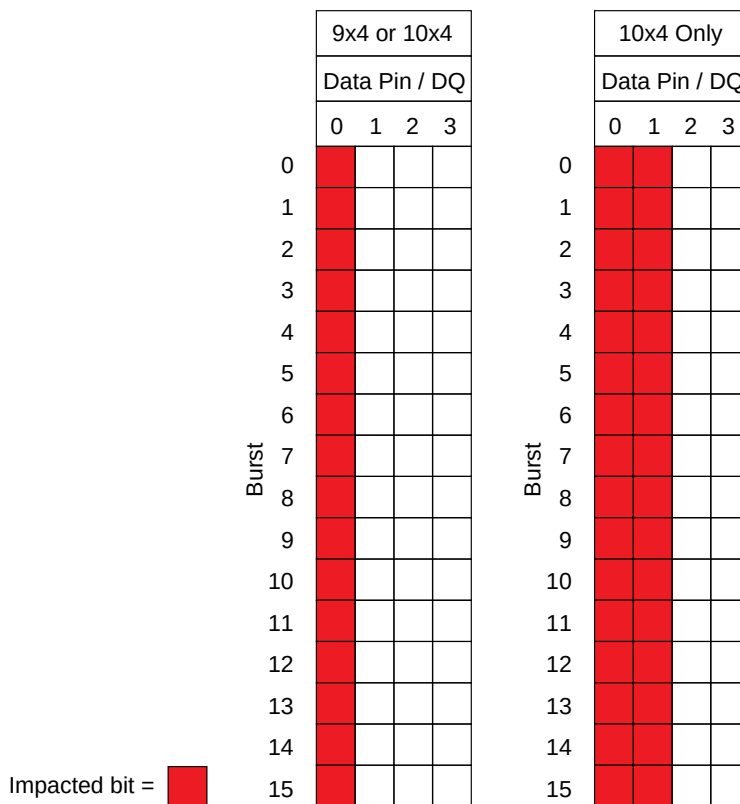
x4 Device Guidelines

A x4 device has similarly defined qualities for the failure boundaries, with the noted exception of the number of bits impacted by a bounded failure. In a device in a 9x4 configuration, bounded failures should not impact more than 16 bits. However, in a 10x4 device, the bounded failure may impact up to 32 bits.

In a x4 device, bounded failures are defined by the following qualities:

- A bounded failure in a device in a 9x4 configuration must not impact more than 16 bits of data in each 64-bit access of a 128-bit prefetch.
- A bounded failure in a device in a 10x4 configuration must not impact more than 32 bits of data in each (either) 64-bit access of a 128-bit prefetch.
- For a device in a 9x4 configuration, the data bits impacted by a bounded failure are confined to one DQ.
- For a device in a 10x4 configuration, the data bits impacted by a bounded failure are confined to at most two DQs.

Figure 41: Examples of x4 Failure Boundaries



Writeback of Data During x4 RMW Operation

The device may optionally support the suppressing of writeback for x4 devices. The Micron device implements the feature in MR15. DDR5 SPD byte 14 bits [2:1] indicate if the feature is supported and also indicates that Micron uses MR15 for enabling the modes. Micron devices define these bits in MR15. For complete details, see the [Mode Registers](#) section.

If MR15:OP[7]=1, x4 devices on writes perform an internal READ-MODIFY-WRITE operation for BL16. BL32 mode does not requires an internal READ-MODIFY-WRITE operation. The device corrects any single bit errors that result from the internal read of 128-bit data before merging the incoming 64-bit

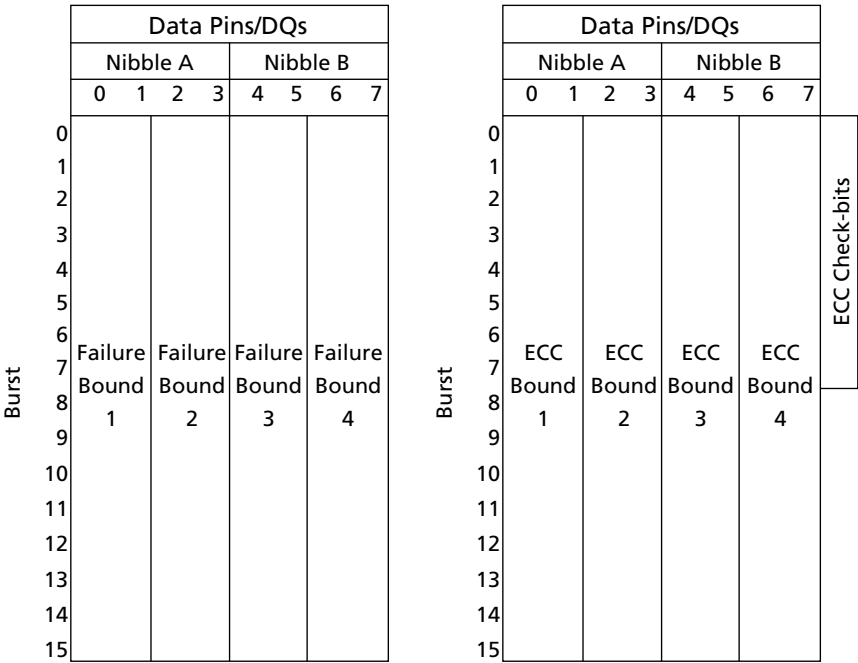
data and then re-computes 8 ECC check bits. Note that ECC check bits are computed after merging the incoming data with the corrected data from the array. The device then writes the incoming 64b data to the array along with the recomputed 8 ECC check bits. The device suppresses the writeback of 64-bit data that was fetched from the array irrespective of whether the 64-bit data needed any correction or not. Suppression of writeback (where applicable due to BC8 or DM usage) is not supported on x8/x16 devices; MR15:OP[7] must be set to 0b.

SEC Code Properties

To maintain the bounded failure design guidelines, miscorrections by the on-die ECC must be restricted when a bounded failure causes a multibit error. In devices with bounded failures, it is suggested that the DRAM vendor uses an on-die ECC code that maintains the failure boundaries. That is, if an error is contained in one boundary, the on-die ECC should not spread the error into a second boundary by miscorrection. Note that if failures are not bounded in the device, the on-die ECC does not need to have these properties.

To restrict miscorrection in devices following bounded failure design guidelines, the data may be divided into blocks aligned with the bounded failure and miscorrection should be restricted in case an error is contained in a single data block. The 128 data bits used to compute a set of 8 check bits may be divided into data blocks up to 32 bits in size. These data blocks are to be determined by the memory vendor to best align with internal DRAM failures. For example, a common component failure may impact 32 bits per 128 data bits; the vendor may choose to divide the 128 data bits into four 32-bit blocks each of which correspond to the bits impacted by one of the components failing.

Figure 42: Example Failure Boundaries vs. On-Die ECC Data Blocks



If a multi-bit error occurs on a read and is limited to one data block, the on-die ECC SEC code should do one of the following

- Miscorrect a bit in the data block containing the error
- Miscorrect a bit in the on-die ECC check bits
- Detect the error (a SEC code may detect some multi-bit errors, but detection of these errors is not guaranteed)

The selection of block size and data blocks is determined by the vendor to best suit the device architecture and possible modes of failure.

Write Operation

The WRITE operation stores data in the device and is initiated by the WRITE command, during which the beginning column address and bank/group address for the data to be written to the array is provided. The data is provided on the DQ inputs CWL cycles after the WRITE command along with the proper waveform on the DQS inputs. CWL is defined and measured from final cycle of the WRITE command to the first rising DQS (excluding write preamble).

Write Data Mask

One write data mask (DM_n) pin for each byte data group is supported on x8 and x16 devices. The DM_n pin/function is enabled via mode register. For the x4 configuration, the DM mode register setting must be disabled. The DM_n pin has identical timings and termination functionality on the WRITE operation as the DQ pins (shown below). The DM_n pin is not used for READ cycles and the pin should behave like a DQ pin driving HIGH or be terminated to RTT_PARK. When the DM function is disabled by MR, the device disables the DM input receiver and output transmitter and does not expect nor drive any valid logic level.

Each data mask burst bit position corresponds to the same bit position in the DQ data burst across the corresponding byte group. If DM is disabled MR5:OP[5], WR_partial (WR_P) must be HIGH. DM_n may be HIGH or LOW.

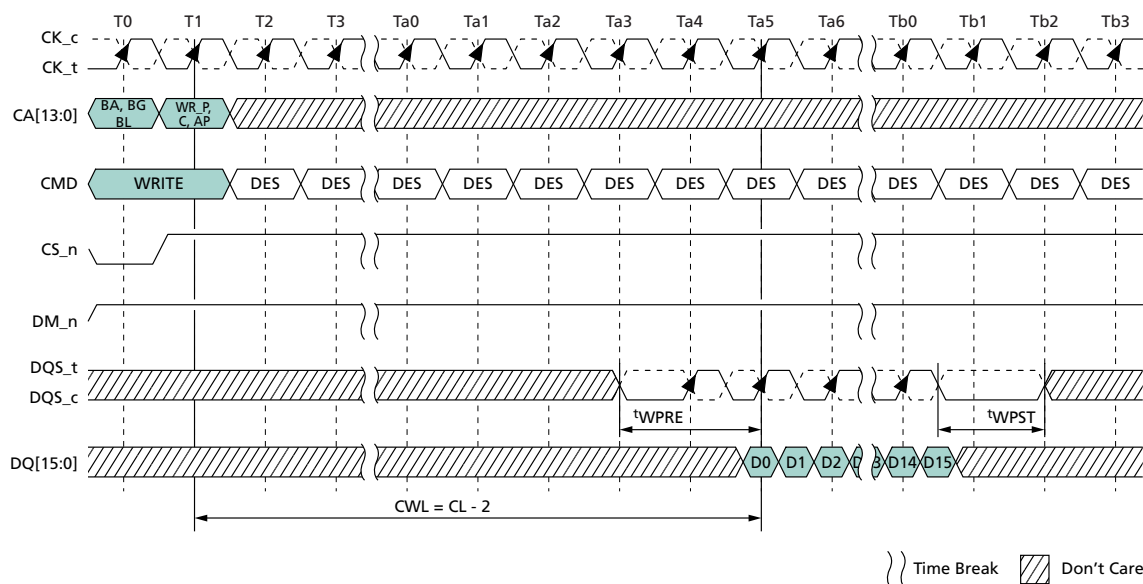
Partial Write

When the Partial Write function is enabled (WR_P = LOW), as part of the WRITE command, it helps start an internal read for READ-MODIFY-WRITE operation during masked writes. This partial write (WR_P = LOW) functionality must be used in conjunction with the DM_n data. If WR_partial = HIGH during write, the mask data on DM_n must be HIGH. If DM is disabled MR5:OP[5], WR_P must be HIGH. DM_n may be HIGH or LOW.

WRITE Burst Operation

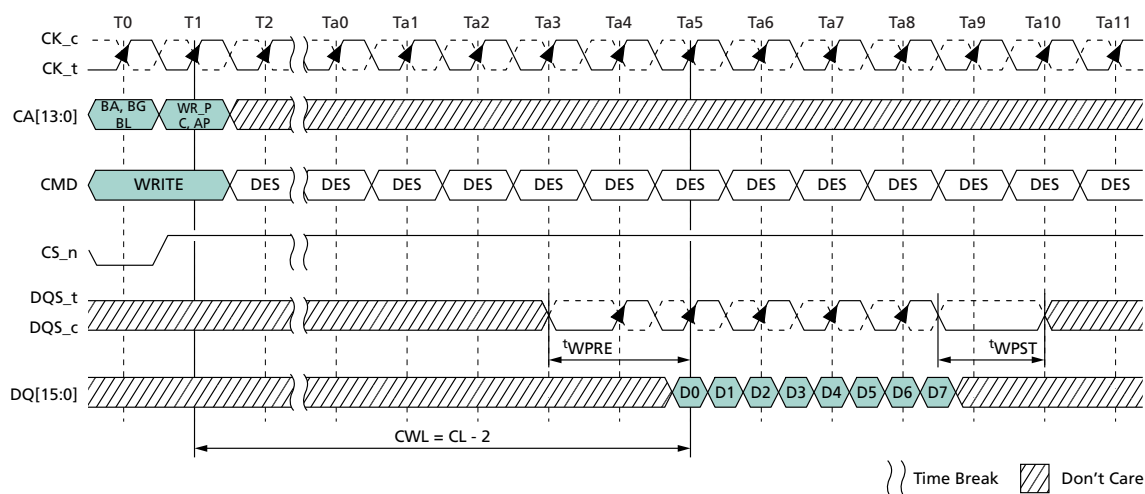
In the following example write timing figures, the details of each write parameter are defined separately for improved understanding. For clarity of illustration, CK and DQS are shown aligned; DQS and DQ are shown center-aligned. Offset between CK and DQS and between DQS and DQ may be appropriate.

Figure 43: WRITE Burst Operation (BL16)



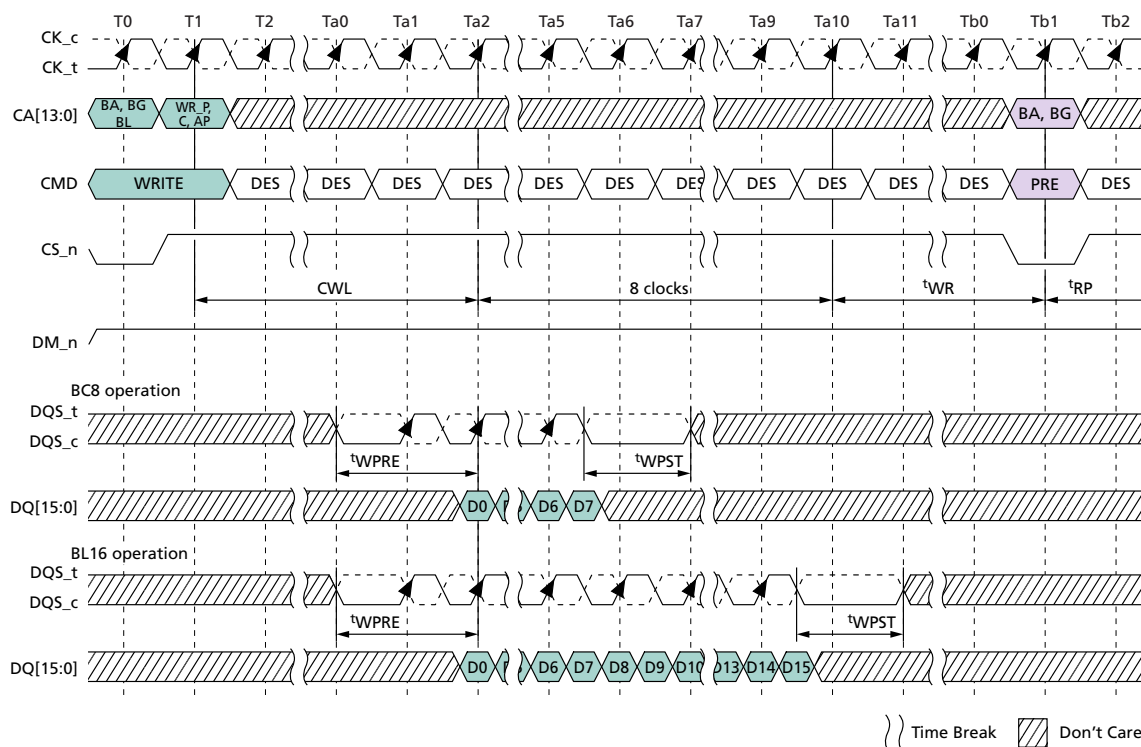
- Notes: 1. BL = 16; preamble = 2^tCK 0010 pattern; postamble = 1.5^tCK .
 2. Dn = data-in from column n.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 4. The DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

Figure 44: WRITE Burst Operation (BC8 OTF)



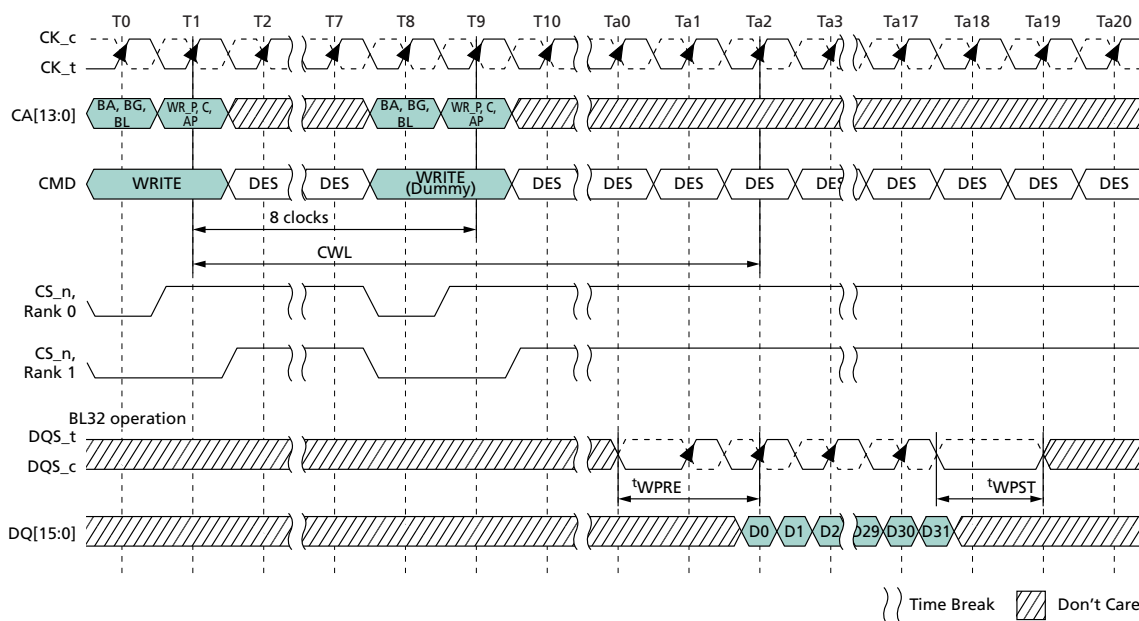
- Notes: 1. BC = 8; preamble = 2^tCK , postamble = 1.5^tCK .
 2. Dn = data-in from column n.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 4. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.
 5. The DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

Figure 45: WRITE (BL16) to PRECHARGE Operation with 2 t^{CK} Preamble



- Notes:
1. BL = 16 or BC = 8; preamble = 2 t^{CK} - 0010 pattern; postamble = 1.5 t^{CK} .
 2. Dn = data-in from column n.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 4. t^{WR} is referenced from the first rising clock edge after the last write data shown at Ta10. t^{WR} specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
 5. The DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

Figure 47: Write Timing for Fixed BL32 and BL32 OTF Mode



Notes: 1. BL = 32; preamble = 2^tCK ; postamble = 1.5^tCK .

2. Dn = data-in from column n.

3. DES commands are shown for ease of illustration; other commands may be valid at these times.

4. A dummy WRITE command is required for the second half of the transfer with a delay of 8 clocks from the first WRITE command.

5. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.

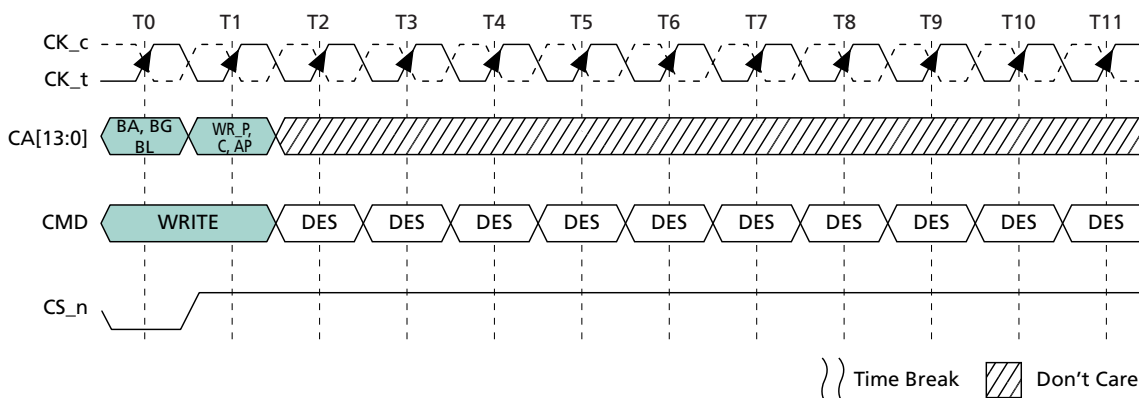
6. C10 is used for burst ordering and must be LOW for the first WRITE command and HIGH for the dummy WRITE command.

7. The device supports an optional fixed BL32 mode and optional BL32 on-the-fly (OTF) mode for x4 devices only.

8. CA bits other than C10 and AP in dummy WRITE command are the same as the first WRITE command.

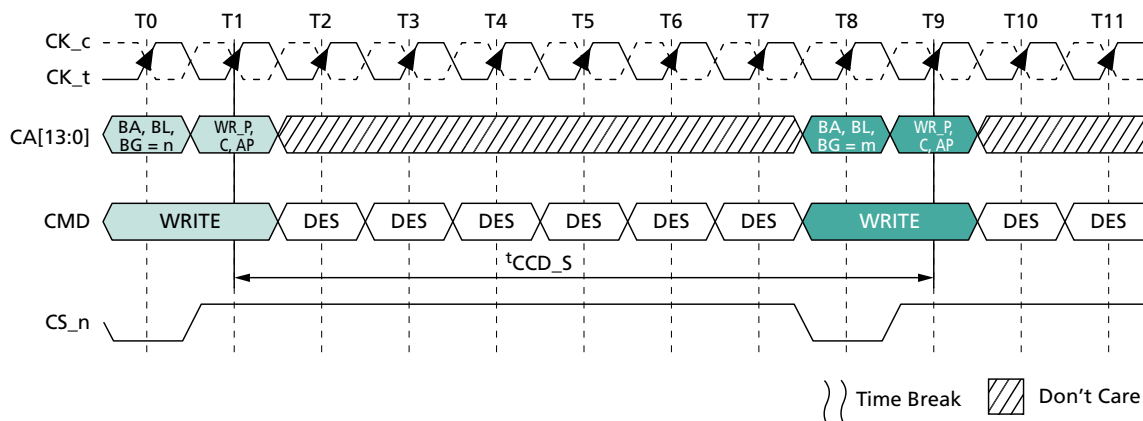
9. The DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

Figure 48: Write Timing for BL16 in BL32 OTF Mode



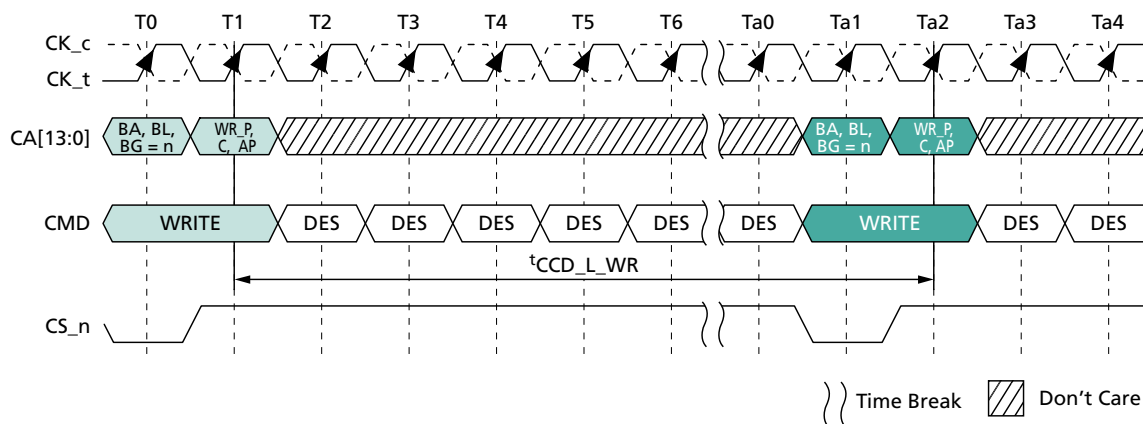
- Notes: 1. The figure shows BL16 WRITE operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy WRITE command is required because the data transfer size is BL16.
2. DES commands are shown for ease of illustration; other commands may be valid at these times.
3. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 49: Write-to-Write to Different Bank Group for BL16 in BL32 OTF



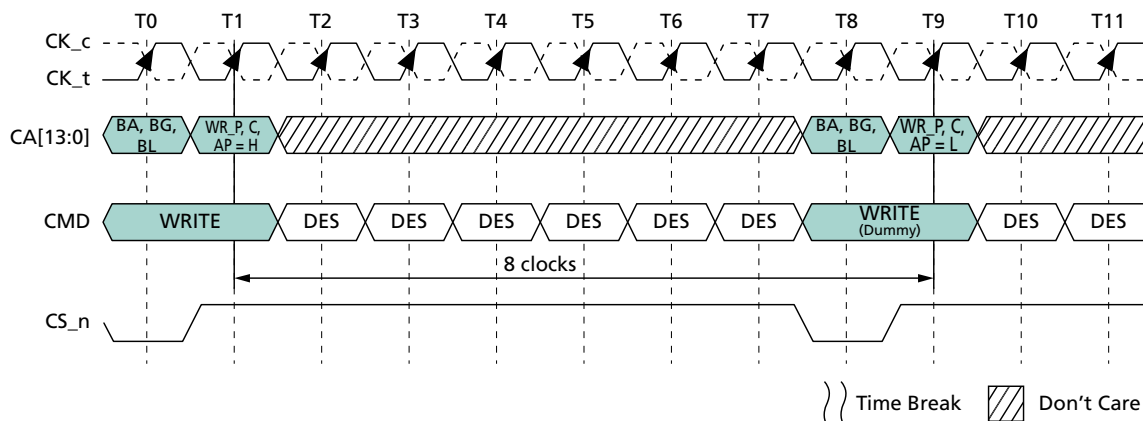
- Notes: 1. Figure shows back-to-back BL16 writes to different bank groups.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 50: Write-to-Write to Same Bank Group for BL16 in BL32 OTF



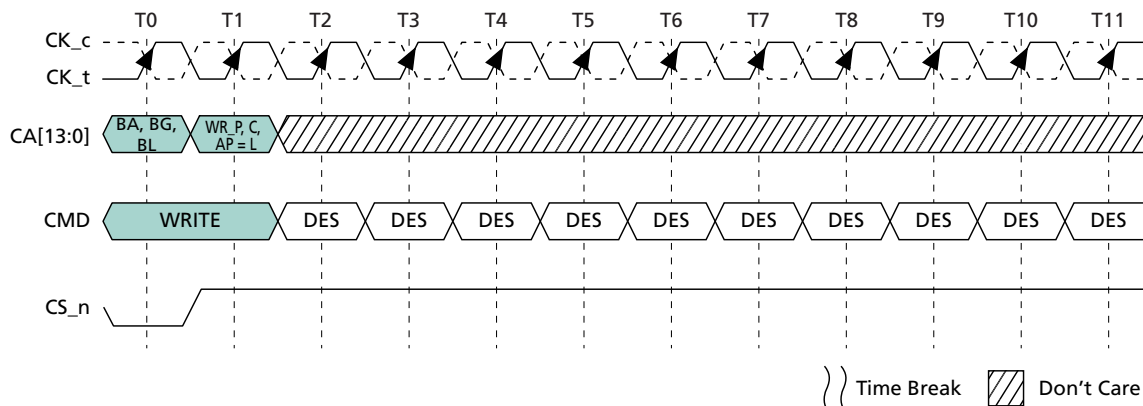
- Notes: 1. Figure shows back-to-back BL16 writes to the same bank group using a timing of t_{CCD_L_WR}.
2. Back-to-back BL32 writes to the same bank group have a minimum separation of 16 clocks.
3. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 51: Write with Auto Precharge for Fixed BL32 and BL32 OTF



- Notes: 1. The AP bit must be set HIGH for the first WRITE command and LOW for the dummy WRITE command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.
3. CA bits other than C10 and AP in dummy WRITE command are the same as the first WRITE command.

Figure 52: Write with Auto Precharge for BL16 in BL32 OTF Mode



- Notes: 1. The AP bit must be set LOW with the WRITE command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Same Bank Group Write-to-Write Timings

DDR5 devices have different same bank group write-to-write timings, based on whether the second write requires read-modify-write (RMW) access or just-write (JW) access. In JW access, the device updates all 128 bits of data on the addressed codeword, while in RMW access, a part of 128 bits is updated.

Table 166: JW Access and RMW Access Definition

Configuration	BL16		BC8		Optional BL32	Notes
	Normal	Data Mask	Normal	Data Mask		
x4	RMW	-	RMW	-	JW	1,2,3
x8/x16	JW	RMW	RMW		-	1,2,3

- Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
2. Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11b) where WRITE command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10b).

3. Data mask refers to data mask mode enabled by MR5 OP[5]=1 and WRITE command with WP=L issued.

Table 167: Same Bank Group Write Access to RMW Access Timings

From	To		Notes
	BL16	BC8	
BL16	$t_{\text{CCD\_L\_WR}}$	$t_{\text{CCD\_L\_WR}}$	1,2,3
BC8	$t_{\text{CCD\_L\_WR}}$	$t_{\text{CCD\_L\_WR}}$	1,2,3
Optional BL32	$8\text{nCK} + t_{\text{CCD\_L\_WR}}$	-	1,2,3,4,5

- Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
2. Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11b) where WRITE command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10b).
3. With Optional BL32, this timing table is regarding the first command, not the dummy command.
4. There is no BL32 to BC8 case.
5. When Write CRC is enabled, the timing increases by 1nCK (that is, $9\text{nCK} + t_{\text{CCD\_L\_WR}}$).

Table 168: Same Bank Group Write Access to JW Access Timings

From	To		Notes
	BL16	Optional 32	
BL16	$t_{\text{CCD\_L\_WR2}}$	$t_{\text{CCD\_L\_WR2}}$	1,2,3
BC8	$t_{\text{CCD\_L\_WR2}}$	-	1,2,3,4
Optional BL32	-	$8\text{nCK} + t_{\text{CCD\_L\_WR2}}$	1,2,3,5

- Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
2. Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11b) where WRITE command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10b).
3. With Optional BL32, this timing table is regarding the first command, not the dummy command.
4. There is no BL32 to BC8 case.
5. When Write CRC is enabled, the timing increases by 1nCK (that is, $9\text{nCK} + t_{\text{CCD\_L\_WR}}$).

Different Bank Group Write-to-Write Timings

Table 169: Different Bank Group Write-to-Write Timings

From	To			Notes
	BL16	BC8	Optional BL32	
BL16	8 nCK	8 nCK	8 nCK	1,2,3
BC8	8 nCK	8 nCK	-	1,2,3,4
Optional BL32	16 nCK	-	16 nCK	1,2,3,4

- Notes: 1. BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
2. Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11b) where WRITE command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10b).
3. With Optional BL32, this timing table is regarding the first command, not the dummy command.
4. There is no BC8 to BL32 case (and vice versa).

$$t_{WPRE\_EN\_ntck} \geq |t_{DQSS} (MIN)| + t_{DQSS} (MAX) + |t_{DQSD} (MIN)| + t_{DQSD} (MAX)$$

Figure 54: t_{DQSS} – External CLK-to-DQS Variation

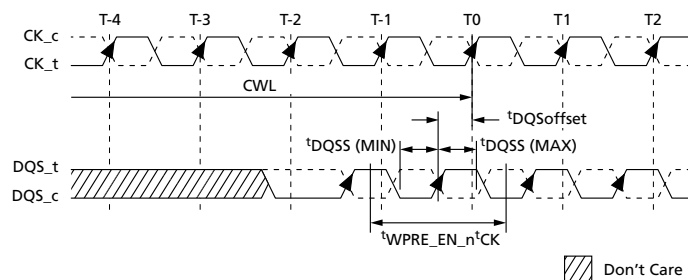
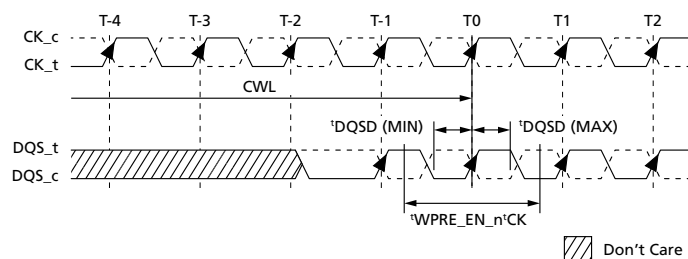


Figure 55: t_{DQSD} – Internal CLK-to-DQS Variation



Module Rank and Channel Limitations for DIMMs During WRITE Operations

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for WRITE operations occurring on a single module. Additionally, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply to limit localized power delivery noise on the module.

To provide best performance, the different channels may initiate commands on the same cycle provided the rank-to-rank timings are met, the maximum number of DRAMs in a given WRITE operation is not exceeded, and the applicable component timings shown elsewhere in this specification are met. Timing and operational relationships for DDR5 DIMMs are shown below.

Table 170: Module Rank and Channel Timings for DDR5 DIMMs

DIMM Configuration	Maximum Number of Die Simultaneous or Overlapping Activity	
	WRITE, WRITE-PATTERN	
	Die per Channel	Die per DIMM
SR x16	No restrictions	
DR x16	2	4
SR x8	No restrictions	
DR x8	5	10
SR x4	No restrictions	
DR x4	10	20
DR x4 (2H 3DS)	10	20
QR x4 (DDP)	10	20
DR x4 (4H 3DS)	10	20
DR x4 (8H 3DS)	10	20

- Notes:
1. Any combination of commands, with up to the maximum of die per channel and per DIMM, per condition is allowed.
 2. t_{CCD} parameters must be met for WRITE and WRITE-PATTERN commands to different logical ranks or physical ranks within the same channel; no overlapping write data bus activity is allowed on two physical or logical ranks within the same channel.
 3. WRITE and WRITE-PATTERN commands to different channels do not require stagger.
 4. Each rank consists of one group of DRAMs making up a 36- or 40-bit channel (32 bits for non-ECC DIMMs).
 5. Restrictions apply to some DIMMs built with JESD301-1 PMIC 50x0 Specification, but may not apply to DIMMs built with higher current capacity PMICs.

Write Timing Violations

Motivation

Generally, if write timing parameters are violated, a complete reset/initialization procedure has to be initiated to ensure the device works properly. However, for certain violations specified below, the device is guaranteed to not “hang up,” and that errors are limited to that particular operation.

For the following, assume that there are no timing violations with regards to the WRITE command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

Data Setup and Hold Offset Violations

If the required data to strobe timing or voltage parameters are violated for any of the data/strobe timing edges or data/strobe voltage limits associated with a WRITE burst data eye (for example: $t_{Rx\_DQ\_Margin}$, t_{Rx_DQS2DQ} , VRx_DQS , VRx_DQ , etc.), incorrect data might be written to the memory locations addressed with this WRITE command.

Subsequent reads from that location might result in unpredictable read data; however, the device will work properly otherwise.

Strobe and Strobe to Clock Timing Violations

Should the strobe timing requirements (t_{WPRE} , t_{WPST}) or the strobe to clock timing requirements (t_{DQSS} , $t_{DQSoffset}$) be violated for any of the strobe edges associated with a WRITE burst, then wrong data might be written to the memory location addressed with the offending WRITE command.

Subsequent reads from that location might result in unpredictable read data; however, the DRAM will work properly otherwise with the following constraints:

1. Both write CRC and data burst OTF are disabled; timing specifications other than t_{WPRE} , t_{WPST} , t_{DQSS} , $t_{DQSoffset}$ are not violated.
2. The offending write strobe (and preamble) arrive no earlier or later than six DQS transition edges from the write latency position.
3. A READ command following an offending WRITE command from any open bank is allowed.
4. One or more subsequent WR or a subsequent WRA {to same bank as offending WR} may be issued t_{CCD_L} later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
5. One or more subsequent WR or a subsequent WRA {to a different bank group} may be issued t_{CCD_S} later but incorrect data could be written; subsequent WR and WRA can be either offending or non-offending writes. Reads from these writes may provide incorrect data.
6. Once one or more precharge commands (PREpb, PREsb or PREab) are issued to device after offending WRITE command and all banks become precharged state (idle state), a subsequent, non-offending WR or WRA to any open bank shall be able to write correct data.
7. DQS strobes including preamble must align to each WRITE commands data burst length configuration. If the DRAM fails to capture or incorrectly de-serializes the incoming data stream because of misalignment or missing strobe edges, errors may occur. These errors will propagate

indefinitely until the DRAM is put into an idle state, i.e., all banks are in the precharged state with t_{RP} satisfied.

WRITE PATTERN and WRITE PATTERN AUTO PRECHARGE Commands

Because of the significant percentage of writes that contain all zeros, the WRITE PATTERN command is being included in the DDR5 specification.

The WRITE PATTERN (WRP) and WRITE PATTERN AUTO PRECHARGE (WRPA) commands can save power and improve performance by not actually sending a specific data pattern (such as all-zeros) across the external data bus.

These commands operate very similar to a standard WRITE (WR) or WRITE AUTO PRECHARGE (WRA) commands except for a few important differences: the data pattern written is the contents of MR48 instead of the data on the external DQ bus, toggling of DQ and DQS is therefore unnecessary, and the device does not turn on internal ODT. ECC parity is based on the write pattern mode data in MR48.

Upon receiving the WRP or WRPA command, the device sources the input for the memory array from the write pattern mode registers instead of from the DQs. The DQ mapping across the burst is shown the Write Pattern DQ Output Mapping table that follows. The host does not send any data during this time.

All timing constraints are still measured from the clocks where the WRITE command data would have transferred. For example, ^tWR is measured from the end of the write burst to the PRE command (shown in the WRITE PATTERN command example figure that follows).

The pattern used for this mode is in defined by the contents of MR48:OP[7:0]. That pattern can be all zeros, all ones, or something else, and can be changed with a MRW command to MR48. The power-on default for this mode register is all zeros. The WRP and WRPA commands support burst lengths of BL16 and BL32, and do not support BC8 OTF or BL32 OTF.

The table that follows details how the pattern stored in MR48 will be mapped in the device array across the DQ bits and burst. The pattern is described as follows:

- In the case of a x4 device, only OP[3:0] is used with each bit of pattern corresponding to DQ[3:0], respectively. The same OP value is repeated over the entire burst for that bit (DQ0 stores OP0 on every UI of the burst). Although OP[7:4] are not used for the x4 device, the previously programmed MRW values are still read during a MRR (OP[7:4] does not revert to the default 0).
- In the case of a x8 device, the whole pattern OP[7:0] is used, with each bit of the pattern corresponding to DQ[7:0], respectively. The same OP[7:0] pattern is repeated over the entire burst for that bit. (DQ0 stores OP0 on every UI of the burst.)
- In the case of a x16 device, the whole pattern OP[7:0] is used, with each bit of the pattern corresponding to DQ[7:0], respectively, and then that pattern is repeated for DQ[15:8]. The same OP[7:0] pattern is repeated over the entire burst for that bit (DQ0 store OP0 on every UI of the burst).

The BL supported in write pattern mode is based on MR0:OP[1:0]; however WRP and WRPA do not support on-the-fly (OTF), limiting the choice to either fixed BL16 or BL32.

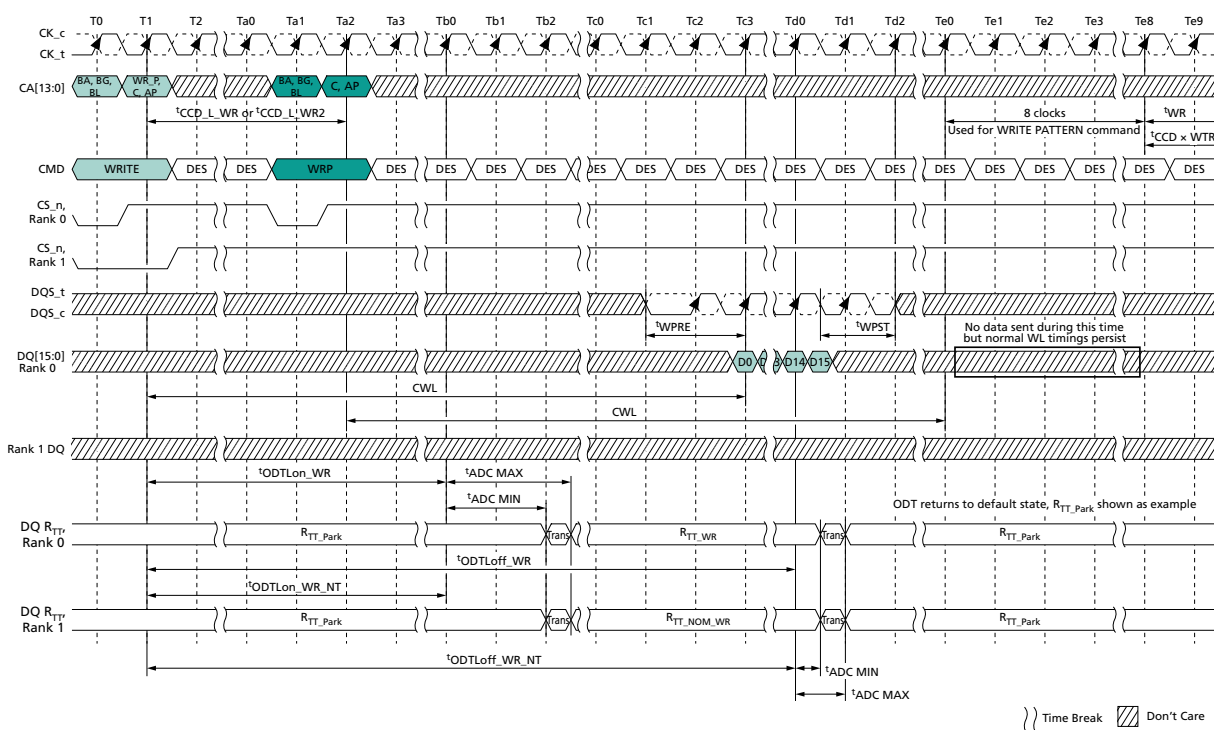
Table 171: Write Pattern DQ Output Mapping

Config	BL16 x16	BL16 x8	BL16 x4	BL32 x4
UI	0–15	0–15	0–15	0–31
DQ0	OP0	OP0	OP0	OP0
DQ1	OP1	OP1	OP1	OP1
DQ2	OP2	OP2	OP2	OP2
DQ3	OP3	OP3	OP3	OP3
DQ4	OP4	OP4	–	–

Table 171: Write Pattern DQ Output Mapping (Continued)

Config	BL16 x16	BL16 x8	BL16 x4	BL32 x4
UI	0–15	0–15	0–15	0–31
DQ5	OP5	OP5	—	—
DQ6	OP6	OP6	—	—
DQ7	OP7	OP7	—	—
DQ8	OP0	—	—	—
DQ9	OP1	—	—	—
DQ10	OP2	—	—	—
DQ11	OP3	—	—	—
DQ12	OP4	—	—	—
DQ13	OP5	—	—	—
DQ14	OP6	—	—	—
DQ15	OP7	—	—	—
DML_n/DML_n	INVALID	INVALID	—	—
DMU_n	INVALID	—	—	—

Figure 56: Example of WRITE PATTERN Command



Notes: 1. See the [JW Access and RMW Access Definition Table](#) for guidance.

- BC8 refers to BC8 OTF mode enabled by MR0 OP[1:0]=01 and WRITE command with BL=L issued.
- Optional BL32 refers to BL32 OTF mode (enabled by MR0 OP[1:0]=11b) where WRITE command is issued with BL=L in CA5, or BL32 fixed mode (enabled by MR0 OP[1:0]=10b).
- Data mask refers to data mask mode enabled by MR5 OP[5]=1 and WRITE command with WP=L issued.

- The DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

READ Operations

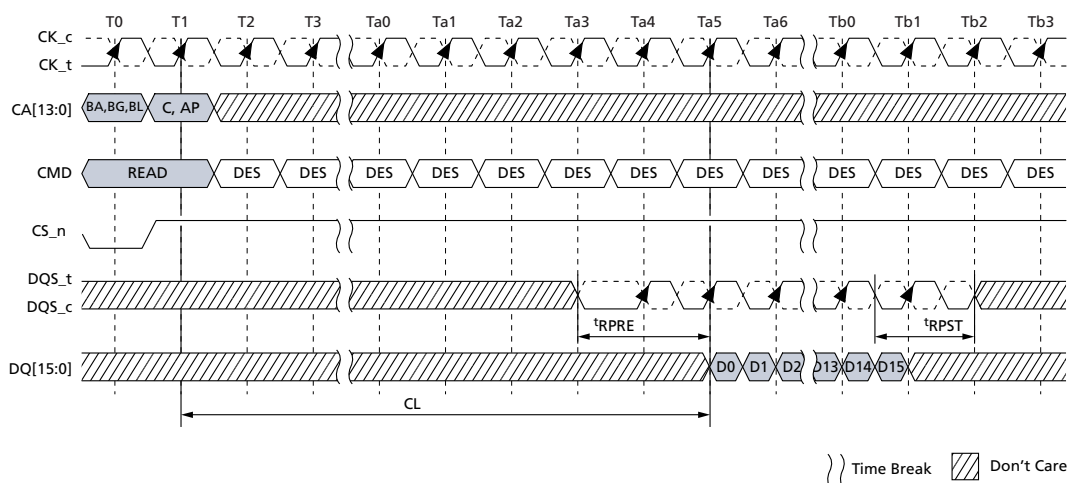
The READ operation causes the device to retrieve and output data stored in its array. The READ operation is initiated by the READ command during which the beginning column address and bank/group address for the data to be retrieved from the array is provided. The retrieved data is driven on to the DQ pins CL cycles after the READ command along with the proper waveform on the DQS inputs. CL is defined from the READ command to data and is not affected by the read DQS offset timing MR40:OP[2:0].

In these read timing diagrams, for clarity of illustration, CK and DQS are shown aligned. As well, DQS and DQ are shown center-aligned. Offset between CK and DQS, and between DQS and DQ may be approximate.

READ Burst Operation

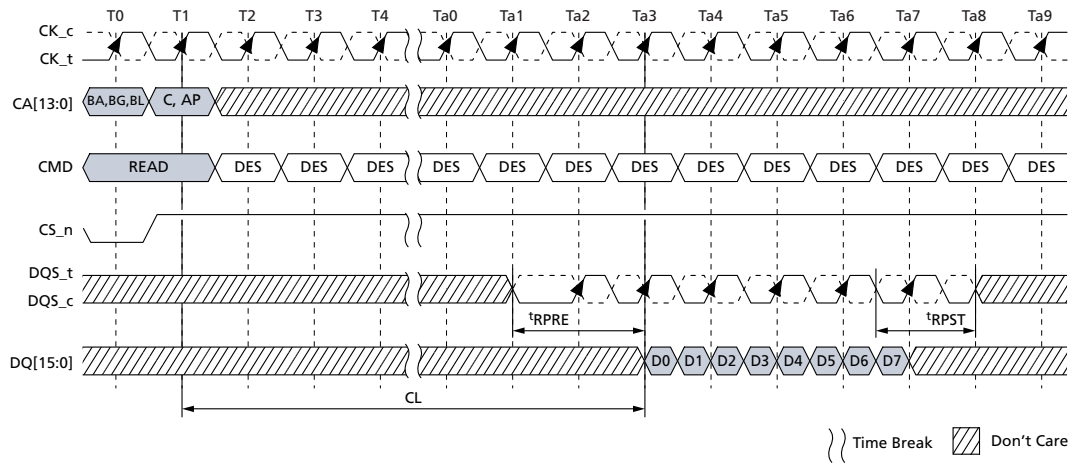
The device supports BL16, BC8 OTF, BL32 (optional), or BL32 OTF (optional) during the READ or WRITE command (auto precharge can be enabled or disabled based on the state of the CA10 pin during the 2nd cycle of the command). MR0[1:0] is used to select BL16, BC8 OTF, BL32 OTF, or BL32 operation mode.

Figure 57: READ Burst Operation (BL16)



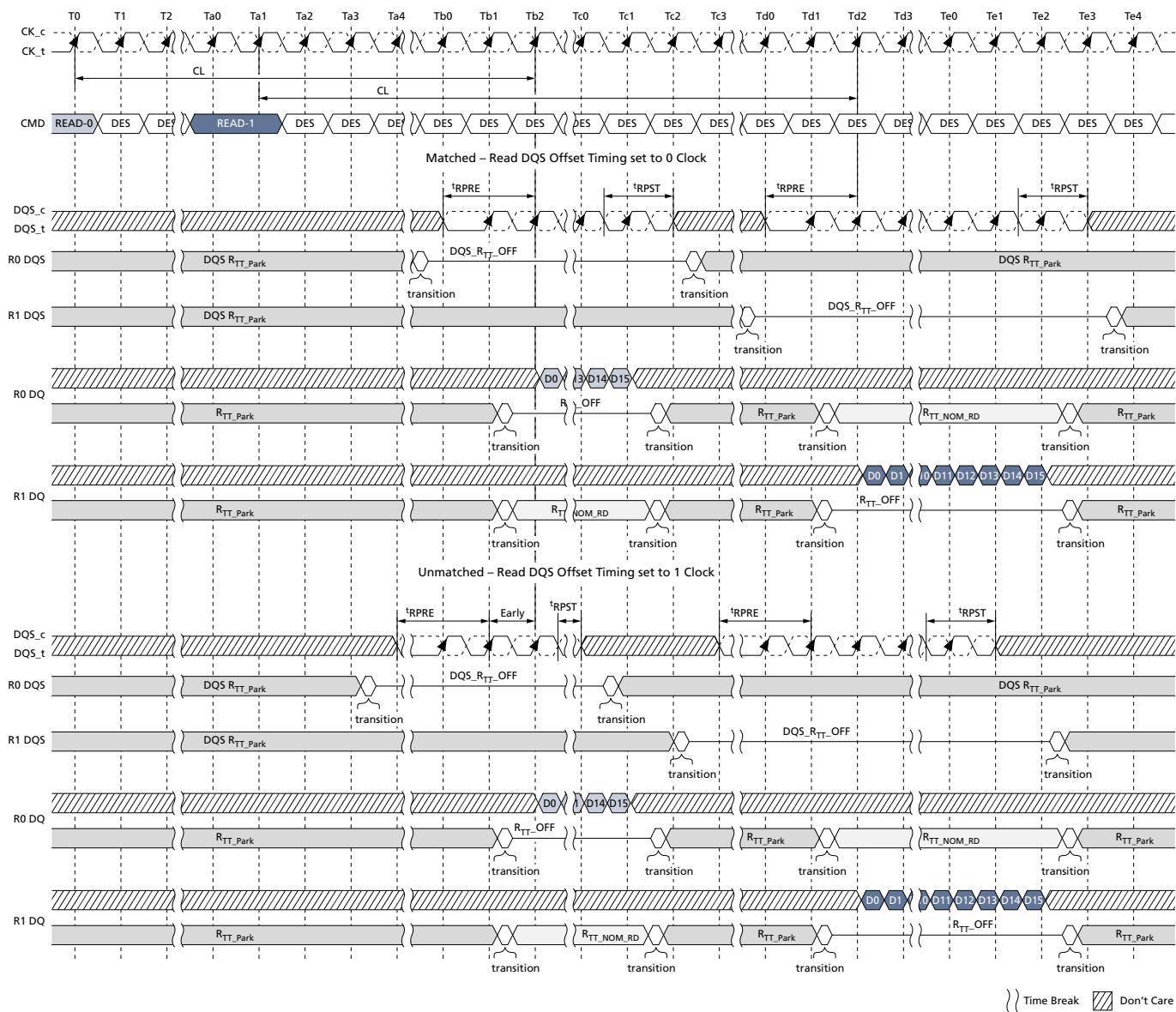
- Notes:
- BL = 16; preamble = 2^tCK 0010 pattern; postamble = 1.5^tCK.
 - D_n = data-out from column n.
 - DES commands are shown for ease of illustration; other commands may be valid at these times.
 - In this example, read DQS offset timing is set to 0 clocks.

Figure 58: READ Burst Operation (BC8 OTF)



- Notes:
1. BL = 8; preamble = 2^tCK 0010 pattern; postamble = 1.5^tCK .
 2. Dn = data-out from column n.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 4. In this example, read DQS offset timing is set to 0 clocks.
 5. In non-CRC mode, DQS_t and DQS_c stop toggling at the completion of the BC8 data bursts, plus the postamble.

Figure 59: READ to READ, Different Ranks Operation With Read DQS Offset Usage (BL16)



Notes: 1. BL = 16; preamble = 2^tCK 0010 pattern; postamble = 1.5^tCK .

2. Dn = data-out from column n.

3. DES commands are shown for ease of illustration; other commands may be valid at these times.

4. Two different examples are shown side by side: The top with the default setting for read DQS offset = 0 clocks; the lower with a 1 clock setting. In the lower case, the DQS is started 1 clock earlier than normal with respect to CL. In both cases, the data does not move.

Burst READ Operation Followed by a Precharge

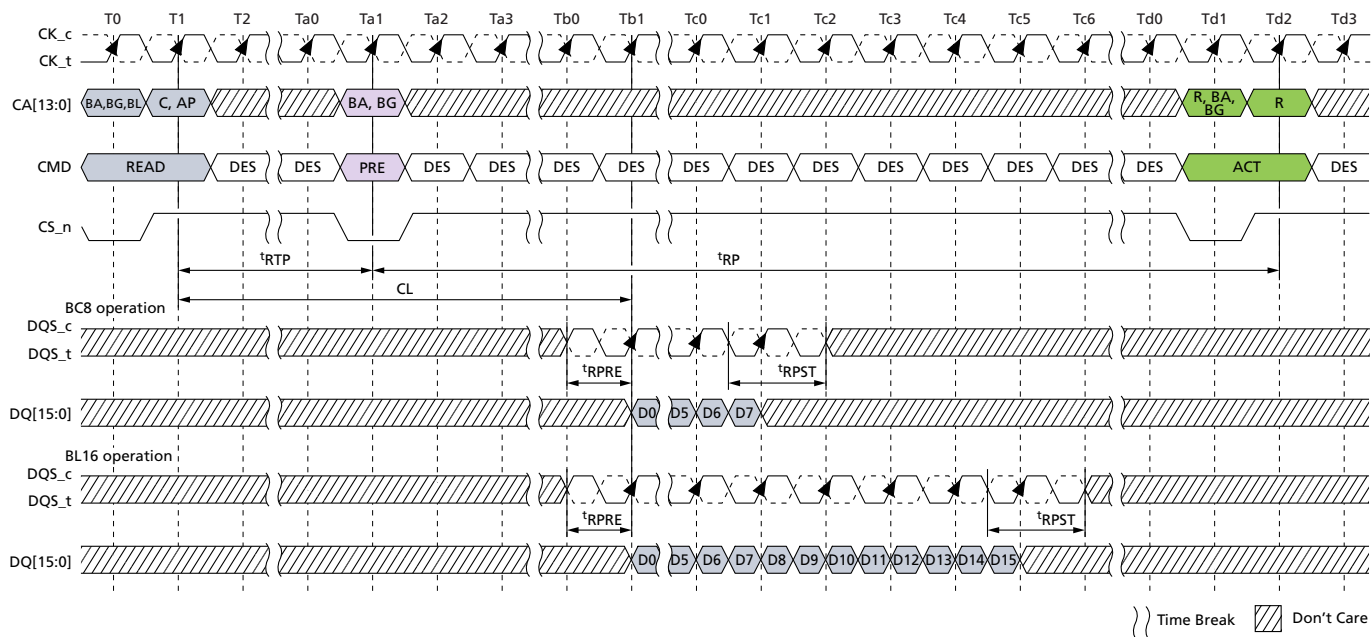
The minimum external READ command to PRECHARGE command spacing to the same bank is equal to t_{RTP} with t_{RTP} being the internal READ command to PRECHARGE command delay. Note that the minimum ACT to PRE timing, t_{RAS} , must be satisfied as well. The minimum value for the internal READ command to PRECHARGE command delay is given by $t_{RTP,min}$. A new bank ACTIVE command may be issued to the same bank if the following two conditions are satisfied simultaneously.

The minimum RAS precharge time ($t_{RP,min}$) has been satisfied from the clock at which the precharge begins.

The minimum RAS cycle time ($t_{RC,min}$) from the previous bank activation has been satisfied.

Examples of READ commands followed by precharge are shown below.

Figure 60: READ to PRECHARGE, With 1^tCK Preamble



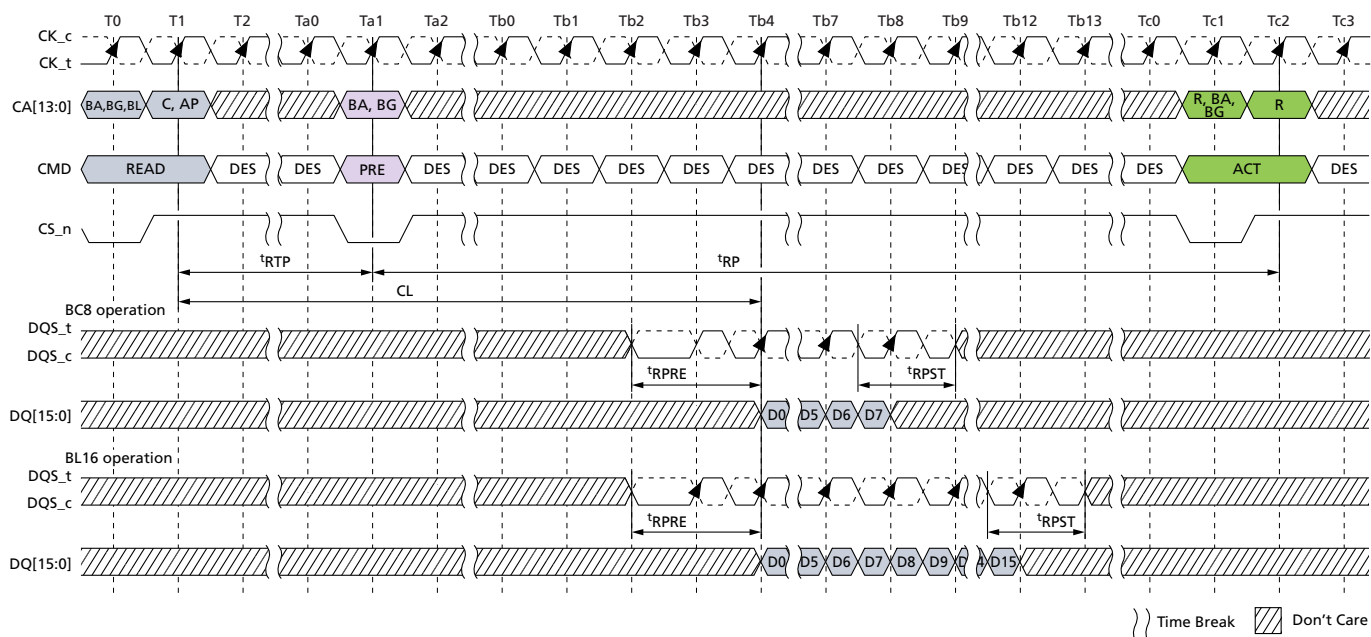
Notes: 1. BL = 16; preamble = 1^tCK; postamble = 1.5^tCK.

2. Dn = data-out from column n.

3. DES commands are shown for ease of illustration; other commands may be valid at these times.

4. The example assumes $t_{RAS,min}$ is satisfied at PRECHARGE command time (t_{a1}) and that $t_{RC,min}$ is satisfied at the next ACTIVE command time (t_{d2}).

Figure 61: READ to PRECHARGE, With 2^tCK Preamble



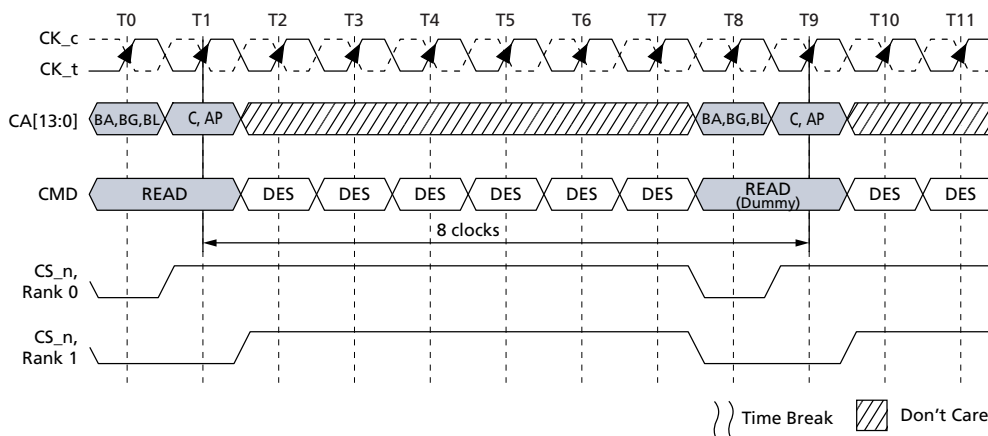
- Notes:
1. BL = 16; preamble = 2^tCK 0010 pattern; postamble = 1.5^tCK.
 2. Dn = data-out from column n.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.
 4. The example assumes $t_{RAS,min}$ is satisfied at PRECHARGE command time (t_{a1}) and that $t_{RC,min}$ is satisfied at the next ACTIVE command time (t_{d2}).

READ Burst Operation for Optional BL32 Mode

The following read timing diagrams cover read timings for fixed BL32, BL32 in BL32 OTF mode, and BL16 in BL32 OTF mode for x4 devices only.

A dummy READ command is required for the second half of the transfer of BL32. If non-target ODT is needed in the system, then a dummy ODT command must be issued to the non-target rank for the second half of the transfer of BL32.

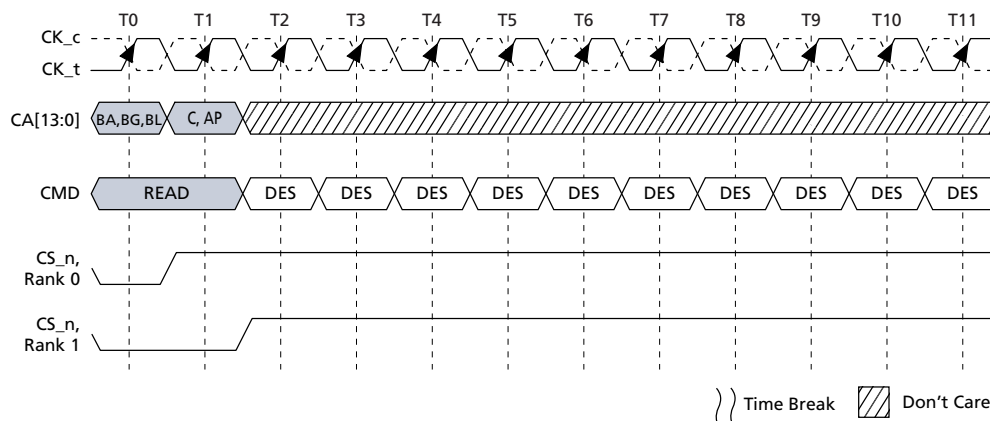
Figure 62: Read Timing for Fixed BL32 and BL32 in BL32 OTF Mode



- Notes:
1. DES commands are shown for ease of illustration; other commands may be valid at these times.

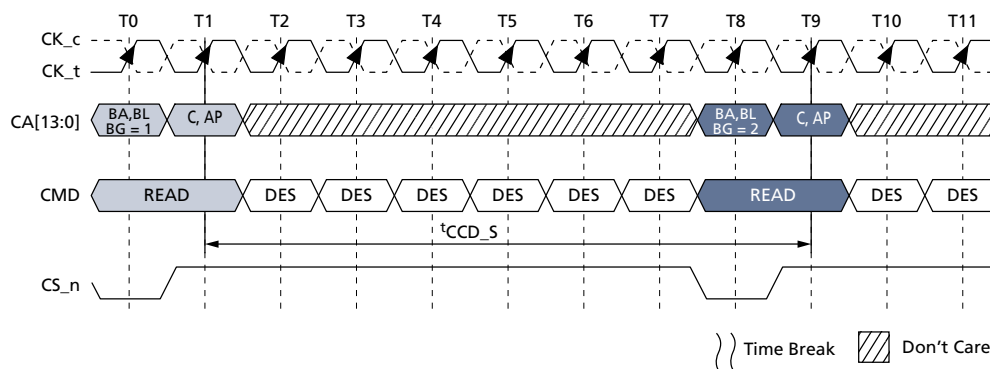
2. A dummy READ command is required for the second half of the transfer with a delay of 8 clocks from the first READ command.
3. The figure also shows a dummy ODT command being issued to non-target rank 1 for the second half of the transfer.
4. C10 is used for burst ordering and can be LOW or HIGH for the first READ command. C10 for the dummy READ command must be the opposite value from the first READ command.
5. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.
6. CA bits other than C10 and AP in the dummy READ command are the same as the first READ command.

Figure 63: READ Timing for BL16 in BL32 OTF Mode



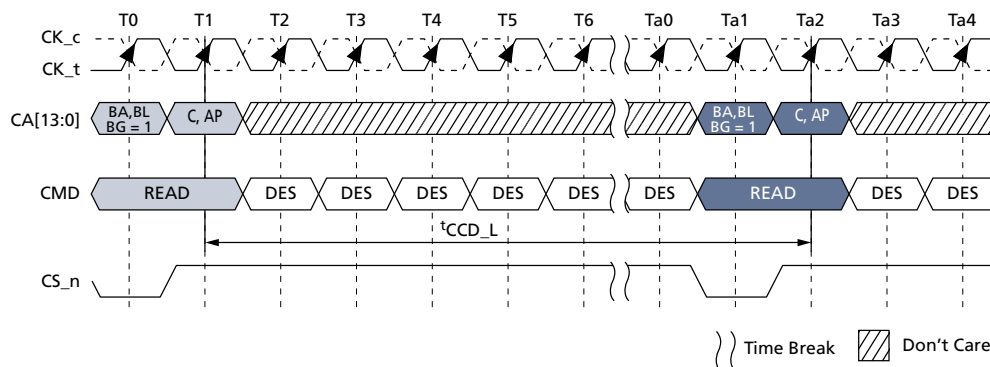
- Notes:
1. The figure shows BL16 READ operation when MR0 is programmed to use BL32 OTF mode. In this case, no dummy READ command is required as transfer size is BL16.
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.
 3. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 64: READ to READ to Different Bank Group for BL16 in BL32 OTF



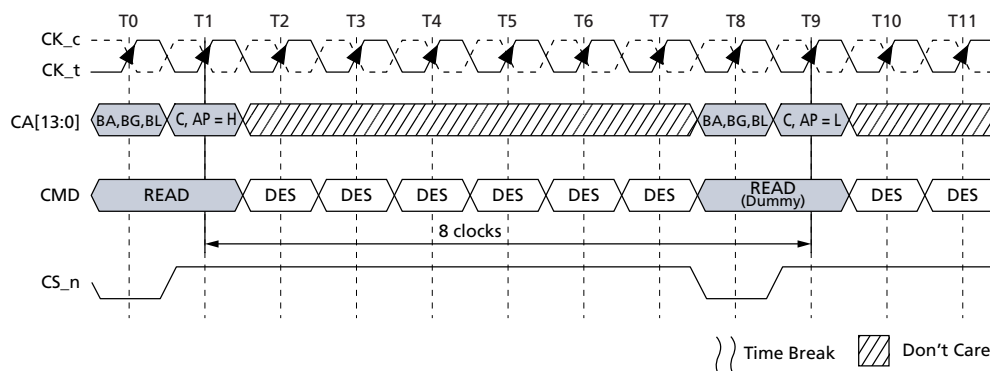
- Notes:
1. The figure shows back-to-back BL16 reads to different bank groups.
 2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 65: READ to READ to Same Bank Group for BL16 in BL32 OTF



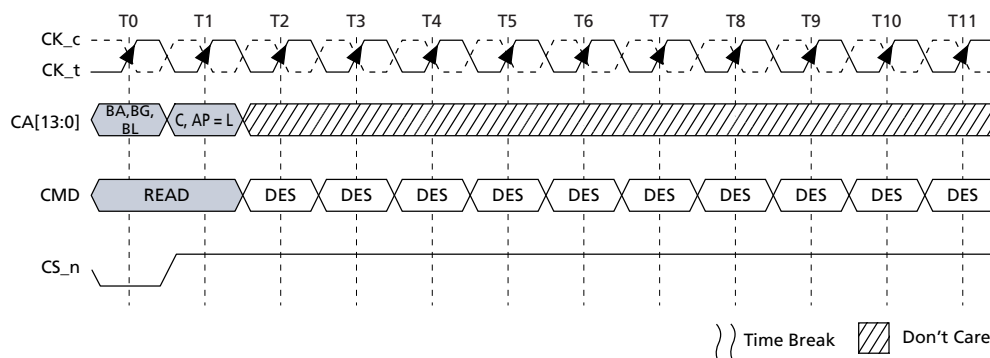
- Notes: 1. The figure shows back-to-back BL16 reads to same bank group using a timing of t_{CCD_L} .
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

Figure 66: READ to READ With Auto Precharge for Fixed BL32 and BL32 in BL32 OTF Mode



- Notes: 1. AP bit must be set HIGH for first READ command and LOW for dummy READ command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.
3. CA bits other than C10 and AP in dummy READ command are the same as the first READ command.

Figure 67: READ With Auto Precharge for BL16 in BL32 OTF Mode



- Notes: 1. AP bit must be set LOW with the READ command.
2. The device supports an optional fixed BL32 mode and optional BL32 OTF mode for x4 devices only.

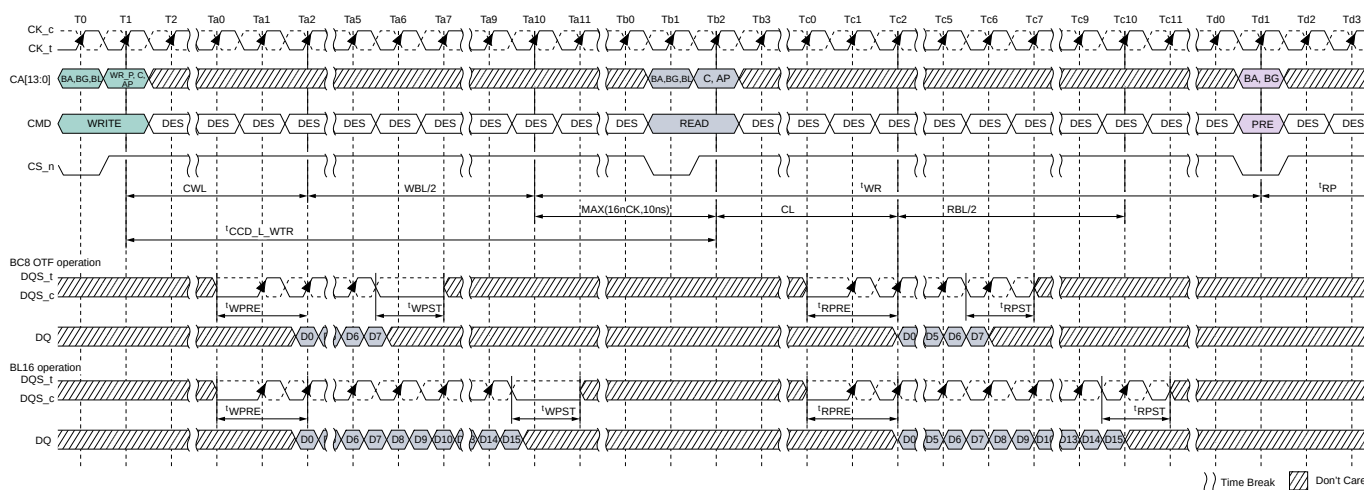
READ and WRITE Command Interval

READ to WRITE as well as WRITE to READ command interval timing requirements are described in the following tables.

Table 172: Minimum READ and WRITE Command Timings (3200-8800)

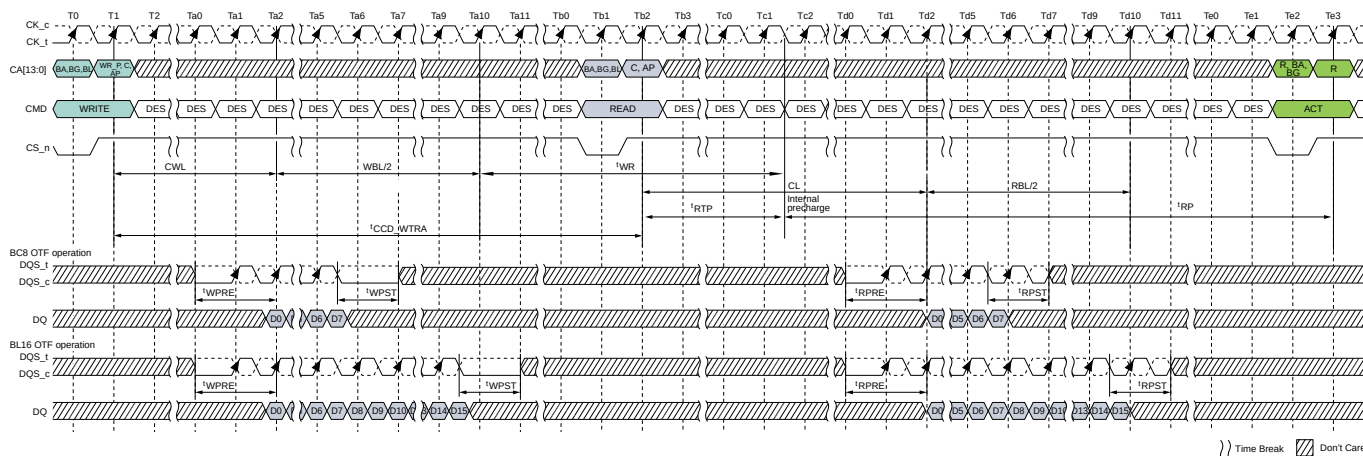
Bank Group	Parameter (MIN)	Symbol
Same	READ-to-WRITE	$t_{\text{CCD\_L\_RTW}}$
	WRITE-to-READ	$t_{\text{CCD\_L\_WTR}}$
	WRITE-to-READ AP, same bank	$t_{\text{CCD\_WTRA}}$
Different	READ-to-WRITE	$t_{\text{CCD\_L\_RTW}}$
	WRITE-to-READ	$t_{\text{CCD\_S\_WTR}}$

Figure 68: WRITE to READ Timing



- Notes:
1. BC OTF = 8 or BL = 16; preamble = $2^t\text{CK} - 0010$ pattern; postamble = 1.5^tCK .
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.
 3. The write recovery time (t_{WR}) is referenced from the first rising clock edge after the last write data shown at Ta10. t_{WR} specifies the last burst write cycle until the PRECHARGE command can be issued to the same bank.
 4. The DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

Figure 69: WRITE to READ With Auto Precharge in the Same Bank Timing



- Notes:
1. BC OTF = 8 or BL = 16; preamble = 2^tCK - 0010 pattern; postamble = 1.5^tCK .
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.
 3. The write recovery time (t_{WR}) is referenced from the first rising clock edge after the last write data shown at Ta_{10} . The internal precharge after the read with auto precharge cannot begin before t_{WR} is satisfied, which is equivalent to $t_{CCD\_WTRA} + t_{RTP}$.
 4. The DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

READ and WRITE Command Interval for Optional BL32 Modes

READ to WRITE as well as WRITE to READ command interval timing requirements for BL32 modes of operation are described in the following tables.

Table 173: Minimum READ to READ Command Timings – Same Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	t_{CCD_L}	t_{CCD_L}	1
BL32 in BL32 OTF mode	$\text{Max}(16n\text{CK}, 5\text{ns})$	$\text{Max}(16n\text{CK}, 5\text{ns})$	1

Note: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

Table 174: Minimum READ to READ Command Timings – Different Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	t_{CCD_S}	t_{CCD_S}	1
BL32 in BL32 OTF mode	$2 * t_{CCD\_S}$	$2 * t_{CCD\_S}$	1

Note: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

Table 175: Minimum WRITE to WRITE Command Timings – Same Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	$t_{CCD\_L\_WR}$	$t_{CCD\_L\_WR2}$	1
BL32 in BL32 OTF mode	$8n\text{CK} + t_{CCD\_L\_WR}$	$9n\text{CK} + t_{CCD\_L\_WR2}$	1

Note: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

DDR5 x8 and x16 devices will have different WRITE to WRITE same bank group timings based on: whether the second write requires a read-modify-write (RMW), the Burst Length mode of the device set by MR0:OP[1:0], or whether data masking is enabled by MR5:OP[5]. BL16 partial writes and BC8 writes require a RMW on x8/x16 devices. BL16 non-partial writes do not require RMW.

Table 176: Minimum WRITE to Write Same Bank Group Timings - x8/x16 Devices

From	To			Units	Notes
	BC8	BL16 Partial Write	BL16 not Partial Write		
BC8 or BL16	$t_{\text{CCD\_L\_WR}}$	$t_{\text{CCD\_L\_WR}}$	$t_{\text{CCD\_L\_WR2}}$		

Table 177: Minimum WRITE to Write Command Timings – Different Bank Group

From	To		Notes
	BL16 in BL32 OTF Mode	BL32 to BL32 OTF Mode	
BL16 in BL32 OTF mode	$t_{\text{CCD\_S\_WR}}$	$t_{\text{CCD\_S\_WR}}$	1
BL32 in BL32 OTF mode	$2 \cdot t_{\text{CCD\_S\_WR}}$	$2 \cdot t_{\text{CCD\_S\_WR}}$	1

Note: 1. The device supports an optional fixed BL32 mode and optional OTF mode for x4 devices only.

READ Command Timing Definitions

Read timing shown in this section is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

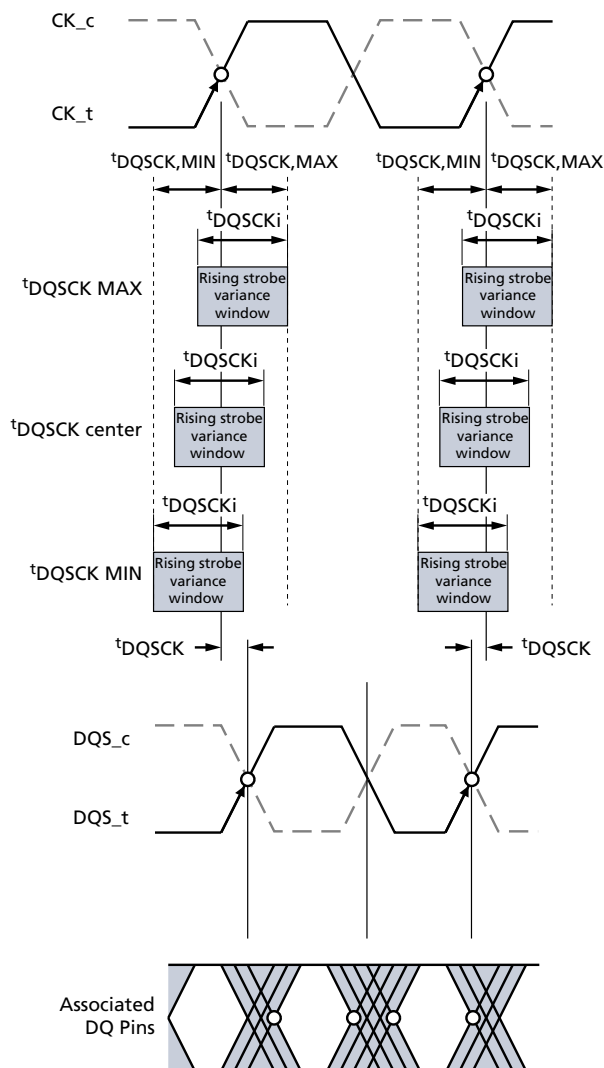
- $t_{DQSCK,MIN}/MAX$ describes the allowed range for a rising data strobe edge relative to CK_t , CK_c
- t_{DQSCK} is the actual position of a rising strobe edge relative to CK_t , CK_c

Falling data strobe edge parameters:

$t_{DQSCK,MIN}$ limit = Earliest of $\{t_{DQSCKi}$ at any valid V_{DD} and temperature, all DQS pairs and parts}.

$t_{DQSCK,MAX}$ limit = Latest of $\{t_{DQSCKi}$ at any valid V_{DD} and temperature all DQS pairs and parts}.

Figure 70: t_{DQSCK} Timing Definition



Temperature Sensor

The device features a temperature sensor whose status (MR4:OP[2:0]) can be read to determine the minimum required refresh rate. The temperature sensor read-out or the device T_{OPER} may be used to determine whether the refresh rate and operating temperature requirements are being met. Additionally, the device's temperature status (MR4:OP[2:0]) can be read by the system to determine the current approximate temperature range sensed by the device.

The device must monitor device temperature and updates MR4 according to t_{TSI} . Upon completion of device initialization, the device temperature status bits must be no older than t_{TSI} . MR4 is updated even when the device is in the self refresh state.

When using the temperature sensor, an actual device case temperature (T_{CASE}) measurement may be higher than the T_{OPER} specification that applies to standard or elevated temperature ranges, as long as the temperature sensor readings remain within range. For example, T_{CASE} may be above 85°C when MR4:OP[2:0]=010b, as long as the sensor readings remain at or below 85°C. The device must allow for a 2°C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly.

When MR4:OP[5]=0 (wide range temperature sensor not supported), the four thresholds of the temperature sensor will be nominally 80°C, 85°C, 90°C and 95°C.

The second threshold (nominally 85°C) should be used by the system to switch to 2X refresh. The fourth threshold (nominally 95°C) should be used to throttle activity/traffic to keep the device at a safe operating temperature. The first threshold (nominally 80°C) enables the system to take actions to avoid reaching the second threshold. The third threshold (nominally 90°C) enables the system to take actions to avoid reaching the fourth threshold.

When MR4:OP[5]=1 (optional wide range extended temperature sensor range supported), the six thresholds of the temperature sensor will be nominally 75°C, 80°C, 85°C, 90°C, 95°C, and 100°C. The third threshold (nominally 85°C) is used by the system to switch to 2X refresh. The fifth threshold (nominally 95°C) is used by the system to throttle activity to keep the device at a safe operating temperature. The sixth threshold (nominally 100°C) is used by the system to perform emergency actions such as forcing the system to power down. Support for temperature sensor readings above 95°C does not imply that the device may operate properly above 95°C. Side effects may include loss of data integrity.

To ensure proper operation using the temperature sensor, consider the following factors:

- TempGradient is the maximum temperature gradient experienced by the device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (t_{TSI}) is the maximum delay between internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and the response by the system.

To determine the required frequency of polling MR4, the system must use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + t_{\text{TSI}} + \text{SysRespDelay}) \leq 2^\circ\text{C}$$

Table 178: Temperature Sensor Parameters

Parameter	Symbol	MIN/MAX	Value	Unit	Notes
System Temperature Gradient	TempGradient	MAX	System-dependent	°C/s	
MR4 Read Interval	ReadInterval	MAX	System-dependent	ms	
Temperature Sensor Interval	t_{TSI}	MAX	32	ms	
System Response Delay	SysRespDelay	MAX	System-dependent	ms	

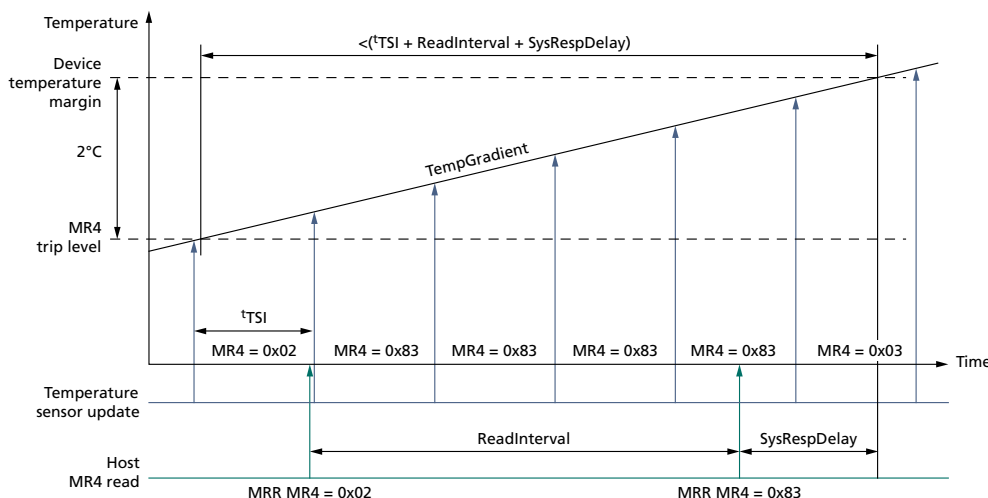
Table 178: Temperature Sensor Parameters (Continued)

Parameter	Symbol	MIN/MAX	Value	Unit	Notes
Device Temperature Margin	TempMargin	MAX	2	°C	1
Temperature Sensor Accuracy, second threshold trip point	TempSensorAcc2	MAX	+/-3	°C	1,2
Temperature Sensor Accuracy, fourth threshold trip point	TempSensorAcc4	MAX	+/-3	°C	1,2
Relative Trip Point, second threshold minus first threshold	RelativeTrip2m1	MIN/MAX	MIN 3 / MAX 7	°C	1,3
Relative Trip Point, third threshold minus second threshold	RelativeTrip3m2	MIN/MAX	MIN 3 / MAX 7	°C	1,4
Relative Trip Point, fourth threshold minus third threshold	RelativeTrip4m3	MIN/MAX	MIN 3 / MAX 7	°C	1,4

- Notes: 1. Verified by design characterization and may not be subject to production test.
2. Only the minimum (negative side) is specified for the second and fourth thresholds. The device vendor is responsible for guaranteeing correct operation of 1X refresh for MR4 ≤ 010b and 2X refresh for MR4 ≤ 100b. (This puts a vendor-specific constraint on the temperature sensor accuracy on the positive side.)
3. The first threshold is defined relative to the second threshold.
4. The third threshold is defined relative to the second and fourth thresholds.

For the table above, if TempGradient is 10°C/s and the SysRespDelay is 1ms: $(10^{\circ}\text{C/s}) \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^{\circ}\text{C/s}$. In this case, ReadInterval must not be greater than 68ms.

Figure 71: Temperature Sensor Timing Diagram



Note: 1. MR4 encodings are examples only and assume MR4:OP[4]=0.

Temperature Sensor Usage for 3D Stacked Devices

In the case of 3D stacked (3DS) devices, the refresh rate (MR4) is related to the hottest die in the stack.

Temperature Encoding

The device provides temperature related information to the controller via an encoding on MR4:OP[2:0]. The encodings define the proper refresh rate expected to maintain data integrity.

REFRESH Operation

The REFRESH command (REF) is used during normal device operation. Since “data” is stored as 0s and 1s in capacitors in a device, and the capacitors leak charge over time, the REFRESH command is issued periodically to restore (refresh) the electrical charge in the capacitors. Each REFRESH command results in one or more ACTIVATE operations to a selected row or rows, followed by a self-timed precharge to close the rows opened during the ACTIVATE operation.

The REFRESH command is non-persistent; therefore, it must be issued each time a refresh is required. The device requires REFRESH commands to be issued at an average periodic interval of t_{REFI} .

Three types of REFRESH operations are supported:

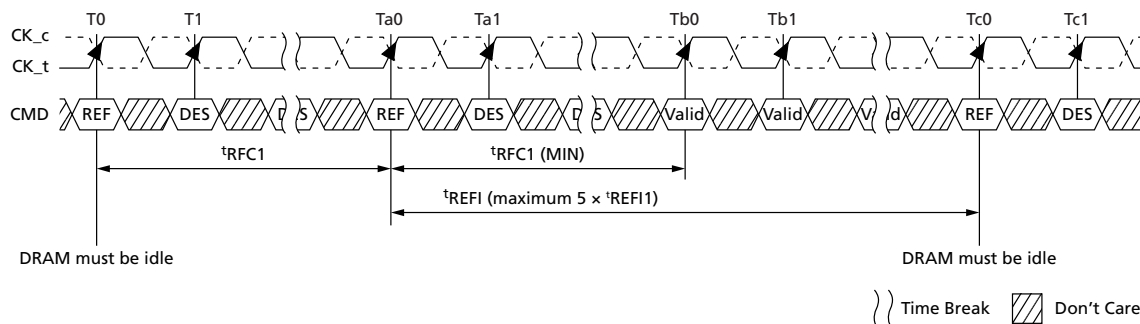
- Normal refresh: Issue the ALL BANK REFRESH (REFab) command in normal refresh mode.
- Fine granularity refresh: Issue the ALL BANK REFRESH (REFab) command in fine granularity refresh mode.
- Same bank refresh: Issue the SAME BANK REFRESH (REFsb) command in fine granularity refresh mode.

This section describes the details of the REFRESH operations, the requirements for each, and the transitions between each type.

For normal REFRESH and fine granularity REFRESH operations, all device banks must be precharged and idle for a minimum of the precharge time (t_{RP} (MIN)) before the ALL BANK REFRESH (REFab) command can be applied.

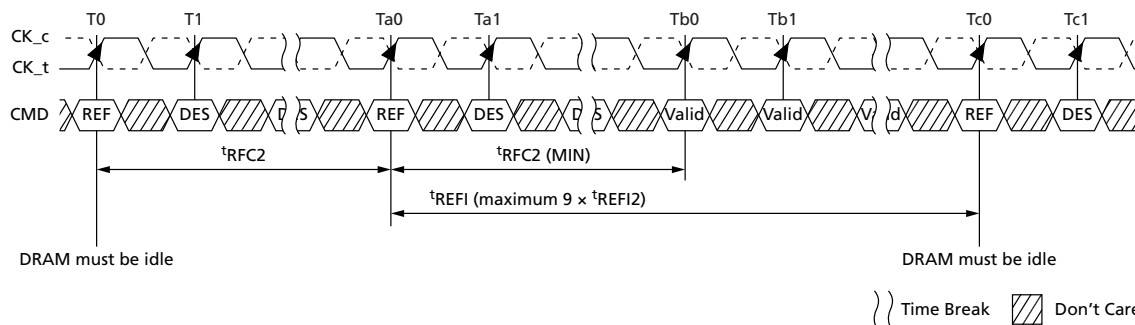
The refresh addressing is generated by the internal refresh controller during the refresh cycle. The external command/address bus (CA[13:0]) is only required to be in a valid state once this cycle has started. When the refresh cycle completes, all device banks will be in the precharged (idle) state. A delay between an issued REFRESH command and the next valid command, except DES, PDE, NOP (PDX) and non-target ODT commands, must be greater than or equal to the minimum refresh cycle time (t_{RFC} (MIN)), as shown in the following figures. Note that the t_{RFC} timing parameter depends on memory density and the refresh mode setting, which can be set to normal refresh mode or fine granularity refresh mode.

Figure 72: REFRESH Command Timing (Normal Refresh Mode Example)



- Notes:
1. Only DES, PDE, NOP (PDX) or non-target ODT commands are allowed after the REF command is issued until t_{RFC1} (MIN) expires.
 2. Time interval between two REF commands may be extended to a maximum of $5 \times t_{REFI1}$.

Figure 73: REFRESH Command Timing (Fine Granularity Refresh Mode Example)



- Notes: 1. Only DES, PDE, NOP (PDX) or non-target ODT commands are allowed after the REF command is issued until t_{RFC2} (MIN) expires.
2. Time interval between two REF commands may be extended to a maximum of $9 \times t_{REFI2}$.

Refresh Modes

The device has two different refresh modes with two different refresh cycle time (t_{RFC}) settings:

- Normal refresh mode
- Fine granularity refresh (FGR) mode

FGR mode provides a shorter refresh cycle time (t_{RFC2}) but also requires ALL BANK REFRESH (REFab) commands to be provided twice as often (t_{REFI} is divided by two; that is, $t_{REFI2} = t_{REFI1}/2$). The refresh mode setting is programmed by the MRW command as shown in the following table. The refresh modes are fixed until changed by MRW command to MR4:OP[4]. On-the-fly refresh mode change is not supported.

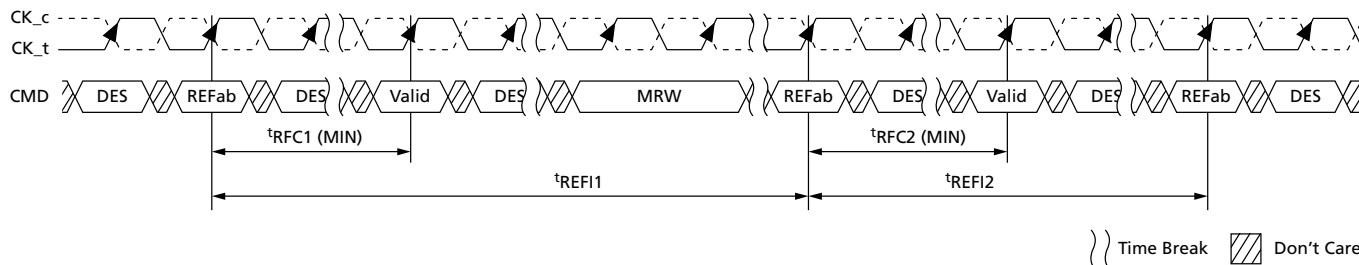
Table 179: Refresh Mode MR Definition

MR4 OP[4]	Refresh Mode (t_{RFC} Setting)
0	Normal refresh mode (t_{RFC1})
1	Fine granularity refresh mode (t_{RFC2})

Changing Refresh Mode

When the refresh mode is changed by MRW, the new t_{REFI} and t_{RFC} parameters are applied from the moment of the rate change. As shown in the following figure, when an ALL BANK REFRESH command is issued in normal refresh mode, t_{RFC1} and t_{REFI1} are applied from the time the command (REFab) was issued. And, when an ALL BANK REFRESH command is issued in FGR mode, t_{RFC2} and t_{REFI2} are satisfied.

Figure 74: Refresh Mode Change Command Timing



Note: 1. Before MRW, the device is in normal refresh mode; after MRW, the device is in FGR mode.

The following conditions must be satisfied before the refresh mode can be changed; otherwise, data retention cannot be guaranteed.

- In normal refresh mode, the REFab command must complete and t_{RFC1} must be satisfied before issuing the MRW command to change the refresh mode.
- If performing REFab commands, it is recommended that an even number of REFab commands be issued to the device since the last change of the refresh mode with an MRW command before the refresh mode is changed again by another MRW command, since a REFab command will reset the internal bank counter. If this condition is met, no additional REFRESH commands are required upon the refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the device upon refresh mode change. This extra REFab command is not counted toward the computation of the average refresh interval (t_{REFI}). See the Refresh Mode Change from FGR 2x to Normal 1x Command Timing image below.
- If performing REFsb commands, it is recommended that all banks have received an even number of REFsb commands since the last change of the refresh mode with an MRW command before the refresh mode is changed again by another MRW command since a REFab command will reset the internal bank counter. If this condition is met, no additional REFRESH commands are required upon the refresh mode change. If this condition is not met, one extra REFab command is required to be issued to the device upon refresh mode change. This extra REFab command is not counted toward the computation of the average refresh interval (t_{REFI}). See the 16Gb and Higher Density DRAM Refresh Mode Change from FGR 2x REFsb to Normal 1x Command figure.

Figure 75: Refresh Mode Change from FGR 2x to Normal 1x Command Timing

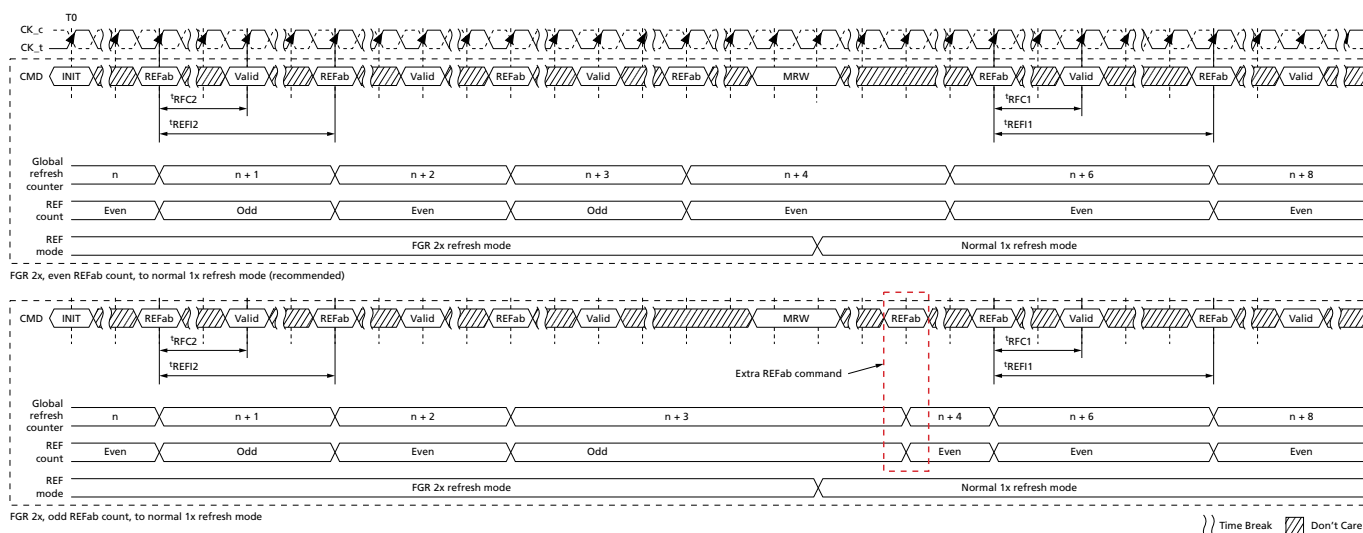
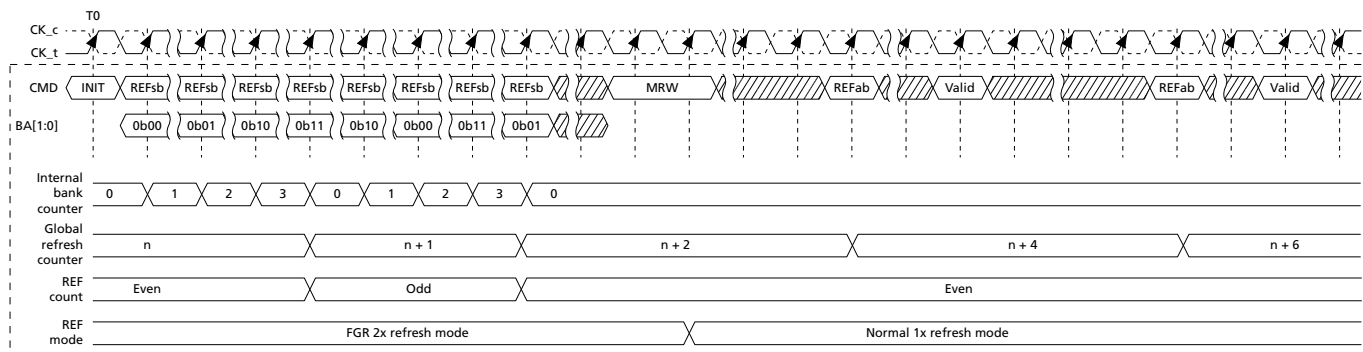
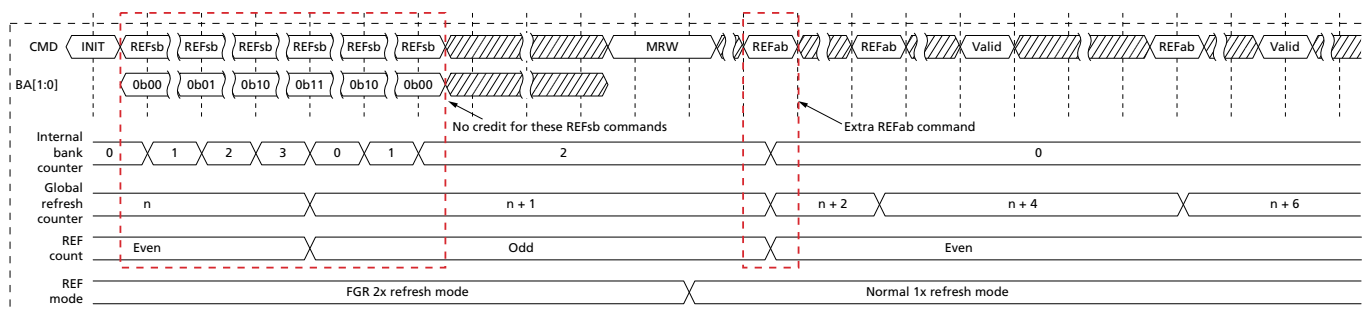


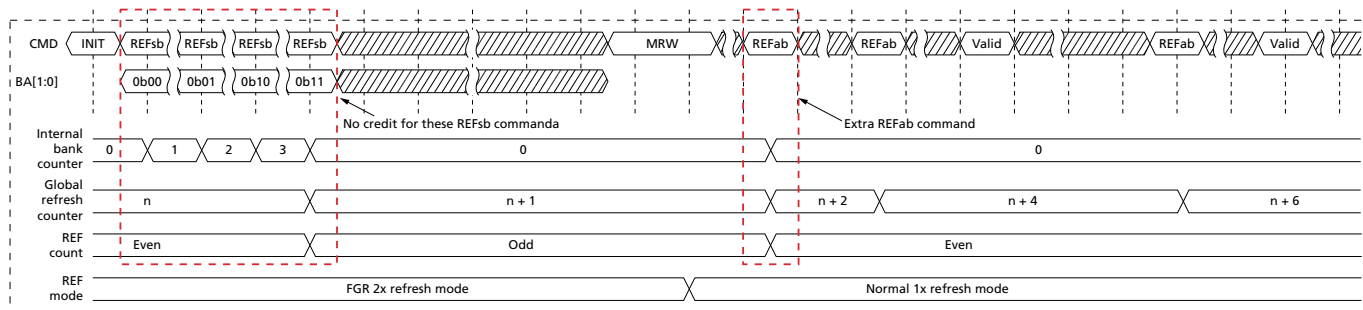
Figure 76: 16Gb and Higher Density DRAM Refresh Mode Change from FGR 2x REFsb to Normal 1x Command Timing



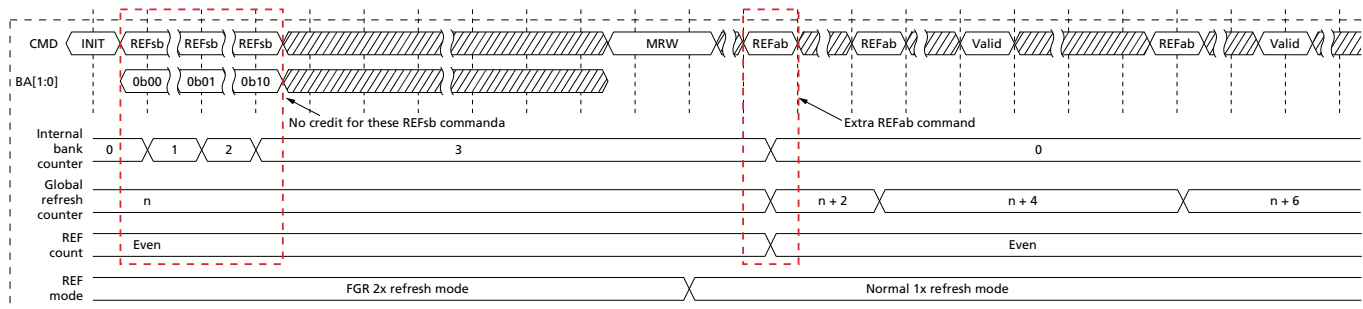
FGR 2x, all banks received REFsb and even REF count, to normal 1x refresh mode (recommended)



FGR 2x, not all banks received REFsb during odd REF count, to normal 1x refresh mode



FGR 2x, all banks received REFsb but odd REF count, to normal 1x refresh mode



FGR 2x, not all banks received REFsb but even REF count, to normal 1x refresh mode

}} Time Break ▨ Don't Care

SAME BANK REFRESH Command

The first SAME BANK REFRESH command (REFsb) applies the refresh process to a specific bank in each bank group (unlike the ALL BANK REFRESH command [REFab], which applies the refresh process to all banks in every bank group). The determination whether a SAME BANK REFRESH or an ALL BANK REFRESH is executed depends on whether a REFsb or REFab command is issued, as shown in the Command Truth Table. The REFsb command is allowed in FGR mode MR4:OP[4]=1b only.

Each REFsb command to each bank increments an internal bank counter, and once the bank counter equals the number of available banks in a bank group, it resets and starts over on the next subsequent REFsb.

Each time the internal bank counter resets and starts over on the next subsequent REFsb, the global refresh counter also increments. An REFsb command can be issued to any bank and in any bank order. A subsequent REFsb command issued to the same bank prior to every bank receiving an REFsb command will repeat refreshing the same row, since the device's global refresh counter does not increment until all banks in a bank group receive an REFsb command.

The first REFsb command issued is the *synchronization* REFsb command, and the synchronization count resets the internal bank counter to zero when either (a) every bank has received one REFsb command, (b) RESET is applied, (c) self refresh mode is entered or exited, or (d) REFab is issued. The global refresh counter increments when either an REFab is issued or when all banks have received their one REFsb command and the synchronization count resets to zero. If an REFab command is issued when the bank counter is not zero (that is, in the middle of same bank refreshing), the global refresh counter does not increment until the completion of REFab, effectively losing the credits for any REFsb commands issued prior to the REFab.

Table 180: 16Gb and Higher Density Bank and Refresh Counter Increment Behavior

Count #	Command	BA1	BA0	Refresh Bank #	Internal Bank #	Global Refresh Counter # (Row Address #)
0	RESET, REFab, SRE or SELF REFRESH EXIT (3 x NOP) commands, and in FGR mode (MR4:OP[4]=1)				To 0	-
1	REFsb	0	0	0	0 to 1	<i>n</i>
2	REFsb	0	1	1	1 to 2	
3	REFsb	1	0	2	2 to 3	
4	REFsb	1	1	3	3 to 0	
5	REFsb	1	0	2	0 to 1	<i>n</i> +1
6	REFsb	0	0	0	1 to 2	
7	REFsb	1	1	3	2 to 3	
8	REFsb	0	1	1	3 to 0	
9	REFsb	0	0	0	0 to 1	<i>n</i> +2
10	REFsb	0	1	1	1 to 2	
11	REFab	V	V	0-3	To 0	
12	REFsb	1	1	3	0 to 1	
13	REFsb	0	1	1	1 to 2	<i>n</i> +3
14	REFsb	0	0	0	2 to 3	
15	REFsb	1	0	2	3 to 0	
16	REFab	V	V	0-3	To 0	
17	REFab	V	V	0-3	To 0	<i>n</i> +5

Table 180: 16Gb and Higher Density Bank and Refresh Counter Increment Behavior (Continued)

Count #	Command	BA1	BA0	Refresh Bank #	Internal Bank #	Global Refresh Counter # (Row Address #)
18	REFab	V	V	0-3	To 0	$n+6$
19	REFsb	0	0	0	0 to 1	$n+7$
20	REFab	V	V	0-3	To 0	
21	REFsb	1	0	2	0 to 1	$n+8$
22	REFsb	0	1	1	1 to 2	
23	REFsb	0	0	0	2 to 3	
24	REFsb	1	1	3	3 to 0	

The REFsb command must not be issued to the device until the following conditions are met:

- t_{RFC1} or t_{RFC2} has been satisfied after the prior 1x or 2x REF command, respectively
- t_{RFCsb} has been satisfied after the prior REFsb command
- t_{RP} has been satisfied after the prior PRECHARGE command to that bank
- t_{RRD_L} has been satisfied after the prior ACTIVATE command (for example, t_{RRD_L} has to be met from ACTIVATE of a different bank in the same bank group to the REFsb targeted at the same bank group)

Additional restrictions for issuing the REFsb/REFab and RFMSb/RFMab commands:

- For mono devices, REFsb and RFMSb count as ACTIVATE commands for the four activate window timing restrictions t_{FAW}
- For 3DS devices, REFsb and RFMSb count as ACTIVATE commands for the four activate timing restriction to the same logical rank (t_{FAW_slr})
- For 3DS devices, REFsb, REFab, RFMSb and RFMab count as ACTIVATE commands for the four activate timing restriction to different logical ranks (t_{FAW_dlr})

After an REFsb is issued, the target banks (one in each bank group) are inaccessible during the same-bank refresh cycle time (t_{RFCsb}); however, the other banks in each bank group are accessible and can be addressed during this same-bank refresh cycle. When the same-bank refresh cycle completes, the banks refreshed via the REFsb will be in idle state.

After issuing an REFsb command, the following conditions must be met:

- t_{RFCsb} must be satisfied before issuing an REF command
- t_{RFCsb} must be satisfied before issuing an ACTIVATE command to the same bank
- $t_{REFSBRD}$ must be satisfied before issuing an ACTIVATE command to a different bank

Table 181: REFRESH Commands Scheduling Separation Requirements

Symbol	Min Delay From	To	Note
t_{RFC1}	REFab	REFab	1
		ACTIVATE command to any bank	
t_{RFC2}	REFab	REFab	2
		ACTIVATE command to any bank	
		REFsb	

Table 181: REFRESH Commands Scheduling Separation Requirements (Continued)

Symbol	Min Delay From	To	Note
t_{RFCsb}	REFsb	REFab	2
		ACTIVATE command to same bank as REFsb	
		REFsb	
$t_{REFSBRD}$	REFsb	ACTIVATE command to different bank from REFsb	2
t_{RRD_L}	ACTIVATE	REFsb to different bank from ACTIVATE	2
$t_{RRD\_L\_slr}$		REFsb to different bank in same logical rank in 3DS	
$t_{RRD\_L\_dlr}$		REFab/sb to different logical rank in 3DS	

Notes: 1. MR4:OP[4] set to normal refresh mode.

2. MR4:OP[4] set to FGR mode. REFsb command is valid in FGR mode only.

t_{REFI} and t_{RFC} Parameters

The maximum average refresh interval (t_{REFI}) requirement depends on the refresh mode setting (normal or FGR) and the device's case temperature (T_{case}).

When the refresh mode is set to normal refresh, REFab commands are issued (t_{RFC1}) and $T_{case} \leq 85^{\circ}\text{C}$ (the maximum average refresh interval [t_{REFI1}]), is t_{REFI} . When the refresh mode is set to FGR mode, REFab commands are issued (t_{RFC2}) and $T_{case} \leq 85^{\circ}\text{C}$ (the maximum average refresh interval [t_{REFI2}]), is $t_{REFI}/2$. This same $t_{REFI}/2$ interval value is also appropriate if the refresh mode is set to normal refresh mode and REFab commands are issued (t_{RFC1}) but $85^{\circ}\text{C} < T_{case} \leq 95^{\circ}\text{C}$. Finally, if the refresh mode is set to FGR mode, REFab commands are issued (t_{RFC2}) and $85^{\circ}\text{C} < T_{case} \leq 95^{\circ}\text{C}$ (the maximum average refresh interval [t_{REFI2}]) is $t_{REFI}/4$.

The device includes an optional method for the host to indicate when REFRESH commands are being issued at the 2X (t_{REFI2}) refresh interval rate. The 2X refresh interval rate indicator (MR4:OP[3]) alerts the device if the host supports the refresh interval rate indication as part of the REF command using CA8. If enabled (MR4:OP[3]=1), the host issues 1X REF commands with CA8=H ($T_{case} \leq 85^{\circ}\text{C}$), and the host issues 2X REF commands with CA8=L (T_{case} any allowable temperature). MR4:OP[3] is a status read/write (SR/W) MR bit that shows DDR5 support of this optional feature. Reading MR4:OP[3] returns a 1 if the 2X refresh interval rate indicator is supported. A 0 is returned if not supported.

When issuing SAME BANK REFRESH (REFsb) commands, the maximum average refresh interval is further divided down by the number of banks in a bank group, represented by "n" (e.g., 16GB: n=4). Where a REFab command maximum average refresh interval in FGR (t_{REFI2}) is either $t_{REFI}/2$ or $t_{REFI}/4$ depending on the case temperature range, the REFsb command maximum average refresh interval is either $t_{REFI}/(2*n)$ or $t_{REFI}/(4*n)$, respectively.

t_{REFI} is based on the 8192 REFRESH commands that need to be issued within the baseline $t_{REF} = 32\text{ms}$ refresh period on the device. t_{REFI} parameters are shown in the table below.

t_{REFI} and t_{RFC} Parameters for 3DS Devices

Typical platforms are designed with the assumption that no more than one physical rank is refreshed simultaneously. To limit the maximum refresh current (I_{DD5B1}) for a 3DS stacked device, it is required to stagger the REFRESH commands to each logical rank within a 3DS stack.

The t_{RFC} time for a single logical rank is defined as t_{RFC_slr} and is specified as the same value as for a monolithic device of equivalent density. The minimum amount of stagger between REFRESH commands sent to different logical ranks (t_{RFC_dlr}) or physical ranks (t_{RFC_dpr}) is specified to be approximately $t_{RFC\_slr}/3$, as shown in the [3DS \$t_{RFC}\$ Parameters by Logical and Physical Rank Density](#) table.

Table 182: t_{REFI} Parameters for REFab and REFsb Commands by Device Density (Including 3DS)

Command	Refresh Mode	Parameter	Temperature	Expression	Value	Unit	Note
REFab	Normal	t_{REFI1}	$0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	t_{REFI}	3.9	μs	1,2,3
			$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	$t_{REFI}/2$	1.95		
REFab	Fine Granularity	t_{REFI2}	$0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	$t_{REFI}/2$	1.95		
			$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	$t_{REFI}/4$	0.975		
REFsb	Fine Granularity	t_{REFIsb}	$0^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85^{\circ}\text{C}$	$t_{REFI}/(2*n)$	$1.95/n$		
			$85^{\circ}\text{C} < T_{\text{CASE}} \leq 95^{\circ}\text{C}$	$t_{REFI}/(4*n)$	$0.975/n$		

- Notes: 1. All 3D-stacked (3DS) devices follow the same requirements as the monolithic die, regardless of logical rank.
2. 3DS specification covers up to 16Gb density. Larger densities such as 24Gb or 32Gb may have different t_{REFI} requirements
3. n is the number of banks in a bank group (for example, 8Gb: $n=2$; 16Gb: $n=4$)

Table 183: Refresh Granularity t_{RFC1} and t_{RFC2} Parameters by Device Density

REFRESH Operation	Parameter	8Gb	16Gb	24Gb	32Gb	Units
Normal	$t_{RFC1,min}$	195	295	410	410	ns
Fine (FGR mode)	$t_{RFC2,min}$	130	160	220	220	ns
Same Bank (REFsb)	$t_{RFCsb,min}$	115	130	190	190	ns

Table 184: 3DS and DDP t_{RFC} Parameters by Logical and Physical Rank Density

REFRESH Operation	Parameter	8Gb	16Gb	24Gb	32Gb	Units	Notes
Normal refresh with 3DS same logical rank	^t RFC1_slr,min	^t RFC1,min				ns	1
Fine granularity refresh (FGR) mode with 3DS same logical rank	^t RFC2_slr,min	^t RFC2,min					1
Same Bank (REFsb) with 3DS same logical rank	^t RFCsb_slr,min	^t RFCsb,min					1
Normal with 3DS different logical rank	^t RFC1_dlr,min	^t RFC1,min/3					3,6
Normal refresh with 3DS or DDP different physical rank	^t RFC1_dpr,min	^t RFC1,min/3					2,3,6
FGR mode with 3DS different logical rank	^t RFC2_dlr,min	^t RFC2,min/3					3,4
FGR mode with 3DS or DDP different physical rank	^t RFC2_dpr,min	^t RFC2,min/3					2,3,4
Same Bank (REFsb) with 3DS different logical rank	^t RFCsb_dlr,min	^t RFCsb,min/3					3,5

- Notes: 1. All 3D-stacked (3DS) devices follow the same requirements as the monolithic die for same logical ranks.
2. Parameter applies to all DDP or dual-physical rank (36 and 40 placement) 3DS-based DIMMs built with JESD301-1 PMIC50x0 Specification, but may not apply to DIMMs built with higher current capacity PMICs.
3. 3DS and DDP t_{RFC} parameters are to be rounded up to the nearest 1ns after the $t_{RFC}*(min)/3$ calculation.
4. Parameter applies from REFab to REFab, and from REFab to REFsb.
5. Parameter applies from REFsb to REFsb, and from REFsb to REFab.
6. Parameter applies from REFab to REFab.

Table 185: Same Bank Refresh Parameters

Refresh Mode	Parameter	8Gb	16Gb	24Gb	32Gb	Units
Same Bank Refresh to ACT delay	$t_{\text{REFSBRD,min}}$	30	30	30	30	ns

Table 186: Refresh Parameters for 3DS 2H, 4H

Refresh Mode	Parameter	8Gb	16Gb	24Gb	32Gb	Units
Same Bank Refresh to ACT delay, SLR	$t_{\text{REFSBRD\_slr,min}}$	30	30	30	30	ns
Same Bank Refresh to ACT delay, DLR	$t_{\text{REFSBRD\_dlr,min}}$	15	15	15	15	
All Bank Refresh to ACT delay DLR	$t_{\text{REFABRD\_dlr,min}}$	15	15	15	15	

Refresh Operation Scheduling Flexibility

In general, a REFab command (or equivalent number of REFsb commands) needs to be issued to the device regularly every t_{REFI} interval. To enable improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

In normal refresh mode, a maximum of four REFab commands can be postponed, meaning that at no point in time more than a total of four REFRESH commands are allowed to be postponed. In a case where four REFab commands are postponed in a row, the resulting maximum interval between the surrounding REFab commands is limited to $5 \times t_{\text{REFI1}}$ (see the Postponing REFRESH Commands Example of Normal Refresh Mode figure below). At any given time, a maximum of five REFab commands can be issued within the $1 \times t_{\text{REFI1}}$ window.

Self-refresh mode may be entered with a maximum of four REFab commands being postponed. After exiting self-refresh mode with one or more REFab commands postponed, additional REFab commands may be postponed to the extent that the total number of postponed REFab commands (before and after the self-refresh) will never exceed four. During self-refresh mode, the number of postponed REFab commands does not change. An additional REFab command is required after self-refresh exit (refer to the Self Refresh Operation section for more information).

In fine granularity refresh (FGR) mode, the maximum REFab commands that may be postponed is eight, with the resulting maximum interval between the surrounding REFab commands limited to $9 \times t_{\text{REFI2}}$ (see the Postponing Refresh Commands Example of Fine Granularity Refresh figure below). At any given time, a maximum of nine REFab commands can be issued within $1 \times t_{\text{REFI2}}$ window. The same maximum count of eight applies to postponed REFab commands around self refresh entry and exit. An additional REFab command is required after self-refresh exit (refer to the Self Refresh Operation section for more information). Where n is the number of banks in a bank group, a single REFab command can be replaced with n REFsb commands for the purpose of scheduling postponed REFRESH commands.

Figure 77: Postponing REFRESH Commands Example of Normal Refresh Mode t_{REFI1} , t_{RFC1}

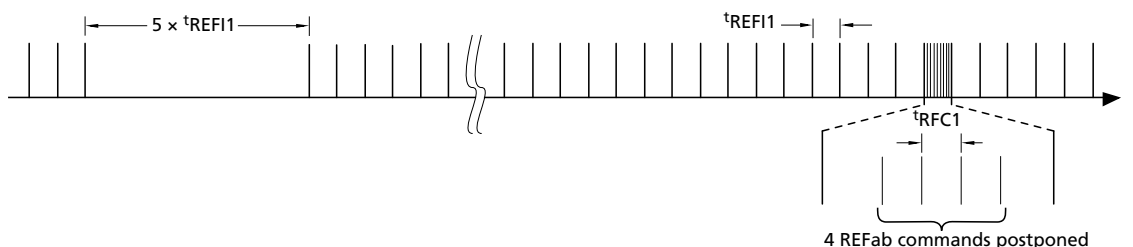
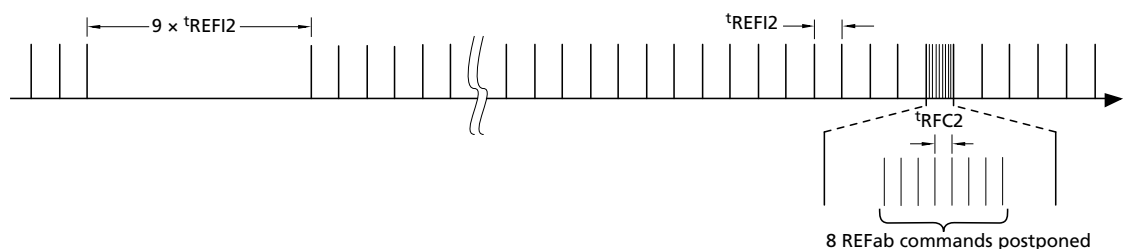


Figure 78: Postponing REFRESH Commands Example of Fine Granularity Refresh Mode t_{REFI2} , t_{RFC2}



Module Rank and Channel Limitations for DDR5 DIMMs

To achieve efficient module power supply design for JEDEC-standard DDR5 DIMMs, minimum timings as well as limitations in the number of DRAMs are provided for refresh occurring on a single module. Additionally, since these modules are organized as two independent 36-bit or 40-bit channels (32 bits for non-ECC DIMMs), additional restrictions apply to limit localized power delivery noise on the module.

To provide best performance, the different channels may initiate commands on the same cycle provided the rank-to-rank timings are met, the maximum number of DRAMs in a given activity is not exceeded, and the applicable component timings shown elsewhere in this specification are met. The timing and operational relationships for DDR5 DIMMs are shown below.

Table 187: Module Rank and Channel Timings During REFRESH Operation

DIMM Configuration	Maximum Number of Die in Simultaneous or Overlapping Activity	
	REFRESH (All-bank REFRESH)	
	Die per Physical Rank	Die per DIMM
SR x16	No restriction	
DR x16	No restriction	
SR x8	No restriction	
DR x8	No restriction	
SR x4	No restriction	
DR x4	No restriction	
DR x4 (2H 3DS)	No restriction	40
QR x4 (DDP)	No restriction	40
DR x4 (4H 3DS)	30	40
DR x4 (8H 3DS)	30	40

- Notes:
- Any combination of commands, with up to the maximum of die per channel and per DIMM, per condition is allowed.
 - REFRESH commands to different channels do not require stagger.
 - t_{RFC_dlr} must be met for REFRESH commands to different logical ranks within a package rank on the same channel.
 - Any device is considered to be in refresh mode until t_{RFC} time has been met.
 - Each rank consists of one group of DRAMs making up a 36- or 40-bit channel (32 bits for non-ECC DIMMs).
 - These restrictions only apply to explicit all-banks REFRESH commands (REFab) and not to SELF REFRESH ENTRY or EXIT.
 - Restrictions apply to DIMMs built with JESD301-1 PMIC50x0 Specification or JESD301-2 PMIC5100 Specification, but may not apply to DIMMs built with higher current capacity PMICs.

Self Refresh Entry and Exit

The device can enter self refresh mode anytime in normal refresh and FGR mode without any restriction on the number of REFRESH commands that have been issued during the mode before entering self refresh. However, upon exiting self refresh, one additional refresh must be issued in addition to the normally scheduled REFRESH commands (refer to the Self Refresh Operation section for more information). Plus, extra REFRESH command(s), in addition the aforementioned additional refresh, may also be required depending on the condition of the self refresh entry. The conditions and requirements for the extra REFRESH command(s) are defined as follows:

- The normal refresh mode has no special restrictions.
- If performing REFab commands in FGR mode, it is recommended there be an even number of REFab commands before entry into self refresh since the last self refresh exit or MRW command that set the FGR mode. If this condition is met, no additional REFRESH commands are required upon self refresh exit. If this condition is not met, one extra REFab command is required to be issued upon self refresh exit. This extra REFRESH command is not counted toward the computation of the average refresh interval (t_{REFI2}). This extra Refresh counts toward the maximum number of refreshes which may be postponed. Refer to the Self Refresh Operation section for more information. See the FGR 2X SREF Command Timing figure below.
- If performing REFsb commands, it is recommended that all banks have received a REFsb command prior to entering self refresh, since entering and exiting self refresh resets the internal bank counter. If this condition is met, no additional REFRESH commands are required upon self refresh exit, and REFsb commands again can be issued to any bank in any bank order. If this condition is not met, one extra REFab command or an extra REFsb command to each bank is required to be issued upon self refresh exit. These extra REFRESH commands are not counted toward the computation of the average refresh interval, t_{REFI2} (see the 16Gb and Higher Density Devices with Four Banks per Bank Group example t_{REFI2} figure below). These extra REFRESH commands count toward the maximum number of refreshes which may be postponed. Refer to the Self Refresh Operation section for more information.

Figure 79: FGR 2X to SREF Command Timing

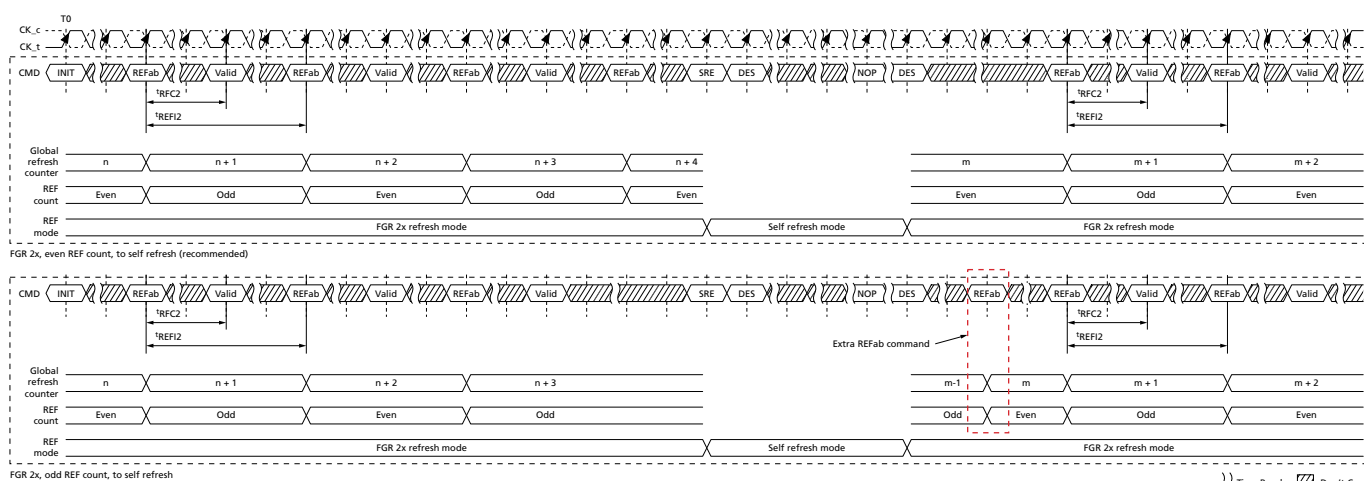
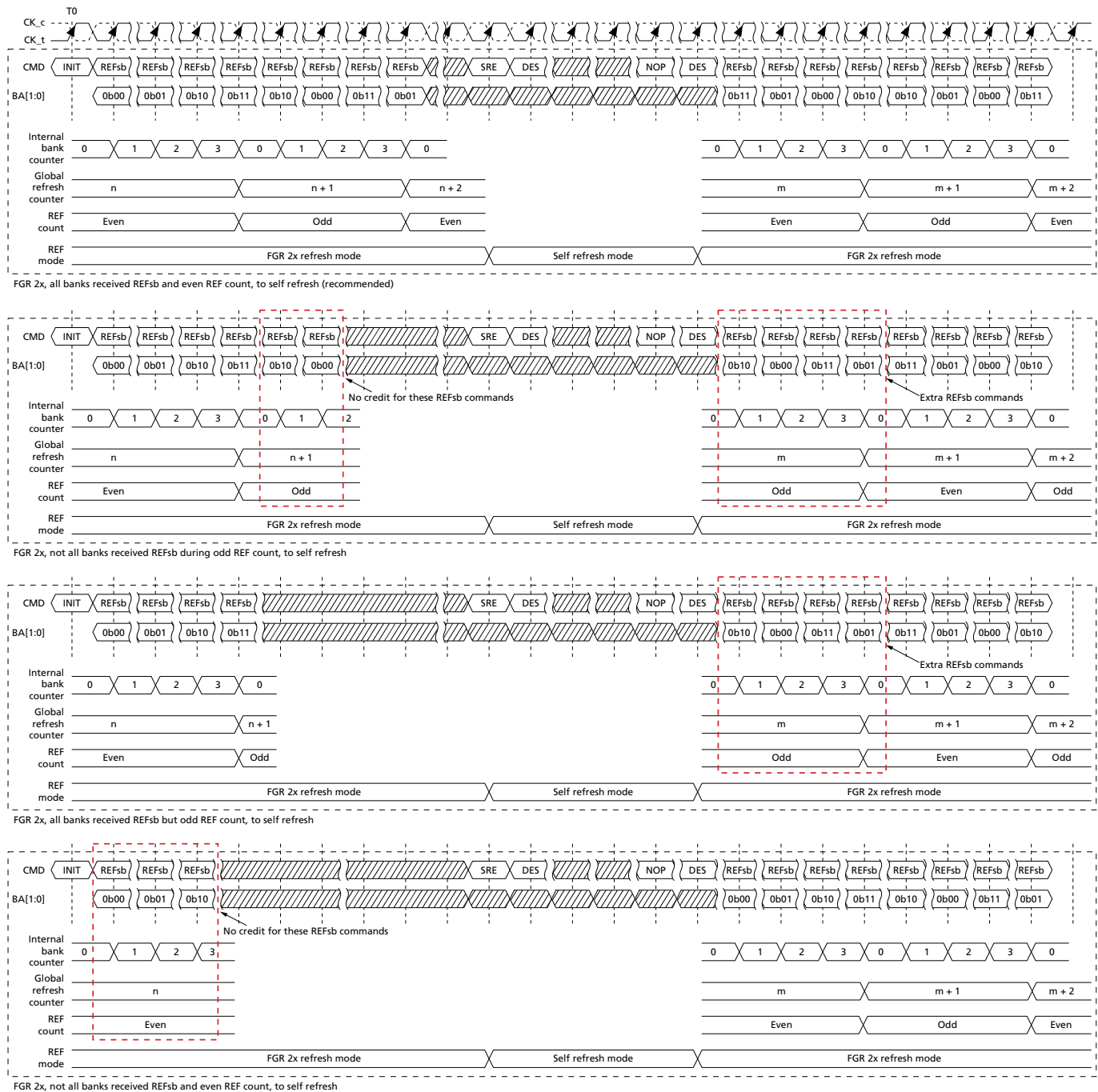


Figure 80: 16Gb and Higher Density FGR 2x REFsb to SREF Command Timing



Self Refresh Operation

Self refresh mode retains data in the device, even if the rest of the system is powered down. When in self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate self refresh operation.

While in self refresh mode, the device adjusts and updates its internal average periodic refresh interval as needed, based on its own temperature sensor. The internal average periodic refresh interval adjustment (increasing, decreasing or staying constant) does not require any external control.

SELF REFRESH ENTRY (SRE) is command-based, while the SELF REFRESH EXIT command is defined by the transition of CS_n LOW to HIGH with a defined pulse width ^tCSH_SRexit, followed by three or more NOP commands (^tCSL_SRexit) to ensure device stability in recognizing exit, as described in detail below. SELF REFRESH EXIT is sometimes referred to as SRX (3 x NOPs).

Before issuing the SRE command, the device must be in an idle state defined as all banks closed (^tRP, etc. satisfied), no data bursts in progress, and all timings from previous operations satisfied (^tMRD, ^tRFC, etc.). A DES command must be registered on the last positive clock edge before issuing the SELF REFRESH ENTRY command. Once the SELF REFRESH ENTRY command is registered, DES commands must also be registered at the next positive clock edge until ^tCPDED is satisfied. After ^tCPDED is satisfied, CS_n must transition LOW. After CS_n transitions LOW at the end of ^tCPDED, CS_n remains LOW until exit. The device may switch to a CMOS-based receiver to save more power, and that transition should coincide with CS_n going LOW.

When CS_n is held LOW, the device automatically disables ODT termination and sets High-Z as the termination state, regardless of R_{TT} configuration for the duration of self refresh mode. Upon exiting self refresh, the device automatically enables ODT termination and sets RTT_PARK (for DQs) asynchronously during ^tXS_DLL when RTT_PARK is enabled. CA/CS/CK ODT reverts to its strapped or MR ODT setting state if previously applied. During normal operation (DLL on), the DLL is automatically disabled upon entering self refresh and is automatically enabled (including a DLL Reset) upon exiting self refresh.

When the device enters self refresh mode, all of the external control signals except CS_n and RESET_n are don't care. For proper self refresh operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS} and V_{PP}) must be at valid levels. The internal V_{REFDQ} and/or V_{REFCA} generator circuitry may remain on or turned off depending on device design. If internal V_{REFDQ} and/or V_{REFCA} circuitry is turned off in self refresh, when the device exits from the self refresh state, it ensures that V_{REFDQ} and/or V_{REFCA} and generator circuitry is powered up and stable within ^tXS period. The first WRITE operation or the first write-leveling activity may not occur earlier than ^tXS_DLL (or ^tXS if the first command does not require a locked DLL) after exit from self refresh mode. The device initiates a minimum of one REFRESH command internally once it enters self refresh mode.

The clock must be valid until ^tCKLCS; however, it is not required after ^tCKLCS expires (but it should be noted that shortly after ^tCPDED, the termination for the clock will be switched off). The clock is internally disabled (inside the device) during the SELF REFRESH operation to save power. The minimum time that the device must remain in self refresh mode is ^tCSL. You may change the external clock frequency or halt the external clock ^tCKLCS after SRE is registered; however, the clock must be restarted and stable ^tCKSRX before the device can exit SELF REFRESH operation.

The procedure for exiting self refresh requires a sequence of events. Because the device switches to a CMOS-based driver to save power, the device triggers self refresh exit upon seeing the CS_n transition from LOW to HIGH, and stays HIGH for ^tCSH_SRexit. From the time ^tCASRX prior to CS_n transitioning HIGH, the CA bus must be driven HIGH. Once ^tCSH_SRexit is satisfied, three NOP commands must be issued; otherwise, the device could be put into an unknown state. The clocks must be valid for ^tCKSRX prior to issuing the NOP command that completes the self refresh exit sequence. Once a self refresh exit is registered, the following timing delays must be satisfied for the subsequent command, depending on if the command requires a locked DLL or not:

Commands that do not require locked DLL:

t^{XS} - ACT, MPC, MRW, PDE, PDX (NOP), PRE(ab,sb,pb), REF(ab,sb), RFM(ab,sb), SRE, SRX (NOP+NOP+NOP), VREFCA, VREFCS

Commands that require locked DLL:

$\text{t}^{\text{XS\_DLL}}$ - MRR, MRR-NT, RD, RD-NT, WR, WR-NT, WRP

Some host system requirements and restrictions use the optional SRX/ NOP Clock-Sync feature. The Clock-Sync feature is intended to address issue in a system where the host clock has duty cycle distortion that is different from cycle to cycle in even/odd clock in a repeating manner, where clock misalignment between the host clock and DRAM internal 4-phase clock can result in worse performance than initially trained.

If the host clock can guarantee the consistent duty cycle on every even/ odd clock as far as meeting CK input spec, the Clock-Sync feature is not needed. If the host clock has the consistent duty cycle on every even/odd clock, but changes direction (that is, from 46% to 54%) after SRX, the Clock-Sync feature won't be able to address such issue.

This Clock-Sync feature can be used only with host system tracking clock from the first SRX Clock-Sync prior to DCA training and guarantees to issue subsequent SRX with the exact same phase. Host system applications (including RCD, Clock Driver) that cannot guarantee the consistent system clock phase between the first SRX Clock-Sync prior to DCA training and subsequent SRX at the first NOP (for example, like a system where system clock is stopped to put host system in low power mode or to do frequency change and put DRAM into self-refresh) cannot use the Clock Sync feature and therefore should not enable this feature.

The SRX/NOP Clock-Sync scheme helps the DRAMs that have 4-phase internal clock to determine whether ICLK or IBCLK will be the first one that is synchronized with the host clock after SELF-REFRESH EXIT (SRX). It also helps host to identify the right DCA MR setting that was pre-trained during the initialization process to the clock edge. The DRAM is responsible to align the first NOP after SRX ($\text{t}^{\text{c}}+1$ in [Write Timing Parameters](#) and [tDQSS: DRAM External CLK-to-DQS Variation](#)) to the internal clock edge that existed during the DCA training. For instance, on the DRAM that aligns the first NOP with internal odd clock, while in SREF, the DRAM detects whether the first NOP arrives via the even or the odd command-decode pipeline. Then, if the first NOP arrives via the odd pipeline, the DRAM does nothing. If the first NOP arrives via the even pipeline, the DRAM initiates the Clock-Sync scheme to sync the first NOP after SRX to the internal odd clock. For all subsequent SRE/SRX sequences, the DRAM will sync its internal clocks with what existed during the DCA training. For the DRAM to do this, the host is required to send SRX first NOP on the exact same clock phase that was used during the DCA training. In this way, the SRX/NOP Clock-Sync feature enforces repeatability of clock phases to an odd phase upon SRX. It also helps on minimizing repeatability of the additive/subtractive effect of the DCA training on Tx jitter. If the host sends SRX first NOP on different clock phase than the phase used during DCA training while the Clock-Sync feature is enabled, DCA adjustment may be in the wrong direction and could result in worse performance than without DCA adjustment.

The SRX/NOP Clock-Sync scheme is an optional feature on DDR5. MR13:OP[5] indicates to the host whether the SRX/NOP Clock-Sync feature is supported or not. When SRX/NOP Clock-Sync feature is enabled by MRW to MR13:OP[5]=1, to make the Clock-Sync Scheme fully functional, (1) the host (including RCD, Clock Driver) is responsible to ensure the phases of the system clock before and after SRX; (2) the host shall issue an initial SRE/SRX pair after CSTM/CATM prior to DCA training to ensure that the Clock-Sync is in effect during DCA training; (3) the continuous system clock during self-refresh is not required to make the Clock-Sync feature fully functional, but every first NOP registered after each $\text{t}^{\text{CSH\_SRExit}}$ shall be the same phase of system clock (for example, odd) that existed at the first NOP at $\text{t}^{\text{c}}+1$ cycle in the initial SRX sequence prior to DCA training so that DRAM can get the consistent phases of system clock when the DRAM does the clock sync; and (4) for DCA training at multiple frequencies, the first NOP after SRX for a given clock frequency shall be the same phase of

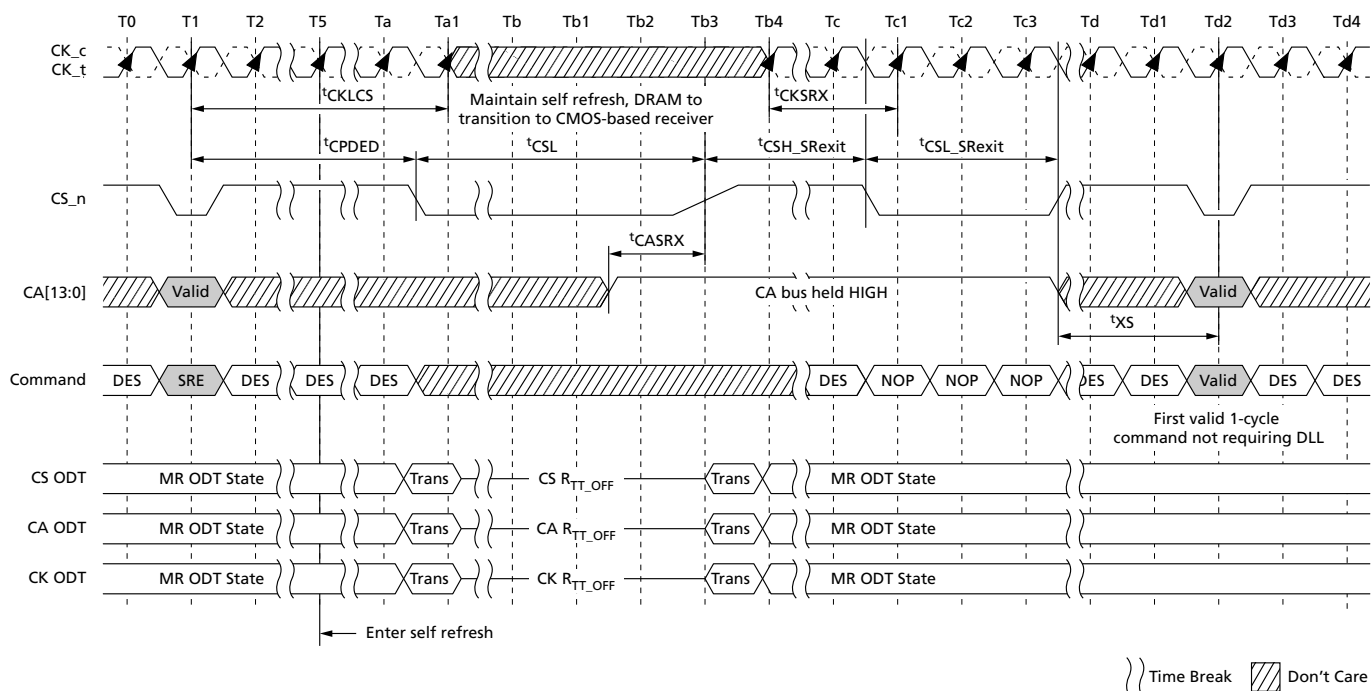
system clock (for example, odd) that existed at exit self refresh w/ frequency change mode prior to DCA training for that frequency.

Depending on the system environment and the amount of time spent in self refresh mode, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in the ZQ Calibration Commands section. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

Upon exiting self refresh, t_{REFI} begins when CS_n rises with t_{CSH_SRexit} (t_{b+3} in the Self Refresh Entry/Exit Timing with One-Cycle Exit Command figure below). One additional refresh must be issued in addition to normally scheduled refreshes. This additional refresh is not counted toward the computation of the average refresh interval (t_{REFI}). If this refresh is not issued by t_{REFI} after CS_n rises with t_{CSH_SRexit} , it counts toward the maximum number of refreshes which may be postponed. This additional refresh does not replace the regularly periodic refresh that is also scheduled at t_{REFI} after CS_n rises with t_{CSH_SRexit} (both of these REFRESH commands count toward the maximum number of refreshes which may be postponed). The additional refresh consists of a single REFAb command or $n \cdot REFsb$, where n is the number of banks in a bank group. If self refresh is to be re-entered, and no regularly scheduled periodic REFRESH commands have been issued, the additional refresh must be issued prior to self refresh re-entry. Additionally, FGR mode may require extra REFRESH command(s), in addition the aforementioned additional refresh, depending on the condition of the self refresh entry (see the Refresh Operation Scheduling Flexibility section for more information).

The exit timing from self refresh exit to first valid command not requiring a locked DLL is t_{XS} . The minimum value of t_{XS} is (t_{RFC1}). This delay is to allow for any refreshes started by the device to complete. t_{RFC1} continues to grow with higher density devices; therefore, t_{XS} will grow as well.

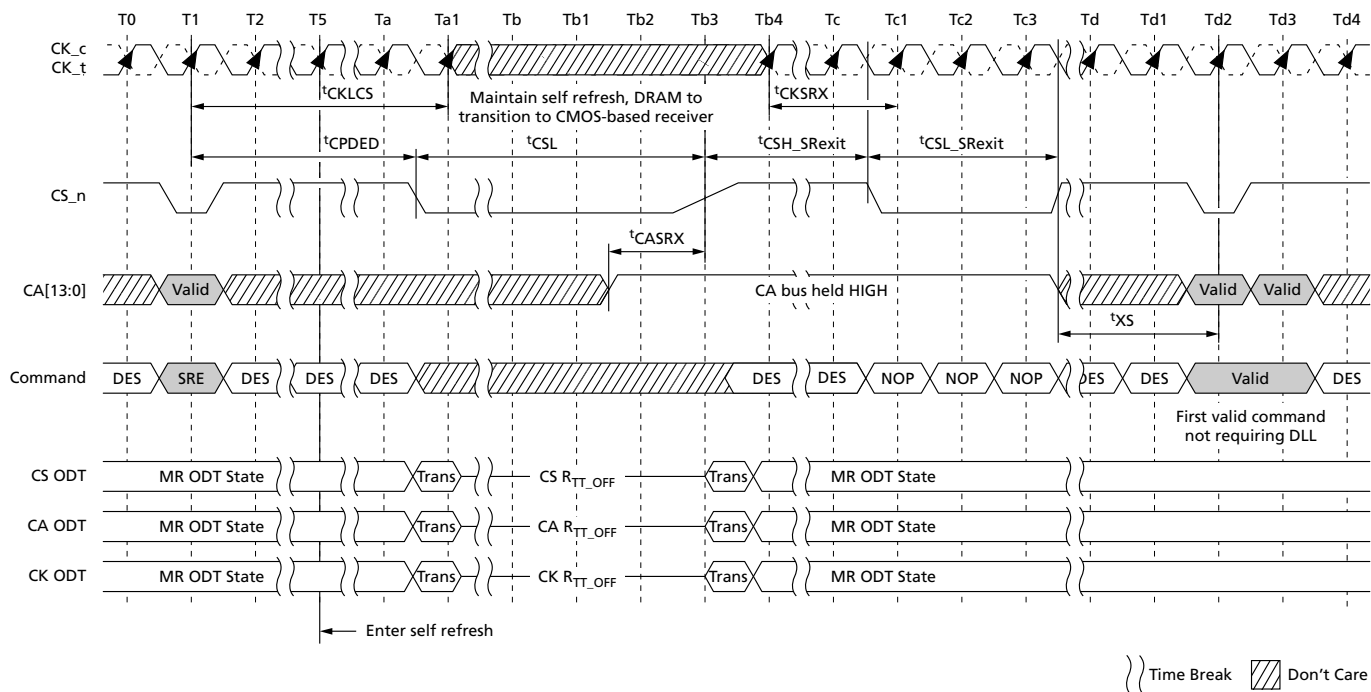
Figure 81: Self Refresh Entry/Exit Timing with One-Cycle Exit Command



Notes: 1. While in 2N mode, t_{CSL_SRExit} is not statically held LOW (as shown above) because it pulses for each two-cycle period. Refer to the 2N mode section for more details.

- When t_{CSH_SRExit} min expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at Tc1, the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters

Figure 82: Self Refresh Entry/Exit Timing with Two-Cycle Exit Command



- Notes:
- While in 2N mode, t_{CSL_SRExit} is not statically held LOW (as shown above) because it pulses for each two-cycle period. Refer to the 2N mode section for more details.
 - When t_{CSH_SRExit} min expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at Tc1, the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters

Partial Array Self Refresh (PASR)

Support for PASR has been deprecated. Details shown in this section are for devices that support the feature.

DDR5 devices may contain an optional feature that disables refresh to selected segments in each bank when in self-refresh mode. The feature enables lower self refresh power if portions of the devices are not required to retain data. Each bank is divided into six or eight segments based on the three highest row address bits supported by the device's density. Non-binary density devices are divided into six segments because the 110 and 111 encodings of the partial array self refresh (PASR) segment row bits are not used. Binary densities are divided into eight segments.

MR60 provides the segment mask for all banks, with one bit per segment. A 0 (default) in the bit position provides normal REFRESH operation for the segment, while a 1 masks that segment. Masked segments are **not** refreshed during self refresh. Note this affects self refresh only. All segments are refreshed by a REFRESH command when out of self-refresh mode.

Segments that are masked are not guaranteed to retain their data if self refresh is entered.

MR19:OP[7] bit indicates whether the device supports PASR. 0 = not supported; 1 = supported

Table 188: MR60 PASR Segment Definition

Segment (PASR Row Bits)	Type	Operand	Data	Note
Segment 0 (000)	W	OP0	0 = Normal, 1 = Masked	
Segment 1 (001)	W	OP1	0 = Normal, 1 = Masked	
Segment 2 (010)	W	OP2	0 = Normal, 1 = Masked	
Segment 3 (011)	W	OP3	0 = Normal, 1 = Masked	
Segment 4 (100)	W	OP4	0 = Normal, 1 = Masked	
Segment 5 (101)	W	OP5	0 = Normal, 1 = Masked	
Segment 6 (110)	W	OP6	0 = Normal, 1 = Masked	Must be 0 for 24Gb devices
Segment 7 (111)	W	OP7	0 = Normal, 1 = Masked	Must be 0 for 24Gb devices

Table 189: PASR Segment Row Address Bits

DRAM Density	PASR Row Bits	Segments
8Gb	R15:13	8
16Gb	R15:13	8
24Gb	R16:14	6
32Gb	R16:14	8

Input Clock Frequency Change

Once initialized, the device requires the clock to be stable during almost all states of normal operation. Once the clock frequency has been set and is in the stable state, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under self refresh with frequency change mode. Outside of self refresh with frequency change mode, it is illegal to change the clock frequency.

Prior to entering self refresh with frequency change mode, the host must program ^tCCD_L/^tCCD_L_WR/^tCCD_L_WR2/^tDLLK via MPC command to update MR13 shadow register to the desired target frequency and configure VREFCA, VREFCS, RTT_CK, RTT_CS and RTT_CA (MR11, MR12, MR32 and MR33) shadow registers if needed.

Once the device has been successfully placed into self refresh with frequency change mode and ^tCKLCS has been satisfied, the state of the clock becomes a don't care. Once in the don't care state, changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^tCKSRX. During ^tCSL_FreqChg and prior to exiting self refresh, the device will automatically apply the changes to ^tCCD_L/^tCCD_L_WR/^tCCD_L_WR2/^tDLLK, VREFCA, VREFCS, RTT_CK, RTT_CS and RTT_CA. Upon entering and exiting self refresh mode when changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in Self Refresh Operation.

For the new clock frequency, mode registers may need to be configured (to program the appropriate CL, preambles, write leveling internal cycle alignment, DFE, DCA, etc.) prior to normal operation. The device input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade.

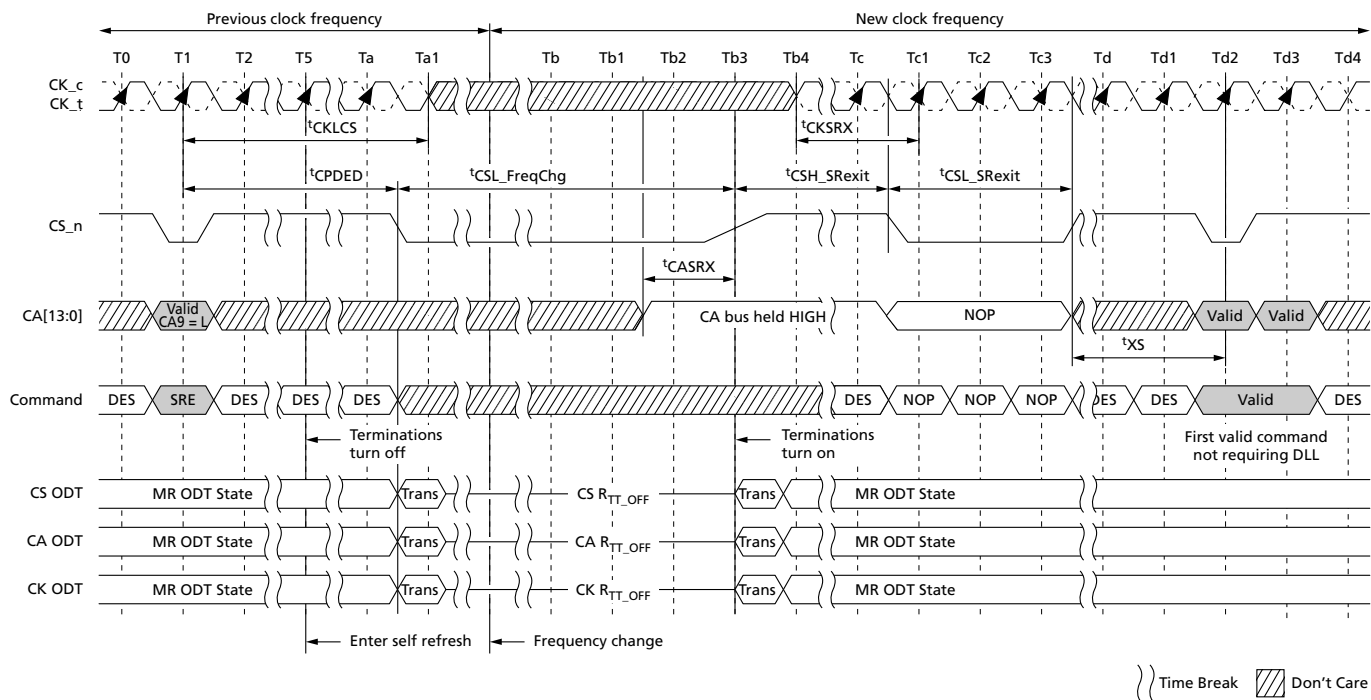
Input Clock Frequency Change Steps

The following steps must be taken to execute a frequency change in the DDR5 device:

1. Prior to executing the SRE command, the shadow register of mode registers MR11/MR12/MR13/MR32/MR33 can be pre-loaded at any time if the device is in an IDLE state:
 - a) The host must program ^tCCD_L/^tCCD_L_WR/^tCCD_L_WR2/^tDLLK via MR13:OP[3:0] to the desired target frequency. During this stage, the values are stored in the MR13 shadow register and shall be applied to MR13 automatically when running SREF w/ CA9=L on the device. This change occurs during ^tCSL_FreqChg when exiting self-refresh w/frequency change.
 - b) The host can optionally configure the appropriate CS/CA/CK ODT settings via mode register (MR32 and MR33) if new values are needed for the new target clock frequency. During this stage, these values are stored in the MR32 and MR33 shadow registers and will be applied to MR32 and MR33 automatically when running SREF w/ CA9=L on the device. This change occurs during ^tCSL_FreqChg when exiting self-refresh w/frequency change.
 - c) The host can optionally configure the VREFCA and/or VREFCS via their corresponding commands. During this stage, these values are stored in the MR11 and MR12 shadow registers and will be applied to (MR11 and MR12) automatically when running SREF w/ CA9=L on the device. This change occurs during ^tCSL_FreqChg when exiting self-refresh w/frequency change.
 - d) Entering and exiting self refresh with the SREF command shall replace the values of MR11, MR12, MR13, MR32 and MR33 with its their shadow register values.
2. Enter SELF REFRESH ENTRY WITH FREQUENCY CHANGE command by sending the SREF command (SRE w/CA9=1).
3. After ^tCPDED (MIN), host transition CS_n LOW, indicating to the device that the terminations are safe to turn off.
4. After ^tCKLCS, the host can turn the clocks off.

5. Device enters self refresh.
6. Changing the clock frequency is permissible, provided the new clock frequency is stable prior to t_{CKLSRX} .
7. Exiting self refresh with frequency change follows the same process as normal self refresh exit.
8. After t_{XS} , any additional mode registers requiring the DLL that are needed for the new frequency can be configured or other commands not requiring a DLL may be issued (ACT, MPC, MRW, PDE, PDX, PREab, PREsb, PREpb, REFab, REFsb, RFMab, RFMsb, SRE, VREFCA, and VREFCS).
9. After t_{XS_DLL} , normal operation resumes and all commands are legal.

Figure 83: Frequency Change During Self Refresh



- Notes:
1. While in 2N mode, t_{CSL_SRExit} will not be statically held LOW (as shown), as it will pulse for each 2-cycle period. Refer to the 2N mode section for more details.
 2. If no V_{REFCS} or V_{REFCA} changes are required by the new frequency, the normal t_{CSL} can be used.
 3. The figure shows a valid 2-cycle command after t_{XS} for simplicity. 1-cycle valid command is also legal.
 4. When t_{CSH_SRExit} (MIN) expires, the CA bus is allowed to transition from all bits HIGH to any valid (V) level. Prior to CS_n being registered LOW at TC1, the CA bus must transition to NOP conforming to the CAI state of the device and complying with applicable device input timing parameters.

Power-Down Mode

Power-down (PD) mode does not use CKE to control entry and exit. Instead, power-down mode entry/power-down exit uses the POWER DOWN ENTRY (PDE)/POWER DOWN EXIT (PDX/NOP) command, triggered by CS_n. After in PD mode, CS_n acts effectively like historic CKE, waiting for it to transition from HIGH to LOW (with its command). In PDE mode, CS_n should be sampled on every edge.

POWER-DOWN ENTRY and POWER-DOWN EXIT Commands

Power-down mode is entered when the POWER-DOWN ENTRY (PDE) command is registered. Unlike self refresh mode, CS_n is NOT held LOW constantly while in power-down. Timing is shown below with details for entry and exit of power-down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. Device design provides AC/DC timing and voltage specifications, along with proper DLL operation, as long as the controller complies with DRAM specifications.

During power-down, if all banks are closed after any in-progress commands are completed, the device will be in precharge power-down mode. If any bank is open after in-progress commands are completed, the device will be in active power-down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CS_n, RESET_n, which remain enabled throughout the duration of power-down. If CA[11] = L during the PDE command, command input buffers CA[1] and CA[4] remain enabled, enabling the appropriate non-target (NT) on-die termination (ODT) command to be passed through and decoded by the non-target DRAM in power-down (that is, the DRAM will monitor commands that use NT ODT and will not exit power-down as a result of a valid NT ODT command being registered). Optionally, command input buffers CA[0], CA[2], CA[3] and CA[5] may remain enabled if needed by the DRAM to properly decode the NT ODT commands during PDE and PDX.

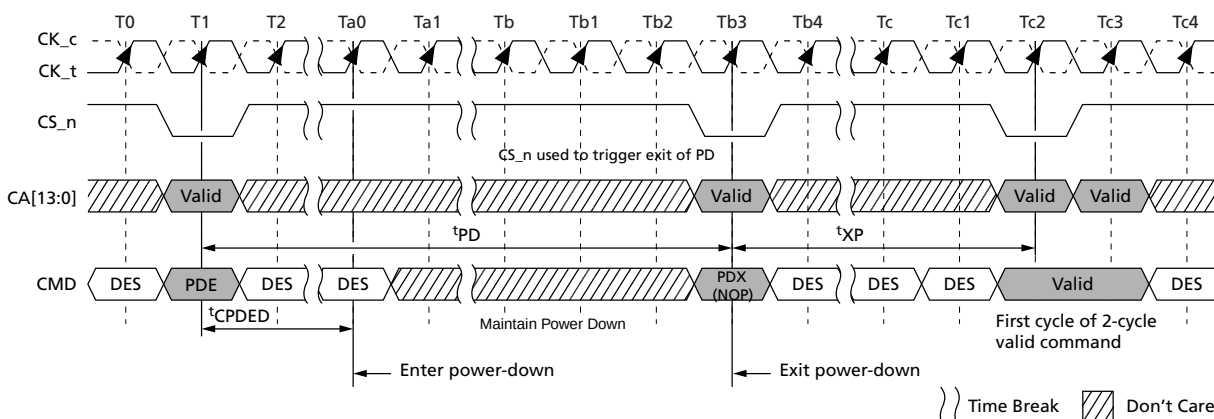
If CA[11] = H during the PDE command, only the NOP command qualified by CS_n is legal during power-down. If CA[11] = L during the PDE command, only NT ODT commands and NOP commands, qualified by CS_n, are legal during power-down. Refer to the command truth table for more information.

Although MRR is BL16 regardless of the MR0 burst length setting, the host must not issue MRR NT ODT commands during power-down when MR0:OP[1:0]=01.

When power-down is entered with NT ODT control enabled (CA[11] = L), the device will continue to accept NT commands throughout the power-down process, including entry and exit. Upon power-down entry, during the ^tCPDED period, the device will be switching from decoding all CA bus command bits to only decoding CA[1] and CA[4]. During this time, all CA command bits must be valid when CS is asserted with a complete READ or WRITE command, because the device may still be decoding the full command.

Following ^tCPDED, only CA[1] and CA[4] need be valid because the device will be ignoring the others. Following the PDX (NOP) command to exit power-down mode, all CA command bits also must be valid for NT termination commands, because the device will be transitioning to decoding all bits. In the optional case where command input buffers CA[0], CA[2], CA[3] and CA[5] remain enabled, all CA command bits must be valid when CS_n is asserted between the PDE command and the completion of ^tXP upon PDX. It is only the time between ^tCPDED completion and ^tXP_{start} that non-CA command bits (CA[13:6]) and CA command bits not being used for the NT ODT command decode need not be valid.

Figure 84: Power-Down Entry and Exit Mode



- Notes:
1. There is no specific PDX command. In the case of systems with register using CAI, the encoding out of the register may be inverted from a NOP-defined command.
 2. Image shows a valid 2-cycle command after t_{XP} for simplicity. 1-cycle valid commands are also legal.
 3. CS_n must be held HIGH, not toggled, during power-down (Ta to Tb2), except NON-TARGET ODT command when PDE with CA[11]=L is asserted.

Table 190: Power-Down Entry Definitions

Device Status	DLL	Power-Down Exit	Relevant Parameters
Active (one or more banks open)	On	Fast	t_{XP}
Precharge (all banks precharged)	On	Fast	t_{XP}

The DLL is kept enabled during precharge power-down or active power-down. (If RESET_n goes LOW during power-down, the device will move out of power-down mode and into reset state.) Power-down duration is limited by $t_{PD}(\text{MAX})$ of the device.

In the following table, the inclusion of Write-NT, Read-NT, and NOP reflects the subset of input signals used for decoding commands while in power-down mode with ODT enabled. These are the same input states detailed in the Command Truth Table. Note that Write-NT and Read-NT are two-cycle commands, requiring CS to be LOW for both cycles. NOP is the only single-cycle command allowed while in power-down mode.

Table 191: Valid Command During Power-Down with ODT Enabled

CA[1]	CA[4]	Command	Operation When Device is in Power-Down
L	L	WRITE	Device will enable ODT_WR_NOM
L	H	READ	Device will enable ODT_WR_NOM
H	L	ILLEGAL	Illegal. CS will NOT be asserted to a powered down device with this CA[1]/CA[4] combination
H	H	PDX (NOP)	Exit power-down

Note: 1. MRR NT ODT commands during power down are not allowed when MR0: OP[1:0]=01.

Maximum Power Saving Mode

Maximum power saving mode (MPSM) provides a way for the device to be in a low power state while also sharing its input signals with other devices that are active. MPSM is different in DDR5 than DDR4 because DDR5 lacks the CKE signal that DDR4 devices use to exit MPSM.

There are three MPSM states:

- Maximum power saving mode idle (MPSM idle)
- Maximum power saving mode power down (MPSM power down)
- Maximum power saving mode deep power down (MPSM deep power down)

These modes enable low power operation by causing the device to ignore most commands, while at the same time providing proper ODT on both CA and IO signals and a means for the device to be brought into an active state through exiting MPSM by issuing a MRW command.

MPSM is enabled by setting MR2:OP[3] = 1 using an MRW command, at which time the device enters MPSM idle. Alternatively, when MPSM for device 15 is enabled by setting the device 15 MPSM enable bit (MR2:OP[5] = 1) using an MRW command, and the device's PDA enumerate ID MR1:OP[3:0] = 15, the device enters MPSM idle.

Setting the device 15 MPSM enable bit to 1 must be done after PDA device enumeration is complete. Once the device is placed into MPSM idle, it can stay in that state indefinitely, or it can subsequently be placed in either MPSM power down or MPSM deep power down.

Data retention is not guaranteed when the device is in any MPSM state. Mode register status and soft PPR information is preserved.

Figure 85: Maximum Power Saving Mode State Diagram

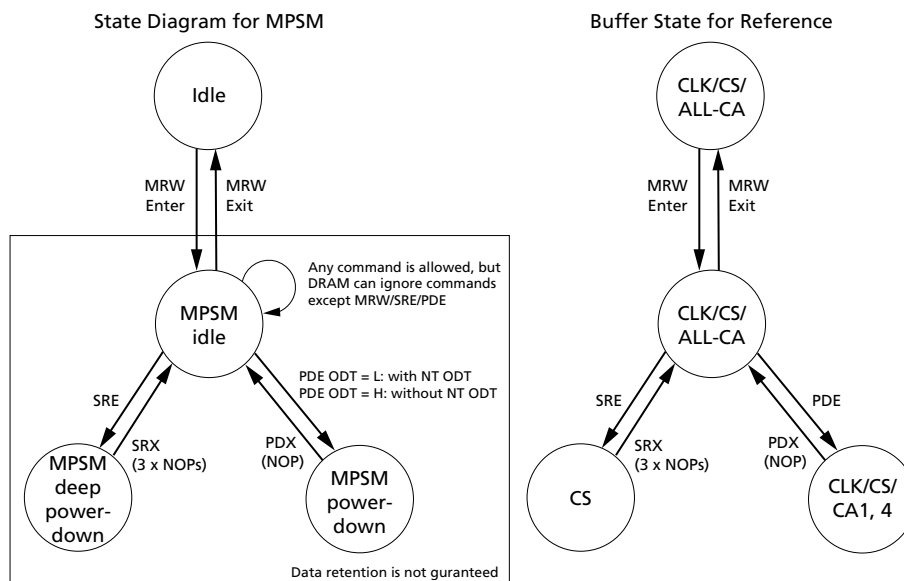


Table 192: MPSM Configuration Options

MPSM MR2:OP[3]	Device 15 MPSM MR2:OP[5]	PDA Enumeration ID MR1:OP[3:0]	Action
1	X	X	Enter MPSM on MRW
X	1	1111	Enter MPSM on MRW
0	0	X	Exit MPSM on MRW

Table 192: MPSM Configuration Options (Continued)

MPSM MR2:OP[3]	Device 15 MPSM MR2:OP[5]	PDA Enumeration ID MR1:OP[3:0]	Action
0	X	Not equal to 1111	Exit MPSM on MRW

MPSM Idle State

When the device is in MPSM idle, it ignores all types of commands except MRW, NT ODT, POWER DOWN ENTRY (PDE) and SELF REFRESH ENTRY (SRE). Only MRW commands to Exit MPSM Idle, as described in the MPSM Configuration Options table, shall be issued. For any other MRW command, the device shall first be taken out of MPSM Idle, then the MRW command may be issued. NT, ODT, PDE and SRE commands are executed normally. The device does not respond to any other command except these four command types. The DLL status is the same as in the normal idle state. The device continues to drive CA ODT as programmed. Normal command timing parameters are applied in this state, except that ^tREFI does not need to be satisfied because the REFRESH command does not need to be issued in this state.

MPSM Power Down State

MPSM power down state is entered by issuing the PDE command from MPSM idle. In this state, the device responds to the NT ODT command normally as it does in the precharged power down state. DLL status is the same as in the normal precharged power down state. When the PDX (NOP) command is issued to exit power down mode, the device returns to MPSM idle after ^tXP. Normal power down command timings are applied in this state, except the ^tREFI requirement.

MPSM Deep Power Down State

MPSM deep power down (DPD) state is entered from MPSM idle with the SRE command, and exited to MPSM idle with the 3 x NOPs used for the SELF REFRESH EXIT (SRX) command. Input signal requirements in this state are the same as those in self refresh mode. The device does not execute any internal REFRESH operations in this state. Normal SELF REFRESH command timings are applied in this state. When the SRX command is issued, the device returns to the MPSM idle state after ^tXS. ^tXS_DLL must be met prior to issuing any commands that require a locked DLL. Normal SELF REFRESH command timings are applied in this state.

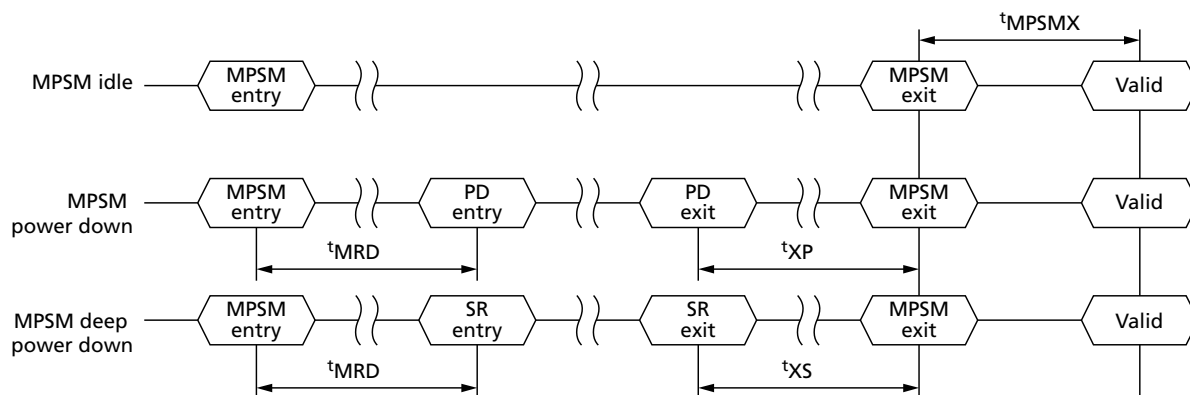
MPSM Command Timings

The device exits from MPSM idle by programming the MPSM enable (MR2:OP[3]) bit to 0 using the MRW command. MPSM exit to the first valid command delay is ^tMPSMX.

Table 193: MPSM Timing Parameters

Symbol	Description	MIN	MAX	Unit
^t MPSMX	MPSM exit to first valid command delay	^t MRD	-	ns

Figure 86: MPSM Exit Timings



Connectivity Test Mode

Connectivity test (CT) mode speeds up testing of electrical continuity of pin interconnection on the PC boards between the memory devices and the memory controller on the SoC.

Designed to work seamlessly with any boundary scan devices, CT mode is required for all devices independent of density and interface width. This applies to x4, x8, and x16 interface widths. Contrary to other conventional shift register-based test modes, where test patterns are shifted in and out of the devices serially in each clock, CT mode in DDR5 enables test patterns to be entered in parallel into the test input pins, and the test results are extracted in parallel from the test output pins of the device at the same time, significantly enhancing connectivity check speed.

Prior to entering CT mode, RESET_n is registered HIGH. CT mode is enabled by asserting the test enable (TEN) pin. After the device is placed in CT mode by asserting the TEN pin, the device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity test results are available for extraction in parallel at the test output pins after a fixed propagation delay. The device must be reset after exiting CT mode.

Pin Mapping

Only digital pins can be tested via CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the device are classified as one of the following types:

- **Test Enable (TEN) pin:** When asserted HIGH, this pin causes the device to enter CT mode. In this mode, the normal memory function inside the device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and is not used during normal memory operation.
- **Chip Select (CS_n) pin:** When asserted LOW, this pin enables the test output pins in the device. When de-asserted, the output pins in the device are HIGH-Z. The CS_n pin serves as the CS_n pin in CT mode.
- **Test Input:** This group of pins used during normal operation are designated as test input pins; these pins are used to enter the test pattern in CT mode. Most test input pins are input pins during normal operation. The ALERT_n pin is the only output pin that is used as a test input during CT mode. The CK_t and CK_c pins are single-ended test input pins during CT mode.
- **Test Output:** This group of pins used during normal operation are designated test output pins; these pins are used for extraction of the connectivity test results in CT mode.
- **Reset:** Fixed high level for RESET_n is required during CT mode (same as normal function).

Table 194: Pin Classification in CT Mode

Pin Type in CT Mode		Pin Names During Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Inputs	A	CA[13:0]
	B	CK_t, CK_c
	C	ALERT_n
Test Outputs		DQL[7:0], DQU[7:0], DQSU_t, DQSU_c, DQSL_t, DQSL_c, DML_n, DMU_n, DM_n/TDQS_t, TDQS_c
Reset		Reset_n

- Notes: 1. Test outputs may contain the upper and lower label identification used with x16 devices. In the case of x4/x8 devices, the lower identification may be removed.
2. CAI and MIR input levels do not affect test output values.

Table 195: Signal Description

Symbol	Type	Function
TEN	Input	Connectivity test mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of V_{DDQ} .

Logic Equations

MTx is an internal signal to be used to generate the signal to drive the output signals. These internal signals are the same across all interface widths and densities.

Table 196: Min Term Equations

Min Term	Intermediate Logic Nodes
MT0	XOR(CA[0,1,2,3,8,9,10,11])
MT1	XOR(CA[0,4,5,6,8,12,13], ALERT_n)
MT2	XOR(CA[1,4,9,12], CK_t, CK_c)
MT3	XOR(CA[2,5,7,10,13], CK_t)
MT4	XOR(CA[3,6,7,11], CK_c, ALERT_n)
MT0_B	!(MT0)
MT1_B	!(MT1)
MT2_B	!(MT2)
MT3_B	!(MT3)
MT4_B	!(MT4)

Table 197: Output Equations per Interface Width

Output	x16	x8	x4
DQL0	MT0	MT0	MT0
DQL1	MT1	MT1	MT1
DQL2	MT2	MT2	MT2
DQL3	MT3	MT3	MT3
DQL4	MT0_B	MT0_B	
DQL5	MT1_B	MT1_B	
DQL6	MT2_B	MT2_B	
DQL7	MT3_B	MT3_B	
DML	MT4	MT4	
TDQS_c		MT4_B	
DQSL_t	MT4	MT4	MT4
DQSL_c	MT4_B	MT4_B	MT4_B
DQU0	MT0		
DQU1	MT1		
DQU2	MT2		
DQU3	MT3		
DQU4	MT0_B		

Table 197: Output Equations per Interface Width (Continued)

Output	x16	x8	x4
DQU5	MT1_B		
DQU6	MT2_B		
DQU7	MT3_B		
DMU	MT4		
DQSU_t	MT4		
DQSU_c	MT4_B		

Note: 1. Test outputs may contain the x16 upper "U" and lower "L" label identification. In the case of x4 and x8 devices, the lower "L" identification would not be present.

Input Levels and Timing Requirement

Input levels during CT Mode are defined in the CT Mode Input Requirements for TEN, CS_n and Test Inputs Table.

RESET_n input level in C: CMOS DC high above 70% V_{DDQ} .

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon assertion of the TEN pin, the CK_t and CK_c signals are ignored and the device enters CT mode after time t_{CT_Enable} . In CT mode, no refresh activities in the memory arrays—initiated either externally (i.e., auto-refresh) or internally (i.e., self refresh)—are maintained.

The TEN pin may be asserted after the device completes power-on, after RESET_n has deasserted, the wait time after the RESET_n de-assertion has elapsed, and prior to starting the clock (CK_t, CK_c).

The TEN pin may be de-asserted at any time in CT mode. Upon exiting CT mode, the device states are unknown and the integrity of the original content of the memory array is not guaranteed; therefore, the reset initialization sequence is required. All output signals at the test output pins are stable within t_{CT_valid} after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained HIGH and LOW, respectively.

Figure 87: CT Mode Timing Diagram

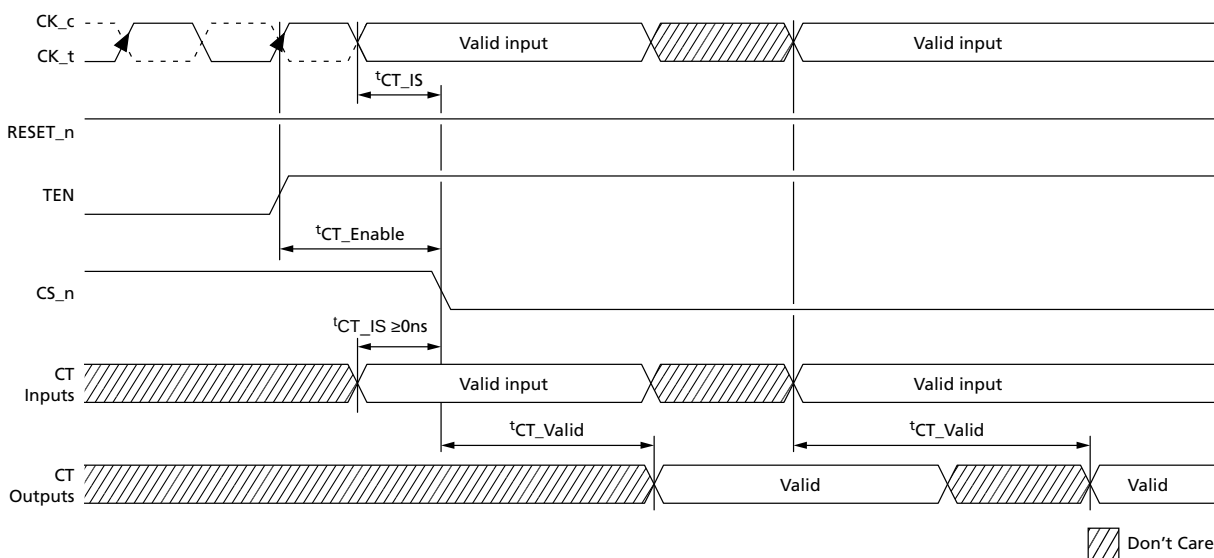


Table 198: CT Mode AC Parameters

Symbol	MIN	MAX	Unit
t_{CT_IS}	0	–	ns
t_{CT_Enable}	200	–	ns
t_{CT_Valid}	–	200	ns

Input Levels

The following input parameters are applied to input signals during CT mode.

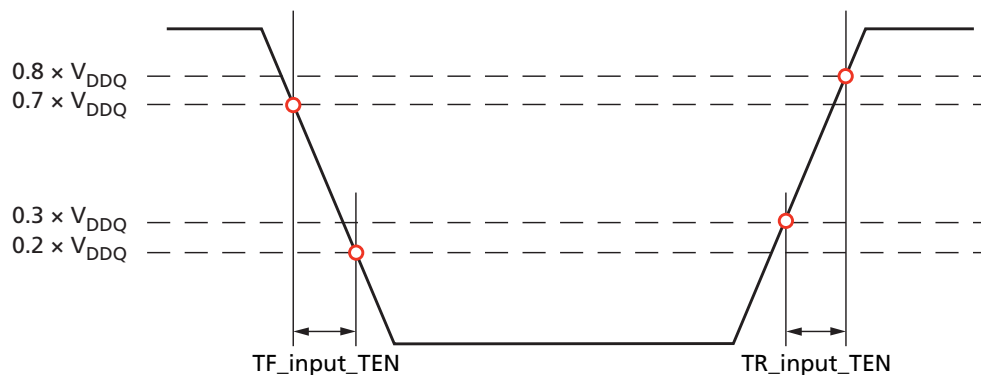
Table 199: CT Mode Input Requirements for TEN, CS_n and Test Inputs

Parameter	Symbol	MIN	MAX	Unit	Notes
TEN, CS_N, Test pins AC input high voltage	$V_{IH(AC\_CT)}$	$0.8 \times V_{DDQ}$	V_{DDQ}	V	1
TEN, CS_N, Test pins DC input high voltage	$V_{IH(DC\_CT)}$	$0.7 \times V_{DDQ}$	V_{DDQ}	V	
TEN, CS_N, Test pins DC input low voltage	$V_{IL(DC\_CT)}$	V_{SS}	$0.3 \times V_{DDQ}$	V	
TEN, CS_N, Test pins AC input low voltage	$V_{IL(AC\_CT)}$	V_{SS}	$0.2 \times V_{DDQ}$	V	2
TEN, CS_N, Test pins input signal falling time	TF_input_CT	–	10	ns	
TEN, CS_N, Test pins input signal rising time	TR_input_CT	–	10	ns	

Notes: 1. Overshoot may occur. It should be limited by the absolute maximum DC ratings.

2. Undershoot may occur. It should be limited by the absolute maximum DC ratings.

Figure 88: CT Mode Input Slew Rate Definition



CMOS Rail-to-Rail Input Levels for RESET_n

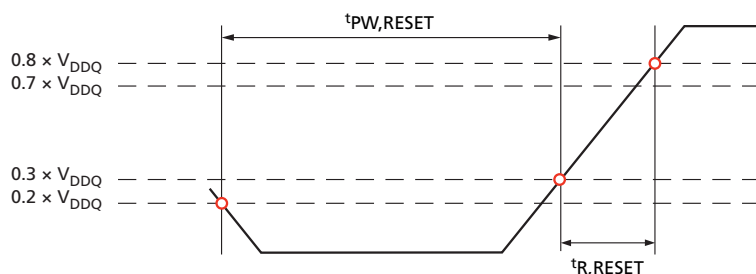
Table 200: CMOS Rail-to-Rail Input Levels for RESET_n

Parameter	Symbol	MIN	MAX	Unit	Notes
AC input high voltage	$V_{IH,AC,RESET}$	$0.8 \times V_{DDQ}$	V_{DDQ}	V	6
DC input high voltage	$V_{IH,DC,RESET}$	$0.7 \times V_{DDQ}$	V_{DDQ}	V	2
DC input low voltage	$V_{IL,DC,RESET}$	V_{SS}	$0.3 \times V_{DDQ}$	V	1
AC input low voltage	$V_{IL,AC,RESET}$	V_{SS}	$0.2 \times V_{DDQ}$	V	
Rise time	$t_{R,RESET}$	–	1.0	μs	4
RESET_n pulse width	$t_{PW,RESET}$	1.0	–	μs	3,5

Notes: 1. After RESET_n is registered LOW, RESET_n level must be maintained below $V_{IL,DC,RESET}$ during t_{PW_RESET} ; otherwise, the device may not be reset.

2. After RESET_n is registered HIGH, RESET_n level must be maintained above $V_{IH,DC,RESET}$; otherwise, device operation is not guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. This definition only applies to the reset procedure at power stable.
5. Overshoot may occur; it should be limited by the absolute maximum DC ratings.
6. Undershoot may occur; it should be limited by the absolute maximum DC ratings.

Figure 89: RESET_n Input Slew Rate Definition



Package Output Driver Test Mode

This optional mode enables characterization of the device package by allowing the host to individually turn on the output driver of a single bit of the device, while all other bits remain terminated. To use this test mode, the host sets MR61:OP[4:0] to select the target DM or DQ output driver. The host also sets the target driver to use the pull-up output driver Impedance of 34 ohms (MR5:OP[2:1] = 00b), while the termination for all the other DMs and DQs are defined by MR34:[2:0] (RTT_PARK). Note that all the supportability of DM termination is decided by MR5:OP[5]. However, when DM is selected as the target driver, the device must set the DM impedance according to MR5:OP[2:1], regardless of MR5:OP[5].

This is a test mode only. Normal functionality is not assumed while in this mode or after enabling this mode unless the device is reset. Enter this mode by programming any value in MR61 other than 0. It is only exited via a RESET to the device. Because this is an optional function, the discovery bit is located in MR5:OP[3].

A reset of the device is required after exiting the package output driver test mode.

Even though only five bits of the mode register are needed, the entire mode register is blocked out to isolate it from normal operating modes.

Table 201: MR5 Register (for reference only - see Mode Register Section for details)

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
5	Valid	Valid	DM Enable	Valid	PODTM Support	Valid	Valid	Valid

Note: 1. OP[7:0] can be programmed with either 0 or 1 appropriate to the other bits controlled by MR5.

Table 202: MR61 Register (for reference only - see Mode Register Section for details)

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
61	RSVD			Package Output Driver Test Mode				

ZQ Calibration Commands

MPC commands are used to perform ZQ calibration, which calibrates the output driver and command/address termination impedance across process, temperature, and voltage. ZQ calibration occurs in the background of device operation.

Two ZQ calibration modes are initiated with the MPC command: ZQCAL START (ZQCST) and ZQCAL LATCH (ZQCLH).

ZQCAL START (ZQCST) OP[7:0] = 0000 0101b initiates the device's calibration procedure and ZQCAL LATCH (ZQCLH) OP[7:0] = 0000 0100b captures the calibration result and loads it into the device drivers and termination circuits.

A ZQCAL START MPC command may be issued anytime the device is in a state in which it can receive valid commands. Two timing parameters are associated with ZQ Calibration: t_{ZQCAL} and t_{ZQLAT} . The table below tabulates the two ZW calibration timing parameters. t_{ZQCAL} is the time from when the ZQCAL START MPC command is sent to when the host can send the ZQCAL LATCH MPC command. t_{ZQLAT} is the time from when the ZQCAL LATCH MPC command is sent by the host to when the CA bus (and subsequently the DQ bus) can be used for normal operation. A ZQCAL LATCH MPC command may be issued anytime outside of power-down after t_{ZQCAL} has expired and all DQ bus operations have completed.

The CA bus must maintain a deselect ($CS_n = \text{HIGH}$) state during t_{ZQLAT} to enable CA ODT calibration settings to be updated.

Issuing consecutive ZQCAL START commands is permitted, and subsequent commands not violating t_{ZQCAL} of an ongoing ZQ calibration initiates a new ZQ calibration operation. ZQCAL START commands violating t_{ZQCAL} may or may not initiate a new ZQ calibration operation. In this case, t_{ZQCAL} should be counted from the last issued ZQCAL START command.

A ZQCAL LATCH command issued before the expiration of t_{ZQCAL} may latch or relatch the results of a previous ZQ calibration operation that completed the calibration. A ZQCAL LATCH command issued without rerunning the ZQ calibration operation relatches the results of the previous ZQ calibration operation that completed.

Table 203: ZQ Calibration Timing Parameters

Parameter	Symbol	Min	Units
ZQ calibration time	t_{ZQCAL}	1	μs
ZQ calibration latch time	t_{ZQLAT}	max(30ns, 8CK)	ns

The appropriate interval between ZQCAL START commands can be determined from the Voltage and Temperature Sensitivity tables below and other application-specific parameters. One method for calculating the interval between ZQCAL START commands, given the temperature ($T_{\text{driftrate}}$) and voltage ($V_{\text{driftrate}}$) drift rates that the device is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(TSens \times T_{\text{driftrate}}) + (VSens \times V_{\text{driftrate}})}$$

Where $TSens = \max(dRTdT, dRondT)$ and $VSens = \max(dRTdV, dRondV)$ define the device temperature and voltage sensitivities.

For example, if $TSens = 1.5\% / ^\circ\text{C}$, $VSens = 0.15\% / \text{mV}$, $T_{\text{driftrate}} = 1^\circ\text{C} / \text{sec}$ and $V_{\text{driftrate}} = 15 \text{ mV} / \text{sec}$, the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

Table 204: ODT Temperature and Voltage Sensitivity

Parameter	Min	Max	Unit
dRTTdT	-1.5	1.5	%/°C
dRTTdV	-0.15	0.15	%/mv

Note: 1. The amount of changes might be design guaranteed, and the actual number would be vendor-specific.

Table 205: Ron Temperature and Voltage Sensitivity

Parameter	Min	Max	Unit
dRondT	-1.5	1.5	%/°C
dRondV	-0.15	0.15	%/mv

Note: 1. The amount of changes might be design guaranteed, and the actual number would be vendor-specific.

ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm $\pm 1\%$ tolerance external resistor must be connected between ZQ and V_{SS} .

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, the device controller must ensure that the ZQ calibrations for each rank do not overlap.

The total capacitive loading on the ZQ pin must not exceed the max external loading of 25pf, with the addition of the device ZQ pincap (5pf) for a total capacitive loading of 30pf.

Per-DRAM Addressability

Per-DRAM addressability (PDA) enables programming of a given device in a rank. For example, it can program different ODT or V_{ref} values on each device on a given rank. Per-DRAM addressability (PDA) applies to MRW, MPC, VREFCA and VREFCS commands. Some per-DRAM settings are required prior to training the CA and CS timings and the DQ write timings. The MPC, VREFCA, and VREFCS command timings with extended setup/hold and multicycle CS assertion may be used for PDA commands if the CA and CS timings have not yet been trained.

DDR5 introduces a CA interface-only method for per-DRAM addressability by having a unique PDA enumerate ID programmable in each device in a rank and the ability to set a PDA select ID for targeted execution of supported commands, as described in the table below.

The unique PDA enumerate ID requires the use of the DQ0 signals of each device in the rank (DQL0 in the x16 configuration), and a PDA enumerate programming mode available through the MPC commands. The PDA enumerate ID and PDA select ID are 4-bit fields. After the PDA enumerate ID is programmed into a device, subsequent commands targeted to that device will not use the DQ0/DQL0 signal (legacy PDA method) to select the device for the commands. Instead, when the PDA select ID (MR1:OP[7:4]) is the same as the PDA enumerate ID (MR1:OP[3:0]), or when the PDA select ID is set to the all-DRAM code of 1111b, the device can be written with an MPC, MRW, VREFCA or VREFCS command. A few MPC commands do not use the PDA select ID to determine if the command is applied; among these are the MPC opcodes to set the PDA enumerate ID and the opcode to set the PDA select ID. During the reset procedure, the receive FIFO must be initialized with all 1s to ensure the PDA enumerate flow does not program an enumerate ID when the strobes are not toggling.

The table below summarizes which MPC commands are dependent on the PDA Select ID values.

Table 206: Commands Supporting/Not Supporting PDA Select ID Usage

Command	Op-code	Uses PDA Select ID to Determine When to Execute Command	Note
MRW	All	Yes	
VREFCA	All	Yes	
VREFCS	All	Yes	
MPC	(Group A and B) RTT_CA	Yes	
MPC	(Group A and B) RTT_CS	Yes	
MPC	(Group A and B) RTT_CK	Yes	
MPC	Set RTT_PARK	Yes	
MPC	Set DQS_RTT_PARK	Yes	
MPC	Apply VREFCA, VREFCS, and RTT_CA/CS/CK	No	
MPC	Enter PDA enumerate programming mode	No	
MPC	Exit PDA enumerate programming mode	No	
MPC	PDA enumerate ID	No	1
MPC	PDA select ID	No	
MPC	All other MPC opcodes	No	

Note: 1. The PDA enumerate ID op-code is the only MPC command that utilizes the PDA enumerate ID programming mode.

Table 207: PDA Mode Register Fields

MR Address	Operating Mode	Description
MR1:OP[3:0]	PDA enumerate ID[3:0]	This is a read-only MR field, which is only programmed through an MPC command with the PDA enumerate ID opcode. xxxxb encoding is set with MPC with the PDA enumerate ID opcode. This can only be set when PDA enumerate programming mode is enabled and the associated DQ0/DQL0 is asserted LOW. The PDA enumerate ID opcode includes four bits for this encoding. Default setting is 1111b.
MR1:OP[7:4]	PDA select ID[3:0]	This is a read-only MR field, which is only programmed through an MPC command with the PDA select ID opcode. xxxxb encoding is set with MPC with the PDA select ID opcode. The PDA select ID opcode includes four bits for this encoding. 1111b = all devices execute MRW, MPC, VREFCS, and VREFCA. For all other encodings, devices execute MRW, MPC, VREFCS, and VREFCA only if PDA select ID[3:0] = PDA enumerate ID[3:0], with some exceptions for specific MPC commands that execute regardless of PDA select ID. Default setting is 1111b.

PDA Enumerate ID Programming

1. PDA enumerate programming mode is enabled by sending one or more MPC command cycles with OP[7:0]=0000 1011b. Data mask and PDA enumerate are not supported for use at the same time. Either data mask must be disabled or DM_n driven HIGH while PDA enumerate programming mode is enabled.
2. In the PDA enumerate programming mode, only the MPC command with PDA enumerate ID opcode is qualified with DQ0 for x4/x8 and DQL0 for x16. The device captures DQ0 for x4/x8 and DQL0 for x16 by using DQS_c and DQS_t for x4/x8 and DQSL_c and DQSL_t for x16 signals as shown in the figure below) where DQ is driven LOW after the SET PDA enumerate ID opcode is set via the MPC command, and DQS starts toggling at 'PDA_DQS_DELAY and DQ is held until after DQS stops toggling. An alternate method is shown in the Single Device PDA Enumerate Programming in Continuous DQS Toggle Mode figure, where DQ is driven LOW and DQS toggles continuously starting prior to the SET PDA Enumerate ID command, and remains toggling until the Exit PDA Enumerate Programming Mode command has finished. If the value on DQ0 for x4/x8 or DQL0 for x16 is 0, the device executes the MPC command to set the PDA Enumerate ID. The controller may choose to drive all the DQ bits. Only the MPC command with PDA Enumerate ID opcodes will be supported in PDA Enumerate Programming mode, and the MPC command to exit PDA Enumerate Programming Mode does not require a DQ qualification.
3. For the "don't enumerate" case where a device is to ignore the MPC command with PDA enumerate ID opcode, the DQS_t/DQS_c and DQ signals (DQSL_t/DQSL_c and DQL/DQU for x16) may be HIGH (either driven or due to RTT_PARK termination) prior to sending the enter PDA enumerate program mode op-code via MPC command. After entering PDA enumerate programming mode, the DQ and DQS signals must remain HIGH until exiting PDA enumerate programming mode. Holding the signals HIGH will ensure this device is not programmed with a PDA enumerate ID, other than the default setting of 0xFh. See the Single Device PDA Enumerate Programming "Don't enumerate" Case in Legacy Mode figure.

Table 208: PDA Enumerate Results

DQS_t/c for x4/x8 (DQSL_t/c for x16)	DQ0 for x4/x8 (DQL0 for x16)	PDA Enumerate Result	Notes
Toggling	LOW	Enumerate	
Toggling	HIGH	Don't Enumerate	
HIGH	LOW	Unknown	1, 2
HIGH	HIGH	Don't Enumerate	2
Differentially LOW	Valid	Don't Enumerate	3

DQS_{t/c} are differential signals and small amounts of noise could appear as toggling, resulting in an unknown state for the PDA enumerate result.

When the DQS signals are HIGH, the DQ signals must be HIGH as well.

Differentially LOW is defined as DQS_t/DQSL_t = LOW and DQS_c/LDQS_c = HIGH.

- A minimum of one complete BL16 set of consecutive strobe edges (8 rising edges and 8 falling edges), plus 1 rising edge and 1 falling edge for the 2 ^tCK and the 3 ^tCK preambles or 2 rising edges and 2 falling edges for the 4 ^tCK preamble) must be sent by the host beginning at ^tPDA_DQS_DELAY after the associated MPC command. The DQ value is captured during any strobe edge during the valid LOW duration of the target DQ. Valid LOW time is defined as the time between ^tPDA_S and ^tPDA_H. If the device captures a 0 on DQ0/DQL0 at any strobe edge in the strobe sequence, the MPC command initiated PDA enumerate ID command must be executed by the device. Because the write timings for the DQ bus have not been trained, the host must ensure a minimum of one complete BL16 set of consecutive strobe (8 rising edges and 8 falling edges, plus 1 rising edge and 1 falling edge for 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for 4 tCK preamble) occurs after a period of ^tPDA_DQS_Delay (MIN) after the associated MPC command. The BC8 OTF mode register setting in the device is ignored while in PDA enumerate programming mode. The DQS assumes preamble/postamble requirements (including the preamble and postamble DQS_t/DQS_c toggles).
- Prior to when the MPC command with enter PDA enumerate programming mode opcode is sent by the host, the host must drive DQS_t and DQS_c differentially LOW, other than when the burst of 16 strobe edges (including the preamble and postamble DQS_t/DQS_c toggles) is sent in association with the PDA enumerate ID MPC command. The host must also include preamble and postamble DQS_t/DQS_c toggles during the qualification of the PDA command. After PDA enumerate programming mode is enabled in the DRAM device, the host memory controller must wait ^tMPC_Delay to the time the first PDA enumerate ID MPC command is issued.
- In the PDA enumerate programming mode, only MPC commands to PDA enumerate ID opcode and exit PDA enumerate program mode opcode are allowed.
- In the PDA enumerate programming mode, the default (or previously programmed) RTT_PARK value is applied to the DQ signals.
- The cycle time for the MPC command with PDA enumerate ID opcode is defined as ^tPDA_DELAY_1 and ^tPDA_DELAY_2. This time is longer than the normal ^tMPC_Delay and must be met to provide time to latch the asserted DQ and complete the WRITE operation to the PDA enumerate ID mode register (MR1:OP[3:0]), prior to executing the next MPC command with PDA enumerate ID opcode (shown in figure below).
- To remove the device from PDA enumerate programming mode, send an MPC command with exit PDA enumerate programming mode opcode (PDAENPX), OP[7:0]=0000 1010b. The MPC command with exit PDA enumerate programming mode opcode is never qualified by the DQ settings and is applied to all devices in the rank.
- During the PDA enumerate ID programming mode, only one MPC command with PDA enumerate ID opcode is allowed to each device. After the PDA enumerate ID is programmed, any change for the PDA enumerate ID requires the device to re-enter into PDA enumerate ID programming mode.

As an example, the following sequence programs the PDA enumerate ID per device:

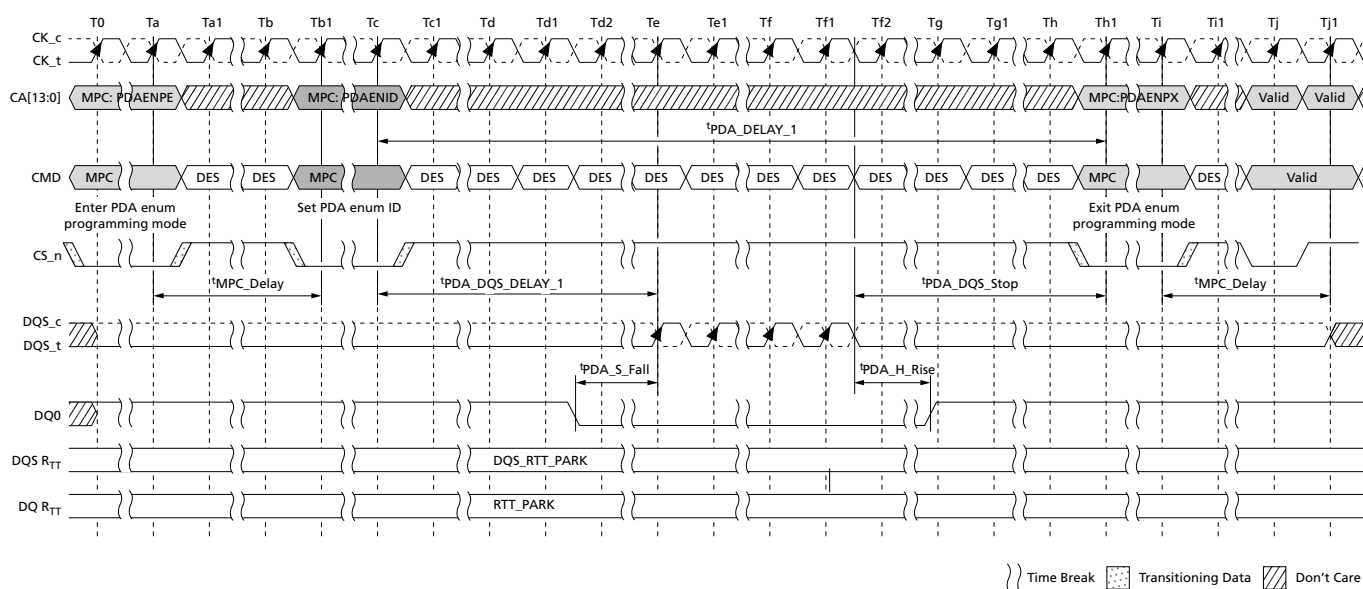
1. Send MPC command with **enter PDA enumerate programming mode** opcode, OP[7:0]=0000 1011b.
2. For (i = 0, i < MAX_DRAMS, i++), send MPC command with PDA enumerate ID opcode with i in the lower four bits of the opcode (4-bit value), with device i's DQ signals LOW.
3. Send MPC command with **exit PDA enumerate programming mode** opcode, OP[7:0]=0000 1010b.

The following figure shows a timing diagram for setting the PDA enumerate ID value for one device. In this case, only one device is programmed prior to exiting PDA enumerate programming mode, but many devices may be programmed prior to exiting this mode.

For a multidevice PDA Enumerate ID operation, the host may choose to either reiterate single-device enumeration as plotted in [Figure 90: Single-Device PDA Enumerate Programming in Legacy Mode](#) on page 212 and [Figure 91: Single-Device PDA Enumerate Programming in Continuous DQS Toggle Mode](#) on page 213, or follow suggested multidevice enumeration sequences as plotted in [Figure 92: Multidevice PDA Enumerate Programming in Legacy Mode With Dedicated DQS](#) on page 213 through [Figure 94: Multidevice PDA Enumerate Programming in Continuous DQS Toggle Mode](#) on page 215.

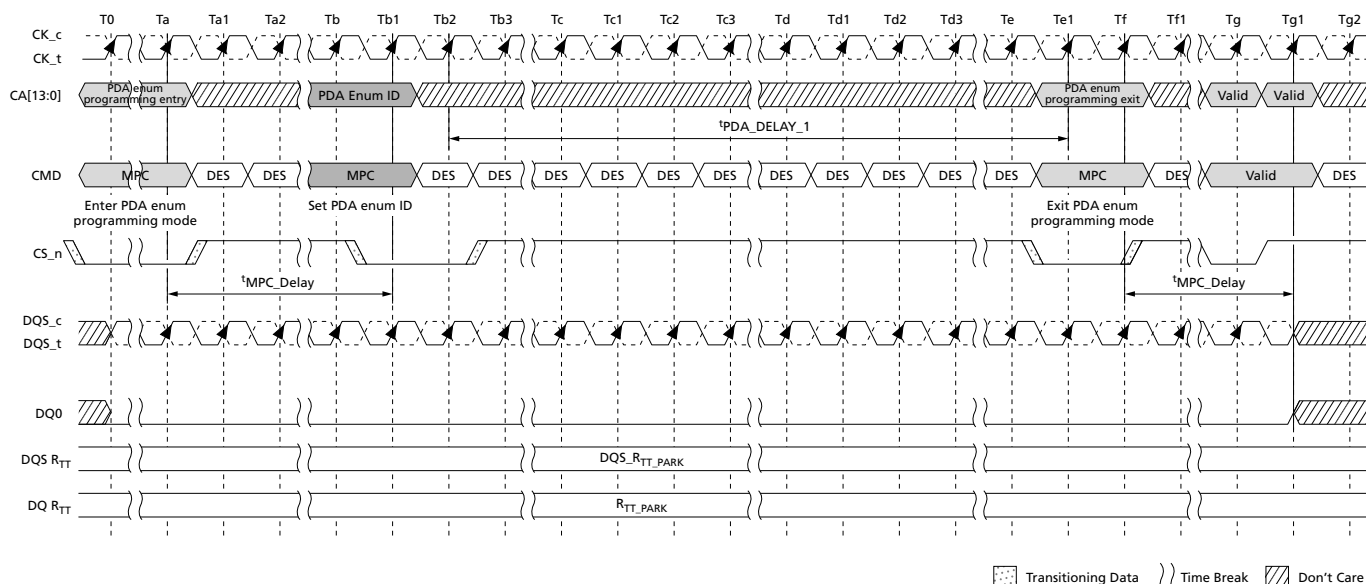
PDA Enumerate Programming With Resulting "Enumerate"

Figure 90: Single-Device PDA Enumerate Programming in Legacy Mode



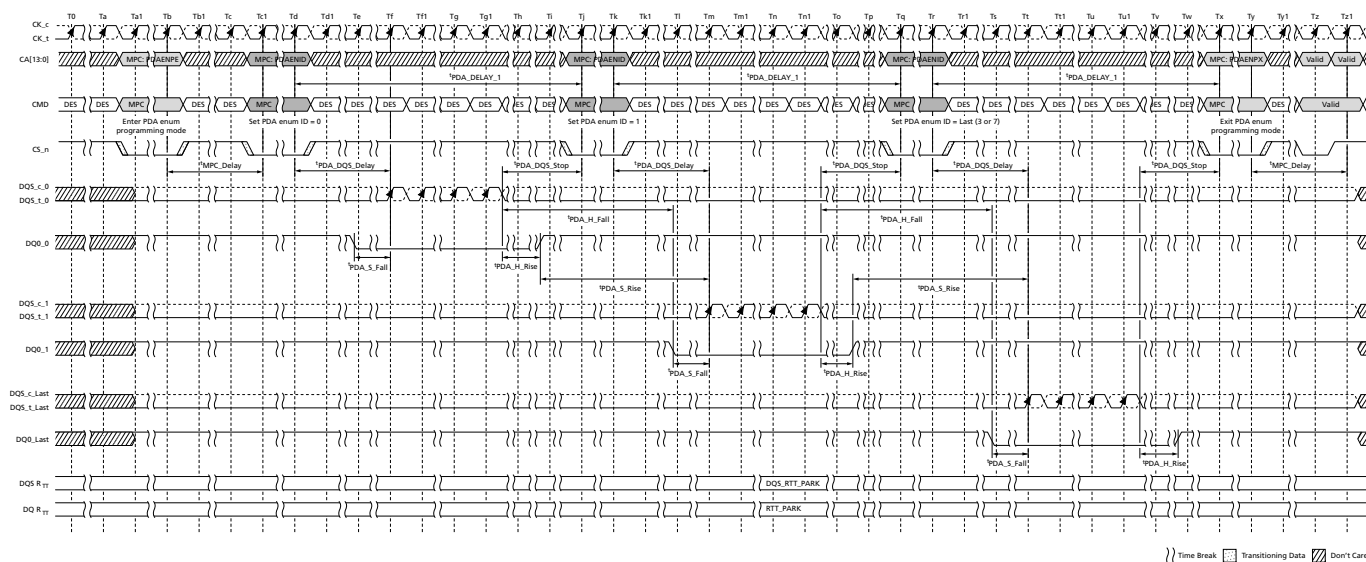
- Notes:
1. The figure assumes a multicycle MPC command and the timings are adjusted to visually show separation between timings, such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings, such as t_{PDF_Delay} .
 2. The figure above assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 t_{CK} and 3 t_{CK} preambles or 2 rising edges and 2 falling edges for the 4 t_{CK} preamble).
 3. $t_{PDA\_S\_FALL}$ and $t_{PDA\_H\_RISE}$ are minimum timing parameters, so DQ0 low from t_0 to t_{j+1} is valid.
 4. No more than one DQ0 transition can occur from t_0 to $t_{PDA\_S\_FALL}$, and no more than one DQ0 transition can occur from $t_{PDA\_H\_RISE}$ to t_{j+1} .

Figure 91: Single-Device PDA Enumerate Programming in Continuous DQS Toggle Mode



Note: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.

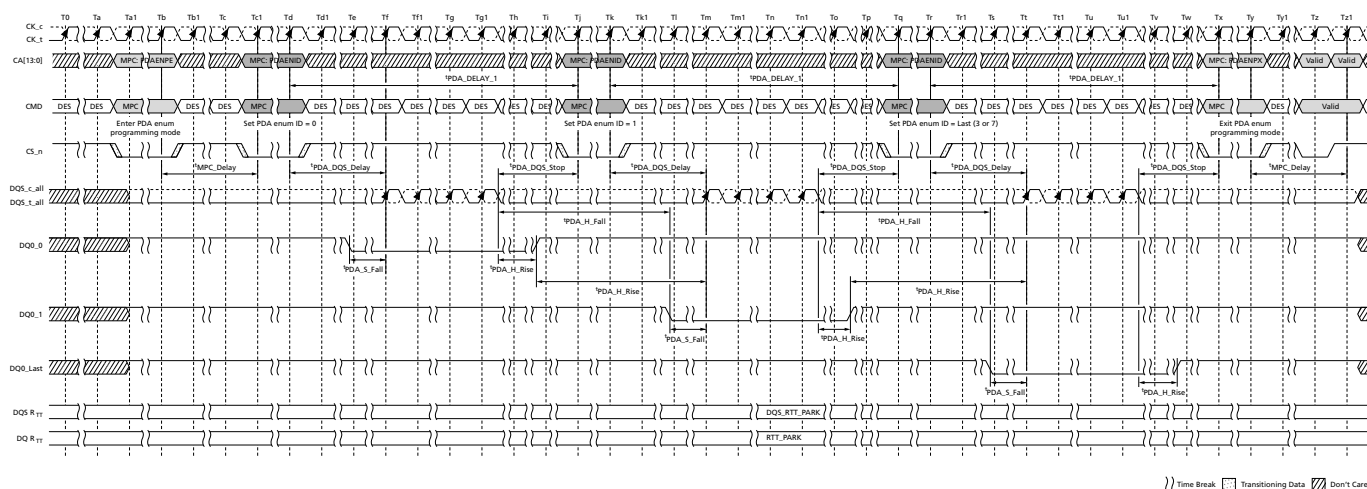
Figure 92: Multidevice PDA Enumerate Programming in Legacy Mode With Dedicated DQS



- Notes:
1. The figure assumes multicycle MPC commands and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.
 2. The figure assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 t_{CK} and 3 t_{CK} preambles or 2 rising edges and 2 falling edges for the 4 t_{CK} preamble).
 3. $t_{PDA\_S\_Fall}$ and $t_{PDA\_H\_Rise}$ are minimum timing parameters, so DQ0 low from t_{a+1} is valid, and DQ0_Last low to t_{z+1} is valid.
 4. No more than one DQ0 transition can occur from t_{a+1} to $t_{PDA\_S\_Fall}$, and no more than one DQ0 transition can occur from $t_{PDA\_H\_Rise}$ to t_{z+1} .

5. $t_{PDA\_DQS\_DELAY}$ and $t_{PDA\_DQS\_STOP}$ apply to all DQ states.

Figure 93: Multidevice PDA Enumerate Programming in Legacy Mode With all DQS



Notes: 1. The figure assumes multicycle MPC commands and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.

2. The figure assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2nd CK and 3rd CK preambles or 2 rising edges and 2 falling edges for the 4th CK preamble).

3. $t_{PDA\_S\_FALL}$ and $t_{PDA\_H\_RISE}$ are minimum timing parameters, so DQ0 low from t_a+1 is valid, and DQ0_Last low to t_z+1 is valid.

4. No more than one DQ0 transition can occur from t_{a+1} to $t_{PDA\_S\_FALL}$, and no more than one DQ0 transition can occur from $t_{PDA\_H\_RISE}$ to t_{z+1} .

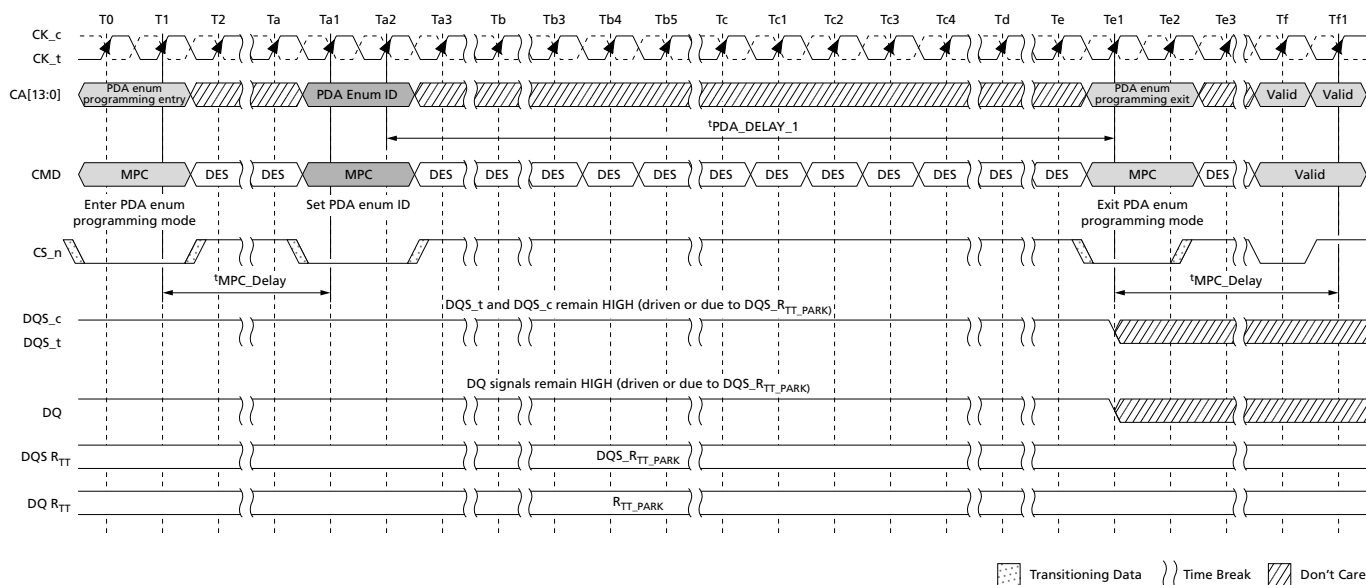
5. $t_{PDA\_DQS\_DELAY}$ and $t_{PDA\_DQS\_STOP}$ apply to all DQ states.

PDA Enumerate Programming With Resulting "Don't Enumerate"

The diagram illustrates the timing sequence for PDA enum programming. It shows the relationship between clock signals (CK_c, CK_t), address (CA[13:0]), command (CMD), chip select (CS_n), data strobes (DQS_c, DQS_t), data bus (DQ0), and data rates (DQS_RTT, DQ_RTT). The sequence includes entering programming mode, setting the enum ID, and exiting programming mode. Key timing parameters like $t_{PDA\_DELAY\_1}$ and t_{MPC_Delay} are marked. Data states are indicated as Valid, Don't Care, or Transitioning.

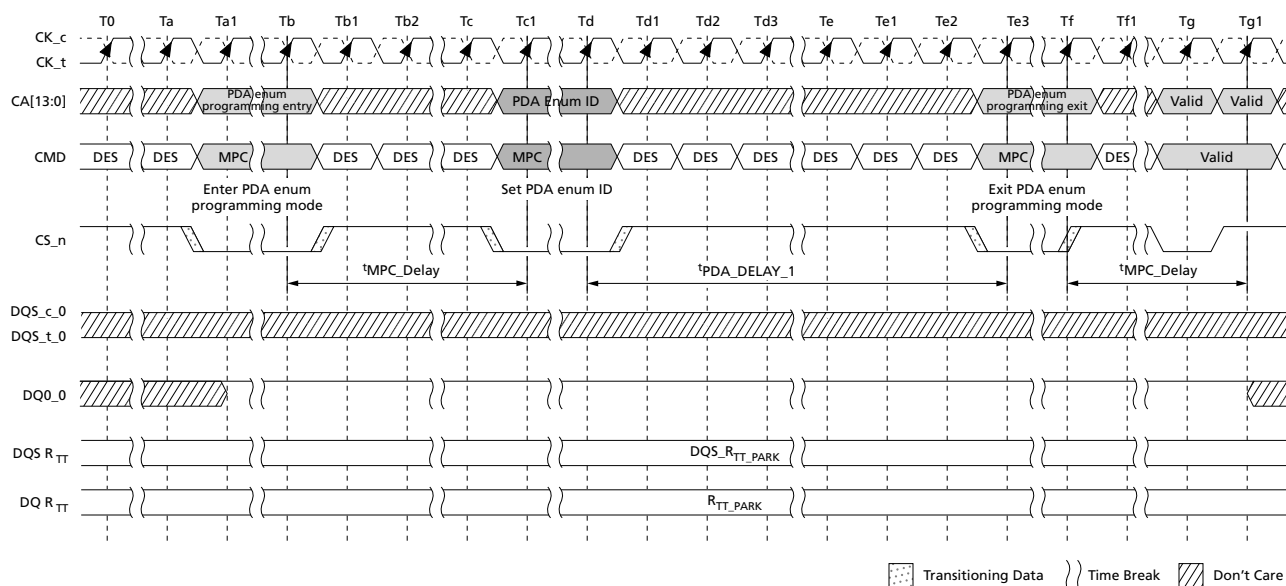
- Notes: 1. The diagram assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.
2. The figure assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 t_{CK} and 3 t_{CK} preambles or 2 rising edges and 2 falling edges for the 4 t_{CK} preamble).

Figure 96: Single-Device PDA Enumerate Programming Don't Enumerate Case in Continuous DQS Toggle Mode



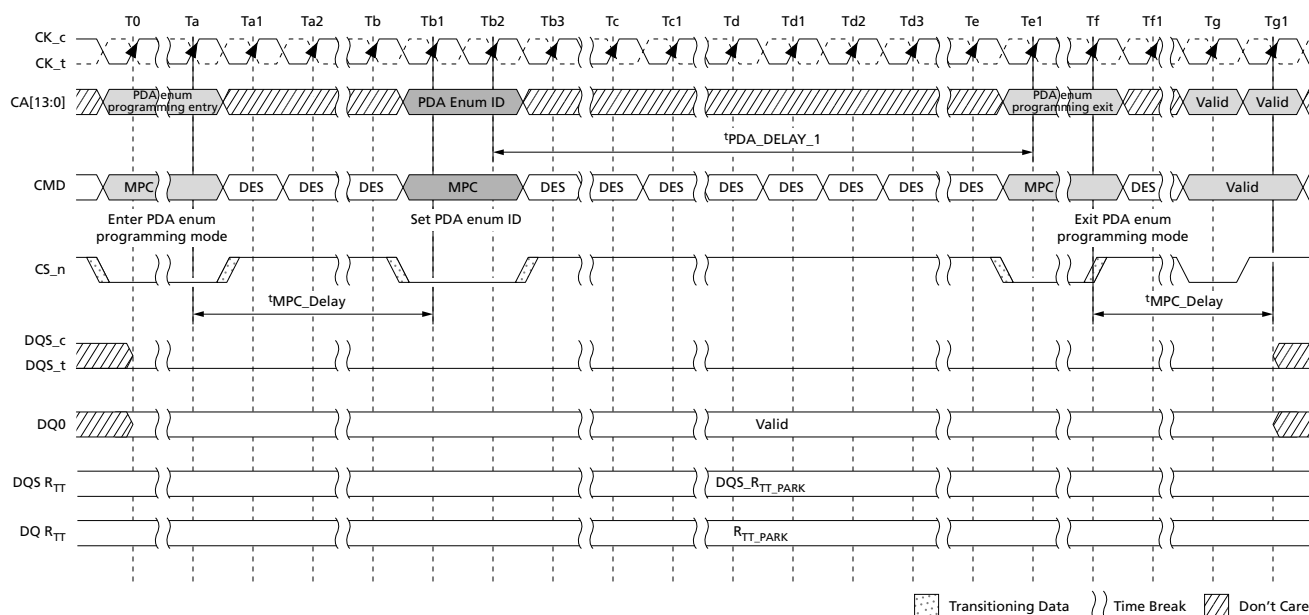
- Note: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.

Figure 97: Single-Device PDA Enumerate Programming Don't Enumerate Case for DQ Held HIGH With any DQS State



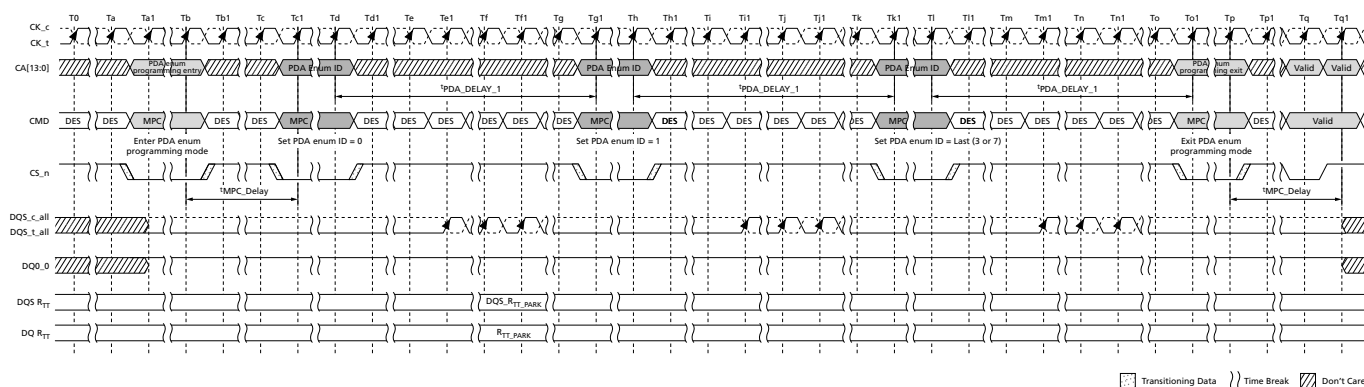
Note: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.

Figure 98: Single-Device PDA Enumerate Programming Don't Enumerate Case for DQ Valid and DQS is Differentially LOW



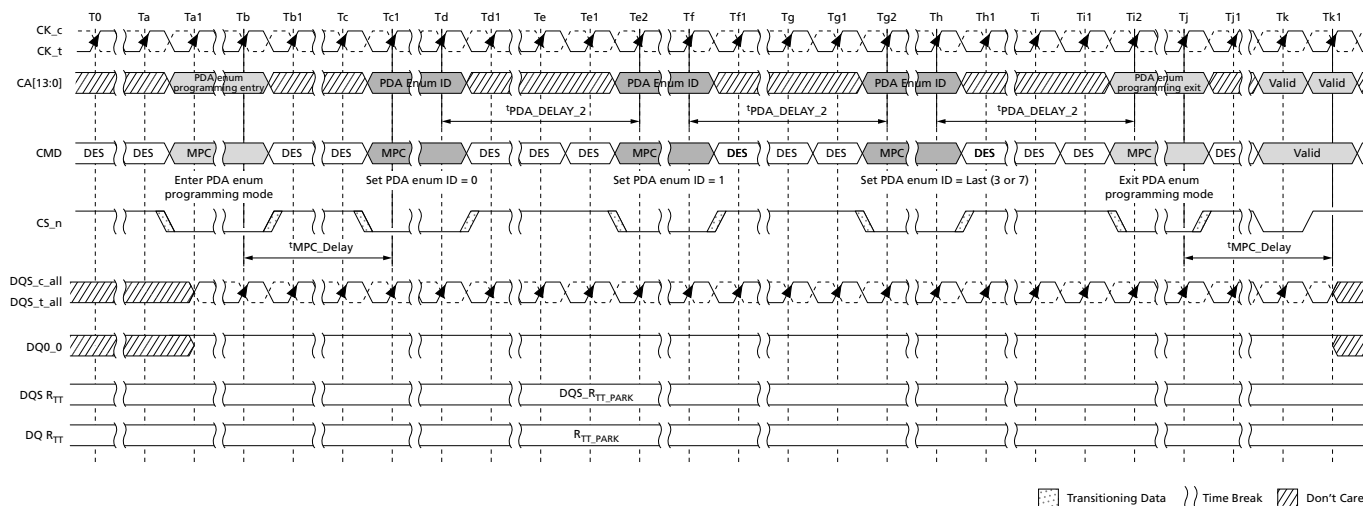
Notes: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.
2. DQ0 must not transition during valid state.

Figure 99: Multidevice PDA Enumerate Programming Don't Enumerate Case in Legacy Mode



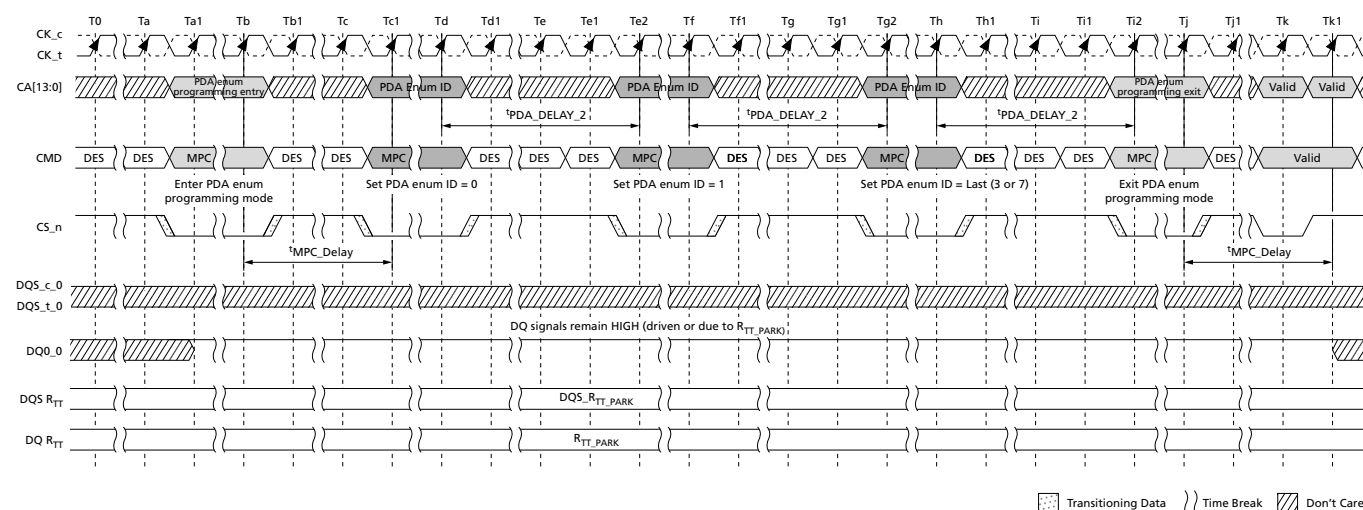
Notes: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_1}$.
2. The figure assumes preamble/postamble requirements for DQS (including 1 rising edge and 1 falling edge for the 2 t_{CK} and 3 t_{CK} preambles or 2 rising edges and 2 falling edges for the 4 t_{CK} preamble).

Figure 100: Multidevice PDA Enumerate Programming Don't Enumerate Case in Continuous DQS Toggle Mode



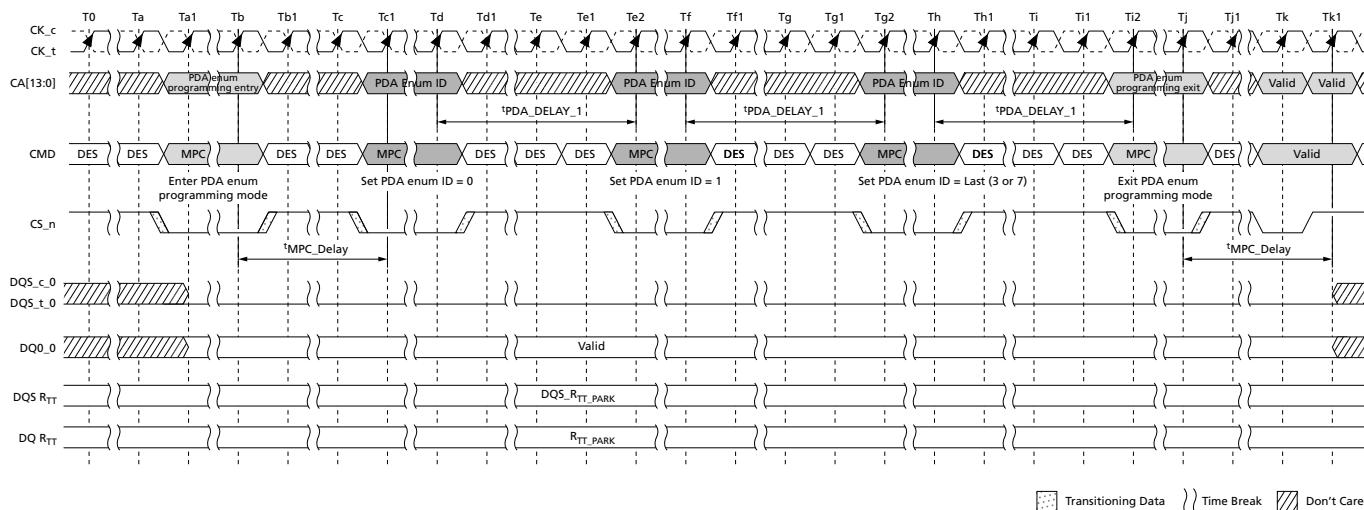
Note: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_2}$.

Figure 101: Multidevice PDA Enumerate Programming Don't Enumerate Case for DQ Held HIGH and any DQS State



Note: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_2}$.

Figure 102: Multidevice PDA Enumerate Programming Don't Enumerate Case for Valid DQ and Differentially LOW DQS



- Notes: 1. The figure assumes multicycle MPC command and the timings are adjusted to visually show separation between timings such as t_{MPC_Delay} (which start at the end of a command cycle and end at the beginning of the next) and other timings such as $t_{PDA\_DELAY\_2}$.
2. DQ0 must not be transitioned during valid state.

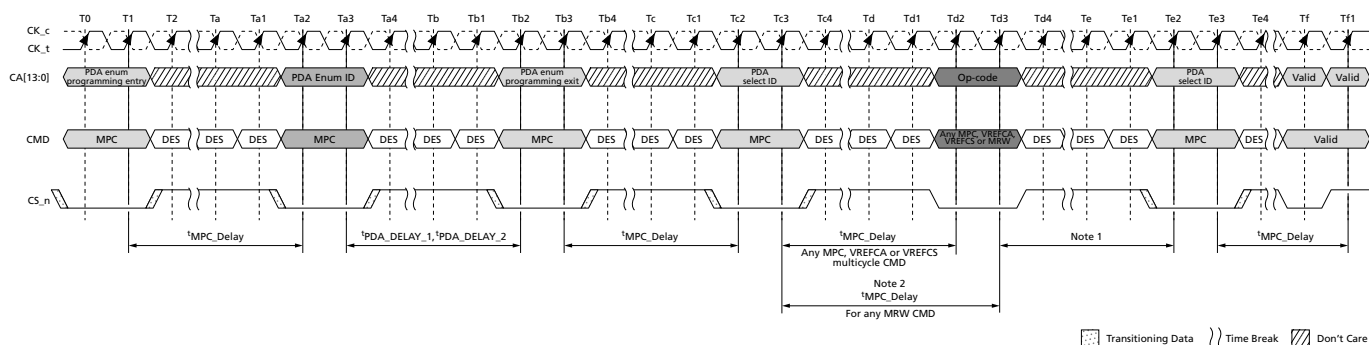
PDA Select ID Operation

After the PDA enumerate IDs have been programmed in all devices, the execution of future MPC/MRW/VREFCA/VREFCS commands depends on the value of the PDA select ID and the type of MPC command. If PDA select ID = 1111b, all devices execute the command. For all MRW, VREFCA and VREFCS commands, and some of the MPC commands (RTT_CA/CS/CK and RTT_PARK opcodes), the PDA select ID is compared to the PDA enumerate ID to determine if the device executes the commands. For all other MPC commands (that is, not the RTT_CA/CS/CK and RTT_PARK opcodes), the device executes the command regardless of the PDA select ID value.

As an example, the following sequence could be used to program unique MR fields per device:

1. Send MPC with PDA select ID opcode, with encoding 0000 included in the opcode.
2. Send MRWs for field settings specific to device 0000. This can be any number of MRWs.
3. Send MPC with PDA select ID opcode, with encoding 0001 included in the opcode.
4. Send MRWs for field settings specific to device 0001. This can be any number of MRWs.
5. Repeat for any number of devices.
6. Send MPC with PDA select ID opcode, with encoding 1111 included in the opcode to enable all devices to execute all MRW, VREFCS, VREFCA, and MPC commands.

Figure 103: Multicycle MPC Command Sequencing with PDA Enumerate and PDA Select ID



- Notes:
1. Commands such as MPC, VREFCA, VREFCS, or MRW have different command spacing requirements. Refer to the command sections for details.
 2. Any multicycle MPC, VREFCA or VREFCS command spacing is measured from the last valid command cycle to the first following valid command cycle, while standard command spacing goes from the last valid command cycle to the last valid command cycle. See MRW command period diagrams for details.

CS Training Mode

CS Training Mode (CSTM) facilitates the loopback of a sampled sequence of the CS_n signal.

In this mode, the CK is running and the CA signals are held in a NOP command encoding state. Once this mode is enabled and the devices are selected to actively sample and drive feedback, the device samples the CS_n signal on the rising edge of CK. Every set of four CK rising edge samples is included in a logical computation to determine the CSTM output result that is sent back to the host on the DQ bus. Once sampling begins, the device must maintain the consecutive grouping of the samples every 4^tCK. When the CS_n Sample[0] and Sample[2] result in a logic 0 and the CS_n Sample[1] and Sample[3] result in a logic 1, the device drives a 0 on all DQ signals. There is no requirement to drive any strobes, and the output signal could transition as often as every 4^tCK.

Entry and Exit

CSTM is enabled when the host sends the MPC command with enter CS training mode opcode (CSTMN) (OP[7:0] = 0000 0001B). Since CS training must occur prior to establishing alignment between CK and CS_n signals, the MPC command extends beyond multiple ^tCK cycles, during which the CS_n signal is asserted. This avoids causing the device to latch invalid commands, as might happen when the CS_n-to-CK setup time is not met. In this mode, commands are actively processed. The only commands that should be sent by the host memory controller while CSTM is enabled are the NOP command and the MPC command with exit CS training mode opcode (CSTMX), OP[7:0] = 0000 0000B. Any other command may produce unreliable results.

Once enabled, the device begins sampling on every rising CK edge, with the four sample groups looping consecutively. Depending on the value of the samples, the DQ signals are driven HIGH or LOW. Prior to entering CSTM, DQ signals are not driven by the device and are terminated according to the default RTT_PARK setting. Once enabled, the DQ signal begins driving the output values based on the CSTM samples. Once the DQ signals are driven by the device, RTT_PARK termination is no longer applied, similar to a READ operation.

To exit CSTM, a MPC command with exit CS training mode opcode (CSTMX) must be sent. Even though the timing relationship between CS_n and CK is understood when exiting CSTM, the host can either send a multi-cycle CS_n assertion during the MPC command while MR2:OP[4] = 0B.

Operation

In CSTM, the CS_n values are sampled on all CK rising edges. Each group of four consecutive samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending to the DQ output. The samples evaluation to determine the output is as follows:

Table 209: Sample Evaluation for Intermediate Output [0]

Intermediate Output[0]	CS _n Sample[0]	CS _n Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 210: Sample Evaluation for Intermediate Output [1]

Intermediate Output[1]	CS _n Sample[2]	CS _n Sample[3]
1	0	0
0	0	1
1	1	0

Table 210: Sample Evaluation for Intermediate Output [1] (Continued)

Intermediate Output[1]	CS_n Sample[2]	CS_n Sample[3]
1	1	1

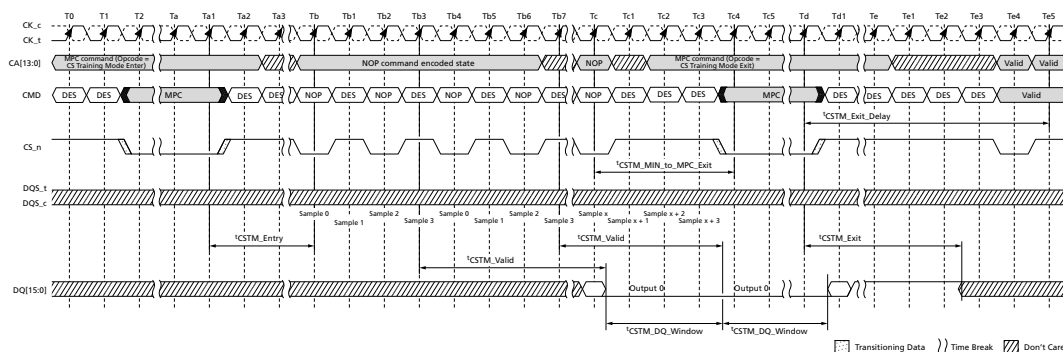
Table 211: Sample Evaluation for Final CSTM Output

CSTM Output ¹	Intermediate Output[0]	Intermediate Output[1]
0	0	0
1	0	1
1	1	0
1	1	0

Note: 1. When there is no change on the CSTM output from previous evaluation, DQ will continue to drive the same value continuously with no switching on the bus.

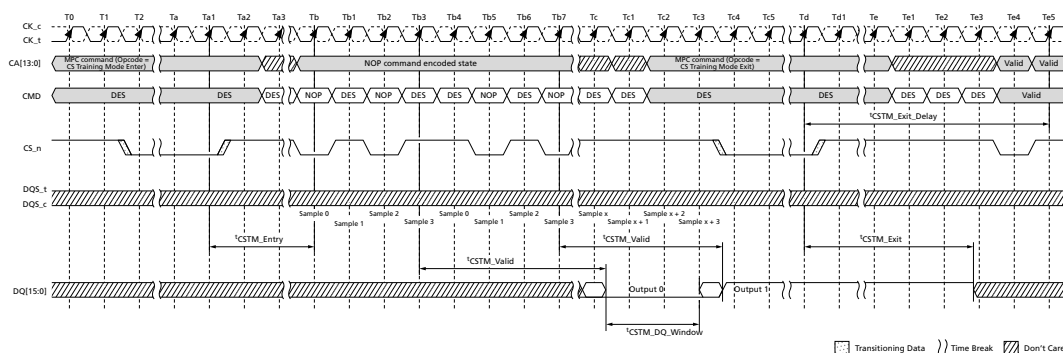
During CSTM, CA ODT is enabled as with a functional operation. The V_{refCS} is set according to the functional setting (using the VREFCS command). The delay from when the CS signals are sampled during the fourth CK rising edge (Sample[3]), to when the output of the sample evaluation is driven to a stable value on the DQ pins, is specified as $t^{\text{CSTM\_Valid}}$, as shown in the following figure. The details of the $t^{\text{CSTM\_entry}}$, $t^{\text{CSTM\_exit}}$, and $t^{\text{CSTM\_DQ\_Window}}$ are also illustrated.

Figure 104: Timing Diagram for CSTM with Consecutive Output Samples = 0



The following figure illustrates an example where the DQ output switches from a logic 0 to a logic 1, demonstrating the minimum $t^{\text{CSTM\_DQ\_Window}}$.

Figure 105: Timing Diagram for CSTM with Consecutive Output Sample Toggle



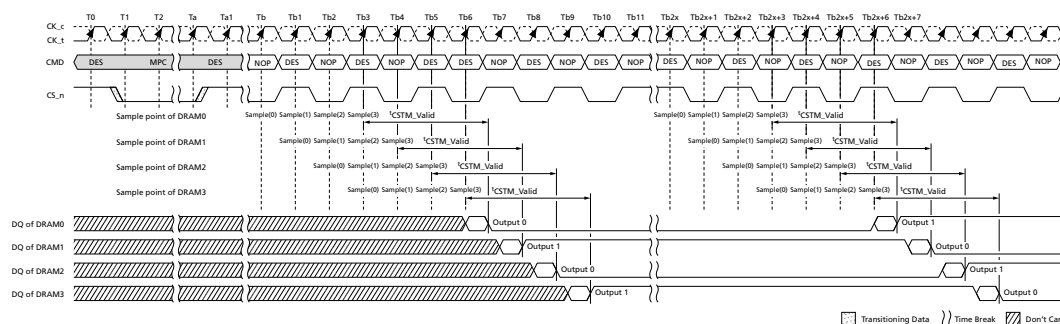
Notes: 1. See MPC Command for details on setup, hold and command register time.

- The CA bus must meet setup and hold times on any clock where it is possible that CS_n might be sampled LOW while in CS training mode.

When the host trains CS_n timing for the device by using CSTM, CS_n sampling timing for each DRAM could be different from each other because the variation of internal timing is different for each DRAM.

Therefore, even though the CS setup/hold time is appropriate for each DRAM, 4^tCK CS_n sampling window, which may have different starting points, could appear differently as shown in the following figure. The host should train CS_n timing based on asserting every edge of CS_n to cover multiple devices without exiting CSTM.

Figure 106: Timing Diagram for CSTM with Multiple DRAMs Output Sample Toggle



Note: 1. See MPC Command for details on setup, hold and command register time.

Output Signals

The following table shows which signals transmit the output of the CSTM loopback sample evaluation. These values are driven asynchronously, but may switch as often as every 4^tCK .

Table 212: CS Sampled Output per Interface Width

Output	x16	x8	x4
DQ0	CSTM Output	CSTM Output	CSTM Output
DQ1	CSTM Output	CSTM Output	CSTM Output
DQ2	CSTM Output	CSTM Output	CSTM Output
DQ3	CSTM Output	CSTM Output	CSTM Output
DQ4	CSTM Output	CSTM Output	
DQ5	CSTM Output	CSTM Output	
DQ6	CSTM Output	CSTM Output	
DQ7	CSTM Output	CSTM Output	
DML			
TDQS_c			
DQSL_t			
DQSL_c			
DQ8	CSTM Output		
DQ9	CSTM Output		
DQ10	CSTM Output		
DQ11	CSTM Output		
DQ12	CSTM Output		



Table 212: CS Sampled Output per Interface Width (Continued)

Output	x16	x8	x4
DQ13	CSTM Output		
DQ14	CSTM Output		
DQ15	CSTM Output		
DMU			
DQSU_t			
DQSU_c			

CA Training Mode

CA Training Mode (CATM) is a method to facilitate the loopback of a logical combination of sampled CA[13:0] signals.

In this mode, the CK is running and CS_n qualifies when the CK samples the CA signals. A loopback equation that includes all of the CA signals results in an output value that is sent asynchronously on the DQ signals back to the host memory controller. The host timings between CS_n, CK, and CA[13:0] signals can then be optimized for proper alignment. In this mode, no functional commands are executed in the device. The functional command interface is restored only after exiting this mode, which requires a CS_n assertion of two or more consecutive ^tCK. Prior to entering CATM, the CS_n signal must be aligned to the CK to meet the CS_n-to-CK timing specifications. This assumes CS training has been completed to determine the correct CS_n timings on the host, so the timing window for the CS to be met to ensure enough setup or hold timing margin prior to entering command/address training mode. Chip select training, through CSTM, can be used to accomplish this.

Entry and Exit

When CATM has completed successfully, CATM is entered by sending an MPC command with enter CA training mode op-code (OP[7:0] = 0000 0011b). Once this MPC command executes, no other commands are interpreted by the device. Only the sampling of the CA signals, evaluation of the XOR result, and loopback to the DQs occurs. While in CATM, the CS_n signal asserts only for a single ^tCK at a time. The maximum sampling rate on the CA signals is every 4^tCK. CATM is disabled by asserting CS_n for two or more cycles up to eight cycles in a row while sending a NOP command on the CA bus.

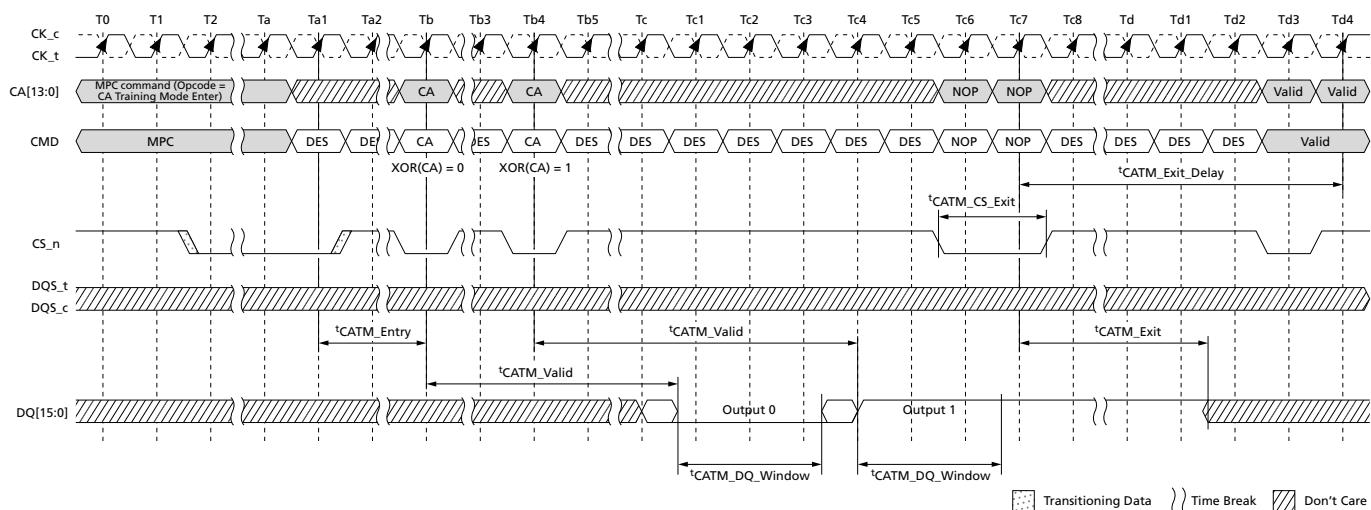
Operation

In CATM, the CA values are sampled in the same way as with functional operation, where the CS_n qualifies which cycle the sampling occurs and the sample is captured by the rising CK edge. Unlike functional operation, there is no concept of multiple cycle commands in CATM. Sampling of the CA signals occurs only when CS_n is asserted LOW. Once the CA signals are sampled, the values are XOR'd to produce an output value. This output value is driven on all the DQ pins, as a pseudo-static value. These output values are held until the next sample is captured on the CA bus, according to the CS_n assertion.

During CATM, the CA ODT is enabled as with a functional operation. The V_{refCA} is set according to the functional setting (through the VREFCA command). The timing requirements for the CA bus (CK_t, CK_c, and CS_n) are the same as with a functional operation.

The delay from when the CA signals are sampled during the CS_n assertion and when the output of the XOR computation is driven on the DQ pins is specified as ^tCATM_Valid, as shown in the following figure. CS_n must be asserted every 4^tCK, and thus, the CA XOR output may transition every 4^tCK. The following figure demonstrates an example where two CS_n assertions occur within 4^tCK. The device exits CATM when CS_n is asserted for two or more consecutive cycles, but limited to eight cycles.

Figure 107: CA Training Mode



CA Loopback Equation

CATM output is computed based on the CS_n assertion and the values of the CA inputs. The following table clarifies the output computation.

Table 213: CATM Output

CS _n	CATM Output	Notes
0	XOR(CA[13:0])	1
1	Hold previous value	

Note: 1. The XOR function occurs after mirroring/inversion recovery, and only includes signals supported on the device (that is, may not include CA[13], depending on density (including stacking). If CA[13] is not needed for the device's density, the logical value is considered 0 for the XOR computation, though as indicated in the pin description table for MIR, the ball location associated with CA13's logical input (which switches with CA12) will be connected to V_{DDQ}.

Output Equations

The following table shows which signals transmit the output of the CATM loopback equation. These values are driven asynchronously as pseudo-static values, updating with a new output at a time t_{CATM_Valid} after each CS_n assertion.

Table 214: Output Equations per Interface Width

Output	x16	x8	x4
DQ0	CATM Output	CATM Output	CATM Output
DQ1	CATM Output	CATM Output	CATM Output
DQ2	CATM Output	CATM Output	CATM Output
DQ3	CATM Output	CATM Output	CATM Output
DQ4	CATM Output	CATM Output	
DQ5	CATM Output	CATM Output	
DQ6	CATM Output	CATM Output	
DQ7	CATM Output	CATM Output	
DML			
TDQS _c			

Table 214: Output Equations per Interface Width (Continued)

Output	x16	x8	x4
DQSL_t			
DQSL_c			
DQ8	CATM Output		
DQ9	CATM Output		
DQ10	CATM Output		
DQ11	CATM Output		
DQ12	CATM Output		
DQ13	CATM Output		
DQ14	CATM Output		
DQ15	CATM Output		
DMU			
DQSU_t			
DQSU_c			

VREFCS Command

The V_{REFCS} voltage level should be set, if needed, prior to training the CS_n and CA bus timings relative to CK. The device supports a 1-cycle command, VREFCS, specifically for setting the internal V_{REFCS} voltage level. This avoids any timing and/or default V_{REFCS} setting issues when sending a 2-cycle MRW command, by enabling the host to extend the setup and hold time for the CA signals. The VREFCS command also supports multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensure the DRAM captures the VREFCS command during at least one rising edge of the differential CK (CK_t - CK_c).

NOTE: The operation, functionality and timings for VREFCS are effectively the same as VREFCA with the exception of the command name, and the fact that it modifies the internal reference voltage level of the chip select (CS_n) pin vs. the CA pins.

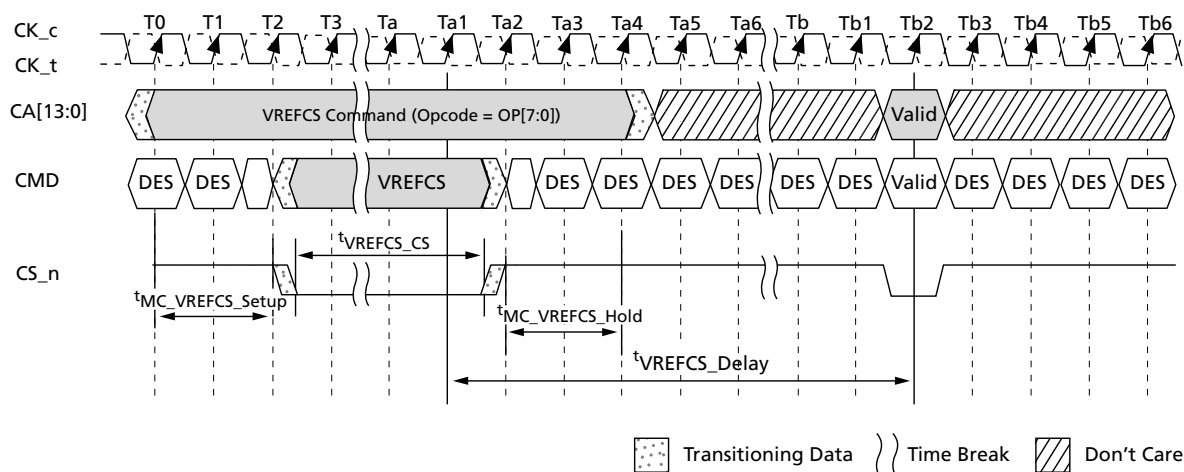
VREFCS Command Timing

The following diagram illustrates a timing sequence example for the VREFCS command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK.

The host must ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK transitions, but it will satisfy the setup/hold requirements relative to at least one rising edge of CK.

Multicycle CS assertion is enabled or disabled by programming the mode register MR2:OP[4] bit. This timing relationship can always be used by the host to send the VREFCS commands even after training has been completed for the interface. To latch the VREFCS command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state at least three cycles prior to CS_n transitioning from HIGH to LOW, CS_n must remain LOW for $t_{\text{VREFCS\_CS}}$, and CA must remain in the proper command state for at least three cycles after CS_n transitions from LOW to HIGH.

Figure 108: VREFCS Command Timing



VREFCA Command

The V_{REFCA} voltage level must be set prior to training the CS_n and CA bus timings relative to CK. The device supports a 1-cycle command, VREFCA, specifically for setting the internal V_{REFCA} voltage level. This avoids any timing and/or default V_{REFCA} setting issues when sending a 2-cycle MRW command, by enabling the host to extend the setup and hold time for the CA signals. The VREFCA command also supports multiple cycles of CS_n assertion. The multiple cycles of CS_n assertion ensures the device captures the VREFCA command during at least one rising edge of the differential CK (CK_t - CK_c).

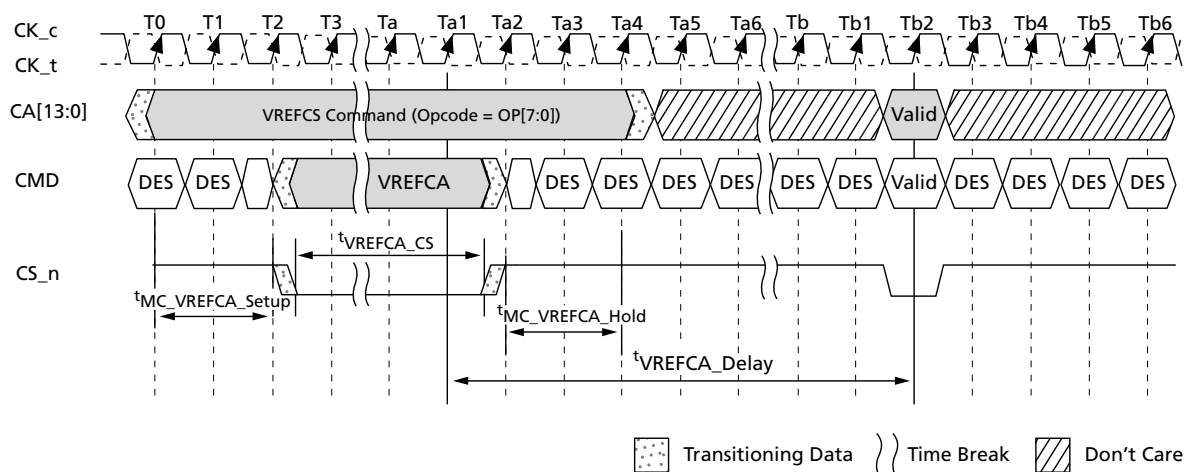
VREFCA Command Timing

The figure below illustrates a timing sequence example for the VREFCA command that occurs prior to CS and CA training. The command is sampled on every rising edge of CK.

The host must ensure that the CA signals are valid during the entire CS_n assertion time. The timing of the CS_n assertion may not satisfy the setup/hold requirements around all CK transitions, but it will satisfy the setup/hold requirements relative to at least one rising edge of CK.

Multicycle CS assertion is enabled or disabled by programming the mode register MR2:OP[4] bit. This timing relationship can always be used by the host to send the VREFCA commands even after training has been completed for the interface. To latch the VREFCA command in cases where the alignment between CS_n, CA, and CK may be unknown, the CA inputs must reach the proper command state at least three cycles prior to CS_n transitioning from HIGH to LOW, CS_n must remain LOW for t_{VREFCA_CS} , and CA must remain in the proper command state for at least three cycles after CS_n transitions from LOW to HIGH.

Figure 109: VREFCA Command Timing

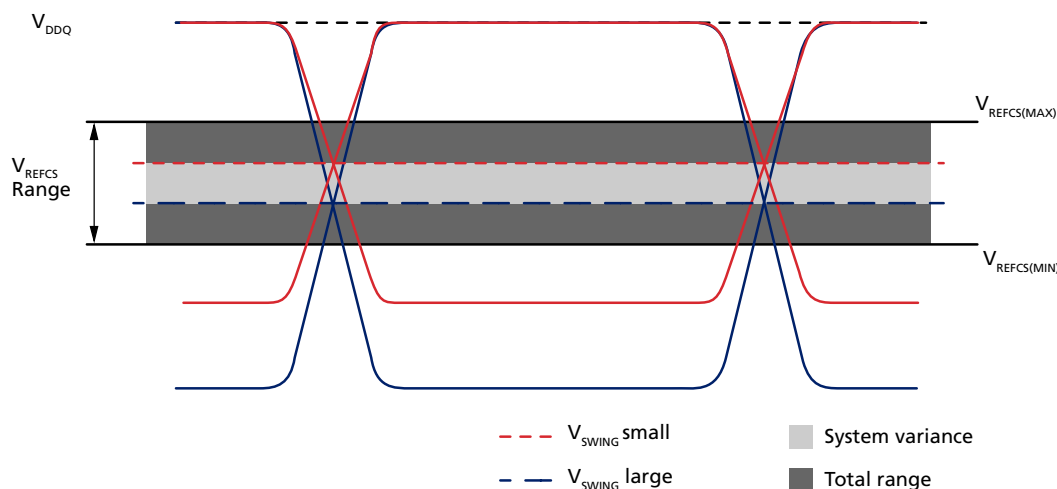


VREFCS Training

The internal V_{REFCS} specification parameters include operating voltage range, step size, step tolerance, step time, and valid voltage levels.

The operating voltage range specifies the minimum required V_{REFCS} setting ranges. These minimum setting ranges are defined by $V_{\text{REFCS(MIN)}}$ to $V_{\text{REFCS(MAX)}}$ as depicted in the following figure.

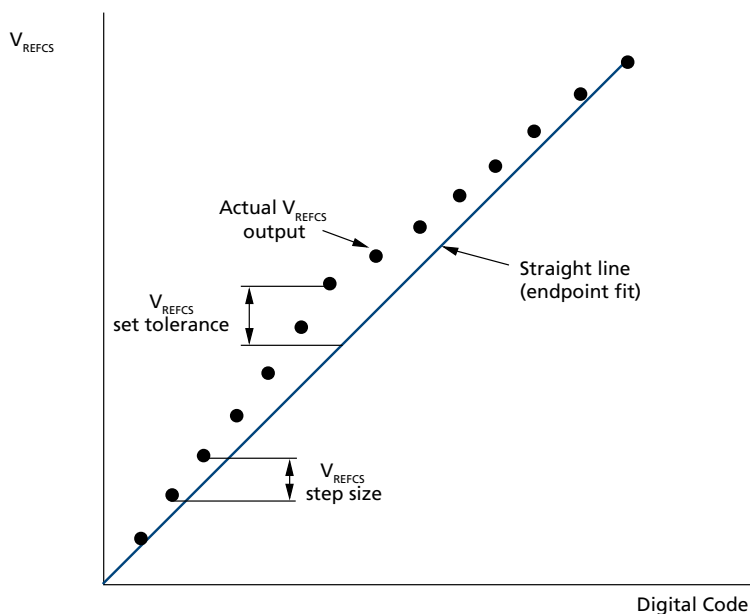
Figure 110: V_{REFCS} Operating Ranges



The step size is defined as the size between adjacent steps. For a given design, the DRAM V_{REFCS} step sizes must be within the specified range.

The set tolerance is the variation in the V_{REFCS} voltage levels from the ideal settings. This accounts for accumulated error over multiple steps. There are two ranges for set tolerance uncertainty. The range of set tolerance uncertainty is a function of number of steps n . The set tolerance is measured with respect to the ideal line, which is based on the two endpoints, $V_{\text{REFCS(MIN)}}$ / $V_{\text{REFCS(MAX)}}$, for the specified ranges.

Figure 111: V_{REFCS} Set Tolerance and Step Size Example – MAX Case



The increment/decrement step times are defined by $V_{\text{REFCS\_time}}$, which is defined from t_0 to t_1 (shown below), where t_1 is referenced to when the V_{REFCS} voltage is at the final DC level within the V_{REFCS} valid tolerance ($V_{\text{REFCS\_val\_tol}}$).

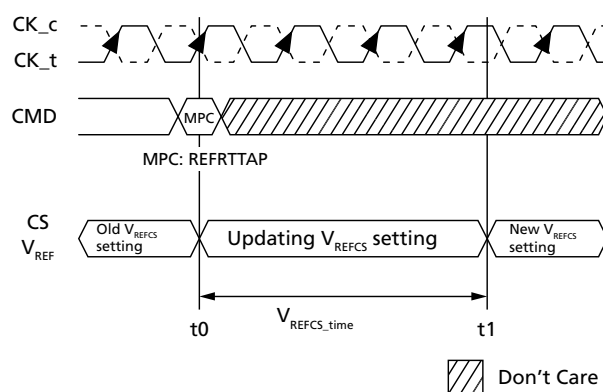
The V_{REFCS} valid level is defined by the valid tolerances to qualify the step time t_1 , as shown in the following figures. This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REFCS} increment or decrement adjustment, and are only applicable for DRAM component-level validation/characterization.

V_{REFCS} time is the time including up to $V_{\text{REFCS, min}}$ to $V_{\text{REFCS, max}}$ or $V_{\text{REFCS, max}}$ to $V_{\text{REFCS, min}}$ change in V_{REFCS} voltage.

t_0 is referenced to MPC APPLY VREFCS and RTT_CA/CS/CK commands.

t_1 is referenced to $V_{\text{REFCS\_val\_tol}}$.

Figure 112: $V_{\text{REFCS\_time}}$ Timing



A VREFCS command is used to store the V_{REF} values into the V_{REFCS} mode register (MR12). This mode register is only programmed via the command but is readable via a normal MRR.

Figure 113: V_{REFCS} Step, Single Step Size Increment Example

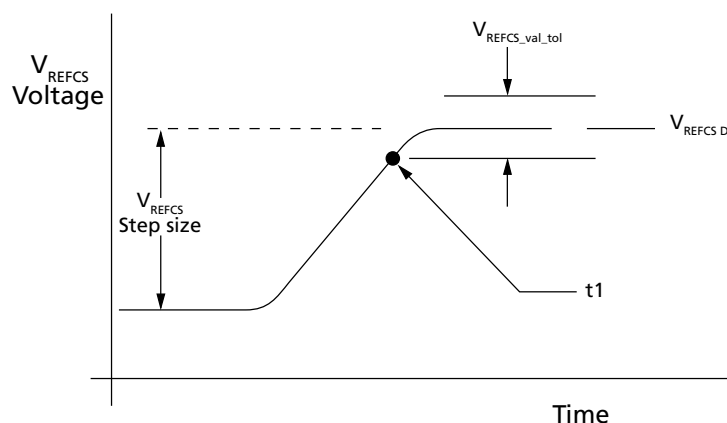


Figure 114: V_{REFCS} Step, Single Step Size Decrement Example

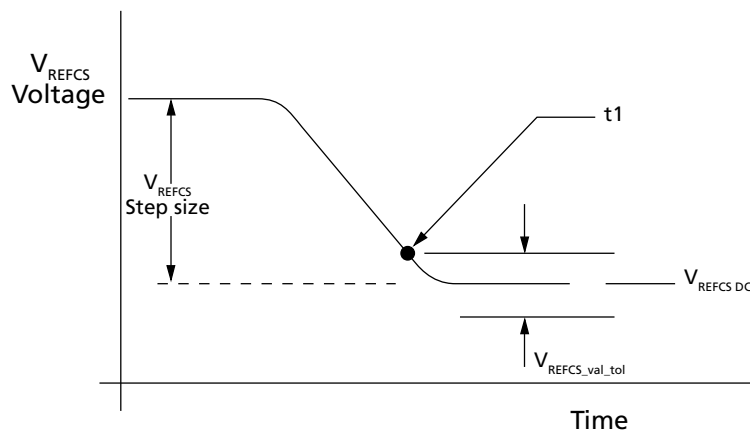


Figure 115: V_{REFCS} Full Step from $V_{\text{REFCS(MIN)}}$ to $V_{\text{REFCS(MAX)}}$ Example

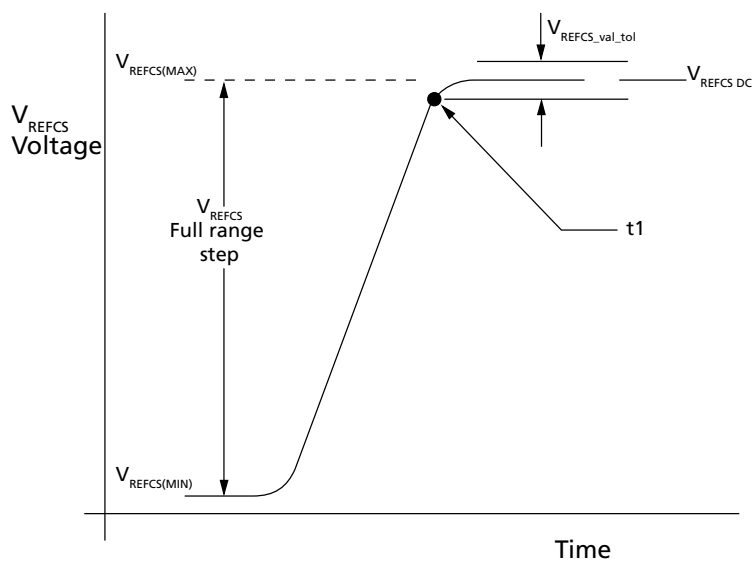


Figure 116: V_{REFCS} Full Step from $V_{\text{REFCS(MIN)}}$ to $V_{\text{REFCS(MAX)}}$ Example

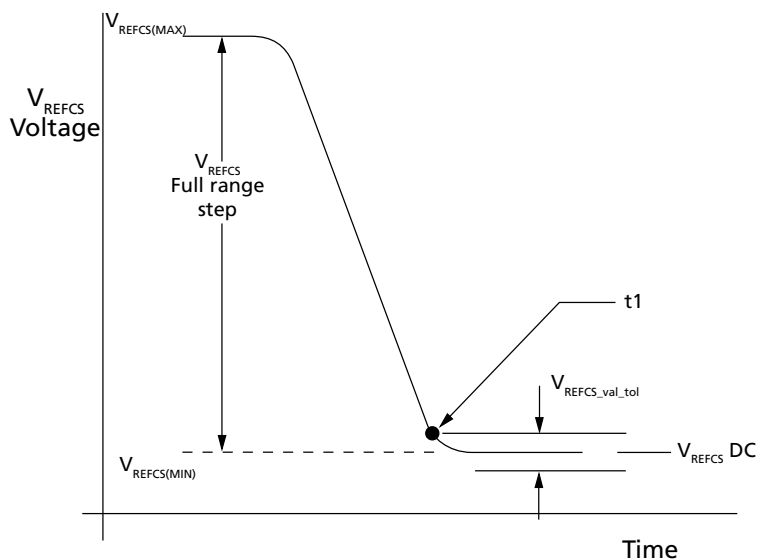


Table 215: Internal V_{REFCS} Specifications

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
$V_{\text{REFCS(MAX)}}$ operating point	$V_{\text{REFCS(MAX)}}$	97.5%	–	–	V_{DDQ}	1
$V_{\text{REFCS(MIN)}}$ operating point	$V_{\text{REFCS(MIN)}}$	–	–	35%	V_{DDQ}	1
V_{REFCS} step size	$V_{\text{REFCS\_step}}$	0.41%	0.50%	0.59%	V_{DDQ}	2
V_{REFCS} set tolerance	$V_{\text{REFCS\_set\_tol}}$	–1.625%	0.00%	1.625%	V_{DDQ}	3, 4, 6
		–0.15%	0.00%	0.15%	V_{DDQ}	3, 5, 7
V_{REFCS} step time	$V_{\text{REFCS\_time}}$	–	–	300	ns	8
V_{REFCS} valid tolerance	$V_{\text{REFCS\_val\_tol}}$	–0.15%	0.00%	0.15%	V_{DDQ}	9

Notes: 1. V_{REFCS} DC voltage reference to V_{DDQ} DC.

2. V_{REFCS} step size increment/decrement range. V_{REFCS} at DC level.

3. $V_{\text{REFCS\_new-setting}} = V_{\text{REFCS\_old-setting}} \pm n * V_{\text{REFCS\_step}}$; n = number of steps; if increment use +; if decrement use -.

4. The minimum value of V_{REFCS} setting tolerance = $V_{\text{REFCS\_new-setting}} - 1.625\% * V_{\text{DDQ}}$. The maximum value of V_{REFCS} setting tolerance = $V_{\text{REFCS\_new-setting}} + 1.625\% * V_{\text{DDQ}}$ for $n > 4$.

5. The minimum value of V_{REFCS} setting tolerance = $V_{\text{REFCS\_new-setting}} - 0.15\% * V_{\text{DDQ}}$. The maximum value of V_{REFCS} setting tolerance = $V_{\text{REFCS\_new-setting}} + 0.15\% * V_{\text{DDQ}}$ for $n \leq 4$.

6. Measured by recording the minimum and maximum values of the V_{REFCS} output over the range, drawing a straight line between those points and comparing all other V_{REFCS} output settings to that line.

7. Measured by recording the minimum and maximum values of the V_{REFCS} output across four consecutive steps ($n = 4$), drawing a straight line between those points and comparing all other V_{REFCS} output settings to that line.

8. Time from MPC command with Apply VREFCS and RTT_CA/CS/CK opcodes to increment or decrement.

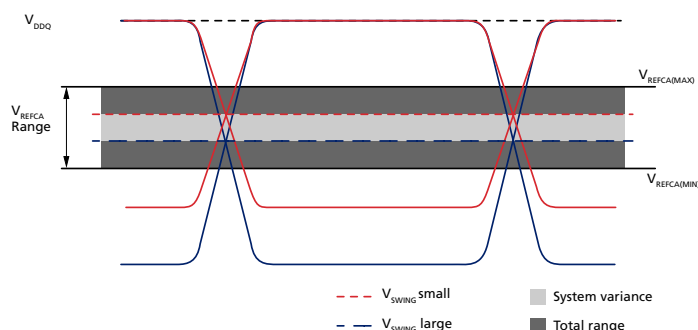
9. Only applicable for DRAM component-level test/characterization purpose. Not applicable for normal mode of operation. V_{REFCS} valid is to qualify the step times which will be characterized at the component level.

VREFCA Training

The internal V_{REFCA} specification parameters include operating voltage range, step size, step tolerance, step time, and valid voltage levels.

The operating voltage range specifies the minimum required V_{REFCA} setting range. These minimum setting ranges are defined by $V_{\text{REFCA,min}}$ to $V_{\text{REFCA,max}}$, as depicted in the following figure.

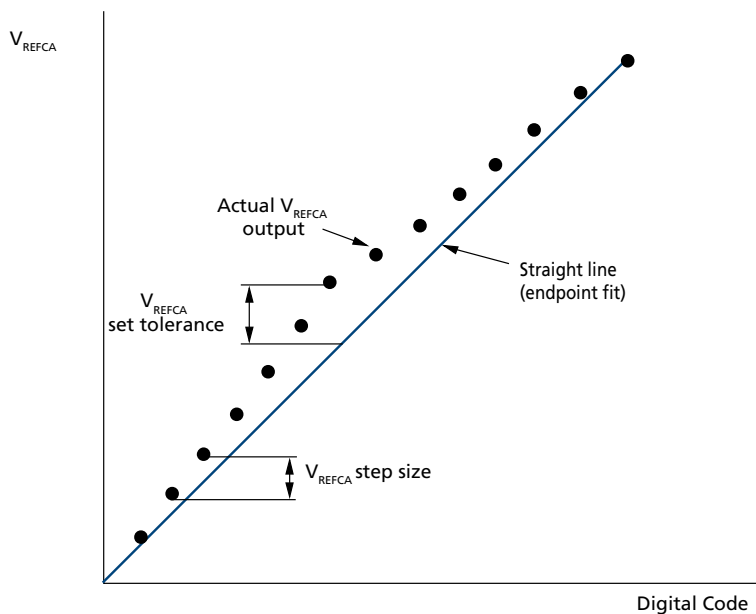
Figure 117: V_{REFCA} Operating Ranges



The step size is defined as the size between adjacent steps. For a given design, the DRAM V_{REFCA} step size must be within the specified range.

The set tolerance is the variation in the V_{REFCA} voltage levels from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for set tolerance uncertainty. The range of set tolerance uncertainty is a function of number of steps n . The set tolerance is measured with respect to the ideal line, which is based on the two endpoints, $V_{\text{REFCA,min}}$ and $V_{\text{REFCA,max}}$, for the specified ranges.

Figure 118: V_{REFCA} Set Tolerance and Step Size Example – MAX Case



The increment/decrement step times are defined by $V_{\text{REFCA,time}}$, which are defined from t_0 to t_1 (shown below), where t_1 is referenced to when the V_{REFCA} voltage is at the final DC level within the V_{REFCA} valid tolerance ($V_{\text{REFCA_val_tol}}$).

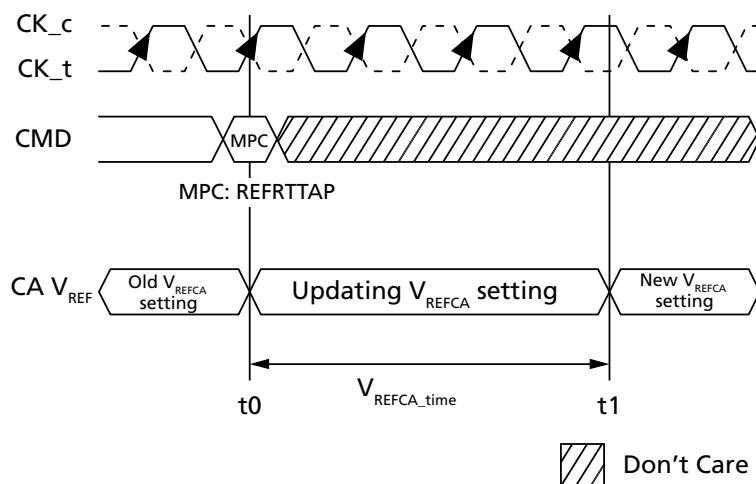
The valid level is defined by the valid tolerances to qualify the step time t_1 , as shown in the following figures. This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REFCA} increment or decrement adjustment, and are only applicable for DRAM component-level validation/characterization.

V_{REFCA} time is the time including up to $V_{REFCA,min}$ to $V_{REFCA,max}$ or $V_{REFCA,max}$ to $V_{REFCA,min}$ change in V_{REFCA} voltage.

t_0 is referenced to MPC APPLY VREFCA and RTT_CA/CS/CK commands.

t_1 is referenced to $V_{REFCA\_val\_tol}$.

Figure 119: V_{REFCA_time} Timing



A VREFCA command is used to store the V_{REF} value into the V_{REFCA} mode register, MR11. This mode register is only programmed via the command but is readable via a normal MRR.

Figure 120: V_{REFCA} Step, Single Step Size Increment Example

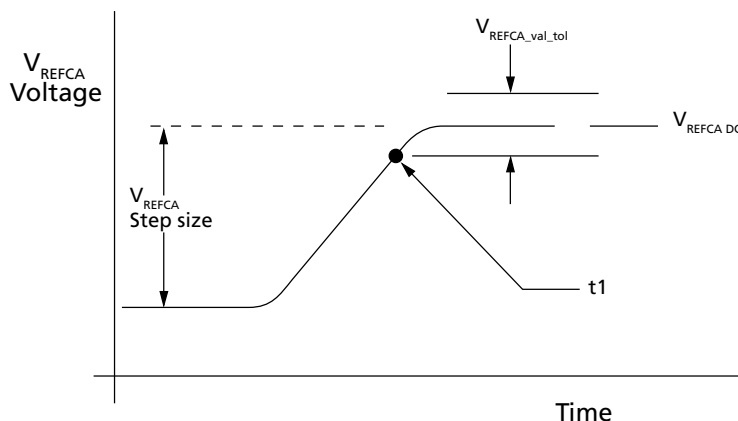


Figure 121: V_{REFCA} Step, Single Step Size Decrement Example

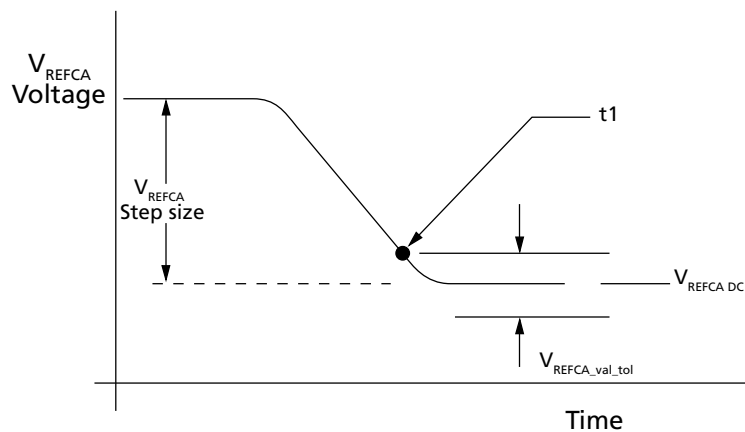


Figure 122: V_{REFCA} Full Step from $V_{\text{REFCA(MIN)}}$ to $V_{\text{REFCA(MAX)}}$ Example

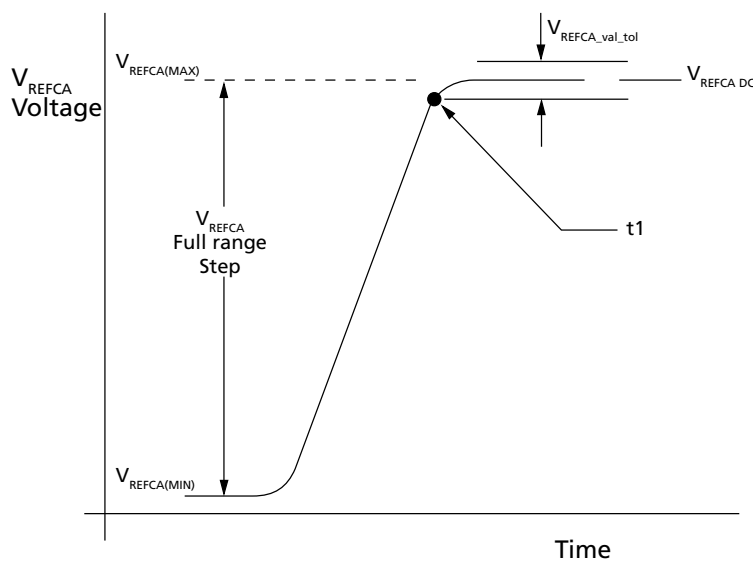


Figure 123: V_{REFCA} Full Step from $V_{\text{REFCA(MIN)}}$ to $V_{\text{REFCA(MAX)}}$ Example

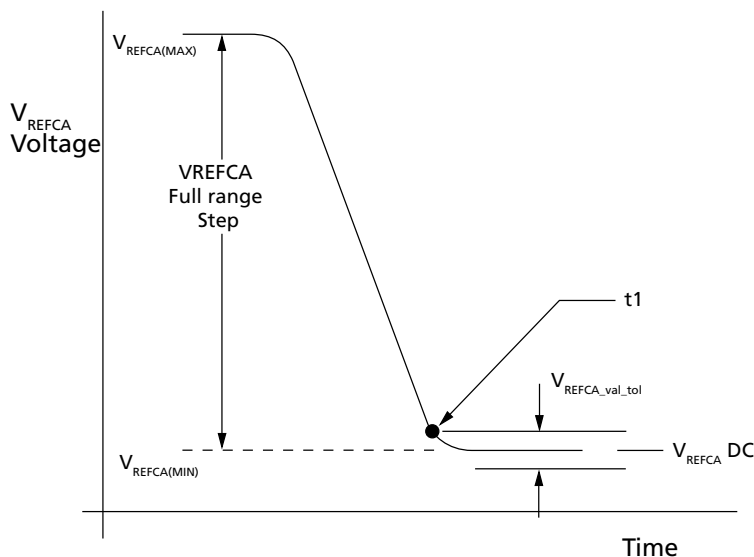


Table 216: Internal V_{REFCA} Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
$V_{\text{REFCA,max}}$ operating point	$V_{\text{REFCA,max}}$	97.5%	–	–	V_{DDQ}	1
$V_{\text{REFCA,min}}$ operating point	$V_{\text{REFCA,min}}$	–	–	35%	V_{DDQ}	1
V_{REFCA} step size	$V_{\text{REFCA,step}}$	0.41%	0.50%	0.59%	V_{DDQ}	2
V_{REFCA} set tolerance	$V_{\text{REFCA,set\_tol}}$	–1.625%	0.00%	1.625%	V_{DDQ}	3, 4, 6
		–0.15%	0.00%	0.15%	V_{DDQ}	3, 5, 7
V_{REFCA} step time	$V_{\text{REFCA,time}}$	–	–	300	ns	8
V_{REFCA} valid tolerance	$V_{\text{REFCA,val\_tol}}$	–0.15%	0.00%	0.15%	V_{DDQ}	9

Notes: 1. V_{REFCA} DC voltage reference to V_{DDQ} DC.

2. V_{REFCA} step size increment/decrement range. V_{REFCA} at DC level.

3. $V_{\text{REFCA\_new-setting}} = V_{\text{REFCA\_old-setting}} + n * V_{\text{REFCA\_step}}$; n = number of steps; if increment use +; if decrement use –.

4. The minimum value of V_{REFCA} setting tolerance = $V_{\text{REFCA\_new-setting}} - 1.625\% * V_{\text{DDQ}}$. The maximum value of V_{REFCA} setting tolerance = $V_{\text{REFCA\_new-setting}} + 1.625\% * V_{\text{DDQ}}$ for $n > 4$.

5. The minimum value of V_{REFCA} setting tolerance = $V_{\text{REFCA\_new-setting}} - 0.15\% * V_{\text{DDQ}}$. The maximum value of V_{REFCA} setting tolerance = $V_{\text{REFCA\_new-setting}} + 0.15\% * V_{\text{DDQ}}$ for $n \leq 4$.

6. Measured by recording the minimum and maximum values of the V_{REFCA} output over the range, drawing a straight line between those points and comparing all other V_{REFCA} output settings to that line.

7. Measured by recording the minimum and maximum values of the V_{REFCA} output across four consecutive steps ($n = 4$), drawing a straight line between those points and comparing all other V_{REFCA} output settings to that line.

8. Time from MPC command with Apply VrefCA and RTT_CA/CS/CK opcode to increment or decrement and voltage settling to within $V_{\text{REFCA\_val\_tol}}$ of the target level.

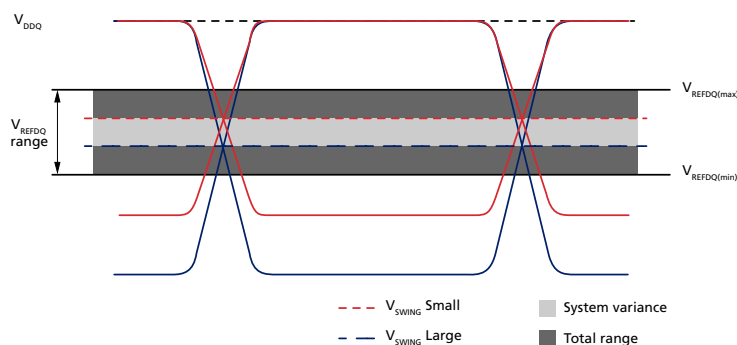
9. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REFCA} valid is to qualify the step times which will be characterized at the component level.

VREFDQ Training

The internal V_{REFDQ} specification parameters are operating voltage range, V_{REFDQ} step size, V_{REFDQ} step tolerance, V_{REFDQ} step time, and V_{REF} full step time, and V_{REFDQ} valid voltage level.

The voltage operating range specifies the minimum required V_{REFDQ} setting range. The minimum range is defined by $V_{\text{REFDQ,max}}$ and $V_{\text{REFDQ,min}}$.

Figure 124: V_{REFDQ} Operating Range – $V_{\text{REFDQ,min}}$ $V_{\text{REFDQ,max}}$

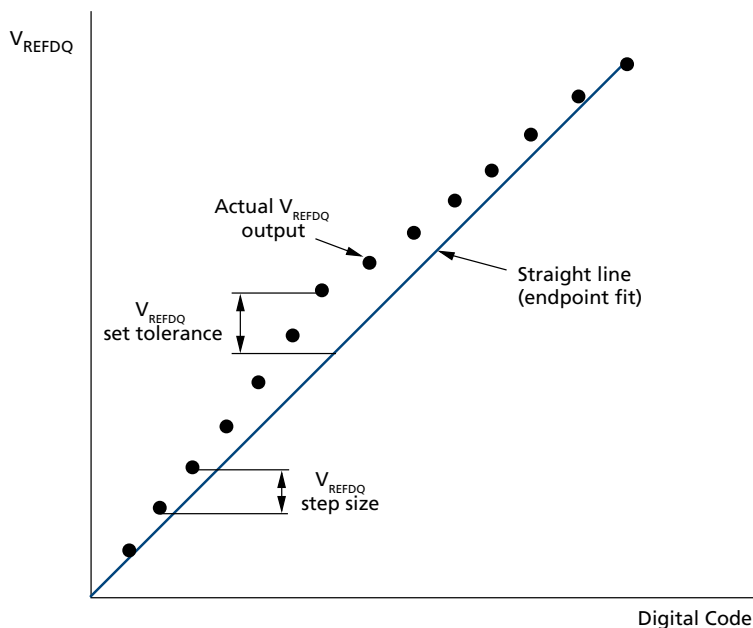


The V_{REFDQ} step size ($V_{\text{REFDQ\_step}}$) is defined as the step size between adjacent steps. For a given design, the V_{REFDQ} step size must be within the range specified.

The V_{REFDQ} set tolerance ($V_{\text{REFDQ\_set\_tol}}$) is the variation in the V_{REFDQ} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REFDQ} set tolerance uncertainty. The range of V_{REFDQ} set tolerance uncertainty is a function of number of steps n .

The V_{REFDQ} set tolerance is measured with respect to the ideal line, which is based on the two endpoints, with the endpoints at MIN and MAX V_{REFDQ} values for a specified range.

Figure 125: V_{REFDQ} Set Tolerance and Step Size – MAX Case



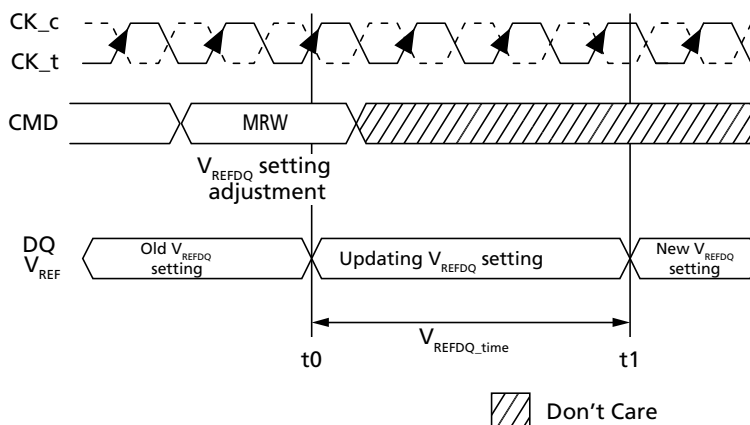
The V_{REFDQ} increment/decrement step times are defined by $V_{\text{REFDQ\_time}}$. $V_{\text{REFDQ\_time}}$, which is defined from t_0 to t_1 (shown below), where t_0 is at the MRW to MR10 (to adjust V_{REFDQ}) and t_1 is where the V_{REFDQ} voltage is at the final DC level within the valid tolerance ($V_{\text{REFDQ\_val\_tol}}$).

The V_{REFDQ} valid level is defined by $V_{\text{REFDQ\_val\_tol}}$ to qualify the step time t_1 , as shown in the following figures. This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REFDQ} increment or decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

t_0 - is referenced to the MRW command which updates the V_{REFDQ} values.

t_1 - is referenced to the $V_{\text{REFDQ\_val\_tol}}$.

Figure 126: $V_{\text{REFDQ\_time}}$ Timing



- Notes:
1. The minimum time required between two MRW commands which update V_{REFDQ} settings is $V_{\text{REFDQ\_time}}$.
 2. An MRW command is used to store the global V_{REFDQ} values into the V_{REFDQ} bits of MR10.
 3. Additional per-pin V_{REFDQ} trims are available for programming in MR118, MR126, MR134, ... MR254, OP[7:4], up to a maximum of ± 3 V_{REFDQ} steps. The combined global and per-pin V_{REFDQ} settings never exceed the available V_{REFDQ} range from 35.0% to 97.5%.

Figure 127: V_{REFDQ} Step, Single Step Size Increment Example

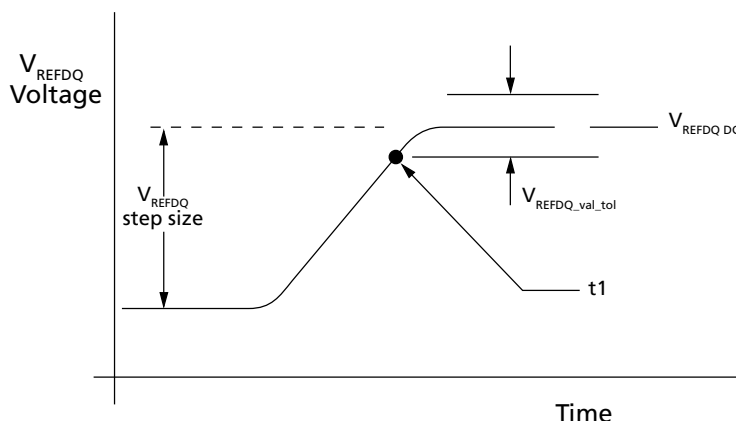


Figure 128: V_{REFDQ} Step, Single Step Size Decrement Example

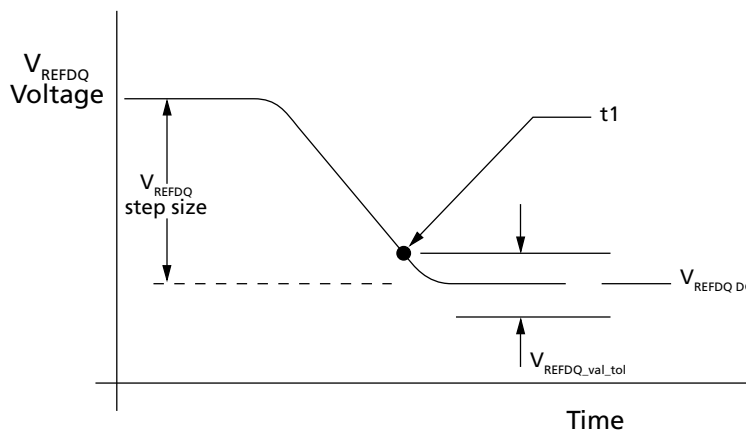


Figure 129: V_{REFDQ} Full Step from $V_{\text{REFDQ(MIN)}}$ to $V_{\text{REFDQ(MAX)}}$ Example

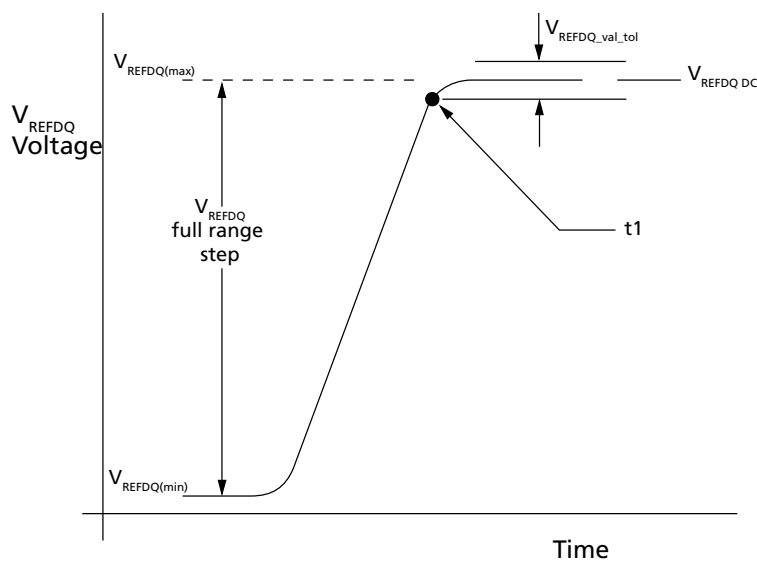


Figure 130: V_{REFDQ} Full Step from $V_{\text{REFDQ(MAX)}}$ to $V_{\text{REFDQ(MIN)}}$ Example

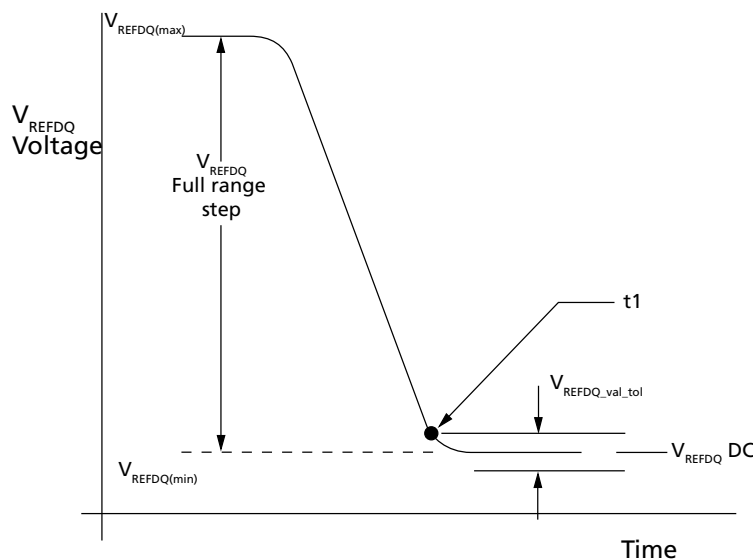


Table 217: Internal V_{REFDQ} Specifications

Parameter	Symbol	MIN	TYP	MAX	Unit	Notes
$V_{\text{REFDQ,max}}$ operating point	$V_{\text{REFDQ,max}}$	97.5%	–	–	V_{DDQ}	1
$V_{\text{REFDQ,min}}$ operating point	$V_{\text{REFDQ,min}}$	–	–	35%	V_{DDQ}	1
V_{REFDQ} step size	$V_{\text{REFDQ\_step}}$	0.41%	0.50%	0.59%	V_{DDQ}	2
V_{REFDQ} set tolerance	$V_{\text{REFDQ\_set\_tol}}$	–1.625%	0.00%	1.625%	V_{DDQ}	3, 4, 6
		–0.15%	0.00%	0.15%	V_{DDQ}	3, 5, 7
V_{REFDQ} step time	$V_{\text{REFDQ\_time}}$	–	–	150	ns	8, 10
		–	–	500		
V_{REFDQ} valid tolerance	$V_{\text{REFDQ\_val\_tol}}$	–0.15%	0.00%	0.15%	V_{DDQ}	9

Notes: 1. V_{REFDQ} DC voltage referenced to V_{DDQDC} .

2. V_{REFDQ} step size increment/decrement range: V_{REFDQ} at DC level.

3. $V_{\text{REFDQ}}(\text{new}) = V_{\text{REFDQ}}(\text{old}) + n * V_{\text{REFDQ\_step}}$; n = number of step; if increment, use +; if decrement, use –.

4. The minimum value of V_{REFDQ} setting tolerance = $V_{\text{REFDQ}}(\text{new}) - 1.625\% * V_{\text{DDQ}}$. The maximum value of V_{REFDQ} setting tolerance = $V_{\text{REFDQ}}(\text{new}) + 1.625\% * V_{\text{DDQ}}$ for $n > 4$.

5. The minimum value of V_{REF} setting tolerance = $V_{\text{REFDQ}}(\text{new}) - 0.15\% * V_{\text{DDQ}}$. The maximum value of V_{REFDQ} setting tolerance = $V_{\text{REFDQ}}(\text{new}) + 0.15\% * V_{\text{DDQ}}$ for $n < 4$.

6. Measured by recording the minimum and maximum values of the V_{REFDQ} output over the range, drawing a straight line between those points and comparing all other V_{REFDQ} output settings to that line.

7. Measured by recording the minimum and maximum values of the V_{REFDQ} output across four consecutive steps ($n = 4$), drawing a straight line between those points and comparing all other V_{REFDQ} output settings to that line.

8. Time from MRW command updating V_{REFDQ} command to increment or decrement and voltage settling to within $V_{\text{REFDQ\_val\_tol}}$ of the target level.

9. Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. V_{REFDQ} valid is to qualify the step times which will be characterized at the component level.

10. The maximum value of V_{REFDQ} step time = 150ns for $n < 16$ and 500ns for $n \geq 16$, where n = number of steps.

Write Leveling (WL) Training Mode

The DDR5 memory modules use a fly-by topology for commands, addresses, control signals, and clocks. Fly-by topology benefits include reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the memory controller to set the timings of the WRITE DQS signaling according to the write latency timing specification at the device. Therefore, the device supports a write leveling feature that enables the controller to compensate for channel skew. Write leveling training also enables for an unmatched path between CK and DQS within the DRAM, supporting an internal write leveling training flow to account for the difference in internal delays.

The device also provides a programmable timing in its write logic, controlled by the write leveling internal cycle alignment (WICA) mode register (MR3), which provides a means for improved performance of the device receivers. The proper setting of this register must be determined by the memory controller, either as described in the sections that follow, or by another means derived through engineering analysis. This delay setting is specific to each device, its write preamble setting, and the operating frequency being used. PDA select ID is allowed while in WL training mode to program settings specific to each device. After the proper delay settings have been determined for a given device byte, write preamble setting and operating frequency, these settings may be restored to the device after reset, power cycle, or return to a previously used operating frequency.

The memory controller can use the write leveling feature and feedback from the device to adjust the controller's differential DQS (DQS_t - DQS_c) output delay to align to the phase and cycle that corresponds to the CAS write latency (CWL) delay after the WRITE command. The memory controller involved in the leveling must have an adjustable delay setting on the DQS to align the rising edge of differential DQS with the timing at the receiver that is the pin-level write latency (external write leveling training), and to align DQS with the internal DRAM write latency timing point (write leveling internal cycle alignment training). The internal DRAM write latency timing point may be skewed from the pin-level write latency timing point. The host will minimize this skew (DQSoffset) through the write leveling training flow.

Because the system and DIMM delays vary, the device supports the ability for the host to align the DQS timings with a pin-level write latency differential CK (CK_t - CK_c) edge. This alignment is referred to as external write leveling. After the DQS host timings are aligned at the DRAM write latency timing, the internal DRAM timings are optimized for lowest power and internal delay. This is accomplished when the host enables the internal write timing setting in MR2. To compensate for the difference in delay, the host will execute an internal write leveling training sequence, which includes sweeping the write leveling internal cycle (WICA) settings in MR3 (write leveling internal cycle alignment operation) and then finalize the differential DQS phase and offset (write leveling internal phase alignment and final host DQS timing operation).

During write leveling training (both external and internal), the DQS pattern must include the full programmed write preamble and only the first toggle of the normal data burst sequence. The device samples the internal write leveling pulse relative to the first DQS toggle of the data burst sequence (last rising differential DQS edge sent by the host) and asynchronously feeds back the result of this sample on the DQ bus, transitioning between ^tWLO (MIN) and ^tWLO (MAX). If the DQ bus output is LOW at ^tWLO (MAX), the internal write leveling pulse signal is sampled while it is deasserted (LOW). Likewise, if the DQ burst output is HIGH at ^tWLO (MAX), the internal write leveling pulse signal is sampled while it is asserted (HIGH).

The sampled feedback state remains on the DQ bus until a subsequent write leveling sample changes the state, or until write leveling training is exited.

The internal write leveling pulse is generated in response to a WRITE command, and held statically LOW otherwise. To perform the write leveling training, the controller repeatedly sends a WRITE

command, delays DQS, and monitors the DQ feedback after t_{WLO} (MAX) until a transition from 0 to 1 is detected, indicating alignment with the internal write leveling pulse.

During internal write leveling training flows, the host will apply an offset to the starting point or the final setting of the DQS signals. The offsets are referred to as WL_ADJ_start and WL_ADJ_end. This will minimize the t_{DQSO} offset variation across different DRAM devices. The WL_ADJ_start and WL_ADJ_end values depend on the t_{WPRE} setting.

When external and internal write leveling training flows are complete and the final WL_ADJ_end offset has been applied to the DQS timings, DQS is phase-aligned and cycle-aligned for write operations. During the training sequence, the DRAM in write leveling training mode will apply ODT to the strobes in the same way as for functional operation.

All non-target ranks (which will not be in write leveling training mode) will apply ODT as defined for functional operation. Prior to executing the write leveling training flow, t_{WPRE} value must be configured to the functional operation setting.

Note: DQS ODT is based on a DQS PARK mode and is not enabled and disabled with DQ ODT timings.

Write Leveling Mode Registers

The MR fields for write leveling training, internal write timing, and write leveling internal cycle alignment are part of MR2 and MR3 (optionally MR7 as well).

To enter write leveling training mode, the controller programs MR2:OP[1] = 1. To exit the write leveling training mode, program MR2:OP[1] = 0. Write leveling internal cycle alignment offers two nibbles to control the upper and lower DQ bytes. The lower byte write leveling internal cycle alignment is intended for x4, x8, and x16 configurations, while the upper byte is only for x16 configurations.

The internal write timing, enabled by (MR2:OP[7]=1), remains enabled through the internal write leveling training flow and for functional operation. The host is responsible for incrementing the write leveling internal cycle alignment setting until the internal write leveling pulse is pulled early enough to align with the differential DQS signal which was previously aligned with the pin-level write latency timing. The write leveling internal cycle alignment setting only applies when the internal write timing is enabled.

Only BL16 mode is supported in write leveling training mode. DM and TDQS shall be disabled by the host (if previously enabled) by setting MR5:OP[5]=0 and MR5:OP[4]=0, respectively, prior to executing write leveling training mode.

External Write Leveling Training Operation

When write leveling mode is enabled (MR2:OP[1]=1) and the internal write timing is disabled (MR2:OP[7]=0), the device will have an internal write leveling pulse that indicates how the DQS signals align to match the pin-level write latency timings. The rising edge of the internal write leveling pulse will align to the rising edge of the differential CK signal that coincides with CAS write latency (CWL), as shown in the following diagrams.

The differential DQS signals driven by the controller during leveling mode must be terminated by the DRAM devices based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations x4, x8, and x16. On a x16 device, both byte lanes are leveled independently. Therefore, a separate feedback mechanism shall be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS (diff_UDQS) to internal write leveling pulse relationship, whereas the lower data bits would indicate the lower diff_DQS (diff_LDQS) to internal write leveling pulse relationship. When training a x16 device, the data bits of a byte remain in the don't care state until its applicable DQS

signals are toggled. Once the DQS signals are toggled, the DQs follow the behavior previously described.

The following diagram shows the timing sequence to enter write leveling training mode, how the operation works during write leveling training mode (with internal write timing disabled), and the timing sequence to exit write leveling training mode. An MRW command is sent to enable write leveling training mode. Prior to sending the MRW command to enable write leveling training mode, the host memory controller must drive the DQS signals differentially LOW. After t_{WLPEN} time, the controller can send a WRITE command, followed by strobe pulses. The DQS signals always drive differentially LOW, except during the preamble and burst strobe sequence. There is no restriction as to how early the strobe pulses are sent, so long as they are no earlier than $CWL/2$ after the WRITE command. The device samples the internal write leveling pulse relative to the first DQS toggle of the data burst sequence and asynchronously feeds back the result of this sample on the DQ bus, transitioning between t_{WLO} (MIN) and t_{WLO} (MAX).

While in write leveling training mode, the host controller may send ACT and PRE commands. The DRAM will ignore these commands, and the addresses associated with these ACT and the WRITE commands may be any value. The following timing diagrams demonstrate the timing requirements associated with write leveling training mode entry, the internal write leveling pulse alignment during external write leveling training, and the DQ sample feedback timing.

Figure 131: Write Leveling Training Mode (External Training, 2N Mode, 0 Sample)

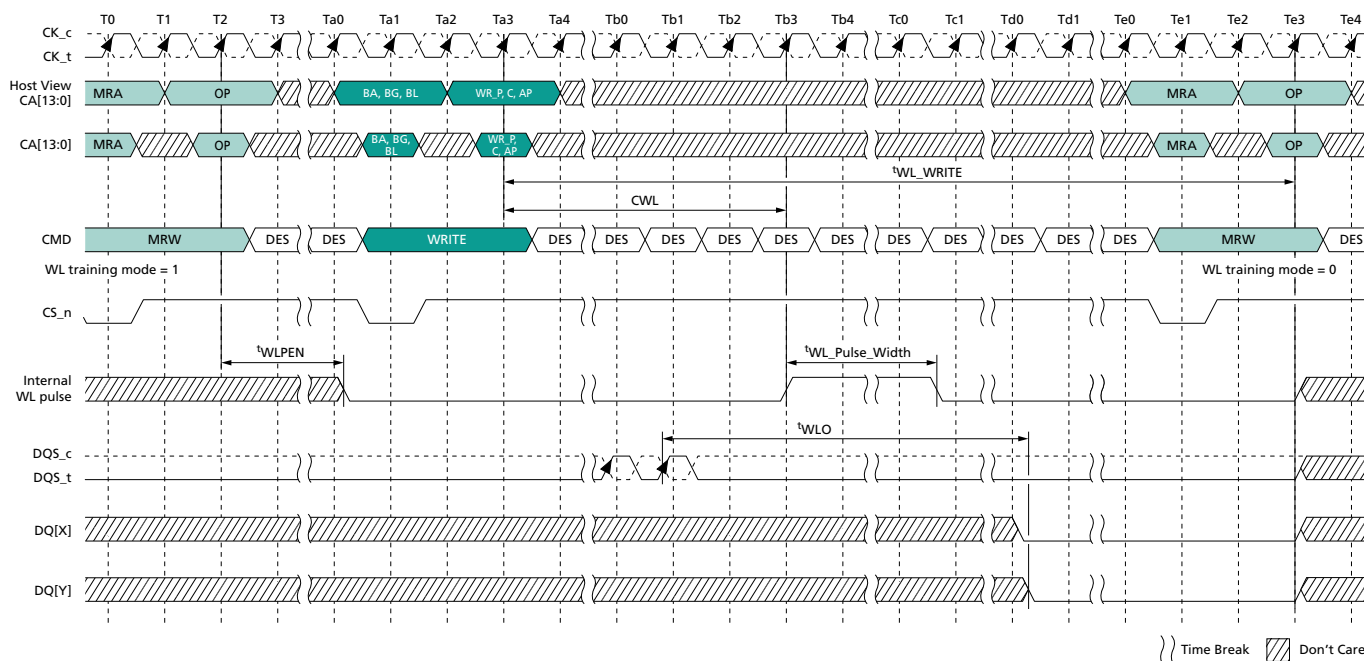


Figure 132: Write Leveling Training Mode (External Training, 1N Mode, 0 Sample)

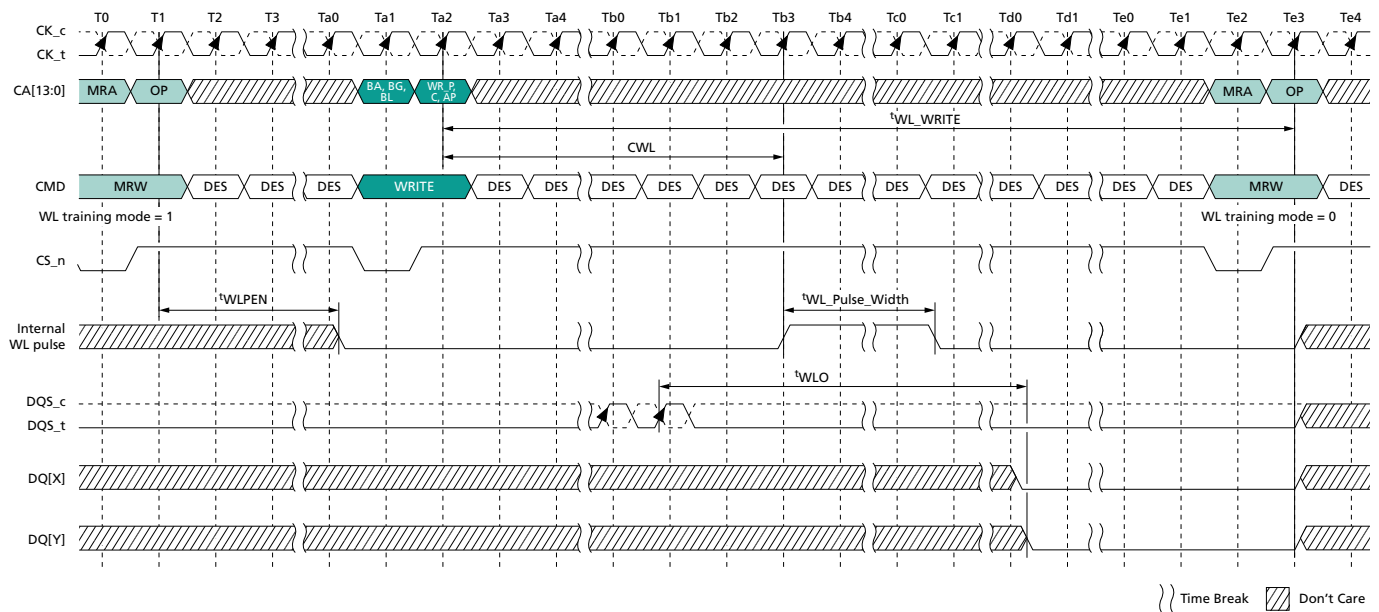


Figure 133: Write Leveling Training Mode (External Training, 2N Mode, 1 Sample)

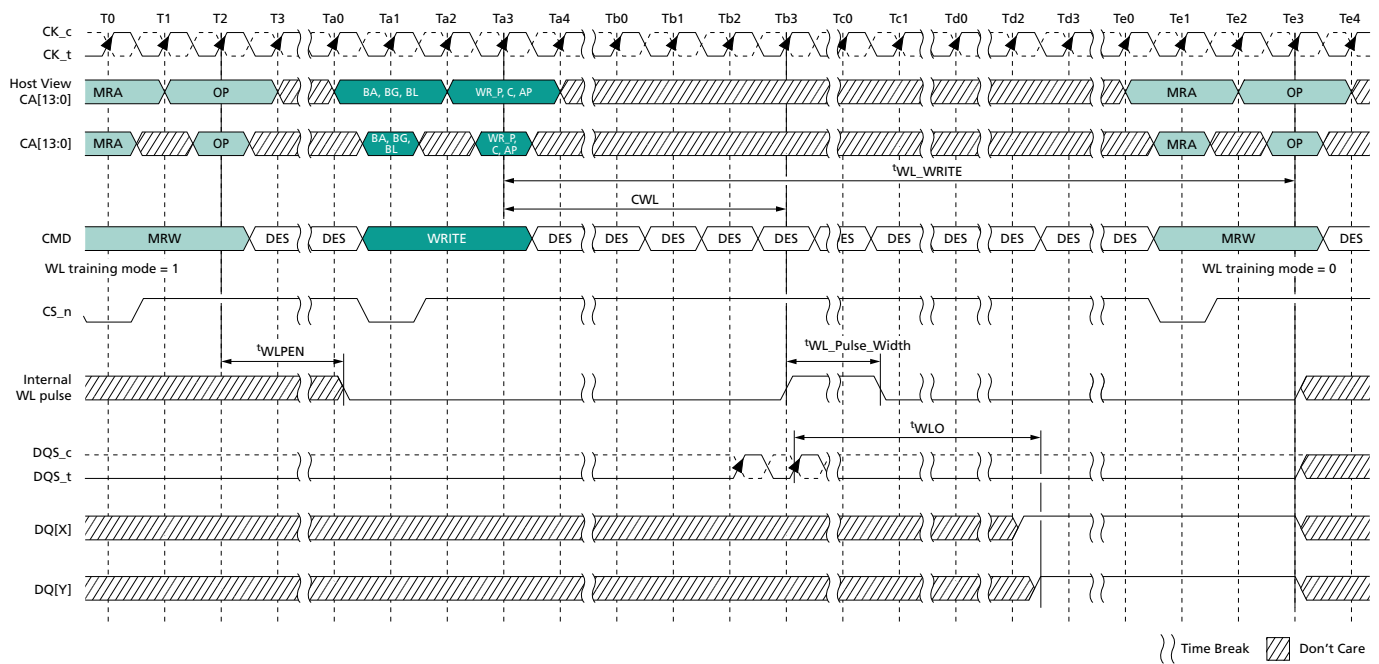
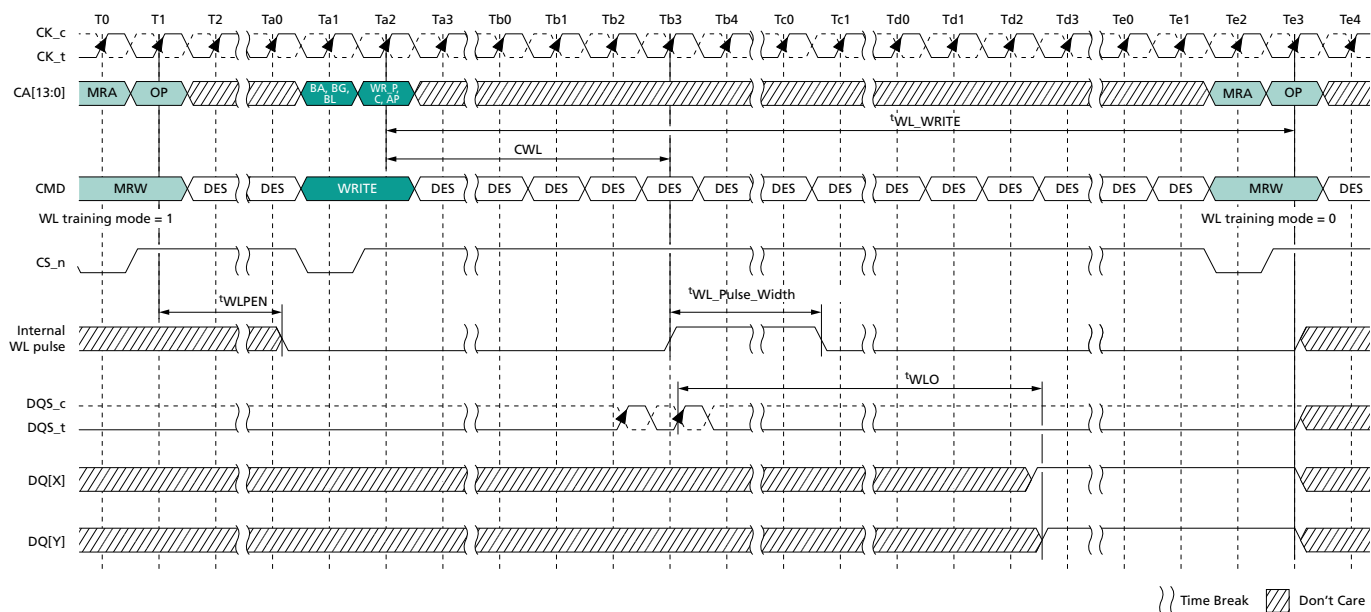


Figure 134: Write Leveling Training Mode (External Training, 1N Mode, 1 Sample)



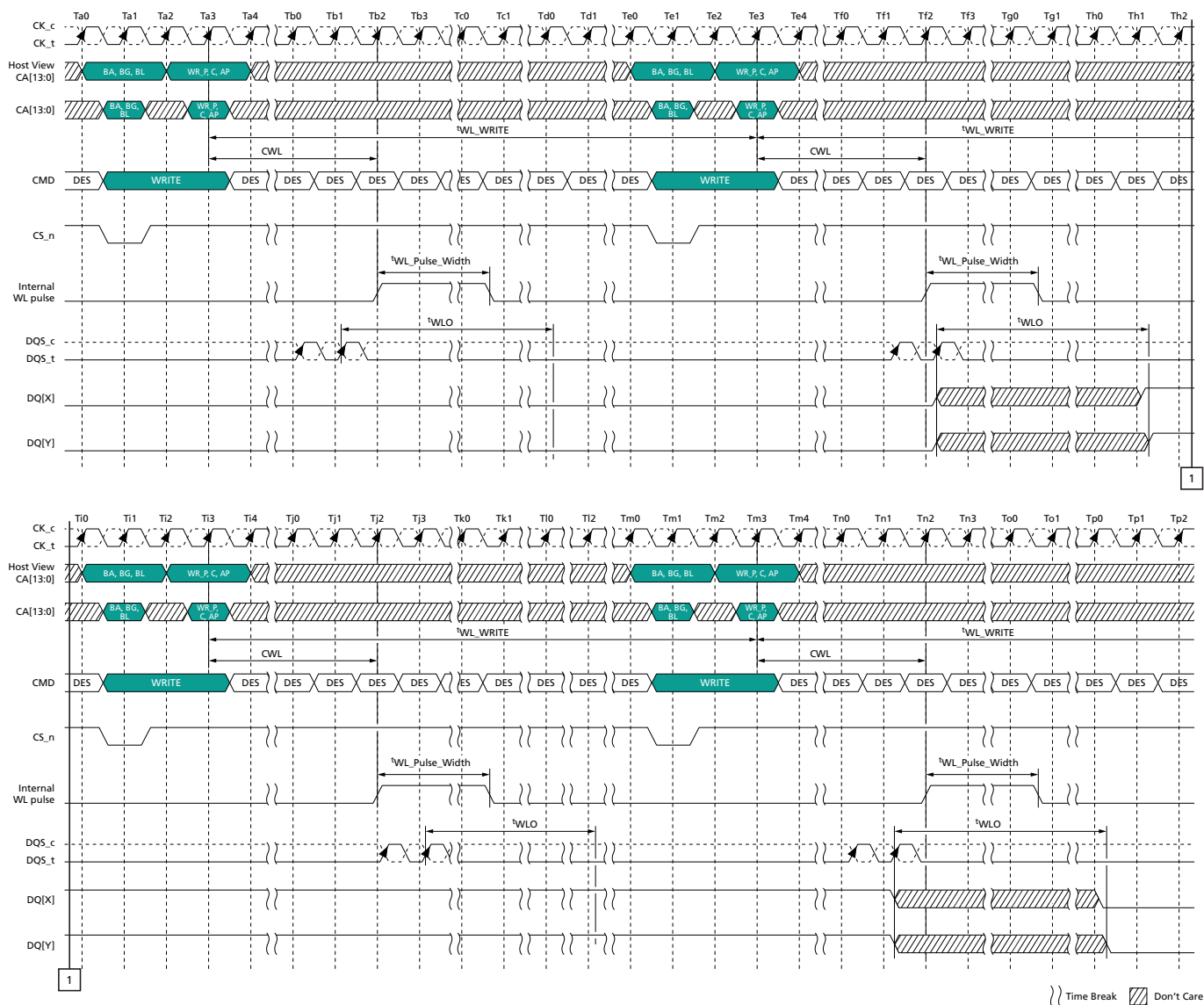
The memory controller initiates write leveling training mode of all DRAMs by setting MR2:OP[1] = 1. When entering write leveling training mode, the DQ pins are in undefined driving mode. Since the controller levels one rank at a time, all non-target ranks will set write leveling training mode to disabled. The controller may assert non-target ODT through the normal WRITE command protocol. The DQS_RTT_PARK termination applies to the DQS_t and DQS_c signals.

The controller drives DQS differentially LOW prior to sending the MRW command to enable write leveling training mode. The WRITE command must occur after a delay of t_{WLPEN} relative to the MRW-enabled write leveling training mode.

The device samples the internal write leveling pulse and asynchronously feeds back the result of this sample on the DQ bus, transitioning between $t_{WLO} (MIN)$ and $t_{WLO} (MAX)$. The controller can sample the state of any DQ bit after $t_{WLO} (MAX)$. Based on the sampled state, the controller decides to increment or decrement the DQS delay setting, and launches the next WRITE command with an associated DQS pulse (or pulse sequence) after some time, which is controller-dependent. Once a 0 to 1 transition on the DQ bus is detected, the controller locks the DQS delay setting and external write leveling is achieved for the device.

Write leveling training may be executed by issuing consecutive WRITE commands after write leveling mode has been enabled (no requirement to exit and re-enter between each WRITE command). The minimum WRITE-to-WRITE command spacing during write leveling mode is t_{WL_Write} and is defined as $\max(CWL, \text{last DQS differential toggle}) + t_{WLO} (MAX) + 2nCK$. An example of consecutive WRITE commands given during write leveling training is shown below.

Figure 135: Consecutive WRITE Commands During Write Leveling Training Mode (External Training, 2N Mode, 4 Samples)



Write Leveling Internal Cycle Alignment Operation

After the external write leveling training step completes, and after the host DQS signals have been aligned to the pin-level write latency timing, the host applies a negative offset (WL_ADJ_start) to the DQS timing. The WL_ADJ_start offset moves the DQS timing prior to the internal write leveling pulse (causing LOW observed on the DQ pins), and it is dependent on the t_{WPRE} setting (shown in the table below). This will be a reference point for aligning the internal write leveling pulse via the WICA settings in MR3.

The internal cycle alignment training begins when an MRW command is issued to enable internal write timing in MR2 (keeping OP[1]=1 and setting MR2:OP[7]=1). The host sweeps the write leveling internal cycle alignment (WICA) delay settings in MR3, starting with the 0 $\times$ CK offset default. Increasing the WICA mode register offset setting speeds up the timing of the WRITE command by reducing the WRITE command to internal write pulse delay until the DQS is aligned with the internal write leveling pulse assertion. Alignment results in a logic HIGH on the DQ pins.

The table below summarizes the WL_ADJ_start and WL_ADJ_end values per t_{WPRE} setting.

Table 218: Write Leveling Internal Cycle Alignment

WL_ADJ Term	Description	$t_{WPRE} = 2^tCK$	$t_{WPRE} = 3^tCK$	$t_{WPRE} = 4^tCK^1$
WL_ADJ_start	Offset that the host applies to the DQS_t/DQS_c timing just after external write leveling alignment to write latency and prior the internal cycle alignment training	-0.75^tCK	-1.25^tCK	-2.25^tCK
WL_ADJ_end	Offset that the host applies to the DQS_t/DQS_c timing after final phase alignment to the rising edge of the write leveling internal pulse. This will center the write leveling internal pulse rising edge within the preamble window	1.25^tCK	1.75^tCK	2.75^tCK

Note: 1. For $t_{WPRE} = 4^tCK$, CL is required to be greater than or equal to 30 during write leveling training mode operation. This is irrespective of the CL setting for $t_{WPRE} = 4^tCK$ during normal operation.

Due to potential measurement errors that can occur during the internal write leveling training, the device may include an optional 0.5^tCK adjustment for optimizing the internal cycle alignment. MR7:OP[0]=1 adds a $+0.5^tCK$ adjustment for the lower byte of the DQs, while MR7:OP[1]=1 adds a $+0.5^tCK$ adjustment for the upper byte of the DQs. The figure below is an example of an internal write leveling training flow with the addition of the $+0.5^tCK$ WICA adjustment (additional flow shown in blue).

Figure 136: Write Leveling Training Flow with Half Step WICA

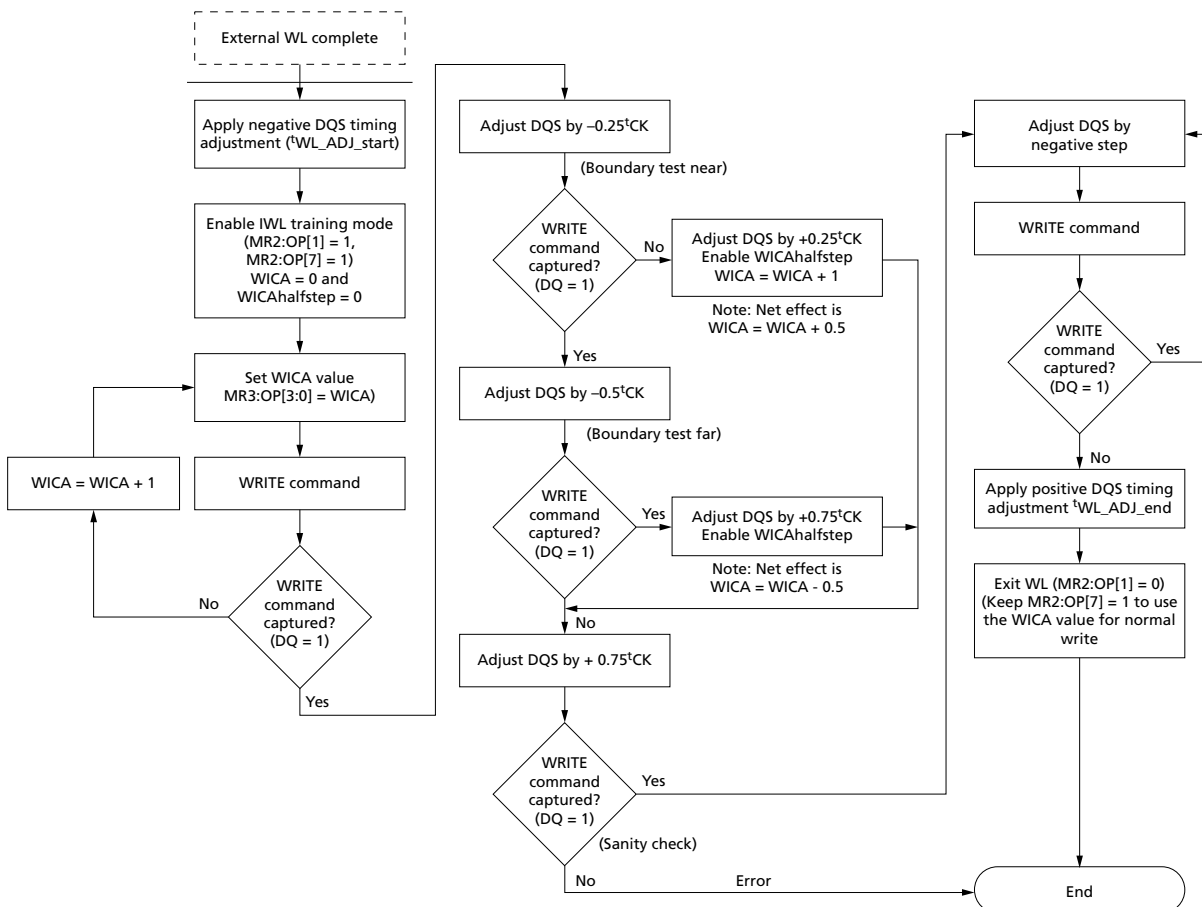


Figure 137: Write Leveling Training Mode (Internal Cycle Alignment, 2N Mode, 0 Sample)

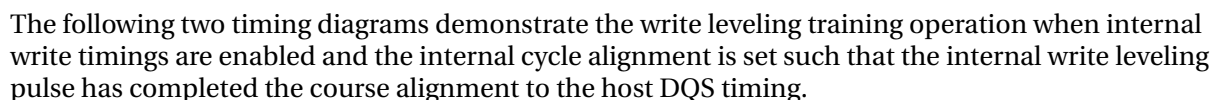


Figure 139: Write Leveling Training Mode (Internal Cycle Alignment, 2N Mode, 1 Sample)

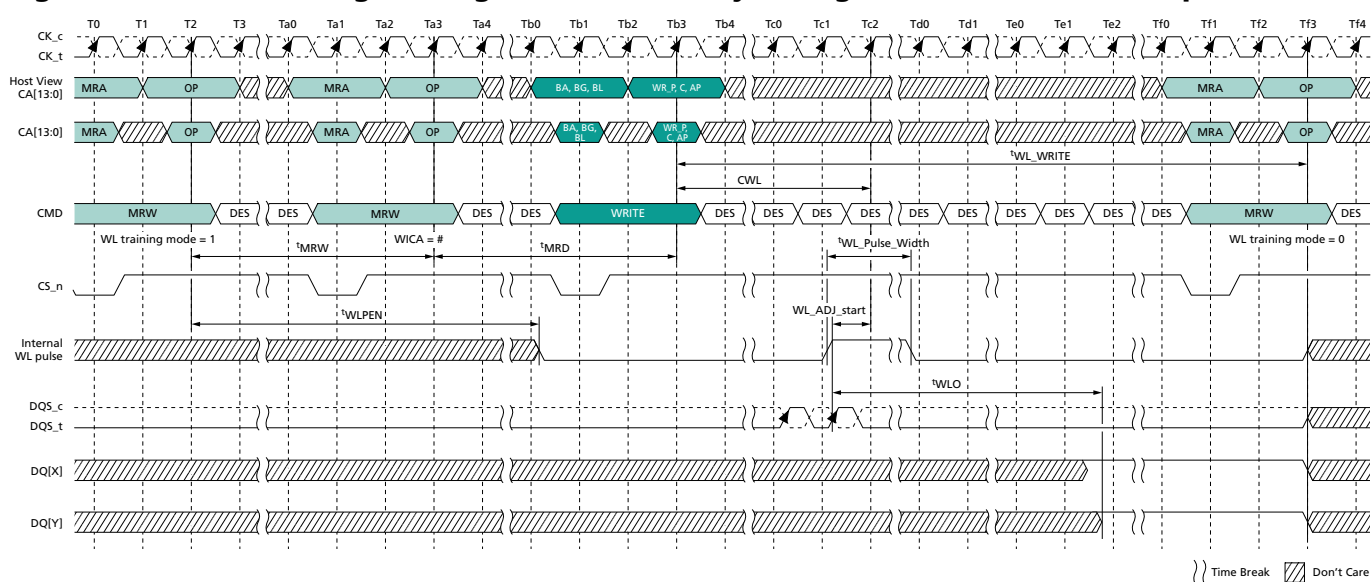
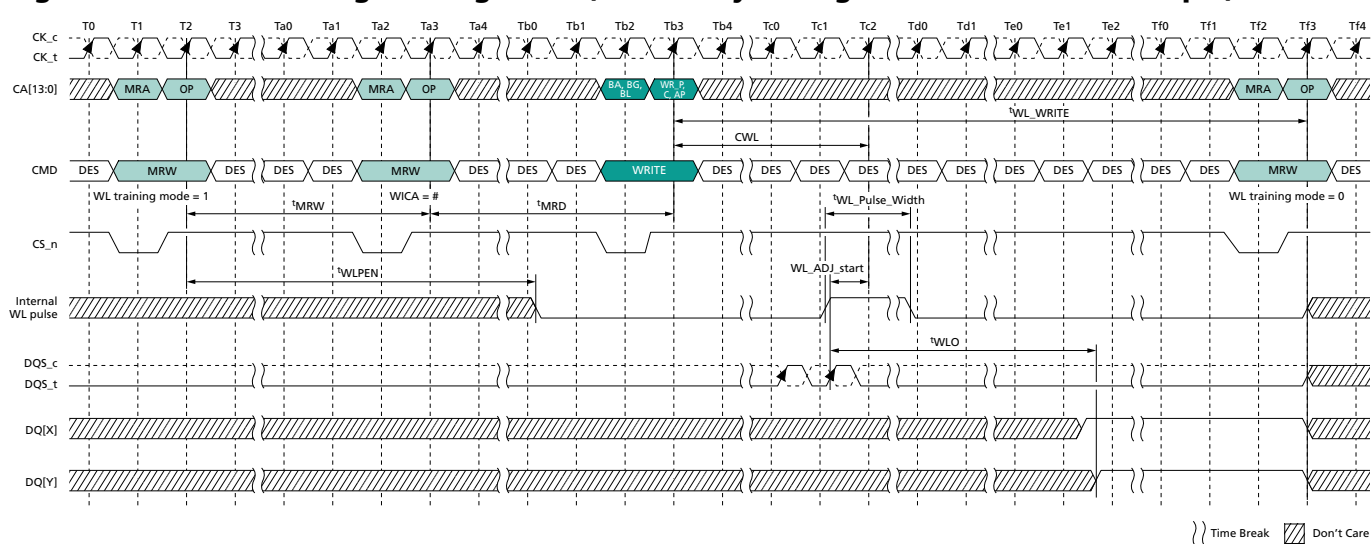
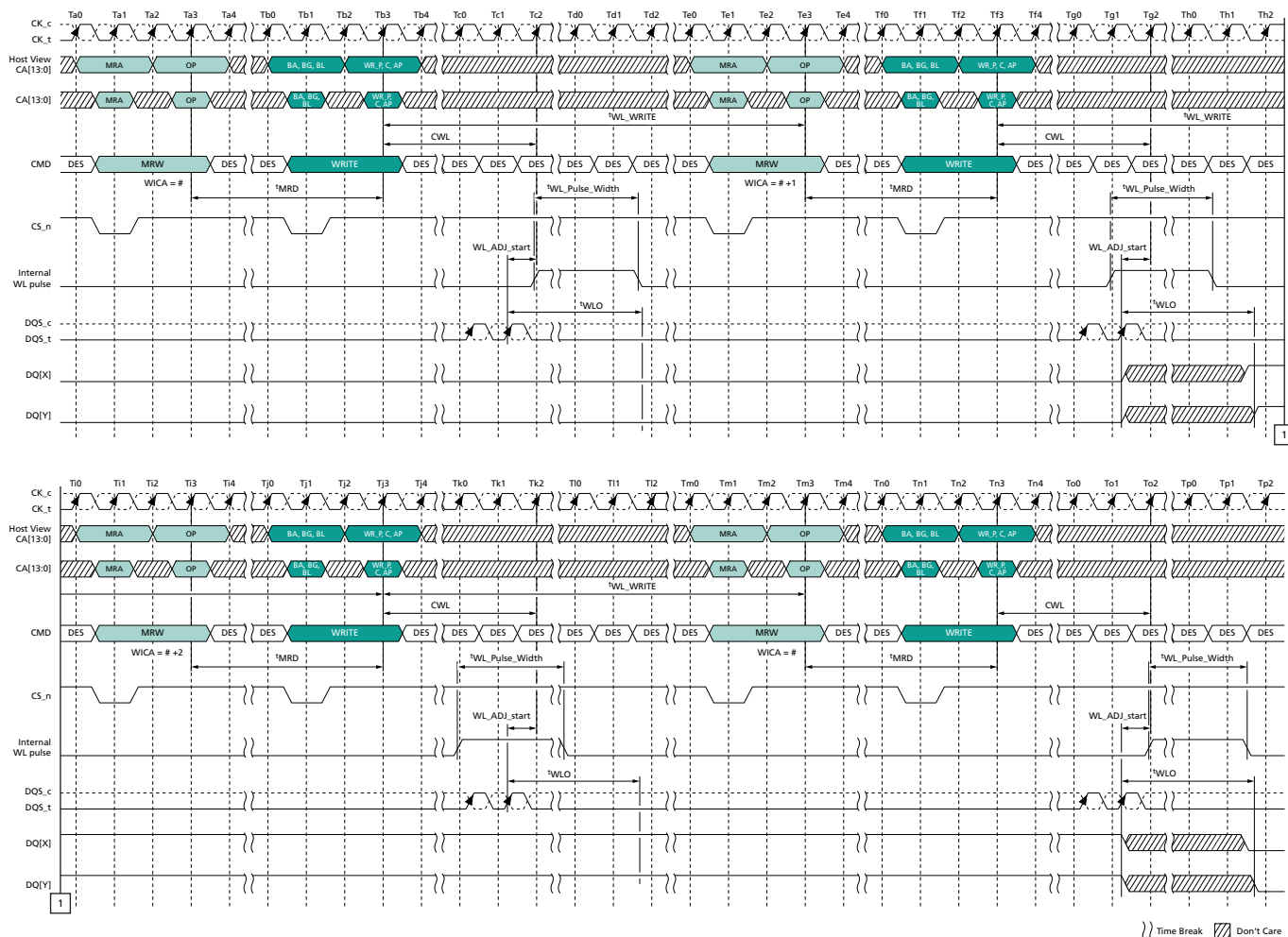


Figure 140: Write Leveling Training Mode (Internal Cycle Alignment, 1N Mode, 1 Sample)



An example of write leveling training internal cycle alignment executed by issuing consecutive WRITE commands after write leveling mode has been enabled (no requirement to exit and re-enter between each WRITE command) is shown below.

Figure 141: Consecutive WRITE Commands During Write Leveling Training Mode (Internal Training, 2N Mode, 4 Samples)



As previously noted, x16 devices enable independent lower and upper byte write leveling training and setting. Although unique values are preferred to optimize (minimize) t_{DQSO} offset, setting both the lower and upper bytes to use the same WICA offset is allowed since the internal paths for both bytes are expected to be closely matched; meaning, internal write leveling training that results in a different byte setting per byte indicates the internal paths are on a boundary between the two settings. When choosing a common WICA offset value, the starting values of the lower and upper WICA offset should differ by no more than one. The higher (smallest absolute value since the WICA values apply a negative offset) of the two values must be programmed in both bytes of the device to minimize the impact on the final training sweep.

Table 219: Common WICA Offset for x16 Upper and Lower Byte

Lower Byte WICA	Upper Byte WICA	Common WICA
-4	-3	-3
-2	-3	-2

When choosing a common 0.5 t_{CK} WICA offset value, the WICA value programmed in both bytes of the device must be the same before applying the 0.5 t_{CK} offset. (If the byte values are different, the higher value is programmed in both bytes of the device, as noted above, and the 0.5 t_{CK} offset step is skipped). If the 0.5 t_{CK} training indicates that one byte requires the +0.5 t_{CK} offset but the other byte

does not, this also indicates the two bytes are on a boundary between the two settings. In this case, the $+0.5 \text{ }^t\text{CK}$ will be applied to both bytes, resulting in the higher (smallest absolute) value being used.

Table 220: Common Half WICA for x16 Upper and Lower Byte

Lower Byte WICA	Lower Byte $+0.5^t\text{CK}$ WICA	Upper Byte WICA	Lower Byte $+0.5^t\text{CK}$ WICA	Common WICA
-4	n/a	-3	n/a	-3
-4	Yes	-4	No	-4 $+0.5$ (-3.5 total)
-3	No	-3	Yes	-3 $+0.5$ (-2.5 total)

When using a common WICA offset value approach to the internal write leveling training, both bytes perform the final training sweep after applying the common WICA offset value (both the full cycle and $0.5 \text{ }^t\text{CK}$ WICA, if applicable).

Write Leveling Internal Phase Alignment and Final Host DQS Timing Operation

After the internal cycle alignment is achieved, the host shall perform a final fine sweep of the DQS timings with internal write timing enabled (MR2:OP[7]=1) to establish an even closer phase alignment to the rising edge of the internal write leveling pulse. Once this is complete, the host will then add a positive offset of WL_ADJ_end (dependent upon $^t\text{WPRE}$) to the DQS_t-DQS_c timings. This results in a $^t\text{DQSoffset}$ between $-0.5 \text{ }^t\text{CK}$ and $+0.5 \text{ }^t\text{CK}$ with measurement adjustments of $^t\text{WLS}/^t\text{WLH}$, placing the rising edge of the internal write leveling pulse within the preamble. If the optional half step WICA process is used during write leveling training, this results in a ^tDQS offset between $-0.25 \text{ }^t\text{CK}$ and $+0.25 \text{ }^t\text{CK}$ with measurement adjustments of $^t\text{WLS}/^t\text{WLH}$. After the WL_ADJ_end offset has been applied, the host will disable write leveling training mode (MR2:OP[1]=0). The internal write timing will remain enabled and the internal cycle alignment setting will retain the coarse setting that was trained. After every reset, the host must either restore these settings or execute the full write leveling training flow.

The following figure shows the timing relationships for the final placement of the host DQS timings relative to the internal write leveling pulse. However, it is not necessary to execute this write leveling training mode measurement to finalize the setting. (Note that this figure is for illustration purposes only.)

Figure 142: Final Timings After Write Leveling Training is Complete (2N Mode)

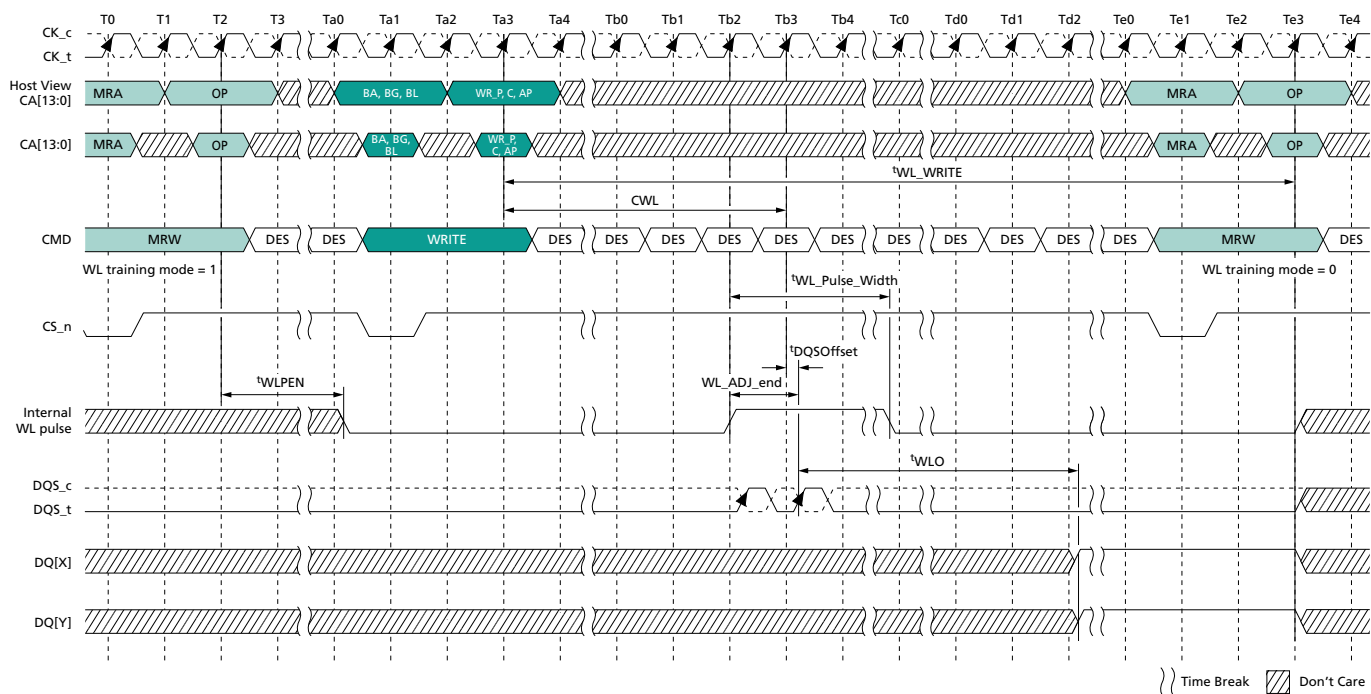
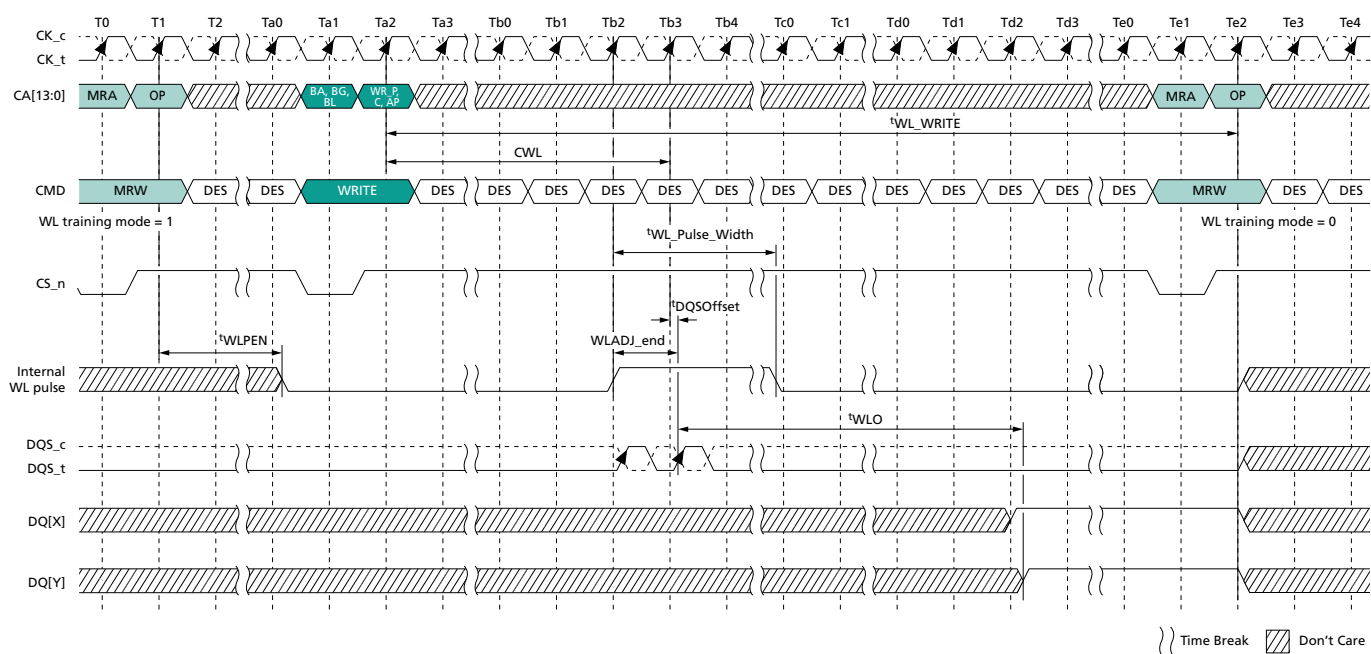


Figure 143: Final Timings After Write Leveling Training is Complete (1N Mode)



DRAM Termination During Write Leveling

When the DRAM is in write leveling mode, the DQS_c/DQS_t termination (DQS_RTT_PARK) and the command and control termination (RTT_CA, RTT_CK, RTT_CS) are the same as for functional operation. The DQ signals are not terminated in the DRAM, but instead are driving values to the controller. The host controller applies termination for the DQ signals.



Table 221: DRAM Termination During Write Leveling

ODT Enabled	DQS_t, DQS_c Termination	DQ Termination
RTT_WR	DQS_RTT_PARK	Off
RTT_Park, RTT_WR disabled	DQS_RTT_PARK	Off

Note: 1. Termination for TDQS/DM is not included since TDQS and DM are disabled during write leveling training mode.

Read Training Pattern

Training of the memory interface requires the ability to read a known pattern from the device, prior to enabling writes to the device. Due to the increased clock frequencies in DDR5, a simple repeating pattern is not sufficient for read training. A linear feedback shift register (LFSR) for a pattern generator is also required.

The read training pattern is accessed when the host issues an MRR command to the MR31 address (OP only need be valid) and CRC must be disabled prior to issuing this command. In this case, the returned data is a pattern instead of the contents of a mode register. The timing of the read data return is the same as for an MRR or READ command, including the operation of the strobes (DQSL_t, DQSL_c, DQSU_t, DQSU_c). The Read Training Pattern is a full BL16 pattern for each MRR command issued to the Read Training Pattern address, regardless of the MR0 burst length setting. No ACT command shall be issued prior to the completion of the BL16 data output. The device also supports non-target ODT.

An alternate continuous burst mode is available and is configured with MRW to MR25:OP[3] = 1. After this mode is configured, an MRR to MR31 on the target device starts the pattern output and automatically continues to output the appropriate pattern until it is stopped by either a system reset or by issuing a MRW to MR25:OP[3] = 0b command that reverts it to the MRR command-based (default) mode, as shown in the Timing Diagram for Continuous Burst Mode Read Training Patterns figure shown later in this section. An MRR to MR31 and an MRW to set MR25:OP[3] = 0 are the only commands allowed after entering Read Training Continuous Burst mode. Issuing any MRR other than to MR31 is invalid and may result in unexpected DQ behavior, requiring the host to issue a reset to exit Continuous Burst mode and restart the training with an MRR to MR31. Data output is a repeated BL16 pattern, regardless of the MR0 Burst Length setting.

Once MR25:OP[3] = 0, MRR command-based (default) mode is registered by the device, it stops all pattern traffic by ^tCont_Exit. Since there is no minimum time for ^tCont_Exit, the device may stop the pattern prior to ^tCont_Exit, potentially truncating any current burst pattern. To ensure the device's state machine doesn't enter metastability while turning off the output pattern, the host must issue a second MRW with MR25:OP[3]=0 after waiting a minimum of ^tMRW but less than a maximum of ^tCBME after the first MRW command with MR25:OP[3] = 0, which then starts ^tCont_Exit_delay. After ^tCont_Exit_delay expires, any other valid command is then legal. No ACT commands shall be issued prior to the completion of read training continuous burst mode. All read training patterns (modes) are supported in continuous burst mode. The host must disable read CRC, if enabled, prior to using continuous burst mode.

While in Read Training Pattern Continuous Burst mode, the DRAM will set the ODT to DQS_RTT_OFF and RTT_OFF for DQS and DQ, respectively, for the duration of the continuous burst mode output. However, if a nontarget rank is intended to provide termination for the duration of the continuous burst mode output on the target rank, the nontarget rank will only terminate the DQ ODT to RTT_NOM_RD (MR35:OP[5:3]) during the BL16 associated with the MRR NT command. Therefore, the host is responsible for ensuring that RTT_PARK (MR34:OP[2:0]) is programmed to align with RTT_NOM_RD (MR35:OP[5:3]), if so desired.

Upon exiting of Read Training Pattern Continuous Burst mode, all RTT_PARK settings of the nontarget rank needs to be programmed for normal operation if previously changed to align with RTT_NOM_RD.

Prior to utilizing either read training pattern mode (Continuous Burst Output mode or MRR Command Based mode), the initial seed value will need to be programmed in MR26-MR30, else the default values will be used. The default value for the Read Pattern Data0/LFSR0 (MR26) register setting is 0x5A, and the default value for the Read Pattern Data1/LFSR1 (MR27) register setting is 0x3C. The Read Pattern Invert (MR28, MR29) register settings default to 0. The Read LFSR Assignments (MR30) register setting default is 0xFE.

The device does not store the current LFSR state when exiting the continuous burst output mode and may clear the pattern values stored in MR26-MR30; therefore, any subsequent pattern reads will require the host to reprogram the seed, pattern, inversion, and LFSR assignments in MR26-MR30.

The read training pattern has two primary modes of operation: serial format and LFSR. LFSR mode is required due to the device's higher frequency bus operation. There is a secondary mode associated with the LFSR mode, which enables the generation of a simple high frequency clock pattern instead of the LFSR pattern. The read training pattern is a full BL16 pattern for each MRR command issued to the read training pattern address.

Table 222: Read Training Pattern Address

MR Address	Operating Mode	Description
MR31	Read Training Pattern	Reserved. No specific register fields are associated with this address. In response to the MRR to this address, the device sends the BL16 read training pattern. All 8 bits associated with this MR address are reserved.

The following table shows the MR field and encodings for the read training pattern format settings. The default value for the read training pattern format register setting is 0x0.

Table 223: Read Training Pattern Format

MR Address	Operating Mode	Description
MR25:OP[0]	Read Training Pattern Format	0 = Serial, 1 = LFSR
MR25:OP[1]	LFSR0 Pattern Option	0 = LFSR, 1 = Clock
MR25:OP[2]	LFSR1 Pattern Option	0 = LFSR, 1 = Clock
MR25:OP[3]	Continuous Burst Mode	0 = MRR command-based (default), 1 = continuous burst output

For serial read training pattern format mode, the following mode registers are programmed with the data pattern. Two 8-bit registers provide a 16 UI pattern length and two 8-bit registers provide up to x16 data width for per-DQ-lane inversion.

LFSR mode requires an 8-bit mode register to program the seed for the 8-bit LFSR. The Read Pattern Data0/LFSR0 and Read Pattern Data1/LFSR1 registers are re-purposed to program the LFSR seed when the Read Training Pattern Format is set to LFSR.

Default Read Pattern Data0/LFSR0 register setting: 0x5A

Table 224: Read Pattern Data0 / LFSR0

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR26	D7	D6	D5	D4	D3	D2	D1	D0

Default Read Pattern Data1/LFSR1 register setting: 0x3C

Table 225: Read Pattern Data1 / LFSR1

MR Address	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR27	D15	D14	D13	D12	D11	D10	D9	D8

The values for the Read Pattern Data0/LFSR0 and Read Pattern Data1/LFSR1 registers may be restored to the default values under the following conditions:

- Self refresh

- Power-down entry
- Exiting continuous burst output mode

If any of the above conditions occur, and non-default values are desired, the host will need to reprogram the contents of MR26 and MR27 prior to utilizing either read training pattern mode (continuous burst output mode or MRR command based mode)

In both cases, when the Read Training Pattern Format is set to serial mode or LFSR mode, the Read Pattern Invert - Lower DQ bits and Read Pattern Invert - Upper DQ bit settings additionally invert the pattern, per DQ bit. The Read Pattern Invert - Lower DQ bits register applies to x4, x8, and x16 devices. The Read Pattern Invert - Upper DQ bits register applies to x16 devices only, for the upper byte.

Default Read Pattern Invert - Lower DQ bits register setting: 0x00

Table 226: Read Pattern Invert - Lower DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR28	DQ Invert	DQL7	DQL6	DQL5	DQL4	DQL3	DQL2	DQL1	DQL0

Default Read Pattern Invert - Upper DQ bits register setting: 0x00

Table 227: Read Pattern Invert - Upper DQ Bits

MR Address	MRW OP	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR29	DQ Invert	DQU7	DQU6	DQU5	DQU4	DQU3	DQU2	DQU1	DQU0

The values for the Read Pattern Invert0 and Read Pattern Invert1 registers may be restored to the default values under the following conditions:

- Power-down entry
- Self refresh entry
- Exiting continuous burst mode

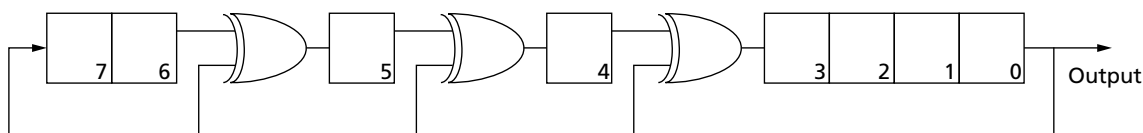
If any of the above conditions occur, the host must reprogram the contents of MR28 and MR29 prior to utilizing either read training pattern mode (continuous burst output mode or MRR command based mode).

A value of 0 in any bit location of the Read Pattern Invert - Lower DQ bits or Read Pattern Invert - Upper DQ bits registers leave the pattern un-inverted for the associated DQ. A value of 1 in any bit location of the Read Pattern Invert - Lower DQ bits or Read Pattern Invert - Upper DQ bits registers invert the pattern for the associated DQ.

LFSR Pattern Generation

The LFSR is an 8-bit Galois LFSR. The polynomial for the LFSR is $x^8 + x^6 + x^5 + x^4 + 1$. The figure below shows the logic to implement the LFSR. The numbered locations within the shift register show the mapping of the seed/state positions within the register. There are two instances of the same LFSR polynomial. These two instances have unique seeds/states and supply patterns to any of the DQ outputs.

Figure 144: Read Training Pattern LFSR



The seed location in the figure clarifies the mapping for the Read Pattern Data0/LFSR0 and Read Pattern Data1/LFSR1 mode registers relative to the LFSR logic. The LFSR output is directed to any number of the DQ outputs, depending on the LFSR assignment programming. These assignments between LFSR0 and LFSR1 to each DQ output create a unique pattern sequence for better coverage of DQ to DQ crosstalk interactions. The LFSR assignments are programmed according to the following table.

Default Read LFSR Assignments register setting: 0xFE

Table 228: Read LFSR Assignments

MR Address	MRW OP	LFSR Assignment	MR Setting	
MR30	OP0	DQL0/DQU0	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1
	OP1	DQL1/DQU1	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1
	OP2	DQL2/DQU2	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1
	OP3	DQL3/DQU3	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1
	OP4	DQL4/DQU4	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1
	OP5	DQL5/DQU5	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1
	OP6	DQL6/DQU6	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1
	OP7	DQL7/DQU7	0 = Read Training Pattern Data0 / LFSR0	1 = Read Training Pattern Data1 / LFSR1

The values for the Read LFSR Assignments register may be restored to the default values under the following conditions:

- Power-down entry
- Self refresh entry
- Exiting continuous burst output mode

If any of the above conditions occur, the host must reprogram the contents of MR30 prior to utilizing either read training pattern mode (continuous burst output mode or MRR command based mode).

The LFSR output changes at the UI frequency, producing a new output value on every UI. The LFSR only changes state to support the read data after the MRR to the Read Training Pattern address (MR31). When there are no MRR accesses to the Read Training Pattern address (MR31), the LFSR retains its previous state (from the end of the previous Read Training Pattern MRR access completion); therefore, the full state space of the LFSR may be traversed through a series of 16 MRR commands, each of which accesses 16 UIs of LFSR output. The BL for the LFSR data is always BL16. The state of the LFSR can also be changed by sending a new MRW command to reset the LFSR0 and LFSR1 seed mode registers (MR26 and MR27) or through the reset conditions listed for those registers. A setting of 0x00 in either of the LFSR seed registers (MR26 and MR27) does not produce a pattern with any transitions to 1. When set to this value, the LFSR produces a constant 0 pattern.

When the LFSR0 Pattern Option (MR25:OP[1]) is set to 1, the pattern supplied by the device is a high-frequency clock pattern instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 0 in the corresponding DQ opcode location in the Read LFSR Assignments register. The

first UI of the pattern has a value of 0. The second UI has a value of 1, and this continues to toggle for each subsequent UI.

When the LFSR1 Pattern Option (MR25:OP[2]) is set to 1, the pattern supplied by the device is a high-frequency clock pattern instead of the LFSR. This clock pattern is sent only to the DQ signals that have a setting of 1 in the corresponding DQ opcode location in the Read LFSR Assignments register. The first UI of the pattern has a value of 0. The second UI has a value of 1, and this continues to toggle for each subsequent UI.

The state of the LFSR does not change when an MRR to MR31 occurs if the associated LFSR Pattern Option is set to 1 in MR25[1] for LFSR0, or MR25[2] for LFSR1, designating the clock pattern. The state of both LFSR0 and LFSR1 also does not change when an MRR to MR31 occurs if the serial mode is selected by setting MR25[0] = 0b. The Read LFSR Assignments settings have no impact on whether or not the LFSR state progresses with each MRR to MR31. Only the Read Training Pattern Format and LFSR Pattern Option settings determine whether the LFSR is actively computing next states.

Read Training Pattern Examples

The following table shows the bit sequence of the read training pattern, for the following programming:

- Read Training Pattern Format = 0 (Serial)
- LFSR0 Pattern Option = 0 (These are don't-cares when in Serial Training Pattern Format)
- LFSR1 Pattern Option = 0 (These are don't-cares when in Serial Training Pattern Format)
- Read Pattern Data0/LFSR0 = 0x1C
- Read Pattern Data1/LFSR1 = 0x59
- Read Pattern Invert0 = 0x55
- Read Pattern Invert1 = 0x55

Table 229: Serial Bit Sequence Example

Pin	Invert	Bit Sequence															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQL6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQL7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU0	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU1	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU2	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU3	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU4	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU5	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQU6	1 (Yes)	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQU7	0 (No)	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

The following table shows the bit sequence of the read training pattern, for the following programming:

- Read Training Pattern Format = 1 (LFSR)
- LFSR0 Pattern Option = 0
- LFSR1 Pattern Option = 0
- Read Pattern Data0/LFSR0 = 0x5A
- Read Pattern Data1/LFSR1 = 0x3C
- Read LFSR Assignments = 0xFE
- Read Pattern Invert0 = 0x00
- Read Pattern Invert1 = 0xFF

Table 230: LFSR Bit Sequence Example 1

Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	0 (No)	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0
DQL1	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL2	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL3	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL4	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL5	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL6	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQL7	0 (No)	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
DQU0	1 (Yes)	0	1	1	0	0	1	1	1	1	1	1	0	0	0	1	0	1
DQU1	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU2	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU3	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU4	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU5	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU6	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
DQU7	1 (Yes)	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1

The following table shows the bit sequence of the read training pattern, for the following programming:

- Read Training Pattern Format = 1 (LFSR)
- LFSR0 Pattern Option = 0
- LFSR1 Pattern Option = 1 (clock pattern option)
- Read Pattern Data0/LFSR0 = 0x00 (when the LFSR seed is set to 0, a constant 0 pattern is produced)
- Read Pattern Data1/LFSR1 = 0x3C (this value is don't care when LFSR1 pattern option = 1)
- Read LFSR Assignment = 0x04
- Read Pattern Invert - Lower DQ bits = 0xFB
- Read Pattern Invert - Upper DQ bits = 0xFB

Table 231: LFSR Bit Sequence Example 2

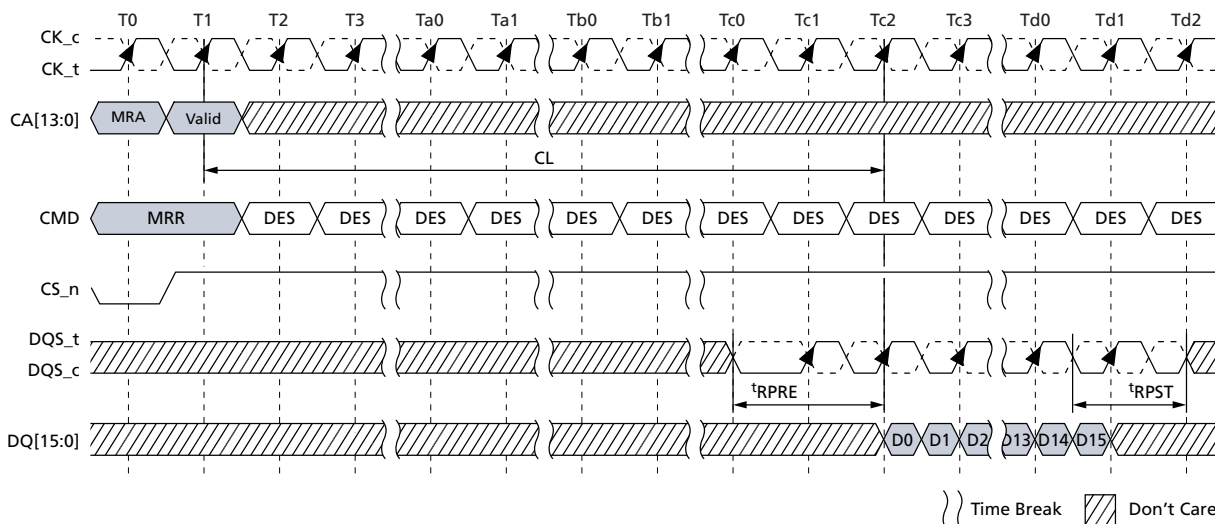
Pin	Invert	LFSR	Bit Sequence															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQL0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQL3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQL7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU0	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU1	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU2	0 (No)	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
DQU3	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU4	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU5	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU6	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DQU7	1 (Yes)	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Read Training Pattern Timing Diagrams

The data return and strobe sequence timings should match the READ operation timing. The timing of the read training pattern is similar to the MRR operation, with the exception that the MRR to the address that invokes the read training pattern is a full BL16 pattern. The timing between MRR commands to access the read training pattern is defined as t_{MRR_p} , which supports back-to-back data patterns. This is faster than a normal MRR-to-MRR condition, which is defined as t_{MRR} .

The following timing diagram shows the general timing sequence for an MRR that accesses the read training pattern.

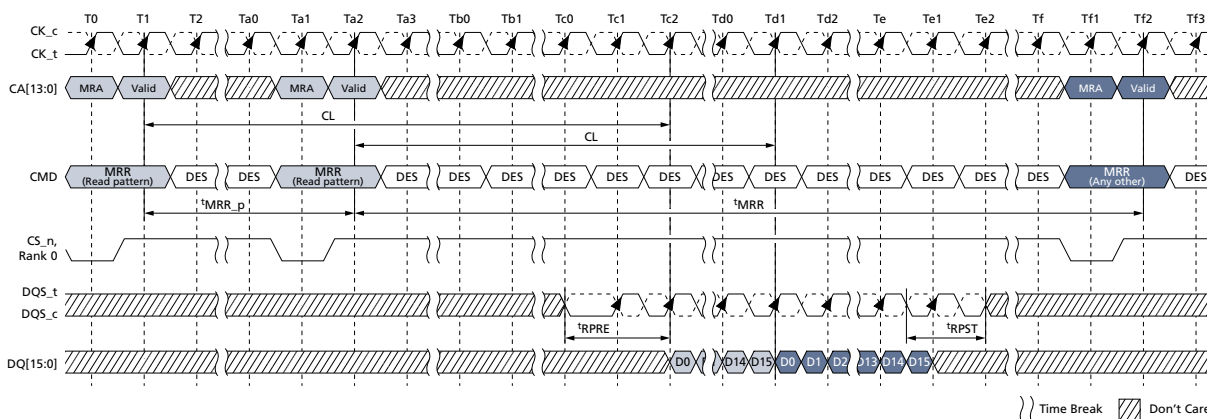
Figure 145: Read Training Patterns



Note: 1. The read training pattern must align to the preamble timings.

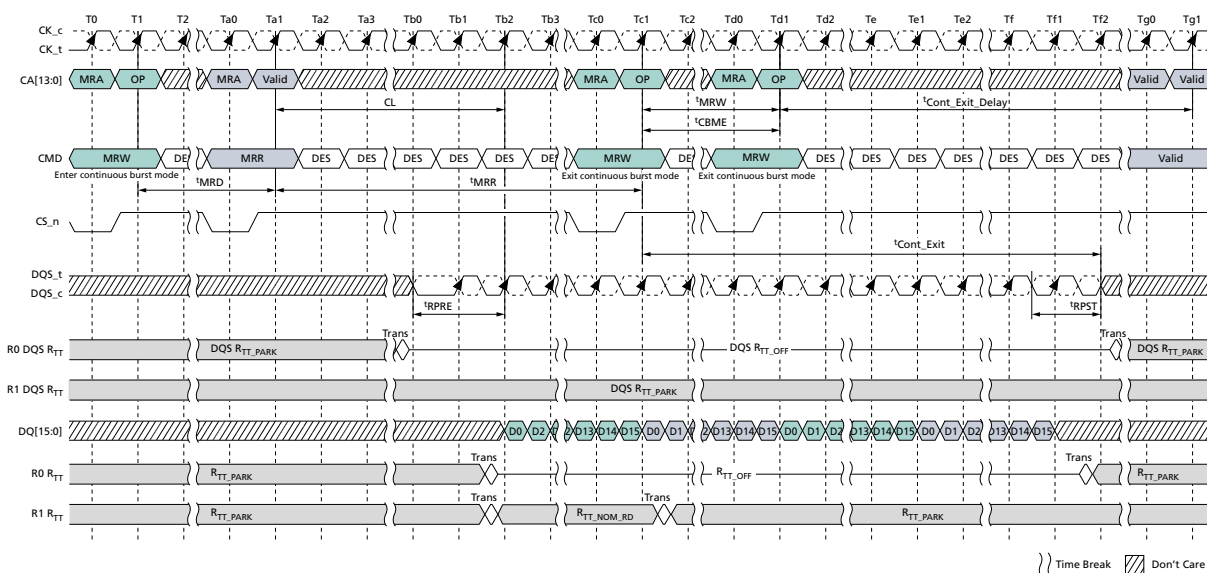
The read training pattern must also support back-to-back traffic for any number of MRR commands sequenced every 8CK. The following timing diagram shows a back-to-back pattern example.

Figure 146: Back-to-Back Read Training Patterns



Note: 1. The read training pattern must align to the preamble timings.

Figure 147: Continuous Burst Mode Read Training Patterns



Notes: 1. The read training pattern shall align to the preamble timings and exits after MRW (continuous exit encoding) is received, but before $t_{\text{Cont\_exit}}$ expires. During $t_{\text{Cont\_exit}}$, the data output may not follow the read pattern data.

2. The host is responsible for properly setting $R_{\text{TT\_PARK}}$ of the nontarget rank is programmed to align with $R_{\text{TT\_NOM\_RD}}$, if desired.

Read Preamble Training Mode

Read preamble training mode supports read leveling of the host receiver timings. This mode supports MRR transactions that access the read training pattern and cannot be used during any other data transactions. Similar to read training pattern mode, read preamble training mode needs to be entered with CRC disabled.

Read preamble training mode changes the read strobe behavior such that the strobes are always driven by the device, and only toggle during a 1^tCK preamble plus the actual burst of the read data. There is no toggle during the postamble time. This mode enables the host to detect the timing of when the first data and associated strobe is returned after a READ command.

Entry and Exit for Preamble Training Mode

The device enters read preamble training mode by setting MR2:OP[0] = 1. Read preamble training mode is exited by setting MR2:OP[0] = 0. Read preamble training model must not be disturbed by an ACT command until the completion of training.

Table 232: Preamble Training Mode Configuration

MR Address	Operating Mode	Description
MR2:OP[0]	Read preamble training mode enable	0 = Normal Mode (default) 1 = Read Preamble Training Mode

Preamble Training Mode Operation

After the device is placed in read preamble training mode, the only data transactions supported are MRR commands. Other data transactions and some non-data transactions are not allowed during read preamble training mode. Commands allowed or not allowed are as follows:

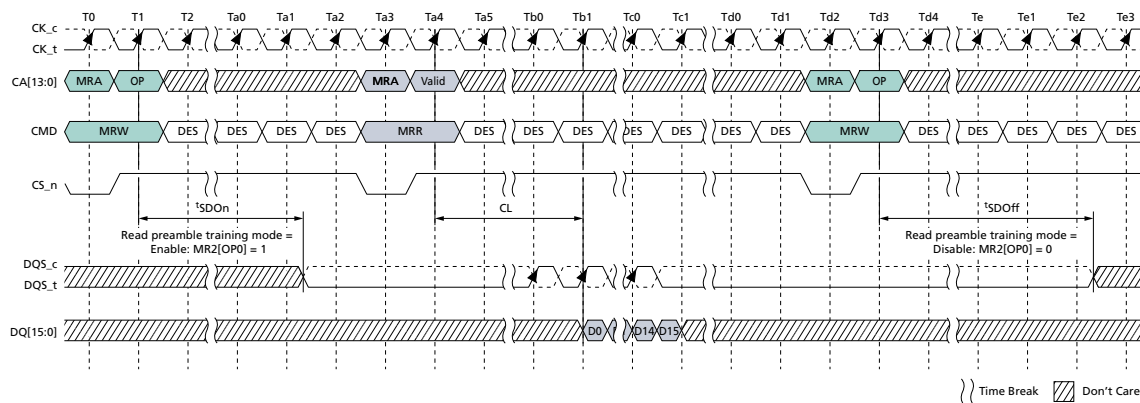
- Allowed while in preamble training mode: MPC functions allowed when current state is Active: MRW, MRR, REFab, REFsb, RFMab, RFMsb, NOP
- Not allowed while in preamble training mode: MPC functions only allowed when current state is All Banks Idle: ACT, WRP, WRPA, WR, WRA, RD, RDA, VrefCA, VrefCS, PREab, PREsb, PREpb, SRE, SREF, PDE, PDX

After read preamble training mode is enabled, the device will drive DQS_t LOW and DQS_c HIGH within ^tSDOn and remain at these levels until an MRR command is issued.

During read preamble training mode, a 1^tCK preamble will be used instead of the programmed DQS preamble setting. After the MRR command is issued, the device will drive DQS_t/DQS_c after CL-^tRPRE (where ^tRPRE = 1CK), like a normal READ burst with the Read DQS Offset setting in MR40 applied. In response to the MRR to the designated read training pattern address, the device must also drive the DQ pattern as per the read pattern configuration while in this mode. The MRR commands may be sequenced to enable back to back bursts on the DQ bus.

Read preamble training mode is exited within ^tSDOff after setting MR2:OP[0]. The following figure shows the timing for the strobe driven differential LOW after read preamble training mode is enabled, and also shows the strobe timings, including a 1^tCK preamble, after an MRR command to access the read training pattern.

Figure 148: Preamble Training Mode Entry, Read Training Pattern Access, and Read Preamble Training Mode Exit



DQS Interval Oscillator

As voltage and temperature changes on the die, the DQS clock tree delay shifts and may require re-training. An internal DQS clock-tree oscillator, which measures the amount of delay over a given time interval (determined by the controller), enables the controller to compare the trained delay value to the delay value seen at a later time. The DQS interval oscillator provides the controller with important information regarding the need to re-train and the magnitude of potential error.

The DQS interval oscillator starts by issuing an MPC command with start DQS interval OSC (DQSOSCST) opcode, OP[7:0] = 0000 0111b set as described in the MPC Operation section. This starts an internal ring oscillator that counts the number of times a signal propagates through a copy of the DQS clock tree.

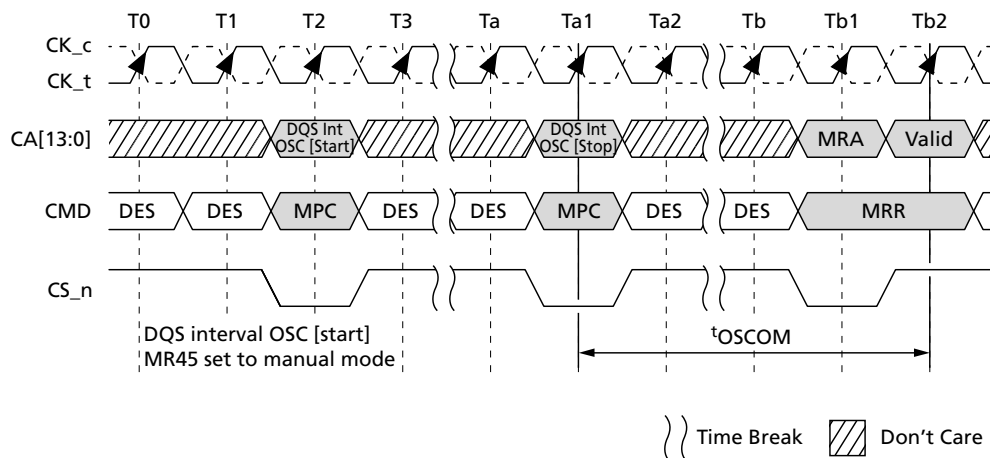
The DQS interval oscillator may be stopped by issuing an MPC command with stop DQS interval OSC (DQSOSCSP) opcode, OP[7:0] = 0000 0110b, as described in the MPC Operation section, or the controller may instruct the device to count for a specific number of clocks and then stop automatically (see mode registers 45, 46 and 47 for more information). If MR45 is set to automatically stop the DQS oscillator, the MPC command with stop DQS interval OSC opcode will not be used. When the DQS oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR46 and MR47 after the oscillator is stopped and within ^tOSCOA for automatic mode and ^tOSCOM for manual mode.

MRW commands to MR45 during an ongoing DQS interval oscillator operation are not permitted. MR45 may be reprogrammed ^tMRD after the oscillator is stopped by the automatic stop.

The device responds in one of two ways if an MPC command with start DQS interval OSC opcode is issued during an ongoing DQS interval oscillator operation (automatic or manual): The device ignores the concurrent start operation, in which case the DQS interval oscillator operation proceeds as normal with all timing constraints referencing the original start operation; or, the device restarts the DQS interval oscillator operation, in which case all timing constraints reference the most recent (subsequent) start operation. The host must account for the worst-case option in the event that a concurrent start operation is issued. If issuing a concurrent MPC command [start DQS interval OSC] results in a loss of run time tracking, the results stored in MR46 and MR47 are ignored and the full operation restarts.

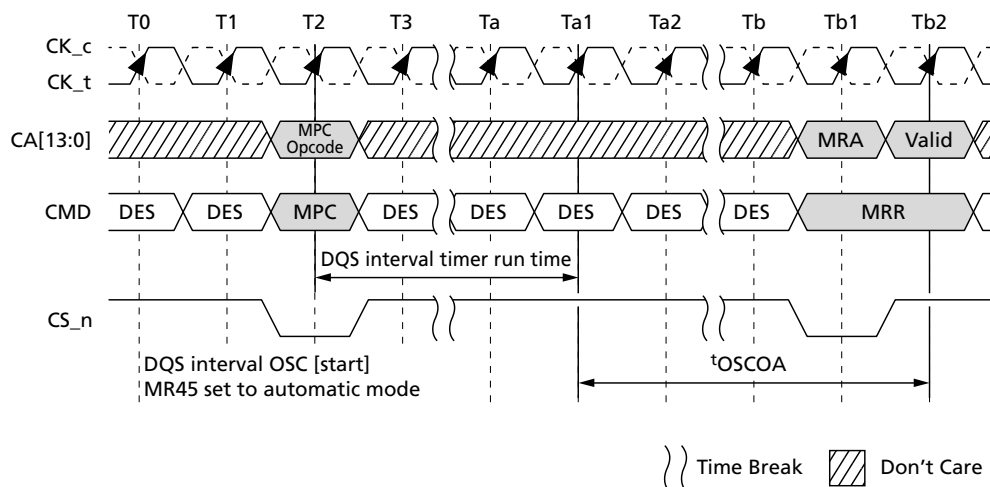
Entering self refresh during an ongoing DQS interval oscillator operation is permitted. Upon exiting self refresh, an operation started in automatic mode is allowed to complete naturally based upon the specified number of clocks (cumulative before and after self refresh). If a manual operation started prior to entering self refresh is not stopped prior as well, the operation is manually stopped upon self refresh exit. The results stored in MR46 and MR47 for a DQS interval oscillator operation that spans self refresh entry/exit is ignored and the full operation restarted.

Figure 149: DQS Interval Oscillator Manual Mode



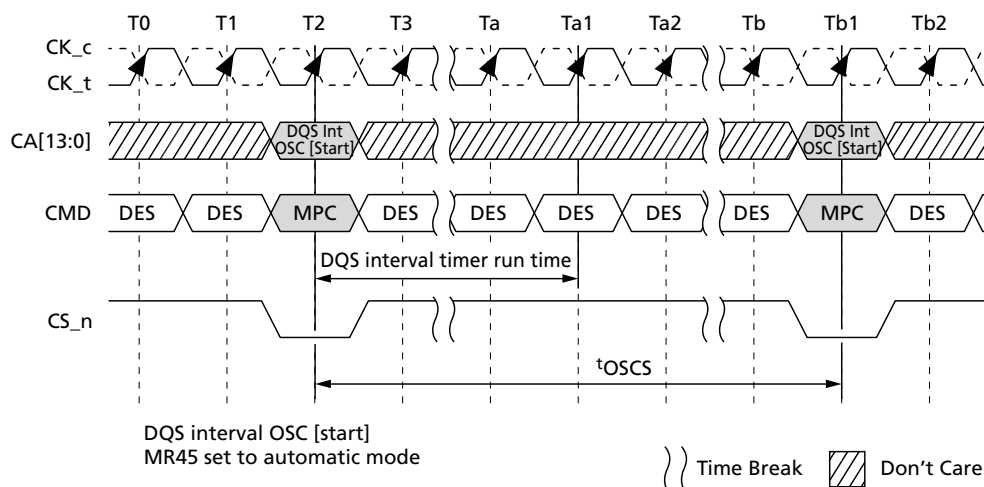
Note: 1. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 150: DQS Interval Oscillator Automatic Mode



Note: 1. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 151: DQS Interval Oscillator with back to back Automatic Mode Timing



Note: 1. DES commands are shown for ease of illustration; other commands may be valid at these times.

The controller may adjust the accuracy of the result by running the DQS interval oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{DQS oscillator granularity error} = \frac{2 \times (\text{DQS delay})}{\text{Run time}}$$

Where:

- Run time = total time between start and stop commands
- DQS delay = value of the DQS clock tree delay t_{RX_DQS2DQ} (MIN/MAX)

An additional device matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific. Therefore, the total accuracy of the DQS oscillator counter is given by:

$$\text{DQS oscillator accuracy} = 1 - \text{granularity error} - \text{matching error}$$

Example: If the total time between start and stop commands is 100ns, and the maximum DQS clock tree delay is 400ps ($t_{RX\_DQS2DQ,MAX}$), the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.4\text{ns})}{100\text{ns}} = 0.8\%$$

This equates to a granularity timing error of 3.2ps.

Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{3.2 + 5.5}{400} = 97.8\%$$

Example: Running the DQS oscillator for a longer period improves the accuracy. If the total time between start and stop commands is 250ns, and the maximum DQS clock tree delay is 400ps ($t_{RX\_DQS2DQ,MAX}$), the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.4\text{ns})}{250\text{ns}} = 0.32\%$$

This equates to a granularity timing error of 1.28ps.

Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{1.28 + 5.5}{400} = 98.3\%$$

The result of the DQS interval oscillator is defined as the number of DQS clock tree delays that can be counted within the run time, determined by the controller. The result of the MPC command [start DQS interval OSC] operation is stored in MR46 and MR47. MR46 contains the least-significant bits (LSB) of the result; MR47 contains the most-significant bits (MSB) of the result. MR46 and MR47 are overwritten by the device when an MPC command [stop DQS interval OSC] is received. The device counter counts to its maximum value ($=2^{16}$) and stops. If the maximum value is read from the mode registers, the memory controller must assume that the counter overflowed the register and discarded the result. The longest run time for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest run time interval} = 2^{16} \times t_{RX\_DQS2DQ} \text{ (MIN)}$$

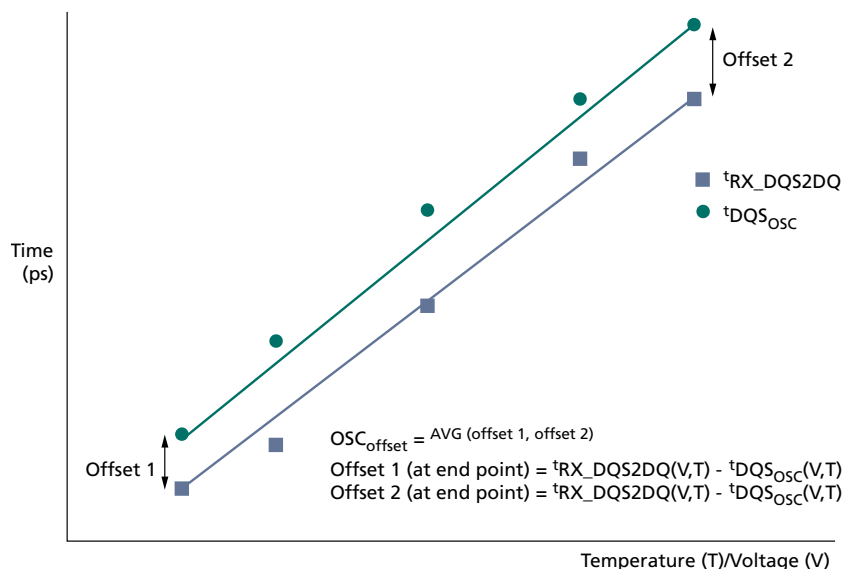
Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the DQS training circuit (interval oscillator) and the actual DQS clock tree across voltage and temperature.

Parameters:

- t_{RX_DQS2DQ} : Actual DQS clock tree delay
- t_{DQSOSC} : Training circuit (interval oscillator) delay
- OSCOffset: Average delay difference over voltage and temperature (shown in the following figure)
- OSCMatch: DQS oscillator matching error

Figure 152: Interval Oscillator Offset OSCOffset



OSCmatch:

$$OSC_{Match} = [t_{RX\_DQS2DQ}(V,T) - t_{DQS\_OSC}(V,T) - OSC_{offset}]$$

t_{DQSOSC} :

$$t_{DQS\_OSC}(V,T) = \frac{\text{Run time}}{2 \times \text{Count}}$$

Table 233: DQS Oscillator Matching Error Specification

Parameter	Symbol	MIN	MAX	Unit	Notes
DQS oscillator matching error	OSC _{Match}	-10	10	ps	1,2,3,4,5,6,7,8
DQS oscillator offset	OSC _{Offset}	-150	150	ps	2,4,6,7

- Notes: 1. OSC_{Match} is the matching error between the actual DQS and DQS interval oscillator over voltage and temperature.
2. This parameter is characterized or guaranteed by design.
3. The OSC_{Match} is defined as the following, where ^tRX_DQS2DQ (V,T) and ^tDQS,OSC (V,T) are determined over the same voltage and temperature conditions:

$$OSC_{Match} = [{}^tRX\_DQS2DQ(V,T) - {}^tDQS,OSC(V,T) - OSC_{offset}]$$

4. The oscillator run time must be at least 200ns for determining ^tDQS,OSC (V,T).

$${}^tDQS,OSC(V,T) = \frac{\text{Run time}}{2 \times \text{Count}}$$

5. The input stimulus for ^tRX_DQS2DQ is consistent over voltage and temperature conditions.
6. The OSC_{Offset} is the average difference of the endpoints across voltage and temperature.
7. These parameters are defined per channel.
8. ^tRX_DQS2DQ (V,T) delay is the average of DQS to DQ delay over the runtime period.
9. The matching error and offset of OSC came from DQS2DQ interval oscillator.

^tRX_DQS2DQ Offset Due to Temperature and Voltage Variation

As temperature and voltage change on the die, the DQS clock tree shifts and may require retraining. The oscillator is typically used to measure the amount of delay over a given time interval (determined by the controller), enabling the controller to compare the trained delay value to the delay value seen at a later time. The ^tRX_DQS2DQ offset due to temperature and voltage variation specification can be used for instances when the oscillator cannot be used to control the ^tRX_DQS2DQ.

Table 234: ^tRX_DQS2DQ Offset Due to Temperature and Voltage Variation: 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit s	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS to DQ offset temperature variation	^t RX_DQS2DQ_t emp	-	12.75	-	11.34	-	10.20	-	9.28	-	8.50	ps/ 10°C	1,3
DQS to DQ offset voltage variation	^t RX_DQS2DQ_v olt	-	45.00	-	43.00	-	41.00	-	39.00	-	32.00	ps/ 50mV	2,3

- Notes: 1. ^tRX_DQS2DQ max delay variation as a function of temperature.
2. ^tRX_DQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD}. It includes the V_{DDQ} and V_{DD} AC noise impact for frequencies >20 MHz and max voltage of 45mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement V_{DDQ}=V_{DD} is assumed
3. Absolute value of DQS to DQ offset.

Table 235: ^tRX_DQS2DQ Offset Due to Temperature and Voltage Variation: 5200-6800

Parameter	Symbol	5200		5600		6000		6400		6800		Unit s	Note s
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS to DQ offset temperature variation	^t RX_DQS2DQ_t emp	-	7.85	-	7.29	-	6.80	-	6.38	-	6.00	ps/ 10°C	1,3

Table 235: t_{RX_DQS2DQ} Offset Due to Temperature and Voltage Variation: 5200-6800 (Continued)

Parameter	Symbol	5200		5600		6000		6400		6800		Unit s	Note s
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS to DQ offset voltage variation	$t_{RX\_DQS2DQ\_volt}$	-	30.00	-	28.00	-	26.25	-	25.00	-	23.75	ps/ 50mV	2,3

- Notes: 1. t_{RX_DQS2DQ} max delay variation as a function of temperature.
2. t_{RX_DQS2DQ} max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD} . It includes the V_{DDQ} and V_{DD} AC noise impact for frequencies >20 MHz and max voltage of 45mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement $V_{DDQ}=V_{DD}$ is assumed.
3. Absolute value of DQS to DQ offset.

Table 236: t_{RX_DQS2DQ} Offset Due to Temperature and Voltage Variation: 7200-8800

Parameter	Symbol	7200		7600		8000		8400		8800		Unit s	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS to DQ offset temperature variation	$t_{RX\_DQS2DQ\_temp}$	-	5.67	-	5.37	-	5.10	-	4.86	-	4.64	ps/ 10°C	1, 3
DQS to DQ offset voltage variation	$t_{RX\_DQS2DQ\_volt}$	-	22.50	-	21.25	-	20.00	-	19.00	-	18.00	ps/ 50mV	2, 3

- Notes: 1. t_{RX_DQS2DQ} max delay variation as a function of temperature.
2. t_{RX_DQS2DQ} max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD} . It includes the V_{DDQ} and V_{DD} AC noise impact for frequencies >20 MHz and max voltage of 45mVpk-pk from DC -20 MHz at a fixed temperature on the package. For tester measurement $V_{DDQ}=V_{DD}$ is assumed.
3. Absolute value of DQS to DQ offset.

Duty Cycle Adjuster

The device supports a mode register adjustable duty cycle adjuster (DCA) to enable the memory controller to adjust the internally generated DQS clock tree and DQ duty cycle to compensate for systemic duty cycle errors of all DQS and DQs.

The DQS DCA is located before the DQS clock tree or equivalent place. The DCA requires a locked DLL state and affects the DQS and DQ duty cycle during the following operations:

- Read
- Read preamble training
- Read training pattern
- Mode register read

The controller can adjust the duty cycle through all DCA mode registers and can determine the optimal mode register setting for DCA in numerous ways.

DCA Range

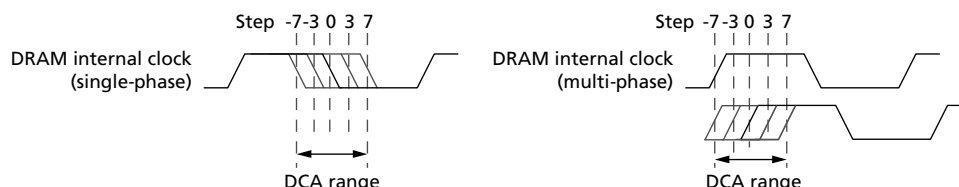
The global DCA step range is from -7 to +7, as defined in MR43 and MR44. The actual step size cannot be defined because the variation of duty cycle by changing DCA code is not linear.

Table 237: DCA Range

Parameter	Min/Avg/Max	Value	Unit	Notes
Duty cycle adjuster range	Min	28	ps	1
	Max	56		

Note: 1. These values are guaranteed by design

Figure 153: DCA Range



Relationship Between DCA Code Change and Single/2-Phase Internal Clock(s)/DQS Timing

In the case where the DQS clock tree is implemented in a single/2-phase clock(s) scheme, the duty/cycle ratio of all DQS per device can be adjusted directly according to the internal clock(s) controlled by the DCA code. DQSCK is not changed by a DCA code change.

Using a 2-phase clock scheme, the rising edge of the 0° clock is the reference edge, while the 180° clock is adjusted based on 0° clock. The rising edge of 0° clock is for even burst bit data, and the rising edge of 180° clock is for odd burst bit data.

The global DCA adjustment uses the DCA for single/two-phase clock(s) mode register bits (MR43:OP[3:0]). A positive DCA adjustment results in a larger duty cycle ratio, while a negative DCA adjustment results in a smaller duty cycle ratio.

In addition to the global DCA adjustment, a per-pin DCA adjustment allows an additional step range of -3 to +3, per DQS/DQ. The 2-phase clock per-pin DCA adjustment uses the OP bits [3,1:0] of MR103 (DQSL_t), MR105 (DQSL_c), MR107 (DQSU_t), MR109 (DQSU_c), MR133 (DQL0), MR141 (DQL1), ...,

MR253 (DQU7). The per-pin DCA adjustment is additive to the global DCA adjustment, as shown in the examples below:

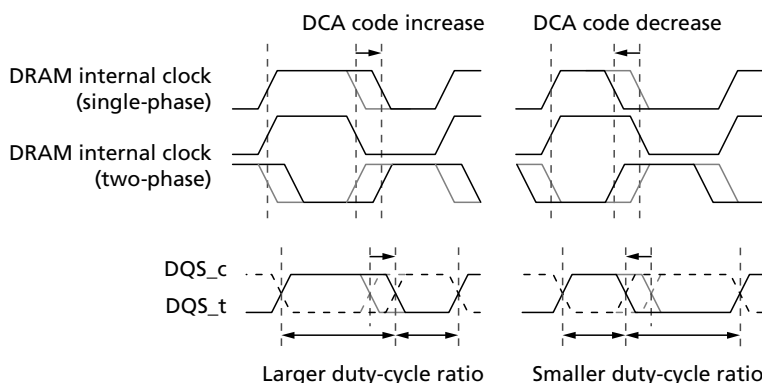
Table 238: DCA Range Examples (Not All Possible Combinations)

Global DCA Adjustment	Per-Pin DCA Adjustment	Total DCA Adjustment at Pin
DCA Step -3	DCA Step -2	DCA Step -5
DCA Step -2	DCA Step +2	DCA Step -0
DCA Step 0	DCA Step +1	DCA Step +1
DCA Step +2	DCA Step -3	DCA Step -1
DCA Step +4	DCA Step +3	DCA Step +7
DCA Step +7	DCA Step +2	DCA Step +9

Like the global DCA adjustment, the actual step size for the per-pin DCA adjustment cannot be defined because the variation of duty cycle by changing DCA code is not linear; however, the per-pin DCA adjustment is approximately the same as the global DCA adjustment.

Mode register OP bits associated with the IBCLK and QBCLK may not be supported on the device with a 2-phase clock scheme.

Figure 154: Example: DCA Code Change and Single/2-Phase Internal Clock(s)/DQS



Relationship Between DCA Code Change and 4-Phase Internal Clock(s)/DQS Timing

In the case where the DQS clock tree implemented in a 4-phase clocks scheme, the even and odd duty/cycle ratio of all DQS per device can be adjusted respectively because the internal 4-phase clocks can be independently controlled by the DCA code.

In case of 4-phase internal clocks, for example, because QCLK(90°)/IBCLK(180°)/QBCLK(270°) are adjusted based on ICLK(0°), the controller can first confirm the first BL is synchronized with ICLK(0°), and then perform the full DCA training operation, which needs to have an even number of MRR (or Read) - MRR (or Read) timing to avoid confusion whether the first BL is synchronized with ICLK(0°) or IBCLK(180°).

Figure 155: Relationship Between DCA Code Change for QCLK and the 4-Phase Internal Clock(s)/DQS Waveform

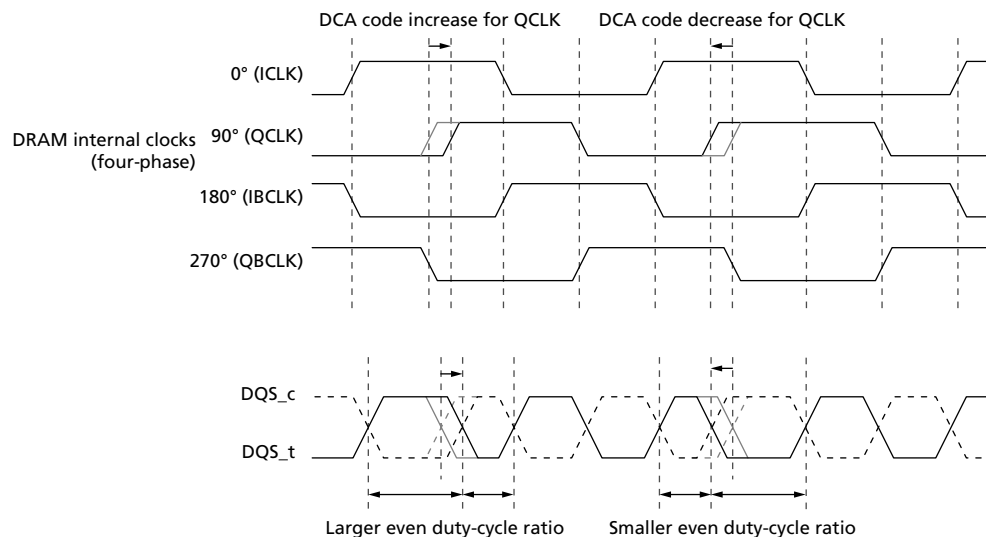


Figure 156: Relationship between DCA Code Change for IBCLK and the 4-Phase Internal Clock(s)/DQS

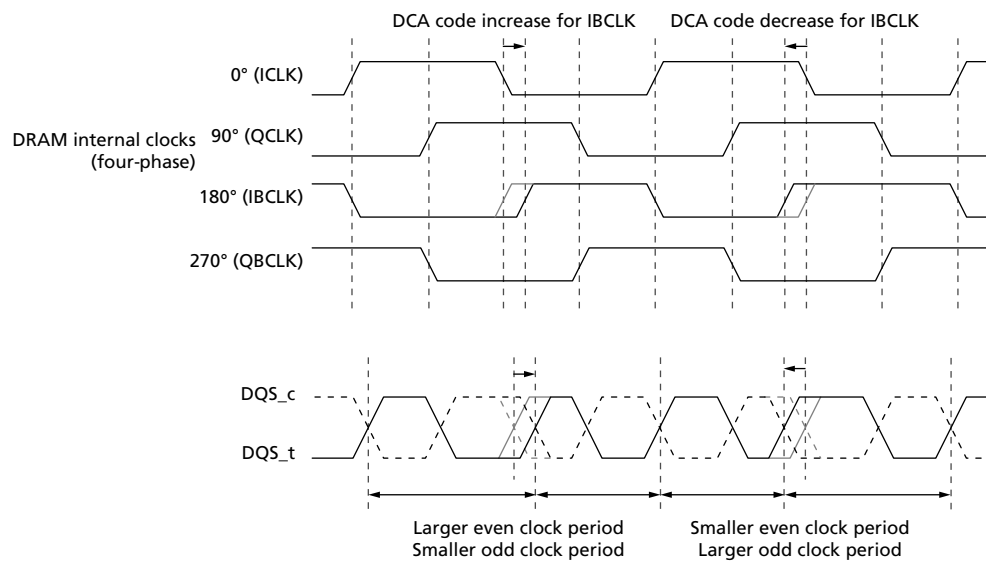
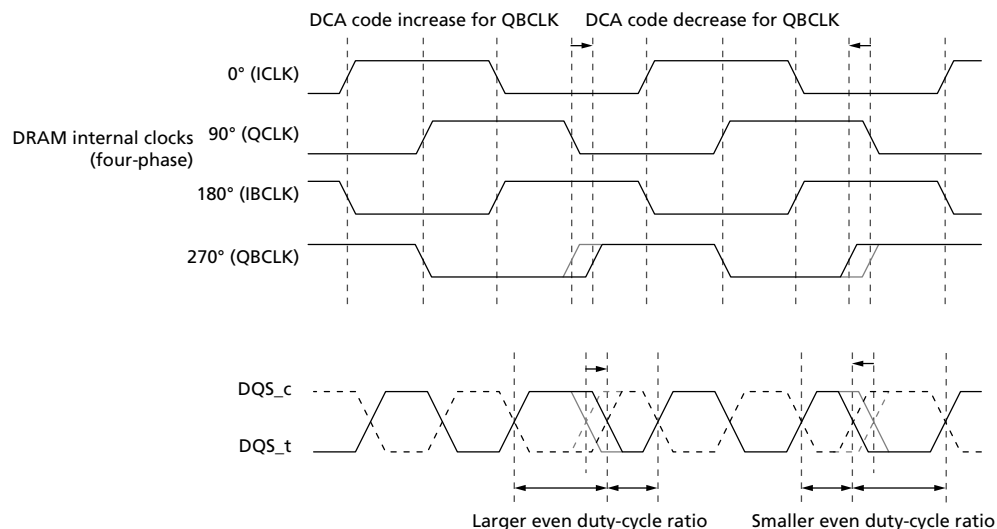


Figure 157: Relationship between DCA Code Change for QBCLK and the 4-Phase Internal Clock(s)/DQS



Relationship Between DCA Code Change and DQs Output/DQS Timing

The DQS DCA code change effect to DQ output is as follows. The rising edge of DQS_t affects the even data output. The falling edge of DQS_t affects the falling edge of the odd data output.

Decision Feedback Equalization

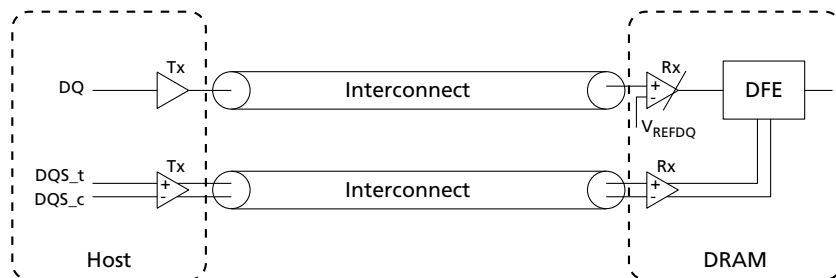
At data rates ≥ 2933 MT/s, signal degradation due to inter symbol interference (ISI) is expected to increase and the data eye at the device ball is expected to be closed. Because the memory channel is very reflective due to the many impedance mismatched points that exist along the memory subsystem, ISI due to reflections is expected to increase.

Traditional methods of characterizing the receiver using the input eye mask are no longer sufficient. DDR5 requires equalization to help improve (or open up) the data eyes after data is latched by the receiver. A 4-tap decision feedback equalization (DFE) helps equalize the DQ signals without amplifying the noise due to insertion loss and reflections, which is a common side effect of other equalization techniques (for example, CTLE). For ISI correction to occur, the Global DFE Gain and Tap (MR111) and per-pin DFE Gain and Tap (MR112-MR252) bits shall be enabled and properly configured for data rates ≥ 2933 MT/s. When the DFE is enabled, the DQs shall be high for a minimum of 4UI prior to the first write data bit to ensure proper DFE synchronization.

The figure below shows an example of a memory subsystem with DFE circuit included on the device.

For systems supporting data channel margins where the DFE is not required to improve signaling, the DFE can be disabled. Also, at the 1980-2100 MT/s data rates, the device's DFE is disabled. Setting either the global DFE gain and tap 1-4 enable bits to disable or setting all DFE gain and tap 1-4 bias bits to step 0 disables the DFE.

Figure 158: Memory Subsystem with DFE Circuit on the Device

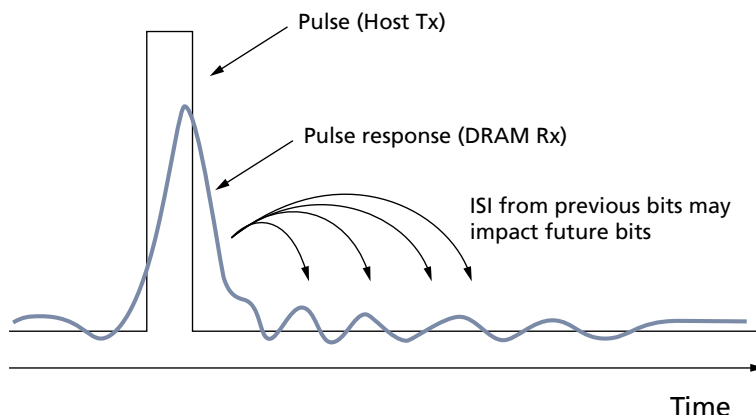


Pulse Response of a Reflective Memory Channel

A reflection-dominated channel, such as those found in a memory subsystem, is anticipated to substantially reduce data eye at the device ball due to the effects of insertion loss and reflections. The following figure illustrates what a pulse response of a very reflective channel might look like.

The attenuation, as well as the ringing of the signal, can cause the data eye to close at the device ball. Moreover, the ringing can impact future bits that are being sent into the channel (that is, if the pulse response is for bit n , then the ringing from bit n can impact the signal integrity of future bits $n+1$, $n+2$, $n+3$, $n+4$, etc). Phrased another way, the signal integrity of any bit (for example bit n) can be impacted by the signals of the previous bits ($n-1$, $n-2$, $n-3$, $n-4$, etc.).

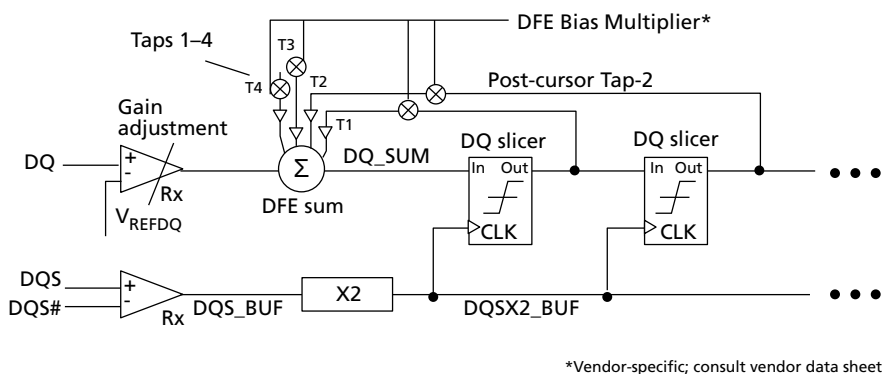
Figure 159: Pulse Response of a Reflective Channel



DFE Components

The 4-tap DFE subsystem consists of a gain amplifier, a DFE summer, four DQ slicers (also called taps) with outputs that loop back to the DFE summer, and a coefficient multiplier for each tap. The gain control of the front end is used to ensure the cursor or the current bit is in a congruent relationship with the ISI correction required for the channel. The taps T1, T2, T3, T4 coefficients provide the corrections needed to the current bit by adding or subtracting the effects of ISI of the previous bits.

Figure 160: 4-Tap DFE



The mode registers shown in the following tables are used by the memory controller to set the strengths of the gain amplifier and the strengths of the correction of the taps to adapt the ISI cancellation in accordance with the channel performance. Optimal values used for the strengths of the gain amplifier and of the taps are system-dependent, and are usually obtained through a combination of simulations, platform characterizations, and other methods.

Table 239: DFE Gain Adjustment MIN/MAX Ranges (3200-8800)

Description	3200-8800			Unit	Notes
	MIN	TYP	MAX		
DFE gain bias max	6	–	–	dB	1,2,3,4
DFE gain bias min	–	–	-6	dB	1,2,3,4
DFE gain bias average step size	-	2	-	dB	1,2,3,4

Table 239: DFE Gain Adjustment MIN/MAX Ranges (3200-8800) (Continued)

Description	3200-8800			Unit	Notes
	MIN	TYP	MAX		
DFE GAIN bias DNL	-1	–	+1	dB	1,2,3,4
DFE GAIN bias INL	-1	–	+1	dB	1,2,3,4
DFE gain bias tolerance time	^t DFE	-	-	ns	1,2,3,4

Notes: 1. All parameters are defined over the Rx V_{REF} range from $0.5 * V_{DDQ}$ to $0.9 * V_{DDQ}$.

2. DFE gain bias are for all voltage and temperature ranges.

3. These values are defined over the entire voltage and temperature ranges.

4. These parameters are to evaluate the relative ratio of DFE gain bias settings, and absolute values of all parameters are not subject to silicon validation or production tests.

Table 240: DFE Tap Coefficients MIN/MAX Ranges (3200-8800)

Description	3200-8800			Unit	Notes
	MIN	TYP	MAX		
DFE tap-1 bias max	50	–	–	mV	1,2,4,5,7
DFE tap-1 bias min	–	–	-200	mV	1,2,4,6,7
DFE tap-2 bias max	75	–	–	mV	2,4,5,7
DFE tap-2 bias min	–	–	-75	mV	2,4,6,7
DFE tap-3 bias max	60	–	–	mV	2,4,5,7
DFE tap-3 bias min	–	–	-60	mV	2,4,6,7
DFE tap-4 bias max	45	–	–	mV	2,4,5,7
DFE tap-4 bias min	–	–	-45	mV	2,4,6,7
DFE tap bias average step size	–	5	–	mV	2,3,4,7
DFE tap bias DNL	-2.5	–	+2.5	mV	2,3,4,7
DFE tap bias INL	-2.5	–	+2.5	mV	2,3,4,7
DFE tap bias step time	^t DFE	–	–	mV	2,3,4

Notes: 1. As speed increases, the impact of loss from the channel makes the bias range of the first cursor asymmetric.

2. Values are defined for the entire voltage, temperature range, and Rx V_{REF} range from $0.5 * V_{DDQ}$ to $0.9 * V_{DDQ}$.

3. Values are identical for taps 1-4.

4. These parameters are suggested to evaluate relative ratio of DFE taps 1~4, and absolute values of all parameters are not subject to silicon validation nor production test.

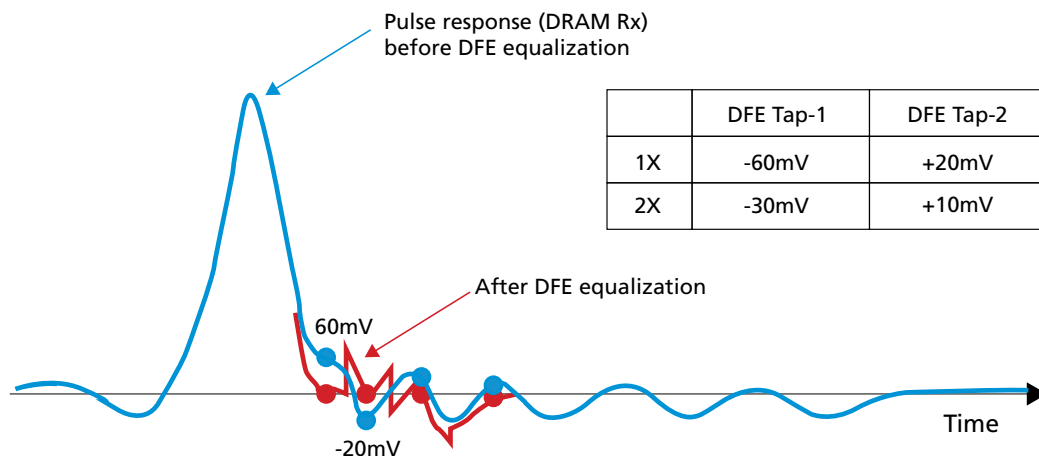
5. For the pulse response (...000010000... pulse pattern), a positive value corrects a negative post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to 0 to apply a positive correction.

6. For the pulse response (...000010000... pulse pattern), a negative value corrects a positive post-cursor by setting the DFE tab bias sign bit (MR113~116, OP[6]) to 1 to apply a negative correction. For example, in a memory channel where the ISI during the first post-cursor is dominated by bandwidth loss, the expected tap-1 bias sign bit will be set to 1.

7. Check the multiplier that is applied to the DFE tap bias setting (MR113, MR114, MR115, etc.) for total DFE feedback swing implemented in hardware.

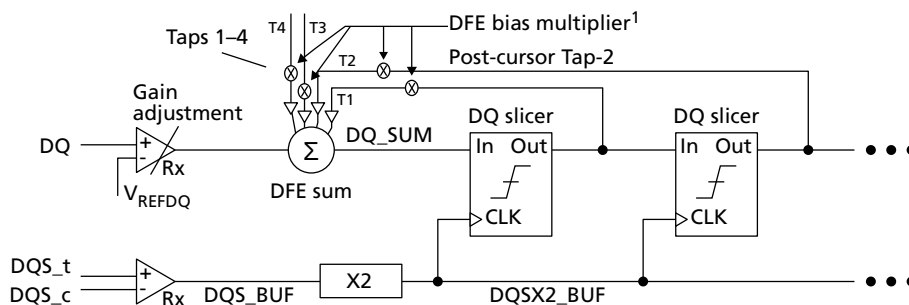
The figure below is an example of 1X and 2X multiplier cases which shows how the DFE tab biases move differently in hardware with the same pulse response.

Figure 161: Example Case of DFE Tap Biases Moving with 1X and 2X Multiplier



The device may implement 1-way interleave, 2-way interleave, or 4-way interleave 4-tap DFE memory circuitry. The 1-way interleaved 4-tap DFE architecture (shown below) requires a strobe multiplier, which is at Nyquist rate. The output of the DQ slicer runs at same speed as received data.

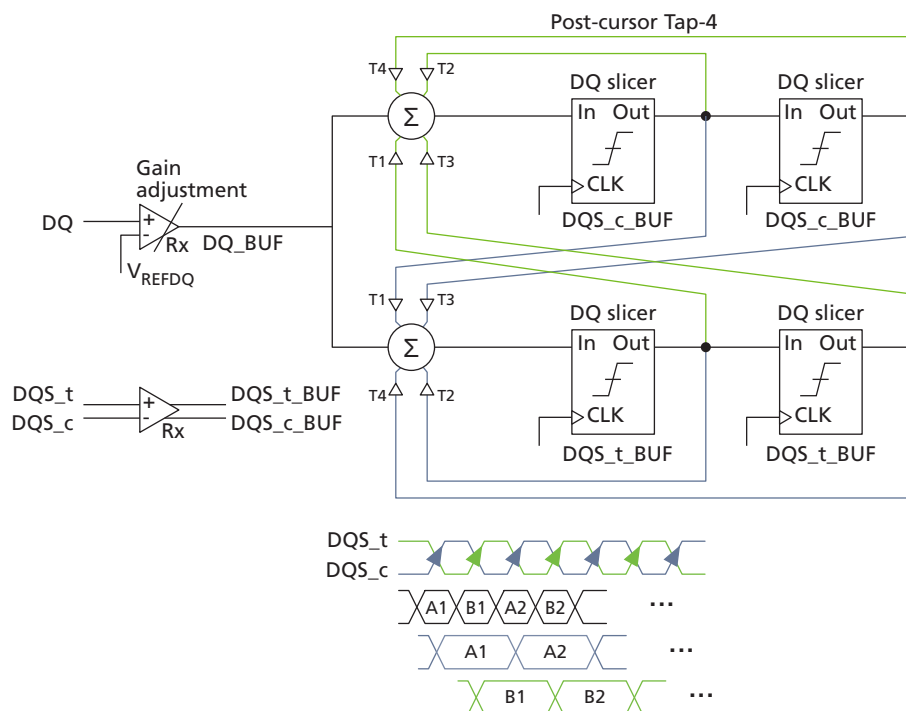
Figure 162: 1-Way Interleave 4-Tap DFE



Note: 1. Vendor-specific; consult vendor data sheet.

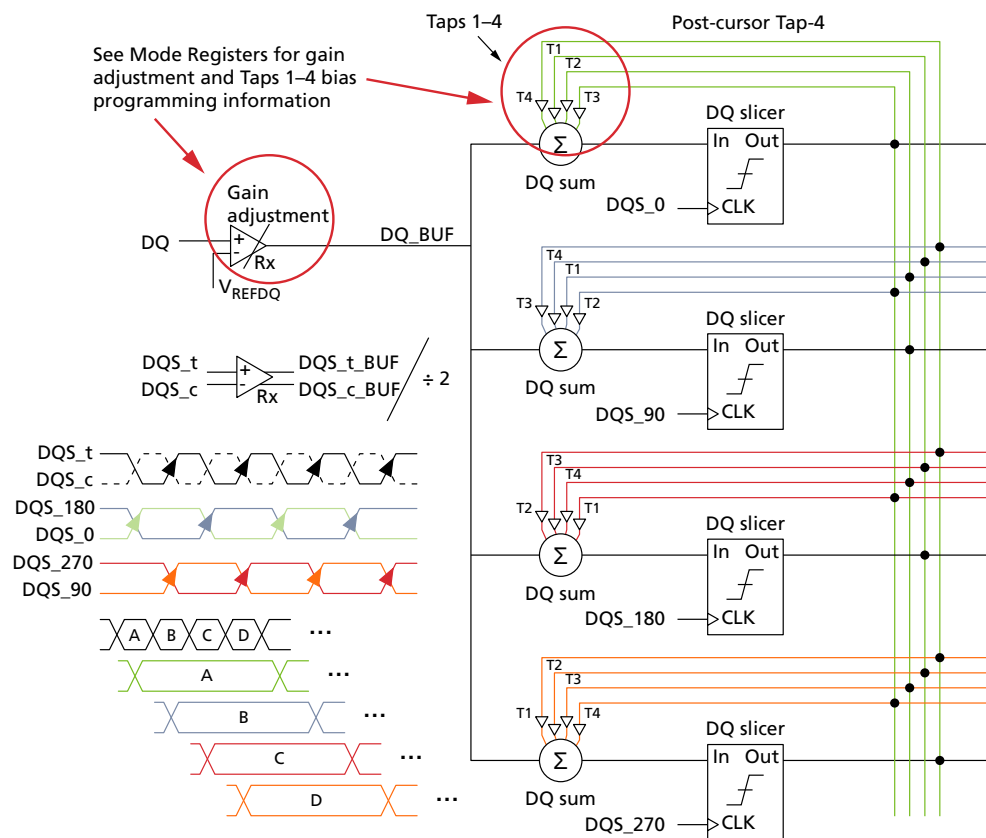
A 2-way interleave 4-tap architecture (shown below), can use the strobe as-is. In this case, the output of the DQ slicer runs at half the speed as received data.

Figure 163: 2-Way Interleave 4-Tap DFE



A 4-way interleave 4-tap architecture (shown below), requires a divided clock. In this case, the output of the DQ slicer runs at one-quarter the speed as received data.

Figure 164: 4-Way Interleave 4-Tap DFE



Loopback Mode

With loopback mode, the device feeds a received signal/data to an external receiver for multiple purposes. This mode enables the host (memory controller or test instrument) to monitor data sent to the device.

Loopback normal output mode requires data be sent to the loopback path before it is sent to the core so that READ/WRITE commands are not required for loopback to be operational (no data is stored in the array nor retrieved from the array). Alternatively, Loopback Write Burst Output Mode only generates loopback data on WRITE commands during normal operation, where data is written to the array. Additionally, there are inherent limitations when characterizing the receiver using statistical analysis methods such as bit error rate (BER) analysis. For example, at $BER=1E^{-16}$, the following occurs: there is not enough memory depth in the device to store all the $1E^{+16}$ data; the amount of time to perform multiple READ/WRITE commands to/from the memory is prohibitively long; because the amount of time involved performing these operations is much longer than the refresh rate interval, the host or memory controller must also manage refreshes during testing to ensure data retention; and, limited pattern depth means limited inter symbol interference (ISI) and limited random jitter (Rj), and therefore, limited errors at the receiver.

Use of loopback is a necessity for characterizing the receiver without the limitations and complexities of other traditional validation methods. Loopback can also be used during normal operation, as described in the Loopback Write Burst Output Mode section below.

Loopback Output Definition

Loopback requires two output pins: one single-ended loopback strobe (LBDQS) and one single-ended loopback data (LBDQ).

The default RTT state for loopback is RTT_OFF, designated by MR36:OP[2:0] = 000b. In this state, both the LBDQS and LBDQ outputs are disabled. If the loopback pins of several DDR5 devices are connected together and the end device needs termination, there is a RZQ/5 (48 ohms) option available by setting MR36:OP[2:0] = 101b.

Selecting a loopback output value via MR53:OP[4:0] other than the default loopback disabled (MR53:OP[4:0] = 00000b) results in the LBDQS and LBDQ pins transitioning from RTT_OFF to a device drive state.

Before changing the loopback output select from upper byte to lower byte or vice versa, the host must set loopback output select to MR53:OP[4:0]=00000b to disable loopback mode.

The LBDQS output transitions with the differential input crossing point of DQS_t/DQS_c for x4 and x8 device configurations, plus latency. LBDQS transitions with DQSL_t/DQSL_c for x16 devices if DML or a DQL is selected for output, or with DQSU_t/DQSU_c for x16 devices if DMU or a DQU is selected for output. If an RFU output is selected, or if DMU or a DQU is selected on a x4 or x8 device where DQSU_t/DQSU_c is not valid, LBDQS remains in a device drive state.

The LBDQ output transitions with the receiver data state of the DM or DQ pin selected by MR53:OP[4:0]. If an RFU output is selected, or if an invalid output for device configuration is selected, the LBDQ output remains in a device drive state.

Table 241: Loopback Output Definition

Condition	LBDQS	LBDQ	Notes
Loopback disabled	RTT_Loopback	RTT_Loopback	
Loopback enabled	Selected phase	Selected phase and selected DQ	1

Note: 1. Selection of an unsupported RFU/DM/DQ for the device configuration results in undefined LBDQS toggling and the LBDQ in a driven state.

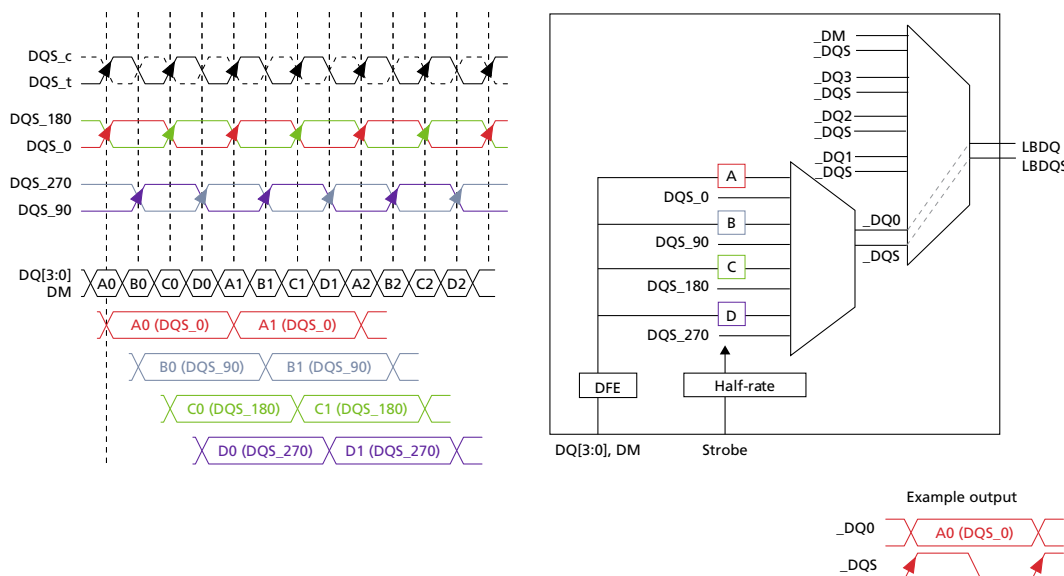
Loopback Phase

Due to the high data rates of the device, loopback may be implemented with 2-way or 4-way interleaved outputs. With a 2-way implementation, the DQS and selected DM/DQ are sampled and output every 1CK or 2UI. Similarly, with a 4-way implementation, the DQS and selected DM/DQ are sampled and output every 2CK or 4UI.

To be able to sample all bits with a 2-way or 4-way interleave implementation, the loopback select phase programmed in MR53:OP[6:5] allows selection of the DQS/DM/DQ phase to be output. In 2-way mode, Phase A and Phase B are valid options. In 4-way mode, Phase A, Phase B, Phase C and Phase D are valid options.

The figure below shows an example loopback implementation for a four-way interleave x4 device. This example requires a divided clock to produce DQS_0, DQS_90, DQS_180 and DQS_270. Phase A-D refers to the four-bit naturally aligned bits in a data stream. The output of the DQ slicer runs at one-quarter the speed as received data. In a four-way interleave design, the data is received at full speed, but internally the data is latched only at quarter speed. For example, if the input bit stream consists of A, B, C, and D, the multiplexer input A receives data bit A and strobe DQS_0; multiplexer input B receives data bit B and strobe DQS_90; multiplexer input C receives data bit C and strobe DQS_180; and multiplexer input D receives data bit D and DQS_270.

Figure 165: Example: Four-Way Interleave Loopback Circuit on a x4 Device



Loopback Output Mode

Loopback output mode selects whether to output LBDQS and LBDQ in normal output mode or write burst output mode, based on MR53:OP[7]. In the default normal output mode (MR53:OP[7] = 0b), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected loopback phase. In write burst output mode (MR53:OP[7] = 1b), the selected DM/DQ state is output on LBDQ when qualified by the write enable, which means data is only captured during the write burst and not during the preamble or postamble.

Loopback Normal Output Mode (Default)

In normal output mode (MR53:OP[7] = 0b), the selected DM/DQ state is captured with every DQS_t/DQS_c toggle for the selected loopback phase and output on LBDQ. The LBDQS output is delayed by t_{LBDLY} from the selected DQS_t/DQS_c loopback phase. Phase C and D are inverted from Phase A and B, respectively. Since no WRITE commands are required in normal output mode, MR settings

pertaining to preamble, postamble, and CWL are ignored by the loopback function. Additional requirements for normal output mode:

- Loopback in normal output mode is not supported after completing write leveling training with internal write timing mode set MR2:OP[7]=1.
- DQS must be driven differentially LOW (DQS_t low, DQS_c high) prior to entry into normal output mode.
- DQS_t/DQS_c must be continuously driven during loopback operation. (HiZ state not allowed.)
- Only DSEL and MRW commands applied at command pins during normal output mode.
- RESET is required to exit loopback normal output mode.

No DFE reset is assumed after first rising edge of DQS_t. Device array data is not guaranteed after entering normal output mode.

Loopback Normal Output Mode Timing Diagrams

Figure 166: Loopback Normal Output Mode Entry

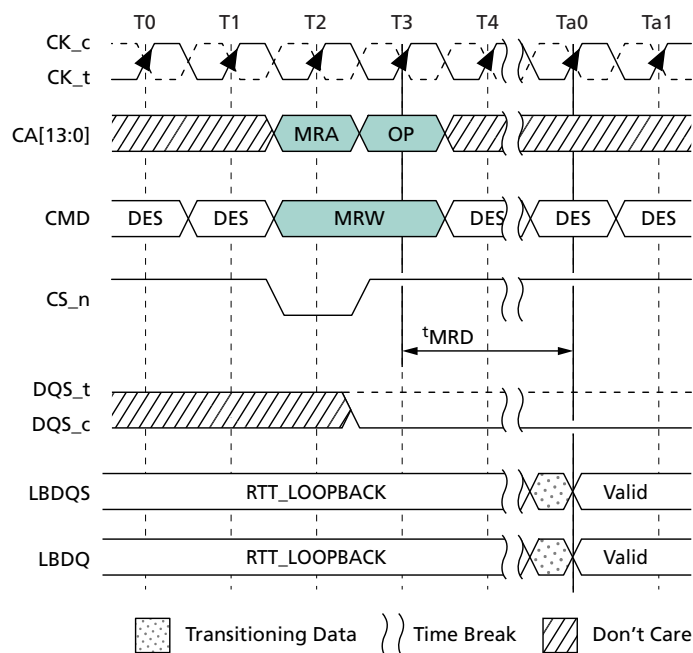
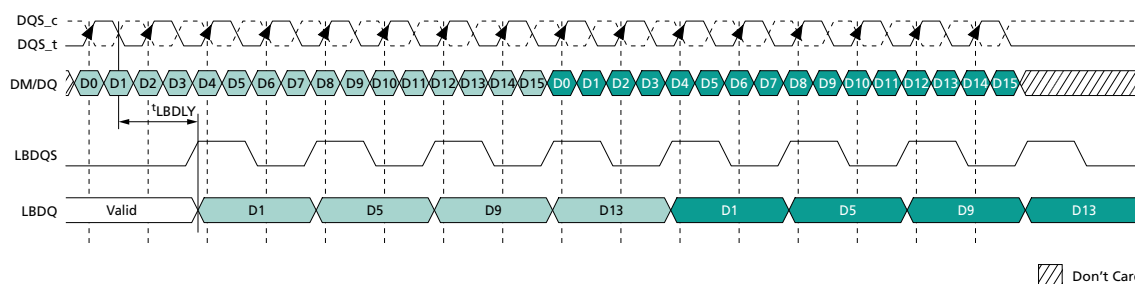


Figure 167: Loopback Normal Output 4-Way Mode Phase B Example

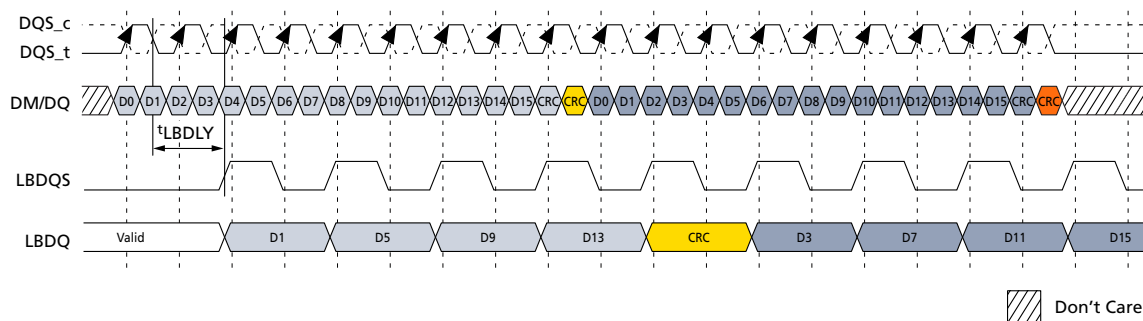


Timing diagram for the LBDQ signal. The diagram shows the relationship between DQS_c, DQS_t, DM/DQ, LBDQS, and LBDQ. DM/DQ is a bus where data is written in bursts of 4 (D0-D3, D4-D7, etc.) and read in bursts of 4 (D0-D3, D4-D7, etc.). LBDQS is a strobe signal that is high during write bursts and low during read bursts. LBDQ is the data bus, which is valid during write bursts and contains data during read bursts. The diagram shows that LBDQ is valid during the LBDQS high periods and contains data during the LBDQS low periods. A legend indicates that hatched areas represent 'Don't Care'.

Timing diagram for LBDQ and LBDQS signals. The diagram shows two data bursts. The first burst starts with DM/DQ signals (D0-D15) and LBDQS (triangular pulses). LBDQ is 'Valid' until the first LBDQS pulse, then shows data D1, D5, D9, and D13. The second burst is similar, with LBDQ showing D1, D5, D9, and D13. A legend indicates that hatched areas represent 'Don't Care'.

The diagram shows the timing of the LBDQ signal relative to the LBDQS signal and the DM/DQ bus. The DM/DQ bus contains data elements D0 to D15, with some elements marked as 'Don't Care'. The LBDQS signal is a strobe signal with a period of 1 LBDLY. The LBDQ signal is valid during the LBDLY period. The diagram illustrates the timing of the LBDQ signal relative to the LBDQS signal and the DM/DQ bus.

Figure 171: Loopback Normal Output 4-Way Mode Phase B with CRC, No Gap



- All write timing and voltage requirements must be followed. Failure to meet this requirement results in unknown data written to the device, and the loopback pins may not output the captured input data as expected.

Loopback Write Burst Output Mode Timing Diagrams

The DM/DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

Figure 174: Loopback Write Burst Output 4-Way Mode Phase B WPRE = 2CK Example

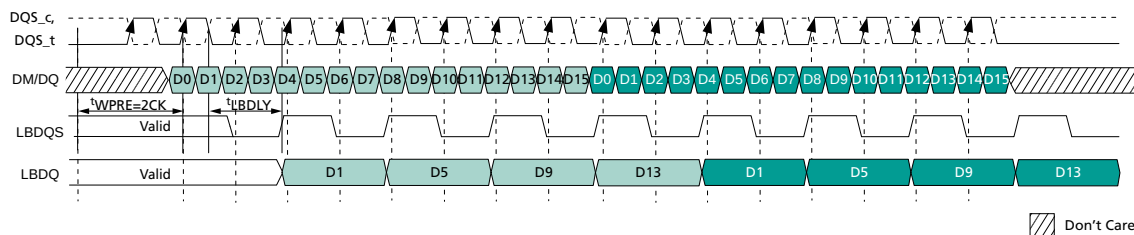


Figure 175: Loopback Write Burst Output 4-Way Mode Phase C WPRE = 2CK Example

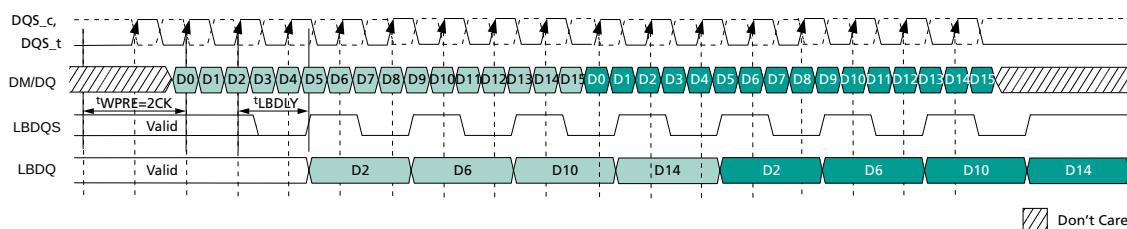


Figure 176: Loopback Write Burst Output 4-Way Mode Phase B Data Burst Bit and Phase D Strobe Alignment WPRE = 4CK Optional Example

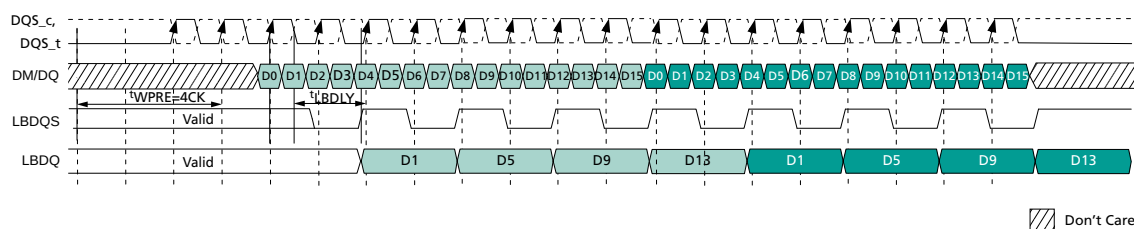
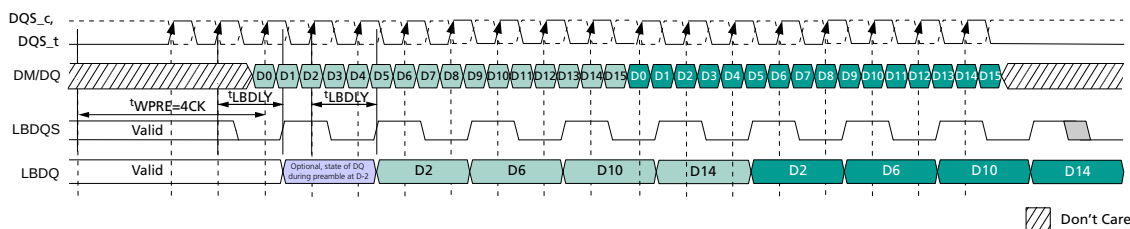


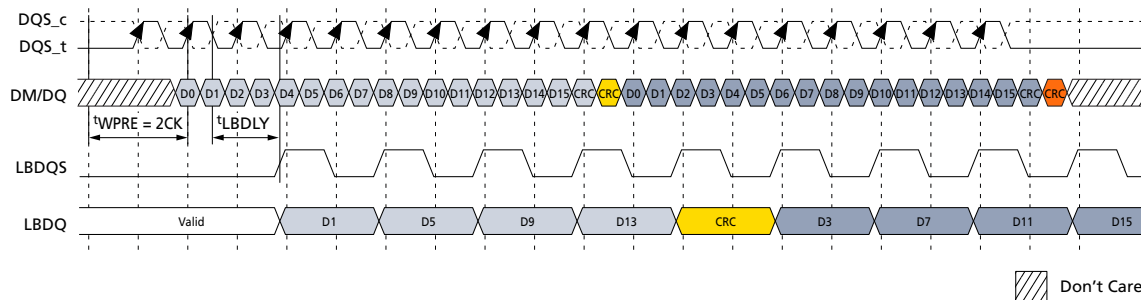
Figure 177: Loopback Write Burst Output 4-Way Mode Phase C Data Burst Bit and Phase A Strobe Alignment WPRE = 4CK Optional Example



Loopback Write Burst with CRC Output Mode Timing Diagrams

The DM/DQ signal is shown as Don't Care before the first write data bit indicating DFE is disabled. When DFE is enabled, the DM/DQ signal shall be high for a minimum of 4UI prior to the first write data bit for proper DFE synchronization.

Figure 178: Loopback Write Burst with CRC Output Mode 4-Way Phase B with CRC, No Gap



Loopback Timing and Levels

The LBDQS output is delayed from the selected DQS_t/DQS_c loopback phase. The timing parameter (t_LBDLY) is shown in the following table.

Table 243: Loopback LBDQS Output Timing (3200-8800)

Speed		3200-8800		Unit
Parameter	Symbol	MIN	MAX	
Loopback Timing: LBDQS Delay from selected DQS loopback phase	t _{LBDLY}	-	20	ns

The interaction between LBDQS and LBDQ is described in the Loopback Output Timing section. ODT for loopback is described in the On-Die Termination for Loopback Signals section. Output driver electrical characteristics for loopback is described in the [Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ](#) section.

Cyclical Redundancy Check

CRC Polynomial and Logic Equation

The device supports cyclical redundancy check (CRC) for READ and WRITE operations, enabled by separate mode register bits. Write CRC and data mask (DM) functions are not supported simultaneously and cannot be enabled together.

The CRC polynomial is the ATM-8 HEC, X^8+X^2+X+1

A combinatorial logic block implementation of this 8-bit CRC for 64-bits of data contains 242 two-input XOR gates contained in eight 6 XOR gate deep trees.

Table 244: Error Detection Details

Error Type	Detection Capability
Random single-bit error	100%
Random double-bit error	100%
Random odd count error	100%
Random multi-bit error within two adjacent transfers	100%

CRC Combinatorial Logic Equations

```

module CRC8_D64;
// polynomial: (0 1 2 8)
// data width: 64
// convention: the first serial data bit is D[63]
// initial condition all 0 implied
function [7:0]
nextCRC8_D64;
input [63:0] Data;
reg [63:0] D;
reg [7:0] NewCRC;
begin
D = Data
;
NewCRC[0] = D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0];
NewCRC[1] = D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[63] ^ D[62] ^ D[61] ^ D[59] ^
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];

```

```

NewCRC[4] = D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D64 = NewCRC;

```

CRC Data Bit Mapping

The following figures show detailed bit mapping for x4, x8, and x16 devices. This bit mapping is common between WRITE and READ CRC operations.

Figure 179: x4 Devices

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Figure 180: x8 Devices

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Note: 1. The CRC of a x8 device is like that of two x4 devices, each nibble with identical CRC trees.

Figure 181: x16 Devices

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	d32	d36	d40	d44	d48	d52	d56	d60	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	d33	d37	d41	d45	d49	d53	d57	d61	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	d34	d38	d42	d46	d50	d54	d58	d62	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	d35	d39	d43	d47	d51	d55	d59	d63	CRC3	CRC7

Note: 1. The CRC of a x16 device is like that of four x4 devices, each nibble with identical CRC trees.

Write CRC for x4, x8 and x16 Devices

The controller generates the CRC checksum and forms the write data frames.

For x8 devices, write CRC can be enabled or disabled independently per nibble. Two separate write CRC enable MR bits (for upper and lower nibbles) are defined. When at least one of two write CRC enable bits is set to 1, the timings of write CRC enable mode are applied to the entire device (both nibbles). When write CRC is enabled in one nibble and disabled in the other nibble in x8, the device does not check CRC errors on the disabled nibble; therefore, the ALERT_n signal and any internal status bit related to the CRC error is not impacted by the disabled nibble.

For x4 and x16 devices, only one of two write CRC enable bits is used, as defined in the mode register 50 table and notes. The unused write CRC enable bit is don't care (MR50:OP[2] is LOW).

The device checks for an error in received code words per each write CRC-enabled nibble by comparing the received checksum against the computed checksum. Errors are reported using the ALERT_n signal if there is a mismatch in any nibble.

The device can write data to the core without waiting for a CRC check for full writes. If bad data is written to the core, as identified by the CRC match and signaled on ALERT_n, the controller retries the transaction and overwrites the bad data. The host controller is responsible for data coherency.

When write CRC is enabled, there is no write latency adder.

Write CRC Auto-Disable

Write CRC auto-disable mode is enabled by programming the write CRC auto-disable mode enable bit MR50:OP[4] to 1.

When enabled, the device counts the number of write CRC error occurrences per device, regardless of configuration (x4, x8, and x16). When the number of write CRC errors occurring within the write CRC

auto-disable window exceeds the write CRC auto-disable threshold (between 0 and 127) as programmed in MR51:OP[6:0], the device disables write CRC error checking of all nibbles and sets the write CRC auto-disable status bit MR50:OP[5] to 1. To exceed the write CRC auto-disable threshold, the number of write CRC errors must occur within the write CRC auto-disable window described below.

After the CRC auto-disable threshold is reached, the device does not drive ALERT_n LOW on subsequent Write CRC errors until Write CRC error checking is re-enabled. However, due to internal timing constraints, the device may drive ALERT_n LOW on the first CRC error that exceeds the CRC auto-disable threshold. Additionally, if the CRC auto-disable threshold is reached and the device was already driving ALERT_n to LOW due to the current or a previous Write CRC error, ALERT_n may be released upon satisfying CRC_ALERT_PW_min.

Unless the write CRC auto-disable status bit is set, the write CRC error counter is reset after the predetermined number of writes between 0 and 127, where 0 means an infinite window), as programmed in MR52:OP[6:0] so that the write CRC error count will accumulate during each write CRC auto-disable window. After the write CRC auto-disable status bit is set, the write CRC error checking is not re-enabled at the end of the write CRC auto-disable window, even though the write CRC error counter is reset below the threshold value.

Write CRC error checking can be re-enabled by resetting the write CRC auto-disable status bit MR50:OP[5] to 0. This will reset the write CRC error counter and restart the write CRC auto-disable window

Prior to changing the write CRC auto-disable threshold as programmed in MR51:OP[6:0] or the write CRC auto-disable window as programmed in MR52:OP[6:0], the host must disable the write CRC auto-disable mode (MR50:OP[4]=0). After the updated values have been programmed in MR51 and/or MR52, write CRC auto-disable mode can be (re)enabled (MR50:OP[4]=1). Disabling the write CRC auto-disable mode, if enabled, resets the write CRC error counter and restarts the write CRC auto-disable window. However, if the write CRC auto-disable status bit had previously been set to 1 (MR50:OP[5]=1), the host is required to set MR50:OP[5]=0 to resume error counting.

Changes to the write CRC auto-disable threshold (MR51) and window (MR52) settings are only allowed when the CRC write auto-disable mode is disabled (MR50:OP[4]=0).

When write CRC auto-disable mode is disabled (MR50:OP[4]=0), write CRC error counters may remain at reset values even if write CRC errors occur.

Read CRC for x4, x8 and x16 Devices

The device generates the read CRC checksum and forms the read data frames as shown in the CRC data bit mapping tables described above. The controller can check for an error in received code words per nibble by comparing the received checksum against the computed checksum. If there is a mismatch in any of nibbles, the controller may retry the transaction.

Read latency adder when read CRC is enabled depends on data rate, as shown below.

Table 245: Read CRC Latency Addr

Data Rate (MT/s)	Read CRC Latency Adder ("CK)
1980 MT/s ≤ Data Rate ≤ 2100 MT/s	0
2933 MT/s ≤ Data Rate ≤ 6000 MT/s	0
6000 MT/s < Data Rate ≤ 8800 MT/s	2

The host must accordingly update MR0:OP[7:2] with the Read CRC Latency Adder when Read CRC is enabled.

CRC Burst Order

When write CRC is enabled, the CRC bits are calculated based on the sequential burst address order of the write data for the WRITE command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T' or '8,9,A,B,C,D,E,F,T,T,T,T,T,T,T' in BC8 OTF.

When read CRC is enabled, the device's CRC generator overrides the CA burst order bits C3 and C2 to '00', and CRC bits are calculated based on the sequential burst address order of the read data for the READ command. This sequential order is '0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F' in BL16, and '0,1,2,3,4,5,6,7,T,T,T,T,T,T,T' or 'T,T,T,T,T,T,T,8,9,A,B,C,D,E,F' in BC8 OTF. The override values do not modify the actual data burst ordering, and are only used for the CRC calculations. Actual data burst follows the burst order as indicated by C3 and C2 in the READ command.

Write CRC Error Handling

When the device detects a CRC error on received code words in any nibble, it drives the ALERT_n signal to 0 for 12-20 clocks.

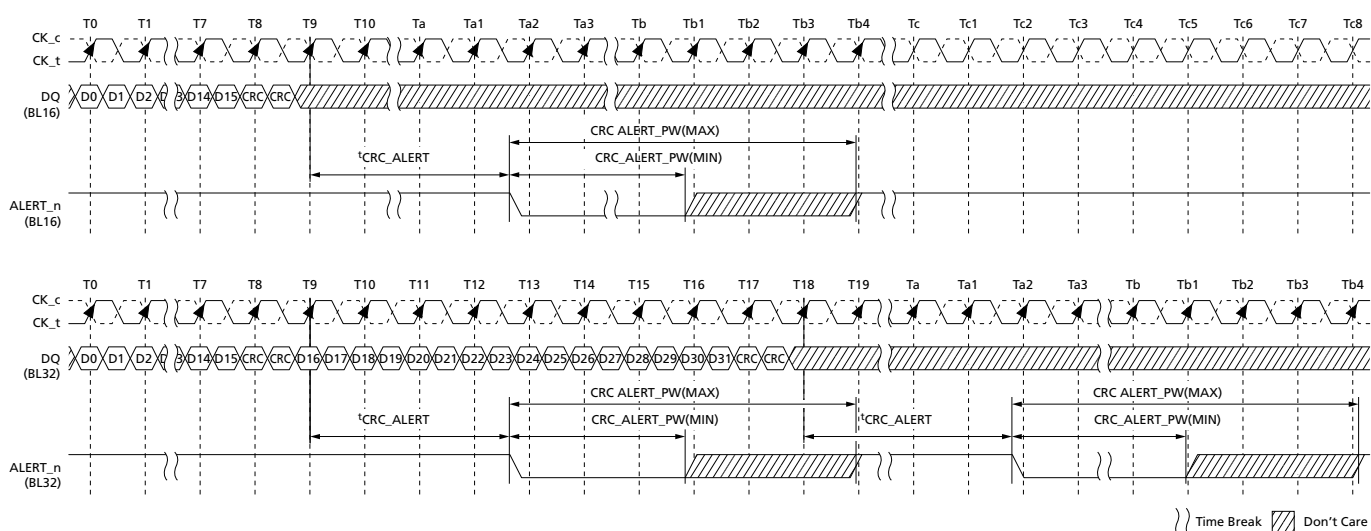
The latency-to-ALERT_n signal is defined as ^tCRC_ALERT in the figure below.

When a write CRC error is detected, the device sets the write CRC error status bit in MR50:OP[3] to 1. The write CRC error status bit remains 1 until the host clears it explicitly using an MRW command.

Upon seeing an error as a pulse width, the controller retries the write transactions. The controller understands the worst-case delay for ALERT_n (during initialization) and can backup the transactions accordingly, or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than 20 clocks at the controller if there are multiple CRC errors, as the ALERT_n is a daisy chain bus.

Figure 182: CRC Error Reporting



- Notes: 1. CRC ALERT_PW is specified from the point where the device starts to drive the signal LOW to the point where the device driver releases and the controller starts to pull the signal up.
2. Timing diagram applies to x4, x8, and x16 devices.

CRC Frame Format with BC8 OTF

CRC bits are always transferred on 17th and 18th UI in BC8 OTF mode. When read CRC is enabled during BC8 OTF read, DQ bits are driven HIGH and DQS is toggled by the device during the chopped data bursts. When write CRC is enabled during BC8 OTF write, DQ bits must be driven HIGH and DQS must be toggled by the controller during the chopped data bursts. In BC8 OTF mode, read CRC and write CRC bits are calculated with the inputs to the CRC engine for the chopped data bursts replaced by all 1s.

Figure 183: x4 Device CRC Bit Mapping in BC8 OTF Mode

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

For a x4 device, the CRC tree input is 32 data bits as shown in the table above. The input for the remaining bits are 1.

CRC data bit mapping for x8 devices (BC8 OTF).

Figure 184: x8 Device CRC Bit Mapping in BC8 OTF Mode

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

For a x8 device, the CRC tree inputs are two groups of 32 bits as shown in the table above. The inputs for the remaining bits are 1.

Figure 185: x16 Device CRC Bit Mapping in BC8 OTF Mode

	Transfer																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
DQ0	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ1	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ2	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ3	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ4	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ5	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ6	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ7	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ8	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ9	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ10	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ11	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7
DQ12	d0	d4	d8	d12	d16	d20	d24	d28	1	1	1	1	1	1	1	1	CRC0	CRC4
DQ13	d1	d5	d9	d13	d17	d21	d25	d29	1	1	1	1	1	1	1	1	CRC1	CRC5
DQ14	d2	d6	d10	d14	d18	d22	d26	d30	1	1	1	1	1	1	1	1	CRC2	CRC6
DQ15	d3	d7	d11	d15	d19	d23	d27	d31	1	1	1	1	1	1	1	1	CRC3	CRC7

For a x16 device, the CRC tree inputs are four groups of 32 bits as shown in the table above. The inputs for the remaining bits are 1.

CRC Bit Mapping in BL32 Mode

In BL32 mode, CRC bits are calculated separately for the first and second halves of the data. CRC bits for the first half of data are transferred on 17th and 18th UI. CRC bits for the second half of data are transferred on the 35th and 36th UI.

ECC Transparency and Error Scrub

The ECC transparency and error scrub feature incorporates an ECC error check and scrub (ECS) mode with an error counting scheme for transparency. ECS mode enables the device to internally read data bits, correct single bit errors, and write back corrected data bits (scrub errors) to the array while providing transparency to error counts. ECS mode contains two options set via the mode register:

- Manual ECS mode (MR14:OP[7] = 1b): enables ECS operations via the multi-purpose command.
- Automatic ECS mode (MR14:OP[7] = 0b) (default): allows for an optional automatic ECS mode to run internally.

ECS is available on all device configurations.

ECS mode implements two counters to track ECC code word errors detected during operation: error counter (EC) and errors per row counter (EpRC).

EC defaults to counting rows with errors; however, it may also be configured to count code words with errors. In row mode (default), EC tracks the number of rows that have at least one code word error detected, subject to a threshold filter. In code word mode, EC tracks the total number of code word errors, also subject to the threshold filter. EpRC, tracks the error count of the row with the largest number of code word errors along with the address of that row. EpRC error reporting is also subject to a separate threshold filter.

A general functional block diagram example of the ECS Mode operation is shown in the figure below while the ECC Error Checking and Scrub mode, Mode Register (MR14), is shown in the following table below.

Figure 186: Functional Block Diagram Example: ECS Mode

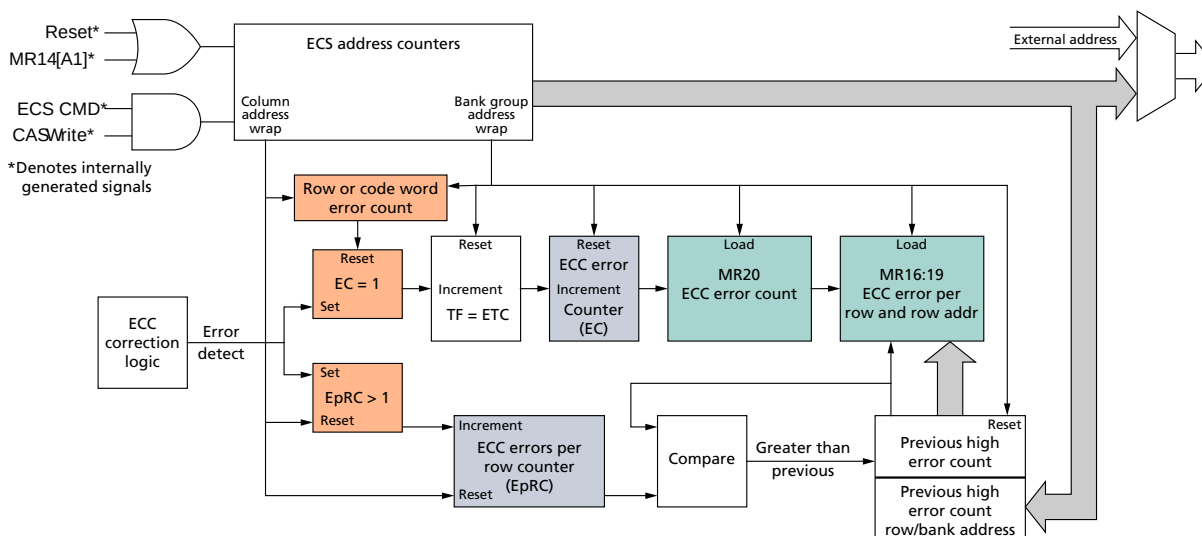


Table 246: Mode Register: ECS Mode

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
14	ECS mode	Reset ECS counters	Code-word/row count mode	RFU	CID3	CID2	CID1	CID0

Note: 1. CID[3:0] are used for 3DS devices only. For mono devices, set CID[3:0] to 0.

Mode Register and Device Initialization Prior to ECS Mode Operation

The ECC transparency and error scrub counters are set to zero. Internal ECS address counters are initialized by a RESET command or by manually writing MR14[6] = 1b. While MR14:OP[6] = 1b, ECS counters are reset and no additional ECS operations will occur. If a manual reset via mode register is utilized, MR14:OP[6] must be written back to 0 before any subsequent ECS operations will continue or a subsequent reset can be applied.

ECS mode register selections, automatic ECS in self-refresh (MR15:OP[3]), ECS threshold filter (MR15:OP[2:0]), manual/automatic ECS mode (MR14:OP[7]), and row/code word mode (MR14:OP[5]) must be programmed during device initialization and must not be changed once the first ECS operation occurs, unless followed by issuing a RESET or ECS RESET COUNTERS; otherwise, an unknown operation could result during subsequent ECS operations.

An ECS RESET COUNTERS operation requires setting MR14:OP[6]=1b to reset MR16 - MR20. Setting MR14:OP[6]=0b is then required to re-enable manual or automatic ECS operations.

Manual ECS mode is enabled by MR14:OP[7] = 1b. A manual ECS operation requires an MPC command with OP[7:0]=0000 1100b.

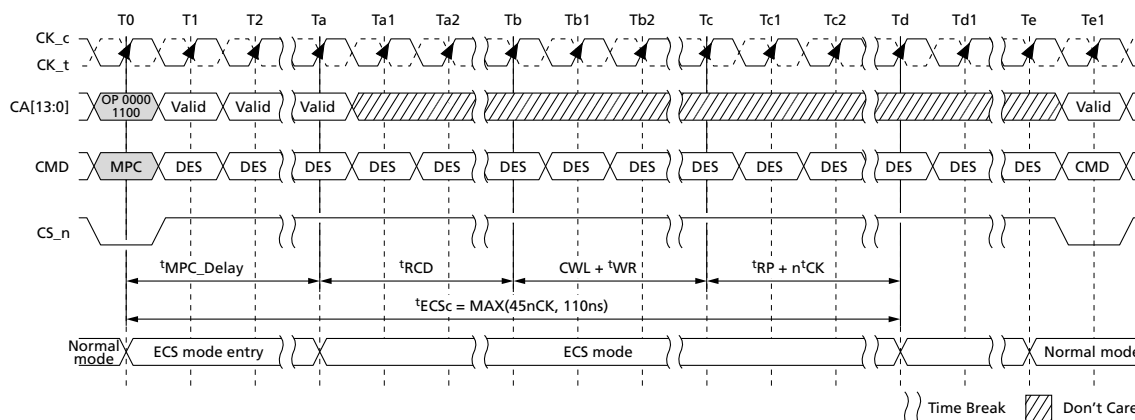
The device must have all array bits written to prior to executing ECS operation to avoid false failures.

ECS Operation

All banks must be precharged and in an idle state prior to executing a manual ECS operation.

Executing a manual ECS operation (MPC command with OP[7:0]=0000 1100b) generates the following internally self-timed command sequence: ACT--> RD --> WR --> PRE. ECS operation example timing shown in the figure below.

Figure 187: ECS Operation Timing Diagram



The minimum time for the ECS operation to execute is t_{ECS} ($t_{MPC\_Delay} + t_{RCD} + CWL + t_{WR} + t_{RP} + n^tCK$). n^tCK is required to satisfy t_{ECS} .

Upon execution of a manual ECS operation, DQs remain in RTT_PARK and DQS in DQS_RTT_PARK. The only commands allowed other than DES during t_{ECS} for a manual ECS operation are ODT NT commands, which may change the DQ and DQS termination state. Any illegal usage of manual ECS mode (for example, refresh or temperature violations) results in operation not being guaranteed.

Executing a manual ECS operation using an MPC command with OP[7:0]=0000 1100b will issue an internally timed ACT command (row activation) based on the internal ECS address counters' row address, (t_{MPC_Delay}) after the MPC command. The ACT command should be followed by a WR command t_{RCD} later. The WR command performs an internal read-modify-write cycle on the code word determined by the internal ECS address counters' column address.

The internal read-modify-write cycle:

- Reads the entire code word (128 data bits and 8 check bits) from the array.
- Corrects a single bit error in the code word or check bits, if an error is detected.
- Writes the resultant code word back to the device array.

The WR command is followed by a PRE command $CWL + {}^tWR$ later. The PRE command automatically re-enables the device I/Os and address inputs, and it returns the device to idle mode (${}^tRP + {}^nCK$) after ${}^tECS$ is satisfied.

For each ECS operation, ECS address counters increment the column address after each internal ECS WR command, such that the next code word and check bits are selected. Once the column counter wraps (all code words and check bits on the row have been accessed), the row counter increments until all code words on each of the rows within a bank are accessed. When the row counter wraps (all rows within the bank have been accessed), the bank counter increments and the next bank within a bank group repeats the process of accessing each code word. When the bank counter wraps, the bank group counter increments and the next bank group repeats the process of accessing each code word, until all bank groups have been accessed.

After all the code words within the device are read, corrected and written once, the bank group counter wraps and the process begins again with the next manual ECS operation. The total number of manual ECS operations required to complete one cycle of error check and scrub is density and configuration dependent, as listed in the table below. The controller must track the number of manual ECS operations to complete a full scrub of the device.

Table 247: Number of Code Words Per Device

Configuration	8Gb	16Gb	24Gb	32Gb	64Gb
x4, x8, x16	2^{26}	2^{27}	$2^{27} * 1.5$	2^{28}	2^{29}

To complete a full error check and scrub within the recommended 24 hours, the average periodic interval per ECS operation (${}^tECSint$) is 86,400 seconds divided by the total number of manual ECS operations to complete one full cycle of ECS. ${}^tECSint$ is included in the following table.

Table 248: Average Periodic ECS Interval (${}^tECSint$)

Configuration	8Gb	16Gb	24Gb	32Gb	64Gb
x4, x8, x16	1.287ms	0.644ms	0.429ms	0.322ms	0.161ms

For the device to perform automatic ECS operations when in automatic ECS mode, the host needs to issue periodic REFab commands or periodically enter self refresh mode. The maximum spacing between REFab commands or self refresh entry for the device to complete the automatic scrub within the recommended 24 hours is ${}^tECSint$. Meeting this REFab/self refresh requirement enables the device to perform the automatic ECS operations without placing additional restrictions on refresh mode usage (i.e., all bank/same bank refresh or normal/FGR mode refresh) while in automatic ECS mode. REFab commands issued in excess of required by the device for automatic ECS operations (one per ${}^tECSint$) may be used by the device for normal refresh operation. Issuing multiple REF commands shall not exceed the total number allowed within a $1 \times {}^tREFI$ window, as described in the Refresh Operation Scheduling Flexibility section of the spec.

When in automatic ECS mode, the ECS commands and timing are generated and satisfied internal to the device, following the average periodic ECS interval timings to ensure the error check and scrub is completed and the transparency registers (MR16-20) are updated within the recommended 24 hour period.

The device is required to perform automatic ECS operations while in self refresh mode if automatic ECS is enabled by MR14 OP[7] = 0b or automatic ECS in self refresh is enabled by MR15 OP[3] = 1b to

meet the average periodic ECS interval timings, regardless if self refresh is entered from manual or automatic ECS mode. However, some variation in the device scrubbing rate may be encountered while in self refresh since the device will need to sync the internal operations to an internal oscillator frequency. Entering and exiting self refresh does not reset the ECS transparency counters/registers. Interval timing for the maximum spacing between REFab commands or another self refresh entry is allowed to restart upon self refresh exit.

Writeback of Data During an ECS Operation

The device may optionally support the suppressing of writeback for ECS writebacks. The Micron device implements the feature in MR15. DDR5 SPD byte 14 bits[2:1] indicate if the feature is supported and also indicates that Micron uses MR15 for enabling the modes. Micron devices define these bits in MR15, as shown in the table below. For complete details, see the Mode Registers section.

If MR15:OP[6]=1, the DRAM suppresses writeback of data and ECC check bits during ECS operation for x4, x8 and x16 devices. The device continues to count errors to provide transparency.

ECS Threshold Filter

The ECC transparency and error scrub scheme incorporates a user-programmable ECS threshold filter that masks error counts less than the programmed filter value. The value is set using MR15 as listed in the table below. The default MR15 setting is 256 fails per Gb of memory cells (OP[2:0]=011b).

Table 249: MR15 Transparency ECC Error Threshold Count per GB of Memory Cells and Automatic ECS in Self Refresh (For Reference Only)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
15	x4 writes	ECS writeback	RFU		Automatic ECS in Self Refresh	OP[2:0]: 011b = 256 (default) OP[2:0]: 100b = 1024 OP[2:0]: 101b = 4096 OP[2:0]: 110b-110b = RFU		

Error Check and Scrub Error Tracking

The type of error tracking provided by the ECC transparency and error scrub is selectable using MR14:OP[5], which can track either the number of rows with errors (default) or code words with errors using the error counter. The row or code word error count is tracked and written to MR20. MR14:OP[5] is programmed during device initialization and should not be changed once the first ECS command is issued, otherwise an unknown operation could result. If MR14:OP[5] is changed without a power cycle of the device, a MR14:OP[6]=1 reset must be issued prior to subsequent ECS commands to reinitialize the counters.

When the ECC row count mode is selected, the EC increments each time a row with check bit errors is detected. After all rows—in all banks, in all bank groups—have ECS operations performed, the result of the EC is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

MR20 is shown in the table below. EC[7:0] indicate error counts within a range. EC0 is set to 1 if EC0(min) (the ETC set by MR15) has been reached, but the fail count is less than or equal to EC0(max) = 2 * ETC * density(Gb) - 1. Likewise, the minimum values of EC[7:1] are defined as EC[x](min) = ETC * density(Gb) * 2^x, and maximum values are defined as EC[x](max) = 2 * (ETC * density(Gb) * 2^x) - 1. The exception is EC7(max), which is unlimited. The corresponding bit is set if the error count is within the required range.

Table 250: MR20 Number of Rows or Code Word Errors by Die (For Reference Only)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
20	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

When the ECC code word error count mode is selected, the EC increments each time a code word with check bit errors is detected. After all code words—on all rows, in all banks, in all bank groups—have ECS commands performed, the result of the error counter is loaded into MR20, subject to error threshold reporting. The EC is reset after the value has been transferred to the mode register.

The ECC errors per row counter (EPRC) increments the number of code word errors on a given row after more than one error on a given row is detected. The EPRC counter resets with each column address wrap. Each row's code word error count is compared to the previous code word error count to determine the row address with the highest error count within the die. After reading all code words on a row, the number of errors counted is compared to the number of errors from the previous row. If the previous row error count is less than the present row error count, the present larger error count is saved to the previous high error count register, its associated address is saved to the previous high error count row/bank address/bank group register, and the present row error counter is cleared. If the previous row error count is greater than the present row error count, the previous row error count and register value remains unchanged; however, the present row error counter is cleared.

After all rows—in all banks, in all bank groups—have executed ECS operations, the result of the previous high error count (address and error count) are latched into MR16-19 when the bank group counter wraps, if the errors per row count (EPRC) meets or exceeds the row error threshold count (RETC) in the MR15 Transparency ECC Error Threshold Count per GB of Memory Cells and Automatic ECS in Self Refresh (For Reference Only table).

MR16-18 show in the table below contains the information for the row with the highest number of code word errors and is allocated as A[17:0] row address, BA[1:0] bank address, BG[2:0] bank group address. MR19 shown in the table below contains the information for the errors per row count (EPRC) for the number of code word errors on the highest failing row. REC[5:0] indicate error counts within a range. REC0 is set to 1 if REC0(min) (the RETC defined in the following table) has been reached, but the fail count is less than or equal to REC0(max) = $2 * RETC - 1$. Likewise, the minimum values of REC[5:1] are defined as REC[x](min) = $RETC * 2^x$, and maximum values are defined as REC[x](max) = $2 * (RETC * 2^x) - 1$. The exception is REC5(max), which is unlimited. The corresponding bit is set if the error count is within the required range.

Table 251: MR16-19 Address of Row with Max Errors and Error Count (For Reference Only)

MR	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
16	R7	R6	R5	R4	R3	R2	R1	R0
17	R15	R14	R13	R12	R11	R10	R9	R8
18	RFU	BG2	BG1	BG0	BA1	BA0	R17	R16
19	RFU	RFU	REC5	REC4	REC3	REC2	REC1	REC0

Table 252: Row Error Threshold Count (RETC)

	Error Count
Row Error Threshold Count (RETC)	4

The error counters (ECC error counter and ECC errors per row counter) reset each time the bank group counter wraps. This process occurs on the ECS operation following the ECS operation that processed the last row in the last bank in the last bank group. MR16-20 are not cleared after being read from; they retain the most recent written data until they are rewritten during a subsequent bank group wrap or reset by either issuing a RESET or ECS RESET COUNTERS command.

3DS Operation

The ECS feature supports 3DS stacking, where the chip ID and MR14:OP[3:0] (CID[3:0] respectively) command bits steer the ECS command to the proper mode registers (MR14-20) within the die stack. The CID[3:0] bits are ignored for MRW commands to MR14 or MR15, resulting in identical transparency settings for all die in a 3DS stack. The CID[3:0] bits must be set for MRR commands to MR14-20 to read out the data from the target die in the 3DS stack. The CID[3:0] bits are also used by the manual ECS MPC command. For single die packages, CID[3:0] should be set to 0.

Mode register configuration and readout of mode register data requires per DRAM addressing (PDA) mode.

Broadcasting the manual ECS MPC command to all die in the stack is not supported. The manual ECS MPC command-to-command spacing requires waiting ^tECSc, even to different die in the stack. No other commands should be entered during ^tECSc. The only commands allowed during ^tECSc for a manual ECS operation are ODT_NT commands.

ECS Operation with PASR Support

Support for PASR has been deprecated. Details shown in this section are for devices that support the feature.

Segments which are masked are not guaranteed to retain their data if self Refresh is entered. If automatic ECS (MR14:OP[7]=0b) or automatic ECS in self refresh (MR15:OP[3]=1b) is enabled, ECS scrubbing will still occur in unmasked segments while in self refresh; however, the DRAM is not required to execute the ECS on the masked segments. ECS transparency may not produce accurate results if any mask bit is set. Additionally, upon exit of self refresh with masked segments, the masked segments will need to be initialized with known data and the ECS counters will need to be reset, if accurate ECS data is required during the next scrub through the full array.

Refresh Management

Periods of high device activity may require additional REFRESH commands to protect data integrity. The requirement for additional REFRESH management (RFM) support is determined by the device; it will set the read-only MR58:OP[0] to show requirement:

MR58:OP[0] = 0 indicates no additional refresh is needed beyond the refresh requirement outlined in the REFRESH Operation section.

MR58:OP[0] = 1 indicates additional refresh management is required to ensure and protect data integrity, specific attempts to by-pass the on-die circuitry designed to protect data integrity may result in data disturb.

Table 253: Refresh Management Mode Register Definition

MR58:OP[0]	Refresh Management (RFM) Requirement
0	RFM not required
1	RFM required

A suggested implementation of refresh management by the controller monitors ACT commands issued per bank to the device. This activity can be monitored as a rolling accumulated ACT (RAA) count. Each ACT command increments the RAA count by 1 for the individual bank receiving the ACT command.

When the RAA counter reaches a vendor-specified initial management threshold (RAAIMT), which is set by the vendor in the read-only MR58:OP[4:1] bits (see table below), additional refresh management is needed. Executing the REFRESH MANAGEMENT (RFM) command enables additional time for the device to manage refresh internally. The RFM operation can be initiated to all banks with the REFRESH MANAGEMENT ALL (RFMab) command, or to a single bank address (BA[1:0]) in all bank groups with the REFRESH SAME BANK (RFMsb) command. A device with MR58:OP[0] = 0 treats the RFM command as a REF command.

Table 254: RAA Initial Management Threshold (RAAIMT) Mode Register Definition (For Reference Only)

MR58:OP[4:1]	RAAIMT Value	
	Normal Refresh Mode	FGR Refresh Mode
0000b-0011b	RFU	RFU
0100b	32	16
0101b	40	20
...	...	...
1001b	72	36
1010b	80	40
1011b-1111b	RFU	RFU

The RFM command bits are the same as the REF command, except for the state of CA9. If the refresh management required bit is 0 (MR58:OP[0] = 0), CA9 is only required to be valid (V) for a REF command, and then the device treats a RFM command as a REF command. If the refresh management required bit is 1 (MR58:OP[0] = 1), CA9 = H executes the REF command. Additionally, CA9 = L executes either an RFMab command if CA10 = L or an RFMsb command if CA10 = H.

The duration of the RFMab command is dependent upon the device being in normal or FGR refresh mode, while the RFMsb command is only allowed in FGR refresh mode. ^tRFM (MIN) is equivalent to ^tRFC (MIN). See the following table.

Table 255: ^tRFM Parameters

REFRESH MANAGEMENT Operation	Symbol	Value
NORMAL REFRESH MANAGEMENT (RFMab)	^t RFM1 (MIN)	^t RFC1 (MIN)
FINE GRANULARITY REFRESH MANAGEMENT (RFMab)	^t RFM2 (MIN)	^t RFC2 (MIN)
SAME BANK REFRESH MANAGEMENT (RFMsb)	^t RFMsb (MIN)	^t RFCsb (MIN)

When an RFM command is issued, the RAA counter in any bank receiving the command can be decremented by the RAAIMT value, down to a minimum RAA value of 0 (no negative or pull-in of RFM commands is allowed). Issuing an RFMab command enables the RAA count in all banks to be decremented by the RAAIMT value. Issuing an RFMsb command with BA[1:0] enables the RAA count only with that bank address across all bank groups to be decremented by the RAAIMT value

RFM commands are allowed to accumulate or postpone, but the RAA counter will never exceed a vendor-specified RAA maximum management threshold (RAAMMT), which is set by the vendor in the read-only MR58:OP[7:5] bits (see the following table). If the RAA counter reaches RAAMMT, no additional ACT commands are allowed until one or more REF or RFM commands have been issued to reduce the RAA counter below the maximum value.

Table 256: RAA Maximum Management Threshold (RAAMMT) Mode Register Definition (For Reference Only)

MR58:OP[7:5]	RAAMMT Value	
	Normal Refresh Mode	FGR Refresh Mode
000b-010b	RFU	RFU
011b	3x RAAIMT	6x RAAIMT
100b	4x RAAIMT	8x RAAIMT
101b	5x RAAIMT	10x RAAIMT
110b	6x RAAIMT	12x RAAIMT
111b	RFU	RFU

RFM command scheduling must meet the same minimum separation requirements as those for the REF command (for an example, see the REFRESH Operation section).

An RFM command does not replace the requirement for the controller to issue periodic REF commands to the device, nor does an RFM command affect internal refresh or bank counters. The RFM commands are bonus time for the device to manage refresh internally. However, issuing an REF command also allows decrementing the RAA counter by the value set by MR59:OP[7:6], as shown in the table below. Hence, any periodic REF command issued enables the RAA counter of the banks being refreshed to be decremented by the MR59:OP[7:6] setting. Issuing an REFab command enables the RAA count in all banks to be decremented. Issuing an REFsb command with BA[1:0] enables the RAA count only with that bank address in all bank groups to be decremented.

Table 257: RAA Counter Decrement per REF Command Mode Register Definition

MR59:OP[7:6]	RAA Counter Decrement per REF Command
00b	RAAIMT
01b	RAAIMT* 0.5
10b	RFU
11b	RFU

No decrement to the RAA count values is allowed for entering/exiting self refresh. The per-bank count values before entering self refresh remain unchanged upon exit.

Adaptive Refresh Management (ARFM)

DDR5 supports an optional refresh management (RFM) mode called adaptive refresh management (ARFM). Because refresh management settings are read-only, adaptive RFM allows the controller flexibility to choose additional RFM threshold settings called RFM levels. The RFM levels permit alignment of the controller-issued RFM commands with the in-DRAM management of these commands. MR59:OP[5:4] enables selection of the adaptive RFM level, as shown in the following table.

Table 258: Mode Register Definition for Adaptive RFM Levels

MR59:OP[5:4]	RFM Level	RFM Requirement	RAAIMT Normal Refresh	RAAMMT Normal Refresh	RAA Decrement per REF Command	Notes
00b	Default	Default	Default	Default	Default	1,2
01b	Level A	RFM Required	RAAIMT-A	RAAMMT-A	RAADEC-A	1,2,3
10b	Level B	RFM Required	RAAIMT-B	RAAMMT-B	RAADEC-B	
11b	Level C	RFM Required	RAAIMT-C	RAAMMT-C	RAADEC-C	

- Notes: 1. RAAIMT values for FGR are half of the normal refresh mode.
 2. RAAMMT values for FGR are double that of the normal refresh mode.
 3. RAAIMT, RAAMMT and RAADEC values for RFM levels A-C are set by the DRAM vendor.

Adaptive RFM mode inherits the RAA counting and decrement attributes of the standard RFM mode, while using the alternate RAAIMT, RAAMMT and RAADEC for the selected RFM level. Increasing the RFM level results in an increased need for RFM commands. Level C is the highest RFM level.

Setting MR59:OP[5:4] bits to something other than the default 00b enables the alternative RFM level for the adaptive RFM mode. The host decrements the rolling accumulated ACT (RAA) count to 0b, either with RFM or pending REF commands, prior to making a change to the RFM level.

To inform the host of required RFM settings as the RFM level is changed by MR59:OP[5:4], the device modifies the corresponding mode register values for RFM required, RAAIMT, RAAMMT and RAADEC (MR58:OP[0], MR58:OP[4:1], MR58:OP[7:5], MR59:OP[7:6], respectively) for subsequent MRR commands. Mode register values that remain the same as the default settings indicate the default RFM threshold levels are supported at the selected ARFM level.

Adaptive RFM also allows a device shipped with RFM not required (MR58:OP[0]=0) to override that initial setting and enable RFM by programming a non-default RFM level. The device internally manages the change to treat the RFM command as an RFM command in this special override case, as shown in the table below. A device that supports ARFM, even if the device is shipped with RFM not required (MR58:OP[0]=0), sets MR58:OP[0] = 1 to indicate the chosen ARFM level is supported.

Table 259: RFM Commands Perceived by the Device

Command	MR58:OP[0]	MR59:OP[5:4]	Command Perceived by the Device	Notes
RFM	0b	00b	REF	1
RFM	0b	01b-11b	REF	
RFM	1b	00b	RFM	
RFM	1b	01b-11b	RFM	1,2

- Notes: 1. If the optional ARFM (MR59:OP[5:4]=01b-11b) is not supported on the device, the command perceived by the device is determined by MR58:OP[0].
 2. Adaptive RFM enables a device shipped with MR58:OP[0]=0 to override the initial setting and enable RFM by programming a non-default RFM level. The device changes MR58:OP[0]=1 to indicate the chosen ARFM level is supported.

3. If the device requires RFM (MR58:OP[0]=1) but the optional ARFM is not supported, the device does not change the programmed value in MR58:OP[0] when the host changes ARFM level settings (MR59:OP[5:4]).
4. If the device is shipped with MR58:OP[0]=0 (RFM not required), any time RFM level is default (MR59:OP[5:4]=00), then MR58:OP[0]=0. For non-default RFM levels (MR59:OP[5:4]=01,10,11), MR58:OP[0]=1 when ARFM is supported on the device.

Directed Refresh Management (DRFM)

Directed Refresh Management (DRFM) is an optional feature on DDR5 that gives the controller additional flexibility for maintaining the data integrity within the device.

The DRFM feature enables the device to capture a host-requested row address, which then is followed by a host-directed RFM command enabling the DRAM to refresh physically adjacent neighboring rows of the requested row address.

When DRFM Enable (DRFE), MR59:OP[0], is set HIGH, DRFM mode is enabled. DDR5 supports two methods to sample a DRFM address:

1. **PREpb:** When DRFM is enabled, CA5 becomes a control bit to select between CA5=H Precharge per Bank or “A5=L Precharge per bank plus sampling DRFM address. Executing the PREpb with CA5=L tells the device to sample the currently activated address for DRFM. When DRFM is disabled, CA5 retains CID3 functionality.
2. **WRPA/WRA/RDA:** When DRFM mode is enabled, CA9 on the second cycle of these two-cycle commands becomes a control bit to select between CA9=H Auto Precharge or CA9=L Auto Precharge plus sampling DRFM address. Executing a WRITE PATTERN, WRITE or READ command with Auto Precharge and CA9=L on the second cycle samples the currently activated address for DRFM. When DRFM is disabled, CA9 is required to be V during the second cycle of their two-cycle commands.

Each DRAM bank has an independent DRFM address register for the DRFM address sample. This DRFM address register is updated with each DRFM address sample to the bank, resulting in the last (most recent) address sample being retained for the host-directed DRFM command.

Although a PREpb is allowed to a closed bank or a bank that is already in the process of precharging, issuing a PREpb plus DRFM address sample to a closed or precharging bank may result in an unknown address sample, potentially overwriting a prior valid address sample.

After the DRFM address sample, the host can then issue a DRFM command to service the sampled DRFM address(es). This DRFM command is supplemental to DRAM RFM requirements.

When DRFM is enabled on DDR5, CA5 becomes a control bit to select between CA5=H RFMab/ RFMsb or CA5=L DRFMab/ DRFMsb. Executing the RFMab or RFMsb commands with CA5=L tells the DRAM to service the sampled DRFM address for all banks where a DRFM address sample occurred. Any banks without a DRFM address sample will use an address internally sampled by the DRAM. Banks with internally sampled addresses enable the host to decrement the RAA count for those banks. Since DRFM is supplemental, any banks with DRFM address samples do not allow RAA counts to be decremented.

RFMab or RFMsb commands with CA5=H will only use DRAM internally sampled addresses and do not interfere with any DRFM sampled addresses. Then DRFM is disabled; CA5 retains CID3 functionality for RFMab or RFMsb commands. See the Command Truth Tables for description of the commands used in this section.

Following a DRFM command to the device, any host-requested row address samples to banks that received the DRFM command will be cleared from further use.

Aside from the DRFM command, a reset is the only other way to clear DRFM-sampled addresses. Any DRFM-sampled addresses will be retained during self refresh, power down, MPSM modes, etc., requiring the host to resample prior to issuing a DRFM command if the address retained in a bank is no longer relevant. Additionally, no RAA credit is given to banks with DRFM sampled addresses, regardless of relevancy.

DRFM command scheduling must meet the same minimum separation requirements as those for the REF command (see the [Refresh Command Scheduling Separation Requirements](#) table in the Refresh Operation section).

On average, any row/bank address combination may be sampled once per DRFM command interval, t_{DRFMI} . t_{DRFMI} is $2 * t_{REFI1}$, resulting in no more than 4,096 DRFM commands to the same row/bank address combination within t_{REF} .

Bounded Refresh Configuration (BRC) and t_{DRFM}

The DRFM command refreshes physically adjacent neighboring rows to the DRFM sampled address, up to the distance specified by the Bounded Refresh Configuration (BRC) as defined by MR59:OP[2:1]. The DRAM is responsible for applying a refresh ratio to the outermost rows being refreshed to protect the DRAM from excessive refreshes on rows adjacent to the outermost rows.

For example, BRC2 will always refresh the ± 1 physically adjacent neighboring rows, and the ± 2 physically adjacent neighboring rows may be refreshed at a reduced rate as determined by the DRAM. Likewise, if BRC4 is programmed, the device will always refresh the ± 1 , ± 2 and ± 3 physically adjacent neighboring rows, while applying a ratio to ± 4 physically adjacent neighboring rows.

The corresponding DRFM command duration (t_{DRFM}) is directly related to the time required to refresh the rows. Due to a single row being refreshed on multiple banks corresponding to the DRFMab or DRFMsb command being issued, the per-row-refresh duration is t_{RRF} , as shown in the following table.

Table 260: t_{RRF} by Device Density

Parameter	Symbol	8Gb	16Gb	24Gb	32Gb	Units
All bank per row refresh duration	t_{RRFab} (MIN)	70	70	70	70	REF
Same bank per row refresh duration	t_{RRFsb} (MIN)	60	60	60	60	REF

The equation for t_{DRFM} is $(2 * t_{RRF}) * BRC$. t_{DRFM} is dependent on the DRFMab or DRFMsb command being issued. The following table shows the allowable BRC options and corresponding t_{DRFM} durations.

Table 261: Bounded Refresh Configuration (BRC) and t_{DRFM} Density

MR59:OP[2:1]	Rows Refreshed	t_{DRFMab}	t_{DRFMsb}	Units
BRC 2	Always ± 1 , Ratio ± 2	280	240	ns
BRC 3	Always ± 1 , ± 2 , Ratio ± 3	420	360	ns
BRC 4	Always ± 1 , ± 2 , ± 3 , Ratio ± 4	560	480	ns
RFU	RFU	RFU	RFU	

BRC Support Level

The BRC support level indicates how many BRC options the device can support, which is set by the device vendor in the read-only MR59:OP[3]. A device with MR59:OP[3]=0 supports all BRC options (BRC2, 3, 4). A device with MR59:OP[3]=1 only supports BRC2. If the device only supports BRC2, MR59:OP[3]=1, the default support is BRC2 regardless of BRC setting in MR59:OP[2:1]. BRC2 only support is a transitional option for early support of DRFM. Device vendors must support all BRC options (BRC2, 3, 4) with future device designs.

Per Row Activation Counting

Per row counting of row activations is an optional feature on 16Gb and higher density devices, with support indicated by MR70:OP[0]. This feature detects row activity that may adversely affect the data stored in cells on physically adjacent rows within the device. As one or more rows' activation counts approach or reach a maximum activation threshold after a REFRESH (REF) or REFRESH MANAGEMENT (RFM) command, the host and device may need to take action to prevent data in affected cells from flipping states.

The intended implementation for per row activation counting (PRAC) is to add activation counter bits to every row in the device. These bits store a count associated with the number of activations received by a row since the last time it was refreshed. Activations to a row include the ACT, REF and RFM commands, and the MPC Manual ECS function.

A device design that supports PRAC shall continue to support “legacy” methods for maintaining data integrity in device cells for backward compatibility. Designs supporting PRAC shall continue to support all features and functions as defined in this specification when running with PRAC disabled.

When PRAC is enabled, (MR70:OP[1]=1b), the following modes are disabled by the device, with MR58 and MR59 retaining their access types and values, and those MRs will reflect the values of any subsequent MRWs:

- RFM Required, as indicated by MR58:OP[0], is disabled internally by the device and not required by the host regardless of value set in the MR
- DRFM Enable, as configured by MR59:OP[0], is disabled internally by the device regardless of host write value

Functionality of the PRAC RFM command is enabled when MR70:OP[1]=1b and replaces the command usage described in the Refresh Management (RFM) section. If refresh management is not required (MR58:OP[0]=0b) and PRAC is disabled (MR70:OP[1]=0b), CA9 is only required to be valid (V) for a REF command, and the device will treat a RFM command as a REF command. If refresh management is required (MR58:OP[0]=1b) or PRAC is enabled (MR70:OP[1]=1B), a REF command requires CA9=H.

DRFM functionality of the WRPA, WRA, RDA, PREpb and DRFM commands is disabled regardless of MR59:OP[0] host write value when MR70:OP[1]=1b. The DRFM address sampling operation is disabled for the WRPA, WRA, RDA, and PREpb commands. CA9 is only required to be valid (V) for WRPA, WRA, and RDA commands. When CID3 is not used, CA5 is required to be valid (V) for RFM and PREpb commands.

The requirements for enabling and using PRAC are described in the following sections. Updates to usage of the PRAC RFM command are described in the Per Row Activation Counting Response and Back-off Protocol sections.

On-the-fly switching between modes is not permitted. Enabling PRAC requires initialization, as described below. Disabling PRAC (re-enabling legacy) requires a device reset.

When PRAC is supported (MR70:OP[0]=1b) but disabled (MR70:OP[1]=0b), all associated mode registers can be written to and read from; however, no PRAC-related behaviors will be executed until PRAC is enabled (MR70:OP[1]=1b). Activation counter initialization, PRAC testing, and alert verification shall be disabled prior to enabling PRAC.

Activation Counter Initialization

Upon power-up or any time the device refresh requirements are violated, the activation counter bits may be in an unknown state, requiring an initialization to put the bits into a known state.

The default state per row activation counting (PRAC) is disabled (MR70:OP[1]=0b), as this is an optional feature. Prior to initialization of the activation counter bits, the PRAC shall be enabled

(MR70:OP[1]=1b) by the host. Once the PRAC is enabled, a full array activation counter initialization (ACI) shall be performed. The device will not track activation counts, nor issue an ALERT BACK-OFF (ABO), until the activation counter bits are initialized. Legacy mode for maintaining of data integrity will not be performed after PRAC is enabled.

To initialize the activation counter bits, the host sets MR70:OP[2]=1b to indicate to the device that a full array refresh will take place. Only REF and MRR commands are permitted during initialization. The REF commands during the initialization period may be issued by the host up to two times (2x) the normal refresh rate (Normal mode: $0.5 \cdot t_{REFI1}$; FGR mode: $0.5 \cdot t_{REFI2}$). Upon completion of a full refresh cycle, the device indicates completion by setting MR70:OP[3]=1b, which the host then follows by setting MR70:OP[2]=0b. The device starts counting activations from that point forward and issues the ABO as necessary.

During ACI, the device does not need to refresh the main array, and any data previously written may be corrupted. If the host reenters activation counter initialization by setting MR70:OP[2]=1b, the device resets MR70:OP[3]=0b until the initialization has been completed. Likewise, a system reset to disable PRAC (MR70:OP[1]=0b) also resets MR70:OP[3]=0b.

Like normal device cells, the activation counter bits require refresh to maintain the stored values. Any time refresh is violated during ACI or after ACI in modes like MPSM or other idle periods, the ACI is performed by the host to set the activation counter bits to a known state. Since array data is also corrupted by refresh violations, previous activation counter values become irrelevant.

The MBIST operation impacts the activation counter bit values, requiring an ACI to be performed prior to rewriting data following the MBIST/mPPR operation.

Per Row Activation Counting Core Timing Parameters

Per row activation counting (PRAC) requires additional counter cells per row in the device to store ACTIVATION (ACT) command counts. Updating the activation counter cells requires a read-modify-write to the activation counter cells, known as activation counter update (ACU), resulting in a change in some of the core timing parameters, when per row activation counting is enabled (timings not noted here remain the same as when PRAC is disabled):

Table 262: Per-Row Activation Counting (PRAC) Core Timing Parameters

Parameter	Symbol	Min	Max	Unit	Notes
ACT to PRE	t_{RAS}	16	$3 \cdot t_{REFI1}$ (Normal), $5 \cdot t_{REFI2}$ (FGR)	nS	1
Row Precharge	t_{RP}	36	-	nS	2
ACT to ACT/REF	t_{RC}	52	-	nS	
Read to Precharge	t_{RTP}	5	-	nS	3
Write Recovery	t_{WR}	10	-	nS	3

Notes: 1. t_{RASmax} is based on the maximum allowance for postponed REF commands.

2. Clock-based nRP timings are defined in the Speed Bin tables.

3. Clock-based nRTP and nWR timings are defined in MR6.

Examples of timings affected by the updating of the activation counter bits are shown below. The “i” references device internal commands, not external commands issued by the host.

Figure 188: ACT-PRE with ACU Example

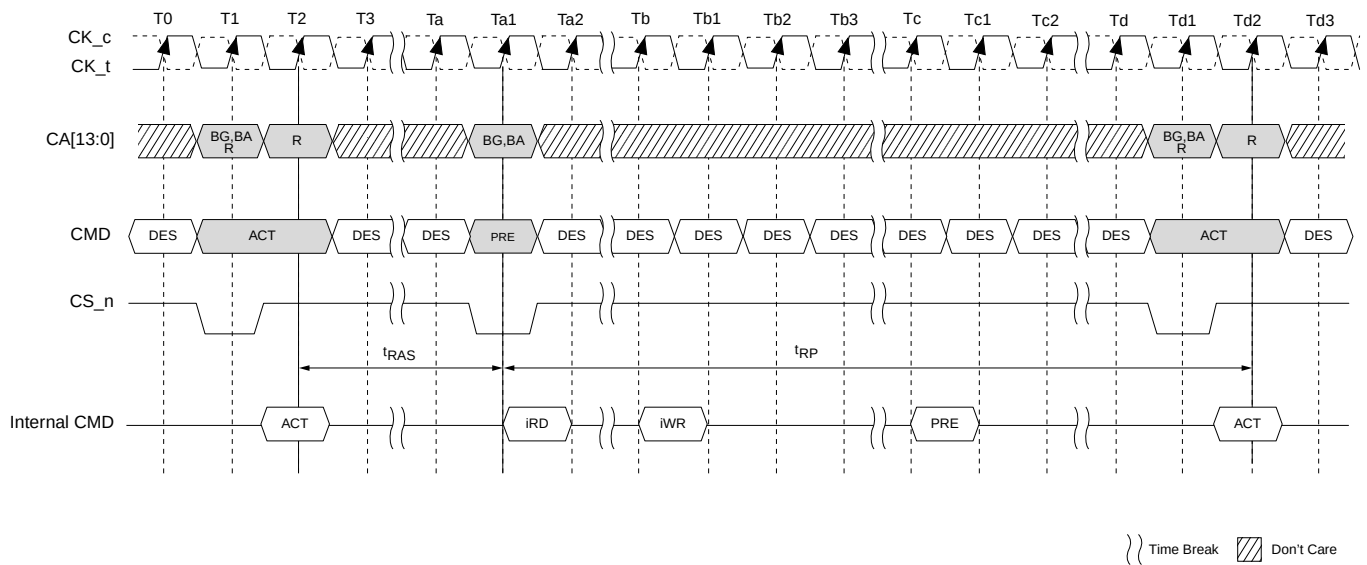


Figure 189: ACT-WRT-PRE with ACU Example

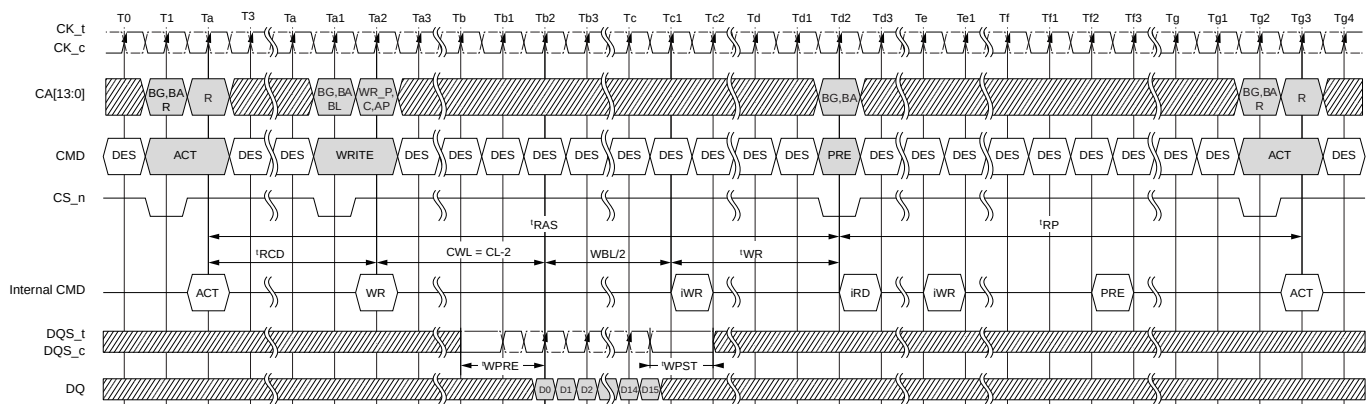
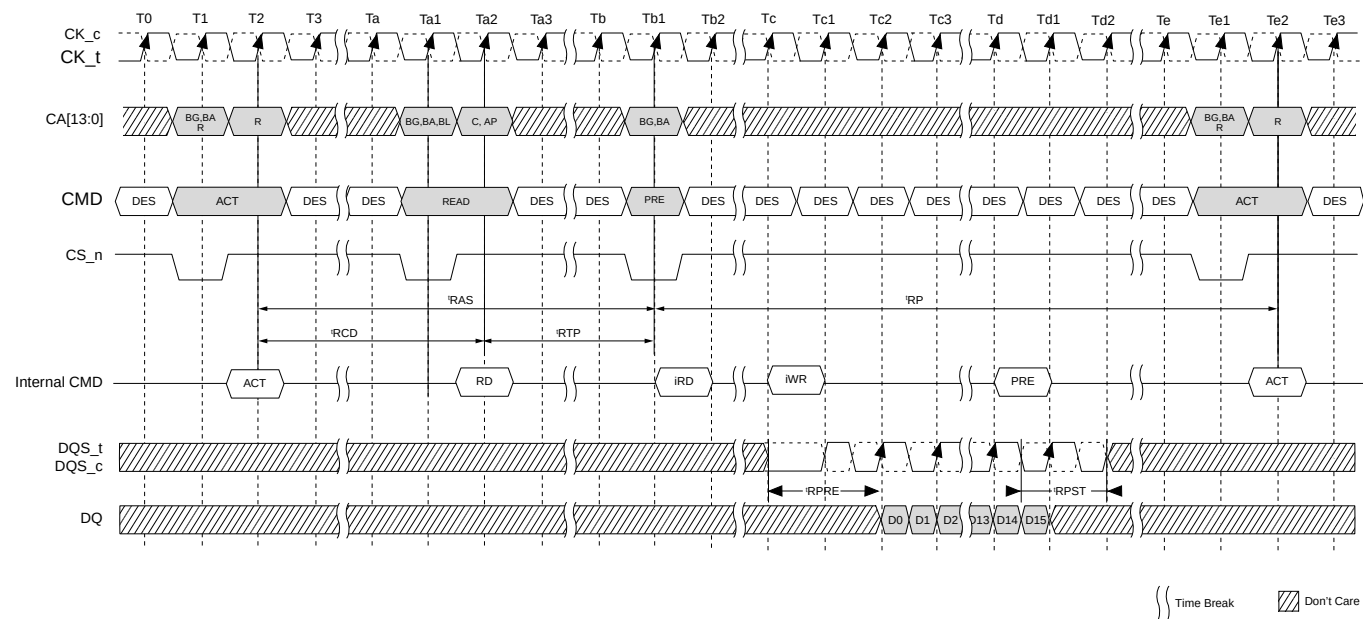


Figure 190: ACT-RD-PRE with ACU Example



Refresh Operation Scheduling Flexibility

Refresh operation scheduling flexibility is reduced when PRAC is enabled to allow targeted refreshes to occur at an improved rate.

In normal refresh mode, a maximum of 2 REFab commands can be postponed. In the case that 2 REFab commands are postponed, the resulting maximum interval between the surrounding REFab commands is limited to $3 \times t_{REFI1}$. At any given time, a maximum of 2 REFab commands can be issued within $1 \times t_{REFI1}$ window.

In FGR Mode, the maximum REFab commands that may be postponed is 4, with the resulting maximum interval between the surrounding REFab commands limited to $5 \times t_{REFI2}$. At any given time, a maximum of 5 REFab commands can be issued within $1 \times t_{REFI2}$ window.

Precharge Timing

Unlike the traditional PRECHARGE (PRE) command, the PRAC PRE initiates an internal READ followed by an internal WRITE to increment the activation counting bits for all open rows affected by the PRE command. To allow for adequate power distribution network (PDN) recovery, the row precharge time (t_{RP}) shall be scaled by the number of rows being closed.

Table 263: Pre Row Activation Counting Precharge Timing

Parameter	Number of Rows	t_{RP} Required
Per Bank Precharge (PREpb)	1	$t_{RP, min}$
Same Bank Precharge (PREsb)	1-8	$t_{RP, min}$
All Bank Precharge (PREab)	1-8 9-32	$t_{RP, min}$ $t_{RP, min} + 4ns$

Per Row Activation Counting Response

Since the device counts ACT commands on a per-row basis, action may be required upon one or more rows reaching a counter threshold level or levels, or when a queue holding row addresses for targeted refreshing reaches or passes a critical level. This action is a request by the device for the host to pause normal activity for a recovery period where refresh management (RFM commands) or other functions may be performed. This action is a “back-off”. The back-off protocol is described in the next section.

The counter and/or queue threshold level(s) may be changed (reduced) by setting the Adaptive Per Row Activation Counting level in MR71:OP[3:2] to something other than the default MR71:OP[3:2]=00b. These alternate levels are based on the default starting value. The counter threshold level(s) reductions are approximately Level A = - 10%, Level B = - 20%, and Level C = - 30%. Changing levels requires an ACI or full array refresh to set/reset all counters to a known state below critical threshold levels and to empty the queue.

In addition to the back-off, which is required to keep activation counts from exceeding the threshold level, the device can proactively perform targeted refreshes during REFRESH (REF) and/or REFRESH MANAGEMENT (RFM) commands to reduce or prevent the occurrence of the alert back-off being triggered.

Targeted Refresh

For targeted refreshing during REFRESH commands, the device adjusts the normal refreshes accordingly to allow time for the additional row refreshing to occur. The backoff protocol exists for cases where the device cannot keep up during normal REFRESH commands. There is no change to ^tRFC when PRAC is enabled.

Targeted RFM

DDR5 does not require issuing RFM commands as proactive mitigation when PRAC is enabled. However, as a guideline for a host that chooses to have the DRAM proactively perform targeted refreshing during REFRESH MANAGEMENT commands, the host may track the level of activity that occurs on a per-bank or sub-bank basis. When the bank activation threshold (BAT) is reached (example BAT shown in table below), the RFMsb or RFMab command is issued.

The duration of the RFM command (^tRFM) is sufficient for the row refresh span of +/-1 and +/-2 physically adjacent rows and the target row to be refreshed. This ^tRFM duration is directly related to the time required to refresh the rows. Due to a single row being refreshed on multiple banks corresponding to the RFMab or RFMsb command being issued, the per row refresh duration is ^tRRE.

Table 264: Example Bank Activation Threshold (BAT)

Parameter	Symbol	Value	Unit	Notes
Bank activation threshold	BAT	75	Activations	1

Note: 1. The example BAT is derived from ^tREFI1=3.9us / ^tRC,min=52ns.

Table 265: Per-Row Refresh Timing

Parameter	Symbol	Duration	Unit
All bank per row refresh	^t RRFab(min)	70	nS
Same bank per row refresh	^t RRFsb(min)	60	nS

Table 266: Refresh Management Command Timing

Parameter	Symbol	Duration	Unit
RFM all bank (RFMab)	^t RFMab	(4+1) * ^t RRFab	nS

Table 266: Refresh Management Command Timing (Continued)

Parameter	Symbol	Duration	Unit
RFM same bank (RFMsb)	t_{RFMsb}	$(4+1) * t_{RRFsb}$	nS

Back-Off Protocol

DDR5 devices may support the optional per-row activation counting (PRAC) for monitoring per row activity to ensure all rows are refreshed as needed to maintain data integrity. To facilitate the refresh activity, the device may request that the host pause normal activity for a maintenance period where REFRESH MANAGEMENT (RFM commands) or other functions may be performed. This is called a “back-off”.

Alert Back-Off Protocol

The back-off protocol uses the ALERT_n signal and mode register settings to provide a handshake between the device and the host. This is the Alert Back-Off (ABO).

PRAC Triggered Alert Back-Off

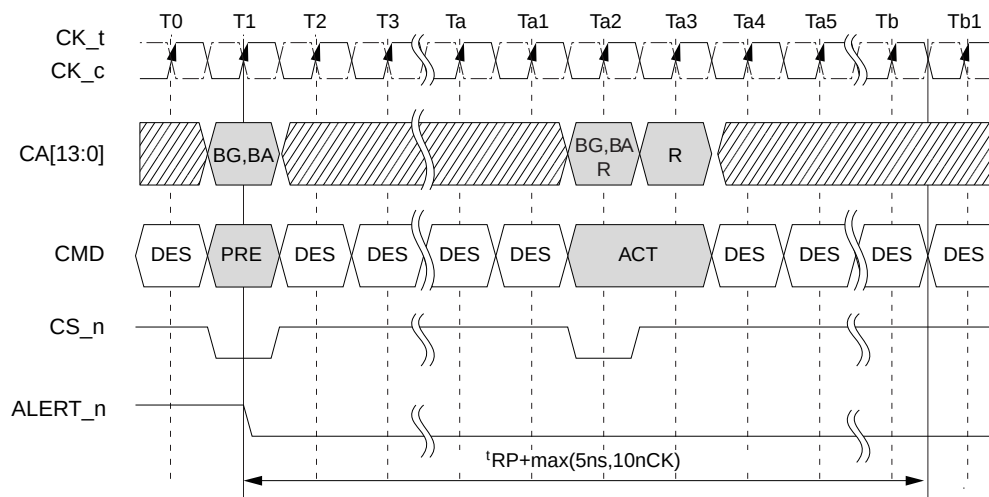
The Alert Back-Off (ABO) protocol is enabled when PRAC is enabled by setting MR70:OP[1]=1b. Upon reaching critical threshold levels by one or more rows, or when a queue holding addresses for targeted refreshing reaches or passes a critical level, the device asserts ALERT_n and sets the ABO flag at MR70:OP[5]=1b, indicating ALERT_n was asserted due to additional refresh management (RFM) being required. All commands received by the device are executed while ALERT_n is asserted to maintain synchronization between devices in the same rank on a DIMM.

Commands that may trigger the ABO include PREab/PREsb/PREpb, WRPA, WRA, RDA, REFab/REFsb and RFMab/RFMsb and the MPC function Manual ECS. ALERT_n will be asserted within t_{ABO_Assert} , which occurs between issuing the trigger command and before the $\max(5ns, 10nCK)$ following the completion of the respective command duration shown in the following table.

Table 267: Duration to ALERT_n Assertion

Symbol	Description	Command	Max
t_{ABO_Assert}	Duration to ALERT_n assertion	PREab/PREsb/PREpb	$t_{RP} + \max(5ns, 10nCK)$
		WRPA/WRA	$CWL + WBL/2 + t_{WR} + t_{RP} + \max(5ns, 10nCK)$
		RDA	$t_{RTP} + t_{RP} + \max(5ns, 10nCK)$
		REFab (Normal)	$t_{RFC1} + \max(5ns, 10nCK)$
		REFab (FGR)	$t_{RFC2} + \max(5ns, 10nCK)$
		REFsb	$t_{RFCsb} + \max(5ns, 10nCK)$
		RFMab	$t_{RFMab} + \max(5ns, 10nCK)$
		RFMsb	$t_{RFMsb} + \max(5ns, 10nCK)$
		MPC function Manual ECS	$t_{ECSc} + \max(5ns, 10nCK)$

Figure 191: Example Duration to ALERT_n Assertion for PRE Command



Since the PREpb required during hPPR/sPPR and the PREab during mPPR have different functions than closing a row, no counter bits will be incremented associated with the repaired row; therefore, no ABO will be triggered in this instance.

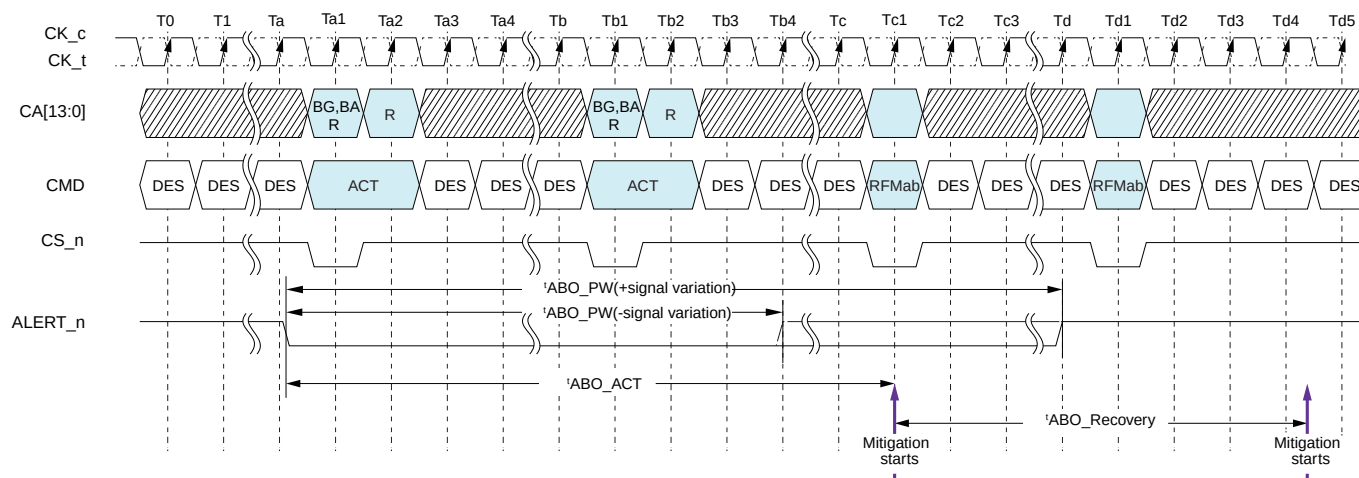
Alert Back-Off

To instantiate the ABO, ALERT_n is asserted by the device with a fixed duration of clock cycles as defined by t_{ABO_PW} .

Table 268: Alert Back-Off Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
t_{ABO_PW}	Alert Back-Off pulse width	-	640	-	nCK
t_{ABO_ACT}	Normal traffic to the device allowed	-	-	180	ns

Figure 192: Alert Back-off Timing Diagram



After the ALERT_n is asserted, a bounded number of ACTIVATE (ACT) commands are permitted before the host starts the RFM-based recovery period. Issuing ACT commands along with normal traffic is allowed within the ^tABO_{ACT} window.

At the end of the ^tABO_{ACT} window, the host begins issuing REFRESH MANAGEMENT (RFM) commands. The only RFM commands allowed during the ^tABO_{Recovery} period are RFMab. The duration of the RFMab command is described in the previous section (Per-Row Activation Counting Response). The number of RFMab commands required to be issued per ABO maintenance period are defined by mode register ABO_{RFM} bits, MR71:OP[1:0]. Systems that have stricter requirements for isochronous bandwidth may limit the number of RFMab commands by setting MR71:OP[1:0] to a lower value.

The recovery period begins when the host issues the first RFMab command in response to ALERT_n. The device self-clears the ABO flag by setting MR70:OP[5]=0b by the end of the ^tABO_{Recovery} period, which ends ^tRFMab after the last RFMab command.

If additional RFM commands are needed, the Alert Back-Off protocol is restarted following the Alert Back-Off delay, as described below.

During the ABO_{Recovery} period, a host may issue only RFMab, REFab/REFsb, PDE, PDX, SRE, PREab and MRR commands. REFRESH commands issued are to ensure that device refresh requirements are not violated. The REFRESH commands do not perform any of the refresh management required.

If power down is entered after ABO has been asserted, but before the ALERT_n pulse has completed, the device continues to assert ALERT_n for the expected ^tABO_{PW} duration; however, the host only resumes issuing RFM commands after exiting power down.

If power down is entered after ABO has been asserted and the ^tABO_{PW} duration has completed, the host is responsible for issuing all of the expected RFM commands as of combination of commands before entering and after exiting power down.

In self refresh, the device de-asserts ALERT_n. Upon exiting self refresh, the device reevaluates and issues a new ALERT_n if ABO is still needed.

Alert Back-Off Delays

ABO_{Delay} defines an interval in which the device services a minimum number of ACTIVATE commands before it can reassert ALERT_n for another Alert Back-Off. ALERT_n asserted for other operations, such as Write DQ CRC errors, is allowed with no timing restrictions.

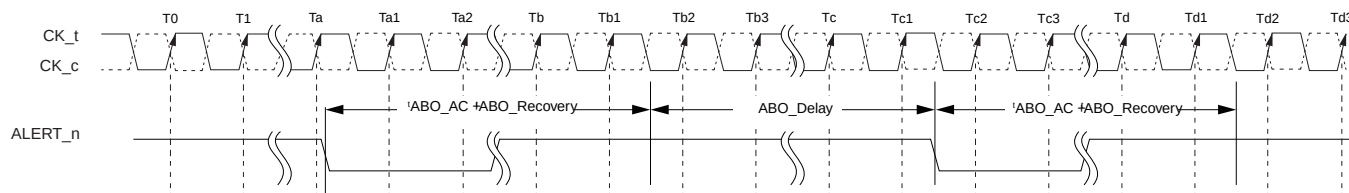
ABO_{Delay} is specified by the number of ACTIVATE commands in MR71:OP[1:0]. Commands that activate one or more rows in a DRAM include ACT, REFab/REFsb and RFMab/RFMSb and the MPC Manual ECS function, and any that occur are included in the total ABO_{Delay} Activates count allowed per bank.

Following ABO_{Delay}, any of the commands included in PRAC Triggered Alert Back-off section may trigger the ABO, as well as an ACT command.

Table 269: Alert Back-Off Delay Parameter

Symbol	Description	Value	Unit
ABO _{Delay}	Minimum number of ACTIVATE commands allowed	MR71:OP[1:0]	Activates

Figure 193: Back-to-Back Alert Back-Off Delay



ALERT_n Priorities

At times, both Write CRC and Alert Back-Off may occur simultaneously resulting in an overlap of ALERT_n assertions, or the occurrence of the two events back-to-back (nonoverlapped) may result in a short “glitch” on ALERT_n.

For all events, the device treats the ALERT_n as a NOR function, where ALERT_n is issued whenever an event occurs and the DRAM sets the corresponding Write CRC (MR50:OP[3]) or Alert Back-Off (MR70:OP[5]) flag indicating which type of event, or possibly both, occurred.

Activation Counter Errors

The device has the capability to detect errors that occur within the counter bits, and the following protocol defines how the device will report the associated failing row address to the host for repair.

If a counter bit error is detected, the device sets the Counter Error Flag, MR72:OP[0]=1b.

While the Counter Error Flag is set, the counter function for the specific row with the error is disabled. The device will not assert the Alert Back-Off to request RFM commands for errors associated with that row. All other rows without counter errors continue to count activity and assert ALERT_n, if necessary.

During ECS (manual or auto mode), if the Counter Error Flag is set and the device logs a failing row address, the device updates MR73-MR75 with the failing row address and sets the Counter Address Report Flag (MR72:OP[1]=1b) when the ECS reaches the failing row. Only the first failing row is reported. Additional rows are reported in a subsequent scrub if they continue to fail after the Counter Address Report Flag is cleared by the host.

A counter RAS error that occurs during the ECS may still trigger the Counter Error Flag, but may not set the Counter Address Report Flag nor report the failing row address.

With the failing row address information, the host can repair the bad row with hPPR/ sPPR or off-line that row.

The host clears the Counter Error Flag and Counter Address Report Flag, once the necessary information about the failing row has been collected and mitigative actions taken.

Per Row Activation Counting Testing

An optional test mode for PRAC may be included to check the ability of the device to reach a threshold per row or fill the row address queue and issue the ABO. Test mode support is indicated by MR71:OP[4]=1b.

PRAC Testing is enabled by setting MR71:OP[5]=1b. Once enabled, the counter for the target row to be tested is initialized by the host setting MR71:OP[6]=1b, followed by an ACT/PRE to the target row or rows. The host then sets MR71:OP[6]=0b and issues 32 or fewer ACT/PRE commands to trigger the ABO (multiple increments to the counter bits may occur depending on tRAS duration, mimicking normal operation). ABO is required as described previously before testing subsequent rows.

Depending on counter bit starting values, all devices on a DIMM may not trigger the Alert Back-Off at the same time (detected by MR70:OP[5]); however, all devices will trigger within 32 activations.

After PRAC testing completes, the test mode is cleared by setting MR71:OP[5]=0b. Since the counter cells will be in an unknown state following testing, a full Activation Counter Initialization (ACI) is required before resuming normal operations. Data in normal cells is not maintained during in PRAC testing.

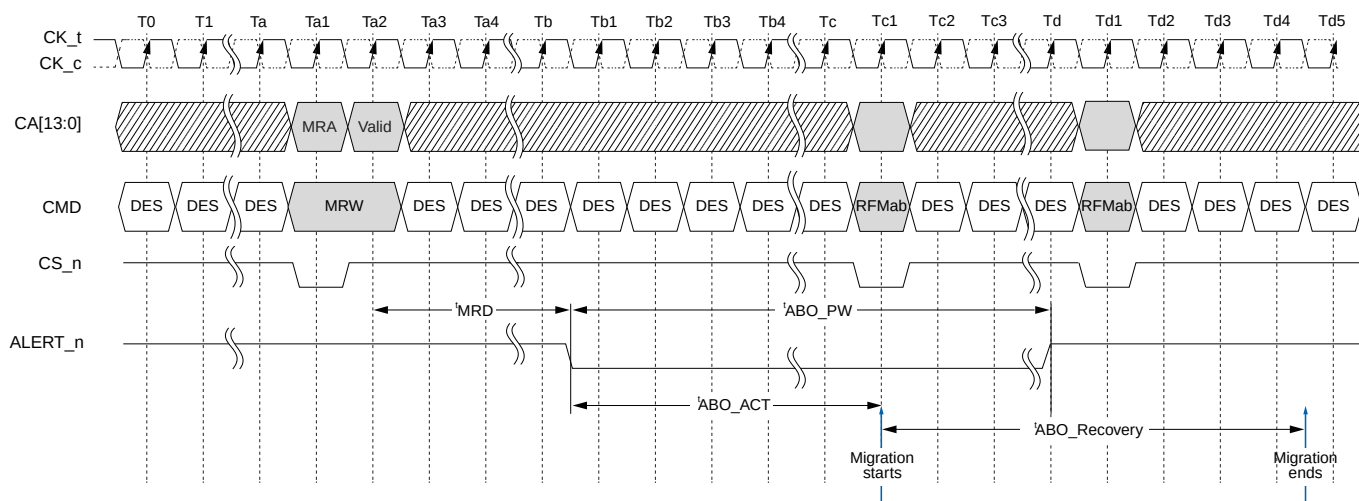
ALERT_n Verification

Support for an optional mode to verify ALERT_n is indicated by MR70:OP[6]=1b.

ALERT_n Verification is triggered by setting MR70:OP[7]=1b. The device asserts ALERT_n and sets the ABO Flag at MR70:OP[5]=1b within t_{MRD} after the MRW and will keep ALERT_n asserted for t_{ABO_PW} . The host shall follow all normal ABO procedures for clearing the ALERT_n. MR70:OP[7] and MR70:OP[5] will be self-cleared by the device prior to the end of the $t_{ABO\_Recovery}$ period.

Data in normal cells is maintained during ALERT_n Verification, as long as refresh is maintained. No per row counter values nor thresholds are altered during this mode.

Figure 194: Alert Verification Mode



Post Package Repair

Post package repair (PPR) enables a simple and easy method for repairing a failed row address. Two methods are provided: hard post package repair (hPPR) for a permanent row repair and soft post package repair (sPPR) for a temporary row repair. Additionally, DDR5 also optionally supports MBIST PPR (mPPR), which is used in conjunction with the MBIST feature to automatically repair failing addresses based on the results of MBIST.

Entry into hPPR, sPPR, MBIST and mPPR is protected through a sequential MRW guard key to prevent unintentional PPR programming. The sequential MRW guard key is the same for hPPR, sPPR, MBIST and mPPR.

The guard key requires a sequence of four MRW commands to be issued immediately after entering hPPR/sPPR/MBIST/mPPR, as shown in the figure below. The guard key sequence must be entered in the order specified in the table below. Any interruptions of the guard key sequence from other MRW/MRR commands or non-MR commands such as ACT, WR, or RD are not allowed. Although interruption of the guard key entry is not allowed, if the guard key is not entered in the required order, or if it is interrupted by other commands, hPPR/sPPR/MBIST/mPPR mode will not execute and the offending command that terminated the hPPR/sPPR/MBIST/mPPR entry may or may not execute correctly. However, the offending command does not cause device lock up. Offending commands that interrupt hPPR/sPPR/MBIST/mPPR include:

- Any interruptions of the guard key sequence from other MRW/MRR commands or non-MR commands
- MRW with CW = HIGH
- Two-cycle commands with CS_n LOW on the second cycle

Additionally, when the hPPR/sPPR/MBIST/mPPR entry sequence is interrupted, subsequent ACT and WR commands are conducted as normal commands. If an hPPR/sPPR/MBIST/mPPR operation is prematurely interrupted and/or terminated, the MR23:OP[1:0] must be reset to 0 prior to performing another hPPR/sPPR/MBIST/mPPR operation. The device does not provide an error indication if an incorrect hPPR/sPPR/MBIST/mPPR guard key sequence is entered.

Figure 195: Guard Key Timing Diagram

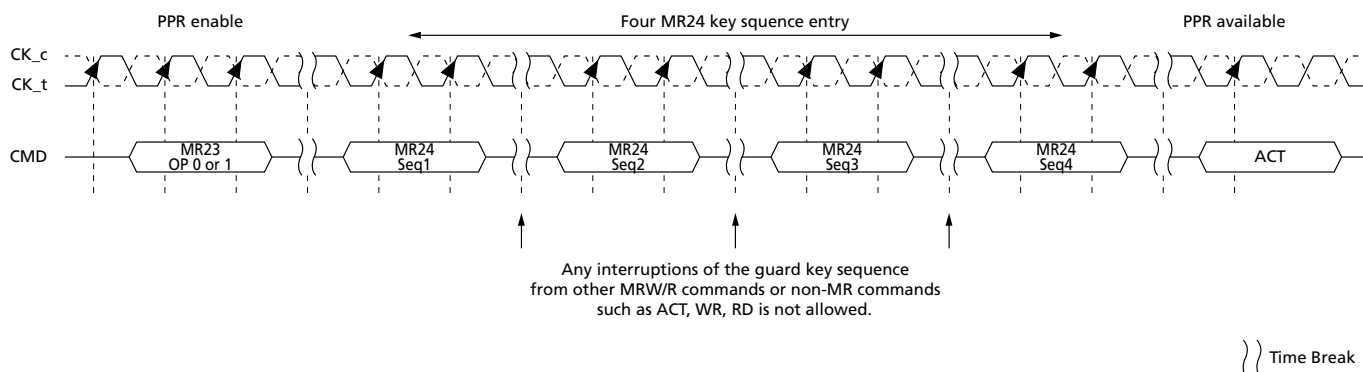


Table 270: hPPR vs. sPPR vs. mPPR

Condition	sPPR	hPPR	mPPR	Note
Persistence of repair	Volatile; repaired as long as V _{DD} is within operating range	Nonvolatile; repair is permanent after the repair cycle	Nonvolatile; repair is permanent after the repair cycle	Soft repairs are erased when V _{DD} is removed, device is reset, or sPPR UNDO command is performed to an unlocked sPPR row.

Table 270: hPPR vs. sPPR vs. mPPR (Continued)

Condition	sPPR	hPPR	mPPR	Note
Length of time to complete repair cycle	CWL + 8*tCK + tWR	tPGM_hPPRa or tPGM_hPPRb	tSELFREPAIR	
Number of repair elements per repair region ¹	1 per bank	At least 1 per bank	Vendor-specific	There is no ability to know how many mPPR elements remain in a given repair region. Host must rely on MBIST transparency in MR to determine mPPR success.
Simultaneous use of sPPR and hPPR within a repair region ¹	Previous hPPR are allowed before sPPR	Any outstanding sPPR must be cleared before a hPPR	Any outstanding sPPR must be cleared before MBIST or mPPR	
Repair sequence	1 method (WR)	1 method (WRA)	1 method (WRA)	
Device retains array data	Yes	No	No	sPPR data is not retained at the repaired row address. It must be copied or re-written.

Note: 1. Repair region defined as the address space for which a single repair can be used. A repair region is either a BG or bank, depending on vendor implementation.

Table 271: Guard Key Encoding for MR24 (For Reference Only)

Guard Key	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
MR24 Seq1	1	1	0	0	1	1	1	1
MR24 Seq2	0	1	1	1	0	0	1	1
MR24 Seq3	1	0	1	1	1	0	1	1
MR24 Seq4	0	0	1	1	1	0	1	1

Hard Post Package Repair

With hard PPR (hPPR), Micron's device can correct at least one row address per bank.

The hPPR resource designation (MR54,55,56,57) indicates hPPR resource availability, and it can be read prior to implementing a repair.

IMPORTANT: hPPR repairs are permanent; the electrical-fuse cannot be switched back to an unfused state once it is programmed. The controller should prevent unintended hPPR mode entry and repair (for example, during the command/address training period).

Entry into hPPR is through a register enable; the ACT command is used to transmit the bank and row address of the row to be replaced. For the non-binary density, an ACT command with invalid row addresses, both MSB and MSB-1 address bits are HIGH, will not be allowed since it may consume the PPR resource. After tRCD time, a BL16 WRA command is used to select the individual device through the DQ bits and to transfer the repair address to the device. After program time and PREpb, hPPR mode must be exited so normal operation can resume.

hPPR Fail Row Address Repair

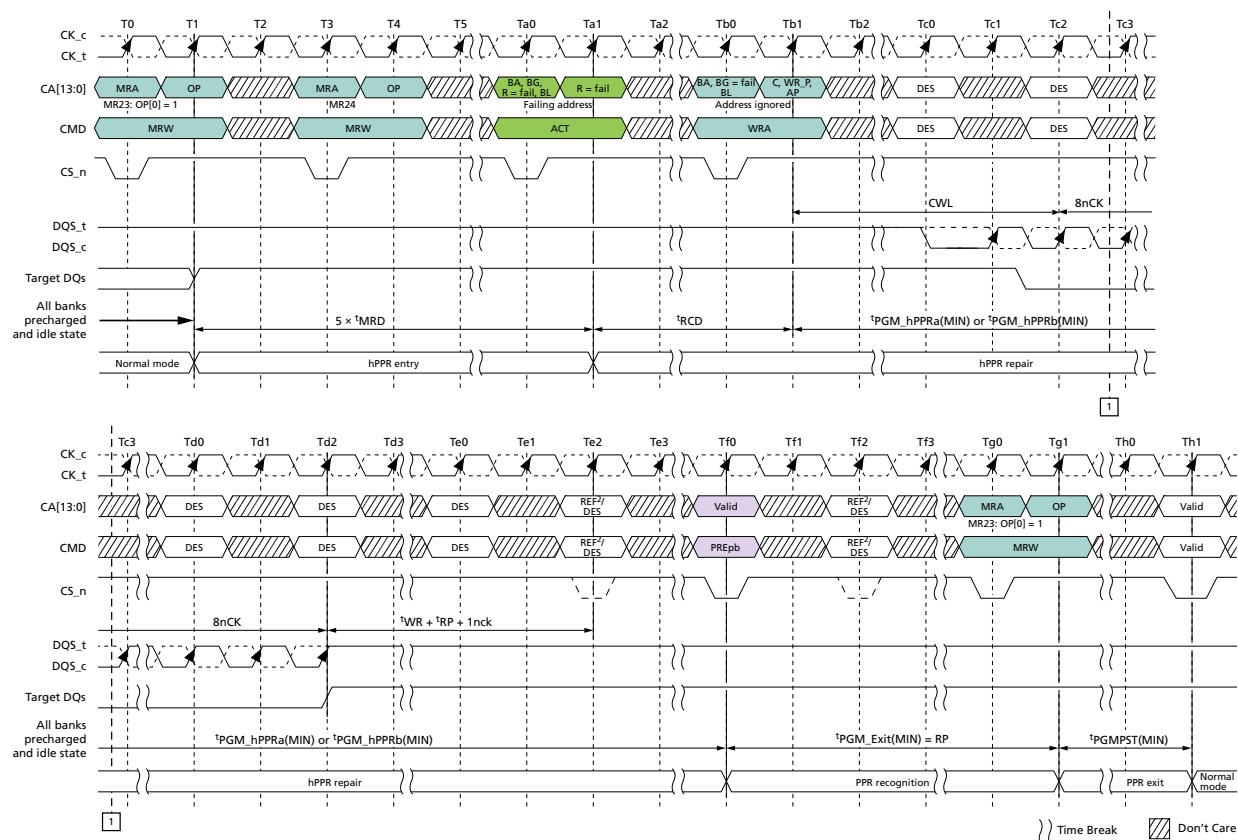
1. Because the mode register address operand allows execution of the hPPR resource, MRR of hPPR resource designation (MR 54,55,56,57) must be read. After checking the hPPR resource availability

of each bank from MRR, hPPR mode can be entered. If the MRR of hPPR resource designation (MR 54,55,56,57) is not available, the host controller should not issue hPPR mode.

2. Before entering hPPR mode, all banks must be precharged and in idle state, and CRC mode must be disabled.
3. Enable hPPR using MR23:OP[0] = 1 and wait t_{MRD}
4. Issue the guard key as four consecutive MR24:OP[7:0] MRW commands, each with a unique address field OP[7:0]. Space each MRW command by t_{MRD} .
5. Issue ACT command with the CID bits, bank group, bank and row fail address. Write data is used to select the individual device in the rank for repair. For non-3DS devices, the CID bits need only be valid and are ignored by the device.
6. After t_{RCD} , issue WRA with a valid address. The device ignores the address given with the WRA command.
7. After CWL (CWL=CL-2), DQ[3:0] of the target device must be LOW for 8^tCK . If HIGH is driven to DQ[3:0] of a device for 8^tCK , the device does not conduct hPPR and retains data if the REFab/REFsb command is properly issued. If more than one device shares the same command bus, the devices not being repaired must have DQ[3:0] driven HIGH for 8^tCK . If all the DQ[3:0] data bits are neither all LOW nor all HIGH for 8^tCK , hPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't care. Note that a previous version of the spec required all DQs to be HIGH or LOW, but this was changed to DQ[3:0] to accommodate ECC UDIMMs and SODIMMs.
8. Wait t_{PGM_hPPRa} or t_{PGM_hPPRb} to allow repair at the target row address to occur internally, and then issue PREpb command.
9. Wait $t_{PGM\_Exit,min}$ after the PREpb command to allow the device to recognize the repaired row address.
10. Exit hPPR by setting MR23:OP[0] = 0.
11. The device will accept any valid command after $t_{PGMPST,min}$
12. In the case of multiple addresses to be repaired, repeat steps 3–10.
13. For a 3DS device the target die for the hPPR is selected by the CID[3:0] bits in the ACT, WRA and PRE commands. The CID bits must match in all three commands.

During hPPR mode, REFab/REFsb commands are allowed; however, array contents are not guaranteed. Upon receiving a REFab or REFsb command in hPPR mode, the device may ignore the refresh operation, but it will not disrupt the repair operation. Other commands except REFab/REFsb during t_{PGM} can cause incomplete repair; therefore, no other commands except refreshes are allowed during t_{PGM} . Once hPPR mode exits, with MR23:OP[0] = 0 and t_{PGMPST} , confirm if the target row is repaired correctly by writing data into the target row and reading it back.

Figure 196: hPPR Fail Row Repair



- Notes:
1. Allow REFab/REFsb from $CWL + 8t_{CK} + t_{WR} + t_{RP} + 1t_{CK}$ after WR (does not guarantee array contents are refreshed during hPPR).
 2. The timing diagram shows possible commands; however, not all shown can be issued at the same time. For example, if REF is issued at Te1, DES must be issued at Te2, as REF would be illegal at Te2. Likewise, DES must be issued t_{RFC} prior to PREpb. All regular timings must still be satisfied.

Soft Post Package Repair

Soft post package repair (sPPR) is a way to quickly, but temporarily, repair one row address per bank (contrasted to hPPR, which takes longer and is a permanent repair of a row address.)

Some limitations and differences exist between an sPPR and an hPPR. Entry into sPPR is through a register enable; the ACT command is used to transmit the bank and row address of the row to be replaced. For the non-binary density, an ACT command with invalid row addresses, both MSB and MSB-1 address bits are HIGH, shall not be allowed since it may consume the PPR resource. After t_{RCD} , a BL16 WR command is used to select the individual devices through the DQ bits and to transfer the repair address into an internal register in the device. After a write recovery time and PREpb command, sPPR mode must be exited and normal operation can resume.

Care must be taken to ensure refresh is not violated for the other rows in the array during the repair time. Also note that the device retains the soft repair information inside the device as long as V_{DD} remains within the operating region. If power is removed or the device is reset, the sPPR reverts to the unrepaired state. hPPR and sPPR may not be enabled at the same time. sPPR must be disabled, cleared and unlocked (if the device supports optional sPPR undo/lock) prior to entering hPPR, MBIST or mPPR mode.

With sPPR, Micron's device can repair one row address per bank. When the hPPR resources for a specific bank or bank group are used up, the specific bank or bank group has no more available resources for sPPR. If a repair sequence is issued to a specific bank or bank group with no hPPR repair resource available, the device ignores the programming sequence.

Note that MR54-MR57 are NOT updated by an sPPR. The host controller must remember which sPPR resources have been updated since the last device reset.

The device may optionally support the sPPR UNDO and sPPR LOCK functions. The sPPR UNDO command undoes a previous sPPR and causes the sPPR resource to be returned to its unused condition. The original row appears back in the memory map at its original location following an sPPR undo. The sPPR LOCK function locks the specific sPPR resource at its current location and does not allow another sPPR or an sPPR UNDO to be performed to that resource.

A row that has been replaced by a spare row does not need to be refreshed by the device. Likewise, a spare row that is not in the memory map — either from never being in the memory map or from an sPPR undo — does not need to be refreshed by the device. If moving a spare row in and out of the memory map, the host controller is responsible for sending enough ACTIVATE commands to any mapped out row to assure any required data retention. The host controller is also responsible for any data copy operations between the original row and spare row.

The host controller should read MR23:OP[2] to determine whether the sPPR UNDO and sPPR LOCK functions are supported. 0=unsupported, 1=supported. The two features are supported together.

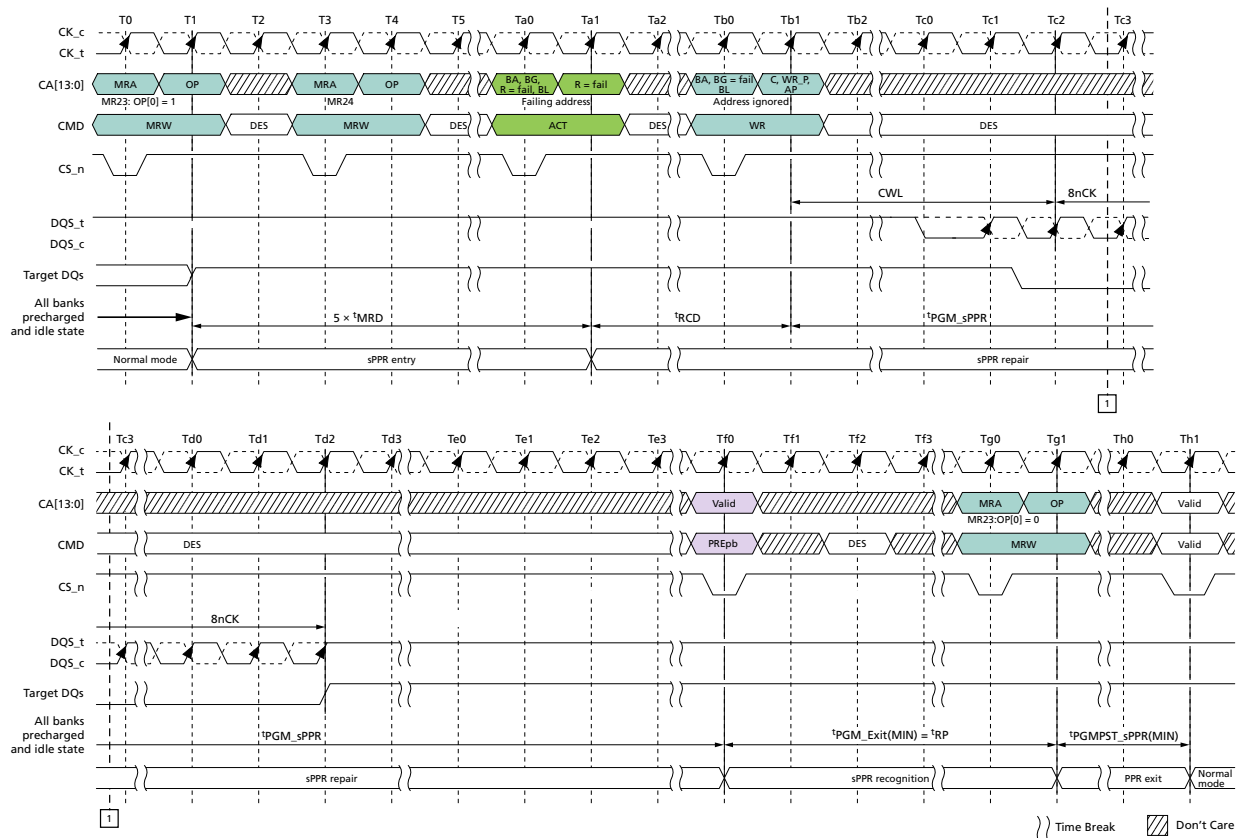
sPPR Fail Row Address Repair

The following is the sPPR procedure with WR command. During this procedure, REFRESH commands are not allowed.

1. Back up the data of the target row address in the bank before executing sPPR. The back up data should be one row per bank. After sPPR completes, restore the data in the repaired array.
2. sPPR resources are shared with hPPR. The hPPR resource designation registers (MR54, 55, 56, 57) should be checked prior to sPPR. If the MRR of hPPR resource designation (MR54, 55, 56, 57) shows hPPR resources in the bank that is targeted for sPPR, the repair is not available. The host controller should not issue sPPR.
3. Before entering sPPR, all banks must be in a precharged and idle state, and CRC mode disabled.
4. Enable sPPR using MR23 bits OP[2:1] = 01 and wait t_{MRD} .
5. Issue the guard key as four consecutive MRW commands, each with a unique address field OP[7:0]. Each MRW command must be spaced by t_{MRD} . The guard key sequence is the same as hPPR.
6. Issue the ACT command with the CID bits, bank group, bank, and row fail address. Write data selects the individual device in the rank for repair. For non-3DS devices, the CID bits need only to be valid and are ignored by the device.
7. Issue a WR command after t_{RCD} , with a valid column address. The device ignores the column address given with the WR command.
8. After CWL (CWL=CL-2), DQ[3:0] of the individual target device must be LOW for $8t_{CK}$. If more than one device shares the same command bus, the devices that are not being repaired must have DQ[3:0] driven HIGH for $8t_{CK}$. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for $8t_{CK}$, sPPR mode will be unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't cares. Note that a previous version of the spec required ALL DQs to be HIGH or LOW; this was changed to DQ[3:0] to accommodate ECC UDIMMs and SODIMMs.
9. Wait $t_{PGM\_sPPR,min}$ for the internal repair register to be written, and then issue the PRE command to the bank.
10. Wait t_{RP} after the PREpb command to allow the device to recognize the repaired row address.
11. Exit sPPR by setting MR23:OP[1] = 0 and waiting t_{MRD} .

12. sPPR can be performed without affecting the previously performed hPPR provided a row is available in the repair region. When more than one sPPR request is made to the same repair region, the most recently issued sPPR address replaces the earlier issued one associated with the given bank and row addresses. In the case of conducting a soft repair address in a different bank group, repeat steps 4–11. During a soft repair, refresh commands are not allowed between sPPR MRS entry and exit.
13. For a 3DS device, the target die for the sPPR is selected by the CID[3:0] bits in the ACT, WR, and PRE commands. The CID bits must match in all three commands.

Figure 197: sPPR Fail Row Repair



sPPR UNDO

sPPR UNDO is a method of setting the sPPR resource back to its unused state, as it was following RESET. It follows the exact same protocol as the sPPR sequence, except with MR23: OP[2:1] set to 10b.

The host controller must send the same CID bits, BG bits, bank bits, and row address in the ACTIVATE command as it did for the most recent sPPR completed in this repair region for this resource. The device may ignore the bank and row address bits if it so chooses, as the CID and BG bits may be enough to uniquely identify the sPPR resource depending on the number of repair elements. For non-3DS DRAMs, the CID bits need only be valid and are ignored by the device. Any cases where the CID bits, BG bits, bank bits or row address does NOT match that of the most recent sPPR to this resource will result in sPPR undo operation not being guaranteed. Any required copying of data is the host controller's responsibility.

Following an sPPR UNDO, a later sPPR may be done to assign the resource to a new or the same location. Data is retained in the sPPR resource, but it need not be refreshed by the device. If the host

controller requires the data to remain valid, it must send enough ACT commands to the row while it is mapped in to guarantee the data.

This feature is optional. The sPPR UNDO function should only be done to devices in which MR23 bit 2 is read as a 1 upon an MRR.

sPPR LOCK

sPPR LOCK allows an sPPR resource to be locked in place. Locks are done to sPPR resources individually. Following an sPPR LOCK, any sPPR or sPPR UNDO is blocked to that spare resource. A hardware reset or power cycle must be done to undo the lock. The hardware reset or power cycle must also be done before any hPPR operation can be done if any sPPR resources are locked.

The sPPR LOCK uses the same protocol as the sPPR function except that MR23: OP[2:1] is set to 11b. The ACTIVATE command must contain the CID bits, BG bits, bank bits and row address of the most recent sPPR for that resource. The device may ignore the bank and row address bits if it so chooses, as the CID and BG may be enough to uniquely identify the sPPR resource depending on the number of repair elements.

For non-3DS devices, the CID bits need only be valid and are ignored by the device. Any cases where the CID bits, BG bits, bank bits or row address does NOT match that of the most recent sPPR to this resource will result in sPPR undo operation not being guaranteed.

This feature is optional. The sPPR lock function should only be done to devices in which MR23 bit 2 is read as a 1 upon an MRR.

Memory Built-in Self Test (MBIST)/Memory Built-in Self Test Post Package Repair (mPPR)

DDR5 devices can support the optional memory built-in self test (MBIST) and memory built-in self test-post package repair (mPPR) to help with hard failures such as single-bit or multi-bit failures in a single device so that weak cells can be scanned and repaired during the initialization phase. There are two distinct associated phases: MBIST (self-test phase) and mPPR (self-repair phase).

During MBIST, the DDR5 device uses vendor-specific patterns to test the memory array and detect hard failures. During mPPR, addresses of hard-failures are automatically repaired out. MBIST and mPPR may only be entered from the all banks Idle state. MBIST may be ran any time after the device has been properly initialized according to the Power-up Initialization Sequence section, but must be run prior to mPPR. After MBIST completes, MR22 transparency must be read. If transparency says that fails remain and the controller chooses to run mPPR, it must perform mPPR immediately after the device transparency is read.

mPPR resources are separated from normal hPPR/sPPR resources. mPPR resources are used for initial scan and repair, and hPPR/sPPR resources still must satisfy the number of repair elements as specified in the hPPR vs sPPR table. Once MBIST is done, the device updates the MBIST/mPPR transparency status in MR22:OP[2:0]. Detailed transparency status is described in mode register 22.

Two timings are associated with MBIST/mPPR: ^tSELFTEST and ^tSELFREPAIR. The time to test the array and detect failures is defined as ^tSELFTEST. The time to repair failures detected in the previous MBIST run using mPPR is defined as ^tSELFREPAIR. Multiple iterations of MBIST and mPPR may be required to repair all failures, and the transparency status will inform the host of this.

For 3DS devices, MBIST must be run on each logical rank in the 3DS package independently by configuring MR14:OP[3:0] prior to invoking MBIST. After MBIST is run on a single logical rank, MBIST/mPPR transparency in MR22 must subsequently be read to determine whether mPPR is needed on that logical rank. The controller may choose to run MBIST on all ranks before performing mPPR on all ranks sequentially, or it may perform MBIST on one rank followed by mPPR to the same rank, proceeding through each logical rank.

MBIST Sequence

The controller is required to issue an MRW command to enter the MBIST operation. The controller sets the MR23:OP[4] to HIGH, subsequently followed by the MR24 commands for the guard key, then the device enters MBIST operation and the device drives ALERT_n to LOW. Once the MBIST is complete, the device drives ALERT_n to HIGH to notify the controller that this operation is complete.

MBIST/mPPR transparency is updated in MR22, and signifies to the host whether mPPR must be performed to repair any found fails. If mPPR is required, the controller follows the mPPR sequence described in the mPPR Sequence section, and transparency is updated once mPPR is complete.

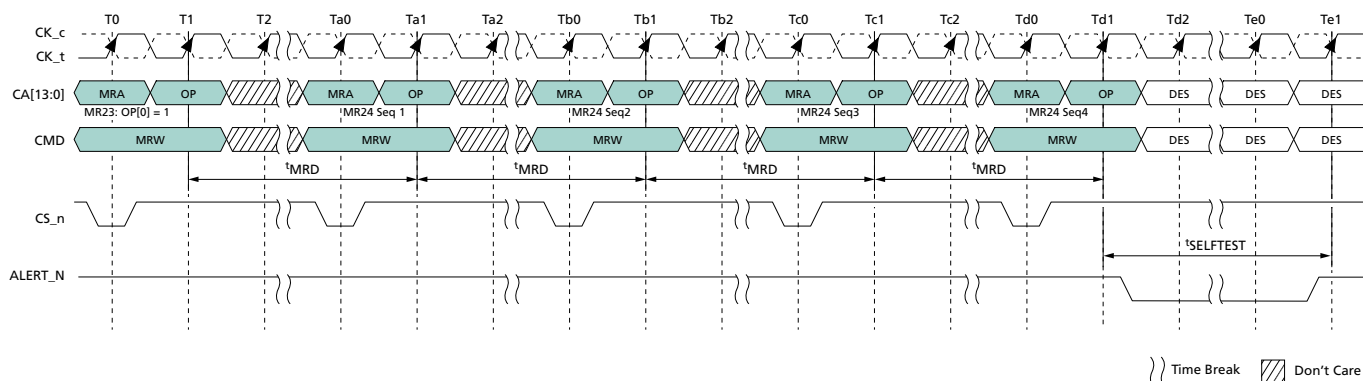
Device data is not guaranteed after MBIST PPR operation. During MBIST mode, only the DESELECT command is allowed. The DQ/DQS may either float (HI-Z) or perform RTT_PARK/DQS_RTT_PARK termination during ^tSELFTEST, depending on vendor-specific implementation, while CA/CS/CK ODT remains unchanged from its programmed state prior to MBIST. MBIST procedure is detailed in the MBIST Procedure table.

Table 272: MBIST Timing Parameter

Parameter	Density			MIN/MAX	Unit	Notes
	8Gb/16Gb	24Gb	32Gb			
^t SELFTEST	9	14	19	MAX	S	1

Note: 1. ^tSELFTEST applies per logical rank.

Figure 198: MBIST Procedure



mPPR Sequence

MBIST-PPR (mPPR) may be used after MBIST to repair failures found during the self-test phase. mPPR may only be performed after MR22 MBIST/mPPR transparency is read, and MR22 MBIST/mPPR transparency must be read after mPPR completes in order to determine if an additional mPPR or MBIST is required. If fails remain after the read of MR22 transparency, the mPPR sequence is described as follows:

1. All banks should be in a precharged and idle state, and CRC mode must be disabled prior to entering mPPR mode.
2. Enable mPPR using MR23:OP[3]=1 and wait t^{MRD} .
3. Issue guard key sequence as four consecutive MR24:OP[7:0] MRW commands, each with a unique address field OP[7:0]. Each MRW command must be spaced by t^{MRD} .
4. Issue the ACT command with a valid address. The device ignores the address given with the ACT command. Write data is used to select the individual DRAM in the rank for repair. For 3DS devices, CID on the ACT must be set to the same value programmed in MR14:OP[3:0], which determined the logical rank MBIST was last run on.
5. After t^{RCD} , issue WRA with a valid address. The device ignores the address given with the WRA command. For 3DS devices, CID on the WRA must be set to the same value programmed in MR14:OP[3:0], which determined the logical rank MBIST was last run on.
6. After CWL (CL-2), DQ[3:0] of the individual target device must be LOW for $8t^{\text{CK}}$. Only devices that most recently have had an MR22 transparency result of 001b may be considered "target DRAMs". If more than one device shares the same command bus, devices that are not being repaired must have DQ[3:0] driven HIGH for $8t^{\text{CK}}$. If all of the DQ[3:0] data bits are neither all LOW nor all HIGH for $8t^{\text{CK}}$, the mPPR mode execution is unknown. For x8 and x16 devices, data bits other than DQ[3:0] are don't cares. Note: a previous version of the specification required all DQs to be HIGH or LOW; this was changed to DQ[3:0] to accommodate ECC UDIMMs and SODIMMs.
7. Wait $t^{\text{SELFREPAIR}}$ to allow the device to self repair the address(es) identified internally by MBIST, and then issue a PREab command.
8. Wait $t^{\text{PGM\_exit}}$ after PREab command to allow the device to update MR22 transparency status.
9. Exit mPPR by setting MR23:OP[3]=0. Wait t^{PGMPST} .
10. Read MR22 transparency status.
11. If additional fails remain, the controller may repeat steps 2-10. If no fails remain or the controller chooses not to perform additional mPPR, the device may continue to the next planned operation.

Figure 199: mPPR Row Repair Timing

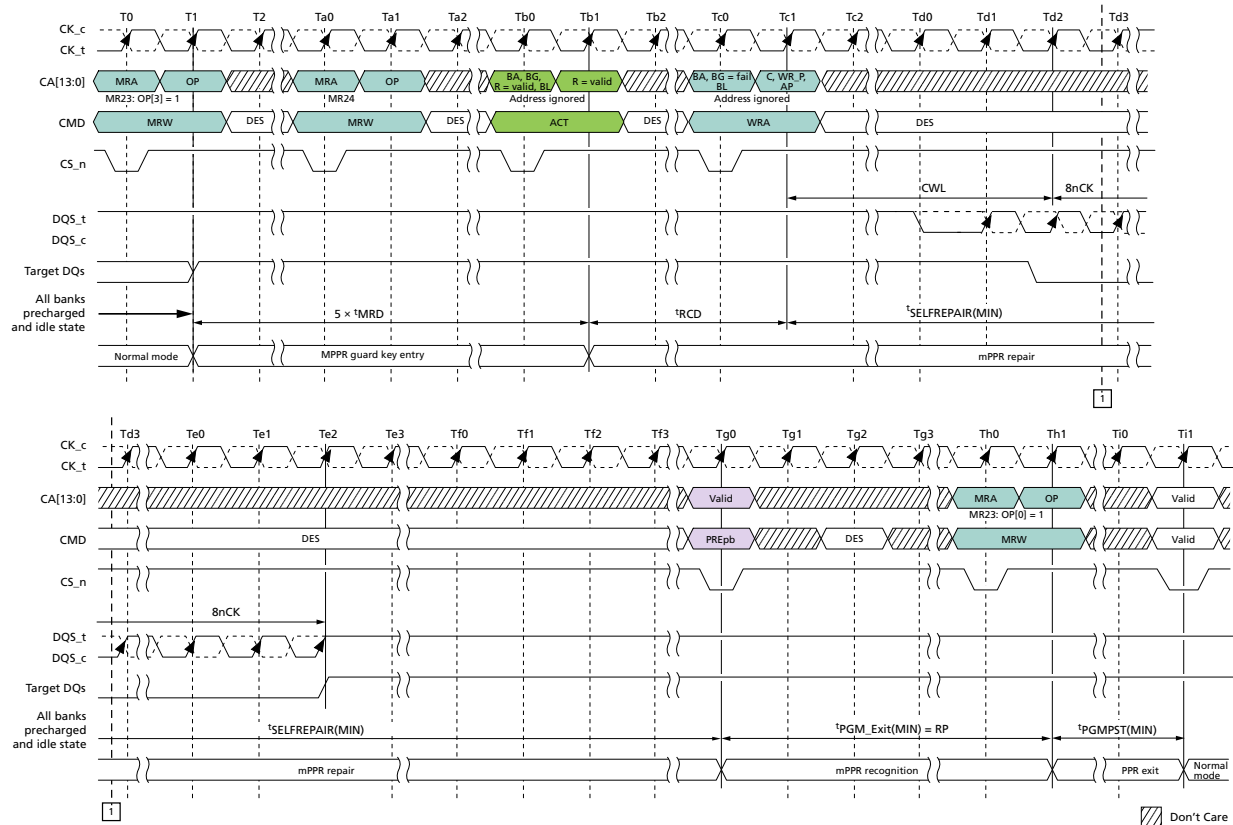
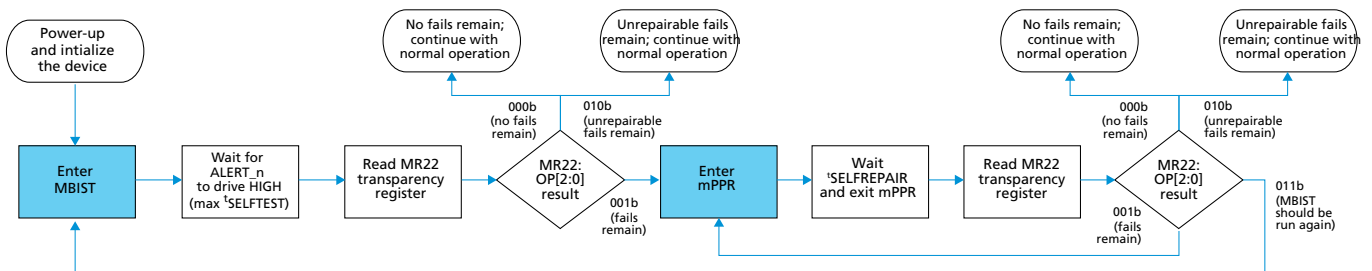


Table 273: mPPR Timings

Parameter	Symbol	3200-8800		Unit
		MIN	MAX	
mPPR programming time: x4,x8,x16	$t_{\text{SELFREPAIR}}$	1000	-	ms

The figure below shows a detailed flow chart of the MBIST/mPPR sequence.

Figure 200: MBIST/mPPR Sequence



Notes: 1. mPPR may only be performed after an MR22:OP[2:0] transparency result of 001b.

2. 011b = **MBIST should be run again** indicates that fails were repaired with mPPR, but MBIST should be run again to load internal fail addresses for mPPR.

-
3. 010b = **Unrepairable fails remain** indicates there are not enough mPPR elements remaining to repair addresses latched during MBIST. It may be updated in MR22:OP[2:0] after either MBIST or mPPR, depending on vendor implementation.

DLL Modes

DLL Reset

DLL reset is performed via an MPC command. Any time the DLL RESET function is used, t_{DLLK} must be met before functions requiring the DLL can be used, including READ, WRITE, MRR, RD-NT, WR-NT, and MRR-NT.

On-Die Termination

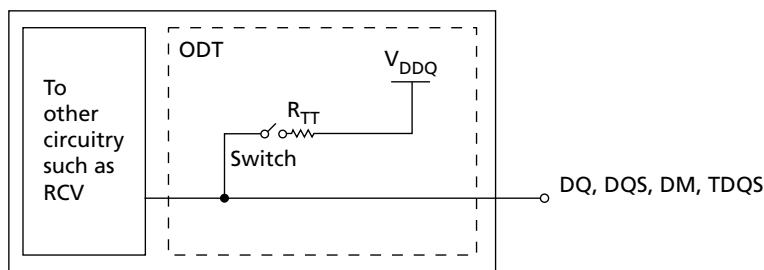
On-Die Termination for DQ, DQS, DM and TDS

On-die termination (ODT) enables the DRAM to change termination resistance for each DQ, DQS, DM and TDQS pin. Unlike previous DDR technologies, DDR5 no longer has a physical ODT pin, and all ODT-based control is now command- and mode register-based. For x4 and x8 configuration devices, ODT is applied to each DQ, DQS_t, DQS_c and DM_n, as well as TDQS_t, TDQS_c for x8 configuration). For x16 configuration devices, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n. ODT is enabled via non-target READ/MODE REGISTER READ commands, WRITE and NON-TARGET WRITE commands, or is set to the default PARK value through settings in MR33-MR35.

The ODT feature is designed to improve signal integrity of the memory channel by enabling the device controller to independently change termination resistance for any or all devices. In addition to the control capability of the DQ ODT, the DQS ODT is now independently programmed via MR33:OP[5:3] and held static. All ODT control is targeted for the DQs. This addition enables adjusting the delay common in an unmatched architecture. DQS RTT offset control mode is enabled via MR40:OP[2:0].

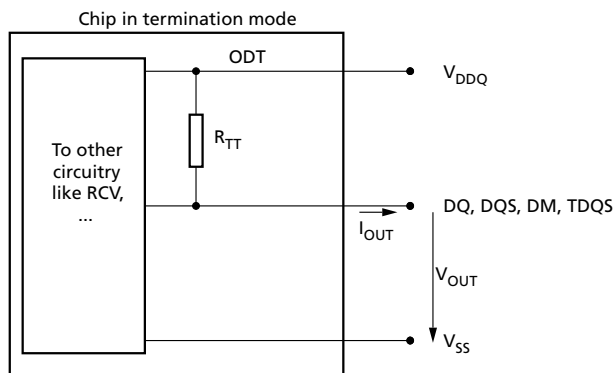
The ODT feature is turned off and not supported in self refresh mode, but does have an optional mode when in power-down. The figure below shows a simple functional representation of the ODT feature.

Figure 201: Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses command decode, mode register settings and other control information (see below). The value of R_{TT} is determined by the settings of mode register bits.

Figure 202: On Die Termination



Note: 1. Supported on die termination effective R_{TT} values are: 240, 120, 80, 60, 48, 40, 34 ohms.

Table 274: ODT Electrical Characteristics $R_{ZQ} = 240\Omega \pm 1\%$ Entire Temperature Range, After Proper ZQ Calibration

RTT	V _{OUT}	MIN	Nom	MAX	Unit	Notes
240 Ω	$V_{OLdc} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	R_{ZQ}	1,2,3
	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	R_{ZQ}	1,2,3
	$V_{OHdc} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	R_{ZQ}	1,2,3
120 Ω	$V_{OLdc} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/2$	1,2,3
	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/2$	1,2,3
	$V_{OHdc} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/2$	1,2,3
80 Ω	$V_{OLdc} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/3$	1,2,3
	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/3$	1,2,3
	$V_{OHdc} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/3$	1,2,3
60 Ω	$V_{OLdc} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/4$	1,2,3
	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/4$	1,2,3
	$V_{OHdc} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/4$	1,2,3
48 Ω	$V_{OLdc} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/5$	1,2,3
	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/5$	1,2,3
	$V_{OHdc} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/5$	1,2,3
40 Ω	$V_{OLdc} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/6$	1,2,3
	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/6$	1,2,3
	$V_{OHdc} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/6$	1,2,3
34 Ω	$V_{OLdc} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/7$	1,2,3
	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/7$	1,2,3
	$V_{OHdc} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/7$	1,2,3
DQ-DQ mismatch within byte	$V_{OMdc} = 0.8 \cdot V_{DDQ}$	0	—	8	%	1,2,4,5,6

- Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the ZQ Calibration Commands section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at $0.8 \cdot V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.5 \cdot V_{DDQ}$ and $0.95 \cdot V_{DDQ}$.
3. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$.
4. DQ to DQ mismatch within byte variation for a given component including DQS_t and DQS_c (characterized).
5. RTT variance range ratio to RTT nominal value in a given component, including DQS_t and DQS_c.

$$\text{DQ-DQ mismatch in a byte} = \frac{R_{TT\_MAX} - R_{TT\_MIN}}{R_{TT\_NOM}} \times 100$$

6. This parameter of x16 device is specified for upper byte and lower byte.

ODT Modes, Timing Diagrams and State Table

ODT mode has five states: data/strobe termination disable, RTT_{WR}, RTT_{NOM_RD}, RTT_{NOM_WR} and RTT_{PARK/DQS_RTTPARK}. ODT mode is enabled based on mode registers for each RTT listed below. In this case, the value of RTT is determined by the settings of those mode register bits.

After entering self-refresh mode, the device automatically disables ODT termination and sets Hi-Z as termination state regardless of these settings.

Application: Controller can control each RTT condition with the WRITE (WR), READ (RD), or MODE REGISTER READ (MRR) commands use of ODT offset control mode registers.

- Data Termination Disable: Device driving data upon receiving READ command disables the termination after CL-1 and re-enables the termination at CL + BL/2 (CL and BL defined in clock cycles).
- Strobe Termination Disable: Device driving strobe upon receiving READ command disables the termination after CL-1-^tRPRE-(Read_DQS_Offset) and re-enables the termination at CL+BL/2-0.5+^tRPST-(Read_DQS_Offset) (CL and BL defined in clock cycles).
- RTT_WR: The rank that is being written to provides termination and adjusts timing based on the ODT control mode register settings.
- RTT_NOM_RD: The device turns this on if it sees CS asserted during the second pulse of the READ command (except when ODT is disabled by MR35:OP[5:3]).
- RTT_NOM_WR: The device turns this on if it sees a CS asserted during the second pulse of the WRITE command (except when ODT is disabled by MR35:OP[2:0]).
- RTT_PARK: The default parked value (set via MR34[2:0]) to be enabled when a READ or WRITE is not active.
- DQS_RTT_PARK: The default parked value (set for DQS via MR33:OP[5:3]); it is enabled when a READ or WRITE is not active.

The RTT values have priority as follows:

1. Data termination disable and strobe termination disable
2. RTT_WR
3. RTT_NOM_RD
4. RTT_NOM_WR
5. RTT_PARK and DQS_RTT_PARK

This means if there is WRITE command, the device turns on RTT_WR (not RTT_NOM_RD or RTT_NOM_WR). Additionally, if there is READ command, the device disables data termination and enters driving mode.

If during the second cycle of a WRITE, READ or MODE REGISTER READ command the CS is held LOW, the NT ODT is enabled and the appropriate RTT_NOM_WR or RTT_NOM_RD is enabled for the non-target rank. This provides additional—and potentially different—term options for the other ranks on the channel.

Table 275: Termination State Table

Command	Mode Register Configuration Settings				Results		Notes
	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Target DRAM Term	Non-Target DRAM Term	
Any	Disabled				Hi-Z (ODT off)		3
Any non-term CMD	Enabled	Don't care			RTT_PARK	RTT_PARK	4
WR	Disabled			Don't care	Hi-Z (ODT off)	Hi-Z (ODT off)	
	Disabled		Enabled	Don't care	Hi-Z (ODT off)	RTT_NOM_WR	
	Disabled	Enabled	Disabled	Don't care	RTT_WR	Hi-Z (ODT off)	
	Don't care	Enabled		Don't care	RTT_WR	RTT_NOM_WR	2
	Enabled		Disabled	Don't care	RTT_WR	Hi-Z (ODT off)	2, 5
	Enabled	Disabled	Enabled	Don't care	RTT_PARK	RTT_NOM_WR	
	Enabled	Disabled		Don't care	RTT_PARK	Hi-Z (ODT off)	5

Table 275: Termination State Table (Continued)

Command	Mode Register Configuration Settings				Results		Notes
	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Target DRAM Term	Non-Target DRAM Term	
RD/MRR	Enabled	Don't care		Disabled	Hi-Z (ODT off)	Hi-Z (ODT off)	1, 5
	Don't care			Enabled	Hi-Z (ODT off)	RTT_NOM_RD	1

- Notes: 1. When a READ command is executed, the termination state of the target rank is Hi-Z for a defined period, independent of the MR setting of RTT_PARK / RTT_NOM_RD / RTT_NOM_WR.
2. If RTT_WR is enabled, RTT_WR is activated by a WRITE command for a defined period of time, independent of the MR setting of RTT_PARK / RTT_NOM_RD / RTT_NOM_WR.
3. If all RTT configurations are disabled, ODT receiver power is turned off to save power.
4. If RTT_PARK is enabled, RTT_PARK termination is enabled while WR / RD / MRR are not being executed.
5. When a non-target ODT command is executed and the RTT_NOM_WR or RTT_NOM_RD is disabled, the termination state of the non-target rank is Hi-Z for a defined period, independent of the MR setting of RTT_PARK.

On-die termination effective resistance RTT is defined by MR bits.

ODT is applied to the DQ, DQS_t / DQS_c, DM and TDQS_t / TDQS_c (x8 devices only) pins.

A functional representation is shown in the [On-Die Termination figure](#).

$$RTT = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the device's termination strength can be changed without issuing an MRW command. This is supported by dynamic ODT mode, which is described as follows:

- Five RTT values are available: RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK, and DQS_RTT_PARK.
 - The value for RTT_NOM_RD is preselected via MR35:OP[5:3]
 - The value for RTT_NOM_WR is preselected via MR35:OP[2:0]
 - The value for RTT_WR is preselected via MR34:OP[5:3]
 - The value for RTT_PARK is preselected via MR34:OP[2:0] - Programmed via MPC
 - The value for DQS_RTT_PARK is preselected via MR33:OP[5:3] - programmed via MPC
- During operation without commands, termination is controlled as follows;
 - Nominal termination strength for all types (RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK, and DQS_RTT_PARK) are selected
 - RTT_NOM_RD and RTT_NOM_WR on/off timings are controlled via the respective NT READ and NT WRITE command and latencies
 - DQS_RTT_PARK is held static and is based on the value programmed in the MR listed above
- With a WRITE command, termination is controlled as follows:
 - A latency ODTLon_WR after the WRITE command, termination strength RTT_WR is selected
 - A latency ODTLoff_WR after the WRITE command termination strength RTT_WR is deselected
- The termination, RTT_NOM_WR, for the WRITE NT command is selected and de-selected by latencies ODTLon_WR_NT and ODTLoff_WR_NT, respectively
- When a READ command (RD) is registered, termination is controlled as follows:

- A latency ODTLoff_RD after the READ command, data termination is disabled. Next, ODTLon_RD after the READ command, data termination is enabled.
- A latency ODTLoff_RD_DQS after the READ command, strobe termination is disabled. ODTLon_RD_DQS after the READ command, strobe termination is enabled.
- The termination, RTT_NOM_RD, for the READ NT command is selected and de-selected by latencies ODTLon_RD_NT and ODTLoff_RD_NT, respectively.

The duration of a WRITE or READ command is a full burst cycle (BL/2). The termination select (ODTLon_...) and de-select (ODTL-off-...) latency settings do not result in an ODT pulse width which violates a burst cycle (BL/2) minimum duration. The equation $ODTLoff\_X - ODTLon\_X \geq BL/2$ must be met, where X is the termination latency setting associated with a particular command type (WR, WR_NT, RD_NT).

To achieve the minimum write burst duration, ODTLoff_X and ODTLon_X latencies contain independent programmable mode register offsets:

- The values for the WRITE command ODT control offsets are preselected via MR37.
 - MR37:OP[2:0] preselects ODTLon_WR_Offset
 - MR37:OP[5:3] preselects ODTLoff_WR_Offset
- The values for the WRITE NT command ODT control offsets are preselected via MR38.
 - MR38:OP[2:0] preselects ODTLon_WR_NT_Offset
 - MR38:OP[5:3] preselects ODTLoff_WR_NT_Offset
- The values for the READ NT command ODT control offsets are preselected via MR39.
 - MR39:OP[2:0] preselects ODTLon_RD_NT_Offset
 - MR39:OP[5:3] preselects ODTLoff_RD_NT_Offset

The combination of allowable ODT offsets are shown in the table below.

Table 276: Allowable Write ODTL Offset Combinations

Setting		ODTLon_WR_Offset Setting						
		-4	-3	-2	-1	0	1	2
ODTLoff_WR_Offset	4	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	3	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid	Valid	Invalid
	0	Valid	Valid	Valid	Valid	Valid	Invalid	Invalid
	-1	Valid	Valid	Valid	Valid	Invalid	Invalid	Invalid
	-2	Valid	Valid	Valid	Invalid	Invalid	Invalid	Invalid

Note: 1. The Write ODTLon -4 offset and Write ODTLoff +4 offset is not allowed for 1980-2100 data rates.

Table 277: Allowable Write NT ODTL Offset Combinations

Setting		ODTLon_WR_NT_Offset Setting						
		-4	-3	-2	-1	0	1	2
ODTLoff_WR_NT_Offset	4	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	3	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid	Valid	Invalid
	0	Valid	Valid	Valid	Valid	Valid	Invalid	Invalid
	-1	Valid	Valid	Valid	Valid	Invalid	Invalid	Invalid
	-2	Valid	Valid	Valid	Invalid	Invalid	Invalid	Invalid

Note: 1. The Write NT ODTLon -4 offset and Write NT ODTLoff +4 offset is not allowed for 1980-2100 data rates.

Table 278: Allowable Read ODTL Offset Combinations

Setting		ODTLon_WR_NT_Offset Setting				
		-3	-2	-1	0	1
ODTLoff_RD_NT_Offset	3	Valid	Valid	Valid	Valid	Valid
	2	Valid	Valid	Valid	Valid	Valid
	1	Valid	Valid	Valid	Valid	Valid
	0	Valid	Valid	Valid	Valid	Invalid
	-1	Valid	Valid	Valid	Invalid	Invalid

See the table below for ODT latency and timing parameter details.

Table 279: Latencies and Timing Parameters Relevant for Dynamic ODT and CRC Disabled

Name and Description	Abbreviation	Defined From	Defined to	Speed Bins	Unit	Note
				3200-8800		
ODT Latency On from WRITE command to R _{TT} Enable	^t ODTLon_WR	Registering external WRITE command	Change R _{TT} strength from previous state to R _{TT} _WR	^t ODTLon_WR = CWL + ODTLon_WR_offset	nCK	1
ODT Latency On from WRITE NT command to R _{TT} Enable	^t ODTLon_WR_NT	Registering external WRITE command	Change R _{TT} strength from previous state to R _{TT} _NOM_WR	^t ODTLon_WR_NT = CWL + ODTLon_WR_NT_offset		1
ODT Latency Off from WRITE command to R _{TT} Disable	^t ODTLoff_WR	Registering external WRITE command	Change R _{TT} strength from R _{TT} _WR to R _{TT} _PARK/ R _{TT} _NOM_RD/ R _{TT} _NOM_WR/ Hi-Z	^t ODTLoff_WR = CWL + BL/2 + ODTLoff_WR_offset	nCK	1
ODT Latency Off from WRITE NT command to R _{TT} Disable	^t ODTLoff_WR_NT	Registering external WRITE command	Change R _{TT} strength from R _{TT} _NOM_WR to R _{TT} _PARK/ R _{TT} _NOM_RD/ R _{TT} _WR/ Hi-Z	^t ODTLoff_WR_NT = CWL + BL/2 + ODTLoff_WR_NT_offset		1
Data Termination Disable	^t ODTLoff_RD	Registering external READ command	Disables termination upon driving data	^t ODTLoff_RD = CL - 1		2
Data Termination Enable	^t ODTLon_RD	Registering external READ command	Re-enables termination after driving data	^t ODTLon_RD = CL + BL/2		2

Table 279: Latencies and Timing Parameters Relevant for Dynamic ODT and CRC Disabled (Continued)

Name and Description	Abbreviation	Defined From	Defined to	Speed Bins	Unit	Note
				3200-8800		
Strobe Termination Disable	$t_{\text{ODTLoFF\_RD\_DQS}}$	Registering external READ command	Disables termination upon driving strobe	$t_{\text{ODTLoFF\_RD\_DQS}} = \text{CL} - 1 - t_{\text{RPRE}} - (\text{Read DQS Offset})$		2
Strobe Termination Enable	$t_{\text{ODTLon\_RD\_DQS}}$	Registering external READ command	Re-enables termination after driving strobe	$t_{\text{ODTLon\_RD\_DQS}} = \text{CL} + \text{BL}/2 + t_{\text{RPST}} - 0.5 - (\text{Read DQS Offset})$		2
ODT Latency On from READ NT command to R_{TT} Enable	$t_{\text{ODTLon\_RD\_NT}}$	Registering external READ command	Change R_{TT} strength from previous state to RTT_NOM_RD	$t_{\text{ODTLon\_RD\_NT}} = \text{CL} + \text{ODTLon\_RD\_NT\_offset}$	nCK	1
ODT Latency Off from READ NT command to R_{TT} Disable	$t_{\text{ODTLoFF\_RD\_NT}}$	Registering external READ command	Change R_{TT} strength from RTT_NOM_RD to $\text{RTT\_PARK}/\text{RTT\_NOM\_WR}/\text{RTT\_WR}/\text{HIZ}$	$t_{\text{ODTLoFF\_RD\_NT}} = \text{CL} + \text{BL}/2 + \text{ODTLoFF\_RD\_NT\_offset}$		1

Notes: 1. All _offset parameters refer to the ODT Configuration mode registers settings in MR37-MR39.

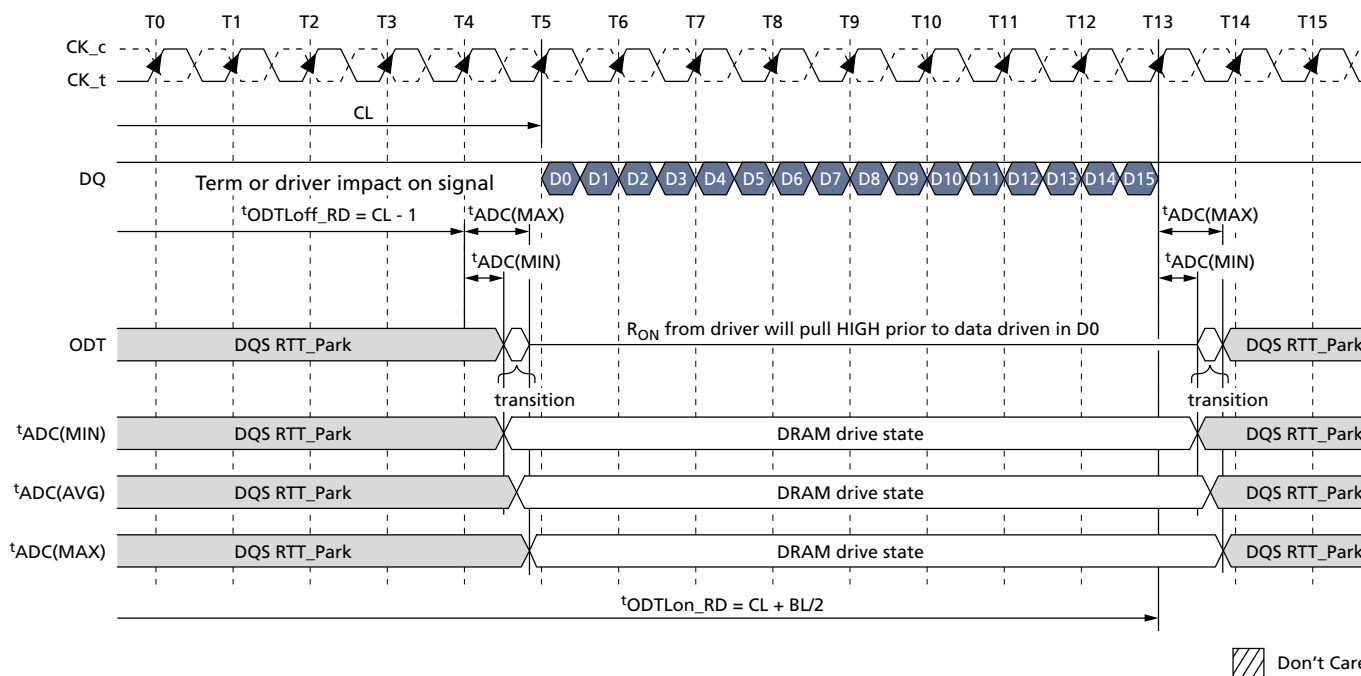
2. For simplicity, READS are assigned the same type of timing parameter; however, unlike others, it is a fixed timing and does not have an offset mode register to control it. To indicate this, it was named Data (or Strobe) termination Disable and Enable.

ODT t_{ADC} Clarifications

t_{ADC} is defined as the time it takes for the device to transition from one R_{TT} state to the next R_{TT} state. In the case of a READ command, it is the time from the current R_{TT} state to the device drive state. Unless the R_{TT} is specifically disabled, no HIGH-Z state is allowed during t_{ADC} . During the device drive state, the R_{ON} will keep the DQ signal HIGH prior to the first DQ transition. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Below is an example showing the t_{ADC} (MIN), t_{ADC} (AVG) and t_{ADC} (MAX) with respect to the R_{TT} status and effects on the DQ lines prior to the burst.

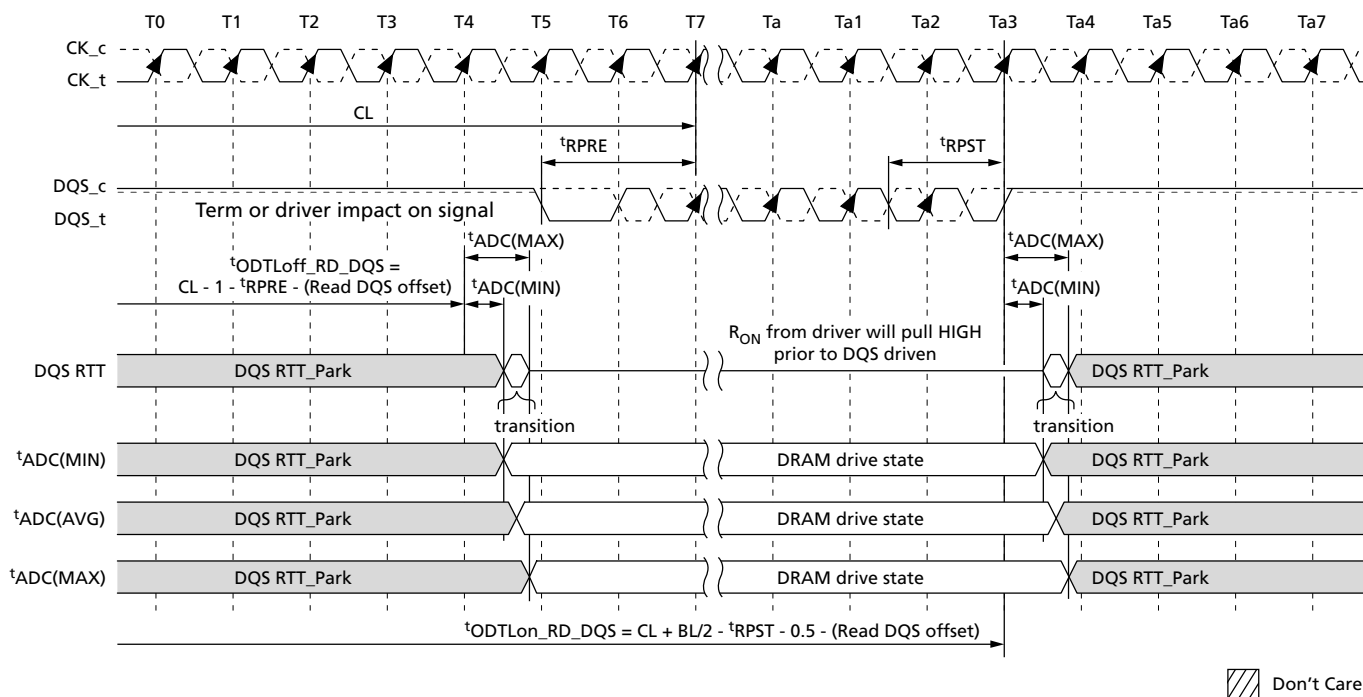
Figure 203: t_{ADC} Clarification - Example 1 DQ R_{TT} Park to Read



- Notes: 1. The diagram shows a transition from RTT_PARK to READ command enabled drive state. When t_{ADC} transitions from RTT to drive state, the R_{ON} from the driver will keep the DQ signal HIGH prior to the data driven in D0. No HIGH-Z time during t_{ADC} is allowed in this example.
2. In the case of term to WRITE, the host keeps the DQ signal HIGH 4UI prior to the data driven in D0.
3. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Below is an example showing the t_{ADC} (MIN), t_{ADC} (AVG) and t_{ADC} (MAX) with respect to the RTT status and effects on the DQS lines prior to the burst.

Figure 204: t_{ADC} Clarification - Example 1 DQS RTT Park to Read



- Note: 1. The diagram shows a transition from DQS RTT_PARK to READ command enabled drive state. When t_{ADC} transitions from RTT to READ command enabled drive state, the R_{ON} from the driver keeps the DQS signal HIGH prior to the DQS driven at t_5 . No HIGH-Z time during t_{ADC} is allowed in this example.

ODT Timing Diagrams

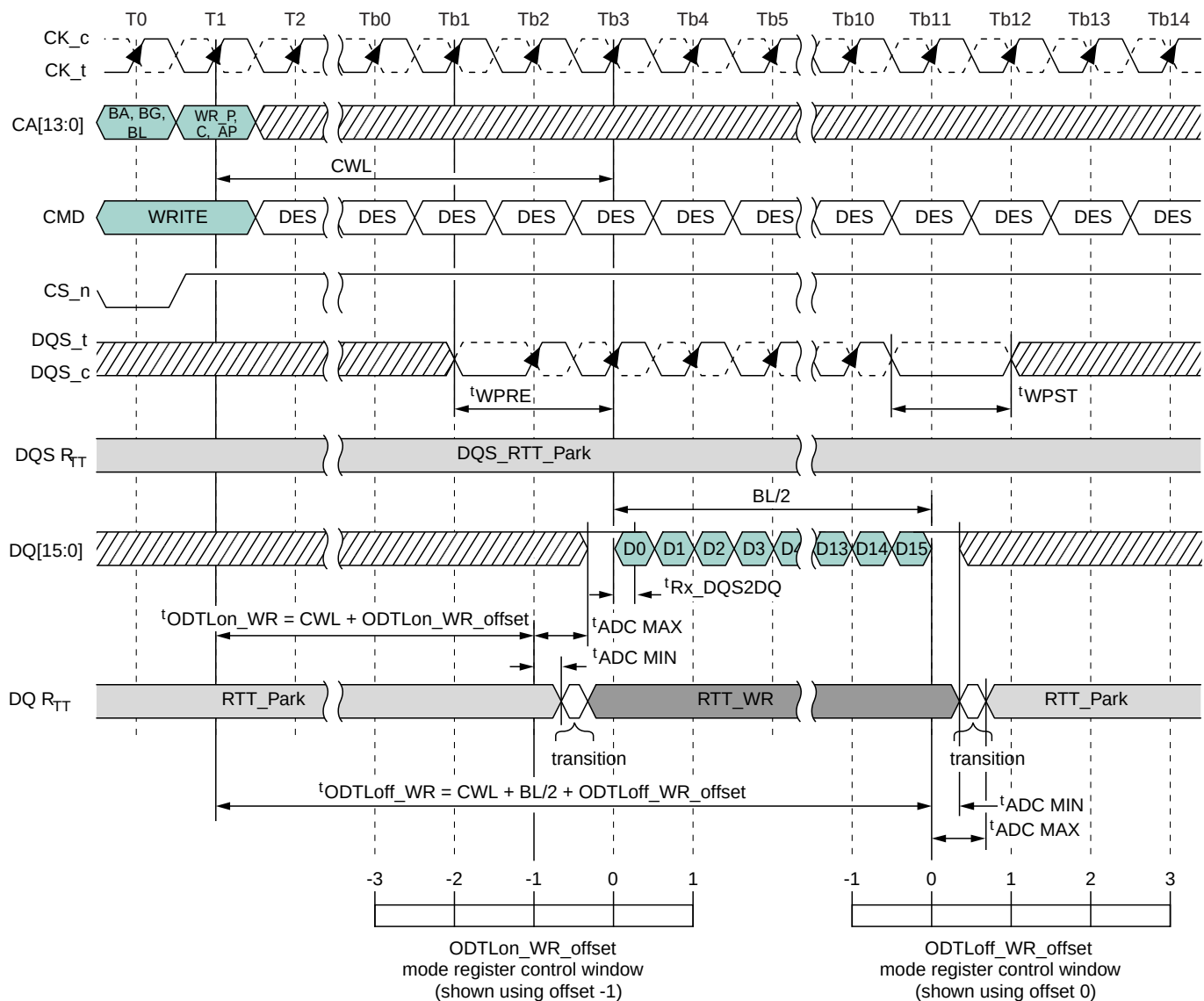
This section provides examples of ODT utilization timing diagrams. Examples of WRITE to WRITE, READ to WRITE and READ to READ are provided for clarification only. Implementations may vary, including termination on other DIMMS.

It is the controller's responsibility to manage command spacing and the programmable aspect of $t_{ODTLon/off}$ times to ensure that preambles and postambles are included in the RTT ON time.

When a 1 t_{CK} ODT control gap for any ODT operation exists (such as shown in the WRITE (BL16) to WRITE (BL16), Different Bank, 2 t_{CK} Gap figure), the gap's RTT value is the same or smaller (weaker termination) than RTT_PARK.

All timings noted in the following figures are for reference only.

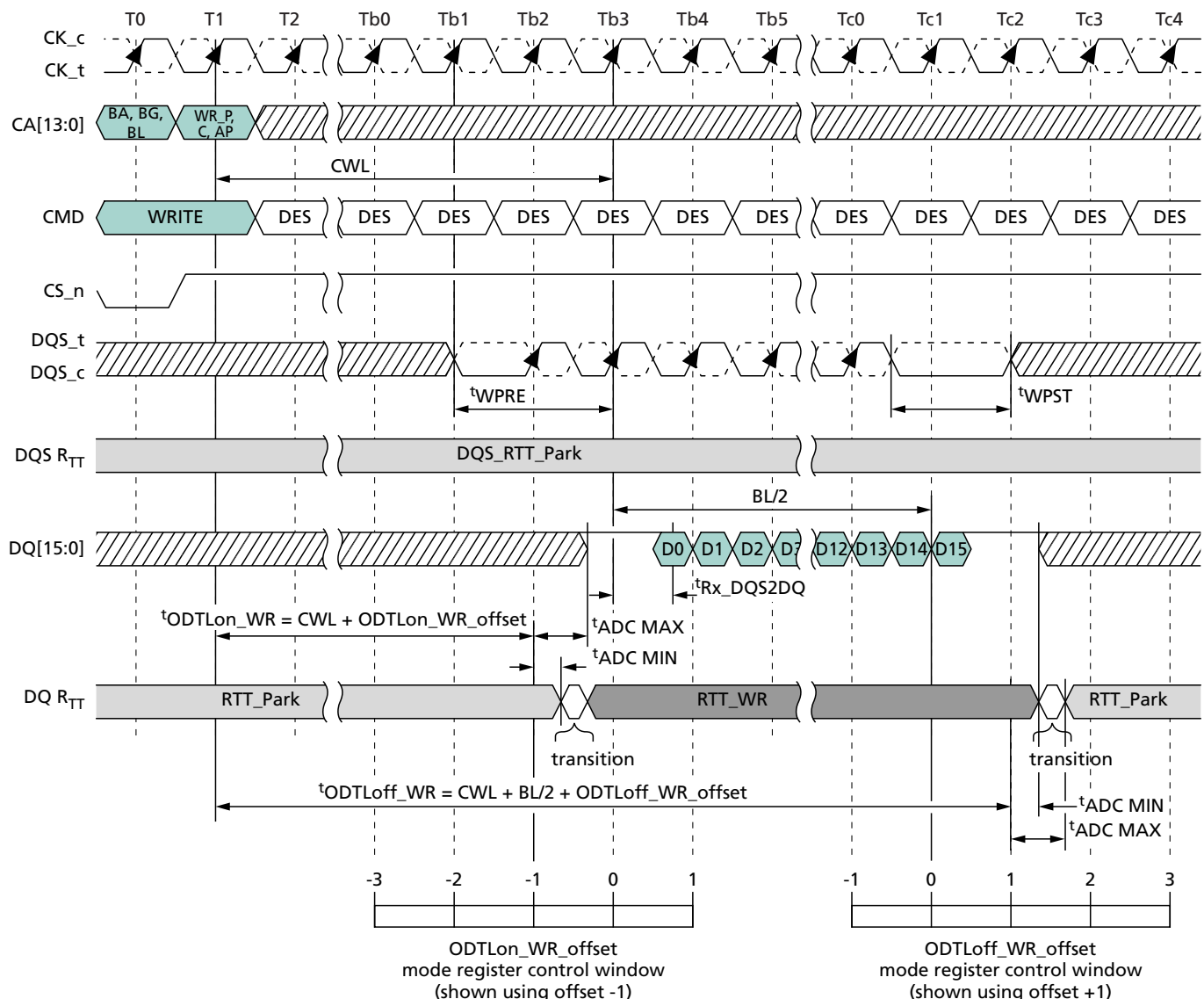
Figure 205: Example 1 — Burst WRITE Operation ODT Latencies and Control Diagrams



}} Time Break Don't Care

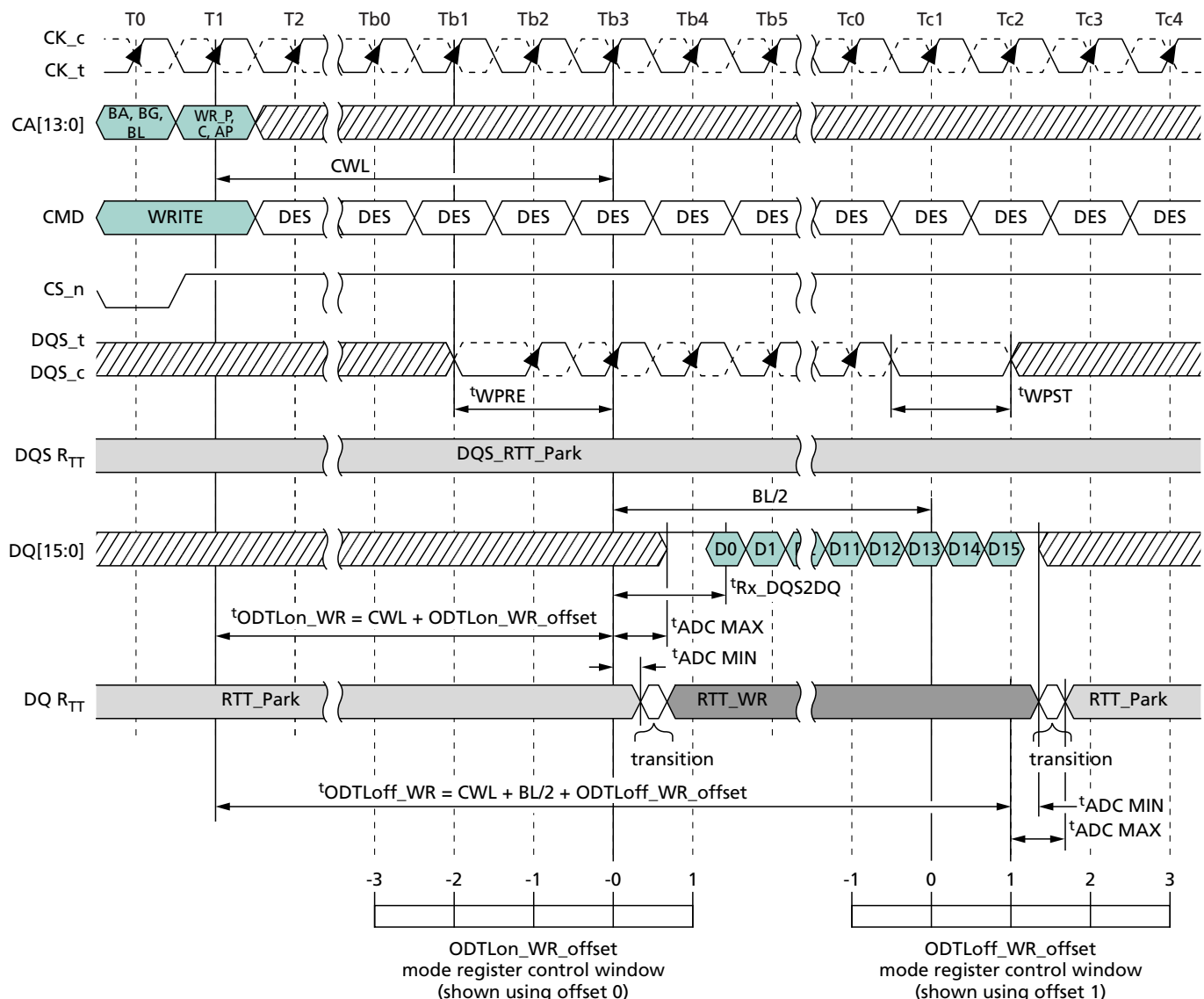
- Notes: 1. For simplicity, the entire range of ODTL control is not shown.
2. Example details - 2^tCK t_{WPRE} , 1.5^tCK t_{WPST} , $0.5UI$ t_{RX_DQS2DQ} , $ODTLon\_WR\_offset$ configured for -1. $ODTLoFF\_WR\_offset$ configured for 0. Example shows how the host may aggressively adjust the offset of the t_{ODTLon_WR} timing to give t_{ADC} the minimum time to settle before data.
3. System designs and margins may vary requiring larger RTT_WR windows.

Figure 206: Example 2 — Burst WRITE Operation ODT Latencies and Control Diagrams



- Notes:
- For simplicity, the entire range of ODTL control is not shown.
 - Example details - 2^tCK t_{WPRE} , 1.5^tCK t_{WPST} , $1.5UI$ t_{RX_DQS2DQ} , $ODTL_{on\_WR\_offset}$ configured for -1. $ODTL_{off\_WR\_offset}$ configured for +1. Example shows how the host may want to add an offset to the $t_{ODTLoFF\_WR}$ time so that RTT_WR stays on for the actual burst.
 - System designs and margins may vary requiring larger RTT_WR windows.

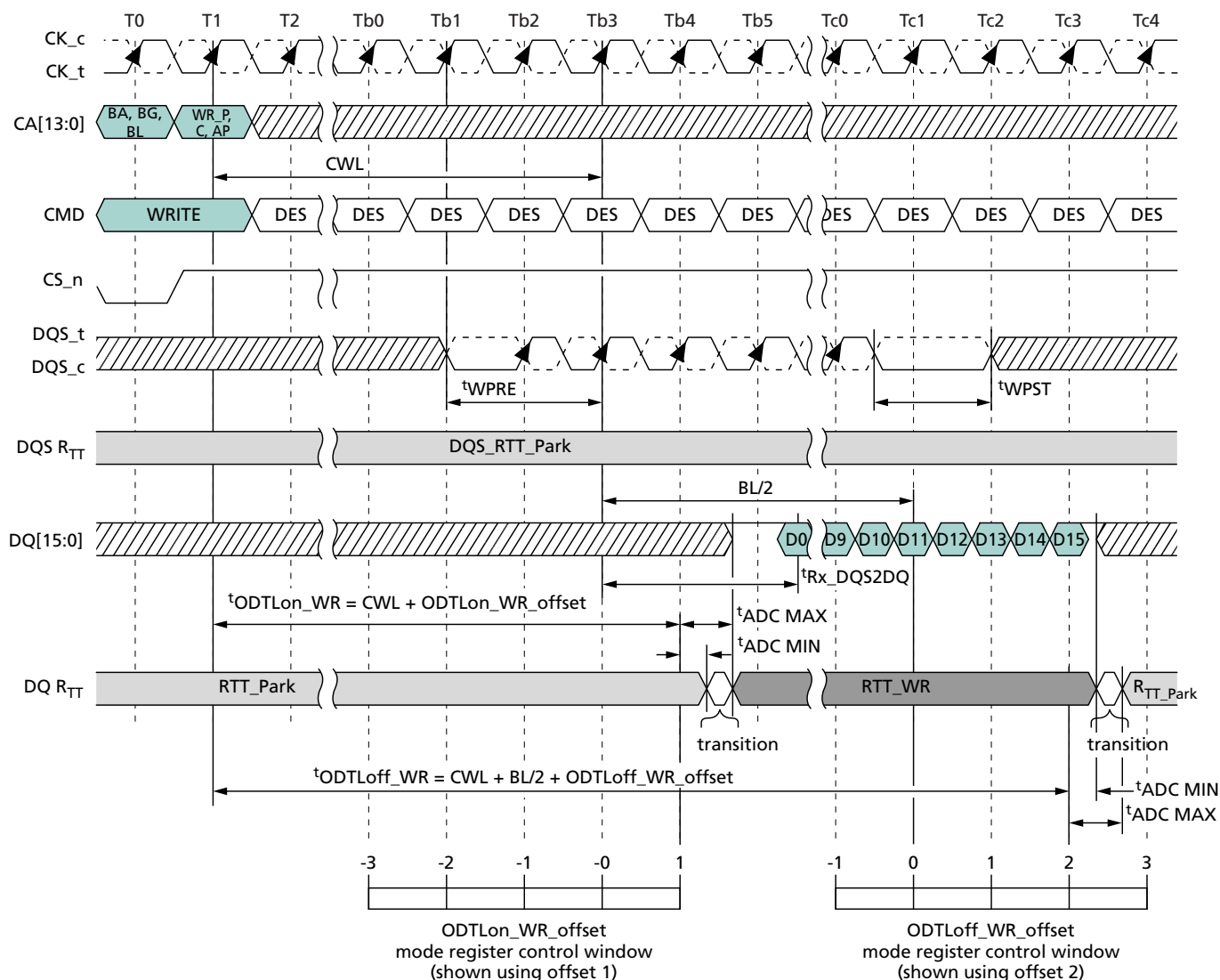
Figure 207: Example 3 — Burst WRITE Operation ODT Latencies and Control Diagrams



}} Time Break Don't Care

- Notes:
- For simplicity, the entire range of ODTL control is not shown.
 - Example details - 2^tCK t_{WPRE} , 1.5^tCK t_{WPST} , $3UI$ t_{RX_DQS2DQ} , $ODTLon\_WR\_offset$ configured for 0. $ODTLoFF\_WR\_offset$ configured for +1. Example shows how the host could leave the RTT_WR ON time to default values with no offset and may want to add an offset to the $t_{ODTLoFF\_WR}$ time so that RTT_WR remains ON for the actual burst.
 - System designs and margins may vary requiring larger RTT_WR windows.

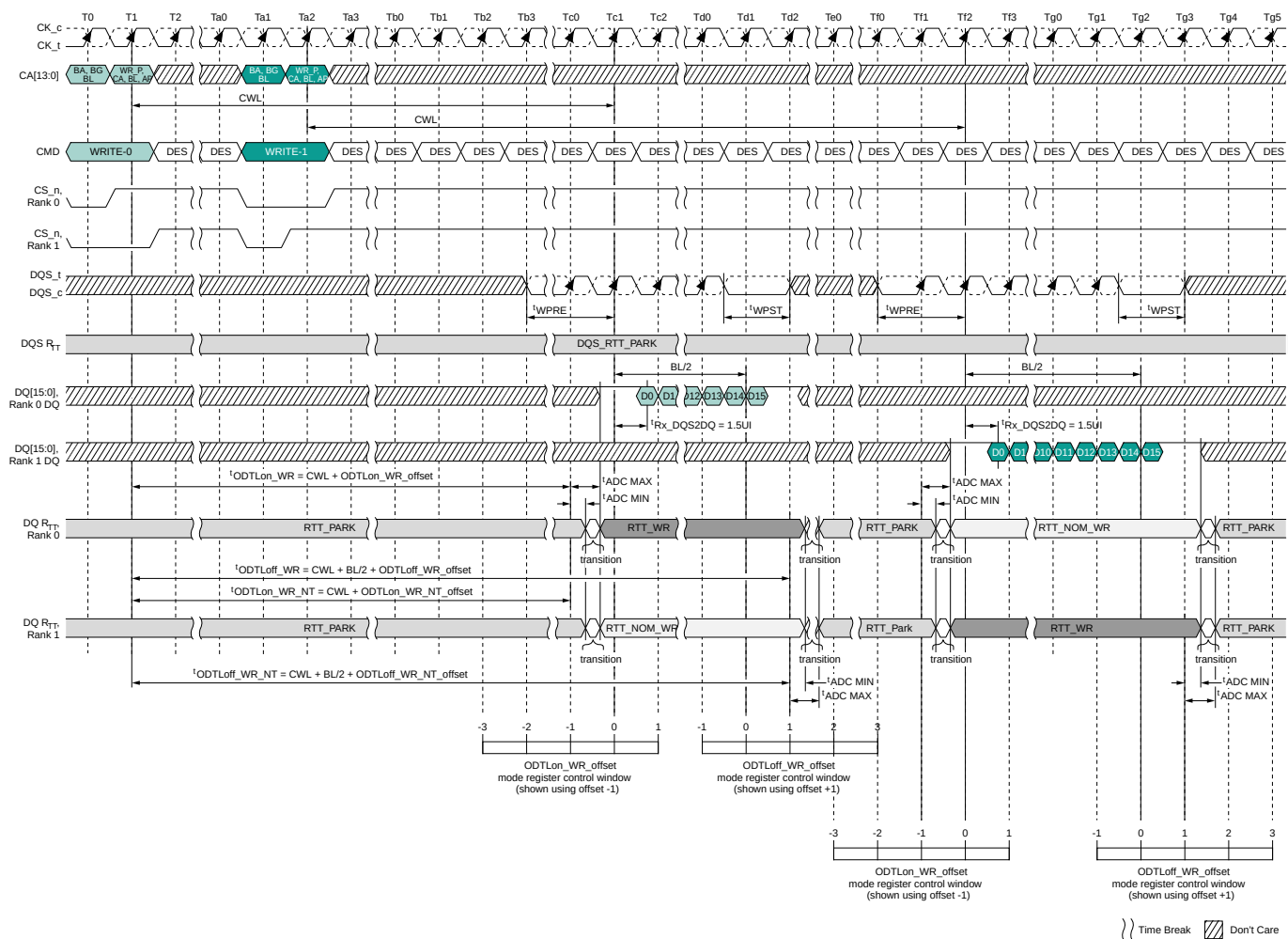
Figure 208: Example 4 — Burst WRITE Operation ODT Latencies and Control Diagrams



Time Break Don't Care

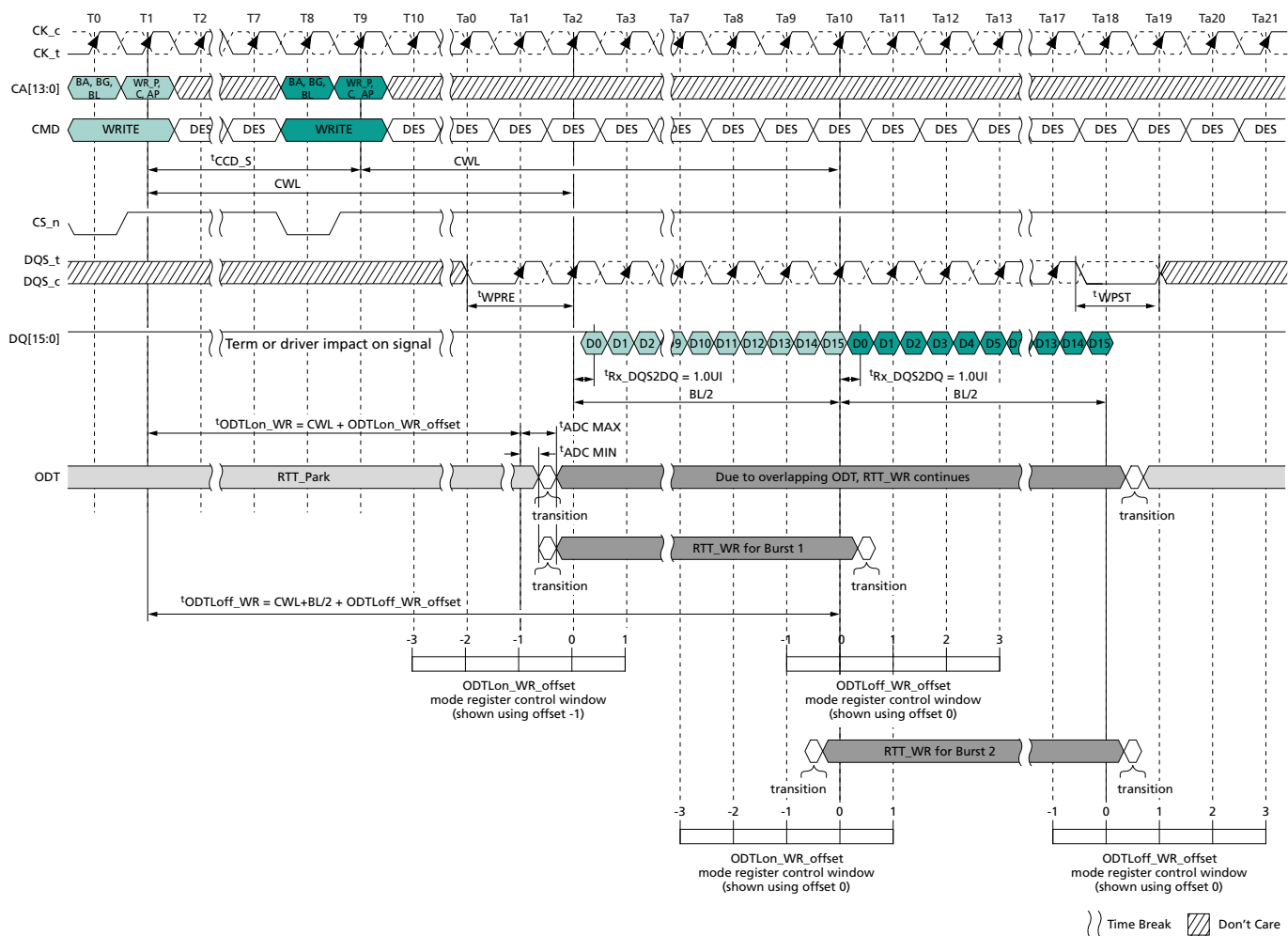
- Notes:
- For simplicity, the entire range of ODTL control is not shown.
 - Example details - $2t_{CK}$ t_{WPRE} , $1.5t_{CK}$ t_{WPST} , $5UI$ t_{RX_DQS2DQ} , $ODTLon\_WR\_offset$ configured for +1. $ODTLoFF\_WR\_offset$ configured for +2. Example shows an extreme case where data is significantly delayed from DQS and how the host may want to add an offset to the t_{ODTLon_WR} time so that RTT_WR doesn't turn ON too early and how the host may want to delay the $t_{ODTLoFF\_WR}$ time so that it remains ON for the entire burst.
 - System designs and margins may vary requiring larger RTT_WR windows.

Figure 209: Example of WRITE to WRITE Turn Around, Different Ranks



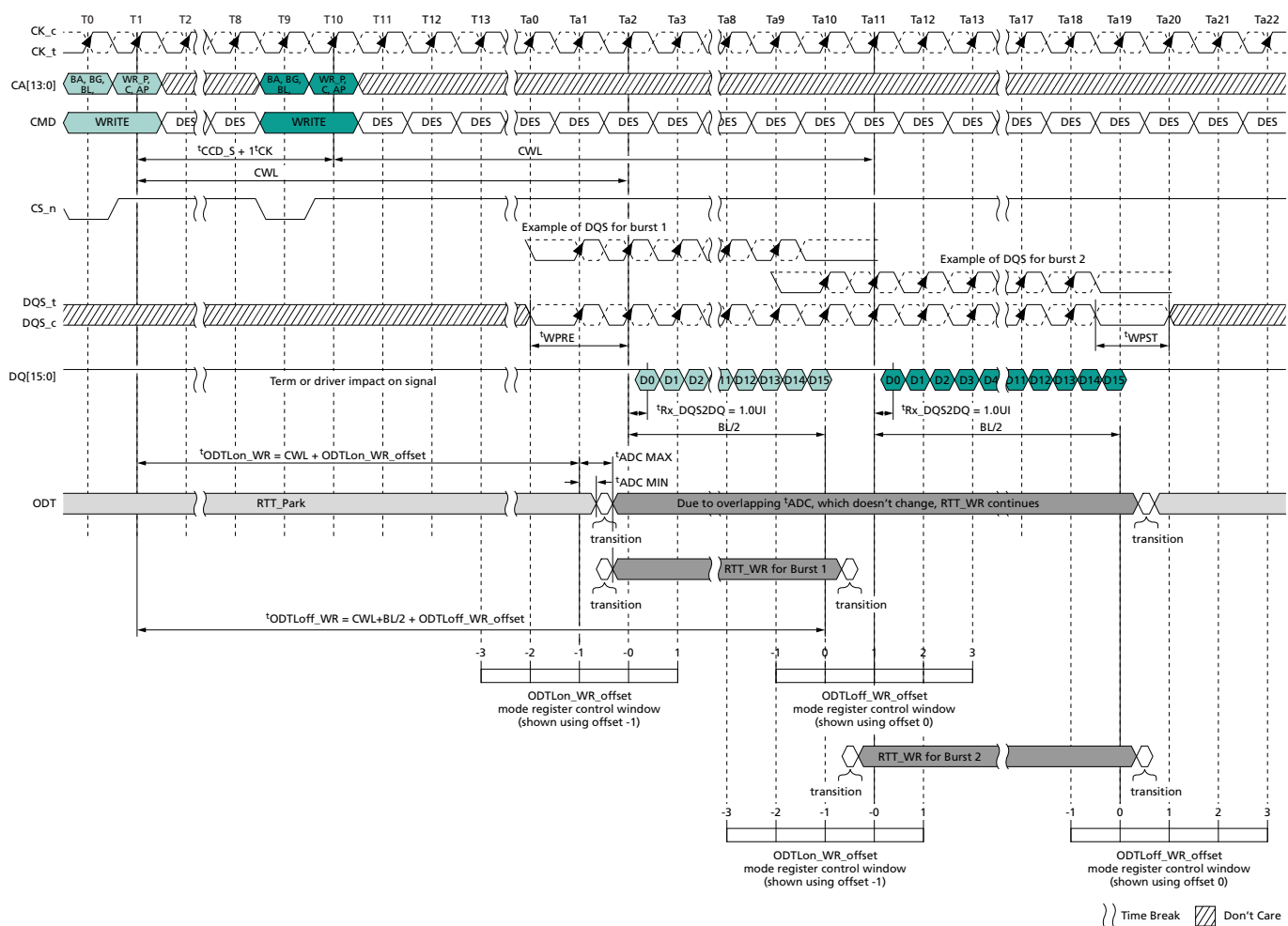
- Notes: 1. ODTLon_WR, ODTLon_WR_NT, ODTLoFF_WR and ODTLoFF_WR_NT are based on mode register settings that can push out or pull in the RTT enable and disable time.
2. For simplicity, the entire range of ODTL control is not shown.

Figure 210: WRITE (BL16) to WRITE (BL16), Different Bank, Seamless Bursts



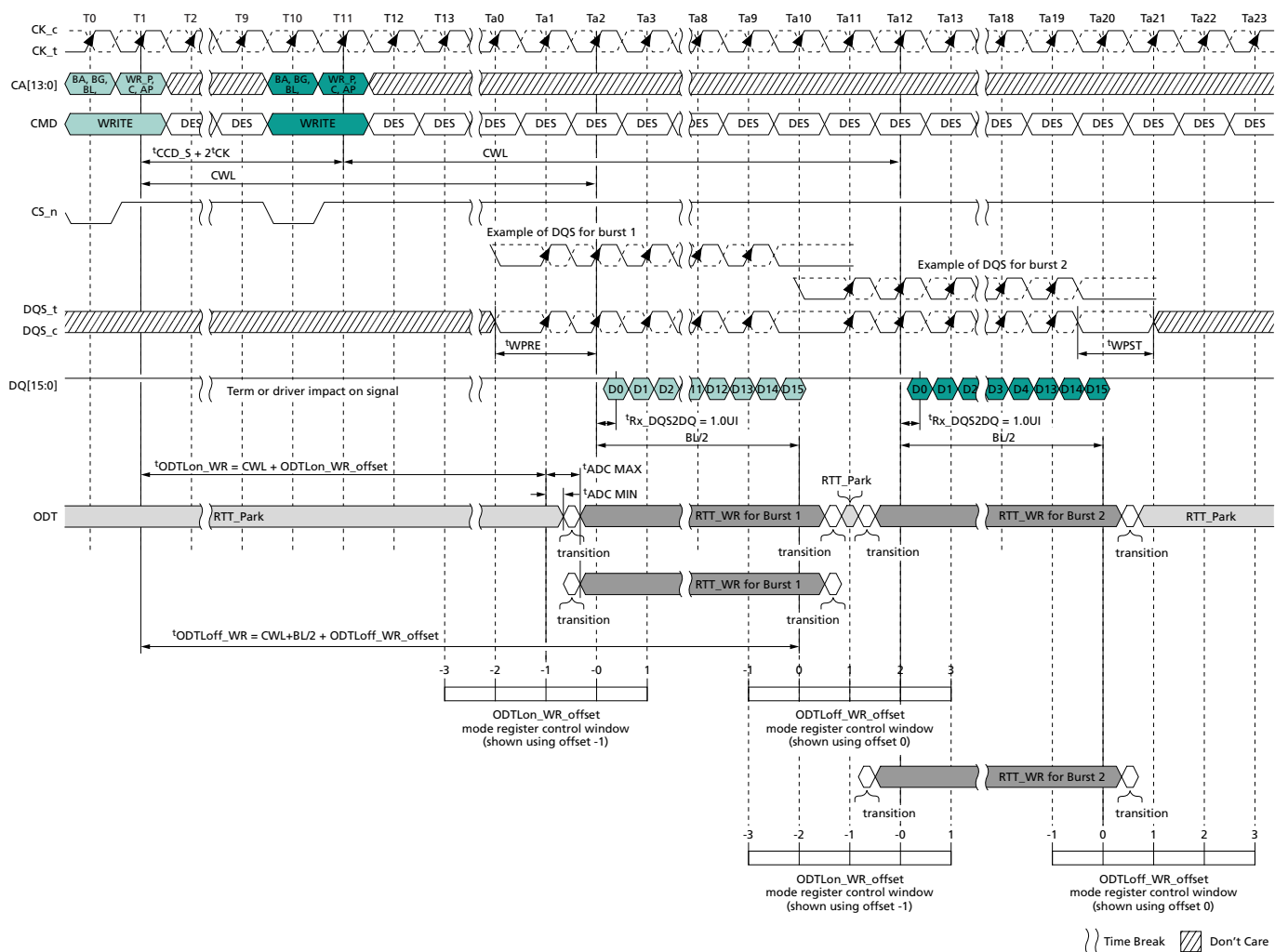
- Notes:
1. BL = 16, preamble = $2 \times CK - 0010$ pattern, postamble = $1.5 \times CK$
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.
 3. $ODT_{Lon\_WR\_offset} = -1$, $ODT_{LoFF\_WR\_offset} = 0$, $t_{RX\_DQS2DQ} = 1.0UI$
 4. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
 5. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 211: WRITE (BL16) to WRITE (BL16), Different Bank, 1 t_{CK} Gap



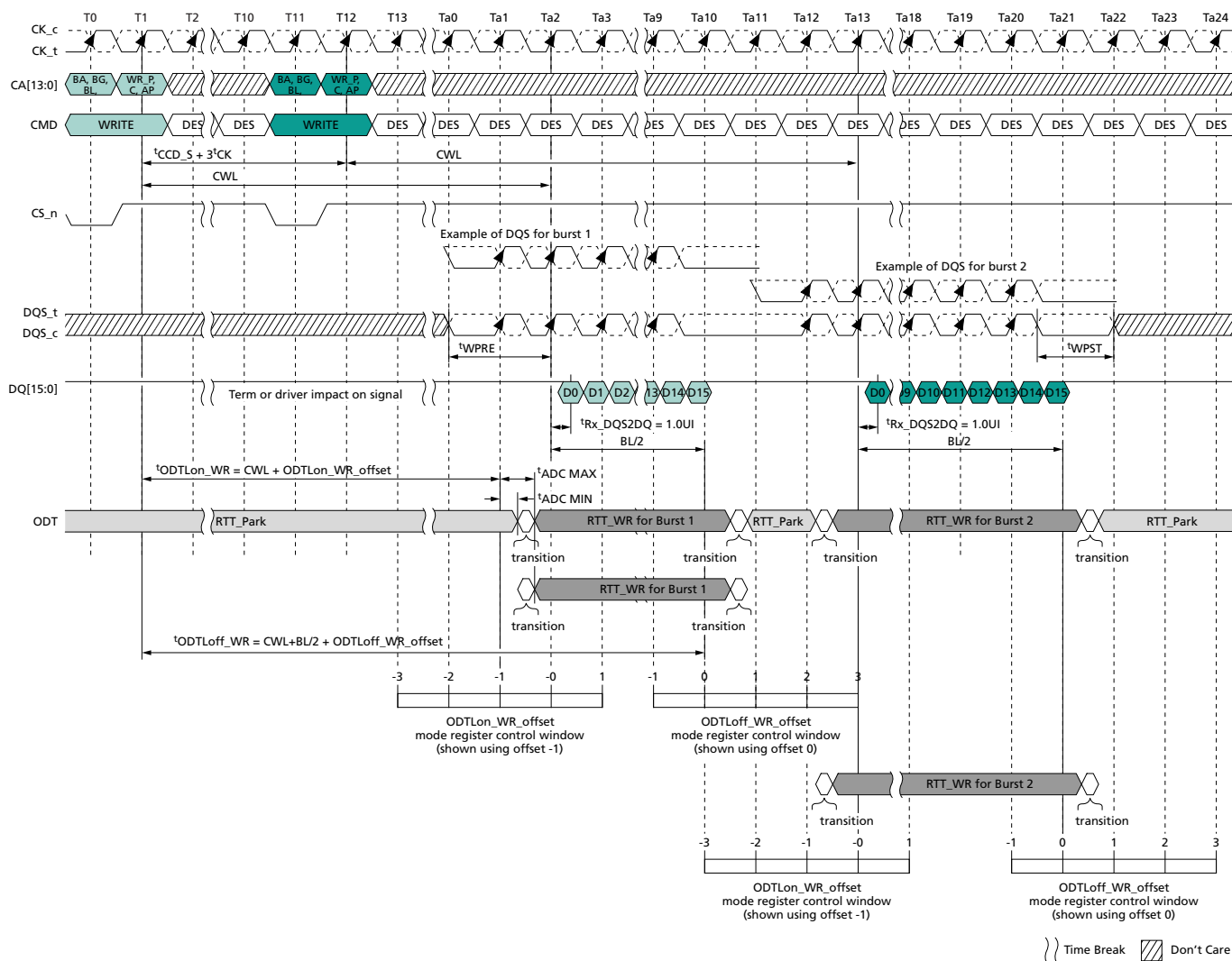
- Notes:
1. BL = 16, preamble = $2 t_{CK}$ - 0010 pattern, postamble = $1.5 t_{CK}$
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.
 3. $ODT_{Lon\_WR\_offset} = -1$, $ODT_{Loff\_WR\_offset} = 0$, $t_{RX\_DQS2DQ} = 1.0UI$
 4. Example DQS bursts are shown for clarification purposes and are not part of an actual signal.
 5. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
 6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 212: WRITE (BL16) to WRITE (BL16), Different Bank, 2 t^{CK} Gap



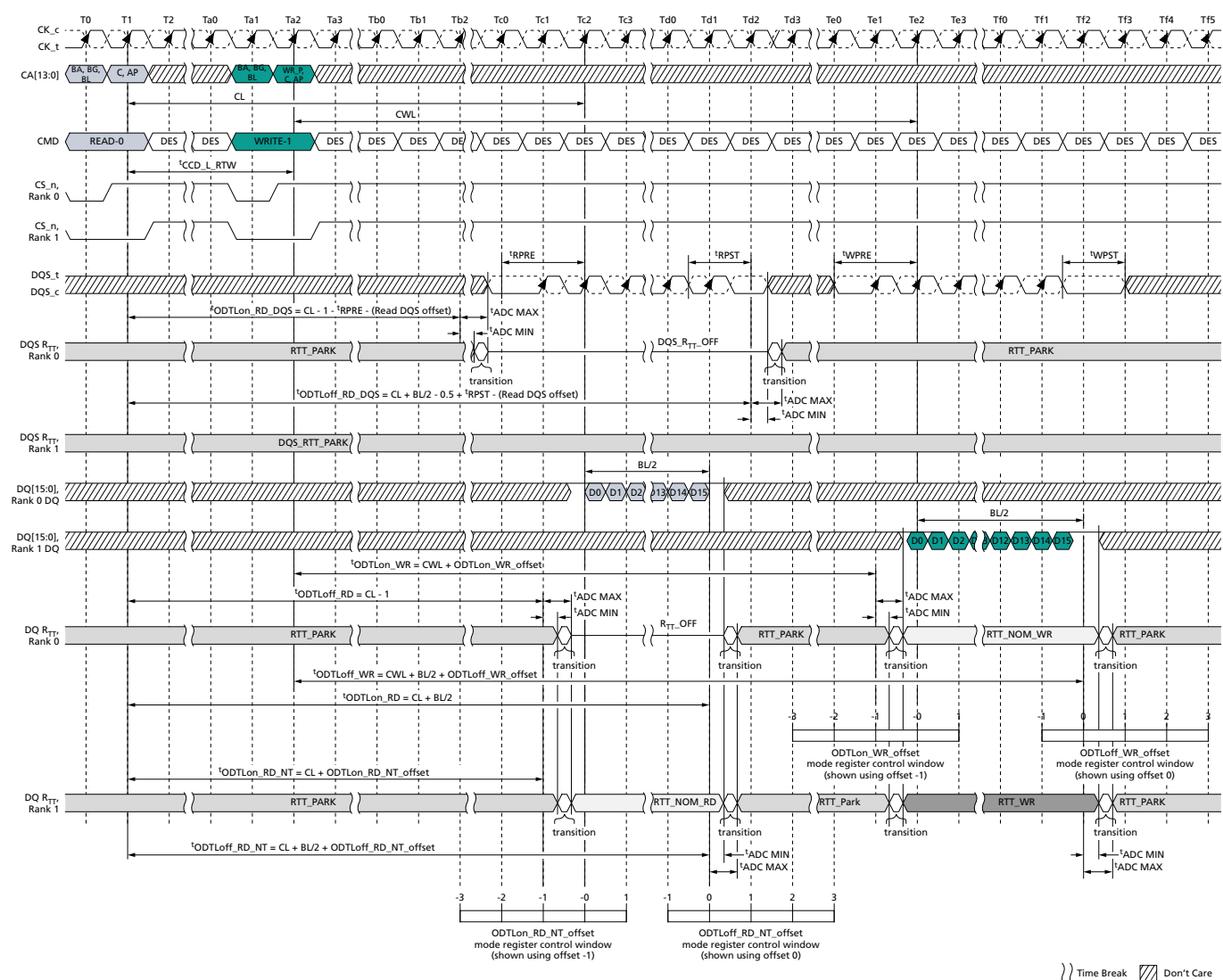
- Notes:
1. BL = 16, preamble = $2 t^{\text{CK}}$ - 0010 pattern, postamble = $1.5 t^{\text{CK}}$
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.
 3. $ODTLoFF\_WR\_offset = -1$, $ODTLoFF\_WR\_offset = 0$, $t^{\text{Rx}}_{DQS2DQ} = 1.0UI$
 4. Example DQS bursts are shown for clarification purposes and are not part of an actual signal.
 5. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
 6. The DFE should assume that 4UI prior to D0 the signal is HIGH.
 7. When a 1 t^{CK} ODT control gap for any ODT operation exists (such as shown in this figure), the gap's RTT value is the same or smaller (weaker termination) than RTT_PARK .

Figure 213: WRITE (BL16) to WRITE (BL16), Different Bank, 3 t_{CK} Gap



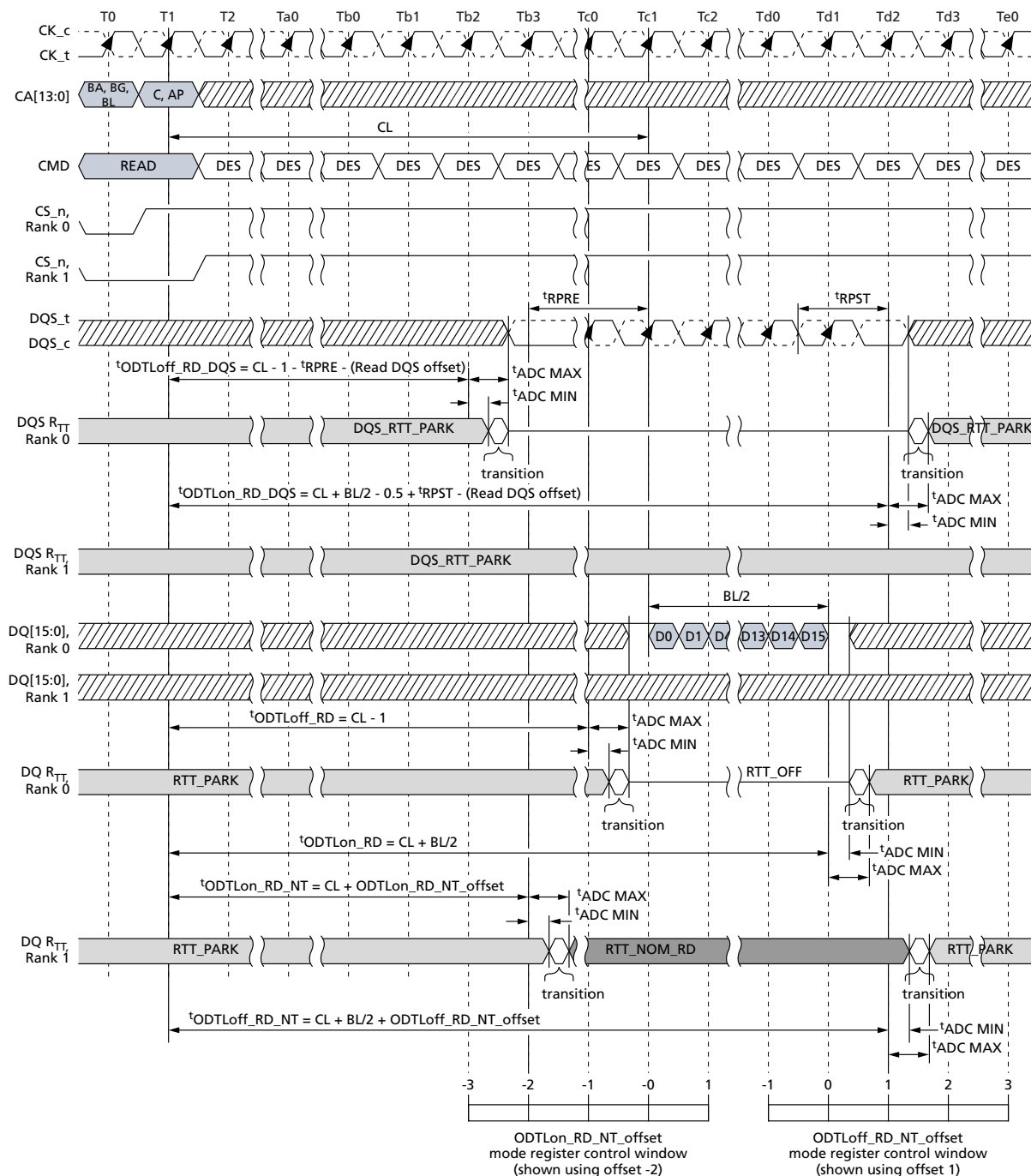
- Notes:
1. BL = 16, preamble = $2t_{CK}$ - 0010 pattern, postamble = $1.5t_{CK}$
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.
 3. $ODTLon\_WR\_offset = -1$, $ODTLoFF\_WR\_offset = 0$, $t_{RX\_DQS2DQ} = 1.0UI$
 4. Example DQS bursts are shown for clarification purposes and are not part of an actual signal.
 5. In a term-to-WRITE case, the host keeps the DQ signal HIGH 4UI prior to the data being driven in D0.
 6. The DFE should assume that 4UI prior to D0 the signal is HIGH.

Figure 214: Example of READ to WRITE turn around, Different Ranks



- Notes:
1. $ODTLoN\_WR$, $ODTLoN\_WR\_NT$, $ODTLoF\_WR$ and $ODTLoF\_WR\_NT$ are based on mode register settings that can push out or pull in the RTT enable and disable time.
 2. $ODTLoN\_RD\_NT$ and $ODTLoF\_RD\_NT$ are based on mode register settings that can push out or pull in the RTT enable and disable time.
 3. For simplicity, $ODTLoN\_WR\_offset$ and $ODTLoF\_WR\_offset$ not shown.
 4. Example shown with near ideal timings for termination settings, exact offset configurations will vary based on system designs.

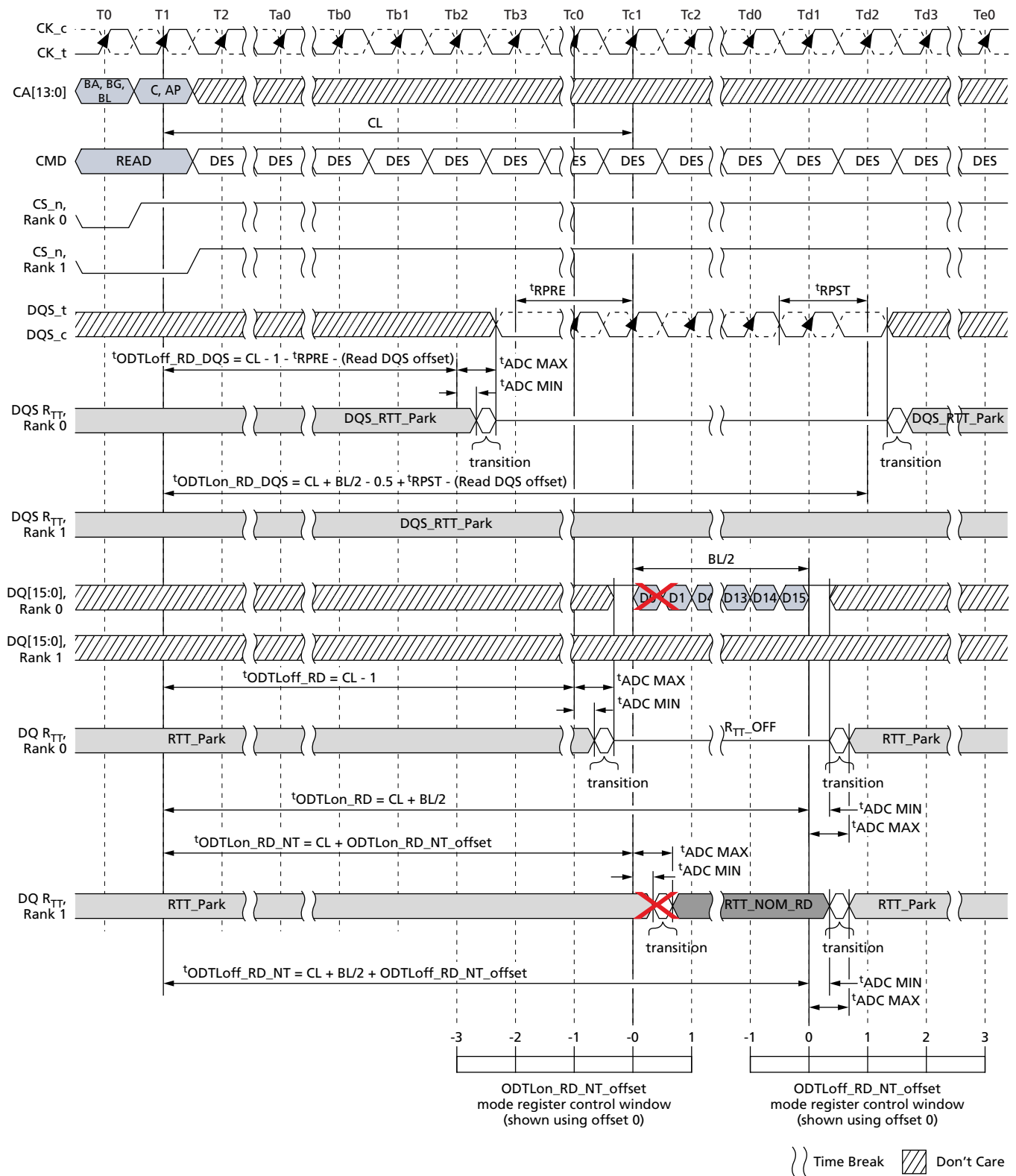
Figure 215: Example of Burst Read Operation ODT Latencies and Control Diagrams



Notes: 1. For simplicity, the entire range of ODTL control is not shown.

2. Example shown with NT_ODT overlapping normal read disable by 1t_{CK} on both sides (ODTLon_RD_NT_offset = -2 and ODTLoFF_RD_NT_offset = +1).

Figure 216: Example of Burst Read Operation with ODTLon_RD_NT_offset Set Incorrectly



Notes: 1. For simplicity, the entire range of ODTL control is not shown.

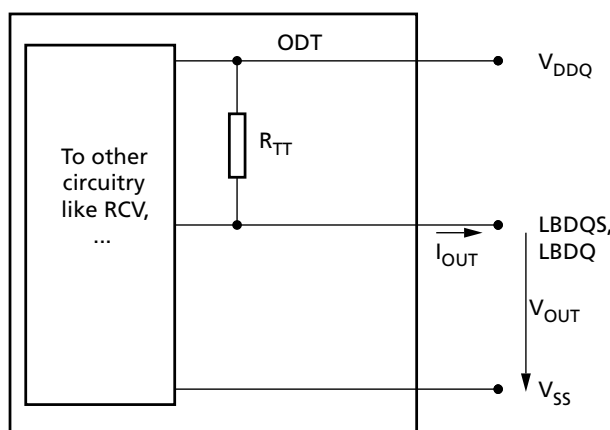
2. Since the ODTLon_RD_NT_Offset was left at zero offset and t_{ADC} still had to be considered, the RTT NT turned on too late for the non-target device. t_{ADC} is not instantaneous.
3. Since the $t_{ODTLoFF\_RD\_NT}$ is referenced from the CL, it is not affected by the offset used for the 'on' time and would turn off 1 clock earlier than the read disable RTT if programed to zero offset. $t_{ODTLoN\_RD\_NT}$ and $t_{ODTLoFF\_RD\_NT}$ are independently set and calculated from CL.

On-Die Termination Loopback Signals

The device includes on-die termination (ODT) resistance for the loopback signals LBDQS and LBDQ.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via MR settings.

Figure 217: Functional Representation of Loopback ODT



The ODT resistance during power up is set to the default R_{TT_OFF} values based on MR36:OP[2:0] definition. The ODT resistance values can be configured by MR36:OP[2:0].

The ODT effective resistance R_{TT} is defined by MR36:OP[2:0] bits = 48 Ohms. ODT is applied to loopback signals LBDQS and LBDQ. ODT effective R_{TT} values supported for the loopback pins is 48 ohms.

$$R_{TT} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

Table 280: ODT Electrical Characteristics $R_{ZQ} = 240\Omega \pm 1\%$ Entire Temperature Operation Range; After Proper ZQ Calibration; $V_{DD} = V_{DDQ}$

R_{TT} (Ohms)	V_{OUT}	Min	Nom	Max	Unit	Notes
48	$V_{OL,DC} = 0.5 \cdot V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/5$	1,2
	$V_{OM,DC} = 0.8 \cdot V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/5$	1,2
	$V_{OH,DC} = 0.95 \cdot V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/5$	1,2
Mismatch LBDQS to LBDQ within Device	$V_{OM,DC} = 0.8 \cdot V_{DDQ}$	0	–	8	%	1,2,3

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the ZQ Calibration Commands section on voltage and temperature sensitivity.

2. Pull-up ODT resistors are recommended to be calibrated at $0.8 \cdot V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above; that is, calibration at $0.5 \cdot V_{DDQ}$ and $0.95 \cdot V_{DDQ}$.

3. Loopback ODT mismatch within device variation for a given component including LBDQS and LBDQ.

$$\text{LBDQS} - \text{LBDQ mismatch in a device} = \frac{R_{\text{TT\_MAX}} - R_{\text{TT\_MIN}}}{R_{\text{TT\_NOM}}} \times 100$$

CA ODT Strap Operation

With the introduction of on-die termination for CA/CS/CK on DDR5 devices, the setting of the termination values per DRAM is different depending on the configuration of DRAMs on the DIMM or system board.

The CA_ODT pin enables the distinction of two sets of CA/CS/CK ODT settings. When the CA_ODT pin is strapped to a constant V_{SS} setting on the DIMM or board, CA/CS/CK ODT setting is referred to as Group A. When the CA_ODT pin is strapped to a constant V_{DDQ} setting on the DIMM or system board, CA/CS/CK ODT setting is referred to as Group B.

Typical usage is to apply a weak termination setting to Group A devices and a stronger termination setting to Group B devices, which would be at the end of the fly-by routing on the DIMM. To support these different settings, two sets of MPC opcodes are used to target either Group A or Group B devices. In addition to these separate groups of devices based on the CA_ODT pin, PDA commands are also supported. However, the correct combination of the PDA Select ID and MPC opcode must be used according to the CA_ODT pin value.

For DDP devices, CA_ODT package pin ties to both top die and bottom die CA_ODT bond pads. CS_n and CS1_n being defined in DDP package ballout. CS is not shared between dies, and each die terminated individually. CK is shared between both dies and both dies terminated. CA is shared between both dies and both dies terminated. Host can program optimal ODT value after initialization.

See CA_ODT pin definition below.

Table 281: CA ODT Pin Definition

Pin Name	Input/Output	Description
CA_ODT	Input	ODT for command and address. Apply group A settings if the pin is connected to V_{SS} . Apply group B settings if the pin is connected to V_{DDQ} .

MR32 and MR33 are defined as follows to show encoding settings for CA,CS,CK and to reflect the need to read the CA_ODT strap value.

Table 282: MR32 Mode Register Settings (For Reference Only)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA_ODT Strap Value	CS ODT			CK ODT		

Table 283: MR33 Mode Register Settings (For Reference Only)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		DQS_RTT_PARK			CA ODT		

If CA_ODT Strap Value MR32:OP[6] is 0, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for Group A ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Set A CK/CS/CA ODT settings.

If CA_ODT Strap Value MR32:OP[6] is 1, the CK ODT, CS ODT, and CA ODT values will reflect the default settings for Group B ODT values, or will reflect what has been written to these mode registers via the MPC opcodes for Set B CK/CS/CA ODT settings.

CA/CS/CK ODT Settings

The following MPC opcodes will be used to set the “Group A” and “Group B” RTT_CA, RTT_CS, and RTT_CK values.

Table 284: ODT MPC Op-Codes (For Reference Only)

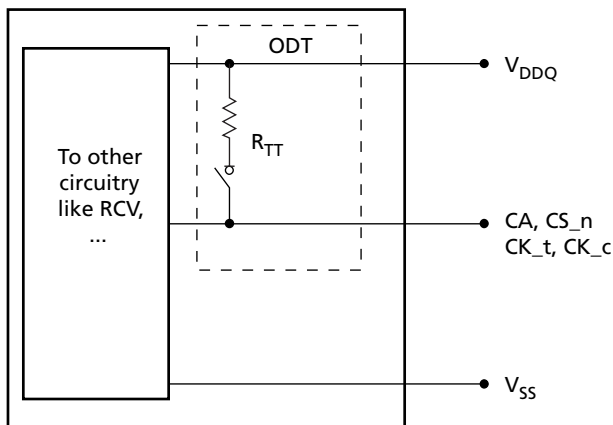
Function	Operand	Data
Initialization and training modes	OP[7:0]	0010 0xxxb: Group A RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0010 1xxxb: Group B RTT_CK = xxx (See MR32:OP[2:0] for encoding) 0011 0xxxb: Group A RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0011 1xxxb: Group B RTT_CS = xxx (See MR32:OP[5:3] for encoding) 0100 0xxxb: Group A RTT_CA = xxx (See MR33:OP[2:0] for encoding) 0100 1xxxb: Group B RTT_CA = xxx (See MR33:OP[2:0] for encoding)

On-Die Termination for CA, CS, CK_t, CK_c

The device includes CA ODT (On-Die Termination) termination resistance for CK_t, CK_c, CS_n and CA signals.

The ODT features are designed to improve signal integrity of the CS, CA, CK_t, and CK_c memory channels by allowing the device controller to turn on and off termination resistance for any target channel on each device via MR settings.

Figure 218: Simple Functional Representation of the CA, CS, CK_t, CK_c ODT Feature



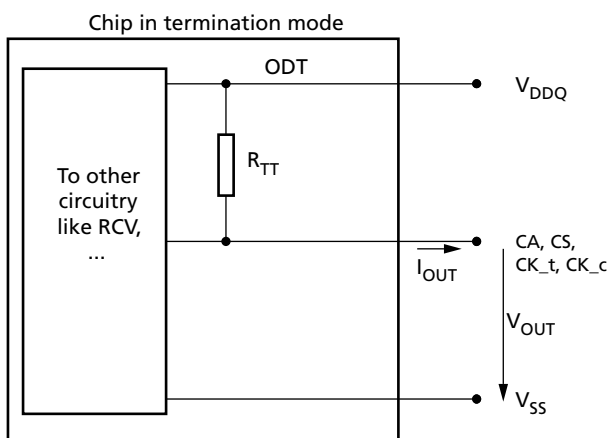
The ODT termination resistance during power up is set to the default values based on MR32 and MR33. The ODT resistance values can be configured using these same registers.

CA On-Die Termination effective resistance R_{TT} is defined by MR bits.

ODT is applied to CK_t, CK_c, CS_n and CA pins. A functional representation is shown below.

$$R_{TT} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

Figure 219: Functional Representation of ODT



Supported On-Die Termination Values

On-die termination effective R_{TT} values supported are 480, 240, 120, 80, 60, 40 ohms.

**Table 285: ODT Electrical Characteristics RZQ = 240Ω ±1% Entire Temperature Operation Range;
After Proper ZQ Calibration; V_{DD} = V_{DDQ}**

MR	R _{TT} (Ohms)	V _{OUT}	Min	Nom	Max	Unit	Notes
MR32 for CK and CSMR33 for CA	480	V _{OL,DC} = 0.5*V _{DDQ}	0.7	1	1.4	R _{ZQ} /2	1,2,4
		V _{OM,DC} = 0.8*V _{DDQ}	0.7	1	1.3	R _{ZQ} /2	1,2,4
		V _{OH,DC} = 0.5*V _{DDQ}	0.6	1	1.3	R _{ZQ} /2	1,2,4
MR32 for CK and CSMR33 for CA	240	V _{OL,DC} = 0.5*V _{DDQ}	0.9	1	1.25	R _{ZQ}	1,2,4
		V _{OM,DC} = 0.8*V _{DDQ}	0.9	1	1.1	R _{ZQ}	1,2,4
		V _{OH,DC} = 0.95*V _{DDQ}	0.8	1	1.1	R _{ZQ}	1,2,4
MR32 for CK and CSMR33 for CA	120	V _{OL,DC} = 0.5*V _{DDQ}	0.9	–	1.25	R _{ZQ} /2	1,2,3,5
		V _{OM,DC} = 0.8*V _{DDQ}	0.9	1	1.1	R _{ZQ} /2	1,2,4,5
		V _{OH,DC} = 0.95*V _{DDQ}	0.8	1	1.1	R _{ZQ} /2	1,2,4,5
MR32 for CK and CSMR33 for CA	80	V _{OL,DC} = 0.5*V _{DDQ}	0.9	1	1.25	R _{ZQ} /3	1,2,4
		V _{OM,DC} = 0.8*V _{DDQ}	0.9	1	1.1	R _{ZQ} /3	1,2,4
		V _{OH,DC} = 0.95*V _{DDQ}	0.8	1	1.1	R _{ZQ} /3	1,2,4
MR32 for CK and CSMR33 for CA	60	V _{OL,DC} = 0.5*V _{DDQ}	0.9	1	1.25	R _{ZQ} /4	1,2,4
		V _{OM,DC} = 0.8*V _{DDQ}	0.9	1	1.1	R _{ZQ} /4	1,2,4
		V _{OH,DC} = 0.95*V _{DDQ}	0.8	1	1.1	R _{ZQ} /4	1,2,4
MR32 for CK and CSMR33 for CA	40	V _{OL,DC} = 0.5*V _{DDQ}	0.9	1	1.25	R _{ZQ} /6	1,2,4
		V _{OM,DC} = 0.8*V _{DDQ}	0.9	1	1.1	R _{ZQ} /6	1,2,4
		V _{OH,DC} = 0.95*V _{DDQ}	0.8	1	1.1	R _{ZQ} /6	1,2,4
Mismatch CA to CA within device		0.8*V _{DDQ}	0	-	10	%	1,2,3,4

- Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the ZQ Calibration Commands section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above; for example, calibration at 0.5*V_{DDQ} and 0.95*V_{DDQ}.
3. CA to CA mismatch within device variation for a given component including CS, CK_t and CK_c (characterized).

$$\text{LBDQS - LBDQ mismatch in a device} = \frac{R_{TT\_MAX} - R_{TT\_MIN}}{R_{TT\_NOM}} \times 100$$

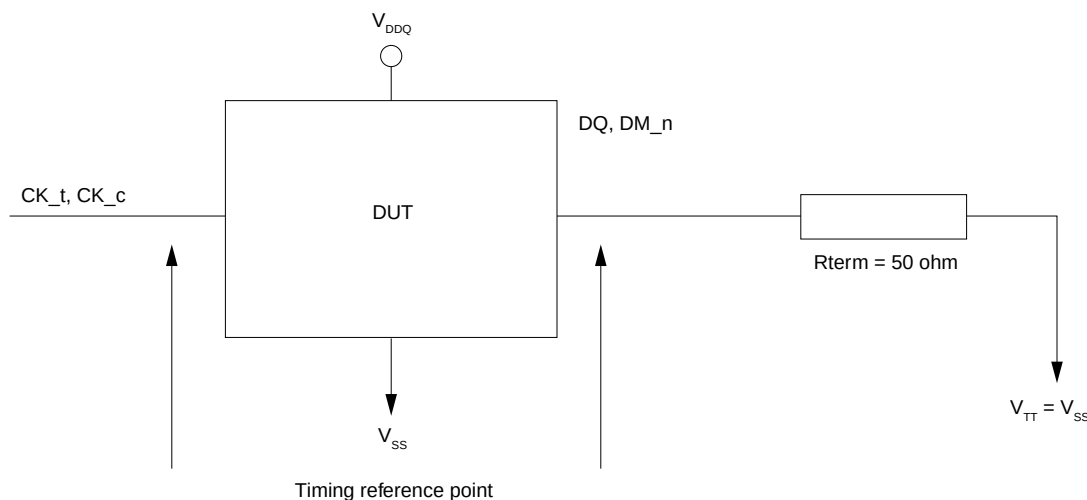
4. Without ZW calibration, ODT effective RTT values have an increased tolerance of ±30%.
5. CK ODT RZQ/2 (120Ω), CS ODT RZQ/2 (120Ω), and CA ODT RZQ/2 (120Ω) are only supported at >5200 MT/s data rates.

ODT Timing Definitions

Test Load for ODT Timings

The reference load for ODT timings is defined in the following figure.

Figure 220: ODT Timing Reference Load



^tADC Measurement Method

Table 286: ^tADC Measurement Timing Definitions

Measured Parameter	Begin Point Definition	End Point Definition	Figure
^t ADC for Target DRAM Write	End of ^t ODTLoff_WR at CK_t/CK_c differential crossing point	Extrapolated point at VRTT_WR	Figure 221: ^t ADC Measurement Method Target DRAM Write on page 355
	End of ^t ODTLon_WR at CK_t/CK_c differential crossing point	Extrapolated point at VSS	Figure 222: ^t ADC Measurement Method Non-Target DRAM Write on page 356
^t ADC for Non Target DRAM Write	End of ^t ODTLoff_WR_NT at CK_t/CK_c differential crossing point	Extrapolated point at VRTT_NOM_WR	
	End of ^t ODTLon_WR_NT at CK_t/CK_c differential crossing point	Extrapolated point at VSS	Figure 223: ^t ADC Measurement Method Non-Target DRAM Read on page 357
^t ADC for Non Target DRAM Read	End of ^t ODTLoff_RD_NT at CK_t/CK_c differential crossing point	Extrapolated point at VRTT_NOM_RD	
	End of ^t ODTLon_RD_NT at CK_t/CK_c differential crossing point	Extrapolated point at VSS	

Table 287: Reference Setting for ODT Timing Measurement

Measured Parameter	RTT_PARK	RTT_WR	RTT_NOM_WR	RTT_NOM_RD	Vsw1	Vsw2	Figure	Notes
^t ADC for Target DRAM Write	RTT_OFF	RZQ/7	-	-	0.20V	0.40V	Figure 221: ^t ADC Measurement Method Target DRAM Write on page 355	1,4
^t ADC for Non Target DRAM Write	RTT_OFF	-	RZQ/7	-	0.20V	0.40V	Figure 222: ^t ADC Measurement Method Non-Target DRAM Write on page 356	2,4
^t ADC for Non Target DRAM Read	RTT_OFF	-	-	RZQ/7	0.20V	0.40V	Figure 223: ^t ADC Measurement Method Non-Target DRAM Read on page 357	3,4

Notes: 1. MR34 OP[2:0]=000B (RTT_PARK setting); MR34 OP[5:3]=111B (RTT_WR setting)
2. MR34 OP[2:0]=000B (RTT_PARK setting); MR35 OP[2:0]=111B (RTT_NOM_WR setting)
3. MR34 OP[2:0]=000B (RTT_PARK setting); MR35 OP[5:3]=111B (RTT_NOM_RD setting)
4. ^tADC measurement method applies to DQs/DM only. It does not apply to DQS_t, DQS_c, TDQS_t and TDQS_c since there is no transition from DQS_{RTT_PARK}.

Figure 221: t_{ADC} Measurement Method Target DRAM Write

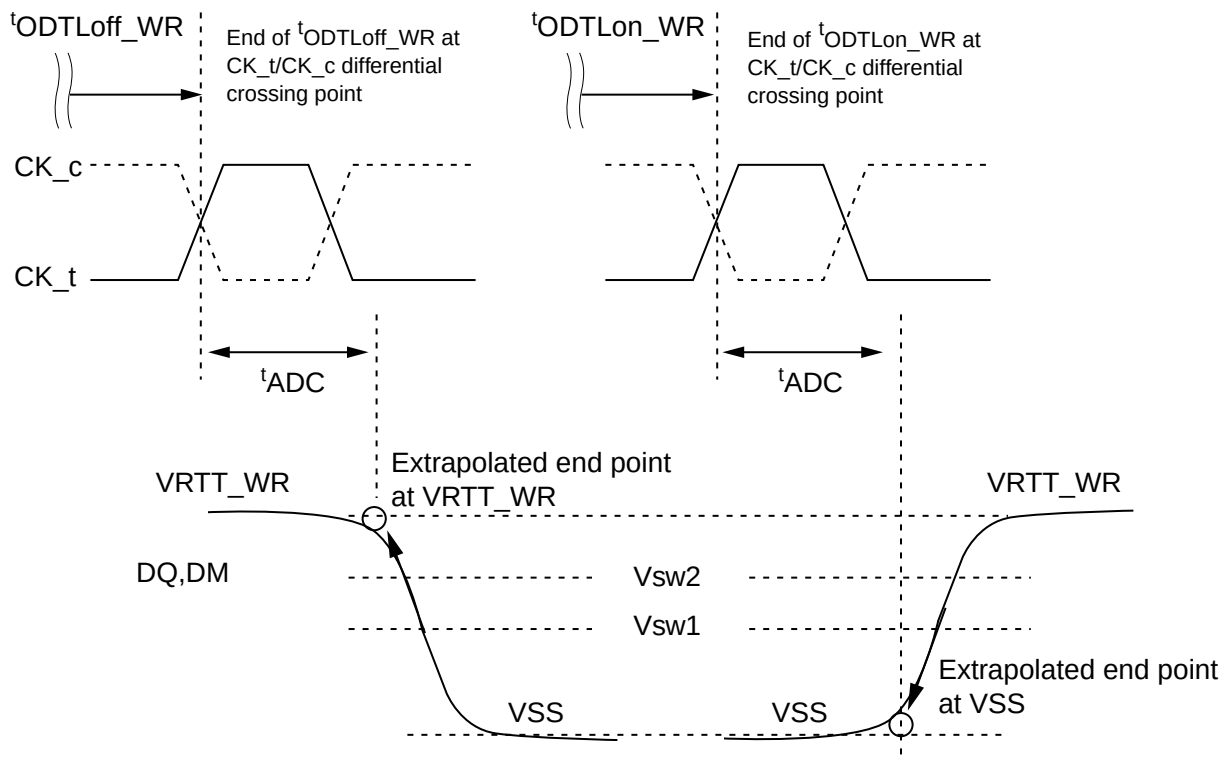


Figure 222: t_{ADC} Measurement Method Non-Target DRAM Write

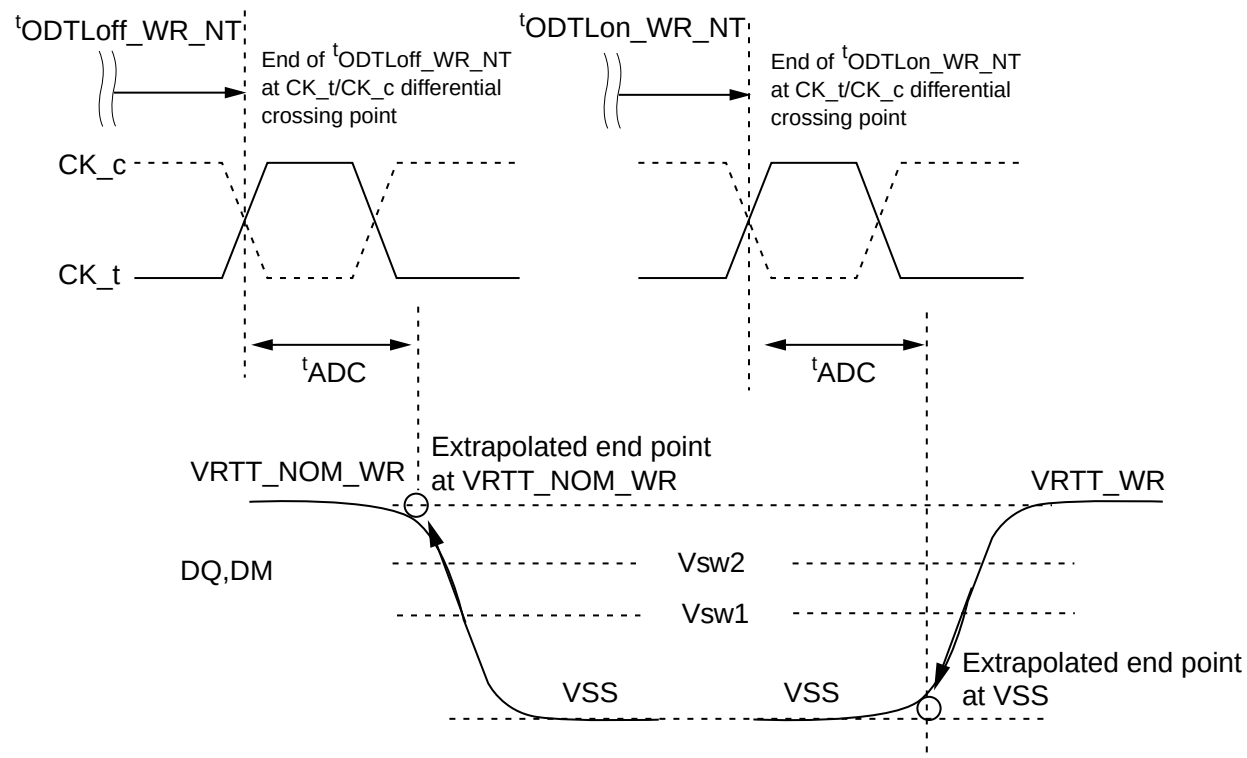
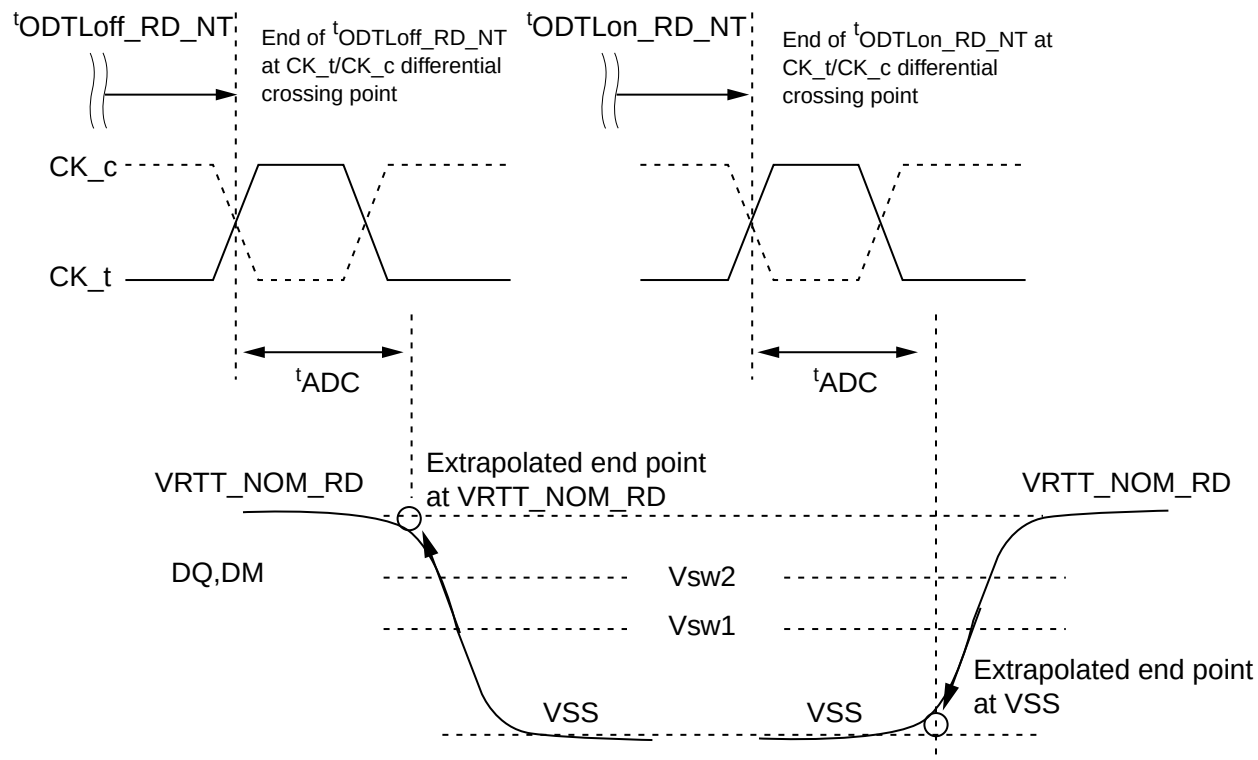


Figure 223: t_{ADC} Measurement Method Non-Target DRAM Read



AC and DC Operating Conditions

Absolute Maximum Ratings

Table 288: Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.3 ~ 1.4	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.3 ~ 1.4	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.3 ~ 2.1	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3 ~ 1.4	V	1
T_{STG}	Storage temperature	-55 to +100	°C	1, 2

- Notes: 1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

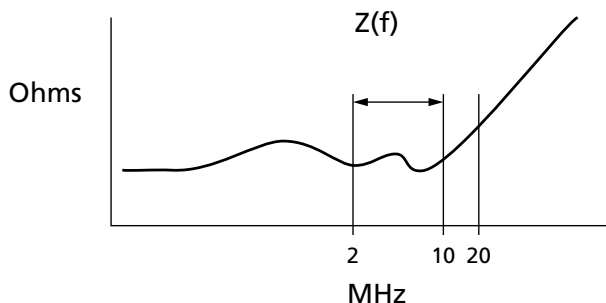
DC Voltage Operating Conditions

Table 289: DC Voltage Operating Conditions

Symbol	Parameter	Low Frequency Voltage Spec				Z(f) Spec Freq: 2-10 MHz		Z(f) Spec Freq: 20 MHz		Notes
		Min	Typ	Max	Unit	Zmax	Unit	Zmax	Unit	
V_{DD}	Supply voltage	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhms	20	mOhms	1, 2, 3, 4
V_{DDQ}	Supply voltage for I/O	1.067 (-3%)	1.1	1.166 (+6%)	V	10	mOhms	20	mOhms	1, 2, 3, 4
V_{PP}	Pump voltage	1.746 (-3%)	1.8	1.908 (+6%)	V	10	mOhms	20	mOhms	3, 4

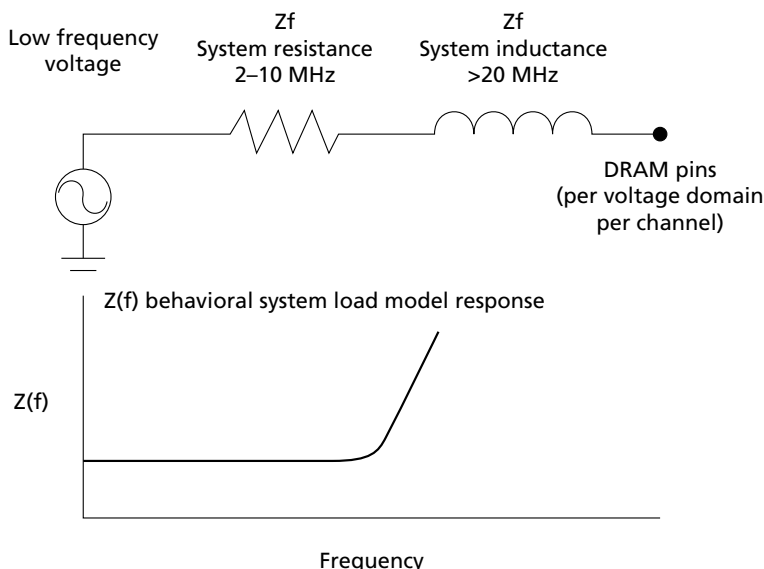
- Notes: 1. V_{DD} must be within 66mV of V_{DDQ} .
2. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.
4. Z(f) is defined for all pins per voltage domain. Z(f) does not include the DRAM package and silicon die.

Figure 224: Zprofile/Z(f) of the System at the DRAM Package Solder Ball (Without DRAM Component)



A simplified electrical system load model for Z(f) with the general frequency response is shown in the figure below. The resistance and inductance can be scaled to generalize the spec response to the DRAM pin.

Figure 225: Simplified Z(f) Electrical Model and Frequency Response of PDN at the DRAM Pin (Without DRAM Component)



Pin Leakage

The following table includes the target pin leakages.

Table 290: Pin Leakage Limits

Condition	Symbol	Temperature Range (Unit °C)		Grade	Notes
		MIN	MAX		
Input leakage (RESET_n)	I_{IN}	-2	2	uA	1
Input leakage: VIN=VDDQ (CA, CS_n, CK)	I_{IN_CApd}	-	2	uA	1
Input leakage: VIN=VSS (CA, CS_n, CK)	I_{IN_CApu}	-50	-		1,4
ZQ leakage	I_{ZQ}	-50	15	uA	1,3
TEN leakage	I_{TEN}	-6	10	uA	1,2
Input leakage (CAI, MIR, CA_ODT)	I_{STRAP}	-6	10	uA	1,2
Output leakage: VOUT=VDDQ (DQ, DQS, LBDQ, LBDQS, DM/TDQS, ALERT_n)	I_{OZpd}	-	15	uA	3,5
Output leakage: VOUT=VSS (DQ, DQS, LBDQ, LBDQS, DM/TDQS, ALERT_n)	I_{OZpu}	-50	-	uA	5,6

Notes: 1. Input under test $0V < V_{IN} < 1.1V$.

2. Additional leakage due to weak pull-down.

3. Additional leakage due to weak pull up

4. Additional leakage due to pin termination.

5. Qs are disabled via MR5:OP[0].

6. ODT is disabled with the MPC commands to set MR33:OP[3-5] DQS_RTT_PARK = 000 (RTT_OFF) and MPC command to set MR34:OP[0-3] RTT_PARK = 000 (RTT_OFF).

Device Component Operating Temperature Range

Table 291: DC Operating Temperature Range

Symbol	Parameter	Temperature Range (Unit °C)		Grade	Notes
		MIN	MAX		
T _{OPER_NORMAL}	Normal operating temperature	0	85	NT	1,2,3,4
T _{OPER_EXTENDED}	Extended operating temperature	0	95	XT	1,2,3,4,5
T _{OPER_INDUST}	Industrial Operating Temperature	-40	95	IT	1,2,3,4,5
T _{OPER_AUTO}	Automotive Operating Temperature	-40	105	AT	1,2,3,4,5

- Notes:
1. All operating temperature symbols, ranges, acronyms from JESD402-1.
 2. Operating temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2.
 3. All devices are required to operate in NT and XT temperature ranges.
 4. When operating above 85°C, the host must provide appropriate refresh mode controls associated with the increased temperature range. The full description of these settings are defined in the ^tREFI parameters for REFab and REFsb Commands by Device Density (including 3DS) table in the Refresh Operation section.
 5. Operating temperature for 3DS devices needs to be derated by the number of device dies as: $[T_{\text{OPER}} - (2.5^{\circ}\text{C} \times \log_2 N)]$, where N is the number of the stacked dies.

Bit Error Rate

This section provides an overview of the bit error rate (BER) and the desired statistical level of confidence.

Figure 226: General Equation

$$n = \left(\frac{1}{BER} \right) \left[-\ln(1 - SLC) + \ln \left(\sum_{k=0}^N \frac{(n \times BER)^k}{k!} \right) \right]$$

Note: 1. Where:

n = number of bits in a trial

SLC = statistical level of confidence

BER = bit error rate

k = intermediate number of specific errors found in trial

N = number of errors recorded during trial

If no errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER} \right) \left[-\ln(1 - SLC) \right]$$

JEDEC recommends testing to 99.5% confidence levels; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N = 0), using BER = 1E⁻⁹ and confidence level SLC = 99.5%, the result is n = (1/BER)(-ln(1 - 0.995)) = 5.298 x 10⁹.

Table 292: Estimated Number of Transmitted Bits (n) – Confidence Level of 70–99.5%

Number of Errors	n = -ln(1 - SLC)/BER							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/BER	4.61/BER	2.99/BER	2.3/BER	1.90/BER	1.61/BER	1.39/BER	1.20/BER

Minimum BER Requirements

The following table specifies the average UI and BER requirements over which certain receiver and transmitter timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER = 1E⁻⁹.

Table 293: Minimum BER Requirements for Rx/Tx Timing and Voltage Tests (3200–8800)

Parameter	Symbol	3200–8800			Unit	Notes
		Min	Nom	Max		
Average UI	UI _{AVG}	0.999 * nom	1.000/f	1.001 * nom	ps	1
Number of UI (min)	N _{Min_UI_Validation}	5.3 x 10 ⁹	–	–	UI	2
Bit error rate	BER _{Lane}	–	–	1E ⁻¹⁶	Events	3,4,5,6

Notes: 1. Average UI size; “f” is data rate.

2. Number of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER=1E⁻⁹.

3. This is a system parameter. It is the raw BER for every lane before any logical PHY or link layer-based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver; therefore, this parameter has to be validated in selected systems using a suitable methodology as deemed by the platform.

4. This is a raw BER-per-lane before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5. This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQS & DQ Voltage Sensitivity, Rx DQS Jitter Sensitivity, Rx DQ Stressed Eye, Tx DQS Jitter, Tx DQ Jitter, and Tx DQ Stressed eye height / eye width specifications.
6. The BER for DDR5 during normal operation is $1E^{-16}$. For validation purposes, the BER used is $1E^{-9}$.

Unit Interval and Jitter Definitions

This section describes the unit interval (UI) and UI jitter definitions associated with the jitter parameters specified in the input clock jitter, Rx stressed eye, Tx DQS jitter, and Tx DQ jitter sections of this specification.

Unit Interval (UI)

The definition of unit interval (UI) is a minimum time interval between condition changes of a signal. DDR-based signals are referenced to the differential crossing point of CK_t and CK_c. $2UI = 1^tCK$ for DDR-based signals (example DQ, DQS).

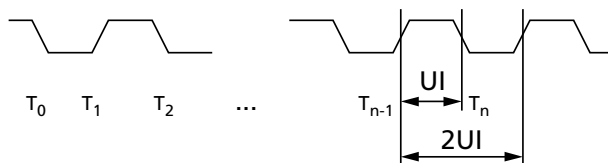
The UI definitions shown in the two following figures are for DDR-based signals.

The times at which the differential crossing points of the clock occur are defined at $t_1, t_2, \dots, t_{n-1}, t_n, \dots$. The UI at index n is defined as an arbitrary time in steady state, where $n = 0$ is chosen as the starting crossing point.

Figure 227: UI Definition in Terms of Adjacent Edge Timings

$$UI_n = t_n - t_{n-1}$$

Figure 228: UI Definition Using Clock Waveforms



UI Jitter Definition

If a number of UI edges are computed or measured at times $t_1, t_2, \dots, t_{n-1}, t_n, \dots, t_K$, where K is the maximum number of samples, then the UI jitter at any instance n is defined below, where T = the ideal UI size.

Figure 229: UI Jitter for “nth” UI Definition (in Terms of Ideal UI)

$$UI(jit)_n = (t_n - t_{n-1}) - T, n = 1, 2, 3, \dots, K$$

In a large sample with random Gaussian-like jitter (very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described above assumes starting from an instant steady state, where $n = 0$ is chosen as the starting point.

1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe. Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (BER) for the link.

UI-UI Jitter Definition

UI-UI (read as “UI to UI”) jitter is defined to be the jitter between two consecutive UI, as shown below.

$$\Delta UI_n = UI_n - UI_{n-1}, n = 2, 3, \dots, K$$

Accumulated Jitter (Over n UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive “n” UI, as shown below.

$$T_{acc} = \sum_{p=m}^{m+N-1} (UI_p - \bar{UI}) \quad m = 1, 2, 3, \dots, K-N$$

Definition of UI

$$\bar{UI} = \frac{\sum_{p=1}^K UI_p}{K} \quad p = 1, 2, 3, \dots, N, \dots, K$$

Differential Input Cross Point Voltage (V_{IX})

Differential Strobe (DQS_t, DQS_c) Input Cross Point Voltage (V_{IX_DQS})

Figure 230: V_{IX_DQS} Definition

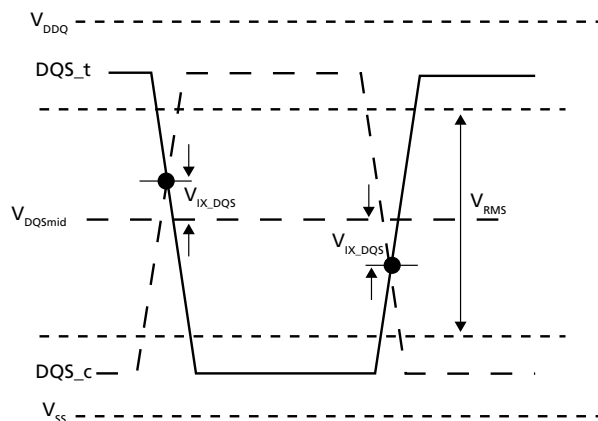


Table 294: Cross Point Voltage for DQS Differential Input Signals (V_{IX_DQS}) — 3200-8800

Parameter	Symbol	3200-8800		Unit	Notes
DQS differential input cross point voltage ratio	$V_{IX\_DQS\_Ratio}$	-	50	%	1,2,3

Notes: 1. The V_{IX_DQS} voltage is referenced to $V_{DQSmid}(\text{mean}) = (\text{DQS\_t voltage} + \text{DQS\_c voltage}) / 2$, where the mean is over 8 UI.

2. $V_{IX\_DQS\_Ratio} = (|V_{IX\_DQS}| / V_{RMS}) * 100\%$, where $V_{RMS} = |\text{RMS}(\text{DQS\_t voltage} - \text{DQS\_c voltage})|$.

3. Only applies when both DQS_t and DQS_c are transitioning (including preamble).

Differential Input Clock (CK_t, CK_c) Cross Point Voltage (V_{IX_CK})

Figure 231: V_{IX_CK} Definition

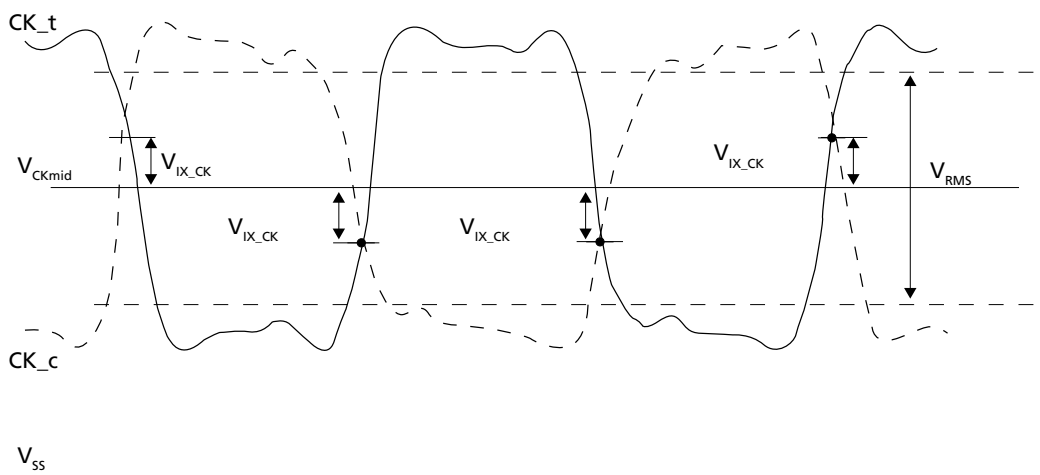


Table 295: Cross Point Voltage for Differential Input Clock (V_{IX_CK}) — 3200-8800

Parameter	Symbol	3200-8800		Unit	Notes
		Min	Max		
CK differential input cross point voltage ratio	$V_{IX\_CK\_Ratio}$	-	50	%	1,2,3

- Notes: 1. The V_{IX_CK} voltage is referenced to $V_{CKmid(mean)} = (CK\_t \text{ voltage} + CK\_c \text{ voltage}) / 2$, where the mean is over 8 UI.
2. $V_{IX\_CK\_Ratio} = (|V_{IX\_CK}| / V_{RMS}) * 100\%$, where $V_{RMS} = \text{RMS} (|CK\_t \text{ voltage} - CK\_c \text{ voltage}|)$.
3. Only applies when both CK_t and CK_c are transitioning.

AC and DC Input Measurement Levels

CA Rx Voltage and Timings

The command, address and control (including chip select) input receiver compliance mask for voltage and timing is shown in the figure below. All CA signals apply the same compliance mask and the CS signal applies its own compliance mask independently. All signals applied to the compliance mask operate in single data rate mode.

The CA input receiver mask (Rx Mask) for voltage and timing is applied across all CA[13:0] pins and the CS_n pin. For the remainder of this section, the reference to "CA" should be applied to the device CA[13:0] pins as well as the CS_n pin. The Rx Mask defines the area the input signal must not encroach for the device input receiver to successfully capture a valid input signal; it is not the valid data-eye.

Figure 232: CA/CS_n Rx Mask

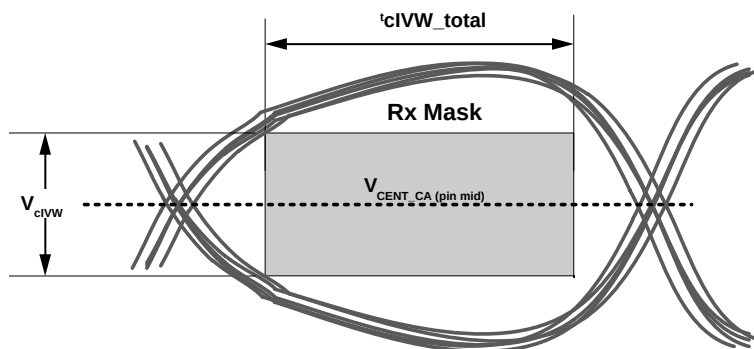
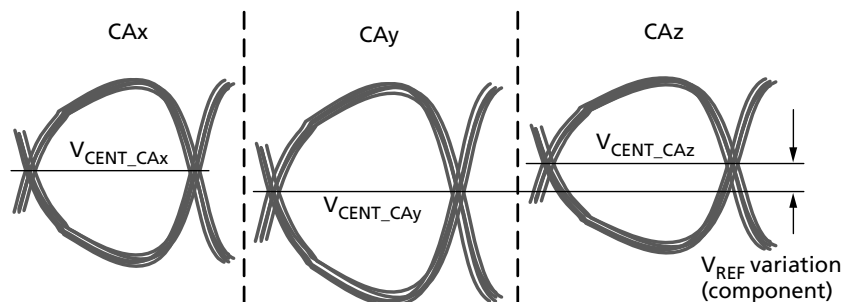


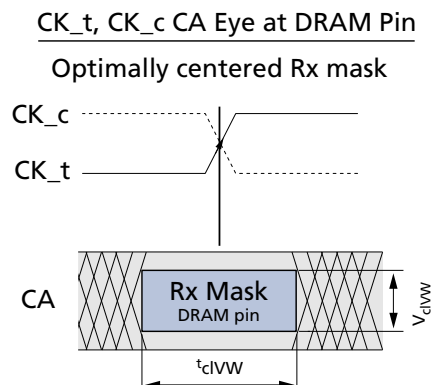
Figure 233: Across-Pin V_{REFCA} Voltage Variation



$V_{cent\_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{cent_CA} voltage level and the smallest V_{cent_CA} voltage level across all CA and CS_n pins for a given device component.

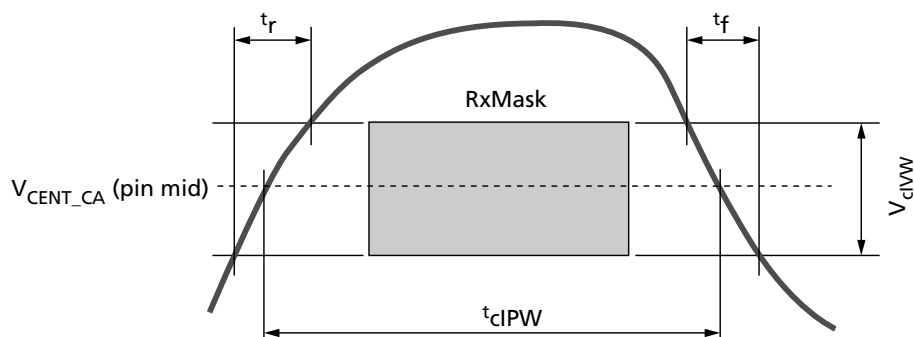
Each CA V_{cent} level is defined by the center (widest opening) of the cumulative data input eye as depicted in the previous figure (Across-Pin V_{REFCA} Voltage Variation). This clarifies any device component level variation must be accounted for within the CA Rx Mask. The component-level V_{REF} is set by the system to account for R_{ON} and ODT settings.

Figure 234: CA/CS_n Timings at the Device Pins



t_{cIVW} is not necessarily center-aligned on CK_t/CK_c crossing at the DRAM pin, but is assumed to be center-aligned at the DRAM latch.

Figure 235: CA T_{cIPW} and S_{RIN_cIVW} Definition (For Each Input Pulse)



Note: 1. $S_{RIN\_cIVW} = V_{cIVW\_Total} / (t_r \text{ or } t_f)$, signal must be monotonic within t_r and t_f range.

Figure 236: CA V_{IHL_AC} Definition (For Each Input Pulse)

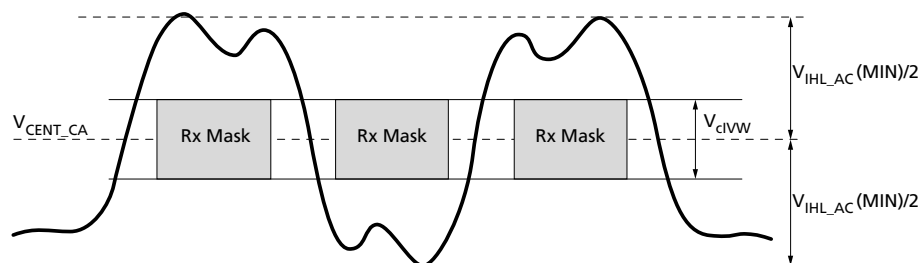


Table 296: DDR5 3200-4800 Command/Address, CS Parametric Values

Symbol	Parameter	3200		3600		4000		4400		4800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V_{cIVW}	Rx Mask voltage - p-p	140	-	140	-	140	-	130	-	130	-	mV	1,2,4
t_{cIVW}	Rx timing window	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	t_{CK}	1,2,3,4
V_{IHL_AC}	CA input pulse amplitude	160		160		160		150		150		mV	7

Table 296: DDR5 3200-4800 Command/Address, CS Parametric Values (Continued)

Symbol	Parameter	3200		3600		4000		4400		4800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{clPW}	CA input pulse width	0.58		0.58		0.58		0.58		0.58		t_{CK}	5
S_{RIN_clVW}	Input slew rate over V_{clVW}	1	7	1	7	1	7	1	7	1	7	V/ns	6

- Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx Mask voltage $V_{clVW\ total(MIN)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{clVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.

Table 297: DDR5 5200-6400 Command/Address, CS Parametric Values

Symbol	Parameter	x4 and x8 Devices				x16 Devices				Unit	Notes
		5200-5600		6000-6400		5200-5600		6000-6400			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V _{clVW}	Rx Mask voltage - p-p	100	-	85	-	110	-	95	-	mV	1,2,4
t _{clVW}	Rx timing window	0.2	-	0.2	-	0.2	-	0.2	-	t _{CK}	1,2,3,4
V _{IHL_} AC	CA input pulse amplitude	115		105		125	-	115	-	mV	7
t _{clPW}	CA input pulse width	0.58		0.58		0.58		0.58		t _{CK}	5
S _{RIN_} clV W	Input slew rate over V _{clVW}	1	7	1	7	1	7	1	7	V/ns	6

- Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx Mask voltage $V_{clVW\ total(MIN)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{clVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.

Table 298: DDR5 6800-8000 Command/Address, CS Parametric Values

Symbol	Parameter	x4 and x8 Devices				x16 Devices				Unit	Notes
		6800-7200		7600-8000		6800-7200		7600-8000			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
V _{clVW}	Rx Mask voltage - p-p	80	-	75	-	90	-	85	-	mV	1,2,4
t _{clVW}	Rx timing window	0.2	-	0.2	-	0.2	-	0.2	-	t _{CK}	1,2,3,4
V _{IHL_} AC	CA input pulse amplitude	100		95		110	-	105	-	mV	7
t _{clPW}	CA input pulse width	0.58		0.58		0.58		0.58		t _{CK}	5
S _{RIN_} clV W	Input slew rate over V _{clVW}	1	7	1	7	1	7	1	7	V/ns	6

- Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
 2. Rx Mask voltage $V_{\text{clVW total(MIN)}}$ must be centered around $V_{\text{cent\_CA(pin mid)}}$.
 3. Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.
 4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
 5. CA only minimum input pulse width defined at the $V_{\text{cent\_CA(pin mid)}}$.
 6. Input slew rate over $V_{\text{clVW Mask}}$ centered at $V_{\text{cent\_CA(pin mid)}}$.
 7. $V_{\text{IHL\_AC}}$ does not have to be met when no transitions are occurring.

Table 299: DDR5 8400-8800 Command/Address, CS Parametric Values

Symbol	Parameter	x4 and x8 Devices		x16 Devices		Unit	Notes
		8400-8800		8400-8800			
		MIN	MAX	MIN	MAX		
V _{clVW}	Rx Mask voltage - p-p	70	-	80	-	mV	1,2,4
t _{clVW}	Rx timing window	0.2	-	0.2	-	t _{CK}	1,2,3,4
V _{IHL_} AC	CA input pulse amplitude	90	-	100	-	mV	7
t _{cIPW}	CA input pulse width	0.58		0.58	0.58	t _{CK}	5
S _{RIN_} clV W	Input slew rate over V _{clVW}	1	7	1	7	V/ns	6

- Notes: 1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
 2. Rx Mask voltage $V_{\text{clVW total(MIN)}}$ must be centered around $V_{\text{cent\_CA(pin mid)}}$.
 3. Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.
 4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
 5. CA only minimum input pulse width defined at the $V_{\text{cent\_CA(pin mid)}}$.
 6. Input slew rate over $V_{\text{clVW Mask}}$ centered at $V_{\text{cent\_CA(pin mid)}}$.
 7. $V_{\text{IHL\_AC}}$ does not have to be met when no transitions are occurring.

Differential Input Voltage Levels for Clock

Table 300: Differential Clock (CK_t, CK_c) Input Levels for DDR5 3200-8800

Symbol	Parameter	3200-8800	Note
$V_{IH,diffCK}$	Differential input high measurement level	$0.75 \times V_{diff,pk-pk}$	1,2
$V_{IL,diffCK}$	Differential input low measurement level	$0.25 \times V_{diff,pk-pk}$	1,2

Notes: 1. $V_{diff,pk-pk}$ defined in the Differential Input Slew Rate Definition for CK_t, CK_c figure (next section).
 2. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples.
 3. All parameters are defined over the entire clock common mode range.

Differential Input Slew Rate Definition for Clock

Figure 237: Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

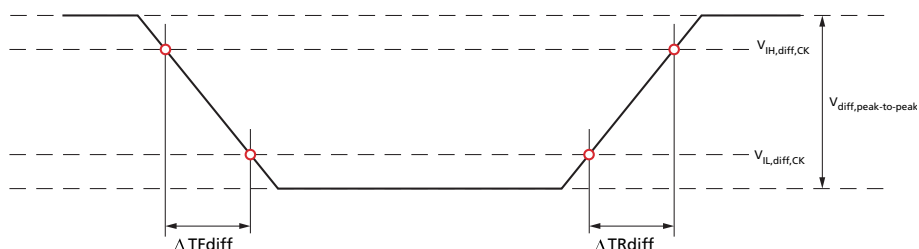


Table 301: Differential Input Slew Rate Definition for Clock (CK_t, CK_c)

Parameter	Measured		Defined By
	From	To	
Differential input slew rate for rising edge (CK _t - CK _c)	$V_{IL,diffCK}$	$V_{IH,diffCK}$	$ V_{IL,diffCK} - V_{IH,diffCK} / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK _t - CK _c)	$V_{IH,diffCK}$	$V_{IL,diffCK}$	$(V_{IH,diffCK} - V_{IL,diffCK}) / \Delta TF_{diff}$

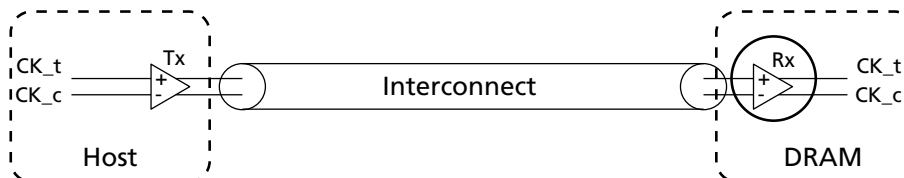
Table 302: Differential Input Slew Rate for Clock (CK_t, CK_c) — 3200-8000

Parameter	Symbol	3200-4800		5200-8800		Unit
		MIN	MAX	MIN	MAX	
Differential input slew rate for CK _t - CK _c	S_{Rdiff_CK}	2	14	2	30	V/ns

Input Clock Jitter Specification

The clock is being driven to the device either by the RCD for L/RDIMM modules, or by the host for U/SODIMM modules.

Figure 238: HOST Driving Clock Signals to the device



Specifications for Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the device.

Note: For the following tables: BUJ = Bounded Uncorrelated Jitter; DCD = Duty Cycle Distortion; Dj = Deterministic Jitter; Rj = Random Jitter; Tj = Total jitter; pp = Peak-to-Peak

Table 303: Input Clock Jitter Specifications for 3200 to 4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Reference clock frequency	t_{CK}	$0.9999 * f_0$	$1.0001 * f_0$	$0.9999 * f_0$	$1.0001 * f_0$	$0.9999 * f_0$	$1.0001 * f_0$	$0.9999 * f_0$	$1.0001 * f_0$	$0.9999 * f_0$	$1.0001 * f_0$	MHz	1,11
Duty Cycle Error	$t_{CK\_Duty\_UI\_Error\_Error}$	-	0.05	-	0.05	-	0.05	-	0.05	-	0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	$t_{CK\_1UI\_Rj\_Error}$	-	0.0037	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	$t_{CK\_1UI\_Dj\_N\_oBUJ}$	-	0.03	-	0.03	-	0.03	-	0.030	-	0.030	UI	3,6,11
Tj value of 1- UI Jitter	$t_{CK\_1UI\_Tj\_N\_oBUJ}$	-	0.09	-	0.09	-	0.09	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N = 2,3	$t_{CK\_NUI\_Rj\_N\_oBUJ, where N = 2,3}$	-	0.0040	-	0.0040	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N = 2,3	$t_{CK\_NUI\_Dj\_N\_oBUJ, where N = 2,3}$	-	0.074	-	0.074	-	0.074	-	0.074	-	0.074	UI	3,7,11
Tj value of N- UI Jitter, where N = 2,3	$t_{CK\_NUI\_Tj\_N\_oBUJ, where N = 2,3}$	-	0.140	-	0.140	-	0.140	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N = 4,5,6,...,30	$t_{CK\_NUI\_Rj\_N\_oBUJ, where N = 4,5,6,...,30}$	-	-	-	-	-	-	-	-	-	-	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N = 4,5,6,...,30	$t_{CK\_NUI\_Dj\_N\_oBUJ, where N = 4,5,6,...,30}$	-	-	-	-	-	-	-	-	-	-	UI	3,10,11,12
Tj value of N- UI Jitter, N = 4,5,6,...,30	$t_{CK\_NUI\_Tj\_N\_oBUJ, where N = 4,5,6,...,30}$	-	-	-	-	-	-	-	-	-	-	UI	3,10,11,12

Notes: 1. f_0 = Data Rate/2, example: if data rate is 3200MT/s, then f_0 = 1600

2. Rise and fall time slopes (V/ns) are measured between +100 mV and -100 mV of the differential output of reference clock

3. On-die noise is similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being a device component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $1 < N < 4$. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $1 < N < 4$. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $3 < N < 31$. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $3 < N < 31$. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as $Dj + 16.2 \cdot Rj$ for BER of $1E^{-16}$

Table 304: Input Clock Jitter Specifications for 5200 to 6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Reference clock frequency	t_{CK}	$0.9999 \cdot f_0$	$1.0001 \cdot f_0$	$0.9999 \cdot f_0$	$1.0001 \cdot f_0$	$0.9999 \cdot f_0$	$1.0001 \cdot f_0$	$0.9999 \cdot f_0$	$1.0001 \cdot f_0$	MHz	1,11
Duty Cycle Error	$t_{CK\_Duty\_UI\_Error}$	-	0.05	-	0.05	-	0.05	-	0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	$t_{CK\_1UI\_Rj\_NoBUJ}$	-	0.0037	-	0.0037	-	0.0037	-	0.0037	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	$t_{CK\_1UI\_Dj\_NoBUJ}$	-	0.030	-	0.030	-	0.030	-	0.030	UI	3,6,11
Tj value of 1- UI Jitter	$t_{CK\_1UI\_Tj\_NoBUJ}$	-	0.090	-	0.090	-	0.090	-	0.090	UI	3,6,11
Rj RMS value of N-UI Jitter, where N = 2,3,4,5	$t_{CK\_NUI\_Rj\_NoBUJ,w}$ here N = 2,3,4,5	-	0.0040	-	0.0040	-	0.0040	-	0.0040	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N = 2,3,4,5	$t_{CK\_NUI\_Dj\_NoBUJ,w}$ here N = 2,3,4,5	-	0.074	-	0.074	-	0.074	-	0.074	UI	3,7,11
Tj value of N- UI Jitter, where N = 2,3,4,5	$t_{CK\_NUI\_Tj\_NoBUJ,w}$ here N = 2,3,4,5	-	0.140	-	0.140	-	0.140	-	0.140	UI	3,8,11
Rj RMS value of N-UI Jitter, where N = 6,...,30	$t_{CK\_NUI\_Rj\_NoBUJ,w}$ here N = 6,...,30	-	-	-	-	-	-	-	-	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N = 6,...,30	$t_{CK\_NUI\_Dj\_NoBUJ,w}$ here N = 6,...,30	-	-	-	-	-	-	-	-	UI	3,10,11,12
Tj value of N- UI Jitter, N = 6,...,30	$t_{CK\_NUI\_Tj\_NoBUJ,w}$ here N = 6,...,30	-	-	-	-	-	-	-	-	UI	3,10,11,12

Notes: 1. f_0 = Data Rate/2, example: if data rate is 3200MT/s, then f_0 = 1600

2. Rise and fall time slopes (V/ns) are measured between +100 mV and -100 mV of the differential output of reference clock
3. On-die noise is similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being a device component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.
4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $1 < N < 6$. This extraction is to be done after software correction of DCD
8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $1 < N < 6$. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $5 < N < 31$. This extraction is to be done after software correction of DCD
10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $5 < N < 31$. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
11. The validation methodology for these parameters will be covered in future ballots
12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as $Dj + 16.2 \cdot Rj$ for BER of $1E^{-16}$

Table 305: Input Clock Jitter Specifications for 6800 to 8800

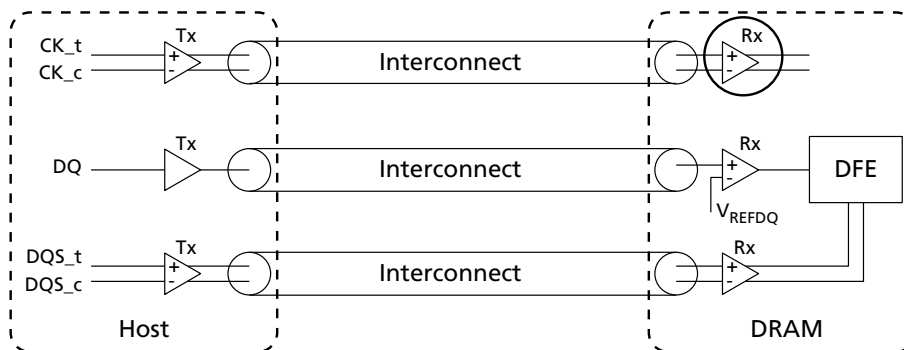
Parameter	Symbol	6800, 8000		7200, 8400		7600, 8800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Reference clock frequency	t_{CK}	$0.9999 \cdot f_0$	$1.0001 \cdot f_0$	$0.9999 \cdot f_0$	$1.0001 \cdot f_0$	$0.9999 \cdot f_0$	$1.0001 \cdot f_0$	MHz	1,11
Duty Cycle Error	$t_{CK\_Duty\_UI\_Error\_Err}$ or	-	0.05	-	0.05	-	0.05	UI	1,4,11
Rj RMS value of 1-UI Jitter	$t_{CK\_1UI\_Rj\_NoBUJ}$	-	0.003145	-	0.003145	-	0.003145	UI (RMS)	3,5,11
Dj pp value of 1-UI Jitter	$t_{CK\_1UI\_Dj\_NoBUJ}$	-	0.0255	-	0.0255	-	0.0255	UI	3,6,11
Tj value of 1- UI Jitter	$t_{CK\_1UI\_Tj\_NoBUJ}$	-	0.0765	-	0.0765	-	0.0765	UI	3,6,11
Rj RMS value of N-UI Jitter, where N = 2,3,4,5	$t_{CK\_NUI\_Rj\_NoBUJ,wh}$ ere N = 2,3,4,5	-	0.0034	-	0.0034	-	0.0034	UI (RMS)	3,7,11
Dj pp value of N-UI Jitter, where N = 2,3,4,5	$t_{CK\_NUI\_Dj\_NoBUJ,wh}$ ere N = 2,3,4,5	-	0.0629	-	0.0629	-	0.0629	UI	3,7,11
Tj value of N- UI Jitter, where N = 2,3,4,5	$t_{CK\_NUI\_Tj\_NoBUJ,wh}$ ere N = 2,3,4,5	-	0.119	-	0.119	-	0.119	UI	3,8,11
Rj RMS value of N-UI Jitter, where N = 6,...,30	$t_{CK\_NUI\_Rj\_NoBUJ,wh}$ ere N = 6,...,30	-	-	-	-	-	-	UI (RMS)	3,9,11,12
Dj pp value of N-UI Jitter, N = 6,...,30	$t_{CK\_NUI\_Dj\_NoBUJ,wh}$ ere N = 6,...,30	-	-	-	-	-	-	UI	3,10,11,12
Tj value of N- UI Jitter, N = 6,...,30	$t_{CK\_NUI\_Tj\_NoBUJ,wh}$ ere N = 6,...,30	-	-	-	-	-	-	UI	3,10,11,12

- Notes: 1. $f_0 = \text{Data Rate}/2$, example: if data rate is 3200MT/s, then $f_0 = 1600$
2. Rise and fall time slopes (V/ns) are measured between +100 mV and -100 mV of the differential output of reference clock
 3. On-die noise is similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being a device component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specifications is met and another violated in which case the signaling analysis should be run to determine link feasibility.
 4. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
 5. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
 6. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
 7. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $1 < N < 6$. This extraction is to be done after software correction of DCD
 8. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $1 < N < 6$. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
 9. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $5 < N < 31$. This extraction is to be done after software correction of DCD
 10. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for $5 < N < 31$. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD
 11. The validation methodology for these parameters will be covered in future ballots
 12. If the clock meets total jitter Tj at BER of $1E^{-16}$, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as $Dj + 16.2 \cdot Rj$ for BER of $1E^{-16}$

Differential Input Clock Voltage Sensitivity

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock varying input voltage in the absence of inter-symbol interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise. This specifies the clock input voltage sensitivity requirement.

Figure 239: Device Memory Interconnect Example



Differential Input Clock Voltage Sensitivity Parameter

Differential input clock (CK_t, CK_c) VRx_CK is defined and measured as shown below. The clock receiver must pass the minimum BER requirements for DDR5.

Table 306: Differential Input Clock Voltage Sensitivity Parameter for 3200 to 4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential)	VRx_CK	-	200	-	200	-	180	-	180	-	160	mV	1

Note: 1. The validation methodology for this parameter is TBD.

Table 307: Differential Input Clock Voltage Sensitivity Parameter for 5200 to 6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential) with no CK buffer	VRx_CK (no CKD)	-	140	-	120	-	100		100	mV	1
Minimum input clock voltage sensitivity (differential) with CK buffer	VRx_CK (with CKD)	-	140	-	120	-	120	-	120	mV	1

Note: 1. The validation methodology for this parameter is TBD.

Table 308: Differential Input Clock Voltage Sensitivity Parameter for 6800 to 7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential) with no CK buffer	VRx_CK (no CKD)	-	100	-	100	-	100	mV	1
Minimum input clock voltage sensitivity (differential) with CK buffer	VRx_CK (with CKD)	-	120	-	120	-	120	mV	1

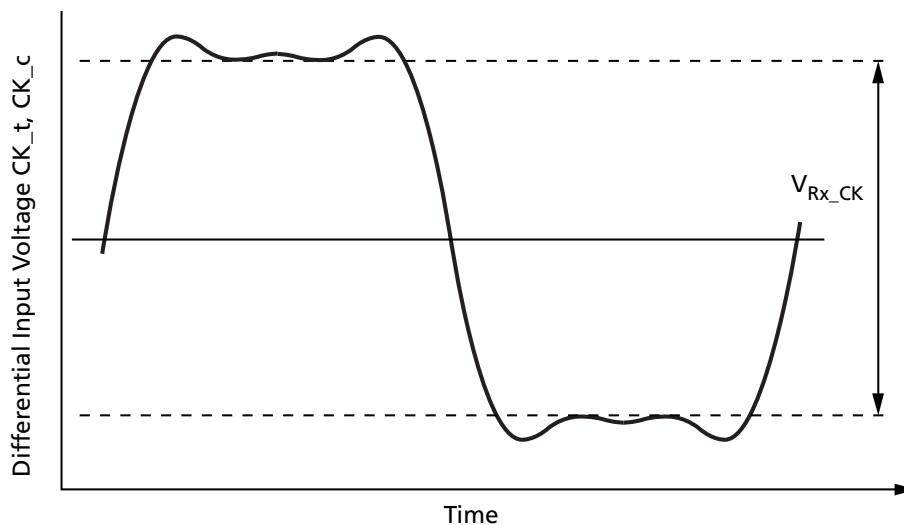
Note: 1. The validation methodology for this parameter is TBD.

Table 309: Differential Input Clock Voltage Sensitivity Parameter for 8000 to 8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		Min	Max	Min	Max	Min	Max		
Minimum input clock voltage sensitivity (differential) with no CK buffer	VRx_CK (no CKD)	-	100	-	100	-	100	mV	1
Minimum input clock voltage sensitivity (differential) with CK buffer	VRx_CK (with CKD)	-	120	-	120	-	120	mV	1

Note: 1. The validation methodology for this parameter is TBD.

Figure 240: VRx_CK



Differential Input Voltage Levels for DQS

Table 310: Differential Input Levels for DQS (DQS_t, DQS_c) — 3200-8800

Parameter	Symbol	3200-8800	Notes
Differential input high measurement level (DQS_t, DQS_c)	$V_{IH,diff}DQS$	$0.75 \times V_{diff,pk-pk}$	1,2,3
Differential input low measurement level (DQS_t, DQS_c)	$V_{IL,diff}DQS$	$0.25 \times V_{diff,pk-pk}$	1,2,3

Notes: 1. $V_{diff,pk-pk}$ defined in the following Differential Input Slew Rate Definition for DQS_t, DQS_c figure.

2. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples.

3. All parameters are defined over the entire clock common mode range.

Differential Input Slew Rate for DQS_t, DQS_c

Input slew rate for differential signals DQS_t, DQS_c are defined and measured as shown below.

Figure 241: Differential Input Slew Rate for DQS_t, DQS_c

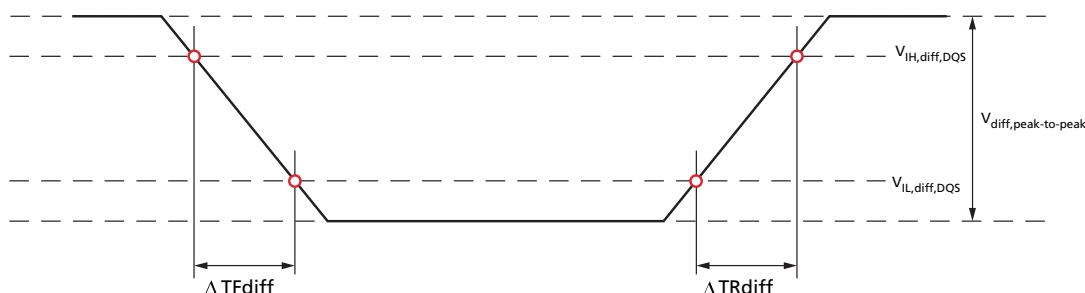


Table 311: Differential Input Slew Rate Definition for DQS_t, DQS_c

Parameter	Measured		Defined By
	From	To	
Differential input slew rate for rising edge (DQS_t - DQS_c)	$V_{IL,diff}DQS$	$V_{IH,diff}DQS$	$ V_{IL,diff}DQS - V_{IH,diff}DQS / \Delta TR_{diff}$
Differential input slew rate for falling edge (DQS_t - DQS_c)	$V_{IH,diff}DQS$	$V_{IL,diff}DQS$	$(V_{IH,diff}DQS - V_{IL,diff}DQS) / \Delta TF_{diff}$

Table 312: Differential Input Slew Rate for DQS_t, DQS_c — 3200-8800

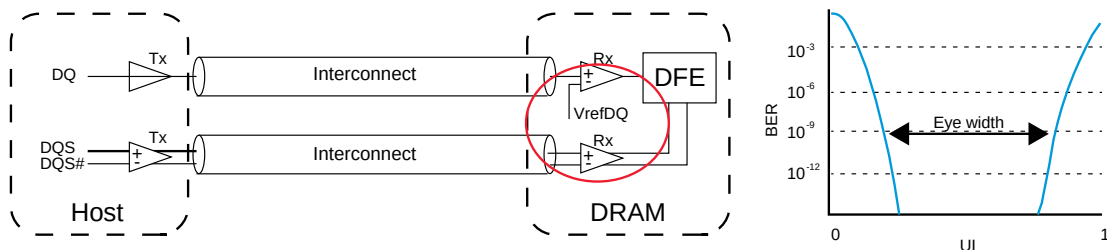
Parameter	Symbol	3200-4800		5200-8800		Unit	Note
		MIN	MAX	MIN	MAX		
Differential input slew rate for rising edge (DQS_t - DQS_c)	$S_{RI,diff,DQS}$	1.5	30	2.0	30	V/ns	1

Note: 1. Applies only when both DQS_t and DQS_c are transitioning.

Rx DQS Jitter Sensitivity

The receiver strobe jitter sensitivity test provides the methodology for testing the receiver's strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input without adding jitter, noise and ISI to the data. The receiver must pass the appropriate BER rate when no crosstalk or ISI is applied and it must pass through the combination of applied DCD and Rj.

Figure 242: Rx Forwarded Strobes for Jitter Sensitivity Testing



Specifications

The following tables provide Rx DQS jitter sensitivity specifications for the receivers when operating at various transfer rates. These parameters are tested on the CTC2 card without Rx equalization set. Additive DFE Gain Bias can be set.

Also note:

- BER = bit error rate; DCD = duty cycle distortion; Rj = random jitter
- Validation methodology will be defined in future ballots. 2UI is defined as 1^tCK for the parameters.
- All measurements at $\text{BER}=1\text{E}-9$.
- The test should be done after the DQS and DQ voltage sensitivity tests are complete and passing.
- Voltage swings and slew rates for strobe and DQ signals can be set as long as they meet specifications. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

Table 313: Rx DQS Jitter Sensitivity — 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	$t_{\text{RX\_DQ\_tMargin}}$	0.900	-	0.875	-	0.825	-	0.825	-	0.825	-	UI	1,2
Degradation of timing width compared to $t_{\text{RX\_DQ\_tMargin}}$ with DCD injection in DQS	$\Delta t_{\text{RX\_DQ\_tMargin\_DQS\_DCD}}$	-	0.060	-	0.060	-	0.060	-	0.060	-	0.060	UI	3
Degradation of timing width compared to $t_{\text{RX\_DQ\_tMargin}}$ with Rj injection in DQS	$\Delta t_{\text{RX\_DQ\_tMargin\_DQS\_Rj}}$	-	0.090	-	0.090	-	0.090	-	0.090	-	0.090	UI	4
Degradation of timing width compared to $t_{\text{RX\_DQ\_tMargin}}$ with DCD and Rj injection in DQS	$\Delta t_{\text{RX\_DQ\_tMargin\_DQS\_DCD\_Rj}}$	-	0.150	-	0.150	-	0.150	-	0.150	-	0.150	UI	1,5
Delay of any data lane relative to $\text{DQS\_t}/\text{DQS\_c}$ crossing	$t_{\text{Rx\_DQS2DQ}}$	114	937	114	833	114	750	114	738	114	729	ps	6

Table 313: Rx DQS Jitter Sensitivity — 3200-4800 (Continued)

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Delay of any data lane relative to any other data lane	t_{Rx_DQ2DQ}	-	50	-	50	-	50	-	50	-	50	ps	6,7,8

- Notes: 1. Each of $\Delta t_{Rx\_DQ\_tMargin\_DQS\_DCD}$, $\Delta t_{Rx\_DQ\_tMargin\_DQS\_Rj}$, and $\Delta t_{Rx\_DQ\_tMargin\_DQS\_DCD\_Rj}$ can be relaxed by up to 5% if $t_{Rx\_DQ\_tMargin}$ exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=1E⁻⁹.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to $t_{Rx\_DQ\_tMargin}$, measured at BER=1E⁻⁹. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=1E⁻⁹, compared to $t_{Rx\_DQ\_tMargin}$. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=1E⁻⁹, compared to $t_{Rx\_DQ\_tMargin}$. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the device balls.
8. This parameter is relative to the per-pin trained DQS2DQ value, and only applies after per-pin DQS2DQ training is complete.

Table 314: Rx DQS Jitter Sensitivity — 5200-6400

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	$t_{RX\_DQ\_tMargin}$	0.835	-	0.835	-	0.845	-	0.845	-	UI	1,2
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with DCD injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD}$	-	0.06	-	0.06	-	0.06	-	0.06	UI	3
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with Rj injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQS\_Rj}$	-	0.09	-	0.09	-	0.09	-	0.09	UI	4
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with DCD and Rj injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD\_Rj}$	-	0.15	-	0.15	-	0.15	-	0.15	UI	1,5
Delay of any data lane relative to DQS _t /DQS _c crossing	t_{Rx_DQS2DQ}	114	721	114	714	114	708	114	703	ps	6

Table 314: Rx DQS Jitter Sensitivity — 5200-6400 (Continued)

Parameter	Symbol	5200		5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Delay of any data lane relative to any other data lane	t_{Rx_DQ2DQ}	-	50	-	50	-	50	-	50	ps	6,7,8

- Notes: 1. Each of $\Delta t_{Rx\_DQ\_tMargin\_DQS\_DCD}$, $\Delta t_{Rx\_DQ\_tMargin\_DQS\_Rj}$, and $\Delta t_{Rx\_DQ\_tMargin\_DQS\_DCD\_Rj}$ can be relaxed by up to 5% if $t_{Rx\_DQ\_tMargin}$ exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=E-9.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to $t_{Rx\_DQ\_tMargin}$, measured at BER=E-9. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to $t_{Rx\_DQ\_tMargin}$. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to $t_{Rx\_DQ\_tMargin}$. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the device balls.
8. This parameter is relative to the per-pin trained DQS2DQ value, and only applies after per-pin DQS2DQ training is complete.

Table 315: Rx DQS Jitter Sensitivity — 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	$t_{RX\_DQ\_tMargin}$	0.845	-	0.845	-	0.845	-	UI	1,2
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with DCD injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQ\_S\_DCD}$	-	0.06	-	0.06	-	0.06	UI	3
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with Rj injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQ\_S\_Rj}$	-	0.09	-	0.09	-	0.09	UI	4
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with DCD and Rj injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQ\_S\_DCD\_Rj}$	-	0.15	-	0.15	-	0.15	UI	1,5
Delay of any data lane relative to DQS _t /DQS _c crossing	t_{Rx_DQS2DQ}	114	703	114	703	114	703	ps	6
Delay of any data lane relative to any other data lane	t_{Rx_DQ2DQ}	-	50	-	50	-	50	ps	6,7,8

- Notes: 1. Each of $\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD}$, $\Delta t_{RX\_DQ\_tMargin\_DQS\_Rj}$, and $\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD\_Rj}$ can be relaxed by up to 5% if $t_{RX\_DQ\_tMargin}$ exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=E-9.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to $t_{RX\_DQ\_tMargin}$, measured at BER=E-9. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to $t_{RX\_DQ\_tMargin}$. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to $t_{RX\_DQ\_tMargin}$. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the device balls.
8. This parameter is relative to the per-pin trained DQS2DQ value, and only applies after per-pin DQS2DQ training is complete.

Table 316: Rx DQS Input Voltage Sensitivity Parameter — 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQ timing width	$t_{RX\_DQ\_tMargin}$	0.845	-	0.845	-	0.845	-	UI	1,2
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with DCD injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD}$	-	0.06	-	0.06	-	0.06	UI	3
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with Rj injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQS\_Rj}$	-	0.09	-	0.09	-	0.09	UI	4
Degradation of timing width compared to $t_{RX\_DQ\_tMargin}$ with DCD and Rj injection in DQS	$\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD\_Rj}$	-	0.15	-	0.15	-	0.15	UI	1,5
Delay of any data lane relative to DQS_t/DQS_c crossing	t_{Rx_DQS2DQ}	114	703	114	703	114	703	ps	6
Delay of any data lane relative to any other data lane	t_{Rx_DQ2DQ}	-	50	-	50	-	50	ps	6,7,8

- Notes: 1. Each of $\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD}$, $\Delta t_{RX\_DQ\_tMargin\_DQS\_Rj}$, and $\Delta t_{RX\_DQ\_tMargin\_DQS\_DCD\_Rj}$ can be relaxed by up to 5% if $t_{RX\_DQ\_tMargin}$ exceeds the spec by 5% or more.
2. DQ timing width: timing width for any data lane using repetitive patterns (check note 3 for the pattern) measured at BER=E-9.
3. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe DQS compared to $t_{RX\_DQ\_tMargin}$, measured at BER=E-9. The magnitude of DCD is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing. Test using clock-like pattern of repeating three 1s and three 0s.

4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe DQS measured at BER=E-9, compared to $t_{RX\_DQ\_tMargin}$. The magnitude of Rj is specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe DQS measured at BER=E-9, compared to $t_{RX\_DQ\_tMargin}$. The magnitudes of DCD and Rj are specified in Test Conditions for Rx DQS Jitter Sensitivity Testing.
6. Delay of any data lane relative to the strobe lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
7. DQ to DQ offset is skew between DQs within a nibble (x4) or a byte (x8, x16) at the device balls.
8. This parameter is relative to the per-pin trained DQS2DQ value, and only applies after per-pin DQS2DQ training is complete.

Test Conditions

The following table lists the amount of duty cycle distortion (DCD) and/or random jitter (Rj) that must be applied to the forwarded strobe when measuring the Rx strobe jitter sensitivity parameters specified in the previous tables.

Table 317: Test Conditions for Rx DQS Jitter Sensitivity Testing — 3200-8800

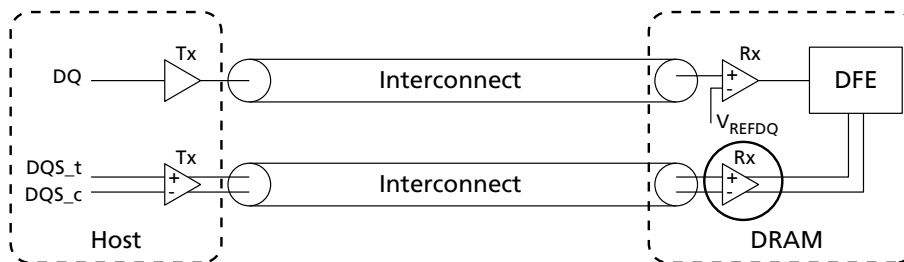
Parameter	Symbol	3200-8800		Unit	Note
		MIN	MAX		
Applied DCD to the DQS	$t_{RX\_DQS\_DCD}$	-	0.045	UI	1,2,3,6,7,10
Applied to Rj RMS to the DQS	$t_{RX\_DQS\_Rj}$	-	0.0075	UI (RMS)	1,2,4,6,8,10
Applied DCD and Rj RMS to the DQS	$t_{RX\_DQS\_DCD\_Rj}$	-	0.045 UI DCD + 0.0075 UI Rj RMS	UI	1,2,5,6,7,9,10

- Notes:
1. While imposing these specifications, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
 2. The jitter response of the forwarded strobe channel depends on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified; instead, the response characterization is done at the specified clock amplitude only. The specified voltages are at the Rx input pin.
 3. Various DCD values should be tested, complying within the maximum limits.
 4. Various Rj values should be tested, complying within the maximum limits.
 5. Various combinations of DCD and Rj values should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of the injected jitter is specified in a separate table.
 6. Although the device has bursty traffic, current available BERTs that can be used for this test do not support burst traffic patterns. A continuous strobe and continuous DQ are used for this parameter. The clock-like pattern repeating three 1s and three 0s is used for this test.
 7. Duty cycle distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).
 8. RMS value of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
 9. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
 10. Voltage swing and slew rates can be set for strobe and DQ signals as long as they meet the specification. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.

Rx DQS Voltage Sensitivity

The receiver strobe input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of inter-symbol interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

Figure 243: Example of DDR5 Memory Interconnect



Receiver Strobe Voltage Sensitivity Parameters

The table below shows how input differential (DQS_t, DQS_c) V_{Rx_DQS} is defined and measured. The receiver must pass the minimum BER requirements for the device. These parameters are tested on the CTC2 card with neither additive gain nor Rx equalization set.

Table 318: Rx DQS Input Voltage Sensitivity Parameter — 3200-4800

Parameter	Symbol	3200		3600		4000		4400-4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	130	-	115	-	105	-	100	mV	1, 2

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. Test using clock-like pattern of repeating three 1s and three 0s

Table 319: Rx DQS Input Voltage Sensitivity Parameter — 5200-6400

Parameter	Symbol	5200-5600		6000-6400		Unit	Note
		MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	90	-	83	mV	1, 2

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. Test using clock-like pattern of repeating three 1s and three 0s

Table 320: Rx DQS Input Voltage Sensitivity Parameter — 6800-7600

Parameter	Symbol	6800-7200		7600		Unit	Note
		MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	80	-	77.5	mV	1, 2

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. Test using clock-like pattern of repeating three 1s and three 0s

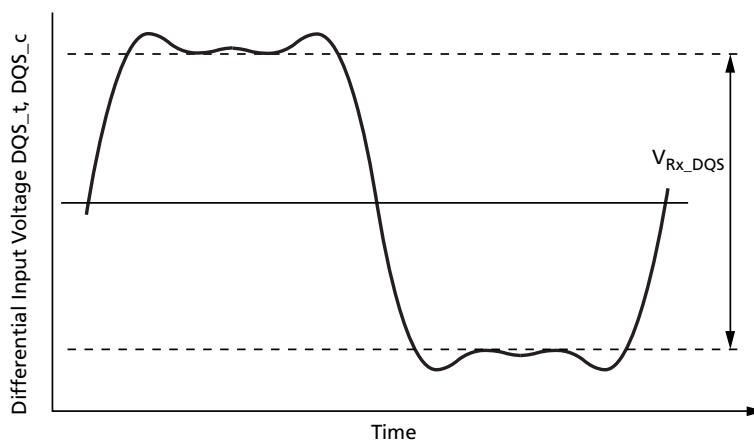
Table 321: Rx DQS Input Voltage Sensitivity Parameter — 8000-8800

Parameter	Symbol	8000		8400-8800		Unit	Note
		MIN	MAX	MIN	MAX		
Minimum DQS Rx input voltage sensitivity (differential)	V_{Rx_DQS}	-	77.5	-	75	mV	1, 2

Notes: 1. Refer to the minimum BER requirements for DDR5.

2. Test using clock-like pattern of repeating three 1s and three 0s

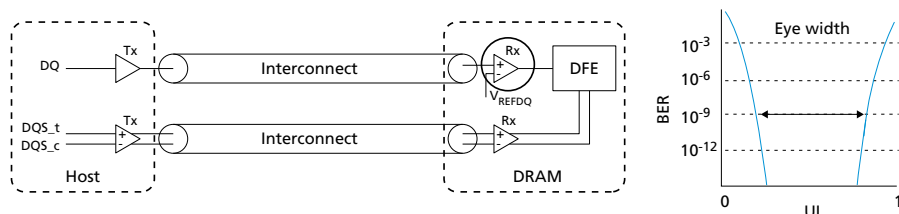
Figure 244: V_{RX_DQS}



Rx DQ Voltage Sensitivity

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of inter-symbol interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

Figure 245: Example of DDR5 Memory Interconnect



Receiver DQ Input Voltage Sensitivity Parameters

Input single-ended V_{RX_DQ} is defined and measured as shown below. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested on the CTC2 card with neither additive gain nor Rx Equalization set.

Table 322: Rx DQ Input Voltage Sensitivity Parameter for DDR5 3200-4800

Parameter	Symbol	3200		3600		4000		4400-4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{RX_DQ}	-	85	-	75	-	70	-	65	mV	1, 2, 3

- Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 323: Rx DQ Input Voltage Sensitivity Parameter for DDR5 5200-6400

Parameter	Symbol	5200-5600		6000-6400		Unit	Note
		MIN	MAX	MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{RX_DQ}	-	60	-	55	mV	1, 2, 3

- Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 324: Rx DQ Input Voltage Sensitivity Parameter for DDR5 6800-7600

Parameter	Symbol	6800-7600		Unit	Note
		MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{RX_DQ}	-	50	mV	1, 2, 3

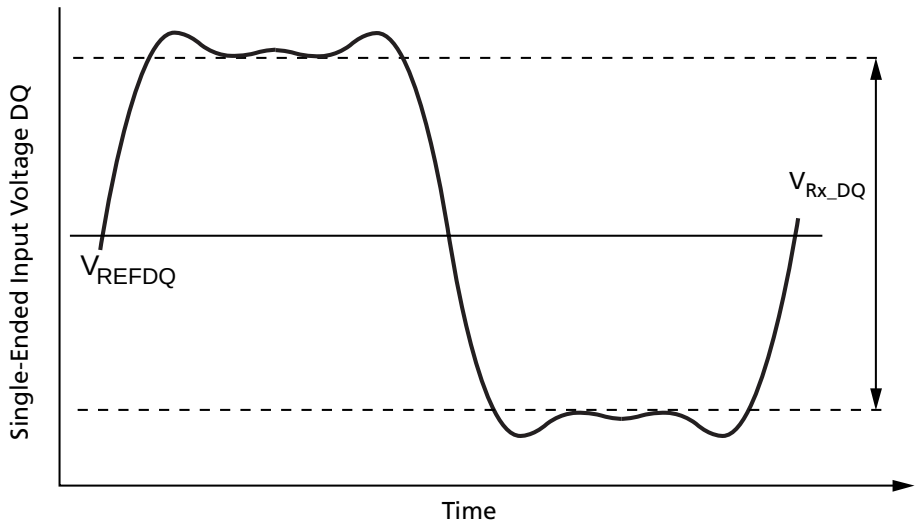
- Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Table 325: Rx DQ Input Voltage Sensitivity Parameter for DDR5 8000-8800

Parameter	Symbol	8000		8400-8800		Unit	Note
		MIN	MAX	MIN	MAX		
Minimum DQ Rx input voltage sensitivity applied around V_{REF}	V_{RX_DQ}	-	50	-	47.5	mV	1, 2, 3

Notes: 1. Refer to the minimum BER requirements for DDR5.
2. The validation methodology for this parameter will be covered in future ballot(s).
3. Test using clock-like pattern of repeating three 1s and three 0s

Figure 246: V_{RX_DQ}



Rx Stressed Eye

The stressed eye tests provide a methodology for creating the appropriate stress for the device's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

Figure 247: Example: RX Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

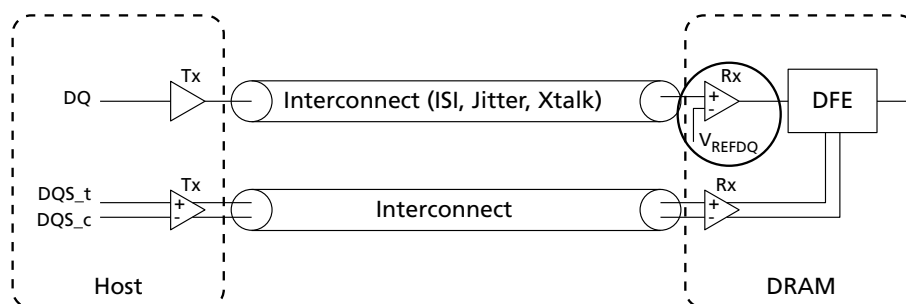
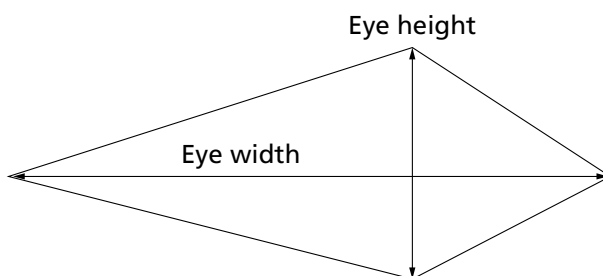


Figure 248: Example of Rx Stressed Eye Height and Eye Width



Parameters

In the following tables, BER = bit error rate, DCD = duty cycle distortion, Rj = random jitter, Sj = sinusoidal jitter, p-p = peak to peak.

Table 326: Test Conditions for Rx Stressed Eye Tests for DDR5 3200-4800

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	95	-	85	-	80	-	75	-	70	-	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	-	600	-	600	mV	1,2

Table 326: Test Conditions for Rx Stressed Eye Tests for DDR5 3200-4800 (Continued)

Parameter	Symbol	3200		3600		4000		4400		4800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	0	125	0	125	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

- Notes: 1. Must meet minimum BER of 10^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER 10^{-9} and extrapolating to BER 10^{-16} .
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and refer to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 should be less than 60mV ($|Tap-2| + |Tap-3| + |Tap-4| < 60mV$) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ} , DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ} , and DFE solution to give the best eye margin.
10. The Rx stressed eye specification applies at 2933 and faster data rates.
11. EH/EW are measured at the slicer of the receiver.

Table 327: Test Conditions for Rx Stressed Eye Tests for DDR5 5200-6400

Parameter	Symbol	5200		5600		6000-6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	65	-	60	-	57.5	-	mV	1,2,3,4,5,6,7,8,9

Table 327: Test Conditions for Rx Stressed Eye Tests for DDR5 5200-6400 (Continued)

Parameter	Symbol	5200		5600		6000-6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	0.235	-	0.235	-	0.230	-	UI	1,2,3,4,5,6,7,8,9
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	-	0.45	-	0.45	-	0.45	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	-	0.04	-	0.04	-	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	-	125	-	125	-	125	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

- Notes: 1. Must meet minimum BER of 1E^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER 1E^{-9} and extrapolating to BER 1E^{-16} .
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and refer to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 must be less than 60mV ($|Tap-2| + |Tap-3| + |Tap-4| < 60\text{mV}$) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ} , DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ} , and DFE solution to give the best eye margin.
10. The Rx stressed eye specification applies at 2933 and faster data rates.
11. EH/EW are measured at the slicer of the receiver.

Table 328: Test Conditions for Rx Stressed Eye Tests for DDR5 6800-7600

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	55	-	55	-	54	-	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	0.23	-	0.23	-	0.23	-	UI	2,3,4,5,6,7,8
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

- Notes: 1. Must meet minimum BER of 10^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER 10^{-9} and extrapolating to BER 10^{-16} .
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and refer to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 must be less than 60mV ($|Tap-2| + |Tap-3| + |Tap-4| < 60mV$) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ} , DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ} and DFE solution to give the best eye margin..
10. The Rx stressed eye specification applies at 2933 and faster data rates.
11. EH/EW are measured at the slicer of the receiver.

Table 329: Test Conditions for Rx Stressed Eye Tests for DDR5 8000-8800

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Eye height of stressed eye for golden reference channel 1	RxEH_Stressed_Eye_Golden_Ref_Channel_1	54	-	53	-	53	-	mV	1,2,3,4,5,6,7,8,9
Eye width of stressed eye golden reference channel 1	RxEW_Stressed_Eye_Golden_Ref_Channel_1	0.23	-	0.23	-	0.23	-	UI	2,3,4,5,6,7,8
Vswing stress to meet above data eye	Vswing_Stressed_Eye_Golden_Ref_Channel_1	-	600	-	600	-	600	mV	1,2
Injected sinusoidal jitter at 200 MHz to meet above data eye	Sj_Stressed_Eye_Golden_Ref_Channel_1	0	0.45	0	0.45	0	0.45	UI p-p	1,2
Injected random wide band (10 MHz-1 GHz) jitter to meet above data eye	Rj_Stressed_Eye_Golden_Ref_Channel_1	0	0.04	0	0.04	0	0.04	UI RMS	1,2
Injected voltage noise as PRBS23, or injected voltage noise at 2.1 GHz	Vnoise_Stressed_Eye_Golden_Ref_Channel_1	0	125	0	125	0	125	mV p-p	1,2
Golden reference channel 1 characteristics as measured at TBD	Golden_Ref_Channel_1_Characteristics	TBD	TBD	TBD	TBD	TBD	TBD	TBD	3

- Notes: 1. Must meet minimum BER of 1E^{-16} or better requirements with the stressed eye at the slicer of the receiver (after equalization is applied in the summer). The eye shape is verified by measuring to BER 1E^{-9} and extrapolating to BER 1E^{-16} .
2. These parameters are applied on the defined golden reference channel with parameters TBD.
3. DFE tap 1-4 bias settings that give the best eye margin are used and refer to the values in the DFE Tap Coefficients MIN/MAX Ranges table. DFE tap range limits apply: sum of absolute values of Tap-2, Tap-3, and Tap-4 must be less than 60mV ($|Tap-2| + |Tap-3| + |Tap-4| < 60\text{mV}$) after the tap multiplier is applied.
4. Evaluated with no DC supply voltage drift.
5. Evaluated with no temperature drift.
6. Supply voltage noise limited according to DC bandwidth specifications (see DC Operating Conditions).
7. The stressed eye is assumed to have a diamond shape.
8. For this test, the following can be adjusted as needed without exceeding the specifications, including the limits described in note 1: V_{REFDQ} , DFE gain bias step, and DFE Taps 1, 2, 3, 4 bias step.
9. The stressed eye is defined as centered on the DQS_t/DQS_c crossing during the calibration. Measurement includes an optimal set of DQS_t/DQS_c location, V_{REFDQ} and DFE solution to give the best eye margin..
10. The Rx stressed eye specification applies at 2933 and faster data rates.
11. EH/EW are measured at the slicer of the receiver.

AC and DC Logic Output Levels and Timing

Output Driver DC Electrical Characteristics for DQS and DQ

The DDR5 driver supports two different R_{ON} values. These R_{ON} values are referred as strong (low R_{ON}) and weak (high R_{ON}) modes. A functional representation of the output buffer is shown in the figure below.

A low voltage V_{DDQ} rail is under investigation and may be added in the future. Output driver impedance R_{ON} is defined as follows:

The individual pull-up and pull-down resistors ($R_{ON,Pu}$ and $R_{ON,Pd}$) are defined as follows:

$$R_{ON,Pu} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPd} \text{ is off}$$

$$R_{ON,Pd} = \frac{V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPu} \text{ is off}$$

Figure 249: Output Driver

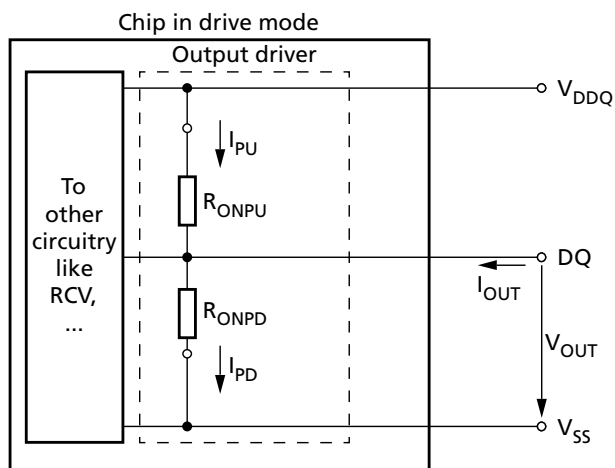


Table 330: Output Driver DC Electrical Characteristics (assuming $R_{ZQ} = 240\Omega$, over entire operating temperature range, and after proper ZQ calibration)

$R_{ON,NOM}$	Resistor	V_{OUT}	MIN	NOM	MAX	Unit	Notes
34 Ω	R_{ON34Pd}	$V_{OLdc} = 0.5 \times V_{DDQ}$	0.73	1	1.1	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	0.83	1	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 0.95 \times V_{DDQ}$	0.83	1	1.25	$R_{ZQ}/7$	1, 2
	R_{ON34Pu}	$V_{OLdc} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/7$	1, 2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/7$	1, 2
		$V_{OHdc} = 0.95 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/7$	1, 2
48 Ω	R_{ON48Pd}	$V_{OLdc} = 0.5 \times V_{DDQ}$	0.73	1	1.1	$R_{ZQ}/5$	1, 2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	0.83	1	1.1	$R_{ZQ}/5$	1, 2
		$V_{OHdc} = 0.95 \times V_{DDQ}$	0.83	1	1.25	$R_{ZQ}/5$	1, 2
	R_{ON48Pu}	$V_{OLdc} = 0.5 \times V_{DDQ}$	0.9	1	1.25	$R_{ZQ}/5$	1, 2
		$V_{OMdc} = 0.8 \times V_{DDQ}$	0.9	1	1.1	$R_{ZQ}/5$	1, 2
		$V_{OHdc} = 0.95 \times V_{DDQ}$	0.8	1	1.1	$R_{ZQ}/5$	1, 2

Table 330: Output Driver DC Electrical Characteristics (assuming $R_{ZQ} = 240\Omega$, over entire operating temperature range, and after proper ZQ calibration) (Continued)

$R_{ON,NOM}$	Resistor	V_{OUT}	MIN	NOM	MAX	Unit	Notes
Mismatch between pull-up and pull-down, MM_{PuPd}		$V_{OMdc} = 0.8 \times V_{DDQ}$	-10		10	%	1, 2, 3, 4
Mismatch DQ-DQ within byte variation pull-up, MM_{Pudd}		$V_{OMdc} = 0.8 \times V_{DDQ}$			10	%	1, 2, 4
Mismatch DQ-DQ within byte variation pull-down, MM_{Pddd}		$V_{OMdc} = 0.8 \times V_{DDQ}$			10	%	1, 2, 4

- Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the ZQ Calibration Commands section on voltage and temperature sensitivity.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at $0.8 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.5 \times V_{DDQ}$ and $0.95 \times V_{DDQ}$.
3. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd} : Measure $R_{ON,Pu}$ and $R_{ON,Pd}$ both at $0.8 \times V_{DD}$ separately; $R_{ON,NOM}$ is the nominal R_{ON} value

$$MM_{PuPd} = \frac{R_{ON,Pu} - R_{ON,Pd}}{R_{ON,NOM}} \times 100$$

4. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including DQS_t and DQS_c .

$$MM_{Pu,dd} = \frac{R_{ON,Pu,Max} - R_{ON,Pu,Min}}{R_{ON,NOM}} \times 100$$

$$MM_{Pd,dd} = \frac{R_{ON,Pd,Max} - R_{ON,Pd,Min}}{R_{ON,NOM}} \times 100$$

5. This parameter of x16 device is specified for upper byte and lower byte.

Output Driver DC Electrical Characteristics for Loopback Signals LBDQS, LBDQ

The DDR5 loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$$R_{ON,Pu} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPd} \text{ is off}$$

$$R_{ON,Pd} = \frac{V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPu} \text{ is off}$$

Figure 250: Output Driver for Loopback Signals

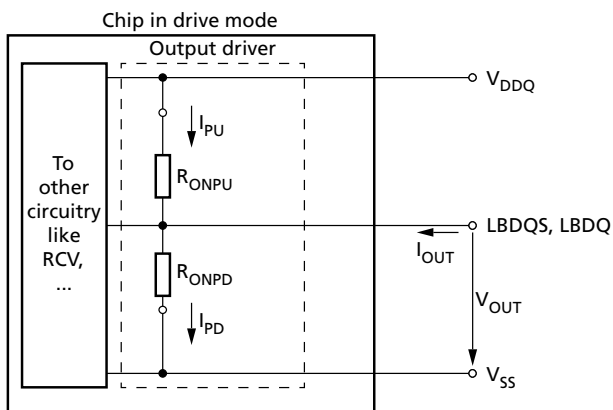


Table 331: Output Driver DC Electrical Characteristics, Assuming $R_{ZQ} = 240\Omega$; Entire Operating Temperature Range; After Proper ZQ Calibration

R _{ON,NOM}	Resistor	V _{OUT}	MIN	NOM	MAX	Unit	Notes
34Ω	R _{ON34Pd}	V _{OLdc} = 0.5 × V _{DDQ}	0.8	1	1.1	R _{ZQ} /7	1, 2
		V _{OMdc} = 0.8 × V _{DDQ}	0.9	1	1.1	R _{ZQ} /7	1, 2
		V _{OHdc} = 0.95 × V _{DDQ}	0.9	1	1.25	R _{ZQ} /7	1, 2
	R _{ON34Pu}	V _{OLdc} = 0.5 × V _{DDQ}	0.9	1	1.25	R _{ZQ} /7	1, 2
		V _{OMdc} = 0.8 × V _{DDQ}	0.9	1	1.1	R _{ZQ} /7	1, 2
		V _{OHdc} = 0.95 × V _{DDQ}	0.8	1	1.1	R _{ZQ} /7	1, 2
Mismatch between pull-up and pull-down, MM _{PuPd}		V _{OMdc} = 0.8 × V _{DDQ}	-10		10	%	1, 2, 3, 4
Mismatch LBDQS-LBDQ within byte variation pull-up, MM _{Pudd}		V _{OMdc} = 0.8 × V _{DDQ}			10	%	1, 2, 4
Mismatch LBDQS-LBDQ within byte variation pull-down, MM _{Pddd}		V _{OMdc} = 0.8 × V _{VDDQ}			10	%	1, 2, 4

Notes: 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see the ZQ Calibration Commands section on voltage and temperature sensitivity (TBD).

2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at $0.8 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.5 \times V_{DDQ}$ and $0.95 \times V_{DDQ}$.

3. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd} : Measure $R_{ON,Pu}$ and $R_{ON,Pd}$ both at $0.8 \times V_{DD}$ separately; $R_{ON,NOM}$ is the nominal R_{ON} value

$$MM_{PuPd} = \frac{R_{ON,Pu} - R_{ON,Pd}}{R_{ON,NOM}} \times 100$$

4. R_{ON} variance range ratio to R_{ON} nominal value in a given component, including LBDQS and LBDQ.

$$MM_{Pu,dd} = \frac{R_{ON,Pu,Max} - R_{ON,Pu,Min}}{R_{ON,NOM}} \times 100$$

$$MM_{Pd,dd} = \frac{R_{ON,Pd,Max} - R_{ON,Pd,Min}}{R_{ON,NOM}} \times 100$$

Loopback Output Timing

The loopback strobe LBDQS to loopback data LBDQ relationship is illustrated in the figure in this section.

- t_{LBQSH} describes the single-ended LBDQS strobe high pulse width
- t_{LBQSL} describes the single-ended LBDQS strobe low pulse width
- t_{LBQ_Set} describes the setup time of LBDQS and where LBDQ needs to remain stable
- t_{LBQ_Hld} describes the hold time of LBDQS and where LBDQ needs to remain stable
- t_{LBDVW} describes the data valid window per device per UI

Table 332: Loopback Output Timing 3200-8800

Parameter	Symbol	3200-5600		6000-8800		Unit	Note
		MIN	MAX	MIN	MAX		
Loopback LBDQS Output Low Time	t_{LBQSL}	0.7	-	0.75	-	t_{CK}	1
Loopback LBDQS Output High Time	t_{LBQSH}	0.7	-	0.75	-	t_{CK}	1

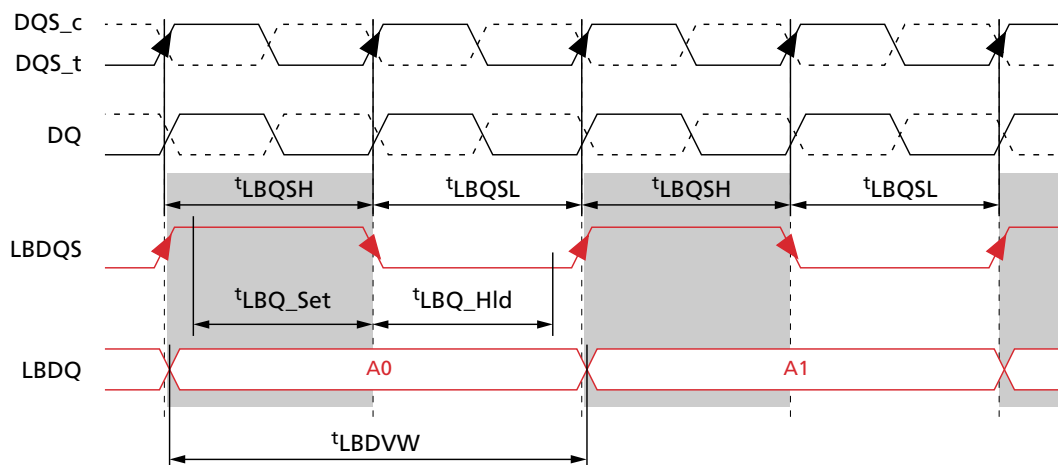
Table 332: Loopback Output Timing 3200-8800 (Continued)

Parameter	Symbol	3200-5600		6000-8800		Unit	Note
		MIN	MAX	MIN	MAX		
Loopback setup time for LBDQS	t_{LBQ_Set}	0.5	-	0.55	-	t_{CK}	1,2
Loopback hold time for LBDQS	t_{LBQ_Hld}	0.5	-	0.55	-	t_{CK}	1,2
Loopback Data valid window of each UI per DRAM	t_{LBDVW}	1.6	-	1.6	-	t_{CK}	1

Notes: 1. Based on loopback four-way interleave setting (see MR53)

2. t_{LBQ_Set} is measured from LBDQ first transition to LBDQS falling edge and t_{LBQ_Hld} is measured from LBDQS falling edge to LBDQ last transition.

Figure 251: Loopback Strobe to Data Relationship



Alert_n Output Driver Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance R_{ON} is defined as follows:

$$R_{ON,Pd} = \frac{V_{OUT}}{|I_{OUT}|} \text{ under the condition that } R_{ONPU} \text{ is off}$$

Figure 252: Alert Driver

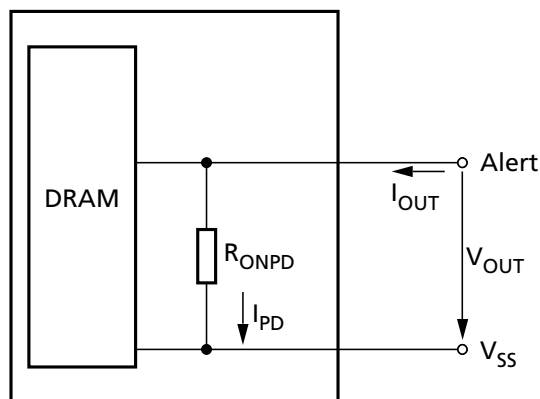


Table 333: Alert_n Output Driver DC Electrical Characteristics

Resistor	V _{OUT}	MIN	MAX	Unit
R _{ONPd}	V _{OLdc} = 0.1 × V _{DDQ}	0.3	1.1	R _{ZQ} /7
	V _{OMdc} = 0.8 × V _{DDQ}	0.4	1.1	R _{ZQ} /7
	V _{OHdc} = 0.95 × V _{DDQ}	0.4	1.25	R _{ZQ} /7

Connectivity Test Mode Output Driver Characteristics

Following output driver impedance, R_{ON} will be applied to the test output pins during connectivity test (CT) mode.

The individual pull-up and pull-down resistors (R_{ON,Pu_CT} and R_{ON,Pd_CT}) are defined as follows:

$$R_{ON,Pu\_CT} = \frac{V_{DDQ} - V_{OUT}}{|I_{OUT}|}$$

$$R_{ON,Pd\_CT} = \frac{V_{OUT}}{|I_{OUT}|}$$

Figure 253: Chip-In Drive Mode

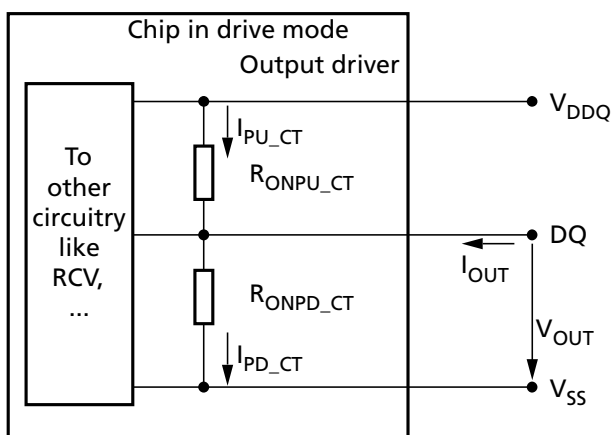


Table 334: Connectivity Test (CT) Mode Output Driver DC Electrical Characteristics

R _{ON,NOM_CT}	Resistor	V _{OUT}	MAX	Unit	Notes
34Ω	R _{ON,Pd_CT}	V _{OB,dc} = 0.2 × V _{DDQ}	1.9	R _{ZQ} /7	1,2
		V _{OLdc} = 0.5 × V _{DDQ}	2.0	R _{ZQ} /7	1,2
		V _{OMdc} = 0.8 × V _{DDQ}	2.2	R _{ZQ} /7	1,2
		V _{OHdc} = 0.95 × V _{DDQ}	2.5	R _{ZQ} /7	1,2
	R _{ON,Pu_CT}	V _{OB,dc} = 0.2 × V _{DDQ}	1.9	R _{ZQ} /7	1,2
		V _{OLdc} = 0.5 × V _{DDQ}	2.0	R _{ZQ} /7	1,2
		V _{OMdc} = 0.8 × V _{DDQ}	2.2	R _{ZQ} /7	1,2
		V _{OHdc} = 1.1 × V _{DDQ}	2.5	R _{ZQ} /7	1,2

Notes: 1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull-up and pull-down is defined.

2. Uncalibrated drive strength tolerance is specified at ±30%.

Single-Ended Output Levels

Table 335: Single-Ended Output Levels for DDR5 3200-8800

Parameter	Symbol	3200-8800	Unit	Notes
Output high measurement level (for output SR)	V_{OH}	$0.75 \times V_{pk-pk}$	V	1
Output low measurement level (for output SR)	V_{OL}	$0.25 \times V_{pk-pk}$	V	1

Note: 1. V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.

Single-Ended Output Levels for Loopback Signals

Table 336: Single-Ended Output Levels for Loopback Signals for DDR5 3200-8800

Parameter	Symbol	3200-8800	Unit	Notes
Output high measurement level (for output SR)	V_{OH}	$0.75 \times V_{pk-pk}$	V	1
Output low measurement level (for output SR)	V_{OL}	$0.25 \times V_{pk-pk}$	V	1

Note: 1. V_{pk-pk} is the mean high voltage minus the mean low voltage over 8UI samples.

Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL} and V_{OH} for single-ended signals, as described in the following tables and figure.

Table 337: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	V_{OL}	V_{OH}	$[V_{OH} - V_{OL}] / \Delta TRse$
Single-ended output slew rate for failing edge	V_{OH}	V_{OL}	$[V_{OL} - V_{OH}] / \Delta TFse$

Note: 1. Output slew rate is verified by design and characterization and may not be subject to production test.

Figure 254: Single-Ended Output Slew Rate Definition

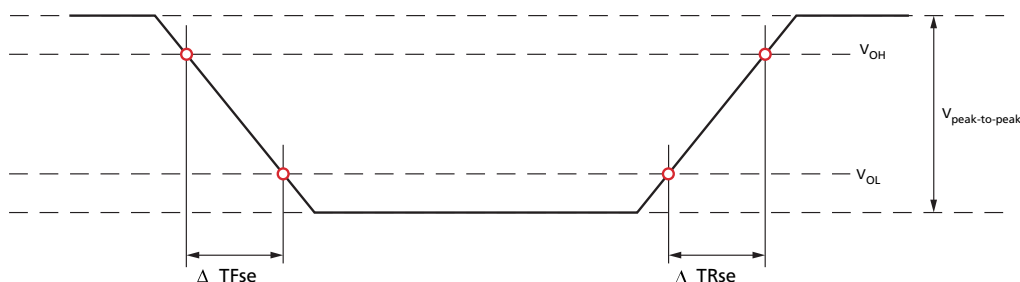


Table 338: New Single-Ended Output Slew Rate for DDR5 3200-8800

Parameter	Symbol	3200-4800		5200-8800		Unit	Note
		MIN	MAX	MIN	MAX		
Single-ended output slew rate	SRQse	8	24	12	24	V/ns	



Table 339: DDP Single-Ended Output Slew Rate for DDR5 3200-6400

Parameter	Symbol	3200-6400		Unit	Note
		MIN	MAX		
Single-ended output slew rate	SRQse	4	15	V/ns	

Differential Output Levels

Table 340: Differential Output Levels for DDR5 3200-8800

Symbol	Parameter	3200-8800	Unit	Note
$V_{OH,diff}$	Differential output high measurement level (for output SR)	$0.75 \times V_{diff,pk-pk}$	V	1
$V_{OL,diff}$	Differential output low measurement level (for output SR)	$0.25 \times V_{diff,pk-pk}$	V	1

Note: 1. $V_{diff,pk-pk}$ is the mean high voltage minus the mean low voltage over 8UI samples.

Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL,diff}$ and $V_{OH,diff}$ for differential signals, as shown in the tables below.

Table 341: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff}$	$V_{OH,diff}$	$[V_{OH,diff}, V_{OL,diff}] / \Delta TR_{diff}$
Differential output slew rate for failing edge	$V_{OH,diff}$	$V_{OL,diff}$	$[V_{OL,diff}, V_{OH,diff}] / \Delta TF_{diff}$

Note: 1. Output slew rate is verified by design and characterization and may not be subject to production test.

Figure 255: Differential Output Slew Rate Definition

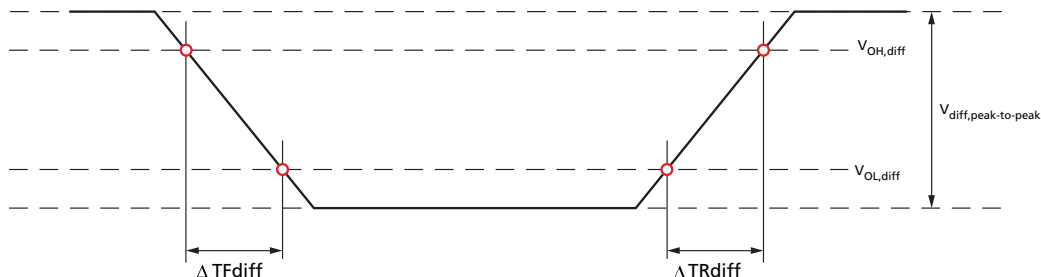


Table 342: Differential Output Slew Rate for DDR5 3200-8800

Parameter	Symbol	3200-4800		5200-8800		Unit
		MIN	MAX	MIN	MAX	
Differential output slew rate	SRQdiff	16	48	24	48	V/ns

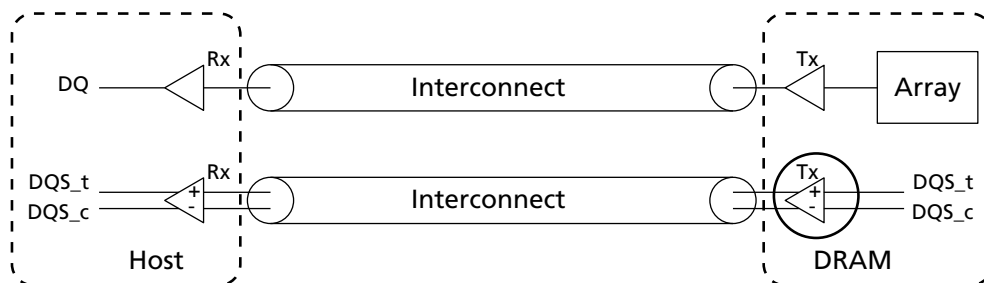
Table 343: DDP Differential Output Slew Rate for DDR5 3200-6400

Parameter	Symbol	3200-6400		Unit
		Min	Max	
Differential output slew rate	SRQdiff	8	30	V/ns

Tx DQS Jitter

The random jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The deterministic jitter (Dj) specified is bounded. The device output jitter must not exceed maximum values specified in the tables below.

Figure 256: Tx DQS Jitter



Tx DQS Jitter Parameters

The following notes apply to all tables:

- DCD = duty cycle distortion; BUJ = bounded uncorrelated jitter; pp = peak to peak
- On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.
- The validation methodology for these parameters will be covered in the future.
- See the AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
- The DQ pins' duty cycle must be adjusted as close to 50% as possible using the Global and Per-Pin Duty Cycle Adjuster feature prior to running the Tx DQS jitter test.
- The mode registers for the Duty Cycle Adjuster are MR43 and MR44. The mode registers for the per-pin DCA of DQS are MR103-MR110.
- Spread spectrum clocking (SSC) must be disabled while running the Tx DQS jitter test.
- These parameters are tested using the continuous clock pattern, which is sent out from the device without the need for sending out continuous MRR commands. Set MR25:OP[3] = 1 to enable this feature.
- These parameters are tested on the CTC2 card only.

Table 344: Tx DQS Jitter Parameters for DDR5 3200-4800

Parameter	Symbol	3200-4800		Unit	Note
		MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	^t TX_DQS_1UI_Rj_NoBUJ	-	^t CK_1UI_Rj_noBUJ + 0.002	UI (RMS)	1,2,3
Dj pp value of 1-UI jitter without BUJ	^t TX_DQS_1UI_Dj_NoBUJ	-	0.150	UI	2

Table 344: Tx DQS Jitter Parameters for DDR5 3200-4800 (Continued)

Parameter	Symbol	3200-4800		Unit	Note
		MIN	MAX		
Rj RMS value of N-UI jitter without BUJ, where N = 2,3	$t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$	-	$t_{CK\_NU\_Rj\_noBUJ} + 0.002$	UI (RMS)	2,3
Dj pp value of N-UI jitter without BUJ, where N = 2,3	$t_{Tx\_DQS\_NUI\_Dj\_NoBUJ}$	-	0.150	UI	2

Notes: 1. Rj RMS value of 1-UI jitter. Without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.

2. See the AC and DC Global Definitions section for details on minimum BER requirements.

3. The maximum value of $t_{TX\_DQS\_1UI\_Rj\_NoBUJ}$ and $t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$ can be 6m UI RMS.

Table 345: Tx DQS Jitter Parameters for DDR5 5200-6400

Parameter	Symbol	5200-5600		6000-6400		Unit	Note
		MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	$t_{TX\_DQS\_1UI\_Rj\_NoBUJ}$	-	$t_{CK\_1UI\_Rj\_noBUJ} + 0.002$	-	$t_{CK\_1UI\_Rj\_NoBUJ} + 0.002$	UI (RMS)	1,2,3
Dj pp value of 1-UI jitter without BUJ	$t_{TX\_DQS\_1UI\_Dj\_NoBUJ}$	-	0.130	-	0.130	UI	2
Rj RMS value of N-UI jitter without BUJ, where $1 < N = 4$	$t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$	-	$t_{CK\_NUI\_Rj\_noBUJ} + 0.002$	-	-	UI (RMS)	2,3
Dj pp value of N-UI jitter without BUJ, where $1 < N = 4$	$t_{Tx\_DQS\_NUI\_Dj\_NoBUJ}$	-	0.130	-	-	UI	2
Rj RMS value of N-UI jitter without BUJ, where $1 < N = 5$	$t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$	-	-	-	$t_{CK\_NUI\_Rj\_NoBUJ} + 0.002$	UI (RMS)	2,3
Dj pp value of N-UI jitter without BUJ, where $1 < N = 5$	$t_{Tx\_DQS\_NUI\_Dj\_NoBUJ}$	-	-	-	0.130	UI	2

Notes: 1. Rj RMS value of 1-UI jitter. Without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.

2. See the AC and DC Global Definitions section for details on minimum BER requirements.

3. The maximum value of $t_{TX\_DQS\_1UI\_Rj\_NoBUJ}$ and $t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$ can be 6m UI RMS.

Table 346: Tx DQS Jitter Parameters for DDR5 6800-8800

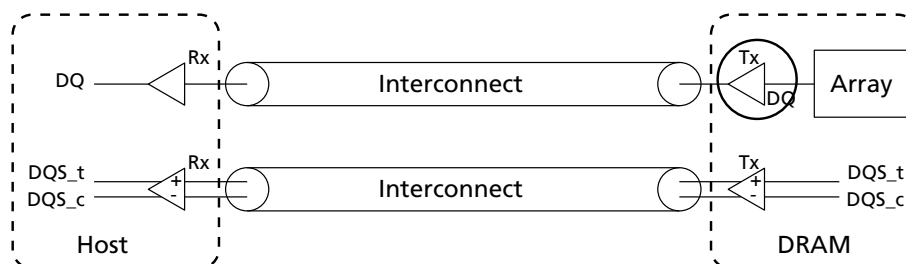
Parameter	Symbol	6800-8800		Unit	Note
		MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	$t_{TX\_DQS\_1UI\_Rj\_NoBUJ}$	-	0.006	UI (RMS)	1,2,3
Dj pp value of 1-UI jitter without BUJ	$t_{TX\_DQS\_1UI\_Dj\_NoBUJ}$	-	0.130	UI	2,3
Rj RMS value of N-UI jitter without BUJ, where $1 < N < 6$	$t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$	-	0.006	UI (RMS)	2,3
Dj pp value of N-UI jitter without BUJ, where $1 < N < 6$	$t_{Tx\_DQS\_NUI\_Dj\_NoBUJ}$	-	0.130	UI	2

Notes: 1. Rj RMS value of 1-UI jitter. Without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
2. See the AC and DC Global Definitions section for details on minimum BER requirements.
3. The maximum value of $t_{TX\_DQS\_1UI\_Rj\_NoBUJ}$ and $t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$ can be 6m UI RMS.

Tx DQ Jitter

The random jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The deterministic jitter (Dj) specified is bounded. The device output jitter must not exceed maximum values specified in the tables below.

Figure 257: Tx DQ Jitter



Tx DQ Jitter Parameters

The following notes apply to all tables:

- Dj=deterministic jitter; Rj=random jitter; DCD=duty cycle distortion; BUJ=bounded uncorrelated jitter; pp=peak-to-peak]
- The validation methodology for these parameters will be covered in the future.
- The mode registers for the Duty Cycle Adjuster are MR43 and MR44. The mode registers for the Per Pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \leq x \leq 7$. The mode registers for the Per Pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \leq y \leq 7$.
- Spread spectrum clocking (SSC) must be disabled while running the Tx DQS jitter test.
- These parameters are tested using the continuous clock pattern, which is sent out from the device without the need for sending out continuous MRR commands. MR25 OP[3] is set to 1 to enable this feature.
- These parameters are tested on the CTC2 card only.

Table 347: Tx DQ Jitter Parameters for DDR5 3200-4800

Parameter	Symbol	3200-4800		Unit	Notes
		MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	$t_{TX\_DQ\_1UI\_Rj\_NoBUJ}$	-	$t_{CK\_1UI\_Rj\_noBUJ} + 0.002$	UI (RMS)	1,2,3,5,6,7
Dj pp value of 1-UI jitter without BUJ	$t_{TX\_DQ\_1UI\_Dj\_NoBUJ}$	-	0.150	UI	3,4
Rj RMS value of N-UI jitter without BUJ, where N = 2,3	$t_{TX\_DQ\_NUI\_Rj\_NoBUJ}$	-	$t_{CK\_NU\_Rj\_noBUJ} + 0.002$	UI (RMS)	2,3,5,6,7
Dj pp value of N-UI jitter without BUJ, where N = 2,3	$t_{Tx\_DQ\_NUI\_Dj\_NoBUJ}$	-	0.150	UI	4,5,6
Delay of any data lane relative to strobe lane	t_{TX_DQS2DQ}	-0.100	0.100	UI	3,4,6

Notes: 1. On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending

patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.

2. Rj RMS value of 1-UI jitter without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
3. Delay of any data lane relative to strobe lane, as measured at Tx output.
4. V_{REF} noise level to DQ jitter should be adjusted to minimize DCD.
5. See AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
6. The DQ pins' duty cycle must be adjusted as close to 50% as possible using the Global and Per Pin Duty Cycle Adjuster (MR43-44) feature prior to running the Tx DQS jitter test.
7. The maximum value of $t_{TX\_DQ\_Rj\_1UI\_NoBUJ}$ and $t_{TX\_DQ\_Rj\_NU\_NoBUJ}$ can be 6m UI RMS.

Table 348: Tx DQ Jitter Parameters for DDR5 5200-6400

Parameter	Symbol	5200-5600		6000-6400		Unit	Notes
		MIN	MAX	MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	$t_{TX\_DQ\_1UI\_Rj\_NoBUJ}$	-	$t_{CK\_1UI\_Rj\_noBUJ} + 0.002$	-	$t_{CK\_1UI\_Rj\_NoBUJ} + 0.002$	UI (RMS)	1,2,3,5,6
Dj pp value of 1-UI jitter without BUJ	$t_{TX\_DQ\_1UI\_Dj\_NoBUJ}$	-	0.130	-	0.130	UI	3,5
Rj RMS value of N-UI jitter without BUJ, where N = 2,3	$t_{TX\_DQ\_NUI\_Rj\_NoBUJ}$	-	$t_{CK\_NUI\_Rj\_noBUJ} + 0.002$	-	-	UI (RMS)	2,3,6
Dj pp value of N-UI jitter without BUJ, where N = 2,3	$t_{Tx\_DQ\_NUI\_Dj\_NoBUJ}$	-	0.130	-	-	UI	4,5
Rj RMS of N-UI jitter without BUJ, where N = 2,3,4	$t_{TX\_DQ\_NUI\_Rj\_NoBUJ}$	-	-	-	$t_{CK\_NUI\_Rj\_NoBUJ} + 0.002$	UI (RMS)	
Dj pp value of N-UI jitter without BUJ, where N = 2,3,4	$t_{Tx\_DQ\_NUI\_Dj\_NoBUJ}$	-	-	-	0.130	UI	
Delay of any data lane relative to strobe lane	t_{TX_DQS2DQ}	-0.100	0.100	-0.100	0.100	UI	3

Notes: 1. On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.

2. Rj RMS value of 1-UI jitter without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
3. Delay of any data lane relative to strobe lane, as measured at Tx output.
4. V_{REF} noise level to DQ jitter should be adjusted to minimize DCD.
5. See AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
6. The maximum value of $t_{TX\_DQS\_1UI\_Rj\_NoBUJ}$ and $t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$ can be 6m UI RMS.

Table 349: Tx DQ Jitter Parameters for DDR5 6800-8800

Parameter	Symbol	6800-8800		Unit	Note
		MIN	MAX		
Rj RMS value of 1-UI jitter without BUJ	$t_{TX\_DQ\_1UI\_Rj\_NoBUJ}$	-	0.006	UI (RMS)	1,2,3,5,6
Dj pp value of 1-UI jitter without BUJ	$t_{TX\_DQ\_1UI\_Dj\_NoBUJ}$	-	0.130	UI	3,5
Rj RMS of N-UI jitter without BUJ, where N=2,3,4,5	$t_{TX\_DQ\_NUI\_Rj\_NoBUJ}$	-	0.006	UI (RMS)	
Dj pp N-UI jitter without BUJ, where N=2,3,4,5	$t_{TX\_DQ\_NUI\_Dj\_NoBUJ}$	-	0.130	UI	
Delay of any data lane relative to strobe lane	t_{TX_DQS2DQ}	-0.100	0.100	UI	3

- Notes: 1. On-die noise similar to what occurs with all toggling transmitter and receiver lanes needs to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the crosstalk or BUJ is not significant or can be estimated within tolerable error, even with all transmitter lanes sending patterns. When a socket is present, such as DUT being device component, the contribution of the crosstalk may be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note there may be cases when one of the Dj and Rj specs is met and another violated, in which case the signaling analysis should be run to determine link feasibility.
2. Rj RMS value of 1-UI jitter without BUJ, but with on-die system-like noise present. This extraction is to be done after software correction of DCD.
 3. Delay of any data lane relative to strobe lane, as measured at Tx output.
 4. V_{REF} noise level to DQ jitter should be adjusted to minimize DCD.
 5. See AC and DC Global Definitions section for details on UI, NUI and jitter definitions.
 6. The maximum value of $t_{TX\_DQS\_1UI\_Rj\_NoBUJ}$ and $t_{TX\_DQS\_NUI\_Rj\_NoBUJ}$ can be 6m UI RMS.

Tx DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER=E-9 and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both eye width and height. To support different host receiver (Rx) designs, it is the responsibility of the host to ensure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (MR40:OP[2:0]).

Figure 258: Tx DQ Stressed Eye

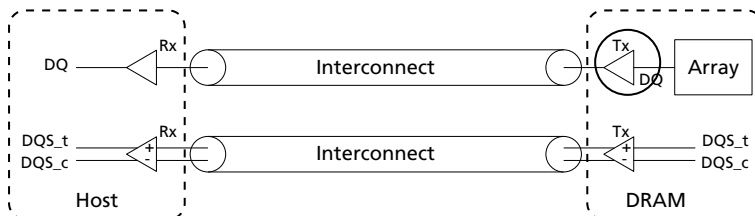


Figure 259: Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 0 UI Skew

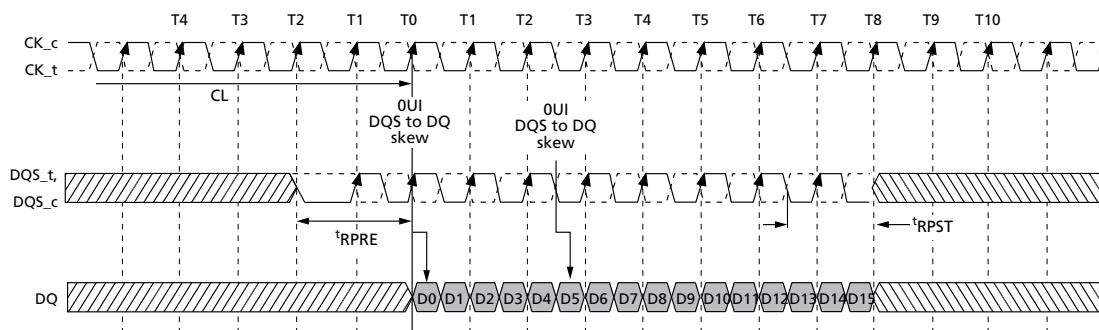
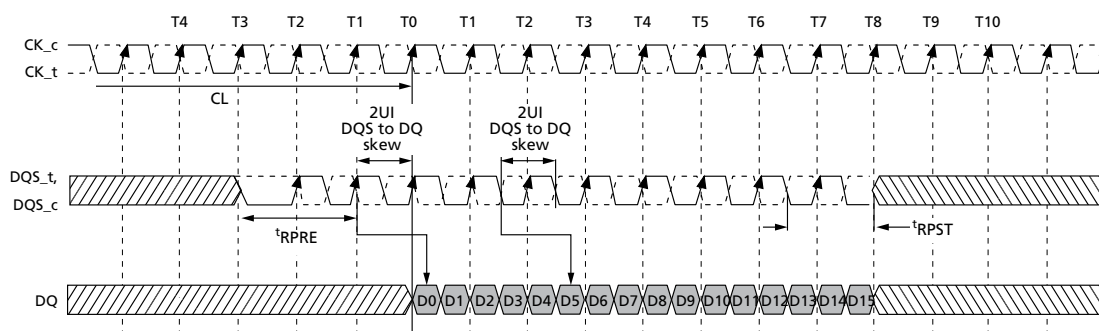


Figure 260: Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 2 UI Skew with Read DQS Offset Timing Set to 1 Clock (2UI)



Tx DQ Stressed Eye Parameters

The following notes apply to all tables:

- EH = Eye Height; EW = Eye Width; BER = Bit Error Rate, SES = Stressed Eye Skew
- Minimum BER E^{-9} and Confidence Level of 99.5% per pin.
- Refer to the minimum Bit Error Rate (BER) requirements for DDR5.
- The validation methodology for these parameters will be covered in the future.
- Mismatch is defined as DQS to DQ mismatch in UI increments.
- The DQ pins' duty cycle must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running the Tx DQS jitter test.
- The mode registers for the Duty Cycle Adjuster are MR43 and MR44. The mode registers for the per-pin DCA of DQS are MR103-MR110. The mode registers for the per-pin DCA of DQLx are MR(133+8x) and MR(134+8x), where $0 \leq x \leq 7$. The mode registers for the per-pin DCA of DQUy are MR(197+8y) and MR(198+8y), where $0 \leq y \leq 7$.
- Spread spectrum clocking (SSC) must be disabled while running these tests.
- These parameters are tested using the continuous PRBS8 LFSR training pattern, which is sent out on all DQ lanes off the device without the need for sending out continuous MRR commands. The MR25 OP[3] is set to 1 to enable this feature.
- These parameters are tested on the CTC2 card only.
- Matched DQS to DQ would require the DQs to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI mismatch would require the DQS to be adjusted 1.5UI. Generally, for XUI mismatch the DQ must be adjusted XUI + 0.5UI to be placed in the center of the eye.

Table 350: Tx DQ Stressed Eye Parameters for DDR5 3200–4800

Parameter	Symbol	3200-4800		Unit	Note
		MIN	MAX		
Eye width specified at the transmitter with a skew between DQ and DQS of 1UI	TXEW_DQ_SES_1UI	0.72	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 2UI	TXEW_DQ_SES_2UI	0.72	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 3UI	TXEW_DQ_SES_3UI	0.72	–	UI	

Table 351: Tx DQ Stressed Eye Parameters for DDR5 5200–6400

Parameter	Symbol	5200-5600		6000-6400		Unit	Note
		MIN	MAX	MIN	MAX		
Eye width specified at the transmitter with a skew between DQ and DQS of 1UI	TXEW_DQ_SES_1UI	0.74	-	0.75	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 2UI	TXEW_DQ_SES_2UI	0.74	-	0.75	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 3UI	TXEW_DQ_SES_3UI	0.74	-	0.75	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 4UI	TXEW_DQ_SES_4UI	0.74	-	0.75	–	UI	1
Eye width specified at the transmitter with a skew between DQ and DQS of 5UI	TXEW_DQ_SES_5UI	-	-	0.75	–	UI	1

Note: 1. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable.

Table 352: Tx DQ Stressed Eye Parameters for DDR5 6800–8800

Parameter	Symbol	6800-8800		Unit	Note
		MIN	MAX		
Eye width specified at the transmitter with a skew between DQ and DQS of 1UI	TXEW_DQ_SES_1UI	0.76	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 2UI	TXEW_DQ_SES_2UI	0.76	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 3UI	TXEW_DQ_SES_3UI	0.76	–	UI	
Eye width specified at the transmitter with a skew between DQ and DQS of 4UI	TXEW_DQ_SES_4UI	0.76	–	UI	1
Eye width specified at the transmitter with a skew between DQ and DQS of 5UI	TXEW_DQ_SES_5UI	0.76	–	UI	1

Note: 1. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable.

Speed Bin Tables by Speed Grade: Standard

DDR5 SDRAM timing is primarily covered by two types of tables: the speed bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The speed bin tables on the following pages list the t_{AA} , t_{RCD} , t_{RP} , t_{RAS} , and t_{RC} limits of a given data rate and speed bin and are applicable to the CL settings in the lower half of the table, provided they are applied in the correct clock range, which is noted. All minimum timing parameters needing translated from the time domain (ns, ps, etc.) to the clock domain (nCK) must be guardbanded by an additional 0.3% according to the rules in the Rounding Definitions and Algorithms section. (Speed bin table notes can be found after the standard DDR5-8800 speed bin table.)

Table 353: DDR5-3200 Speed Bins and Operating Conditions

Speed Bin				DDR5-3200AN		DDR5-3200B		DDR5-3200BN		DDR5-3200C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				24-24-24		26-26-26		26-26-26		28-28-28				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				t _{AA}	15.000	22.222	16.250	22.222	16.250	22.222	17.500	22.222	ns	12
Activate-to-read or write delay time				t _{RCD}	15.000	–	16.250	–	16.250	–	17.500	–	ns	7
Row precharge time				t _{RP}	15.000	–	16.250	–	16.250	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13
ACTIVATE-to-ACTIVATE or REFRESH command period				t _{RC} (t _{RAS} + t _{RP})	47.000	–	48.250	–	48.250	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								nCK	12
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
Supported CL					22,24,26,28		22,26,28		22,26,28		22,28		nCK	12

Table 354: DDR5-3600 Speed Bins and Operating Conditions

Speed Bin				DDR5-3600AN		DDR5-3600B		DDR5-3600BN		DDR5-3600C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				26-26-26		30-30-30		30-30-30		32-32-32				
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data			t _{AA}	14.444	22.222	16.250	22.222	16.666	22.222	17.500	22.222	ns	12	
Activate-to-read or write delay time			t _{RCD}	14.444	–	16.250	–	16.666	–	17.500	–	ns	7	
Row precharge time			t _{RP}	14.444	–	16.250	–	16.666	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period			t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period			t _{RC} (t _{RAS} + t _{RP})	46.444	–	48.250	–	48.666	–	49.500	–	ns	7,8	
CAS WRITE latency			CWL	CL - 2								nCK	12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Min	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3200BN,B	16.666	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
Supported CL					22,24,26,28, 30,32		22,26,28,30,32		22,28,30,32		22,28,32		nCK	12

Table 355: DDR5-4000 Speed Bins and Operating Conditions

Speed Bin				DDR5-4000AN		DDR5-4000B		DDR5-4000BN		DDR5-4000C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				28-28-28		32-32-32		32-32-32		36-35-35				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				^t _{AA}	14.000	22.222	16.000	22.222	16.000	22.222	17.500	22.222	ns	12
Activate-to-read or write delay time				^t _{RCD}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
Row precharge time				^t _{RP}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				^t _{RAS}	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	ns	7,13
ACTIVATE-to-ACTIVATE or REFRESH command period				^t _{RC} (^t _{RAS} + ^t _{RP})	46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								<i>n</i> CK	12
Speed Bin ⁵	^t _{AAmin} (ns) ⁵	^t _{RCDmin} ^t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	14.000	14.000	28	^t _{CK} (AVG)	0.500	<0.555	Reserved						ns	
Supported CL					22,24,26,28,30, 32 36		22,26 28,30,32,36		22,26,28,30,32,36		22,28,32,36		<i>n</i> CK	12

Table 356: DDR5-4400 Speed Bins and Operating Conditions

Speed Bin				DDR5-4400AN			DDR5-4400B			DDR5-4400BN			DDR5-4400C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				32-32-32			36-36-36			36-36-36			40-39-39				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data				t _{AA}	14.545	22.222	16.000	22.222	16.363	22.222	16.363	22.222	17.500	22.222	ns	12	
Activate-to-read or write delay time				t _{RCD}	14.545	–	16.000	–	16.363	–	16.363	–	17.500	–	ns	7	
Row precharge time				t _{RP}	14.545	–	16.000	–	16.363	–	16.363	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period				t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period				t _{RC} (t _{RAS} + t _{RP})	46.545	–	48.000	–	48.363	–	48.363	–	49.500	–	ns	7,8	
CAS WRITE latency				CWL	CL - 2											12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins													
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes	
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9	
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns		
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved					ns			
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved							ns			
3600C	17.777	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns		
3600BN,B	16.666	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved			ns			
3600AN	14.444	14.444	26	t _{CK} (AVG)	Reserved										ns		
4000C	18.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns		
4000BN,B	16.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved					ns			
4000AN	14.000	14.000	28	t _{CK} (AVG)	Reserved										ns		
4400C	18.181	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns		
4400BN,B	16.363	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved			ns			
4400AN	14.545	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved							ns			
Supported CL					22,24,26,28,30,32,36,40			22,26,28,30,32,36, 40			22,28,30,32,36,40			22,28,32,36,40		nCK	12

Table 357: DDR5-4800 Speed Bins and Operating Conditions

Speed Bin				DDR5-4800AN		DDR5-4800B		DDR5-4800BN		DDR5-4800C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				34-34-34		40-39-39		40-40-40		42-42-42				
Parameter		Symbol		Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data		t _{AA}		14.166	22.222	16.000	22.222	16.666	22.222	17.500	22.222	ns	12	
Activate-to-read or write delay time		t _{RCD}		14.166	–	16.000	–	16.666	–	17.500	–	ns	7	
Row precharge time		t _{RP}		14.166	–	16.000	–	16.666	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period		t _{RAS}		32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period		t _{RC} (t _{RAS} + t _{RP})		46.166	–	48.000	–	48.666	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								nCK	12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved					ns		
3600C	17.777	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved					ns		
4000C	18.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	t _{CK} (AVG)	Reserved							ns		
4400C	18.181	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	14.545	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved					ns		
4800C	17.500	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	14.166	14.166	34	t _{CK} (AVG)	0.416	<0.454	Reserved					ns		
Supported CL				22,24,26,28,30, 32,34,36,40,42		22,26,28,30,32,36,40, 42		22,28,30,32,36,40,42		22,28,32,36,40,42		nCK	12	

Table 358: DDR5-5200 Speed Bins and Operating Conditions

Speed Bin				DDR5-5200AN			DDR5-5200B		DDR5-5200BN		DDR5-5200C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP				38-38-38			42-42-42		42-42-42		46-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				^t AA	14.615	22.222	16.000	22.222	16.153	22.222	17.500	22.222	ns	12
Activate-to-read or write delay time				^t RCD	14.615	–	16.000	–	16.153	–	17.500	–	ns	7
Row precharge time				^t RP	14.615	–	16.000	–	16.153	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				^t RAS	32.000	5× ^t REFI (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI (Norm) 9× ^t REFI2 (FGR)	ns	7,13
ACTIVATE-to-ACTIVATE or REFRESH command period				^t RC (^t RAS + ^t RP)	46.615	–	48.000	–	48.153	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								<i>n</i> CK	12
Speed Bin ⁵	^t AAmin (ns) ⁵	^t RCDmin ^t RPmin (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^t CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^t CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^t CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^t CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^t CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^t CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^t CK (AVG)	Reserved								ns	
4000C	18.000	17.500	36	^t CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^t CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	^t CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	^t CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^t CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	^t CK (AVG)	Reserved								ns	
4800C	17.500	17.500	42	^t CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^t CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^t CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	^t CK (AVG)	Reserved								ns	
5200C	17.692	17.692	46	^t CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	^t CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	

Table 358: DDR5-5200 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5200AN		DDR5-5200B		DDR5-5200BN		DDR5-5200C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					38-38-38		42-42-42		42-42-42		46-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46		22,26,28,30,32,36,40,42,46		22,26,28,30,32,36,40,42,46		22,28,32,36,40,42, 46		nCK	12

Table 359: DDR5-5600 Speed Bins and Operating Conditions

Speed Bin				DDR5-5600AN		DDR5-5600B		DDR5-5600BN		DDR5-5600C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				40-40-40		46-45-45		46-46-46		50-49-49				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				t _{AA}	14.285	22.222	16.000	22.222	16.428	22.222	17.500	22.222	ns	12
Activate-to-read or write delay time				t _{RCD}	14.285	–	16.000	–	16.428	–	17.500	–	ns	7
Row precharge time				t _{RP}	14.285	–	16.000	–	16.428	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				t _{RAS}	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	ns	7,13
ACTIVATE-to-ACTIVATE or REFRESH command period				t _{RC} (t _{RAS} + t _{RP})	46.285	–	48.000	–	48.428	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								<i>n</i> CK	12
Speed Bin ⁵	t _{AA} min n (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	t _{CK} (AVG)	Reserved								ns	
4400C	18.181	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	14.545	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	14.166	14.166	34	t _{CK} (AVG)	Reserved								ns	
5200C	17.692	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	

Table 359: DDR5-5600 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5600AN		DDR5-5600B		DDR5-5600BN		DDR5-5600C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					40-40-40		46-45-45		46-46-46		50-49-49			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46,50		22,26,28,30,32,36,40,42,46,50		22,28,30,32,36,40,42,46,50		22,28,32,36,40,42,46,50		nCK	12

Table 360: DDR5-6000 Speed Bins and Operating Conditions

Speed Bin				DDR5-6000AN		DDR5-6000B		DDR5-6000BN		DDR5-6000C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				42-42-42		48-48-48		48-48-48		54-53-53				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				t _{AA}	14.000	22.222	16.000	22.222	16.000	22.222	17.500	22.222	ns	12
Activate-to-read or write delay time				t _{RCD}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
Row precharge time				t _{RP}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				t _{RAS}	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	ns	7,13
ACTIVATE-to-ACTIVATE or REFRESH command period				t _{RC} (t _{RAS} + t _{RP})	46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								<i>n</i> CK	12
Speed Bin ⁵	t _{AA} min (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	14.000	14.000	28	t _{CK} (AVG)	0.500	<0.555	Reserved						ns	
4400C	18.181	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	t _{CK} (AVG)	0.416	<0.454	Reserved						ns	
5200C	17.692	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	

Table 360: DDR5-6000 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6000AN		DDR5-6000B		DDR5-6000BN		DDR5-6000C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					42-42-42		48-48-48		48-48-48		54-53-53			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	Reserved		ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	0.333	<0.357	Reserved						ns	
Supported CL					22,24,26,28,30,32,34,36,38,40,42,46,48,50,54		22,26,28,30,32,36,40,42,46,48,50,54		22,26,28,30,32,36,40,42,46,48,50,54		22,28,32,36,40,42,46,50,54		nCK	12

Table 361: DDR5-6400 Speed Bins and Operating Conditions

Speed Bin				DDR5-6400AN		DDR5-6400B		DDR5-6400BN		DDR5-6400C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				46-46-46		52-52-52		52-52-52		56-56-56				
Parameter		Symbol		Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data		t _{AA}		14.375	22.222	16.000	22.222	16.250	22.222	17.500	22.222	ns	12	
Activate-to-read or write delay time		t _{RCD}		14.375	–	16.000	–	16.250	–	17.500	–	ns	7	
Row precharge time		t _{RP}		14.375	–	16.000	–	16.250	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period		t _{RAS}		32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period		t _{RC} (t _{RAS} + t _{RP})		46.375	–	48.000	–	48.250	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								nCK	12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	t _{CK} (AVG)	Reserved								ns	
4400C	18.181	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	

Table 361: DDR5-6400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6400AN		DDR5-6400B		DDR5-6400BN		DDR5-6400C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					46-46-46		52-52-52		52-52-52		56-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4400BN,B	16.363	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	t _{CK} (AVG)	Reserved								ns	
5200C	17.692	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	Reserved								ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	Reserved								ns	
6400C	17.500	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	

Table 361: DDR5-6400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6400AN		DDR5-6400B		DDR5-6400BN		DDR5-6400C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					46-46-46		52-52-52		52-52-52		56-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
6400AN	14.375	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
Supported CL					22,24,26,28,30, 32,36,38,40,42,46,4 8,50,52,54,56		22,26,28,30,32,36,40,42 ,46,48,50,52,54,56		22,26,28,30,32,36, 40,42,46,50,52, 54,56		22,28,32,36,40,42, 46,50,54,56		<i>n</i> CK	12

Table 362: DDR5-6800 Speed Bins and Operating Conditions

Speed Bin				DDR5-6800AN		DDR5-6800B		DDR5-6800BN		DDR5-6800C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				48-48-48		56-55-55		56-56-56		60-60-60				
Parameter		Symbol		Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data		t [‡] AA		14.117	–	16.000	–	16.470	–	17.500	22.222	ns	12	
Activate-to-read or write delay time		t [‡] RCD		14.117	–	16.000	–	16.470	–	17.500	–	ns	7	
Row precharge time		t [‡] RP		14.117	–	16.000	–	16.470	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period		t [‡] RAS		32.000	5×t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5×t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5×t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5×t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period		t [‡] RC (t [‡] RAS + t [‡] RP)		46.117	–	48.000	–	48.000	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								<i>n</i> CK	12	
Speed Bin ⁵	t [‡] AAmin (ns) ⁵	t [‡] RCDmin t [‡] RPmin (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t [‡] CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t [‡] CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t [‡] CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	t [‡] CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	t [‡] CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t [‡] CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t [‡] CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	t [‡] CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t [‡] CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	t [‡] CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	t [‡] CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	

Table 362: DDR5-6800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6800AN		DDR5-6800B		DDR5-6800BN		DDR5-6800C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					48-48-48		56-55-55		56-56-56		60-60-60			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
4400BN,B	16.363	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	14.545	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	14.166	14.166	34	t _{CK} (AVG)	0.416	<0.454	Reserved						ns	
5200C	17.692	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	Reserved								ns	
6400C	17.500	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	

Table 362: DDR5-6800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6800AN		DDR5-6800B		DDR5-6800BN		DDR5-6800C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					48-48-48		56-55-55		56-56-56		60-60-60			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
6400AN	14.375	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
6800C	17.647	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	16.470	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	14.117	14.117	48	t _{CK} (AVG)	0.294	<0.312	Reserved						ns	
Supported CL					22,24,26,28,30,32,34,36,38,40,42,46,48,50,52,54,56,60		22,26,28,30,32,36,40,42,46,48,50,52,54,56,60		22,28,30,32,36,40,42,46,50,54,56, 60		22,28,32,36,40,42,46,50,54,56,60		<i>n</i> CK	12

Table 363: DDR5-7200 Speed Bins and Operating Conditions

Speed Bin				DDR5-7200AN		DDR5-7200B		DDR5-7200BN		DDR5-7200C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				52-52-52		58-58-58		58-58-58		64-63-63				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				^t AA	14.444	–	16.000	–	16.111	–	17.500	22.222	ns	12
Activate-to-read or write delay time				^t RCD	14.444	–	16.000	–	16.111	–	17.500	–	ns	7
Row precharge time				^t RP	14.444	–	16.000	–	16.111	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				^t RAS	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	ns	7,13
ACTIVATE-to-ACTIVATE or REFRESH command period				^t RC (^t RAS + ^t RP)	46.444	–	48.000	–	48.111	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								<i>n</i> CK	12
Speed Bin ⁵	^t AAmin (ns) ⁵	^t RCDmin ^t RPmin (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^t CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^t CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^t CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^t CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^t CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^t CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^t CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^t CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^t CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	^t CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	^t CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^t CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	^t CK (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	^t CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^t CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^t CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	^t CK (AVG)	Reserved								ns	
5200C	17.692	17.692	46	^t CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	^t CK (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	14.615	14.615	38	^t CK (AVG)	0.384	<0.416	Reserved						ns	

Table 363: DDR5-7200 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-7200AN		DDR5-7200B		DDR5-7200BN		DDR5-7200C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					52-52-52		58-58-58		58-58-58		64-63-63			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	Reserved								ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	Reserved								ns	
6400C	17.500	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	
6400AN	14.375	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
6800C	17.647	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	16.470	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	14.117	14.117	48	t _{CK} (AVG)	0.294	<0.312	Reserved						ns	
7200C	17.077	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	Reserved		ns	
7200AN	14.444	14.444	52	t _{CK} (AVG)	0.277	<0.294	Reserved						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46,48,50,52,54,56,60,64		22,26,28,30,32,36,40,42,46,48,50,52,54,56,58,60,64		22,26,28,30,32,36,40,42,46,50,52,54,56,58,60,64		22,28,32,36,40,42,46,50,54,56,60,64		<i>n</i> CK	12

Table 364: DDR5-7600 Speed Bins and Operating Conditions

Speed Bin				DDR5-7600AN		DDR5-7600B		DDR5-7600BN		DDR5-7600C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				54-54-54		62-61-61		62-62-62		68-67-67				
Parameter		Symbol		Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data		t [‡] AA		14.210	–	16.000	–	16.315	–	17.500	–	ns	12	
Activate-to-read or write delay time		t [‡] RCD		14.210	–	16.000	–	16.315	–	17.500	–	ns	7	
Row precharge time		t [‡] RP		14.210	–	16.000	–	16.315	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period		t [‡] RAS		32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period		t [‡] RC (t [‡] RAS + t [‡] RP)		46.210	–	48.000	–	48.315	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								nCK	12	
Speed Bin ⁵	t [‡] AAmin (ns) ⁵	t [‡] RCDmin t [‡] RPmin (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t [‡] CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t [‡] CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t [‡] CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	t [‡] CK (AVG)	0.625	0.681	Reserved					ns		
3600C	17.777	17.777	32	t [‡] CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t [‡] CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t [‡] CK (AVG)	0.555	<0.625	Reserved					ns		
4000C	18.000	17.500	36	t [‡] CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t [‡] CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	t [‡] CK (AVG)	Reserved							ns		
4400C	18.181	17.727	40	t [‡] CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	t [‡] CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	t [‡] CK (AVG)	0.454	<0.500	Reserved					ns		
4800C	17.500	17.500	42	t [‡] CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t [‡] CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t [‡] CK (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	14.166	14.166	34	t [‡] CK (AVG)	Reserved							ns		
5200C	17.692	17.692	46	t [‡] CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	t [‡] CK (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	

Table 364: DDR5-7600 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-7600AN		DDR5-7600B		DDR5-7600BN		DDR5-7600C			
CL- <i>n</i> RCD- <i>n</i> RP					54-54-54		62-61-61		62-62-62		68-67-67			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	Reserved								ns	
6400C	17.500	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	Reserved				ns	
6400AN	14.375	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
6800C	17.647	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	16.470	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	14.117	14.117	48	t _{CK} (AVG)	Reserved								ns	
7200C	170777	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	Reserved				ns	
7200AN	14.444	14.444	52	t _{CK} (AVG)	0.277	<0.294	Reserved						ns	
7600C	17.894	17.631	68	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	16.315	16.315	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	Reserved		ns	
7600B	16.315	16.052	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns	
7600AN	14.210	140210	54	t _{CK} (AVG)	0.263	<0.277	Reserved						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46,48,50,52,54,56,60,64,68		22,26,28,30,32,36,40,42,46,48,50,52,54,56,58,60,64,68		22,28,30,32,36,40,42,46,50,54,56,60,64,68		22,28,32,36,40,42,46,50,54,56,60,64, 68		nCK	12

Table 365: DDR5-8000 Speed Bins and Operating Conditions

Speed Bin				DDR5-8000AN		DDR5-8000B		DDR5-8000BN		DDR5-8000C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				56-56-56		64-64-64		64-64-64		70-70-70				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
READ command to first data				^t _{AA}	14.000	–	16.000	–	16.000	–	17.500	–	ns	12
Activate-to-read or write delay time				^t _{RCD}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
Row precharge time				^t _{RP}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7
ACTIVATE-to-PRECHARGE command period				^t _{RAS}	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	32.000	5× ^t _{REFI1} (Norm) 9× ^t _{REFI2} (FGR)	ns	7,13
ACTIVATE-to-ACTIVATE or REFRESH command period				^t _{RC} (^t _{RAS} + ^t _{RP})	46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8
CAS WRITE latency				CWL	CL - 2								<i>n</i> CK	12
Speed Bin ⁵	^t _{AAmin} (ns) ⁵	^t _{RCDmin} ^t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	^t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	^t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	^t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	^t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	^t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	^t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	^t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	^t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	14.000	14.000	28	^t _{CK} (AVG)	0.500	<0.555	Reserved						ns	
4400C	18.181	17.727	40	^t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	^t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	^t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	^t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	^t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	^t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	^t _{CK} (AVG)	0.416	<0.454	Reserved						ns	
5200C	17.692	17.692	46	^t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	^t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	

Table 365: DDR5-8000 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8000AN		DDR5-8000B		DDR5-8000BN		DDR5-8000C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					56-56-56		64-64-64		64-64-64		70-70-70			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	Reserved		ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	0.333	<0.357	Reserved						ns	
6400C	17.500	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	
6400AN	14.375	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
6800C	17.647	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	16.470	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800AN	14.117	14.117	48	t _{CK} (AVG)	0.294	<0.312	Reserved						ns	
7200C	170777	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	Reserved		ns	
7200AN	14.444	14.444	52	t _{CK} (AVG)	0.277	<0.294	Reserved						ns	
7600C	17.894	17.631	68	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	16.315	16.315	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	Reserved		ns	
7600B	16.315	16.052	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	Reserved		ns	
7600AN	14.210	140210	54	t _{CK} (AVG)	0.263	<0.277	Reserved						ns	
8000C	170750	17.500	70	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	16.000	16.000	64	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	Reserved		ns	
8000AN	14.000	14.000	56	t _{CK} (AVG)	0.250	<0.263	Reserved						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46,48,50,52,54,56,58,60,62,64,68,70		22,26,28,30,32,36,40,42,46,48,50,52,54,56,58,60,62,64,68,70		22,26,28,30,32,36,40,42,46,48,50,52,54,56,58,60,62,64,68,70		22,28,32,36,40,42,46,50,54,56,60,64,68,70		<i>n</i> CK	12

Table 366: DDR5-8400 Speed Bins and Operating Conditions

Speed Bin				DDR5-8400AN		DDR5-8400B		DDR5-8400BN		DDR5-8400C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				60-60-60		68-68-68		68-68-68		74-74-74				
Parameter		Symbol		Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data		t [‡] AA		14.285	–	16.000	–	16.190	–	17.500	–	ns	12	
Activate-to-read or write delay time		t [‡] RCD		14.285	–	16.000	–	16.190	–	17.500	–	ns	7	
Row precharge time		t [‡] RP		14.285	–	16.000	–	16.190	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period		t [‡] RAS		32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	32.000	5× t [‡] REFI1 (Norm) 9× t [‡] REFI2 (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period		t [‡] RC (t [‡] RAS + t [‡] RP)		46.285	–	48.000	–	48.190	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								<i>n</i> CK	12	
Speed Bin ⁵	t [‡] AAmin (ns) ⁵	t [‡] RCDmin t [‡] RPmin (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t [‡] CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t [‡] CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t [‡] CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	15.000	15.000	24	t [‡] CK (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	t [‡] CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t [‡] CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t [‡] CK (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	t [‡] CK (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t [‡] CK (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	t [‡] CK (AVG)	Reserved								ns	
4400C	18.181	17.727	40	t [‡] CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	t [‡] CK (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	t [‡] CK (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	t [‡] CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t [‡] CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t [‡] CK (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	14.166	14.166	34	t [‡] CK (AVG)	Reserved								ns	
5200C	17.692	17.692	46	t [‡] CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	t [‡] CK (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	

Table 366: DDR5-8400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8400AN		DDR5-8400B		DDR5-8400BN		DDR5-8400C			
CL- <i>n</i> RCD- <i>n</i> RP					60-60-60		68-68-68		68-68-68		74-74-74			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	Reserved								ns	
6400C	17.500	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	
6400AN	14.375	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
6800C	17.647	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	16.470	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	14.117	14.117	48	t _{CK} (AVG)	Reserved								ns	
7200C	170777	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	Reserved				ns	
7200AN	14.444	14.444	52	t _{CK} (AVG)	0.277	<0.294	Reserved						ns	
7600C	17.894	17.631	68	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	16.315	16.315	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	Reserved		ns	
7600B	16.315	16.052	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns	
7600AN	14.210	140210	54	t _{CK} (AVG)	Reserved								ns	
8000C	170750	17.500	70	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	16.000	16.000	64	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	Reserved				ns	
8000AN	14.000	14.000	56	t _{CK} (AVG)	Reserved								ns	
8400C	17.619	170619	74	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns	
8400BN,B	16.190	16.190	68	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	Reserved		ns	
8400AN	14.285	14.285	60	t _{CK} (AVG)	0.238	<0.250	Reserved						ns	
Supported CL					22,24,26,28,30,32,36,38,40,42,46,48,50,52,54,56,58,60,62,64,68,70,74		22,26,28,30,32,36,40,42,46,48,50,52,54,56,58,60,62,64,68,70,74		22,26,28,30,32,36,40,42,46,50,52,54,56,60,62,64,68,70,74		22,28,32,36,40,42,46,50,54,56,60,64,68,70,74		nCK	12

Table 367: DDR5-8800 Speed Bins and Operating Conditions

Speed Bin				DDR5-8800AN		DDR5-8800B		DDR5-8800BN		DDR5-8800C		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				62-62-62		72-71-71		72-72-72		78-77-77				
Parameter		Symbol		Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data		t _{AA}		14.090	–	16.000	–	16.363	–	17.500	–	ns	12	
Activate-to-read or write delay time		t _{RCD}		14.090	–	16.000	–	16.363	–	17.500	–	ns	7	
Row precharge time		t _{RP}		14.090	–	16.000	–	16.363	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period		t _{RAS}		32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period		t _{RC} (t _{RAS} + t _{RP})		46.090	–	48.000	–	48.363	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								<i>n</i> CK	12	
Speed Bin ⁵	t _{AA} min (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	17.500	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	16.250	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	15.000	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	17.777	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	16.666	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	14.444	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	18.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	16.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	14.000	14.000	28	t _{CK} (AVG)	Reserved								ns	
4400C	18.181	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	16.363	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	14.545	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	17.500	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	16.666	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	16.666	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	14.166	14.166	34	t _{CK} (AVG)	0.416	<0.454	Reserved						ns	
5200C	17.692	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	16.153	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	

Table 367: DDR5-8800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8800AN		DDR5-8800B		DDR5-8800BN		DDR5-8800C		Unit	Notes
CL-nRCD-nRP					62-62-62		72-71-71		72-72-72		78-77-77			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200AN	14.615	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	17.857	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	16.428	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	16.428	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	14.285	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	18.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	16.000	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	14.000	14.000	42	t _{CK} (AVG)	Reserved								ns	
6400C	17.500	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	16.250	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	Reserved				ns	
6400AN	14.375	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
6800C	17.647	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	16.470	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	16.470	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	14.117	14.117	48	t _{CK} (AVG)	0.294	<0.312	Reserved						ns	
7200C	170777	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	16.111	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	Reserved				ns	
7200AN	14.444	14.444	52	t _{CK} (AVG)	0.277	<0.294	Reserved						ns	
7600C	17.894	17.631	68	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	16.315	16.315	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns	
7600B	16.315	16.052	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns	
7600AN	14.210	140210	54	t _{CK} (AVG)	0.263	<0.277	Reserved						ns	
8000C	170750	17.500	70	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	16.000	16.000	64	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	Reserved				ns	
8000AN	14.000	14.000	56	t _{CK} (AVG)	Reserved								ns	
8400C	17.619	170619	74	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns	
8400BN,B	16.190	16.190	68	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	Reserved				ns	
8400AN	14.285	14.285	60	t _{CK} (AVG)	0.238	<0.250	Reserved						ns	
8800C	17.727	17.500	78	t _{CK} (AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	0.227	<0.238	ns	
8800BN	16.363	16.363	72	t _{CK} (AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	Reserved		ns	
8800B	16.363	16.136	72	t _{CK} (AVG)	0.227	<0.238	0.227	<0.238	Reserved				ns	

Table 367: DDR5-8800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8800AN		DDR5-8800B		DDR5-8800BN		DDR5-8800C		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					62-62-62		72-71-71		72-72-72		78-77-77			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
8800AN	14.090	14.090	62	tCK (AVG)	0.227	<0.238	Reserved						ns	
Supported CL					22,24,26,28,30, 32,36,38,40,42,46,48 ,50,52,54,56,58,60,6 2,64,68,70,72,74,78	22,26,28,30,32,36, 40,42,46,48,50,52, 54,56,58,60,62,64, 68,70,72,74,78	22,28,30,32,36, 40,42,46,50, 54,56,60,62,64, 68,70,72,74,78	22,28,32,36,40,42, 46,50,54,56,60,64, 68,70,72,74,78			nCK	12		

Notes: 1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.

- The translation of all timing parameters from ns values to *n*CK values must follow the Rounding Algorithm. The translation of ^tAA to CL follows the explicit combinations listed in the Speed Bin Tables.
- The CL setting and CWL setting result in ^tCK(avg) MIN and ^tCK(avg) MAX requirements. When selecting ^tCK(avg), requirements from the CL setting, as well as requirements from the CWL setting, must be fulfilled.
- Reserved settings are not allowed. User must program a different value.
- This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm and depending on the specific speed bin and down clock frequency combination. When down clocking any "C" speed bin to any slower "C" speed bin, the resulting timings always match the speed bin tables according to the Founding Algorithm. When down clocking any "B" speed bin (and any BN speed bin, if supported) to any slower "B" speed bin, the resulting timings always match the speed bin tables except when down clocking to 3600B, in which case, faster ^tRCD(min) and ^tRP(min) may be allowed according to the Rounding Algorithm.
- 3DS DDR5-3200 AC timing applies if the device operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
- Parameters apply from ^tCK,AVG (MIN) to ^tCK,AVG (MAX) at all standard JEDEC clock period values, as stated in the Speed Bin Tables.
- ^tRC(min) must always be greater than or equal to ^tRAS(min) + ^tRP(min), and when using the appropriate rounding algorithms, *n*RC(min) must always be greater than or equal to *n*RAS(min) + *n*RP(min).
- ^tCK(avg) MAX of 1.010ns (1980 MT/s data rate) is defined to enable for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
- Each speed bin lists the timing requirements that must be supported in order for a given device to be JEDEC-compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.
- Any speed bin also supports functional operation at slower frequencies as shown in the table, which are not subject to production tests but are verified by design/characterization.
- The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the speed bin tables. The CL algorithm calculates supported CAS latencies by rounding the operating frequency up to the next fastest native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting ^tCK(avg) MIN and the bin target timings, the CL algorithm then uses the Rounding Algorithm to calculate the valid CAS latency. Because the DDR5 SDRAM specification only supports even CAS latencies, odd CAS latencies are rounded up to the next even CAS latency. The 1980-2100 MT/s data rate always uses CL22. If ^tAA (corrected) or ^tRCD ^tRP (corrected) are violated, the CL algorithm uses a slower combination of ^tAA (target) and ^tRCD ^tRP (target) to return slower valid CAS latencies. The DDR5 SDRAM can support up to four valid CAS latencies, CL(AN), CL(B), CL(BN), and CL(C) for a given frequency. ^tAA (corrected) and ^tRCD ^tRP (corrected) are calculated by reducing ^tAA(min), ^tRCD(min), and ^tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL must be determined by the memory controller, either by using the Speed bin tables or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information. When read CRC is enabled, CL is increased according to the read CRC latency adder. When CRC is enabled, there is no write CRC latency adder.

13. $t_{RAS}(max)$ must always be less than or equal to $5 \times t_{REFI}(max)$ during normal refresh mode and less than or equal to $9 \times t_{REFI2}(max)$ during fine granularity refresh mode, and when using the rounding algorithms, $nRAS(max)$ must always be less than or equal to $5 \times nRREFI(max)$ during normal refresh mode and less than or equal to $9 \times nREFI2(max)$ during fine granularity refresh mode.

8800 MT/s)

```
// Variables already defined in o
CorrFact = 0.30
ScaledCorrFact = 997
tCKreal = 1011-952, 682-238
tAAmin MONO=14000-17500,
tRCDtRPmin MONO=14000-17500,
tAAcorr = TRUNC(tAAmin*Sca
tRCDtRPcorr = TRUNC(tRCDtRPmin
FUNC[RA(targ)] = TRUNC((targ*Scal
// Round tCKreal down to the next
IF (TRUNC(2000000/(2000*99%))>=TR
tCKstd=TRUNC(2000000/2000)
ELSE IF (TRUNC(2000000/(2000+7*(1
tCKstd=TRUNC(2000000/3200)
ELSE
FOR (DataRateNom=3200; DataRateN
IF (TRUNC(2000000/DataRateN
tCKstd=TRUNC(2000000/(Data
ELSE
tCKstd=RESERVED

// Timing targets (ps) that have
// MONO targets 3DS
BinAN_tAAtarg = 14000 BinA
BinB__tAAtarg = 16000 BinB
BinBN_tAAtarg = 16000 BinB
BinC__tAAtarg = 17500 BinC
BinAN_tRCDtRPtarg = 14000 BinA
BinBN_tRCDtRPtarg = 16000 BinB
BinC__tRCDtRPtarg = 17500 BinC
IF (TRUNC(2000000/3600)>tCKstd)
BinB__tRCDtRPtarg = 16000 BinB
ELSE
// 16250=(2000000/3200)*EVEN(T
```

```
t her areas of the DDR5 SDRAM specification
// (%) Rounding Algorithm correction factor
// Scaled correction factor (1000*(1-0.30%))
// (ps) Real application tCK(AVG) (1980-2100MT/s, 2933-
3DS=16000-20000 // (ps) From Speed Bin Tables and DIMM SPD bytes 30-31
3DS=14000-17500 // (ps) From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
ledCorrFactor/1000) // (ps) Corrected tAA(min) per the Rounding Algorithm rules
*ScaledCorrFactor/1000) // (ps) Corrected tRCD(min), tRP(min) per the Rounding Algorithm
edCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
faster standard frequency (tCK in ps)
UNC(tCKreal)>=TRUNC(2000000/(2000*105%))) // Check for 1980-2100 nominal data rates
// Assign standard 2000 tCK (ps)
33+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200)) // Check for 2933-3200 nominal data rates
// Assign standard 3200 tCK (ps)

eNom<=8400 ; DataRateNom=DataRateNom+400) // Check for >3200- 8800 nominal data rates
om)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
t aRateNom+400)) // Assign standard 3600- 8800 tCK (ps)

// No valid data rate found

been used to define the Speed Bin Tables
t argets
N_tAAtarg = 16000 // tAA target for AN bins
__tAAtarg = 18500 // tAA target for AN, B bins
N_tAAtarg = 18500 // tAA target for AN, B, BN bins
__tAAtarg = 20000 // tAA target for AN, B, BN, C bins
N_tRCDtRPtarg = 14000 // tRCD, tRP target for AN bins
N_tRCDtRPtarg = 16000 // tRCD, tRP target for AN, B, BN bins
__tRCDtRPtarg = 17500 // tRCD, tRP target for AN, B, BN, C bins
// tRCD, tRP target for B bins is frequency dependent
__tRCDtRPtarg = 16000 // tRCD, tRP target for AN, B bins data rates faster than 3600
RUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
```

```

BinB__tRCDtRPtarg = 16250 BinB

// CL Algorithm using variables d
// Up to four valid CL's can be r
// The B and BN bins return the s
// Only even CL's (not odd CL's)
// nRCD, nRP are only even at sta
// nRCD, nRP may be even or odd a
IF (TRUNC(2000000/2000)=tCKStd)
    CL(AN)=22
    CL(B )=22
    CL(BN)=22
    CL(C )=22
ELSE IF (TRUNC(2000000/3200)>=tCK
    IF ((EVEN(RA(BinAN__tAAtar
        CL(AN)=EVEN(RA(BinAN__tAAtar
        CL(B )=EVEN(RA(BinB__tAAtar
        CL(BN)=EVEN(RA(BinBN__tAAtar
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE IF ((EVEN(RA(BinB__tAAtar
        CL(AN)=RESERVED
        CL(B )=EVEN(RA(BinB__tAAtar
        CL(BN)=EVEN(RA(BinBN__tAAtar
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE IF ((EVEN(RA(BinBN__tAAtar
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=EVEN(RA(BinBN__tAAtar
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE IF ((EVEN(RA(BinC__tAAtar
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=RESERVED
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=RESERVED
        CL(C )=RESERVED
    ELSE
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=RESERVED
        CL(C )=RESERVED

__tRCDtRPtarg = 16250 // tRCD, tRP target for AN, B bins for data rates 3600 and slower

efined above
eturned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
ame CL
are valid per the DDR5 SDRAM specification
ndard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
t standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
    // CL22 is the only valid CL for 1980-2100 data rates
    // Valid even CL for AN bins
    // Valid even CL for AN, B, bins
    // Valid even CL for AN, B, BN bins
    // Valid even CL for AN, B, BN, C bins
std>=TRUNC(2000000/ 8800)) // Valid CL for 2933- 8800 data rates
g))*tCKStd>=tAAcorr)AND(EVEN(RA(BinAN__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even only
g))
// Valid even CL for AN bins
g))
// Valid even CL for AN, B bins
g))
// Valid even CL for AN, B, BN bins
g))
// Valid even CL for AN, B, BN, C bins
g))*tCKStd>=tAAcorr)AND( (RA(BinB__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even, odd
// Valid even CL for AN bins
g))
// Valid even CL for AN, B bins
g))
// Valid even CL for AN, B, BN bins
g))
// Valid even CL for AN, B, BN, C bins
g))*tCKStd>=tAAcorr)AND(EVEN(RA(BinBN__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even only
// Valid even CL for AN bins
// Valid even CL for AN, B bins
g))
// Valid even CL for AN, B, BN bins
g))
// Valid even CL for AN, B, BN, C bins
g))*tCKStd>=tAAcorr)AND( (RA(BinC__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even, odd
// Valid even CL for AN bins
// Valid even CL for AN, B bins
// Valid even CL for AN, B, BN bins
g))
// Valid even CL for AN, B, BN, C bins
// No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
// Valid even CL for AN bins
// Valid even CL for AN, B bins
// Valid even CL for AN, B, BN bins
// Valid even CL for AN, B, BN, C bins
// No valid data rate found
// Valid even CL for AN bins
// Valid even CL for AN, B bins
// Valid even CL for AN, B, BN bins
// Valid even CL for AN, B, BN, C bins

```

Speed Bin Tables by Speed Grade: 3DS

DDR5 SDRAM timing is primarily covered by two types of tables: the speed bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The speed bin tables on the following pages list the t_{AA} , t_{RCD} , t_{RP} , t_{RAS} , and t_{RC} limits of a given data rate and speed bin and are applicable to the CL settings in the lower half of the table, provided they are applied in the correct clock range, which is noted. All minimum timing parameters needing translated from the time domain (ns, ps, etc.) to the clock domain (nCK) must be guardbanded by an additional 0.3% according to the rules in the Rounding Definitions and Algorithms section. (3DS speed bin table notes can be found after the 3DS DDR5-8800 speed bin table.)

Table 368: 3DS DDR5-3200 Speed Bins and Operating Conditions

Speed Bin				DDR5-3200AN 3DS		DDR5-3200B 3DS		DDR5-3200BN 3DS		DDR5-3200C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				26-24-24		30-26-26		30-26-26		32-28-28				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.250	22.222	18.750	22.222	18.750	22.222	18.750	22.222	20.000	22.222	ns	12	
Activate-to-read or write delay time	t _{RCD}	15.000	–	16.250	–	16.250	–	16.250	–	17.500	–	ns	7	
Row precharge time	t _{RP}	15.000	–	16.250	–	16.250	–	16.250	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	45.750	–	48.250	–	48.250	–	48.250	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL	CL - 2									<i>n</i> CK	12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
Supported CL					22,26,30,32		22,30,32		22,30,32		22,32		<i>n</i> CK	12

Table 369: 3DS DDR5-3600 Speed Bins and Operating Conditions

Speed Bin				DDR5-3600AN 3DS		DDR5-3600B 3DS		DDR5-3600ABN 3DS		DDR5-3600C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				30-26-26		34-30-30		34-30-30		36-32-32				
Parameter			Symbol	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data			^t AA	16.666	22.222	18.750	22.222	18.888	22.222	20.000	22.222	ns	12	
Activate-to-read or write delay time			^t RCD	14.444	–	16.250	–	16.666	–	17.500	–	ns	7	
Row precharge time			^t RP	14.444	–	16.250	–	16.666	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period			^t RAS	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	32.000	5× ^t REFI1 (Norm) 9× ^t REFI2 (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period			^t RC (^t RAS + ^t RP)	46.444	–	48.250	–	48.666	–	49.500	–	ns	7,8	
CAS WRITE latency			CWL	CL - 2								<i>n</i> CK	12	
Speed Bin ⁵	^t AAmin (ns) ⁵	^t RCDmin ^t RPmin (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	^t CK (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	^t CK (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	^t CK (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	^t CK (AVG)	Reserved								ns	
3600C	20.000	17.777	36	^t CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	^t CK (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	^t CK (AVG)	0.555	<0.625	Reserved						ns	
Supported CL				22,30,32,34,36		22,30,32,34,36		22,32,34,36		22,32,36		<i>n</i> CK	12	

Table 370: 3DS DDR5-4000 Speed Bins and Operating Conditions

Speed Bin				DDR5-4000AN 3DS		DDR5-4000B 3DS		DDR5-4000BN 3DS		DDR5-4000C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				32-28-28		38-32-32		38-32-32		40-35-35				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.000	22.222	18.750	22.222	19.000	22.222	20.000	22.222	20.000	22.222	ns	12	
Activate-to-read or write delay time	t _{RCD}	14.000	–	16.000	–	16.000	–	16.000	–	17.500	–	ns	7	
Row precharge time	t _{RP}	14.000	–	16.000	–	16.000	–	16.000	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.000	–	48.000	–	48.000	–	48.000	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL	CL - 2									nCK	12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	0.500	<0.555	Reserved						ns	
Supported CL					22,26,30, 32,34,36,38,40		22,30,32,34,36,38,40		22,32,36,38,40		22,32,36,40		nCK	12

Table 371: 3DS DDR5-4400 Speed Bins and Operating Conditions

Speed Bin				DDR5-4400AN 3DS		DDR5-4400B 3DS		DDR5-4400BN 3DS		DDR5-4400C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				36-32-32		42-36-36		42-36-36		44-39-39				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.363	22.222	18.750	22.222	19.090	22.222	20.000	22.222	20.000	22.222	ns	12	
Activate-to-read or write delay time	t _{RCD}	14.545	–	16.000	–	16.363	–	17.500	–	17.500	–	ns	7	
Row precharge time	t _{RP}	14.545	–	16.000	–	16.363	–	17.500	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR))	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7	
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.545	–	48.000	–	48.363	–	49.500	–	49.500	–	ns	7,8	
CAS WRITE latency	CWL	CL - 2										<i>n</i> CK	12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins									Unit	Notes
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	Reserved								ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	Reserved				ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	Reserved								ns	
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	Reserved								ns	
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
Supported CL					22,30,32,34,36,38,40,42,44		22,30,32,34,36,38,40,42,44		22,32,36,40,42,44		22,32,36,40,44		<i>n</i> CK	12

Table 372: 3DS DDR5-4800 Speed Bins and Operating Conditions

Speed Bin				DDR5-4800AN 3DS		DDR5-4800B 3DS		DDR5-4800BN 3DS		DDR5-4800C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				40-34-34		46-39-39		46-40-40		48-42-42				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.666	22.222	18.750	22.222	19.166	22.222	20.000	22.222	ns	12			
Activate-to-read or write delay time	t _{RCD}	14.166	–	16.000	–	16.666	–	17.500	–	ns	7			
Row precharge time	t _{RP}	14.166	–	16.000	–	16.666	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7			
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.166	–	48.000	–	48.666	–	49.500	–	ns	7,8			
CAS WRITE latency		CWL	CL - 2									nCK	12	
Speed Bin ⁵	t _{AA} min (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins									Unit	Notes
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	Reserved							ns		
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	Reserved				ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	0.555	<0.625	Reserved					ns		
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	Reserved							ns		
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	Reserved							ns		
4800C	20.000	17.500	48	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	t _{CK} (AVG)	0.416	<0.454	Reserved					ns		

Table 372: 3DS DDR5-4800 Speed Bins and Operating Conditions (Continued)

Speed Bin		DDR5-4800AN 3DS		DDR5-4800B 3DS		DDR5-4800BN 3DS		DDR5-4800C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP		40-34-34		46-39-39		46-40-40		48-42-42			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Supported CL		22,30,32,34,36,38,40,42,44,46,48		22,30,32,34,36,38,40,42,44,46,48		22,32,36,40,44,46, 48		22,32,36,40,44,48		<i>n</i> CK	12

Table 373: 3DS DDR5-5200 Speed Bins and Operating Conditions

Speed Bin				DDR5-5200AN 3DS		DDR5-5200B 3DS		DDR5-5200BN 3DS		DDR5-5200C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				42-38-38		50-42-42		50-42-42		52-46-46				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.153	22.222	18.750	22.222	19.230	22.222	20.000	22.222	20.000	22.222	ns	12	
Activate-to-read or write delay time	t _{RCD}	14.615	–	16.000	–	16.153	–	17.500	–	17.500	–	ns	7	
Row precharge time	t _{RP}	14.615	–	16.000	–	16.153	–	17.500	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5 × t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.615	–	48.000	–	48.153	–	49.500	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								nCK	12	
Speed Bin ⁵	t _{AA} min (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins									Unit	Notes
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	Reserved				ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	Reserved								ns	
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	Reserved								ns	
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	Reserved								ns	
4800C	20.000	17.500	48	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800B	19.166	16.250	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	t _{CK} (AVG)	Reserved								ns	
5200C	20.000	17.692	52	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	

Table 373: 3DS DDR5-5200 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5200AN 3DS		DDR5-5200B 3DS		DDR5-5200BN 3DS		DDR5-5200C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					42-38-38		50-42-42		50-42-42		52-46-46			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200BN,B	19.230	16.153	50	^t CK (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	
5200AN	16.153	14.615	42	^t CK (AVG)	0.384	<0.416	Reserved						ns	
Supported CL					22,26,30,32, 34,36,38,40,42,44,4 6,48,50,52		22,30,32,34,36,38,40,42 ,44,46,48,50,52		22,32,36, 40,44,48,50,52		22,32,36,40,44, 48,52		<i>n</i> CK	12

Table 374: 3DS DDR5-5600 Speed Bins and Operating Conditions

Speed Bin				DDR5-5600AN 3DS		DDR5-5600B 3DS		DDR5-5600BN 3DS		DDR5-5600C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				46-40-40		52-45-45		52-46-46		56-49-49				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.428	22.222	18.571	22.222	18.571	22.222	18.571	22.222	20.000	22.222	ns	12	
Activate-to-read or write delay time	t _{RCD}	14.285	–	16.000	–	16.428	–	16.428	–	17.500	–	ns	7	
Row precharge time	t _{RP}	14.285	–	16.000	–	16.428	–	16.428	–	17.500	–	ns	7	
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7	
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.285	–	48.000	–	48.428	–	48.428	–	49.500	–	ns	7,8	
CAS WRITE latency		CWL		CL - 2								nCK	12	
Speed Bin ⁵	t _{AA} min (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	Reserved								ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	Reserved								ns	
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	Reserved								ns	
4800C	20.000	17.500	48	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	t _{CK} (AVG)	Reserved								ns	
5200C	20.000	17.692	52	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	

Table 374: 3DS DDR5-5600 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-5600AN 3DS		DDR5-5600B 3DS		DDR5-5600BN 3DS		DDR5-5600C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					46-40-40		52-45-45		52-46-46		56-49-49			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200BN,B	19.230	16.153	50	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	16.153	14.615	42	t _{CK} (AVG)	Reserved								ns	
5600C	20.000	17.500	56	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	18.571	16.071	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
Supported CL					22,30,32, 34,36,38,40,42,44,4 6,48,50,52,56		22,30,32,34,36,38,40,42 ,44,46,48,50,52,56		22,32,34,36, 38,40,42,44,46,48, 50,52,56		22,32,36,40,44, 48,52,56		<i>n</i> CK	12

Table 375: 3DS DDR5-6000 Speed Bins and Operating Conditions

Speed Bin				DDR5-6000AN 3DS		DDR5-6000B 3DS		DDR5-6000BN 3DS		DDR5-6000C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				48-42-42		56-48-48		56-48-48		60-53-53				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.000	22.222	18.571	22.222	18.666	22.222	20.000	22.222	ns	12			
Activate-to read or write delay time	t _{RCD}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7			
Row precharge time	t _{RP}	14.000	–	16.000	–	16.000	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13			
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.000	–	48.000	–	48.000	–	49.500	–	ns	7,8			
CAS WRITE latency	CWL	CL - 2									<i>n</i> CK	12		
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.727	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.090	16.363	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	16.363	14.545	32	t _{CK} (AVG)	0.500	<0.555	Reserved						ns	
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	Reserved								ns	
4800C	20.000	17.500	48	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	16.666	14.166	40	t _{CK} (AVG)			Reserved						ns	
5200C	20.000	17.692	52	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	

Table 375: 3DS DDR5-6000 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6000AN 3DS		DDR5-6000B 3DS		DDR5-6000BN 3DS		DDR5-6000C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					48-42-42		56-48-48		56-48-48		60-53-53			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200BN,B	19.230	16.153	50	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	
5200AN	16.153	14.615	42	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	20.000	17.500	56	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	18.571	16.071	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	20.000	17.666	60	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	Reserved		ns	
6000AN	16.600	14.000	48	t _{CK} (AVG)	0.333	<0.357	Reserved						ns	
Supported CL					22,26,30,32, 34,36,38,40,42,44,4 6,48,50,52,56, 60		22,30,32,34,36,38, 40,42,44,46,48,50, 52,56, 60		22,30,32,34,36, 38,40,42,44,46,48, 50,52,56,60		22,32,36,40,44, 48,52,56,60		<i>n</i> CK	12

Table 376: 3DS DDR5-6400 Speed Bins and Operating Conditions

Speed Bin				DDR5-6400AN 3DS		DDR5-6400B 3DS		DDR5-6400BN 3DS		DDR5-6400C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				52-46-46		60-52-52		60-52-52		64-56-56				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.250	22.222	18.571	22.222	18.750	22.222	20.000	22.222	ns	12			
Activate-to read or write delay time	t _{RCD}	14.375	–	16.000	–	16.250	–	17.500	–	ns	7			
Row precharge time	t _{RP}	14.375	–	16.000	–	16.250	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13			
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.375	–	48.000	–	48.250	–	49.500	–	ns	7,8			
CAS WRITE latency	CWL	CL - 2									nCK	12		
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	Reserved								ns	
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	20.000	17.500	48	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	16.666	14.166	40	t _{CK} (AVG)	Reserved								ns	
5200C	20.000	17.692	52	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	

Table 376: 3DS DDR5-6400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6400AN 3DS		DDR5-6400B 3DS		DDR5-6400BN 3DS		DDR5-6400C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					52-46-46		60-52-52		60-52-52		64-56-56			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200BN,B	19.230	16.153	50	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	16.153	14.615	42	t _{CK} (AVG)	Reserved								ns	
5600C	20.000	17.500	56	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	18.571	16.071	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	t _{CK} (AVG)	Reserved								ns	
6000C	20.000	17.666	60	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	16.600	14.000	48	t _{CK} (AVG)	Reserved								ns	
6400C	20.000	17.500	64	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	
6400AN	16.250	14.375	52	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
Supported CL					22,26,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64		22,30,32,34,36,38,40,42,44,46,48,50,52,54,56,60,64		22,30,32,34,36,40,42,46,48,52,56,60,64		22,32,36,40,44,48,52,56,60,64		<i>n</i> CK	12

Table 377: 3DS DDR5-6800 Speed Bins and Operating Conditions

Speed Bin				DDR5-6800AN 3DS		DDR5-6800B 3DS		DDR5-6800BN 3DS		DDR56800C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				56-48-48		64-55-55		64-56-56		68-60-60				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t ^{AA}	16.470	22.222	18.571	22.222	18.823	22.222	20.000	22.222	ns	12			
Activate-to-read or write delay time	t ^{RCD}	14.117	–	16.000	–	16.470	–	17.500	–	ns	7			
Row precharge time	t ^{RP}	14.117	–	16.000	–	16.470	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t ^{RAS}	32.000	5× t ^{REFI1} (Norm) 9× t ^{REFI2} (FGR)	32.000	5× t ^{REFI1} (Norm) 9× t ^{REFI2} (FGR)	32.000	5× t ^{REFI1} (Norm) 9× t ^{REFI2} (FGR)	32.000	5× t ^{REFI1} (Norm) 9× t ^{REFI2} (FGR)	ns	7,13			
ACTIVATE-to-ACTIVATE or REFRESH command period	t ^{RC} (t ^{RAS} + t ^{RP})	46.117	–	48.000	–	48.000	–	49.500	–	ns	7,8			
CAS WRITE latency	CWL	CL - 2									<i>n</i> CK	12		
Speed Bin ⁵	t ^{AAmin} (ns) ⁵	t ^{RCDmin} t ^{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t ^{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t ^{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t ^{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	t ^{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	t ^{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t ^{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	t ^{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	t ^{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t ^{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t ^{CK} (AVG)	Reserved								ns	
4400C	20.000	17.727	44	t ^{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t ^{CK} (AVG)	0.454	<0.500	0.454	<0.500	Reserved				ns	
4400AN	16.363	14.545	36	t ^{CK} (AVG)	Reserved								ns	
4800C	20.000	17.500	48	t ^{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t ^{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	t ^{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	t ^{CK} (AVG)	0.416	<0.454	Reserved						ns	
5200C	20.000	17.692	52	t ^{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	

Table 377: 3DS DDR5-6800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-6800AN 3DS		DDR5-6800B 3DS		DDR5-6800BN 3DS		DDR56800C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					56-48-48		64-55-55		64-56-56		68-60-60			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200BN,B	19.230	16.153	50	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	16.153	14.615	42	t _{CK} (AVG)	Reserved								ns	
5600C	20.000	17.500	56	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	18.571	16.071	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	20.000	17.666	60	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	16.600	14.000	48	t _{CK} (AVG)	Reserved								ns	
6400C	20.000	17.500	64	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	Reserved				ns	
6400AN	16.250	14.375	52	t _{CK} (AVG)	Reserved								ns	
6800AN	20.000	17.647	68	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	18.823	16.176	64	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	16.470	14.117	56	t _{CK} (AVG)	0.294	<0.312	Reserve						ns	
Supported CL					22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68		22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68		22,32,34,36,40,44,46,48,50,52,56,60,64,68		22,32,36,40,44,48,52,56,60,64,68		<i>n</i> CK	

Table 378: 3DS DDR5-7200 Speed Bins and Operating Conditions

Speed Bin				DDR5-7200AN 3DS		DDR5-7200B 3DS		DDR5-7200BN 3DS		DDR57200C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				58-52-52		68-58-58		68-58-58		72-63-63				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.111	22.222	18.571	22.222	18.888	22.222	20.000	22.222	ns	12			
Activate-to read or write delay time	t _{RCD}	14.444	–	16.000	–	16.111	–	17.500	–	ns	7			
Row precharge time	t _{RP}	14.444	–	16.000	–	16.111	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13			
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.444	–	48.000	–	48.111	–	49.500	–	ns	7,8			
CAS WRITE latency	CWL	CL - 2									nCK	12		
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins								Unit	Notes	
				Symbol	Min	Max	Min	Max	Min	Max	Min			Max
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	Reserved								ns	
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	20.000	17.500	48	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	16.666	14.166	40	t _{CK} (AVG)	Reserved								ns	
5200C	20.000	17.692	52	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	

Table 378: 3DS DDR5-7200 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-7200AN 3DS		DDR5-7200B 3DS		DDR5-7200BN 3DS		DDR57200C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					58-52-52		68-58-58		68-58-58		72-63-63			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200BN,B	19.230	16.153	50	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	
5200AN	16.153	14.615	42	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	20.000	17.500	56	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	18.571	16.071	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	t _{CK} (AVG)	Reserved								ns	
6000C	20.000	17.666	60	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	16.600	14.000	48	t _{CK} (AVG)	Reserved								ns	
6400C	20.000	17.500	64	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	Reserved				ns	
6400AN	16.250	14.375	52	t _{CK} (AVG)	Reserved								ns	
6800C	20.000	17.647	68	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800B	18.823	16.176	64	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	16.470	14.117	56	t _{CK} (AVG)	Reserve								ns	
7200C	20.000	17.500	72	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200N,B	18.888	16.111	68	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	Reserved		ns	
7200AN	16.111	14.444	58	t _{CK} (AVG)	0.277	<0.294	Reserved						ns	
Supported CL					22,26,30,32,34,36,38,40,42,44,46,48,50,52,56,58,60,64,68,72		22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72		22,32,34,36,40,42,44,46,48,50,52,56,60,64,68,72		22,32,36,40,44,48,52,56,60,64,68,72		<i>n</i> CK	

Table 379: 3DS DDR5-7600 Speed Bins and Operating Conditions

Speed Bin				DDR5-7600AN 3DS		DDR5-7600B 3DS		DDR5-7600BN 3DS		DDR57600C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				62-54-54		72-61-61		72-62-62		76-67-67				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.315	22.222	18.571	22.222	18.947	22.222	20.000	22.222	ns	12			
Activate-to read or write delay time	t _{RCD}	14.210	–	16.000	–	16.315	–	17.500	–	ns	7			
Row precharge time	t _{RP}	14.210	–	16.000	–	16.315	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13			
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.210	–	48.000	–	48.315	–	49.500	–	ns	7,8			
CAS WRITE latency	CWL	CL - 2									nCK	12		
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	32	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	30	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved				ns	
3200AN	16.250	15.000	26	t _{CK} (AVG)	Reserved								ns	
3600C	20.000	17.777	36	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	34	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	30	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	40	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	38	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved				ns	
4000AN	16.000	14.000	32	t _{CK} (AVG)	Reserved								ns	
4400C	20.000	17.727	44	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	42	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	36	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	20.000	17.500	48	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	46	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved				ns	
4800AN	16.666	14.166	40	t _{CK} (AVG)	Reserved								ns	
5200C	20.000	17.692	52	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	

Table 379: 3DS DDR5-7600 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-7600AN 3DS		DDR5-7600B 3DS		DDR5-7600BN 3DS		DDR57600C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					62-54-54		72-61-61		72-62-62		76-67-67			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200BN,B	19.230	16.153	50	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved				ns	
5200AN	16.153	14.615	42	t _{CK} (AVG)	Reserved								ns	
5600C	20.000	17.500	56	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	18.571	16.071	52	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	46	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	20.000	17.666	60	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	56	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	16.600	14.000	48	t _{CK} (AVG)	Reserved								ns	
6400C	20.000	17.500	64	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	60	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	Reserved				ns	
6400AN	16.250	14.375	52	t _{CK} (AVG)	Reserved								ns	
6800C	20.000	17.647	68	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	64	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	18.823	16.176	64	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	16.470	14.117	56	t _{CK} (AVG)	Reserve								ns	
7200C	20.000	17.500	72	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200N,B	18.888	16.111	68	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	Reserved				ns	
7200AN	16.111	14.444	58	t _{CK} (AVG)	Reserved								ns	
7600C	20.000	17.631	76	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	18.347	16.315	72	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	Reserved		ns	
7600B	18.347	16.052	72	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns	
7600AN	16.315	14.210	62	t _{CK} (AVG)	0.263	<0.277	Reserved						ns	
Supported CL					22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,62,64,68,72,76		22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72,76		22,32,34,36,40,42,44,46,48,50,52,56,60,64,68,72		22,32,36,40,44,48,52,56,60,64,68,72,76		<i>n</i> CK	

Table 380: 3DS DDR5-8000 Speed Bins and Operating Conditions

Speed Bin				DDR5-8000AN 3DS		DDR5-8000B 3DS		DDR5-8000BN 3DS		DDR5-8000C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				64-56-56		74-64-64		74-64-64		80-70-70				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.000	–	18.500	–	18.500	–	20.000	–	22.222	–	ns	12	
Activate-to-read or write delay time	t _{RCD}	14.000	–	16.000	–	16.000	–	17.500	–	–	–	ns	7	
Row precharge time	t _{RP}	14.000	–	16.000	–	16.000	–	17.500	–	–	–	ns	7	
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5×t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5×t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13	
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.000	–	48.000	–	48.000	–	49.500	–	–	–	ns	7,8	
CAS WRITE latency		CWL	CL - 2									nCK	12	
Speed Bin ⁵	t _{AAmin} (ns) ⁵	t _{RCDmin} t _{RPmin} (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins										
				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved						ns	
3600C	20.000	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved						ns	
4000C	20.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	Reserved		ns	
4000AN	16.000	14.000	28	t _{CK} (AVG)	0.500	<0.555	Reserved						ns	
4400C	20.000	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved						ns	
4800C	20.00	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800AN	16.666	14.166	34	t _{CK} (AVG)	0.416	<0.454	Reserved						ns	
5200C	20.000	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	Reserved		ns	

Table 380: 3DS DDR5-8000 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8000AN 3DS		DDR5-8000B 3DS		DDR5-8000BN 3DS		DDR5-8000C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					64-56-56		74-64-64		74-64-64		80-70-70			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
5200AN	16.153	14.615	38	t _{CK} (AVG)	0.384	<0.416	Reserved						ns	
5600C	20.000	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600B	18.571	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns	
5600AN	16.428	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	20.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	Reserved		ns	
6000AN	16.600	14.000	42	t _{CK} (AVG)	0.333	<0.357	Reserved						ns	
6400C	20.000	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns	
6400AN	16.250	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns	
6800C	20.000	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	18.823	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800AN	16.470	14.117	48	t _{CK} (AVG)	0.294	<0.312	Reserved						ns	
7200C	20.000	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns	
7200BN,B	18.888	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	Reserved		ns	
7200AN	16.111	14.444	52	t _{CK} (AVG)	0.277	<0.294	Reserved						ns	
7600C	20.000	17.631	68	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	18.347	16.315	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	Reserved		ns	
7600B	18.347	16.052	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	Reserved		ns	
7600AN	16.315	140210	54	t _{CK} (AVG)	0.263	<0.277	Reserved						ns	
8000C	20.000	17.500	70	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	18.500	16.000	64	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	Reserved		ns	
8000AN	16.000	14.000	56	t _{CK} (AVG)	0.250	<0.263	Reserved						ns	
Supported CL					22,26,30,32,34,36,38,40,42,44,46,48,50,52,56,58,60,62,64,68,72,74,76,80		22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72,74,76,80		22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72,74,76,80		22,32,36,40,44,48,52,56,60,64,68,72,76,80		<i>n</i> CK	

Table 381: 3DS DDR5-8400 Speed Bins and Operating Conditions

Speed Bin				DDR5-8400AN 3DS		DDR5-8400B 3DS		DDR5-8400BN 3DS		DDR5-8400C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				68-60-60		78-68-68		78-68-68		84-74-74				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.190	–	18.500	–	18.571	–	20.000	22.222	ns	12			
Activate-to-read or write delay time	t _{RCD}	14.285	–	16.000	–	16.190	–	17.500	–	ns	7			
Row precharge time	t _{RP}	14.285	–	16.000	–	16.190	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13			
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.285	–	48.000	–	48.190	–	49.500	–	ns	7,8			
CAS WRITE latency	CWL	CL - 2									nCK	12		
Speed Bin ⁵	t _{AA} min (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins								Unit	Notes	
				Symbol	Min	Max	Min	Max	Min	Max	Min			Max
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	Reserved		ns	
3200AN	16.250	15.000	24	t _{CK} (AVG)	0.625	0.681	Reserved					ns		
3600C	20.000	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved					ns		
4000C	20.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved			ns		
4000AN	16.000	14.000	28	t _{CK} (AVG)	Reserved							ns		
4400C	20.000	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved					ns		
4800C	20.000	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved			ns		
4800AN	16.166	14.166	34	t _{CK} (AVG)	Reserved							ns		
5200C	20.000	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved			ns		

Table 381: 3DS DDR5-8400 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8400AN 3DS		DDR5-8400B 3DS		DDR5-8400BN 3DS		DDR5-8400C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP					68-60-60		78-68-68		78-68-68		84-74-74				
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max			
5200AN	16.153	14.615	38	t _{CK} (AVG)	Reserved								ns		
5600C	20.000	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns		
5600BN	18.571	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	Reserved		ns		
5600B	18.571	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns		
5600AN	16.428	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns		
6000C	20.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns		
6000BN,B	18.666	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns		
6000AN	16.600	14.000	42	t _{CK} (AVG)	Reserved								ns		
6400C	20.000	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns		
6400BN,B	18.750	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	Reserved		ns		
6400AN	16.250	14.375	46	t _{CK} (AVG)	0.312	<0.333	Reserved						ns		
6800C	20.000	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns		
6800BN	18.823	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns		
6800B	18.823	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns		
6800AN	16.470	14.117	48	t _{CK} (AVG)	Reserved								ns		
7200C	20.000	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294	ns		
7200BN,B	18.888	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	Reserved				ns		
7200AN	16.111	14.444	52	t _{CK} (AVG)	Reserved								ns		
7600C	20.000	17.631	68	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns		
7600BN	18.347	16.315	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns		
7600B	18.347	16.052	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns		
7600AN	16.315	140210	54	t _{CK} (AVG)	Reserved								ns		
8000C	20.000	17.500	70	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns		
8000BN,B	18.500	16.000	64	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	Reserved				ns		
8000AN	16.000	14.000	56	t _{CK} (AVG)	Reserved								ns		
8400C	20.000	17.619	84	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns		
8400BN,B	18.571	16.190	78	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	Reserved		ns		
8400AN	16.190	14.285	68	t _{CK} (AVG)	0.238	<0.250	Reserved						ns		
Supported CL					22,26,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72,74,76,78,80,84		22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72,74,76,78,80,84			22,30,32,34,36,40,42,44,46,48,52,56,60,64,68,72,76,78,80,84		22,32,36,40,44,48,52,56,60,64,68,72,76,80,84		<i>n</i> CK	

Table 382: 3DS DDR5-8800 Speed Bins and Operating Conditions

Speed Bin				DDR5-8800AN 3DS		DDR5-8800B 3DS		DDR5-8800BN 3DS		DDR5-8800C 3DS		Unit	Notes	
CL- <i>n</i> RCD- <i>n</i> RP				72-62-62		82-71-71		82-72-72		88-76-76				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
READ command to first data	t _{AA}	16.363	–	18.500	–	18.636	–	20.000	22.222	ns	12			
Activate-to-read or write delay time	t _{RCD}	14.090	–	16.000	–	16.363	–	17.500	–	ns	7			
Row precharge time	t _{RP}	14.090	–	16.000	–	16.363	–	17.500	–	ns	7			
ACTIVATE-to-PRECHARGE command period	t _{RAS}	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	32.000	5× t _{REFI1} (Norm) 9× t _{REFI2} (FGR)	ns	7,13			
ACTIVATE-to-ACTIVATE or REFRESH command period	t _{RC} (t _{RAS} + t _{RP})	46.090	–	48.000	–	48.363	–	49.500	–	ns	7,8			
CAS WRITE latency	CWL	CL - 2									nCK	12		
Speed Bin ⁵	t _{AA} min (ns) ⁵	t _{RCD} min t _{RP} min (ns) ⁵	READ CL ¹²	Supported Frequency Down Bins								Unit	Notes	
				Symbol	Min	Max	Min	Max	Min	Max	Min			Max
–	20.952	–	22	t _{CK} (AVG)	0.952	1.010	0.952	1.010	0.952	1.010	0.952	1.010	ns	6,9
3200C	20.000	17.500	28	t _{CK} (AVG)	0.625	0.681	0.625	0.681	0.625	0.681	0.625	0.681	ns	
3200BN,B	18.750	16.250	26	t _{CK} (AVG)	0.625	0.681	0.625	0.681	Reserved			ns		
3200AN	16.250	15.000	24	t _{CK} (AVG)	Reserved							ns		
3600C	20.000	17.777	32	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	0.555	<0.625	ns	
3600BN,B	18.888	16.666	30	t _{CK} (AVG)	0.555	<0.625	0.555	<0.625	0.555	<0.625	Reserved		ns	
3600AN	16.666	14.444	26	t _{CK} (AVG)	0.555	<0.625	Reserved					ns		
4000C	20.000	17.500	36	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	0.500	<0.555	0.500	<0.555	ns	
4000BN,B	19.000	16.000	32	t _{CK} (AVG)	0.500	<0.555	0.500	<0.555	Reserved			ns		
4000AN	16.000	14.000	28	t _{CK} (AVG)	Reserved							ns		
4400C	20.000	17.727	40	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	0.454	<0.500	ns	
4400BN,B	19.090	16.363	36	t _{CK} (AVG)	0.454	<0.500	0.454	<0.500	0.454	<0.500	Reserved		ns	
4400AN	16.363	14.545	32	t _{CK} (AVG)	0.454	<0.500	Reserved					ns		
4800C	20.000	17.500	42	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	0.416	<0.454	ns	
4800BN	19.166	16.666	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	0.416	<0.454	Reserved		ns	
4800B	19.166	16.250	40	t _{CK} (AVG)	0.416	<0.454	0.416	<0.454	Reserved			ns		
4800AN	16.666	14.166	34	t _{CK} (AVG)	Reserved							ns		
5200C	20.000	17.692	46	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	0.384	<0.416	0.384	<0.416	ns	
5200BN,B	19.230	16.153	42	t _{CK} (AVG)	0.384	<0.416	0.384	<0.416	Reserved			ns		

Table 382: 3DS DDR5-8800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8800AN 3DS		DDR5-8800B 3DS		DDR5-8800BN 3DS		DDR5-8800C 3DS			
CL- <i>n</i> RCD- <i>n</i> RP					72-62-62		82-71-71		82-72-72		88-76-76			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
5200AN	16.153	14.615	38	t _{CK} (AVG)	Reserved								ns	
5600C	20.000	17.500	50	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	0.357	<0.384	0.357	<0.384	ns	
5600BN	18.571	16.428	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600B	18.571	16.071	46	t _{CK} (AVG)	0.357	<0.384	0.357	<0.384	Reserved				ns	
5600AN	16.428	14.285	40	t _{CK} (AVG)	0.357	<0.384	Reserved						ns	
6000C	20.000	17.666	54	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	0.333	<0.357	0.333	<0.357	ns	
6000BN,B	18.666	16.000	48	t _{CK} (AVG)	0.333	<0.357	0.333	<0.357	Reserved				ns	
6000AN	16.600	14.000	42	t _{CK} (AVG)	Reserved								ns	
6400C	20.000	17.500	56	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	0.312	<0.333	0.312	<0.333	ns	
6400BN,B	18.750	16.250	52	t _{CK} (AVG)	0.312	<0.333	0.312	<0.333	Reserved				ns	
6400AN	16.250	14.375	46	t _{CK} (AVG)	Reserved								ns	
6800C	20.000	17.647	60	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	0.294	<0.312	ns	
6800BN	18.823	16.470	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	0.294	<0.312	Reserved		ns	
6800B	18.823	16.176	56	t _{CK} (AVG)	0.294	<0.312	0.294	<0.312	Reserved				ns	
6800AN	16.470	14.117	48	t _{CK} (AVG)	0.294	<0.312	Reserved						ns	
7200C	20.000	17.500	64	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	0.277	<0.294	0.277	<0.294		
7200BN,B	18.888	16.111	58	t _{CK} (AVG)	0.277	<0.294	0.277	<0.294	Reserved					
7200AN	16.111	14.444	52	t _{CK} (AVG)	Reserved								ns	
7600C	20.000	17.631	68	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	0.263	<0.277	0.263	<0.277	ns	
7600BN	18.347	16.315	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns	
7600B	18.347	16.052	62	t _{CK} (AVG)	0.263	<0.277	0.263	<0.277	Reserved				ns	
7600AN	16.315	140210	54	t _{CK} (AVG)	Reserved								ns	
8000C	20.000	17.500	70	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	0.250	<0.263	0.250	<0.263	ns	
8000BN,B	18.500	16.000	64	t _{CK} (AVG)	0.250	<0.263	0.250	<0.263	Reserved				ns	
8000AN	16.000	14.000	56	t _{CK} (AVG)	Reserved								ns	
8400C	20.000	17.619	84	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	0.238	<0.250	0.238	<0.250	ns	
8400BN,B	18.571	16.190	78	t _{CK} (AVG)	0.238	<0.250	0.238	<0.250	Reserved				ns	
8400AN	16.190	14.285	68	t _{CK} (AVG)	Reserved								ns	
8800C	20.000	17.500	88	t _{CK} (AVG)	0.227	<0.238	<0.227	<0.238	0.227	<0.238	0.227	<0.238	ns	
8800BN	18.636	16.363	82	t _{CK} (AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	Reserved		ns	
8800B	18.636	16.136	82	t _{CK} (AVG)	0.227	<0.238	0.227	<0.238	0.227	<0.238	Reserved		ns	

Table 382: 3DS DDR5-8800 Speed Bins and Operating Conditions (Continued)

Speed Bin					DDR5-8800AN 3DS		DDR5-8800B 3DS		DDR5-8800BN 3DS		DDR5-8800C 3DS		Unit	Notes
CL- <i>n</i> RCD- <i>n</i> RP					72-62-62		82-71-71		82-72-72		88-76-76			
Parameter				Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
8800AN	16.636	14.090	82	t _{CK} (AVG)	0.227	<0.238	Reserved						ns	
Supported CL					22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72,74,76,78,80,82,84,88	22,30,32,34,36,38,40,42,44,46,48,50,52,56,60,64,68,72,74,76,78,80,82,84,88	22,32,34,36,40,42,44,46,48,52,56,60,64,68,72,76,80,82,84,88	22,32,36,40,44,48,52,56,60,64,68,72,76,80,84,88					nCK	

- Notes:
1. Minimum timing parameters are defined according to the rules in the Rounding Definitions and Algorithms section.
 2. The translation of all timing parameters from ns values to nCK values must follow the Rounding Algorithm. The translation of ^tAA to CL follows the explicit combinations listed in the Speed Bin Tables.
 3. The CL setting and CWL setting result in ^tCK(avg) MIN and ^tCK(avg) MAX requirements. When selecting ^tCK(avg), requirements from the CL setting, as well as requirements from the CWL setting, must be fulfilled.
 4. Reserved settings are not allowed. User must program a different value.
 5. This column shows the intended native speed bin timings to be replaced and supported when down clocking. This column does not necessarily show the actual minimum speed bin timings allowed and supported when down clocking because the timings could be faster according to the Rounding Algorithm and depending on the specific speed bin and down clock frequency combination.
 6. 3DS DDR5-3200 AC timing applies if the device operates slower than the 2933 MT/s data rate. This is not limited to only the Speed Bin Table timings.
 7. Parameters apply from ^tCK,AVG (MIN) to ^tCK,AVG (MAX) at all standard JEDEC clock period values, as stated in the Speed Bin Tables.
 8. ^tRC(min) is always greater than or equal to ^tRAS(min) + ^tRP(min), and when using the appropriate rounding algorithms, nRC(min) is always greater than or equal to nRAS(min) + nRP(min).
 9. ^tCK(avg) MAX of 1.010ns (1980 MT/s data rate) is defined to allow for 1% SSC down-spreading at a data rate of 2000 MT/s according to JESD404-1.
 10. Each speed bin lists the timing requirements that must be supported in order for a given device to be JEDEC-compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.
 11. Any speed bin also supports functional operation at slower frequencies as shown in the table, which are not subject to production tests but are verified by design/characterization.
 12. The CL Algorithm can be used to mathematically determine the valid CAS Latencies listed in the speed bin tables. The CL algorithm calculates supported CAS latencies by rounding the operating frequency up to the next fastest native speed bin (i.e., 3200 MT/s, 3600 MT/s...). Using the resulting ^tCK(avg) MIN and the bin target timings, the CL algorithm then uses the Rounding Algorithm to calculate the valid CAS latency. Because the DDR5 SDRAM specification only supports even CAS latencies, odd CAS latencies are rounded up to the next even CAS latency. The 1980-2100 MT/s data rate always uses CL22. If ^tAA (corrected) or ^tRCD ^tRP (corrected) are violated, the CL algorithm uses a slower combination of ^tAA (target) and ^tRCD ^tRP (target) to return slower valid CAS latencies. The DDR5 SDRAM can support up to four valid CAS latencies, CL(AN), CL(B), CL(BN), and CL(C) for a given frequency. ^tAA (corrected) and ^tRCD ^tRP (corrected) are calculated by reducing ^tAA(min), ^tRCD(min), and ^tRP(min) by the Rounding Algorithm correction factor. The proper setting of CL shall be determined by the memory controller, either by using the Speed Bin tables or by using the CL Algorithm, or by some other means. Refer to the Rounding Definitions and Algorithm section for more information. When Read CRC is enabled, CL is increased according to the Read CRC Latency Adder. When Write CRC is enabled, there is no Write CRC Latency Adder.

13. $t_{RAS}(max)$ must always be less than or equal to $5 \times t_{REFI}(max)$ during normal refresh mode and less than or equal to $9 \times t_{REFI2}(max)$ during fine granularity refresh mode, and when using the rounding algorithms, $nRAS(max)$ must always be less than or equal to $5 \times nREFI(max)$ during normal refresh mode and less than or equal to $9 \times nREFI2(max)$ during fine granularity refresh mode.

8800 MT/s)

```
// Variables already defined in o
CorrFact = 0.30
ScaledCorrFact = 997
tCKreal = 1011-952, 682-238
tAAmin MONO=14000-17500,
tRCDtRPmin MONO=14000-17500,
tAAcorr = TRUNC(tAAmin*Sca
tRCDtRPcorr = TRUNC(tRCDtRPmin
FUNC[RA(targ)] = TRUNC((targ*Scal
// Round tCKreal down to the next
IF (TRUNC(2000000/(2000*99%))>=TR
tCKstd=TRUNC(2000000/2000)
ELSE IF (TRUNC(2000000/(2000+7*(1
tCKstd=TRUNC(2000000/3200)
ELSE
FOR (DataRateNom=3200; DataRateN
IF (TRUNC(2000000/DataRateN
tCKstd=TRUNC(2000000/(DataRateN
ELSE
tCKstd=RESERVED

// Timing targets (ps) that have
// MONO targets 3DS
BinAN_tAAtarg = 14000 BinA
BinB__tAAtarg = 16000 BinB
BinBN_tAAtarg = 16000 BinB
BinC__tAAtarg = 17500 BinC
BinAN_tRCDtRPtarg = 14000 BinA
BinBN_tRCDtRPtarg = 16000 BinB
BinC__tRCDtRPtarg = 17500 BinC
IF (TRUNC(2000000/3600)>tCKstd)
BinB__tRCDtRPtarg = 16000 BinB
ELSE
// 16250=(2000000/3200)*EVEN(T
```

```
t her areas of the DDR5 SDRAM specification
// (%) Rounding Algorithm correction factor
// Scaled correction factor (1000*(1-0.30%))
// (ps) Real application tCK(AVG) (1980-2100MT/s, 2933-
3DS=16000-20000 // (ps) From Speed Bin Tables and DIMM SPD bytes 30-31
3DS=14000-17500 // (ps) From Speed Bin Tables and DIMM SPD bytes 32-33 (tRCD=tRP)
ledCorrFactor/1000) // (ps) Corrected tAA(min) per the Rounding Algorithm rules
*ScaledCorrFactor/1000) // (ps) Corrected tRCD(min), tRP(min) per the Rounding Algorithm
edCorrFact/tCKstd+1000)/1000) // (nCK) Use Rounding Algorithm to convert bin target timing to nCK
faster standard frequency (tCK in ps)
UNC(tCKreal)>=TRUNC(2000000/(2000*105%))) // Check for 1980-2100 nominal data rates
// Assign standard 2000 tCK (ps)
33+1/3)))>=TRUNC(tCKreal)>=TRUNC(2000000/3200)) // Check for 2933-3200 nominal data rates
// Assign standard 3200 tCK (ps)

eNom<=8400 ; DataRateNom=DataRateNom+400) // Check for >3200- 8800 nominal data rates
om)>TRUNC(tCKreal)>=TRUNC(2000000/(DataRateNom+400)))
t aRateNom+400)) // Assign standard 3600- 8800 tCK (ps)

// No valid data rate found

been used to define the Speed Bin Tables
t argets
N_tAAtarg = 16000 // tAA target for AN bins
__tAAtarg = 18500 // tAA target for AN, B bins
N_tAAtarg = 18500 // tAA target for AN, B, BN bins
__tAAtarg = 20000 // tAA target for AN, B, BN, C bins
N_tRCDtRPtarg = 14000 // tRCD, tRP target for AN bins
N_tRCDtRPtarg = 16000 // tRCD, tRP target for AN, B, BN bins
__tRCDtRPtarg = 17500 // tRCD, tRP target for AN, B, BN, C bins
// tRCD, tRP target for B bins is frequency dependent
__tRCDtRPtarg = 16000 // tRCD, tRP target for AN, B bins data rates faster than 3600
RUNC((BinB__tRCDtRPtarg*ScaledCorrFact/(2000000/3200)+1000)/1000))
```



```

BinB__tRCDtRPtarg = 16250 BinB

// CL Algorithm using variables d
// Up to four valid CL's can be r
// The B and BN bins return the s
// Only even CL's (not odd CL's)
// nRCD, nRP are only even at sta
// nRCD, nRP may be even or odd a
IF (TRUNC(2000000/2000)=tCKStd)
    CL(AN)=22
    CL(B )=22
    CL(BN)=22
    CL(C )=22
ELSE IF (TRUNC(2000000/3200)>=tCK
    IF ((EVEN(RA(BinAN__tAAtar
        CL(AN)=EVEN(RA(BinAN__tAAtar
        CL(B )=EVEN(RA(BinB__tAAtar
        CL(BN)=EVEN(RA(BinBN__tAAtar
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE IF ((EVEN(RA(BinB__tAAtar
        CL(AN)=RESERVED
        CL(B )=EVEN(RA(BinB__tAAtar
        CL(BN)=EVEN(RA(BinBN__tAAtar
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE IF ((EVEN(RA(BinBN__tAAtar
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=EVEN(RA(BinBN__tAAtar
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE IF ((EVEN(RA(BinC__tAAtar
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=RESERVED
        CL(C )=EVEN(RA(BinC__tAAtar
    ELSE
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=RESERVED
        CL(C )=RESERVED
    ELSE
        CL(AN)=RESERVED
        CL(B )=RESERVED
        CL(BN)=RESERVED
        CL(C )=RESERVED

__tRCDtRPtarg = 16250 // tRCD, tRP target for AN, B bins for data rates 3600 and slower

efined above
eturned for a specific freq: CL(AN), CL(B), CL(BN), CL(C), depending on tAAmin, tRCDmin, tRPmin
ame CL
are valid per the DDR5 SDRAM specification
ndard native frequencies for the AN, BN bins (can be even or odd at intermediate frequencies)
t standard native frequencies for the B, C bins (can be even or odd at intermediate frequencies)
    // CL22 is the only valid CL for 1980-2100 data rates
    // Valid even CL for AN bins
    // Valid even CL for AN, B, bins
    // Valid even CL for AN, B, BN bins
    // Valid even CL for AN, B, BN, C bins
std>=TRUNC(2000000/ 8800)) // Valid CL for 2933- 8800 data rates
g))*tCKStd>=tAAcorr)AND(EVEN(RA(BinAN__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even only
g))
    // Valid even CL for AN bins
g))
    // Valid even CL for AN, B bins
g))
    // Valid even CL for AN, B, BN bins
g))
    // Valid even CL for AN, B, BN, C bins
g))*tCKStd>=tAAcorr)AND( (RA(BinB__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even, odd
    // Valid even CL for AN bins
g))
    // Valid even CL for AN, B bins
g))
    // Valid even CL for AN, B, BN bins
g))
    // Valid even CL for AN, B, BN, C bins
g))*tCKStd>=tAAcorr)AND(EVEN(RA(BinBN__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even only
    // Valid even CL for AN bins
    // Valid even CL for AN, B bins
g))
    // Valid even CL for AN, B, BN bins
g))
    // Valid even CL for AN, B, BN, C bins
g))*tCKStd>=tAAcorr)AND( (RA(BinC__tRCDtRPtarg))*tCKStd>=tRCDtRPcorr)) // nRCD, nRP even, odd
    // Valid even CL for AN bins
    // Valid even CL for AN, B bins
    // Valid even CL for AN, B, BN bins
    // Valid even CL for AN, B, BN, C bins
g))
    // Valid even CL for AN, B, BN, C bins
    // No valid CL found (tAAmin, tRCDmin, tRPmin are too slow)
    // Valid even CL for AN bins
    // Valid even CL for AN, B bins
    // Valid even CL for AN, B, BN bins
    // Valid even CL for AN, B, BN, C bins
    // No valid data rate found
    // Valid even CL for AN bins
    // Valid even CL for AN, B bins
    // Valid even CL for AN, B, BN bins
    // Valid even CL for AN, B, BN, C bins

```

IDD and IDDQ Parameters and Test Conditions

This section defines IDD, IPP and IDDQ measurement conditions such as test load and patterns. Setup and test load for IDD, IPP and IDDQ measurements are shown in the Measurement Setup and Test Load for IPP, IPP and IDDQ Measurements figure.

The following IDD currents are measured as time-averaged currents with all VDD balls of the device under test tied together. Any IPP or IDDQ current is not included in IDD currents:

IDD0, IDDQ0, IPP0, IDD0F, IDDQ0F, IPP0F, IDD2N, IDDQ2N, IPP2N, IDD2NT, IDDQ2NT, IPP2NT, IDD2P, IDDQ2P, IPP2P, IDD3N, IDDQ3N, IPP3N, IDD3P, IDDQ3P, IPP3P, IDD4R, IDDQ4R, IPP4R, IDD4RC, IDD4W, IDDQ4W, IPP4W, IDD4WC, IDD5F, IDDQ5F, IPP5F, IDD5B, IDDQ5B, IPP5B, IDD5C, IDDQ5C, IPP5C, IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD7, IDDQ7, IPP7, IDD8, IDDQ8, IPP8, IDD9, IDD9Q, IPP9.

IDDQ currents are measured as time-averaged currents with all VDDQ balls of the device under test tied together. Any IDD or IPP current is not included in IDDQ currents.

IPP currents are measured as time-averaged currents with all VPP balls of the device under test tied together. Any IDD or IDDQ current is not included in IPP currents.

Important:IDDQ values cannot be directly used to calculate IO power of the DDR5 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in the Correlation from Simulated Channel IO Power to Actual Channel IO Power Supported by IDDQ Measurement figure.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- 0 and LOW defined as $V_{IN} \leq V_{ILAC,max}$
- 1 and HIGH defined as $V_{IN} \geq V_{IHAC,min}$
- MID-LEVEL is defined as inputs $V_{REF} = 0.75 * V_{DDQ}$
- Timings used for IDD, IPP and IDDQ measurement loop patterns are found in the timing parameter tables
- Basic IDD, IPP and IDDQ measurement conditions are described in the Basic IDD, IPP and IDDQ Measurement Conditions table later in this section
- Detailed IDD, IPP and IDDQ measurement loop patterns are described in the measurement loops tables in the following sections
- IDD measurements are done after properly initializing and training the device. This includes, but is not limited to, setting:
 - TDQS_t disabled in MR5
 - CRC disabled in MR5
 - DM disabled in MR5
 - 1N mode enabled by setting CS assertion duration bit MR2:OP[4]=1b, unless otherwise specified in the IDD, IDDQ, and IPP patterns conditions definitions
- **Important:**The IDD, IPP and IDDQ measurement loop patterns need to be executed at least one time before actual IDD, IPP or IDDQ measurement is started, with the exception of IDD9 which can be measured any time after the device enters MBIST mode.
- T_{CASE} is defined as 0 - 95°C, unless stated in the specific condition definition table below.
- For all IDD, IDDQ, IPP measurement loop timing parameters, refer to the timing parameters defined in the spec to calculate the nCK required.

Figure 261: Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

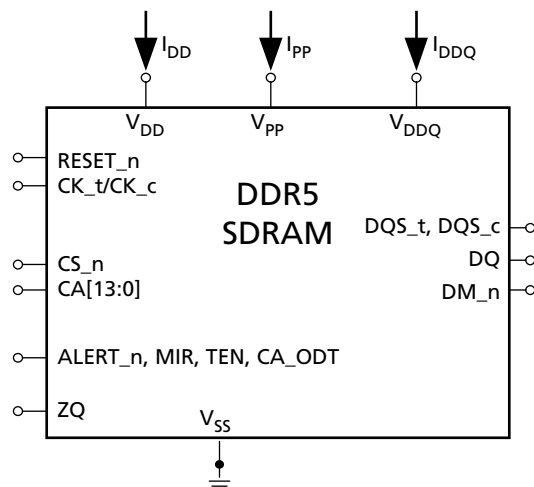


Figure 262: Correlation From Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

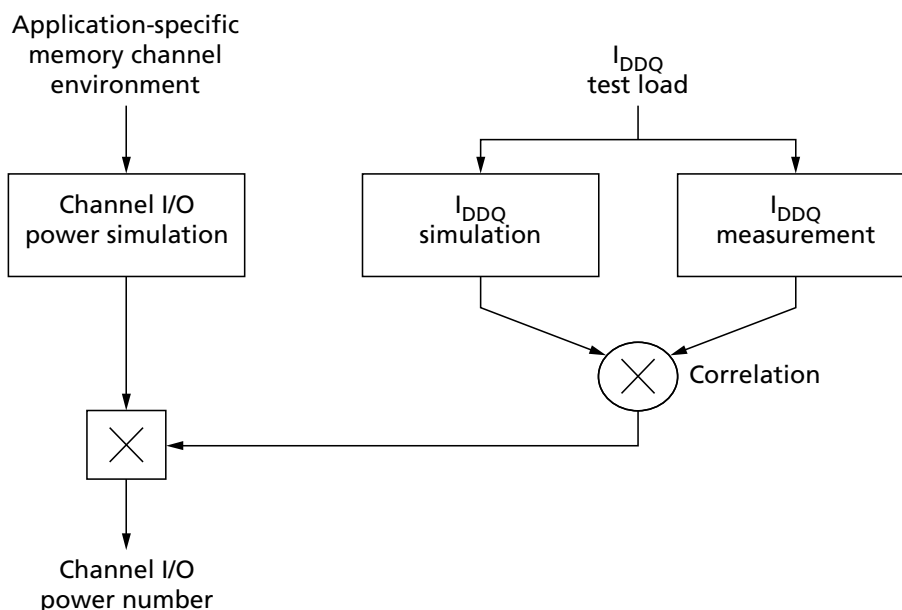


Table 383: Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge IDD Current External clock: On; t_{CK} , t_{RC} , t_{RAS} , t_{RP} , t_{RRD} CA[13:0]: see Timing Parameter Tables; BL: 16 ¹ ; CS_n: HIGH between ACT and PRE; CA Inputs: Partially toggling according to IDD0, IDD0Q, IPP0 table; Data IO: V_{DDQ} ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD0, IDD0Q, IPP0 table); Output Buffer and RTT: Enabled in mode registers ² ; Pattern Details: See IDD0, IDD0Q, IPP0 table
IDDQ0	Operating One Bank Active-Precharge IDDQ Current Same conditions as IDD0, however measuring IDDQ current instead of IDD current
IPP0	Operating One Bank Active-Precharge IPP Current Same conditions as IDD0, however measuring IPP current instead of IDD current

Table 383: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDD0F	Operating Four Bank Active-Precharge IDD Current External clock: On; t_{CK} , t_{RC} , t_{RAS} , t_{RP} , t_{RRD} CA[13:0]: see Timing Parameter Tables; BL: 16 ¹ ; CS_n: HIGH between ACT and PRE; CA Inputs: Partially toggling according to the IDD0F, IDDQ0F, IPP0F table; Data IO: V_{DDQ} ; DM_n: Stable at 1; Bank Activity: Cycling with four banks active at a time: (see the IDD0F, IDDQ0F, IPP0F table); Output Buffer and RTT: Enabled in mode registers ² ; Pattern Details: See the IDD0F, IDDQ0F, IPP0F table
IDDQ0F	Operating Four Bank Active-Precharge IDDQ Current Same conditions with IDD0F, however measuring IDDQ current instead of IDD current
IPP0F	Operating Four Bank Active-Precharge IPP Current Same condition with IDD0F, however measuring IPP current instead of IDD current
IDD2N	Precharge Standby IDD Current External clock: On; t_{CK} : see Timing Parameter Tables; CS_n: stable at 1; CA Inputs: Partially toggling according to the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table; Data IO: V_{DDQ} ; DM_n: Stable at 1; Bank Activity: All banks closed; Output Buffer and RTT: Enabled in mode registers ² ; Pattern Details: See the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table
IDDQ2N	Precharge Standby IDDQ Current Same conditions with IDD2N, however measuring IDDQ current instead of IDD current
IPP2N	Precharge Standby IPP Current Same conditions with IDD2N, however measuring IPP current instead of IDD current
IDD2NT	Precharge Standby Non-Target Command IDD Current External clock: On; t_{CK} ; CS_n: See Timing Parameter Tables; BL: 16 ¹ ; CS_n: HIGH between WRITE NT commands; CS_n, CA Inputs: Partially toggling according to the IDD2NT, IDDQ2NT, IPP2NT table; Data IO: V_{DDQ} ; DM_n: Stable at 1; Bank Activity: All banks closed; Output Buffer and RTT: Enabled in mode registers ² ; Pattern Details: see the IDD2NT, IDDQ2NT, IPP2NT table
IDDQ2NT (optional)	Precharge Standby Non-Target Command IDDQ Current Same conditions with IDD2NT, however measuring IDDQ current instead of IDD current
IPP2NT (optional)	Precharge Standby Non-Target Command IPP Current Same conditions with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	Precharge Power-Down IDD Current Device in Precharge Power-Down with ODT control disabled during Power-Down, External clock: On; t_{CK} see Timing Parameter Tables; CS_n: Stable at 1 after POWER DOWN ENTRY (PDE) command; CA Inputs: CA11=HIGH during PDE command; Data IO: V_{DDQ} ; DM_n: Stable at 1; Bank Activity: All banks closed; Output Buffer and RTT: Enabled in mode registers ² ; Pattern Details: see the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table
IDDQ2P	Precharge Power-Down IDDQ Current Same conditions with IDD2P, however measuring IDDQ current instead of IDD current
IPP2P	Precharge Power-Down IPP Current Same conditions with IDD2P, however measuring IPP current instead of IDD current
IDD3N	Active Standby IDD Current External clock: On; t_{CK} : see Timing Parameter Tables; CS_n: Stable at 1; CA Inputs: Partially toggling according to the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table; Data IO: V_{DDQ} ; DM_n: Stable at 1; Bank Activity: All banks open; Output Buffer and RTT: Enabled in mode registers ² ; Pattern Details: See the IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N table
IDDQ3N	Active Standby IDDQ Current Same conditions with IDD3N, however measuring IDDQ current instead of IDD current
IPP3N	Active Standby IPP Current Same conditions with IDD3N, however measuring IPP current instead of IDD current

Table 383: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDD3P	Active Power-Down IDD Current Device in Active Power-Down with ODT control disabled during Power-Down, External clock: On; t_{CK} : see Timing Parameter Tables; CS_n : Stable at 1 after POWER DOWN ENTRY (PDE) command; CA Inputs : Stable at 1, CA11=HIGH during PDE command; Data IO : V_{DDQ} ; DM_n : Stable at 1; Bank Activity : All banks open; Output Buffer and RTT : Enabled in mode registers ²
IDDQ3P	Active Power-Down IDDQ Current Same conditions with IDD3P, however measuring IDDQ current instead of IDD current
IPP3P	Active Power-Down IPP Current Same conditions with IDD3P, however measuring IPP current instead of IDD current
IDD4R	Operating Burst Read IDD Current External Clock: On; t_{CK} , t_{CCD_S} , CL: see Timing Parameter Tables; BL : 16 ¹ ; CS_n : HIGH between RD; CA Inputs : Partially toggling according to the IDD4R, IDDQ4R, IPP4R table; Data IO : Seamless read data burst with different data between one burst and the next one according to the IDD4R, IDDQ4R, IPP4R table; DM_n : Stable at 1; Bank Activity : All banks open, RD commands cycling through banks (see the IDD4R, IDDQ4R, IPP4R table); Output Buffer and RTT : Enabled in mode registers ² ; Pattern Details : See the IDD4R, IDDQ4R, IPP4R table
IDD4RC	Operating Burst Read IDD Current with Read CRC Read CRC enabled ⁴ , Other conditions : See IDD4R
IDDQ4R	Operating Burst Read IDDQ Current Same conditions with IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	Operating Burst Read IPP Current Same conditions with IDD4R, however measuring IPP current instead of IDD current
IDD4W	Operating Burst Write IDD Current External clock: On; t_{CK} , t_{CCD_S} , CL: see Timing Parameter Tables; BL : 16 ¹ ; CS_n : HIGH between WR; CA Inputs : Partially toggling according to the IDD4W, IDDQ4W, IPP4W table; Data IO : Seamless write data burst with different data between one burst and the next one according to the IDD4W, IDDQ4W, IPP4W table; DM_n : Stable at 1; Bank Activity : All banks open, WR commands cycling through banks (see the IDD4W, IDDQ4W, IPP4W table); Output Buffer and RTT : Enabled in mode registers ² ; Pattern Details : See the IDD4W, IDDQ4W, IPP4W table
IDD4WC	Operating Burst Write IDD Current with Write CRC Write CRC enabled ³ , Other conditions : See IDD4W
IDDQ4W	Operating Burst Write IDDQ Current Same conditions with IDD4W, however measuring IDDQ current instead of IDD current
IPP4W	Operating Burst Write IPP Current Same conditions with IDD4W, however measuring IPP current instead of IDD current
IDD5B	Burst Refresh IDD Current (Normal Refresh Mode) External clock: On; t_{CK} , t_{RFC1} : see Timing Parameter Tables; CS_n : HIGH between REF; CA Inputs : Partially toggling according to the IDD5B, IDDQ5B, IPP5B table; Data IO : V_{DDQ} ; DM_n : Stable at 1; Bank Activity : REF command every t_{RFC1} (see the IDD5B, IDDQ5B, IPP5B table); Output Buffer and RTT : Enabled in mode registers ² ; Pattern Details : See the IDD5B, IDDQ5B, IPP5B table
IDDQ5B	Burst Refresh IDDQ Current (Normal Refresh Mode) Same conditions with IDD5B, however measuring IDDQ current instead of IDD current
IPP5B	Burst Refresh IPP Current (Normal Refresh Mode) Same conditions with IDD5B, however measuring IPP current instead of IDD current
IDD5F	Burst Refresh IDD Current (Fine Granularity Refresh Mode) Same conditions with IDD5B, FGR mode enabled in MR4, $t_{RFC}=t_{RFC2}$, Bank Activity : REF command every t_{RFC2} , Pattern Details : See the IDD5B, IDDQ5B, IPP5B table
IDDQ5F	Burst Refresh IDDQ Current (Fine Granularity Refresh Mode) Same conditions with IDD5F, however measuring IDDQ current instead of IDD current

Table 383: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IPP5F	Burst Refresh IPP Current (Fine Granularity Refresh Mode) Same conditions with IDD5F, however measuring IPP current instead of IDD current
IDD5C	Burst Refresh IDD Current (Same Bank Refresh Mode) External clock: On; t_{CK} , t_{RfCSb} : See Timing Parameter Tables; BL: 16 ¹ ; CS_n: HIGH between REF; CA Inputs: Partially toggling according to the IDD5C, IDDQ5C, IPP5C table; Data IO: V_{DDQ} ; DM_n: Stable at 1; Bank Activity: REF command every t_{RfCSb} (see the IDD5C, IDDQ5C, IPP5C table); Output Buffer and RTT: Enabled in mode registers ² ; FGR mode enabled in MR4. Pattern Details: See the IDD5C, IDDQ5C, IPP5C table.
IDDQ5C	Burst Refresh IDDQ Current (Same Bank Refresh Mode) Same conditions with IDD5C, however measuring IDDQ current instead of IDD current
IPP5C	Burst Refresh IPP Current (Same Bank Refresh Mode) Same conditions with IDD5C, however measuring IPP current instead of IDD current
IDD6N	Self Refresh IDD Current: Normal Temperature Range T_{CASE} : 0-85°C; External clock: Off; CK_t and $CK_{c\#}$: HIGH; t_{CK} , t_{CPDED} : See Timing Parameter Tables; BL: 16 ¹ ; CS_n#: LOW; CA Inputs Data IO: HIGH; DM_n: Stable at 1; Bank Activity: Self-refresh operation; Output Buffer and RTT: Disabled by the DRAM upon entry into self-refresh; Pattern Details: see the IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R table
IDDQ6N	Self Refresh IDDQ Current: Normal Temperature Range Same conditions with IDD6N, however measuring IDDQ current instead of IDD current
IPP6N	Self Refresh IPP Current: Normal Temperature Range Same conditions with IDD6N, however measuring IPP current instead of IDD current
IDD6E	Self Refresh IDD Current: Extended Temperature Range T_{CASE} : 85°C-95°C; External clock: Off; CK_t and $CK_{c\#}$: HIGH; t_{CK} , t_{CPDED} : see Timing Parameter Tables; BL: 16 ¹ ; CS_n#: LOW; CA Inputs, Data IO: HIGH; DM_n: Stable at 1; Bank Activity: Self refresh operation; Output Buffer and RTT: Disabled by the DRAM upon entry into self-refresh; ² ; Pattern Details: see the IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E, IDD6R, IDDQ6R, IPP6R table
IDDQ6E	Self Refresh IDDQ Current: Extended Temperature Range Same conditions with IDD6E, however measuring IDDQ current instead of IDD current
IPP6E	Self Refresh IPP Current: Extended Temperature Range Same conditions with IDD6E, however measuring IPP current instead of IDD current
IDD7	Operating Bank Interleave Read IDD Current External clock: On; t_{CK} , t_{RC} , t_{RAS} , t_{RCD} , t_{RRD_s} , t_{FAW} , t_{CCD_s} , CL: see Timing Parameter Tables; BL: 16 ¹ ; CS_n: HIGH between ACT and RDA; CA Inputs: Partially toggling according to the IDD7, IDDQ7, IPP7 table; Data IO: Read data bursts with different data between one burst and the next one according to the IDD7, IDDQ7, IPP7 table; DM_n: Stable at 1; Bank Activity: Two times interleaved cycling through bank groups (0, 1, ...7) with different addressing, see the IDD7, IDDQ7, IPP7 table; Output Buffer and RTT: Enabled in mode registers ² ; Pattern Details: See the IDD7, IDDQ7, IPP7 table
IDDQ7	Operating Bank Interleave Read IDDQ Current Same conditions with IDD7, however measuring IDDQ current instead of IDD current
IPP7	Operating Bank Interleave Read IPP Current Same conditions with IDD7, however measuring IPP current instead of IDD current
IDD8	Maximum Power Saving Deep Power Down IDD Current External clock: Off; CK_t and $CK_{c\#}$: HIGH; t_{CK} , t_{CPDED} : see Timing Parameter Tables; BL: 16 ¹ ; CS_n: LOW; CA: High; DM_n: Stable at 1; Bank Activity: All banks closed and device in MPSM deep power down mode ⁵ ; Output Buffer and RTT: Enabled in mode registers ² ; Patterns Details: Same as IDD6N table, but MPSM is enabled in mode register
IDDQ8	Maximum Power Saving Deep Power Down IDDQ Current Same conditions with IDD8 however measuring IDDQ current instead of IDD current
IPP8	Maximum Power Saving Deep Power Down IPP Current Same conditions with IDD8 however measuring IDDQ current instead of IDD current

Table 383: Basic IDD, IPP and IDDQ Measurement Conditions (Continued)

Symbol	Description
IDD9 (optional)	MBIST IDD Current Device in MBIST mode; External clock : On; CS_n : Stable at 1 after MBIST entry; CA Inputs : Stable at 1; Data IO : VDDQ; Bank Activity : MBIST operation; Output Buffer and RTT : Enabled in mode registers ²
IDDQ9 (optional)	MBIST IDDQ Current Same condition with IDD9; however, measuring IDDQ current instead of IDD current
IPP9 (optional)	MBIST IPP Current Same condition with IDD9; however, measuring IPP current instead of IDD current

- Notes: 1. Burst Length: BL16 fixed by MR0 OP[1:0]=00b
2. Output buffer enable:
- Set MR5:OP[0] = 0b: Qoff = output buffer enabled
 - Set MR5:OP[2:1] = 00b: pull-up output driver impedance = RZQ/7
 - Set MR5:OP[7:6] = 00b: pull-down output driver impedance = RZQ/7
- 2a. RTT_Nom enable:
- Set MR35 OP[5:3] = 110110b: RTT_NOM_WR = RTT_NOM_RD = RZQ/6
- 2b. RTT_WR enable:
- Set MR34 OP[5:3] = 010b: RTT_WR = RZQ/2
 - CA/CS/CK ODT, DQS_RTT_PARK, and RTT_PARK disable
 - Set MR32 OP[5:0] = 000000b
 - Set MR33 OP[5:0] = 000000b
 - Set MR34 OP[2:0] = 000b
3. WRITE CRC enable: Set MR50 OP[2:1] = 11b
4. Read CRC enable: Set MR50 OP[0] = 1b
5. MPSM Deep Power Down Mode
- Set MR2:OP[3] = 1b if PDA Enumerate ID not equal to 15
 - Set MR2:OP[5] = 1b if PDA Enumerate ID equal to 15

IDD and IDDQ ACTIVE and PRECHARGE Measurement Loops

IDD0, IDD0Q, IPP0

Executes ACTIVE and PRECHARGE commands with tightest timing possible while exercising all bank and bank group addresses. Note 2 applies to entire table.

Table 384: IDD0, IDD0Q, IPP0

Subloop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L	-	0x00000	0x0	0x00	0x0	
			H						
	1	DES	H	Toggling ¹					Repeat sequence to satisfy ^t RAS (MIN), truncate if required
	2	PREpb	L	-		0x0	0x00	0x0	
	3	DES	H	Toggling ¹					Repeat sequence to satisfy ^t RP (MIN), truncate if required
	4	ACT	L	-	0x03FFF	0x0	0x00	0x0	
			H						
	5	DES	H	Toggling ¹					Repeat sequence to satisfy ^t RAS (MIN), truncate if required
1	6	PREpb	L	-		0x0	0x00	0x0	
	7	DES	H	Toggling ¹					Repeat sequence to satisfy ^t RP (MIN), truncate if required
	8-15	Repeat subloop 0, use BG[2:0]=0x1 instead							
	16-23	Repeat subloop 0, use BG[2:0]=0x2 instead							
	24-31	Repeat subloop 0, use BG[2:0]=0x3 instead							
	32-39	Repeat subloop 0, use BG[2:0]=0x4 instead							Skip for x16
	40-47	Repeat subloop 0, use BG[2:0]=0x5 instead							Skip for x16
	48-55	Repeat subloop 0, use BG[2:0]=0x6 instead							Skip for x16
2	56-63	Repeat subloop 0, use BG[2:0]=0x7 instead							Skip for x16
	64-127	Repeat subloops 0-7, use BA[1:0]=0x1 instead							
	128-191	Repeat subloops 0-7, use BA[1:0]=0x2 instead							
	192-255	Repeat subloops 0-7, use BA[1:0]=0x3 instead							
	...	Repeat subloops 0-31 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

- Notes: 1. Utilize DESELECTs between commands while toggling all C/A bits per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD0F, IDDQ0F, IPP0F Pattern

Executes four ACTIVE and PRECHARGE commands per ^tRC time while exercising all bank, bank group, and CID addresses. Note 2 applies to entire table.

Table 385: IDD0F, IDDQ0F, IPP0F

Sub-loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
0	0	ACT	L		0x00000	0x0	0x00	0x0	
			H						
	1	DES	H	Toggling ¹					Repeat to satisfy ^t RRD (MIN) (6 DES to meet 8nCK)
	2	ACT	L		0x00000	0x0	0x01	0x0	
			H						
	3	DES	H	Toggling ¹					Repeat to satisfy ^t RRD (MIN) (6 DES to meet 8nCK)
	4	ACT	L		0x00000	0x0	0x02	0x0	
			H						
	5	DES	H	Toggling ¹					Repeat to satisfy ^t RRD (MIN) (6 DES to meet 8nCK)
	6	ACT	L		0x00000	0x0	0x03	0x0	
			H						
	7	DES	H	Toggling ¹					Repeat to satisfy ^t RAS(MIN) from sequence 0
	8	PREpb	L			0x0	0x00	0x0	
	9	DES	H	Toggling ¹					Repeat for ^t RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^t RAS (MIN)
	10	PREpb	L			0x0	0x01	0x0	
	11	DES	H	Toggling ¹					Repeat for ^t RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^t RAS (MIN)
	12	PREpb	L			0x0	0x02	0x0	
	13	DES	H	Toggling ¹					Repeat for ^t RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^t RAS (MIN)
	14	PREpb	L			0x0	0x03	0x0	
0 (cont)	15	DES	H	Toggling ¹					Repeat for ^t RRD (MIN) (7 DES to meet 8nCK); This allows for next PRE to meet ^t RAS (MIN)
	16	DES	H	Toggling ¹					Repeat for ^t RC (MIN) from sequence 0 first ACTIVATE. This will be zero DESELECTS for 4000 MT/s and slower.
1	17-33	Repeat subloop 0, use row address = 0x03FFF for the ACT instead							
2-3	34-67	Repeat subloop 0-1, use BG[2:0]=0x4,0x5,0x6,0x7 instead of 0x0,0x1,0x2,0x3							Skip for x16
4-7	68-101	Repeat subloops 0-3, use BA[1:0]=0x1 instead							

Table 385: IDD0F, IDDQ0F, IPP0F (Continued)

Sub-loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	BA [1:0]	BG [2:0]	CID [2:0]	Special Instructions
8-11	102-135	Repeat subloops 0-3, use BA[1:0]=0x2 instead							
12-15	136-169	Repeat subloops 0-3, use BA[1:0]=0x3 instead							
...	...	Repeat subloops 0-15 for each 3DS logical rank, if applicable							CID[2:0]=0x1-0x7

Notes: 1. Utilize DESELECTs between commands while toggling all C/A bits per the four-cycle sequence defined in the IDD2N, IDD3N pattern.

2. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N

Executes DESELECT commands while exercising all command/address pins in a predefined pattern.
All notes apply to entire table.

Table 386: IDD2N, IDD3N, IDDQ2N, IDDQ3N, IPP2N, IPP3N

Sequence	Command	CS	C/A [13:0]
0	DES	H	0x0000
1	DES	H	0x3FFF
2	DES	H	0x3FFF
3	DES	H	0x3FFF

Notes: 1. Data is pulled to V_{DDQ}.

2. DQS_t and DQS_c are pulled to V_{DDQ}.

3. Command/address ODT is disabled.

4. Repeat sequences 0-3.

5. For 3DS devices, all logical ranks have these test conditions.

IDD2NT, IDDQ2NT, IPP2NT

Executes non-target WRITE commands simulating rank-to-rank timing while exercising all C/A bits.
Notes 3-6 apply to entire table.

Table 387: IDD2NT, IDDQ2NT, IPP2NT

Sequence	Command	CS_n	C/A [13:0]	Special Instructions
0	WRITE ¹	L	0x002D	All valid C/A inputs to VSS
		L	0x0000	
1	DES	H	Toggling ²	Repeat sequence to meet 1* ^t CCD _S (MIN), truncate if required
2	WRITE ¹	L	0x3FED	All valid C/A inputs to VDDQ
		L	0x3FFF	
3	DES	H	Toggling ²	Repeat sequence to meet 1* ^t CCD _S (MIN), truncate if required

Notes: 1. WRITE with CS_n=L on both cycles indicates a non-target WRITE.

2. Utilize DESELECTs between commands while toggling C/A bits per the four-cycle sequence defined in the IDD2N, IDD3N pattern.

3. Time between non-target WRITES reflect ^tCCD_S (MIN) for one rank.

4. DQ signals are V_{DDQ}.

5. DQS_t, DQS_c are V_{DDQ}.

6. Repeat 0-3.

IDD4R, IDDQ4R, and IPP4R

Executes READ commands with the tightest possible timing while exercising all bank and bank group addresses. Notes 2-10 apply to entire table.

Table 388: IDD4R, IDDQ4R, IPP4R

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	READ	L	-	0x000	0x00	0x0	0x0	Pattern A	All valid inputs = V _{DDQ}
			H							
	1	DES	H	Toggling ¹	-					Repeat sequence to satisfy t _{CCD_S} (MIN), truncate if required
1	2	READ	L	-	0x3F0	0x00	0x1	0x0	Pattern B	All valid inputs = V _{DDQ}
			H							
	3	DES	H	Toggling ¹	-					Repeat sequence to satisfy t _{CCD_S} (MIN), truncate if required
2	4-5	Repeat subloop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat subloop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat subloop 0, use BG[2:0]=0x4 instead								Skip for x16
5	10-11	Repeat subloop 1, use BG[2:0]=0x5 instead								Skip for x16
6	12-13	Repeat subloop 0, use BG[2:0]=0x6 instead								Skip for x16
7	14-15	Repeat subloop 1, use BG[2:0]=0x7 instead								Skip for x16
8	16	READ	L	-	0x3F0	0x00	0x0	0x0	Pattern B	All valid inputs = V _{DDQ}
			H							
	17	DES	H	Toggling ¹						Repeat sequence to satisfy t _{CCD_S} (MIN), truncate if required
9	18	READ	L	-	0x000	0x00	0x1	0x0	Pattern A	All valid inputs = V _{DDQ}
			H							
	19	DES	H	Toggling ¹						Repeat sequence to satisfy t _{CCD_S} (MIN), truncate if required
10	20-21	Repeat subloop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat subloop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat subloop 8, use BG[2:0]=0x4 instead								Skip for x16
13	26-27	Repeat subloop 9, use BG[2:0]=0x5 instead								Skip for x16
14	28-29	Repeat subloop 8, use BG[2:0]=0x6 instead								Skip for x16
15	30-31	Repeat subloop 9, use BG[2:0]=0x7 instead								Skip for x16
16-31	32-33	Repeat subloops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat subloops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat subloops 0-15, use BA[1:0]=0x3 instead								

Table 388: IDD4R, IDDQ4R, IPP4R (Continued)

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
...	...	Repeat subloops 0-63 for each 3DS logical rank, if applicable								CID[2:0] = 0x1-0x7

- Notes: 1. Utilize Deselects between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with auto precharge = HIGH, burst chop = HIGH.
3. Row address is set to 0x0000.
4. Data reflects burst length of 16.
5. Data pattern A for x4: 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0xF, 0x0, 0x0, 0xF, 0x0, 0xF, 0x0, 0xF.
6. Data pattern B for x4: 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0x0, 0xF, 0xF, 0x0, 0xF, 0x0, 0xF, 0x0.
7. Data pattern for x8 each beat will reflect two like nibbles (data pattern A = 0x00, 0xFF, 0xFF...).
8. Data pattern for x16 each beat will reflect two like bytes (data pattern A = 0x0000, 0xFFFF, 0xFFFF...).
9. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.
10. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD4W, IDDQ4W, and IPP4W

Executes WRITE commands with the tightest possible timing while exercising all bank and bank group addresses. Notes 2-7 apply to entire table.

Table 389: IDD4W, IDDQ4W, IPP4W

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	WRITE	L	-	0x000	0x00	0x0	0x0	Pattern A	All valid inputs = V _{DDQ}
			H							
	1	DES	H	Toggling ¹	-					Repeat sequence to satisfy t _{CCD_S_WR} (MIN), truncate if required
1	2	WRITE	L	-	0x3F0	0x00	0x1	0x0	Pattern B	All valid inputs = V _{DDQ}
			H							
	3	DES	H	Toggling ¹	-					Repeat sequence to satisfy t _{CCD_S} (MIN), truncate if required
2	4-5	Repeat subloop 0, use BG[2:0]=0x2 instead								
3	6-7	Repeat subloop 1, use BG[2:0]=0x3 instead								
4	8-9	Repeat subloop 0, use BG[2:0]=0x4 instead								Skip for x16
5	10-11	Repeat subloop 1, use BG[2:0]=0x5 instead								Skip for x16
6	12-13	Repeat subloop 0, use BG[2:0]=0x6 instead								Skip for x16
7	14-15	Repeat subloop 1, use BG[2:0]=0x7 instead								Skip for x16

Table 389: IDD4W, IDDQ4W, IPP4W (Continued)

Subloop	Sequence	Command	CS_n	C/A [13:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
8	16	WRITE	L	-	0x3F0	0x00	0x0	0x0	Pattern B	All valid inputs = V _{DDQ}
			H							
	17	DES	H	Toggling ¹						Repeat sequence to satisfy ^t CCD_S_WR (MIN), truncate if required
9	18	WRITE	L	-	0x000	0x00	0x1	0x0	Pattern A	All valid inputs = V _{DDQ}
			H							
	19	DES	H	Toggling ¹						Repeat sequence to satisfy ^t CCD_S (MIN), truncate if required
10	20-21	Repeat subloop 8, use BG[2:0]=0x2 instead								
11	22-23	Repeat subloop 9, use BG[2:0]=0x3 instead								
12	24-25	Repeat subloop 8, use BG[2:0]=0x4 instead								Skip for x16
13	26-27	Repeat subloop 9, use BG[2:0]=0x5 instead								Skip for x16
14	28-29	Repeat subloop 8, use BG[2:0]=0x6 instead								Skip for x16
15	30-31	Repeat subloop 9, use BG[2:0]=0x7 instead								Skip for x16
16-31	32-33	Repeat subloops 0-15, use BA[1:0]=0x1 instead								
32-47	34-35	Repeat subloops 0-15, use BA[1:0]=0x2 instead								
48-63	36-37	Repeat subloops 0-15, use BA[1:0]=0x3 instead								
...	...	Repeat subloops 0-63 for each 3DS logical rank, if applicable								CID[2:0] = 0x1-0x7

- Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. WRITES performed with auto precharge = HIGH, burst chop = HIGH.
3. Row address is set to 0x0000.
4. Data reflects burst length of 16.
5. Refer to IDD4R measurement loop table for data pattern definition.
6. Where C/A column is not populated, refer to command truth table, column address, BA, BG, and CID for the C/A state.
7. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Executes REFRESH (all banks) commands at minimum ^tRFC1. Notes 3-6 apply to entire table.

Table 390: IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F

Sequence	Command	CS_n	C/A[13:0]	CA[9:8]	CID[2:0]	Special Instructions
0	REFab	L	-	H	0x0	All valid inputs = V _{DDQ}
1	DES	H	Toggling ¹	-	-	Repeat sequence to satisfy ^t RFC (MIN) ² , truncate if required
2	REFab	L	-	H	0x0	All valid inputs = V _{DDQ}
3	DES	H	Toggling ¹	-	-	Repeat sequence to satisfy ^t RFC (MIN) ² , truncate if required

Table 390: IDD5B, IDDQ5B, IPP5B, IDD5F, IDDQ5F, IPP5F (Continued)

Sequence	Command	CS_n	C/A[13:0]	CA[9:8]	CID[2:0]	Special Instructions
...	Repeat sequence 0-3 for each 3DS logical rank, if applicable					CID[2:0] = 0x1-0x7

- Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. For IDD5B, use ^tRFC1 (MIN). For IDD5F, use ^tRFC2 (MIN).
3. DQ signals are V_{DDQ}.
4. For 3DS devices, all non-target logical ranks have I_{DD2N} conditions.
5. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.
6. Must set CA[9:8]=H on REFab commands to indicate 1X refresh rate on devices that support RIR.

IDD5C, IDDQ5C, IPP5C

Executes REFRESH (same bank) commands at minimum ^tRFCsb. All notes apply to entire table.

Table 391: IDD5C, IDDQ5C, IPP5C

Sequence	Command	CS_n	C/A[13:0]	CA[9:8]	BA[1:0]	CID[2:0]	Special Instructions
0	REFsb	L	-	H	0x0	0x0	
1	DES	H	Toggling ¹	-	-	-	Repeat sequence to satisfy ^t RFCsb (MIN), truncate if required
2	REFsb	L	-	H	0x1	0x0	
3	DES	H	Toggling ¹	-	-	-	Repeat sequence to satisfy ^t RFCsb (MIN), truncate if required
4	REFsb	L	-	H	0x2	0x0	
5	DES	H	Toggling ¹	-			Repeat sequence to satisfy ^t RFCsb (MIN), truncate if required
6	REFsb	L	-	H	0x3	0x0	
7	DES	H	Toggling ¹	-			Repeat sequence to satisfy ^t RFCsb (MIN), truncate if required
...	Repeat sequence 0-7 for each 3DS logical rank, if applicable					CID[2:0] = 0x1-0x7	

- Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. DQ signals are V_{DDQ}.
3. For 3DS devices, all non-target logical ranks have I_{DD2N} conditions.
4. Where C/A[13:0] column is not populated, refer to command truth table, CA[9:8], and CID columns for the C/A state.

IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

All notes apply to entire table.

Table 392: IDD6N, IDDQ6N, IPP6N, IDD6E, IDDQ6E, IPP6E

Sequence	Command	Clock	CS_n	C/A[13:0]	Special Instructions
0	SRE	Valid	L	0x3BF7	Clocks must be valid ^t CKLCS (MIN) time
1	DES	Valid	H	0x3FFF	Repeat sequence to satisfy ^t CPDED (MIN), truncate if required
2	All C/A=H	Valid	L	0x3FFF	
3	All C/A=H	CK_t=CK_c=H	L	0x3FFF	Repeat sequence indefinitely

- Notes: 1. Data is pulled to V_{DDQ}.
2. DQS_t and DQS_c are pulled to V_{DDQ}.

3. For 3DS, all banks of all logical ranks mimic the same test condition.

IDD7, IDDQ7, IPP7

Executes ACTIVATE, READ/A commands with tightest timing possible while exercising all bank and bank group addresses. All notes apply to entire table.

Table 393: IDD7, IDDQ7, IPP7

Sub-loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions
0	0	ACT	L	-	0x00000	-	0x0	0x0	0x0	-	
			H								
	1	DES	H	Toggling ¹							Repeat sequence to satisfy ^t RRD_S (MIN) and ^t FAW (MIN), and ^t RCD (MIN). Truncate if needed.
1	2	ACT	L	-	0x03FFF	-	0x0	0x1	0x0	-	
			H								
	3	DES	H	Toggling ¹							Repeat sequence to satisfy ^t RRD_S (MIN) and ^t FAW (MIN), and ^t RCD (MIN). Truncate if needed.
2	4-5	Repeat subloop 0, use BG[2:0]=0x2 instead									
3	6-7	Repeat subloop 1, use BG[2:0]=0x3 instead									
4	8-9	Repeat subloop 0, use BG[2:0]=0x4 instead									Skip for x16
5	10-11	Repeat subloop 1, use BG[2:0]=0x5 instead									Skip for x16
6	12-13	Repeat subloop 0, use BG[2:0]=0x6 instead									Skip for x16
7	14-15	Repeat subloop 1, use BG[2:0]=0x7 instead									Skip for x16
8	16	RDA	L	-	-	0x3F0	0x0	0x0	0x0	Pattern A	
			H								
	17	ACT	L	-	0x00000	-	0x1	0x0	0x0	-	
			H								
	18	DES	H	Toggling ¹							Repeat sequence to satisfy ^t RRD_S (MIN) and ^t FAW (MIN), and ^t RCD (MIN). Truncate if needed.

Table 393: IDD7, IDDQ7, IPP7 (Continued)

Sub-loop	Sequence	Command	CS_n	C/A [13:0]	Row Address [17:0]	Column Address [10:0]	BA [1:0]	BG [2:0]	CID [2:0]	Data Burst (BL=16)	Special Instructions							
9	19	RDA	L	-	-	0x000	0x0	0x0	0x0	Pattern B								
			H															
	20	ACT	L	-	0x03FFF	-	0x1	0x1	0x0	-								
			H															
	21	DES	H	Toggling ¹							Repeat sequence to satisfy ^t RRD_S (MIN) and ^t FAW (MIN), and ^t RCD (MIN). Truncate if needed.							
10	22-24	Repeat subloop 8, use BG[2:0]=0x2 instead																
11	25-27	Repeat subloop 9, use BG[2:0]=0x3 instead																
12	28-30	Repeat subloop 8, use BG[2:0]=0x4 instead									Skip for x16							
13	31-33	Repeat subloop 9, use BG[2:0]=0x5 instead									Skip for x16							
14	34-36	Repeat subloop 8, use BG[2:0]=0x6 instead									Skip for x16							
15	37-39	Repeat subloop 9, use BG[2:0]=0x7 instead									Skip for x16							
16-23	40-64	Repeat subloops 8-15, use BA[1:0]=0x1 for the RDA and BA[1:0]=0x2 for the ACT																
24-31	65-89	Repeat subloops 8-15, use BA[1:0]=0x2 for the RDA and BA[1:0]=0x3 for the ACT																
32-39	90-114	Repeat subloops 8-15, use BA[1:0]=0x3 for the RDA and BA[1:0]=0x0 for the ACT																
...	...	Repeat subloops 0-18 for each 3DS logical rank, if applicable									CID[2:0] = 0x1-0x7							

- Notes: 1. Utilize DESELECTs between commands per the four-cycle sequence defined in the IDD2N, IDD3N pattern.
2. READs performed with auto precharge = LOW, burst chop = HIGH.
3. Data reflects burst length of 16.
4. Refer to IDDR4 measurement loop table for data pattern definition.
5. For 3DS devices, all non-target logical ranks have IDD2N conditions.

IDD Specifications

DDR5 IDD/IDDQ/IPP current specifications are found in the DDR5 Die Revision specific data sheet addendums.

Input/Output Capacitance

Table 394: Silicon Pad I/O Capacitance for SPD DDR5 3200-6400

Parameter	Symbol	3200/3600/4000		4400/4800		5200/5600		6000/6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Input/output capacitance (DQ, DM_n, DQS_t and DQS_c, TDQS_t, TDQS_c)	C _{IO}	0.3	0.9	0.3	0.9	0.3	0.85	0.3	0.8	pF	1,2
Input/output capacitance delta (DQ, DM_n)	C _{DIO}	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,8
Input/output capacitance delta (DQS_t and DQS_c)	C _{DDQS}	-	0.04	-	0.04		0.04		0.04	pF	1,2,4
Input capacitance (CK_t and CK_c)	C _{CK}	0.2	0.7	0.2	0.6	0.2	0.55	0.2	0.5	pF	1,2
Input capacitance delta (CK_t and CK_c)	C _{DCK}	-	0.05	-	0.05		0.05		0.05	pF	1,2,3
Input capacitance (CS_n and CA[13:0] pins only)	C _I	0.2	0.7	0.2	0.6	0.20	C _I option1 0.55 C _I option2 0.5	0.2	0.5	pF	1,2,5, 12
Input capacitance delta (CS_n pins only)	C _{DI_CS}	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,6
Input capacitance delta (CA[13:0] pins only)	C _{DI_CA}	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,7
Input/output capacitance of ALERT	C _{ALERT}	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	pF	1,2
Input/output capacitance of Loopback (LBDQ, LBDQS)	C _{Loopback}	0.3	1.0	0.3	1.0	0.3	1.0	0.3	1.0	pF	1,2
Input capacitance of TEN	C _{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,2,9
Input capacitance of ZQ	C _{ZQ}	-	5	-	5	-	5	-	5	pF	1,2,11
Input capacitance of MIR, CAI, CA_ODT pins	C _{STRAP}	-	10	-	10	-	10	-	10	pF	1,2,10

Notes: 1. This parameter is not subject to production test. This parameter is measured by using vendor-specific measurement methodology.

2. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.

3. Absolute value C_{IO}(CK_t) - C_{IO}(CK_c)

4. Absolute value of C_{IO}(DQS_t) - C_{IO}(DQS_c)

5. C_I applies to CS_n and CA[13:0]

6. C_{DI_CS_n} = C_I(CS_n) - 0.5 × (C_I(CLK_t) + C_I(CLK_c))

7. C_{DI_CA} = C_I(CA) - 0.5 × (C_I(CLK_t) + C_I(CLK_c)).

8. C_{DIO} = C_{IO}(DQ,DM) - Avg(C_{IO}(DQ,DM))

9. TEN pin may be DRAM internally pulled LOW through a weak pull-down resistor to V_{SS}. In this case, C_{TEN} might not be valid and the system must verify TEN signal with vendor-specific information.

10. MIR, CAI, and CA_ODT are strap pins used to configure module or point-to-point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.

11. Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality/accuracy with the max capacitive load is characterized.

12. CI options are incorporated V_{CI}VW in the DRAM CA, CS Parametric Values for DDR5-5200-5600 table.

1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.

2. Rx Mask voltage V_{CI}VW total(MIN) must be centered around V_{cent_CA}(pin mid)

3. Rx differential CA to CK jitter total timing window at the V_{CI}VW voltage levels.

4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.

5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{clVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.

Table 395: Silicon Pad I/O Capacitance for SPD DDR5 6800-8800

Parameter	Symbol	6800/7200		7600/8000		8400/8800		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Input/output capacitance (DQ, DM_n, DQS_t and DQS_c, TDQS_t, TDQS_c)	C_{IO}	0.3	0.8	0.3	0.75	0.3	0.70	pF	1,2
Input/output capacitance delta (DQ, DM_n)	C_{DIO}	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,8
Input/output capacitance delta (DQS_t and DQS_c)	C_{DDQS}		0.04		0.04		0.04	pF	1,2,4
Input capacitance (CK_t and CK_c)	C_{CK}	0.2	0.5	0.2	0.45	0.2	0.40	pF	1,2
Input capacitance delta (CK_t and CK_c)	C_{DCK}		0.05		0.05		0.05	pF	1,2,3
Input capacitance (CS_n and CA[13:0] pins only)	C_I	0.2	0.5	0.2	0.45	0.2	0.40	pF	1,2,5
Input capacitance delta (CS_n pins only)	$C_{DI\_CS\_n}$	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,6
Input capacitance delta (CA[13:0] pins only)	C_{DI_CA}	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,7
Input/output capacitance of ALERT	C_{ALERT}	0.3	1.5	0.3	1.5	0.3	1.5	pF	1,2
Input/output capacitance of Loopback (LBDQ, LBDQS)	$C_{Loopback}$	0.3	1.0	0.3	1.0	0.3	1.0	pF	1,2
Input capacitance of TEN	C_{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,2,9
Input capacitance of ZQ	C_{ZQ}	-	5	-	5	-	5	pF	1,2,11
Input capacitance of MIR, CAI, CA_ODT pins	C_{STRAP}	-	10	-	10	-	10	pF	1,2,10

- Notes: 1. This parameter is not subject to production test. This parameter is measured by using vendor-specific measurement methodology.
2. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
3. Absolute value $C_{IO}(CK\_t) - C_{IO}(CK\_c)$
4. Absolute value of $C_{IO}(DQS\_t) - C_{IO}(DQS\_c)$
5. C_I applies to CS_n and CA[13:0]
6. $C_{DI\_CS\_n} = C_I(CS\_n) - 0.5 \times (C_I(CLK\_t) + C_I(CLK\_c))$
7. $C_{DI\_CA} = C_I(CA) - 0.5 \times (C_I(CLK\_t) + C_I(CLK\_c))$.
8. $C_{DIO} = C_{IO}(DQ,DM) - Avg(C_{IO}DQ,DM))$
9. TEN pin may be DRAM internally pulled LOW through a weak pull-down resistor to V_{SS} . In this case, C_{TEN} might not be valid and the system must verify TEN signal with vendor-specific information.
10. MIR, CAI, and CA_ODT are strap pins used to configure module or point-to-point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
11. Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality/accuracy with the max capacitive load is characterized.

Table 396: Silicon Pad I/O Capacitance for SPD DDR5 3200-6400

Parameter	Symbol	3200/3600/4000		4400/4800		5200/5600		6000/6400		Unit	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Input/output capacitance (DQ, DM_n, DQS_t and DQS_c, TDQS_t, TDQS_c)	C _{IO}	0.6	1.8	0.6	1.8	0.6	1.7	0.6	1.6	pF	1,2
Input/output capacitance delta (DQ, DM_n)	C _{DIO}	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	pF	1,2,9
Input/output capacitance delta (DQS_t and DQS_c)	C _{DDQS}		0.08		0.08		0.08		0.08	pF	1,2,4
Input capacitance (CK_t and CK_c)	C _{CK}	0.4	1.4	0.4	1.2	0.4	1.1	0.4	1.0	pF	1,2
Input capacitance delta (CK_t and CK_c)	C _{DCK}		0.1		0.1		0.1		0.1	pF	1,2,3
Input capacitance (CA[13:0] pins)	C _{I_CA}	0.4	1.4	0.4	1.2	0.4	1.1	0.4	1.0	pF	1,2,5,12
Input capacitance (CS_n pin)	C _{I_CS_n}	0.2	0.7	0.2	0.6	0.2	0.55	0.2	0.5	pF	1,2,6,12
Input capacitance delta (CS_n pins only)	C _{DI_CS_n}	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	pF	1,2,7
Input capacitance delta (CA[13:0] pins only)	C _{DI_CA}	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	pF	1,2,8
Input/output capacitance of ALERT	C _{ALERT}	0.6	3.0	0.6	3.0	0.6	3.0	0.6	3.0	pF	1,2
Input/output capacitance of Loopback (LBDQ, LBDQS)	C _{Loopback}	0.6	2.0	0.6	2.0	0.6	2.0	0.6	2.0	pF	1,2
Input capacitance of ZQ	C _{ZQ}	-	5	-	5	-	5	-	5	pF	1,2,11,13
Input capacitance of MIR, CAI, CA_ODT pins	C _{STRAP}	-	20	-	20	-	20	-	20	pF	1,2,10

- Notes: 1. This parameter is not subject to production test. This parameter is measured by using vendor-specific measurement methodology.
2. This parameter applies to DDP devices only, but does not include RDL layer portion. RDL layer portion is covered in package electrical specification.
3. Absolute value $C_{IO}(CK_t) - C_{IO}(CK_c)$
4. Absolute value of $C_{IO}(DQS_t) - C_{IO}(DQS_c)$
5. C_{I_CA} applies to CA[13:0]
6. $C_{I\_CS\_n}$ applies to CS_npin and CS1_n pin individually.
7. $C_{DI\_CS\_n} = C_I(CS_n) - 0.5 \times (C_I(CLK_t) + C_I(CLK_c))$.
8. $C_{DI\_CA} = C_I(CA) - 0.5 \times (C_I(CLK_t) + C_I(CLK_c))$.
9. $C_{DIO} = C_{IO}(DQ, DM) - \text{Avg}(C_{IO}(DQ, DM))$.
10. TEN pin may be DRAM internally pulled LOW through a weak pull-down resistor to V_{SS}. In this case, C_{TEN} might not be valid and the system must verify TEN signal with vendor-specific information.
11. MIR, CAI, and CA_ODT are strap pins used to configure module or point-to-point use cases depending on power, signal integrity, and termination requirements. No active AC signaling requirements defined for these pins.
12. Maximum external load capacitance on ZQ pin: 25pF. The ZQ functionality/accuracy with the max capacitive load is characterized.
13. C_{I_CA} , $C_{I\_CS\_n}$ options are incorporated V_{clVW} in Table 296: DDR5 3200-4800 Command/Address, CS Parametric Values on page 367 and Table 297: DDR5 5200-6400 Command/Address, CS Parametric Values on page 368.
- CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
 - Rx Mask voltage V_{clVW total(MIN)} must be centered around V_{cent_CA(pin mid)}.
 - Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.

4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{clVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.
1. CA Rx Mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx Mask voltage $V_{clVW\ total(MIN)}$ must be centered around $V_{cent\_CA(pin\ mid)}$.
3. Rx differential CA to CK jitter total timing window at the V_{clVW} voltage levels.
4. Defined over the CA internal V_{REF} range. The Rx Mask at the pin must be within the internal V_{REFCA} (or V_{REFCS}) range, irrespective of the input signal common mode.
5. CA only minimum input pulse width defined at the $V_{cent\_CA(pin\ mid)}$.
6. Input slew rate over $V_{clVW\ Mask}$ centered at $V_{cent\_CA(pin\ mid)}$.
7. V_{IHL_AC} does not have to be met when no transitions are occurring.
14. C_{ZQ} applies to ZQ pin and ZQ1 pin individually.

Table 397: DRAM SDP Package Electrical Specifications (x4/x8) for DDR5 3200-8800

Parameter	Symbol	3200-4800		5200-8800		Unit	Notes
		MIN	MAX	MIN	MAX		
Input/output Zpkg	Zpkg_DQ	45	75	50	75	ohms	1,2,4,5,10
Input/output pkg delay	Tpkg_delay_DQ	10	35	10	32	ps	1,3,4,5
DQS_t, DQS_c Zpkg	Zpkg_DQS	45	75	50	75	ohms	1,2,5,10,12
DQS_t, DQS_c pkg delay	Tpkg_delay_DQS	10	35	10	32	ps	1,3,5,10,12
Delta Zpkg DQS_t, DQS_c	DZpkg_DQS	–	5	–	5	ohms	1,2,5,7,10
Delta delay DQS_t, DQS_c	DTpkg_delay_DQS	–	2	–	2	ps	1,3,5,7,10
Input-CTRL pins Zpkg	Zpkg_CTRL	45	75	45	75	ohms	1,2,5,9,10
Input-CTRL pins pkg delay	Tpkg_delay_CTRL	10	35	10	28	ps	1,3,5,9,10
Input-CMD ADD pins Zpkg	Zpkg_CA	45	75	45	75	ohms	1,2,5,8,10
Input-CMD ADD pins pkg delay	Tpkg_delay_CA	10	35	10	35 (Option 1), 31 (Option 2), 29 (Option 3)	ps	1,3,5,8,10,13
CLK_t and CLK_c Zpkg	Zpkg_CLK	45	75	45	75	ohms	1,2,5,10
CLK_t and CLK_c pkg delay	Tpkg_delay_CLK	10	30	10	25	ps	1,3,5,10
Delta Zpkg CLK_t and CLK_c	DZpkg_delay_CLK	–	5	–	5	ohms	1,2,5,6,10
Delta delay CLK_t and CLK_c	DTpkg_delay_CLK	–	2	–	2	ps	1,3,5,6,10
ALERT Zpkg	Zpkg_ALERT	45	75	45	75	ohms	1,2,5,10
ALERT delay	Tpkg_delay_ALERT	10	60	10	60	ps	1,3,5,10
Loopback Zpkg	Zpkg_Loopback	45	75	45	75	ohms	1,2,5,10,11
Loopback delay	Tpkg_delay_Loopback	10	60	10	60	ps	1,3,5,10,11

- Notes: 1. This parameter is not subject to production test.
2. This parameter is measured by using vendor-specific measurement methodology.
 3. This parameter is measured by using vendor-specific measurement methodology.
 4. Zpkg_DQ and Tpkg_delay_DQ applies to DQ, DM, TDQS_t, and TDQS_c.
 5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here.
 6. Absolute value of $Z_{pkg\_CK\_t} - Z_{pkg\_CK\_c}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_CK\_t} - T_{pkg\_delay\_CK\_c}$ for delay (Tpkg_delay).
 7. Absolute value of $Z_{pkg(DQS\_t)} - Z_{pkg(DQS\_c)}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_DQS\_t} - T_{pkg\_delay\_DQS\_c}$ for delay (Tpkg_delay).
 8. Zpkg_CA and Tpkg_delay_CA applies to CA[13:0].
 9. Zpkg_CTRL and Tpkg_delay_CTRL applies to CS_n.

10. Package implementations must meet specifications if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ and $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12. Z_{pkg_DQS} and $T_{pkg\_delay\_DQS}$ applies to DQS_C, DQS_T, TDQS_T and TDQS_C.
13. T options are incorporated VclVW in the DDR5 5200-6400 Command/Address, CS Parametric Values table.

Table 398: DRAM SDP Package Electrical Specifications (x16) for DDR5 3200-8800

Parameter	Symbol	3200-4800		5200-8800		Unit	Notes
		MIN	MAX	MIN	MAX		
Input/output Z_{pkg}	Z_{pkg_DQ}	45	75	45	75	ohms	1,2,4,5,10
Input/output pkg delay	$T_{pkg\_delay\_DQ}$	10	40	10	38	ps	1,3,4,5,10
DQS_t, DQS_c Z_{pkg}	Z_{pkg_DQS}	45	75	45	75	ohms	1,2,5,10,12
DQS_t, DQS_c pkg delay	$T_{pkg\_delay\_DQS}$	10	40	10	38	ps	1,3,5,10,12
Delta Z_{pkg} DQS_t, DQS_c	DZ_{pkg_DQS}	–	5	–	5	ohms	1,2,5,7,10
Delta delay DQS_t, DQS_c	$DT_{pkg\_delay\_DQS}$	–	2	–	2	ps	1,3,5,7,10
Input-CTRL pins Z_{pkg}	Z_{pkg_CTRL}	45	75	45	75	ohms	1,2,5,9,10
Input-CTRL pins pkg delay	$T_{pkg\_delay\_CTRL}$	10	40	10	40	ps	1,3,5,9,10
Input-CMD ADD pins Z_{pkg}	Z_{pkg_CA}	45	75	45	75	ohms	1,2,5,8,10
Input-CMD ADD pins pkg delay	$T_{pkg\_delay\_CA}$	10	45	10	44	ps	1,3,5,8,10
CLK_t and CLK_c	Z_{pkg_CLK}	45	75	45	75	ohms	1,2,5,10
CLK_t and CLK_c pkg delay	$T_{pkg\_delay\_CLK}$	10	45	10	44	ps	1,3,5,10
Delta Z_{pkg} CLK_t and CLK_c	$DZ_{pkg\_delay\_CLK}$	–	5	–	5	ohms	1,2,5,6,10
Delta delay CLK_t and CLK_c	$DT_{pkg\_delay\_CLK}$	–	2	–	2	ps	1,3,5,6,10
ALERT Z_{pkg}	Z_{pkg_ALERT}	45	75	45	75	ohms	1,2,5,10
ALERT delay	$T_{pkg\_delay\_ALERT}$	10	60	10	60	ps	1,3,5,10
Loopback Z_{pkg}	$Z_{pkg\_Loopback}$	45	75	45	75	ohms	1,2,5,10,11
Loopback delay	$T_{pkg\_delay\_Loopback}$	10	60	10	60	ps	1,3,5,10,11

Notes: 1. This parameter is not subject to production test.

2. This parameter is measured by using vendor-specific measurement methodology.
3. This parameter is measured by using vendor-specific measurement methodology.
4. Z_{pkg_DQ} and $T_{pkg\_delay\_DQ}$ applies to DQ, DMU, and DMI.
5. This parameter applies to monolithic devices only; Stacked/dual-die devices are not covered here.
6. Absolute value of $Z_{pkg\_CK\_t} - Z_{pkg\_CK\_c}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_CK\_t} - T_{pkg\_delay\_CK\_c}$ for delay (T_{pkg_delay}).
7. Absolute value of $Z_{pkg(DQS\_t)} - Z_{pkg(DQS\_c)}$ for impedance (Z) or absolute value of $T_{pkg\_delay\_DQS\_t} - T_{pkg\_delay\_DQS\_c}$ for delay (T_{pkg_delay}).
8. Z_{pkg_CA} and $T_{pkg\_delay\_CA}$ applies to CA[13:0].
9. Z_{pkg_CTRL} and $T_{pkg\_delay\_CTRL}$ apply to CS_n.
10. Package implementations must meet specifications if the designed Z_{pkg} and T_{pkg_delay} fall within the ranges shown.
11. $Z_{pkg\_Loopback}$ and $T_{pkg\_delay\_Loopback}$ applies to LBDQ and LBDQS.
12. Z_{pkg_DQS} and $T_{pkg\_delay\_DQS}$ applies to DQS_C, DQS_T, TDQS_T and TDQS_C.

Table 399: DRAM DDP Package Electrical Specifications (x4/x8) for DDR5 3200-6400

Parameter	Symbol	3200-6400		Unit	Notes
		MIN	MAX		
Input/output Z _{pkg}	Z _{pkg} _DQ	20	75	ohms	1,2,3,4,9
Input/output pkg delay	T _{pkg} _delay_DQ	25	100	ps	1,2,3,4,9
DQS _t , DQS _c Z _{pkg}	Z _{pkg} _DQS	20	75	ohms	1,2,4,9,11
DQS _t , DQS _c pkg delay	T _{pkg} _delay_DQS	25	100	ps	1,2,4,9,11
Delta Z _{pkg} DQS _t , DQS _c	DZ _{pkg} _DQS	–	5	ohms	1,2,4,6,9
Delta delay DQS _t , DQS _c	DT _{pkg} _delay_DQS	–	2	ps	1,2,4,6,9
Input-CTRL pins Z _{pkg}	Z _{pkg} _CTRL	20	75	ohms	1,2,4,8,9
Input-CTRL pins pkg delay	T _{pkg} _delay_CTRL	25	100	ps	1,2,4,8,9
Input-CMD ADD pins Z _{pkg}	Z _{pkg} _CA	20	75	ohms	1,2,4,7,9
Input-CMD ADD pins pkg delay	T _{pkg} _delay_CA	25	100	ps	1,2,4,7,9
CLK _t and CLK _c Z _{pkg}	Z _{pkg} _CLK	20	75	ohms	1,2,4,9
CLK _t and CLK _c pkg delay	T _{pkg} _delay_CLK	25	100	ps	1,2,4,9
Delta Z _{pkg} CLK _t and CLK _c	DZ _{pkg} _delay_CLK	–	5	ohms	1,2,4,5,9
Delta delay CLK _t and CLK _c	DT _{pkg} _delay_CLK	–	2	ps	1,2,4,5,9
ALERT Z _{pkg}	Z _{pkg} _ALERT	20	75	ohms	1,2,4,9
ALERT delay	T _{pkg} _delay_ALERT	25	100	ps	1,2,4,9
Loopback Z _{pkg}	Z _{pkg} _Loopback	20	75	ohms	1,2,4,9,10
Loopback delay	T _{pkg} _delay_Loopback	25	100	ps	1,2,4,9,10

Notes: 1. This parameter is not subject to production test.

2. This parameter is verified by design.

3. Z_{pkg}_DQ and T_{pkg}_delay_DQ applies to DQ, DM.

4. This parameter applies to DDP only.

5. Absolute value of Z_{pkg}_CK_t - Z_{pkg}_CK_c for impedance (Z) or absolute value of T_{pkg}_delay_CLK_t - T_{pkg}_delay_CLK_c for delay (T_{pkg}_delay).

6. Absolute value of Z_{pkg}(DQS_t) - Z_{pkg}(DQS_c) for impedance (Z) or absolute value of T_{pkg}_delay_DQS_t - T_{pkg}_delay_DQS_c for delay (T_{pkg}_delay)

7. Z_{pkg}_CA and T_{pkg}_delay_CA applies to CA[13:0].

8. Z_{pkg}_CTRL and T_{pkg}_delay_CTRL apply to CS_n and CS1_n.

9. Package implementations must meet specifications if the designed Z_{pkg} and T_{pkg}_delay fall within the ranges shown.

10. Z_{pkg}_Loopback and T_{pkg}_delay_Loopback applies to LBDQ and LBDQS.

11. Z_{pkg}_DQS and T_{pkg}_delay_DQS applies to DQS_C, DQS_T, TDQS_T and TDQS_C.

ESD Sensitivity Characteristics

Table 400: ESD Sensitivity Characteristics¹

Parameter	Symbol	MIN	MAX	Units	Notes
Human body model (HBM)	ESD _{HBM}	1000	–	V	3
Charged device model (CDM)	ESC _{CDM}	250	–	V	3

Notes: 1. State-of-the-art ESD control measures must be in place when handling devices.

2. Refer to ESDA/JEDEC Joint Standard JS-001 for measurement procedures.

3. Refer to ESDA/JEDEC Joint Standard JS-002 for measurement procedures.

Electrical Characteristics and AC Timing

Reference Load for AC Timing and Output Slew Rate

The figure below represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

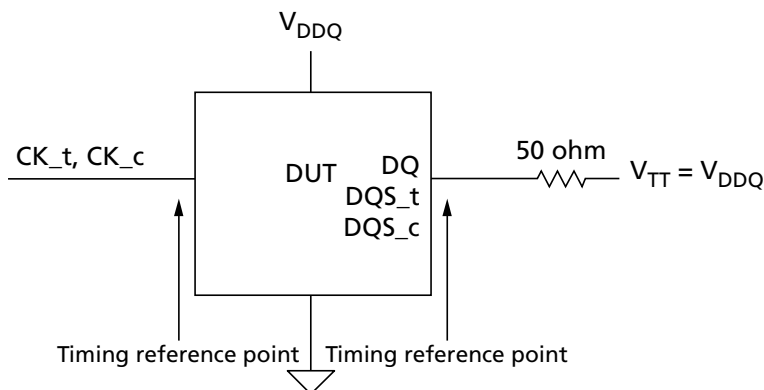
R_{ON} nominal of DQ, DQS_t, and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

- The maximum DC high level of output signal = $1.0 \times V_{DDQ}$.
- The minimum DC low level of output signal = $\{34 / (34 + 50)\} \times V_{DDQ} = 0.4 \times V_{DDQ}$
- The nominal reference level of an output signal can be approximated by the following:
 - The center of maximum DC high and minimum DC low
 $= \{(1 + 0.4) / 2\} \times V_{DDQ} = 0.7 \times V_{DDQ}$

The actual reference level of output signal might vary with driver R_{ON} and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 263: Reference Load for AC Timing and Output Slew Rate



Timing Parameters by Speed Grade: Standard

SDP Timing Parameters for DDR5 3200-4000

The analog timing parameters in this section have been defined based on nominal t_{CK} (AVG) MIN according to the rounding rules which can be found in the Rounding Definitions and Algorithms section. All minimum timing parameters needing to be translated from the time domain (ns, ps, etc.) to the clock domain (nCK) must be guard banded by an additional 0.3% according to the rules in the Rounding Definitions and Algorithms section.

Table 401: DDR5 3200-4000: Clock Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.625		0.555		0.500		ns	22

Table 402: DDR5 3200-4000: Command and Address Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
READ to READ command delay for same bank, in same bank group	t_{CCD_L}	$\max(RBL/2, 5ns)$							43
READ to READ command delay for different bank in same bank group	t_{CCD_M}	t_{CCD_L}						nCK, ns	43
WRITE to WRITE command delay for same bank, in same bank group	$t_{CCD\_L\_WR}$	$\max(32nCK, 20ns)$							43
WRITE to WRITE command delay for different bank, in same bank group	$t_{CCD\_M\_WR}$	$t_{CCD\_L\_WR}$						nCK, ns	43
WRITE to WRITE command delay for same bank group, second WRITE not RMW	$t_{CCD\_L\_WR2}$	$\max(16nCK, 10ns)$							43
READ to WRITE command delay for same bank group	$t_{CCD\_L\_RTW}$	$CL - CWL + RBL/2 + 2 t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for same bank, in same bank group	$t_{CCD\_L\_WTR}$	$CWL + WBL/2 + \max(16nCK, 10ns)$						nCK, ns	29,31, 43
WRITE to READ command delay for different bank, in same bank group	$t_{CCD\_M\_WTR}$	$t_{CCD\_L\_WTR}$						nCK, ns	29,31, 43
READ to READ command delay for different bank group	t_{CCD_S}	$RBL/2$						nCK	43
WRITE to WRITE command delay for different bank group	$t_{CCD\_S\_WR}$	$WBL/2$						nCK	43
READ to WRITE command delay for different bank group	$t_{CCD\_S\_RTW}$	$CL - CWL + RBL/2 + 2 t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for different bank group	$t_{CCD\_S\_WTR}$	$CWL + WBL/2 + \max(4nCK, 2.5ns)$						nCK, ns	29,31, 43

Table 402: DDR5 3200-4000: Command and Address Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
WRITE to READ with AUTO PRECHARGE command delay for same bank	t_{CCD_WTRA}	CWL + WBL/2 + $t_{WR} - t_{RTP}$						nCK, ns	29,31, 34,43
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	$t_{RRD\_L,1K}$	max(8nCK, 5ns)							43
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	$t_{RRD\_L,2K}$	max(8nCK, 5ns)							43
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	$t_{RRD\_S,1K}$	8						nCK	42
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	$t_{RRD\_S,2K}$	8						nCK	42
Four activate window for 1KB page size	$t_{FAW,1K}$	max(32nCK, 20.000ns)	-	max(32nCK, 17.777ns)	-	max(32nCK, 16.000ns)	-		
Four activate window for 2KB page size	$t_{FAW,2K}$	max(40nCK, 25.000ns)	-	max(40nCK, 22.222ns)	-	max(40nCK, 20.000ns)	-		
READ to PRECHARGE command delay	t_{RTP}	max(12nCK, 7.5ns)							43
PRECHARGE to PRECHARGE command delay	t_{PPD}	2						nCK	36,43
WRITE recovery time	t_{WR}	30						ns	1, 43
DLL locking time	t_{DLLK}	1024	-	1024	-	1280	-	nCK	

Table 403: DDR5 3200-4000: Mode Register Read/Write Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	t_{MRR}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		2
Mode register READ pattern to mode register READ pattern command spacing	t_{MRR_p}	8	-	8	-	8	-	nCK	
Mode register WRITE command period	t_{MRW}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		2
Mode register SET command delay	t_{MRD}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		
DFE mode register WRITE update delay time	t_{DFE}	80	-	80	-	80	-	ns	3

Table 404: DDR5 3200-4000: Data Strobe Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS _t , DQS _c differential READ preamble (1tCK preamble)	t_{RPRE1}	0.900	-	0.900	-	-	-	tCK	47,48

Table 404: DDR5 3200-4000: Data Strobe Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ preamble (2tCK preamble)	t_{RPRE2}	1.80	-	1.80	-	1.80	-	tCK	37,47
DQS_t, DQS_c differential READ preamble DDR4 (2tCK preamble)	$t_{\text{RPRE2\_D4}}$	1.80	-	1.80	-	1.80		tCK	37,47
DQS_t, DQS_c differential READ preamble (3tCK preamble)	t_{RPRE3}	-	-	-	-	2.70	-	tCK	38,47
DQS_t, DQS_c differential READ preamble (4tCK preamble)	t_{RPRE4}	-	-	-	-	-	-	tCK	39,47
DQS_t, DQS_c differential READ postamble (0.5tCK)	$t_{\text{RPST0.5}}$	0.450	-	0.450	-	0.450	-	tCK	40,46
DQS_t, DQS_c differential READ postamble (1.5tCK)	$t_{\text{RPST1.5}}$	1.200	-	1.200	-	1.200	-	tCK	42,47
DQS_t, DQS_c differential WRITE preamble (2tCK preamble)	t_{WPRE2}	1.800	-	1.800	-	1.800	-	tCK (avg)	37,49
DQS_t, DQS_c differential WRITE preamble (3tCK preamble)	t_{WPRE3}	-	-	-	-	2.700		tCK (avg)	38,47
DQS_t, DQS_c differential WRITE preamble (4tCK preamble)	t_{WPRE4}	-	-	-	-	3.600	-	tCK (avg)	40,47
DQS_t, DQS_c differential initial low pulse width during WRITE preamble (2tCK preamble)	t_{DQSL2PRE}	0.900	-	0.900	-	0.900	-	tCK (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (3tCK preamble)	t_{DQSL3PRE}	-	-	-	-	1.800	-	tCK (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (4tCK preamble)	t_{DQSL4PRE}	-	-	-	-	1.800	-	tCK (avg)	
DQS_t, DQS_c differential WRITE postamble - 0.5tCK	$t_{\text{WPST0.5}}$	0.450	-	0.450	-	0.450	-	tCK (avg)	41,47
DQS_t, DQS_c differential WRITE postamble - 1.5tCK	$t_{\text{WPST1.5}}$	-	-	-	-	1.200	-	tCK (avg)	42,47
DQS_t, DQS_c differential high toggle pulse width during DDR4 2tCK READ preamble	$t_{\text{DQSH2PRE\_D4}}$	1.35	-	1.35	-	1.35	-	tCK	
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	$t_{\text{DQSH\_pre}}$	0.395	0.605	0.395	0.605	0.395	0.605	tCK (avg)	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	$t_{\text{DQSL\_pre}}$	0.395	0.605	0.395	0.605	0.395	0.605	tCK (avg)	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	t_{DQSCk}	-0.240	0.240	-0.252	0.252	-0.270	0.270	tCK	6,9,16
DQS_t, DQS_c rising edge output variance window	t_{DQSCkI}	-	0.410	-	0.430	-	0.460	tCK	7,8,9,16,33

Table 405: DDR5 3200-4000: Write Enable Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2- t_{CK} WRITE preamble enable window	$t_{WPRE\_EN\_2}^{t_{CK}}$	1.5	-	1.5	-	1.5	-	t_{CK}	
3- t_{CK} WRITE preamble enable window	$t_{WPRE\_EN\_3}^{t_{CK}}$	2.5	-	2.5	-	2.5	-	t_{CK}	
4- t_{CK} WRITE preamble enable window	$t_{WPRE\_EN\_4}^{t_{CK}}$	2.5	-	2.5	-	2.5	-	t_{CK}	
Final trained value of host DQS_ t_{DQS_c} timing relative to CWL CK_ t_{CK_c} edge	$t_{DQSoffset}$	-0.5	0.5	-0.5	0.5	-0.5	0.5	t_{CK}	26
Write leveling setup time	t_{WLS}	-80	80	-80	80	-80	80	ps	
Write leveling hold time	t_{WLH}	-80	80	-80	80	-80	80	ps	
Voltage/temperature drift window of first rising DQS_ t preamble edge relative to CWL CK_ t_{CK_c} edge (x4/x8/x16)	t_{DQSD}	-0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	-0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	-0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	t_{CK}	5
Host and system voltage/temperature drift window of first rising DQS_ t preamble edge relative to CWL CK_ t_{CK_c} edge (x4/x8/x16)	t_{DQSS}	-0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	-0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	-0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	0.25 x $t_{WPRE\_E}^{N\_n}$ $t_{CK(min)}$	t_{CK}	5,32

Table 406: DDR5 3200-4000: Dynamic ODT Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RTT change skew timing - transitioning from one valid RTT state to the next valid RTT state	t_{ADC}	0.20	0.80	0.20	0.80	0.20	0.80	t_{CK} (avg)	45,46

Table 407: DDR5 3200-4000: MPSM Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	t_{MPSMX}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	ns	

Table 408: DDR5 3200-4000: ZQ Calibration Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	t_{ZQCAL}	1	-	1	-	1	-	μs	
ZQ calibration latch time	t_{ZQLAT}	max(30ns, 8 nCK)	-	max(30ns, 8 nCK)	-	max(30ns, 8 nCK)	-	nCK, ns	

Table 409: DDR5 3200-4000: Reset Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_ n low time for reset initialization with stable power	t_{PW_RESET}	1	-	1	-	1	-	μs	

Table 409: DDR5 3200-4000: Reset Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Time after RESET_n assertion to ODT off	t _{RST_ADC}	-	50	-	50	-	50	ns	

Table 410: DDR5 3200-4000: Self Refresh Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t _{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		
Self refresh CS_n low pulse width	t _{CSL}	10	-	10	-	10	-	ns	
Self refresh exit CS_n high pulse width	t _{CSH_SRexit}	13	200	13	200	13	200	ns	
Self refresh exit CS_n low pulse width	t _{CSL_SRexit}	3nCK	30ns	3nCK	30ns	3nCK	30ns	nCK, ns	11
Self refresh exit CS_n low pulse width with frequency change	t _{CSL_FreqChg}	VREFCA_t _{ime}	-	VREFCA_t _{ime}	-	VREFCA_t _{ime}	-	ns	12
Valid clock requirement before SRE	t _{CKSRX}	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-		
Valid clock requirement after SRE	t _{CKLCS}	t _{CPDED} + 1nCK	-	t _{CPDED} + 1nCK	-	t _{CPDED} + 1nCK	-	nCK, ns	
Self refresh exit CS_n HIGH	t _{CASRX}	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	t _{XS}	t _{RFC1}	-	t _{RFC1}	-	t _{RFC1}	-	ns	
Exit self refresh to commands requiring a locked DLL	t _{XS_DLL}	t _{DLLK}	-	t _{DLLK}	-	t _{DLLK}	-	nCK	

Table 411: DDR5 3200-4000: Power-Down Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t _{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		
Power-down duration	t _{PD}	max(7.5ns, 8nCK)	5*t _{REFI1} (normal) 9*t _{REFI2} (FGR)	max(7.5ns, 8nCK)	5*t _{REFI1} (normal) 9*t _{REFI2} (FGR)	max(7.5ns, 8nCK)	5*t _{REFI1} (normal) 9*t _{REFI2} (FGR)		28,44
Power-down exit command to next valid command (excluding NT ODT commands when PDE with CA11=L)	t _{XP}	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)			
ACTIVATE command to POWER DOWN ENTRY command	t _{ACTPDEN}	2	-	2	-	2	-	nCK	13
PRECHARGE, PRECHARGE ALL, or PRECHARGE SAME BANK command to POWER DOWN ENTRY command	t _{PRPDEN}	2	-	2	-	2	-	nCK	13

Table 411: DDR5 3200-4000: Power-Down Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
READ or READ w/ AUTO PRECHARGE command to POWER DOWN ENTRY command	t_{RDPDEN}	$CL+RBL/2+1$	-	$CL+RBL/2+1$	-	$CL+RBL/2+1$	-	nCK	24, 30
WRITE command to POWER DOWN ENTRY command	t_{WRPDEN}	$CWL+WBL / 2+WR+1$	-	$CWL+WBL / 2+WR+1$	-	$CWL+WBL / 2+WR+1$	-	nCK	14, 24,31
WRITE w/ AUTO PRECHARGE command to POWER DOWN ENTRY command	$t_{WRAPDEN}$	$CWL+WBL / 2+t_{WR}+1$	-	$CWL+WBL / 2+t_{WR}+1$	-	$CWL+WBL / 2+t_{WR}+1$	-	nCK	14, 15, 24,31
REFRESH ALL or REFRESH SAME BANK command to POWER DOWN ENTRY command	$t_{REFPDEN}$	2	-	2	-	2	-	nCK	
MRR command to POWER DOWN ENTRY command	$t_{MRRPDEN}$	$CL+8+1$	-	$CL+8+1$	-	$CL+8+1$	-	nCK	24
MRW command to POWER DOWN ENTRY command	$t_{MRWPDEN}$	$t_{MRD} \text{ (MIN)}$	-	$t_{MRD} \text{ (MIN)}$	-	$t_{MRD} \text{ (MIN)}$	-	nCK	
MPC command to POWER DOWN ENTRY command	$t_{MPCPDEN}$	t_{MPC_delay}	-	t_{MPC_delay}	-	t_{MPC_delay}	-	nCK	25

Table 412: DDR5 3200-4000: MPC Command Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	t_{MPC_Delay}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	$t_{MC\_MPC\_Setup}$	3	-	3	-	3	-	nCK	21
Time between first rising CS edge and stable MPC command (hold)	$t_{MC\_MPC\_Hold}$	3	-	3	-	3	-	nCK	21
Time CS_n is held LOW to register MPC command	t_{MPC_CS}	3.5	8	3.5	8	3.5	8	nCK	20

Table 413: DDR5 3200-4000: PDA Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle time	$t_{PDA\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY} \text{ (MAX)} + BL/2 + 19ns$	-	$t_{PDA\_DQS\_DELAY} \text{ (MAX)} + BL/2 + 19ns$	-	$t_{PDA\_DQS\_DELAY} \text{ (MAX)} + BL/2 + 19ns$	-	nCK, ns	
PDA ENUMERATE ID command to any other command cycle time for multi-device continuous DQS toggle mode	$t_{PDA\_DELAY\_2}$	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} \text{ (MIN)}$	-	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} \text{ (MIN)}$	-	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} \text{ (MIN)}$	-	nCK, ns	

Table 413: DDR5 3200-4000: PDA Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay to rising strobe edge used for sampling DQ during PDA operation	$t_{PDA\_DQS\_DELAY}$	5	18	5	18	5	18	ns	4
Delay to falling DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY(MIN)} - t_{PDA\_S\_FALL(MIN)}$	$t_{PDA\_DQS\_DELAY(MAX)} - t_{PDA\_S\_FALL(MIN)}$	$t_{PDA\_DQS\_DELAY(MIN)} - t_{PDA\_S\_FALL(MIN)}$	$t_{PDA\_DQS\_DELAY(MAX)} - t_{PDA\_S\_FALL(MIN)}$	$t_{PDA\_DQS\_DELAY(MIN)} - t_{PDA\_S\_FALL(MIN)}$	$t_{PDA\_DQS\_DELAY(MAX)} - t_{PDA\_S\_FALL(MIN)}$	nCK, ns	
Delay to rising DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_2}$	$t_{PDA\_DELAY\_1(MIN)}$	-	$t_{PDA\_DELAY\_1(MIN)}$	-	$t_{PDA\_DELAY\_1(MIN)}$	-	nCK, ns	
Delay after last DQS toggle used for sampling DQ during PDA	$t_{PDA\_DQS\_STOP}$	$t_{MPC\_DELAY(MIN)} + t_{PDA\_H\_RISE(MIN)}$	-	$t_{MPC\_DELAY(MIN)} + t_{PDA\_H\_RISE(MIN)}$	-	$t_{MPC\_DELAY(MIN)} + t_{PDA\_H\_RISE(MIN)}$	-	nCK, ns	
Delay after last DQ toggle used for sampling DQ during PDA	$t_{PDA\_DQ\_STOP}$	$t_{MPC\_DELAY(MIN)}$	-	$t_{MPC\_DELAY(MIN)}$	-	$t_{MPC\_DELAY(MIN)}$	-	nCK, ns	
Falling DQ edge setup time during PDA operation	$t_{PDA\_S\_FALL}$	max(3nCK, 1.875ns)	-	max(3nCK, 1.666ns)	-	max(3nCK, 1.500ns)	-	nCK, ns	
Rising DQ edge hold time during PDA operation	$t_{PDA\_H\_RISE}$	max(3nCK, 1.875ns)	-	max(3nCK, 1.666ns)	-	max(3nCK, 1.500ns)	-	nCK, ns	
Rising DQ Edge setup time during PDA operation	$t_{PDA\_S\_RISE}$	$t_{MPC\_DELAY(MIN)}$	-	$t_{MPC\_DELAY(MIN)}$	-	$t_{MPC\_DELAY(MIN)}$	-	nCK, ns	
Falling DQ Edge hold time during PDA operation	$t_{PDA\_H\_FALL}$	$t_{MPC\_DELAY(MIN)}$	-	$t_{MPC\_DELAY(MIN)}$	-	$t_{MPC\_DELAY(MIN)}$	-	nCK, ns	

Table 414: DDR5 3200-4000: Read Training Timing

Parameter	Symbol	3200		3600		4000		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Registration of MRW continuous burst mode exit to next valid command delay	$t_{Cont\_Exit\_Delay}$	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	-
Registration of MRW continuous burst mode exit to end of training mode	t_{Cont_Exit}	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-
Maximum delay between first exit continuous burst mode MRW command and the second exit continuous burst mode MRW command	t_{CBME}	-	CL - 10nCK	-	CL - 10nCK	-	CL - 10nCK	-

Table 415: DDR5 3200-4000: Read Preamble Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	t_{SDOn}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		
Delay from MRW command to DQS disabled	t_{SDOff}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		

Table 416: DDR5 3200-4000: CA Training Mode Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	t_{CATM_Entry}	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	t_{CATM_Exit}	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	$t_{CATM\_Exit\_Delay}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	t_{CATM_Valid}	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{CATM\_DQ\_Window}$	2	-	2	-	2	-	nCK	27
CS_n assertion duration to exit CATM	$t_{CATM\_CS\_Exit}$	2	8	2	8	2	8	nCK	

Table 417: DDR5 3200-4000: CS Training Mode Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	t_{CSTM_Entry}	20	-	20	-	20	-	ns	
Registration of CSTM exit command to end of training mode	t_{CSTM_Exit}	-	20	-	20	-	20	ns	
Registration of CSTM exit to next valid command delay	$t_{CSTM\_Exit\_Delay}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	t_{CSTM_Valid}	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{CSTM\_DQ\_Window}$	2	-	2	-	2	-	nCK	27
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	$t_{CSTM\_Min\_to\_MPC\_exit}$	4	-	4	-	4	-	nCK	

Table 418: DDR5 3200-4000: Write Leveling Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	t_{WLPEN}	-	15	-	15	-	15	ns	

Table 418: DDR5 3200-4000: Write Leveling Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling output delay	t_{WLO}	–	9.5	–	9.5	–	9.5	ns	
Width of write leveling internal pulse	$t_{WL\_Pulse\_Width}$	2	–	2	–	2	–	t_{CK}	17
Write leveling write to subsequent command spacing	t_{WL_Write}	$\max(CWL, \text{last DQS differential toggle}) + t_{WLO(MAX)} + 2nCK$	–	$\max(CWL, \text{last DQS differential toggle}) + t_{WLO(MAX)} + 2nCK$	–	$\max(CWL, \text{last DQS differential toggle}) + t_{WLO(MAX)} + 2nCK$	–		

Table 419: DDR5 3200-4000: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{REFCA} command to any other valid command delay	t_{VREFCA_Delay}	t_{MRD}	–	t_{MRD}	–	t_{MRD}	–	nCK	
V_{REFCS} command to any other valid command delay	t_{VREFCS_Delay}	t_{MRD}	–	t_{MRD}	–	t_{MRD}	–	nCK	
Time CS _n is held LOW to register V_{REFCA} command	t_{VREFCA_CS}	3.5	8	3.5	8	3.5	8	nCK	18,19
Time CS _n is held LOW to register V_{REFCS} command	t_{VREFCS_CS}	3.5	8	3.5	8	3.5	8	nCK	18,19
MIN time between stable V_{REFCA} command and first falling CS edge (SETUP)	$t_{MC\_VREFCA\_Setup}$	3	–	3	–	3	–	nCK	10
MIN time between first rising CS edge and stable V_{REFCA} command (HOLD)	$t_{MC\_VREFCA\_Hold}$	3	–	3	–	3	–	nCK	10
MIN time between stable V_{REFCS} command and first falling CS edge (SETUP)	$t_{MC\_VREFCS\_Setup}$	3	–	3	–	3	–	nCK	10
MIN time between first rising CS edge and stable V_{REFCS} command (HOLD)	$t_{MC\_VREFCS\_Hold}$	3	–	3	–	3	–	nCK	10

Table 420: DDR5 3200-4000: hPPR/sPPR Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	t_{PGM_hPPRa}	1000	–	1000	–	1000	–	ms	
hPPR programming time (x16)	t_{PGM_hPPRb}	2000	–	2000	–	2000	–	ms	
sPPR programming time	t_{PGM_sPPR}	$CWL + 8t_{CK} + t_{WR}$		$CWL + 8t_{CK} + t_{WR}$		$CWL + 8t_{CK} + t_{WR}$		t_{CK}	
hPPR/sPPR exit recognition time	t_{PGM_Exit}	t_{RP}	–	t_{RP}	–	t_{RP}	–	ns	
hPPR program exit and new address setting time	t_{PGMPST}	50	–	50	–	50	–	μs	
sPPR program exit and new address setting time	t_{PGMPST_sPPR}	t_{MRD}	–	t_{MRD}	–	t_{MRD}	–	ns	

Table 421: DDR5 3200-4000: DQS Interval Oscillator Readout Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	t_{OSCOM}	t_{MPC_Delay}	-	t_{MPC_Delay}	-	t_{MPC_Delay}	-	nCK	23
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	t_{OSCOA}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	23
DQS interval oscillator start gap in automatic stop mode	t_{OSCS}	t_{MPC_Delay} +DQS interval timer run time						nCK	23,43

Table 422: DDR5 3200-4000: ESC Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	t_{ECSc}	max(176nCK, 110ns)	-	max(176nCK, 110ns)	-	max(176nCK, 110ns)	-		

Table 423: DDR5 3200-4000: CRC Error Reporting Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT_n latency	t_{CRC_ALERT}	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	nCK	

Timing Parameters for DDR5 4400-5200

The analog timing parameters in this section have been defined based on nominal $t_{CK(avg)min}$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 424: DDR5 4400-5200: Clock Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.454	-	0.416	-	0.384		ns	22

Table 425: DDR5 4400-5200: Command and Address Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
READ to READ command delay for same bank, in same bank group	t_{CCD_L}	max(RBL/2,5ns)							43
READ to READ command delay for different bank,in same bank group	t_{CCD_M}	t_{CCD_L}						nCK, ns	43
WRITE to WRITE command delay for same bank, in same bank group	$t_{CCD\_L\_WR}$	max(32nCK,20ns)							43
Write to Write command delay for different bank,in same bank group	$t_{CCD\_M\_WR}$	$t_{CCD\_L\_WR}$						nCK, ns	43

Table 425: DDR5 4400-5200: Command and Address Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
WRITE to WRITE command delay for same bank group, second WRITE not RMW	$t_{CCD\_L\_WR2}$	$\max(16nCK, 10ns)$							43
READ to WRITE command delay for same bank group	$t_{CCD\_L\_RTW}$	$CL - CWL + RBL/2 + 2 t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for same bank, in same bank group	$t_{CCD\_L\_WTR}$	$CWL + WBL/2 + \max(16nCK, 10ns)$							29,31, 43
WRITE to READ command delay for different bank, in same bank group	$t_{CCD\_M\_WTR}$	$t_{CCD\_L\_WTR}$						nCK, ns	29,31, 43
READ to READ command delay for different bank group	t_{CCD_S}	$RBL/2$						nCK	43
WRITE to WRITE command delay for different bank group	$t_{CCD\_S\_WR}$	$WBL/2$						nCK	43
READ to WRITE command delay for different bank group	$t_{CCD\_S\_RTW}$	$CL - CWL + RBL/2 + 2 t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5 t_{CK}) + t_{WPR}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for different bank group	$t_{CCD\_S\_WTR}$	$CWL + WBL/2 + \max(4nCK, 2.5ns)$							29,31, 43
WRITE to READ with AUTO PRECHARGE command for same bank	t_{CCD_WTRA}	$CWL + WBL/2 + t_{WR} - t_{RTP}$						nCK, ns	29,31, 34,43
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	$t_{RRD\_L,1K}$	$\max(8nCK, 5ns)$							43
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	$t_{RRD\_L,2K}$	$\max(8nCK, 5ns)$							43
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	$t_{RRD\_S,1K}$	8						nCK	43
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	$t_{RRD\_S,2K}$	8						nCK	43
Four activate window for 1KB page size	$t_{FAW,1K}$	$\max(32nCK, 14.545ns)$	-	$\max(32nCK, 13.333ns)$	-	$\max(32nCK, 12.307ns)$	-		
Four activate window for 2KB page size	$t_{FAW,2K}$	$\max(40nCK, 18.181ns)$	-	$\max(40nCK, 16.666ns)$	-	$\max(40nCK, 15.384ns)$	-		
READ command to PRECHARGE command delay	t_{RTP}	$\max(12nCK, 7.5ns)$							43
PRECHARGE to PRECHARGE command delay	t_{PPD}	2						nCK	36,43
WRITE recovery time	t_{WR}	30						ns	1,43
DLL locking time	t_{DLLK}	1280	-	1536	-	1536	-	nCK	

Table 426: DDR5 4400-5200: Mode Register Read/Write Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	t_{MRR}	$\max(14ns, 16nCK)$	-	$\max(14ns, 16nCK)$	-	$\max(14ns, 16nCK)$	-		2

Table 426: DDR5 4400-5200: Mode Register Read/Write Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ pattern to mode register READ pattern command spacing	t_{MRR_p}	8	-	8	-	8	-	nCK	
Mode register WRITE command period	t_{MRW}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		2
Mode register SET command delay	t_{MRD}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		
DFE mode register WRITE update delay time	t_{DFE}	80	-	80	-	80	-	ns	3

Table 427: DDR5 4400-5200: Data Strobe Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Preamble (1tCK Preamble)	t_{RPRE1}	-	-	-	-	-	-	tCK	47,48
DQS_t, DQS_c differential READ Preamble (2tCK Preamble)	t_{RPRE2}	1.80	-	1.80	-	-	-	tCK	37,47
DQS_t, DQS_c differential READ Preamble DDR4 (2tCK Preamble)	t_{RPRE2_D4}	1.80	-	1.80	-	-	-	tCK	37,47
DQS_t, DQS_c differential READ Preamble (3tCK Preamble)	t_{RPRE3}	2.70	-	2.70	-	2.70	-	tCK	38,47
DQS_t, DQS_c differential READ Preamble (4tCK Preamble)	t_{RPRE4}	-	-	-	-	-	-	tCK	39,47
DQS_t, DQS_c differential READ Postamble - 0.5tCK	$t_{RPST0.5}$	0.45	-	0.45	-	-	-	tCK	41,47
DQS_t, DQS_c differential READ Postamble - 1.5tCK	$t_{RPST1.5}$	1.20	-	1.20	-	1.20	-	tCK	42,47
DQS_t, DQS_c differential WRITE Preamble (2tCK Preamble)	t_{WPRE2}	1.800	-	1.800	-	-	-	tCK (avg)	37,47
DQS_t, DQS_c differential WRITE Preamble (3tCK Preamble)	t_{WPRE3}	2.700	-	2.700	-	2.700	-	tCK (avg)	38,47
DQS_t, DQS_c differential WRITE Preamble (4tCK Preamble)	t_{WPRE4}	3.600	-	3.600	-	3.600	-	tCK (avg)	40,47
DQS_t, DQS_c differential high toggle pulse width during DDR4 2tCK READ Preamble	$t_{DQSH2PRE\_D4}$	1.35	-	1.35	-	-	-	tCK	
DQS_t, DQS_c differential initial low pulse width during WRITE Preamble (2tCK Preamble)	$t_{DQSL2PRE}$	0.900	-	0.900	-	-	-	tCK (avg)	
DQS_t, DQS_c differential initial low pulse width during Preamble (3tCK Preamble)	$t_{DQSL3PRE}$	1.800	-	1.800	-	1.800	-	tCK (avg)	

Table 427: DDR5 4400-5200: Data Strobe Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential initial low pulse width during Preamble (4tCK Preamble)	$t_{DQSL4PRE}$	1.800	-	1.800	-	1.800	-	tCK (avg)	
DQS_t, DQS_c differential WRITE Postamble - 0.5tCK	$t_{WPST0.5}$	0.450	-	0.450	-	-	-	tCK (avg)	41,47
DQS_t, DQS_c differential WRITE Postamble - 1.5tCK	$t_{WPST1.5}$	1.200	-	1.200	-	1.200	-	tCK (avg)	41,47
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	t_{DQSH_pre}	0.395	0.605	0.430	0.570	0.430	0.570	tCK (avg)	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	t_{DQSL_pre}	0.395	0.605	0.430	0.570	0.430	0.570	tCK (avg)	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	t_{DQSCK}	-0.286	0.286	-0.300	0.300	-0.313	0.313	tCK	6,9,16
DQS_t, DQS_c rising edge output variance window	t_{DQSCKi}	-	0.475	-	0.490	-	0.510	tCK	7,8,9,16,33

Table 428: DDR5 4400-5200: Write Enable Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2-tCK WRITE preamble enable window	$t_{WPRE\_EN\_2tCK}$	1.5	-	1.5	-	1.5	-	tCK	
3-tCK WRITE preamble enable window	$t_{WPRE\_EN\_3tCK}$	2.5	-	2.5	-	2.5	-	tCK	
4-tCK WRITE preamble enable window	$t_{WPRE\_EN\_4tCK}$	2.5	-	2.5	-	2.5	-	tCK	
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	$t_{DQSoffset}$	-0.5	0.5	-0.5	0.5	-0.5	0.5	tCK	26
Write leveling setup time	t_{WLS}	-80	80	-80	80	-80	80	ps	
Write leveling hold time	t_{WLH}	-80	80	-80	80	-80	80	ps	
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	t_{DQSD}	-0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	-0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	-0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	tCK	5
Host and system voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	t_{DQSS}	-0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	-0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	-0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	0.25 x $t_{WPRE\_EN\_N\_n}tCK$ (MIN)	tCK	5,32

Table 429: DDR5 4400-5200: Dynamic ODT Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RTT change skew timing - transitioning from one valid RTT state to the next valid RTT state	t_{ADC}	0.20	0.80	0.20	0.80	0.20	0.80	t_{CK} (avg)	45,46

Table 430: DDR5 4400-5200: MPSM Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	t_{MPSMX}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	ns	

Table 431: DDR5 4400-5200: ZQ Calibration Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	t_{ZQCAL}	1		1		1		μs	
ZQ calibration latch time	t_{ZQLAT}	max(30ns, 8nCK)		max(30ns, 8nCK)		max(30ns, 8nCK)			

Table 432: DDR5 4400-5200: Reset Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_n low time for reset initialization with stable power	t_{PW_RESET}	1	-	1	-	1	-	μs	
Time after RESET_n assertion to ODT off	t_{RST_ADC}	-	50	-	50	-	50	ns	

Table 433: DDR5 4400-5200: Self Refresh Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t_{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		
Self refresh CS_n low pulse width	t_{CSL}	10	-	10	-	10	-	ns	
Self refresh exit CS_n high pulse width	t_{CSH_SExit}	13	200	13	200	13	200	ns	
Self refresh exit CS_n low pulse width	t_{CSL_SExit}	3nCK	30ns	3nCK	30ns	3nCK	30ns		11
Self refresh exit CS_n low pulse width with frequency change	$t_{CSL\_FreqChg}$	VREFCA_time	-	VREFCA_time	-	VREFCA_time	-	ns	12
Valid clock requirement before SRX	t_{CKSRX}	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-		
Valid clock requirement after SRE	t_{CKLCS}	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	nCK, ns	
Self refresh exit CS_n HIGH	t_{CASRX}	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC1}	-	t_{RFC1}	-	t_{RFC1}	-	ns	

Table 433: DDR5 4400-5200: Self Refresh Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Exit self refresh to commands requiring a locked DLL	t_{XS_DLL}	t_{DLLK}	-	t_{DLLK}	-	t_{DLLK}	-	nCK	

Table 434: DDR5 4400-5200: Power-Down Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t_{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		
Power-down duration	t_{PD}	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)		28, 44
Power-down exit command to next valid command (excluding NT ODT commands when PDE with CA11=L)	t_{XP}	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-		
ACTIVATE command to POWER DOWN ENTRY command	$t_{ACTPDEN}$	2	-	2	-	2	-	nCK	13
PRECHARGE, PRECHARGE ALL, or PRECHARGE SAME BANK command to POWER DOWN ENTRY command	t_{PRPDEN}	2	-	2	-	2	-	nCK	13
READ or READ w/ AUTO PRECHARGE command to POWER DOWN ENTRY command	t_{RDPDEN}	CL+RBL/2+1	-	CL+RBL/2+1	-	CL+RBL/2+1	-	nCK	24, 30
WRITE command to POWER DOWN ENTRY command	t_{WRPDEN}	CWL+WBL/2+WR+1	-	CWL+WBL/2+WR+1	-	CWL+WBL/2+WR+1	-	nCK	14, 24, 31
WRITE w/ AUTO PRECHARGE command to POWER DOWN ENTRY command	$t_{WRAPDEN}$	CWL+WBL/2+- t_{WR} +1	-	CWL+WBL/2+- t_{WR} +1	-	CWL+WBL/2+- t_{WR} +1	-	nCK	14, 15, 24, 31
REFRESH ALL or REFRESH SAME BANK command to POWER DOWN ENTRY command	$t_{REFPDEN}$	2	-	2	-	2	-	nCK	
MRR command to POWER DOWN ENTRY command	$t_{MRRPDEN}$	CL+8+1	-	CL+8+1	-	CL+8+1	-	nCK	24
MRW command to POWER DOWN ENTRY command	$t_{MRWPDEN}$	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	nCK	
MPC command to POWER DOWN ENTRY command	$t_{MPCPDEN}$	t_{MPC_delay}	-	t_{MPC_delay}	-	t_{MPC_delay}	-	nCK	25

Table 435: DDR5 4400-5200: MPC Command Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	t_{MPC_Delay}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	$t_{MC\_MPC\_Setup}$	3	-	3	-	3	-	nCK	21
Time between first rising CS edge and stable MPC command (HOLD)	$t_{MC\_MPC\_Hold}$	3	-	3	-	3	-	nCK	21
Time CS _n is held LOW to register MPC command	t_{MPC_CS}	3.5	8	3.5	8	3.5	8	nCK	20

Table 436: DDR5 4400-5200: PDA Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle time	$t_{PDA\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY} (MAX) + BL/2 + 19ns$	-	$t_{PDA\_DQS\_DELAY} (MAX) + BL/2 + 19ns$	-	$t_{PDA\_DQS\_DELAY} (MAX) + BL/2 + 19ns$	-	nCK, ns	
PDA ENUMERATE ID command to any other command cycle time for multi-device continuous DQS toggle mode	$t_{PDA\_DELAY\_2}$	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} (MIN)$	-	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} (MIN)$	-	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} (MIN)$	-	nCK, ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	$t_{PDA\_DQS\_DELAY}$	5	18	5	18	5	18	ns	4
Delay to falling DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY} (MIN) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MAX) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MIN) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MAX) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MIN) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MAX) - t_{PDA\_S\_FALL} (MIN)$	nCK, ns	
Delay to rising DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_2}$	$t_{PDA\_DELAY\_1} (MIN)$	-	$t_{PDA\_DELAY\_1} (MIN)$	-	$t_{PDA\_DELAY\_1} (MIN)$	-	nCK, ns	
Delay after last DQStoggle used for sampling DQ during PDA	$t_{PDA\_DQS\_STOP}$	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	nCK, ns	
Delay after last DQ toggle used for sampling DQ during PDA	$t_{PDA\_DQ\_STOP}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	nCK, ns	
Falling DQS edge setup time during PDA operation	$t_{PDA\_S\_FALL}$	Max(3nCK, 1.363ns)	-	Max(3nCK, 1.250ns)	-	Max(3nCK, 1.250ns)	-		
Rising DQS edge hold time during PDA operation	$t_{PDA\_H\_RISE}$	Max(3nCK, 1.363ns)	-	Max(3nCK, 1.250ns)	-	Max(3nCK, 1.250ns)	-		

Table 436: DDR5 4400-5200: PDA Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Rising DQ Edge setup time during PDA operation	$t_{PDA\_S\_RISE}$	t_{MPC_DELAY} (MIN)	-	t_{MPC_DELAY} (MIN)	-	t_{MPC_DELAY} (MIN)	-	nCK, ns	
Falling DQ Edge hold time during PDA operation	$t_{PDA\_H\_FALL}$	t_{MPC_DELAY} (MIN)	-	t_{MPC_DELAY} (MIN)	-	t_{MPC_DELAY} (MIN)	-	nCK, ns	

Table 437: DDR5 4400-5200: Read Training Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	$t_{Cont\_Exit\_Delay}$	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	-	
Registration of MRW continuous burst mode exit to end of training mode	t_{Cont_Exit}	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	
Maximum delay between first exit continuous burst mode MRW command and the second exit continuous burst mode MRW command	t_{CBME}	-	CL-10nCK	-	CL-10nCK	-	CL-10nCK	-	

Table 438: DDR5 4400-5200: Read Preamble Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	t_{SDOn}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		
Delay from MRW command to DQS disabled	t_{SDOff}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		

Table 439: DDR5 4400-5200: CA Training Mode Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	t_{CATM_Entry}	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	t_{CATM_Exit}	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	$t_{CATM\_Exit\_Delay}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	t_{CATM_Valid}	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{CATM\_DQ\_Window}$	2	-	2	-	2	-	nCK	27
CS_n assertion duration to exit CATM	$t_{CATM\_CS\_Exit}$	2	8	2	8	2	8	nCK	

Table 440: DDR5 4400-5200: CS Training Mode Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	$t_{\text{CSTM\_Entry}}$	20	-	20	-	20	-	ns	
Registration of CSTM exit command to end of training mode	$t_{\text{CSTM\_Exit}}$	-	20	-	20	-	20	ns	
Registration of CSTM exit to next valid command delay	$t_{\text{CSTM\_Exit\_Delay}}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	$t_{\text{CSTM\_Valid}}$	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{\text{CSTM\_DQ\_Window}}$	2	-	2	-	2	-	nCK	27
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	$t_{\text{CSTM\_Min\_to\_MPC\_exit}}$	4	-	4	-	4	-	nCK	

Table 441: DDR5 4400-5200: Write Leveling Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	t_{WLPEN}	-	15	-	15	-	15	ns	
Write leveling output delay	t_{WLO}	-	9.5	-	9.5	-	9.5	ns	
Width of write leveling internal pulse	$t_{\text{WL\_Pulse\_Width}}$	2	-	2	-	2	-	tCK	17
Write leveling write to subsequent command spacing	$t_{\text{WL\_Write}}$	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-		

Table 442: DDR5 4400-5200: $V_{\text{REFCA}}/V_{\text{REFCS}}$ Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
VREFCA command to any other valid command delay	$t_{\text{VREFCA\_Delay}}$	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
VREFCS command to any other valid command delay	$t_{\text{VREFCS\_Delay}}$	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time CS_n is held LOW to register VREFCA command	$t_{\text{VREFCA\_CS}}$	3.5	8	3.5	8	3.5	8	nCK	18,19
Time CS_n is held LOW to register VREFCS command	$t_{\text{VREFCS\_CS}}$	3.5	8	3.5	8	3.5	8	nCK	18,19
MIN time between stable VREFCA command and first falling CS edge (SETUP)	$t_{\text{MC\_VREFCA\_Setup}}$	3	-	3	-	3	-	nCK	10
MIN time between first rising CS edge and stable VREFCA command (HOLD)	$t_{\text{MC\_VREFCA\_Hold}}$	3	-	3	-	3	-	nCK	10

Table 442: DDR5 4400-5200: VREFCA/VREFCS Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MIN time between stable VREFCS command and first falling CS edge (SETUP)	$t_{MC\_VREFCS\_Setup}$	3	-	3	-	3	-	nCK	10
MIN time between first rising CS edge and stable VREFCS command (HOLD)	$t_{MC\_VREFCS\_Hold}$	3	-	3	-	3	-	nCK	10

Table 443: DDR5 4400-5200: hPPR/sPPR Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	t_{PGM_hPPRa}	1000	-	1000	-	1000	-	ms	
hPPR programming time (x16)	t_{PG_hPPRMb}	2000	-	2000	-	2000	-	ms	
sPPR programming time	t_{PGM_sPPR}	$CWL+8t_{CK}+t_{WR}$		$CWL+8t_{CK}+t_{WR}$		$CWL+8t_{CK}+t_{WR}$		t_{CK}	
hPPR/sPPR exit recognition time	t_{PGM_Exit}	t_{RP}	-	t_{RP}	-	t_{RP}	-	ns	
hPPR program exit and new address setting time	t_{PGMPST}	50	-	50	-	50	-	μs	
sPPR program exit and new address setting time	t_{PGMPST_sPPR}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	ns	

Table 444: DDR5 4400-5200: DQS Interval Oscillator Readout Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	t_{OSCOM}	t_{MPC_Delay}	-	t_{MPC_Delay}	-	t_{MPC_Delay}	-	nCK	23
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	t_{OSCOA}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	23
DQS interval oscillator start gap in automatic stop mode	t_{OSCS}	$t_{MPC\_Delay} + \text{DQS interval timer runtime}$						nCK	23,43

Table 445: DDR5 4400-5200: ESC Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	t_{ECSc}	$\max(176nCK, 110ns)$	-	$\max(176nCK, 110ns)$	-	$\max(176nCK, 110ns)$	-		

Table 446: DDR5 4400-5200: CRC Error Reporting Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT_n latency	t_{CRC_ALERT}	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	nCK	

Timing Parameters for DDR5 5600-6400

The analog timing parameters in this section have been defined based on nominal $t_{CK(avg)min}$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 447: DDR5 5600-6400: Clock Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.357		0.333	–	0.312	–	ns	22

Table 448: DDR5 5600-6400: Command and Address Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
READ to READ command delay for same bank, in same bank group	t_{CCD_L}	$\max(RBL/2, 5ns)$							43
READ to READ command delay for different bank, in same bank group	t_{CCD_M}	t_{CCD_L}						nCK, ns	43
WRITE to WRITE command delay for same bank, in same bank group	$t_{CCD\_L\_WR}$	$\max(32nCK, 20ns)$							43
WRITE to WRITE command delay for different bank, in same bank group	$t_{CCD\_M\_WR}$	$\max(32nCK, 20ns)$							43
WRITE to WRITE command delay for same bank group, second WRITE not RMW	$t_{CCD\_L\_WR2}$	$\max(16nCK, 10ns)$							43
READ to WRITE command delay for same bank group	$t_{CCD\_L\_RTW}$	$CL - CWL + RBL/2 + 2 t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for same bank, in same bank group	$t_{CCD\_L\_WTR}$	$CWL + WBL/2 + 16nCK, 10ns (MAX)$						nCK, ns	29,31, 43
WRITE to READ command delay for different bank, in same bank group	$t_{CCD\_M\_WTR}$	$CWL + WBL/2 + 16nCK, 10ns (MAX)$						nCK, ns	29,31, 43
READ to READ command delay for different bank group	t_{CCD_S}	$RBL/2$						nCK	43
WRITE to WRITE command delay for different bank group	$t_{CCD\_S\_WR}$	$WBL/2$						nCK	43
READ to WRITE command delay for different bank group	$t_{CCD\_S\_RTW}$	$CL - CWL + RBL/2 + 2 t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for different bank group	$t_{CCD\_S\_WTR}$	$CWL + WBL/2 + 4nCK, 2.5ns (MAX)$							29,31, 43
WRITE to READ with AUTO PRECHARGE command for same bank	t_{CCD_WTRA}	$CWL + WBL/2 + t_{WR} - t_{RTP}$						nCK, ns	29,31, 34,43
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	$t_{RRD\_L,1K}$	$\max(8nCK, 5ns)$							43
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	$t_{RRD\_L,2K}$	$\max(8nCK, 5ns)$							43

Table 448: DDR5 5600-6400: Command and Address Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	$t_{RRD\_S,1K}$	8						nCK	43
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	$t_{RRD\_S,2K}$	8						nCK	43
Four activate window for 2KB page size	$t_{FAW,2K}$	max(40nCK, 14.285ns)	-	max(40nCK, 13.333ns)	-	max(40nCK, 12.500ns)	-		
Four activate window for 1KB page size	$t_{FAW,1K}$	max(32nCK, 11.428ns)	-	max(32nCK, 10.666ns)	-	max(32nCK, 10.000ns)	-		
READ command to PRECHARGE command delay	t_{RTP}	max(12nCK, 7.5ns)							43
PRECHARGE to PRECHARGE command delay	t_{PPD}	2						nCK	36,43
WRITE recovery time	t_{WR}	30						ns	1,43
DLL locking time	t_{DLLK}	1792	-	1792	-	2048	-	nCK	

Table 449: DDR5 5600-6400: Mode Register Read/Write Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	t_{MRR}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		2
Mode register READ pattern to mode register READ pattern command spacing	t_{MRR_p}	8	-	8	-	8	-	nCK	
Mode register WRITE command period	t_{MRW}	5ns, 8nCK (MAX)	-	5ns, 8nCK (MAX)	-	5ns, 8nCK (MAX)	-		2
Mode register SET command delay	t_{MRD}	14ns, 16nCK (MAX)	-	14ns, 16nCK (MAX)	-	14ns, 16nCK (MAX)	-		
DFE mode register WRITE update delay time	t_{DFE}	80	-	80	-	80	-	ns	3

Table 450: DDR5 5600-6400: Data Strobe Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ preamble (1tCK preamble)	t_{RPRE1}	-	-	-	-	-	-	tCK	47,48
DQS_t, DQS_c differential READ preamble (2tCK preamble)	t_{RPRE2}	1.800	-	1.800	-	1.800	-	tCK	37,47
DQS_t, DQS_c differential READ preamble DDR4 (2tCK preamble)	t_{RPRE2_D4}	-	-	-	-	-	-	tCK	37,47
DQS_t, DQS_c differential READ preamble (3tCK preamble)	t_{RPRE3}	2.70	-	2.70	-	2.70	-	tCK	38,47
DQS_t, DQS_c differential READ preamble (4tCK preamble)	t_{RPRE4}	3.60	-	3.60	-	3.60	-	tCK	39,47
DQS_t, DQS_c differential READ postamble - 0.5tCK	$t_{RPST0.5}$	0.450	-	0.450	-	0.450	-	tCK	41,47
DQS_t, DQS_c differential READ postamble - 1.5tCK	$t_{RPST1.5}$	1.20	-	1.20	-	1.20	-	tCK	42,47

Table 450: DDR5 5600-6400: Data Strobe Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential WRITE preamble (2tCK preamble)	t_{WPRE2}	-	-	-	-	-	-	t _{CK} (avg)	37,47
DQS_t, DQS_c differential WRITE preamble (3tCK preamble)	t_{WPRE3}	2.700	-	2.700	-	2.700	-	t _{CK} (avg)	38,47
DQS_t, DQS_c differential WRITE preamble (4tCK preamble)	t_{WPRE4}	3.600	-	3.600	-	3.600	-	t _{CK} (avg)	40,47
DQS_t, DQS_c differential initial low pulse width during preamble (2tCK Ppreamble)	$t_{DQSL2PRE}$	-	-	-	-	-	-	t _{CK} (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (3tCK preamble)	$t_{DQSL3PRE}$	1.800	-	1.800	-	1.800	-	t _{CK} (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (4tCK preamble)	$t_{DQSL4PRE}$	1.800	-	1.800	-	1.800	-	t _{CK} (avg)	
DQS_t, DQS_c differential WRITE postamble - 0.5tCK	$t_{WPST0.5}$	-	-	-	-	-	-	t _{CK} (avg)	41,47
DQS_t, DQS_c differential WRITE postamble - 1.5tCK	$t_{WPST1.5}$	1.200	-	1.200	-	1.200	-	t _{CK} (avg)	42,47
DQS_t, DQS_c differential high toggle pulse width during DDR4 2tCK READ preamble	$t_{DQSH2PRE\_D4}$	-	-	-	-	-	-	t _{CK}	
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	t_{DQSH_pre}	0.430	0.570	0.430	0.570	0.430	0.570	t _{CK} (avg)	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	t_{DQSL_pre}	0.430	0.570	0.430	0.570	0.430	0.570	t _{CK} (avg)	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	t_{DQSCK}	-0.325	0.325	-0.337	0.337	-0.348	0.348	t _{CK}	6,9,16
DQS_t, DQS_c rising edge output variance window	t_{DQSCKi}	-	0.530	-	0.549	-	0.567	t _{CK}	7,8,9,16,33

Table 451: DDR5 5600-6400: Write Enable Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2·t _{CK} WRITE preamble enable window	$t_{WPRE\_EN\_2tCK}$	1.5	-	1.5	-	1.5	-	t _{CK}	
3·t _{CK} WRITE preamble enable window	$t_{WPRE\_EN\_3tCK}$	2.5	-	2.5	-	2.5	-	t _{CK}	
4·t _{CK} WRITE preamble enable window	$t_{WPRE\_EN\_4tCK}$	2.5	-	2.5	-	2.5	-	t _{CK}	
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	$t_{DQSoffset}$	-0.5	0.5	-0.5	0.5	-0.5	0.5	t _{CK}	26
Write leveling setup time	t_{WLS}	-80	80	-80	80	-80	80	ps	
Write leveling hold time	t_{WLH}	-80	80	-80	80	-80	80	ps	

Table 451: DDR5 5600-6400: Write Enable Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Voltage/temperature drift window of first rising DQS _t preamble edge relative to CWL CK _t -CK _c edge (x4/x8/x16)	t _{DQSD}	-0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	-0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	-0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	t _{CK}	5
Host and system voltage/temperature drift window of first rising DQS _t preamble edge relative to CWL CK _t -CK _c edge (x4/x8/x16)	t _{DQSS}	-0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	-0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	-0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	0.25 x t _{WPRE_E} N _n t _{CK} (MIN)	t _{CK}	5,32

Table 452: DDR5 5600-6400: Dynamic ODT Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RTT change skew timing - transitioning from one valid RTT state to the next valid RTT state	t _{ADC}	0.20	0.80	0.18	0.82	0.16	0.84	t _{CK} (avg)	45,46

Table 453: DDR5 5600-6400: MPSM Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	t _{MPSMX}	t _{MRD}	-	t _{MRD}	-	t _{MRD}	-	ns	

Table 454: DDR5 5600-6400: ZQ Calibration Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	t _{ZQCAL}	1		1		1		μs	
ZQ calibration latch time	t _{ZQLAT}	max(30ns, 8nCK)		max(30ns, 8nCK)		max(30ns, 8nCK)			

Table 455: DDR5 5600-6400: Reset Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET _n low time for reset initialization with stable power	t _{PW_RESET}	1	-	1	-	1	-	μs	
Time after RESET _n assertion to ODT off	t _{RST_ADC}	-	50	-	50	-	50	ns	

Table 456: DDR5 5600-6400: Self Refresh Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t _{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		
Self refresh CS _n low pulse width	t _{CSL}	10	-	10	-	10	-	ns	
Self refresh exit CS _n high pulse width	t _{CSH_SRexit}	13	200	13	200	13	200	ns	

Table 456: DDR5 5600-6400: Self Refresh Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Self refresh exit CS_n low pulse width	t_{CS_SRExit}	3nCK	30ns	3nCK	30ns	3nCK	30ns		11
Self refresh exit CS_n low pulse width with frequency change	$t_{CS\_FreqChg}$	VREFCA_time	-	VREFCA_time	-	VREFCA_time	-	ns	12
Valid clock requirement before SRX	t_{CKSRX}	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-		
Valid clock requirement after SRE	t_{CKLCS}	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	nCK, ns	
Self refresh exit CS_n HIGH	t_{CASRX}	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC1}	-	t_{RFC1}	-	t_{RFC1}	-	ns	
Exit self refresh to commands requiring a locked DLL	t_{XS_DLL}	t_{DLLK}	-	t_{DLLK}	-	t_{DLLK}	-	nCK	

Table 457: DDR5 5600-6400: Power-Down Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t_{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	ns	
Power-down duration	t_{PD}	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	ns	28,44
Power-down exit command to next valid command (excluding NT ODT commands when PDE with CA11=L)	t_{XP}	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)		ns	
ACTIVATE command to POWER-DOWN ENTRY command	$t_{ACTPDEN}$	2	-	2	-	2	-	nCK	13
PRECHARGE, PRECHARGE ALL, or PRECHARGE SAME BANK command to POWER-DOWN ENTRY command	t_{PRPDEN}	2	-	2	-	2	-	nCK	13
READ or READ w/ AUTO PRECHARGE command to POWER-DOWN ENTRY command	t_{RDPDEN}	CL+RBL/2+1	-	CL+RBL/2+1	-	CL+RBL/2+1	-	nCK	24, 30
WRITE command to POWER-DOWN ENTRY command	t_{WRPDEN}	CWL+WBL/2+WR+1	-	CWL+WBL/2+WR+1	-	CWL+WBL/2+WR+1	-	nCK	14, 24,31
WRITE w/ AUTO PRECHARGE command to POWER-DOWN ENTRY command	$t_{WRAPDEN}$	CWL+WBL/2+ $t_{WR}+1$		CWL+WBL/2+ $t_{WR}+1$		CWL+WBL/2+ $t_{WR}+1$		nCK	14, 15, 24,31

Table 457: DDR5 5600-6400: Power-Down Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
REFRESH ALL or REFRESH SAME BANK command to POWER-DOWN ENTRY command	t_{REFPDEN}	2	-	2	-	2	-	nCK	
MRR command to POWER-DOWN ENTRY command	t_{MRRPDEN}	CL+8+1	-	CL+8+1	-	CL+8+1	-	nCK	24
MRW command to POWER-DOWN ENTRY command	t_{MRWPDEN}	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	nCK	
MPC command to POWER-DOWN ENTRY command	t_{MPCPDEN}	$t_{\text{MPC\_delay}}$	-	$t_{\text{MPC\_delay}}$	-	$t_{\text{MPC\_delay}}$	-	nCK	25

Table 458: DDR5 5600-6400: MPC Command Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	$t_{\text{MPC\_Delay}}$	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	$t_{\text{MC\_MPC\_Setup}}$	3	-	3	-	3	-	nCK	21
Time between first rising CS edge and stable MPC command (HOLD)	$t_{\text{MC\_MPC\_Hold}}$	3	-	3	-	3	-	nCK	21
Time CS _n is held LOW to register MPC command	$t_{\text{MPC\_CS}}$	3.5	8	3.5	8	3.5	8	nCK	20

Table 459: DDR5 5600-6400: PDA Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle time	$t_{\text{PDA\_DELAY\_1}}$	$t_{\text{PDA\_DQS\_DELAY,max}} + \text{BL}/2 + 19\text{ns}$	-	$t_{\text{PDA\_DQS\_DELAY,max}} + \text{BL}/2 + 19\text{ns}$	-	$t_{\text{PDA\_DQS\_DELAY,max}} + \text{BL}/2 + 19\text{ns}$	-	nCK,ns	
PDA ENUMERATE ID command to any other command cycle time for multi-device continuous DQS toggle mode	$t_{\text{PDA\_DELAY\_2}}$	$t_{\text{PDA\_DELAY\_1}} + t_{\text{MPC\_DELAY}}$ (MIN)	-	$t_{\text{PDA\_DELAY\_1}} + t_{\text{MPC\_DELAY}}$ (MIN)	-	$t_{\text{PDA\_DELAY\_1}} + t_{\text{MPC\_DELAY}}$ (MIN)	-	nCK,ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	$t_{\text{PDA\_DQS\_DELAY}}$	5	18	5	18	5	18	ns	4
Delay to falling DQ edge during PDA operation	$t_{\text{PDA\_DQ\_DELAY\_1}}$	$t_{\text{PDA\_DQS\_DELAY,min}} + t_{\text{PDA\_S\_FALL}}$ (MIN)	$t_{\text{PDA\_DQS\_D\_DELAY}} + t_{\text{PDA\_S\_FALL}}$ (MAX)- $t_{\text{PDA\_S\_FALL}}$ (MIN)	$t_{\text{PDA\_DQS\_DELAY,min}} + t_{\text{PDA\_S\_FALL}}$ (MIN)	$t_{\text{PDA\_DQS\_D\_DELAY}} + t_{\text{PDA\_S\_FALL}}$ (MAX)- $t_{\text{PDA\_S\_FALL}}$ (MIN)	$t_{\text{PDA\_DQS\_DELAY,min}} + t_{\text{PDA\_S\_FALL}}$ (MIN)	$t_{\text{PDA\_DQS\_D\_DELAY}} + t_{\text{PDA\_S\_FALL}}$ (MAX)- $t_{\text{PDA\_S\_FALL}}$ (MIN)	nCK,ns	
Delay to rising DQ edge during PDA operation	$t_{\text{PDA\_DQ\_DELAY\_2}}$	$t_{\text{PDA\_DELAY\_1}}$ (MIN)	-	$t_{\text{PDA\_DELAY\_1}}$ (MIN)	-	$t_{\text{PDA\_DELAY\_1}}$ (MIN)	-	nCK,ns	

Table 459: DDR5 5600-6400: PDA Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay after last DQS toggle used for sampling DQ during PDA	$t_{PDA\_DQS\_STOP}$	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	nCK,ns	
Delay after last DQ toggle used for sampling DQ during PDA	$t_{PDA\_DQ\_STOP}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	nCK,ns	
Falling DQ edge setup time during PDA operation	$t_{PDA\_S\_FALL}$	max(3nCK, 1.250ns)	-	max(3nCK, 1.250ns)	-	max(3nCK, 1.250ns)	-	nCK,ns	
Rising DQ edge hold time during PDA operation	$t_{PDA\_H\_RISE}$	max(3nCK, 1.250ns)	-	max(3nCK, 1.250ns)	-	max(3nCK, 1.250ns)	-	nCK,ns	
Rising DQ edge setup time during PDA operation	$t_{PDA\_S\_RISE}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	nCK,ns	
Falling DQ edge hold time during PDA operation	$t_{PDA\_H\_FALL}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	nCK,ns	

Table 460: DDR5 5600-6400: Read Training Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	$t_{Cont\_Exit\_Delay}$	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	-	
Registration of MRW continuous burst mode exit to end of training mode	t_{Cont_Exit}	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	
Maximum delay between first exit continuous burst mode MRW command and the second exit continuous burst mode MRW command	t_{CBME}	-	CL-10nCK	-	CL-10nCK	-	CL-10nCK	-	

Table 461: DDR5 5600-6400: Read Preamble Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	t_{SDOn}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		
Delay from MRW command to DQS disabled	t_{SDOff}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		

Table 462: DDR5 5600-6400: CA Training Mode Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	t_{CATM_Entry}	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	t_{CATM_Exit}	-	14	-	14	-	14	ns	

Table 462: DDR5 5600-6400: CA Training Mode Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM exit to next valid command delay	$t_{\text{CATM\_Exit\_Delay}}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	$t_{\text{CATM\_Valid}}$	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{\text{CATM\_DQ\_Window}}$	2	-	2	-	2	-	nCK	27
CS_n assertion duration to exit CATM	$t_{\text{CATM\_CS\_Exit}}$	2	8	2	8	2	8	nCK	

Table 463: DDR5 5600-6400: CS Training Mode Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	$t_{\text{CSTM\_Entry}}$	20	-	20	-	20	-	ns	
Registration of CSTM exit command to end of training mode	$t_{\text{CSTM\_Exit}}$	-	20	-	20	-	20	ns	
Registration of CSTM exit to next valid command delay	$t_{\text{CSTM\_Exit\_Delay}}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	$t_{\text{CSTM\_Valid}}$	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{\text{CSTM\_DQ\_Window}}$	2	-	2	-	2	-	nCK	27
Min time between last CS_n pulse and first pulse of MPC command to exit CSTM	$t_{\text{CSTM\_Min\_to\_MPC\_exit}}$	4	-	4	-	4	-	nCK	

Table 464: DDR5 5600-6400: Write Leveling Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	$t_{\text{WLPE}}N$	-	15	-	15	-	15	ns	
Write leveling output delay	t_{WLO}	-	9.5	-	9.5	-	9.5	ns	
Width of write leveling internal pulse	$t_{\text{WL\_Pulse\_Width}}$	2	-	2	-	2	-	tCK	17
Write leveling write to subsequent command spacing	$t_{\text{WL\_Write}}$	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-		

Table 465: DDR5 5600-6400: V_{REFCA} / V_{REFCS} Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{REFCA} command to any other valid command delay	$t_{\text{VREFCA\_Delay}}$	tMRD	-	tMRD	-	tMRD	-	nCK	
V_{REFCS} command to any other valid command delay	$t_{\text{VREFCS\_Delay}}$	tMRD	-	tMRD	-	tMRD	-	nCK	

Table 465: DDR5 5600-6400: VREFCA/VREFCS Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Time CS _n is held LOW to register VREFCA command	t_{VREFCA_CS}	3.5	8	3.5	8	3.5	8	nCK	18,19
Time CS _n is held LOW to register VREFCS command	t_{VREFCS_CS}	3.5	8	3.5	8	3.5	8	nCK	18,19
MIN time between stable VREFCA command and first falling CS edge (SETUP)	$t_{MC\_VREFCA\_Setup}$	3	-	3	-	3	-	nCK	10
MIN time between first rising CS edge and stable VREFCA command (HOLD)	$t_{MC\_VREFCA\_Hold}$	3	-	3	-	3	-	nCK	10
MIN time between stable VREFCS command and first falling CS edge (SETUP)	$t_{MC\_VREFCS\_Setup}$	3	-	3	-	3	-	nCK	10
MIN time between first rising CS edge and stable VREFCS command (HOLD)	$t_{MC\_VREFCS\_Hold}$	3	-	3	-	3	-	nCK	10

Table 466: DDR5 5600-6400: hPPR/sPPR Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	t_{PGM_hPPRa}	1000	-	1000	-	1000	-	ms	
hPPR programming time (x16)	t_{PGM_hPPRb}	2000	-	2000	-	2000	-	ms	
sPPR programming time	t_{PGM_sPPR}	CWL +8 t_{CK} + t_{WR}		CWL +8 t_{CK} + t_{WR}		CWL +8 t_{CK} + t_{WR}		t_{CK}	
hPPR/sPPR exit recognition time	t_{PGM_Exit}	t_{RP}	-	t_{RP}	-	t_{RP}	-	ns	
hPPR program exit and new address setting time	t_{PGMPST}	50	-	50	-	50	-	μs	
sPPR program exit and new address setting time	t_{PGMPST_sPPR}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	ns	

Table 467: DDR5 5600-6400: DQS Interval Oscillator Readout Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	t_{OSCOM}	t_{MPC_Delay}	-	t_{MPC_Delay}	-	t_{MPC_Delay}	-	nCK	23
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	t_{OSCOA}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	23
DQS interval oscillator start gap in automatic stop mode	t_{OSCS}	t_{MPC_Delay} + DQS interval timer run time						nCK	23,43

Table 468: DDR5 5600-6400: ESC Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	t_{ECSc}	max(76nCK ,110ns)	-	max(176nCK ,110ns)	-	max(176nCK ,110ns)	-		

Table 469: DDR5 5600-6400: CRC Error Reporting Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT n_latency	$t_{\text{CRC\_ALERT}}$	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	nCK	

Timing Parameters for DDR5 6800-7600

Analog timing parameters are to be rounded to 1ps of accuracy. Parameter minimum values, which scale with t_{CK} (MIN), are to be defined using the t_{CK} (MIN) in the associated data rate.

Table 470: DDR5 6800-7600: Clock Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{\text{CK,AVG}}$	0.294		0.277	–	0.263	–	ns	22

Table 471: DDR5 6800-7600: Command and Address Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
READ to READ command delay for same bank, in same bank group	$t_{\text{CCD\_L}}$	$\max(\text{RBL}/2, 5\text{ns})$							43
READ to READ command delay for different bank, in same bank group	$t_{\text{CCD\_M}}$	$\max(8n\text{CK}, 4.705\text{ns})$	–	$\max(8n\text{CK}, 4.444\text{ns})$	–	$\max(8n\text{CK}, 4.210\text{ns})$	–		43
WRITE to WRITE command delay for same bank, in same bank group	$t_{\text{CCD\_L\_WR}}$	$\max(32n\text{CK}, 20\text{ns})$							43
WRITE to WRITE command delay for different bank, in same bank group	$t_{\text{CCD\_M\_WR}}$	$\max(32n\text{CK}, 18.823\text{ns})$	–	$\max(32n\text{CK}, 17.777\text{ns})$ [$\max(32n\text{CK}, 17.22\text{ns})$]	–	$\max(32n\text{CK}, 16.842\text{ns})$	–		43
WRITE to WRITE command delay for same bank group, second WRITE not RMW	$t_{\text{CCD\_L\_WR2}}$	$\max(16n\text{CK}, 10\text{ns})$							43
READ to WRITE command delay for same bank group	$t_{\text{CCD\_L\_RTW}}$	$\text{CL} - \text{CWL} + \text{RBL}/2 + 2t_{\text{CK}} - (\text{Read DQS offset}) + (t_{\text{RPST}} - 0.5t_{\text{CK}}) + t_{\text{WPRE}}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for same bank, in same bank group	$t_{\text{CCD\_L\_WTR}}$	$\text{CWL} + \text{WBL}/2 + \max(16n\text{CK}, 10\text{ns})$						nCK, ns	29,31, 43
WRITE to READ command delay for different bank, in same bank group	$t_{\text{CCD\_M\_WTR}}$	$\text{CWL} + \text{WBL}/2 + \max(16n\text{CK}, 9.411\text{ns})$	–	$\text{CWL} + \text{WBL}/2 + \max(16n\text{CK}, 8.888\text{ns})$	–	$\text{CWL} + \text{WBL}/2 + \max(16n\text{CK}, 8.421\text{ns})$	–	nCK, ns	29,31
READ to READ command delay for different bank group	$t_{\text{CCD\_S}}$	$\text{RBL}/2$						nCK	43

Table 471: DDR5 6800-7600: Command and Address Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
WRITE to WRITE command delay for different bank group	$t_{CCD\_S\_WR}$	WBL/2						nCK	43
READ to WRITE command delay for different bank group	$t_{CCD\_S\_RTW}$	CL - CWL + RBL/2 + 2tCK - (Read DQS offset)+ (t_{RPST} - 0.5tCK) + t_{WPRE}						nCK,ns	29,30, 35,43
WRITE to READ command delay for different bank group	$t_{CCD\_S\_WTR}$	CWL + WBL/2 + max(4nCK, 2.352ns)	-	CWL + WBL/2 + max(4nCK, 2.222ns)	-	CWL + WBL/2 + max(4nCK , 2.105ns)	-	nCK, nsCK	29,31, 43
WRITE to READ with AUTO PRECHARGE command for same bank	t_{CCD_WTRA}	CWL + WBL/2 + t_{WR} - t_{RTP}						nCK, ns	29,31, 34,43
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	$t_{RRD\_L,1K}$	max(8nCK, 4.705ns)	-	max(8nCK, 4.444ns)	-	max(8nCK , 4.210ns)	-	nCK, ns	43
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	$t_{RRD\_L,2K}$	max(8nCK, 4.705ns)	-	max(8nCK, 4.444ns)	-	max(8nCK , 4.210ns)	-	nCK, ns	43
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	$t_{RRD\_S,1K}$	8						nCK	42
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	$t_{RRD\_S,2K}$	8						nCK	42
Four activate window for 2KB page size	$t_{FAW,2K}$	MAX(40nCK, 11.764ns)	-	MAX(40nCK, 11.111ns)	-	MAX (32nCK,10 .526ns)	-	nCK, ns	
Four activate window for 1KB page size	$t_{FAW,1K}$	MAX (32nCK,9.41 1ns)	-	MAX (32nCK,8.88 8ns	-	MAX (32nCK,8. 421ns)	-	nCK, ns	
READ command to PRECHARGE command delay	t_{RTP}	MAX(12nCK, 7.5ns)							43
PRECHARGE to PRECHARGE command delay	t_{PPD}	2			4	4	4	nCK	36,43
WRITE recovery time	t_{WR}	30						ns	1,43
DLL locking time	t_{DLLK}	2048	-	2304	-	TBD	-	nCK	

Table 472: DDR5 6800-7600: Mode Register Read/Write Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	t_{MRR}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		2
Mode register READ pattern to mode register READ pattern command spacing	t_{MRR_p}	8	-	8	-	8	-	nCK	

Table 472: DDR5 6800-7600: Mode Register Read/Write Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register WRITE command period	t_{MRW}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		2
Mode register SET command delay	t_{MRD}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		
DFE mode register WRITE update delay time	t_{DFE}	80	-	80	-	80	-	ns	3

Table 473: DDR5 6800-7600: Data Strobe Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ preamble (1tCK preamble)	t_{RPRE1}	-	-	-	-	-	-	t_{CK}	47,48
DQS_t, DQS_c differential READ preamble (2tCK preamble)	t_{RPRE2}	1.800	-	1.800	-	1.800	-	t_{CK}	37,47
DQS_t, DQS_c differential READ preamble DDR4 (2tCK preamble)	t_{RPRE2_D4}	-	-	-	-	-	-	t_{CK}	37,47
DQS_t, DQS_c differential READ preamble (3tCK preamble)	t_{RPRE3}	-	-	-	-	-	-	t_{CK}	38,47
DQS_t, DQS_c differential READ preamble (4tCK preamble)	t_{RPRE4}	3.600	-	3.600	-	3.600	-	t_{CK}	39,47
DQS_t, DQS_c differential READ postamble - 0.5tCK	$t_{RPST0.5}$	0.450	-	0.450	-	0.450	-	t_{CK}	41,47
DQS_t, DQS_c differential READ postamble - 1.5tCK	$t_{RPST1.5}$	1.200	-	1.200	-	1.300	-	t_{CK}	42,47
DQS_t, DQS_c differential WRITE preamble (2tCK preamble)	t_{WPRE2}	-	-	-	-	-	-	t_{CK} (avg)	37,47
DQS_t, DQS_c differential WRITE preamble (3tCK preamble)	t_{WPRE3}	-	-	-	-	-	-	t_{CK} (avg)	38,47
DQS_t, DQS_c differential WRITE preamble (4tCK preamble)	t_{WPRE4}	3.600	-	3.600	-	3.600	-	t_{CK} (avg)	40,47
DQS_t, DQS_c differential high toggle pulse width during DDR4 2tCK READ preamble	$t_{DQSH2PRE\_D4}$	-	-	-	-	-	-	t_{CK}	
DQS_t, DQS_c differential initial low pulse width during preamble (2tCK preamble)	$t_{DQSL2PRE}$	-	-	-	-	-	-	t_{CK} (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (3tCK preamble)	$t_{DQSL3PRE}$	-	-	-	-	-	-	t_{CK} (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (4tCK preamble)	$t_{DQSL4PRE}$	1.800	-	1.800	-	1.800	-	t_{CK} (avg)	
DQS_t, DQS_c differential WRITE postamble - 0.5tCK	$t_{WPST0.5}$	-	-	-	-	-	-	t_{CK} (avg)	41,47
DQS_t, DQS_c differential WRITE postamble - 1.5tCK	$t_{WPST1.5}$	1.200	-	1.200	-	1.200	-	t_{CK} (avg)	42,47
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	t_{DQSH_pre}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK} (avg)	

Table 473: DDR5 6800-7600: Data Strobe Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	t_{DQSL_pre}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK} (avg)	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	t_{DQSCK}	-0.359	0.359	-0.370	0.370	-0.380	0.380	t_{CK}	6,9,16
DQS_t, DQS_c rising edge output variance window	t_{DQSCKi}	-	0.585	-	0.602	-	0.619	t_{CK}	7,8,9,16,33

Table 474: DDR5 6800-7600: Write Enable Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2- t_{CK} WRITE preamble enable window	$t_{WP\_EN\_2t_{CK}}$	1.5	-	1.5	-	1.5	-	t_{CK}	
3- t_{CK} WRITE preamble enable window	$t_{WP\_EN\_3t_{CK}}$	2.5	-	2.5	-	2.5	-	t_{CK}	
4- t_{CK} WRITE preamble enable window	$t_{WP\_EN\_4t_{CK}}$	2.5	-	2.5	-	2.5	-	t_{CK}	
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	$t_{DQSo\text{ffset}}$	-0.5	0.5	-0.5	0.5	-0.5	0.5	t_{CK}	26
Write leveling setup time	t_{WLS}	-80	80	-80	80	-80	80	ps	
Write leveling hold time	t_{WLH}	-80	80	-80	80	-80	80	ps	
Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	t_{DQSD}	-0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	-0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	-0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	t_{CK}	5
Host and system voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16)	t_{DQSS}	-0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	-0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	-0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	0.25 x $t_{WP\_E\ N\_n t_{CK}}$ (MIN)	t_{CK}	5,32

Table 475: DDR5 6800-7600: Dynamic ODT Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RTT change skew timing - transitioning from onevalid RTT state to the nextvalid RTT state	t_{ADC}	0.14	0.86	0.12	0.88	0.10	0.90	t_{CK} (avg)	45,46

Table 476: DDR5 6800-7600: MPSM Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	t_{MPSMX}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	ns	

Table 477: DDR5 6800-7600: ZQ Calibration Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	t_{ZQCAL}	1		1		1		μs	
ZQ calibration latch time	t_{ZQLAT}	max(30ns, 8nCK)		max(30ns, 8nCK)		max(30ns, 8nCK)			

Table 478: DDR5 6800-7600: Reset Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET_n low time for reset initialization with stable power	t_{PW_RESET}	1	-	1	-	1	-	μs	
Time after RESET_n assertion to ODT off	t_{RST_ADC}	-	50	-	50	-	50	ns	

Table 479: DDR5 6800-7600: Self Refresh Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t_{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	nCK, ns	
Self refresh CS_n low pulse width	t_{CSL}	10	-	10	-	10	-	ns	
Self refresh exit CS_n high pulse width	t_{CSH_SExit}	13	200	13	200	13	200	ns	
Self refresh exit CS_n low pulse width	t_{CSL_SExit}	3nCK	30ns	3nCK	30ns	3nCK	30ns	nCK, ns	11
Self refresh exit CS_n low pulse width with frequency change	$t_{CSL\_FreqChg}$	VREFCA_time	-	VREFCA_time	-	VREFCA_time	-	ns	12
Valid clock requirement before SRX	t_{CKSRX}	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-	nCK, ns	
Valid clock requirement after SRE	t_{CKLCS}	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	nCK, ns	
Self refresh exit CS_n HIGH	t_{CASRX}	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC1}	-	t_{RFC1}	-	t_{RFC1}	-	ns	
Exit self refresh to commands requiring a locked DLL	t_{XS_DLL}	t_{DLLK}	-	t_{DLLK}	-	t_{DLLK}	-	nCK	

Table 480: DDR5 6800-7600: Power-Down Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t_{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	ns	
Power-down duration	t_{PD}	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	ns	28,44

Table 480: DDR5 6800-7600: Power-Down Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Power-down exit command to next valid command (excluding NT ODT commands when PDE with CA11=L)	t_{XP}	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)		ns	
ACTIVATE command to POWER-DOWN ENTRY command	$t_{ACTPDEN}$	2	-	2	-	2	-	nCK	13
PRECHARGE, PRECHARGE ALL, or PRECHARGE SAME BANK command to POWER-DOWN ENTRY command	t_{PRPDEN}	2	-	2	-	2	-	nCK	13
READ or READ w/ AUTO PRECHARGE command to POWER-DOWN ENTRY command	t_{RDPDEN}	CL+RBL/2+1	-	CL+RBL/2+1	-	CL+RBL/2+1	-	nCK	24, 30
WRITE command to POWER-DOWN ENTRY command	t_{WRPDEN}	CWL+WBL/2+WR+1	-	CWL+WBL/2+WR+1	-	CWL+WBL/2+WR+1	-	nCK	14, 24,31
WRITE w/ AUTO PRECHARGE command to POWER-DOWN ENTRY command	$t_{WRAPDEN}$	CWL+WBL/2+ $t_{WR}+1$		CWL+WBL/2+ $t_{WR}+1$		CWL+WBL/2+ $t_{WR}+1$		nCK	14, 15, 24,31
REFRESH ALL or REFRESH SAME BANK command to POWER-DOWN ENTRY command	$t_{REFPDEN}$	2	-	2	-	2	-	nCK	
MRR command to POWER-DOWN ENTRY command	$t_{MRRPDEN}$	CL+8+1	-	CL+8+1	-	CL+8+1	-	nCK	24
MRW command to POWER-DOWN ENTRY command	$t_{MRWPDEN}$	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	nCK	
Timing of MPC command to POWER-DOWN ENTRY command	$t_{MPCPDEN}$	t_{MPC_delay}	-	t_{MPC_delay}	-	t_{MPC_delay}	-	nCK	25

Table 481: DDR5 6800-7600: MPC Command Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	t_{MPC_Delay}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	$t_{MC\_MPC\_Setup}$	3	-	3	-	3	-	nCK	21
Time between first rising CS edge and stable MPC command (HOLD)	$t_{MC\_MPC\_Hold}$	3	-	3	-	3	-	nCK	21
Time CS_n is held LOW to register MPC command	t_{MPC_CS}	3.5	8	3.5	8	3.5	8	nCK	20

Table 482: DDR5 6800-7600: PDA Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle time	$t_{PDA\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY} (MAX) BL/2 + 19ns$	-	$t_{PDA\_DQS\_DELAY} (MAX) BL/2 + 19ns$	-	$t_{PDA\_DQS\_DELAY} (MAX) BL/2 + 19ns$	-	nCK,ns	
PDA ENUMERATE ID command to any other command cycle time for multi-device continuous DQS toggle mode	$t_{PDA\_DELAY\_2}$	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} (MIN)$	-	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} (MIN)$	-	$t_{PDA\_DELAY\_1} + t_{MPC\_DELAY} (MIN)$	-	nCK,ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	$t_{PDA\_DQS\_DELAY}$	5	18	5	18	5	18	ns	4
Delay to falling DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY} (MIN) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MAX) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MIN) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MAX) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MIN) - t_{PDA\_S\_FALL} (MIN)$	$t_{PDA\_DQS\_DELAY} (MAX) - t_{PDA\_S\_FALL} (MIN)$	nCK,ns	
Delay to rising DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_2}$	$t_{PDA\_DELAY\_1} (MIN)$	-	$t_{PDA\_DELAY\_1} (MIN)$	-	$t_{PDA\_DELAY\_1} (MIN)$	-	nCK,ns	
Delay after last DQStoggle used for sampling DQ during PDA	$t_{PDA\_DQS\_STOP}$	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	$t_{MPC\_DELAY} (MIN) + t_{PDA\_H\_RISE} (MIN)$	-	nCK,ns	
Delay after last DQ toggle used for sampling DQ during PDA	$t_{PDA\_DQ\_STOP}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	nCK,ns	
Falling DQ edge setup time during PDA operation	$t_{PDA\_S\_FALL}$	MAX (3nCK, 1.250ns)	-	MAX (3nCK, 1.250ns)	-	MAX (3nCK, 1.250ns)	-		
Rising DQ edge hold time during PDA operation	$t_{PDA\_H\_RISE}$	MAX (3nCK, 1.250ns)	-	MAX (3nCK, 1.250ns)	-	MAX (3nCK, 1.250ns)	-		
Rising DQ edge setup time during PDA operation	$t_{PDA\_S\_RISE}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-		
Falling DQ edge hold time during PDA operation	$t_{PDA\_H\_FALL}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-		

Table 483: DDR5 6800-7600: Read Training Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	$t_{Cont\_Exit\_Delay}$	$t_{Cont\_Exit} + t_{MRW}$	-	$t_{Cont\_Exit} + t_{MRW}$	-	$t_{Cont\_Exit} + t_{MRW}$	-	-	
Registration of MRW continuous burst mode exit to end of training mode	t_{Cont_Exit}	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	

Table 483: DDR5 6800-7600: Read Training Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Maximum delay between first exit continuous burst mode MRW command and the second exit continuous burst mode MRW command	t_{CBME}	-	CL - 10nCK	-	CL - 10nCK	-	CL - 10nCK	-	

Table 484: DDR5 6800-7600: Read Preamble Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	t_{SDOn}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		
Delay from MRW command to DQS disabled	t_{SDOff}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		

Table 485: DDR5 6800-7600: CA Training Mode Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	t_{CATM_Entry}	20	-	20	-	20	-	ns	
Registration of CATM exit CS _n assertion to end of training mode (when DQ is no longer driven by the device).	t_{CATM_Exit}	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	$t_{CATM\_Exit\_Delay}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	t_{CATM_Valid}	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{CATM\_DQ\_Window}$	2	-	2	-	2	-	nCK	27
CS _n assertion duration to exit CATM	$t_{CATM\_CS\_Exit}$	2	8	2	8	2	8	nCK	

Table 486: DDR5 6800-7600: CS Training Mode Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	t_{CSTM_Entry}	20	-	20	-	20	-	ns	
Min time between last CS _n pulse and first pulse of MPC command to exit CSTM	$t_{CSTM\_Min\_to\_MPC\_exit}$	4	-	4	-	4	-	nCK	
Registration of CSTM exit command to end of training mode	t_{CSTM_Exit}	-	20	-	20	-	20	ns	
Time from sample evaluation to output on DQ bus	t_{CSTM_Valid}	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{CSTM\_DQ\_Window}$	2	-	2	-	2	-	nCK	27
Registration of CSTM exit to next valid command delay	$t_{CSTM\_Exit\_Delay}$	20	-	20	-	20	-	ns	

Table 487: DDR5 6800-7600: Write Leveling Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	t_{WLPEN}	–	15	–	15	–	15	ns	
Write leveling output delay	t_{WLO}	–	9.5	–	9.5	–	9.5	ns	
Width of write leveling internal pulse	$t_{WL\_Pulse\_Width}$	2	–	2	–	2	–	t_{CK}	17
Write leveling write to subsequent command spacing	t_{WL_Write}	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	–	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	–	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	–		

Table 488: DDR5 6800-7600: V_{REFCA}/V_{REFCS} Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
VREFCA command to any other valid command delay	t_{VREFCA_Delay}	t_{MRD}	–	t_{MRD}	–	t_{MRD}	–	nCK	
VREFCS command to any other valid command delay	t_{VREFCS_Delay}	t_{MRD}	–	t_{MRD}	–	t_{MRD}	–	nCK	
Time CS_n is held LOW to register VREFCA command	t_{VREFCA_CS}	3.5	8	3.5	8	3.5	8	nCK	18,19
Time CS_n is held LOW to register VREFCS command	t_{VREFCS_CS}	3.5	8	3.5	8	3.5	8	nCK	18,19
MIN time between stable VREFCA command and first falling CS edge (SETUP)	$t_{MC\_VREFCA\_Setup}$	3	–	3	–	3	–	nCK	10
MIN time between first rising CS edge and stable VREFCA command (HOLD)	$t_{MC\_VREFCA\_Hold}$	3	–	3	–	3	–	nCK	10
MIN time between stable VREFCS command and first falling CS edge (SETUP)	$t_{MC\_VREFCS\_Setup}$	3	–	3	–	3	–	nCK	10
MIN time between first rising CS edge and stable VREFCS command (HOLD)	$t_{MC\_VREFCS\_Hold}$	3	–	3	–	3	–	nCK	10

Table 489: DDR5 6800-7600: hPPR/sPPR Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	t_{PGM_hPPRa}	1000	–	1000	–	1000	–	ms	
hPPR programming time (x16)	t_{PGM_hPPRb}	2000	–	2000	–	2000	–	ms	
hPPR program exit and new address setting time	t_{PGMPST}	50	–	50	–	50	–	μs	
sPPR programming time	t_{PGM_sPPR}	CWL+8 t_{CK} + t_{WR}		CWL+8 t_{CK} + t_{WR}		CWL+8 t_{CK} + t_{WR}		t_{CK}	
sPPR program exit and new address setting time	t_{PGMPST_sPPR}	t_{MRD}	–	t_{MRD}	–	t_{MRD}	–	ns	
hPPR/sPPR exit recognition time	t_{PGM_Exit}	t_{RP}	–	t_{RP}	–	t_{RP}	–	ns	

Table 490: DDR5 6800-7600: DQS Interval Oscillator Readout Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	t_{OSCOM}	t_{MPC_Delay}	-	t_{MPC_Delay}	-	t_{MPC_Delay}	-	nCK	23
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	t_{OSCOA}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	23
DQS interval oscillator start gap in automatic stop mode	t_{OSCS}	t_{MPC_Delay} + DQS interval timer run time						nCK	23,43

Table 491: DDR5 6800-7600: ESC Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	t_{ECSc}	max(176nCK, 110ns)	-	max(176nCK, 110ns)	-	max(176nCK, 110ns)	-		

Table 492: DDR5 6800-7600: CRC Error Reporting Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT n_latency	t_{CRC_ALERT}	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	nCK	

Timing Parameters for DDR5 8000-8800

Analog timing parameters are to be rounded to 1ps of accuracy. Parameter minimum values, which scale with t_{CK} (MIN), are to be defined using the t_{CK} (MIN) in the associated data rate.

Table 493: DDR5 8000-8800: Clock Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.250		0.238	-	0.227	-	ns	22

Table 494: DDR5 8000-8800: Command and Address Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
READ to READ command delay for same bank, same bank group	t_{CCD_L}	max(RBL/2, 5ns)						nCK, ns	43
READ to READ command delay for different bank, to same bank group	t_{CCD_M}	max(8nCK, 4.000ns)	-	max(8nCK, 4.000ns)	-	max(8nCK, 3.863ns)	-	nCK, ns	43
WRITE to WRITE command delay for same bank, to same bank group	$t_{CCD\_L\_WR}$	max(32nCK, 20ns)						nCK, ns	43
WRITE to WRITE command delay for different bank, to same bank group	$t_{CCD\_M\_WR}$	max(32nCK, 16.000ns)	-	max(32nCK, 15.238ns)	-	max(32nCK, 14.545ns)	-	nCK, ns	

Table 494: DDR5 8000-8800: Command and Address Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
WRITE to WRITE command delay for same bank group, second WRITE not RMW	$t_{CCD\_L\_WR2}$	$\max(16nCK, 10ns)$						nCK	43
READ to WRITE command delay for same bank group	$t_{CCD\_L\_RTW}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	29,30, 35,43
WRITE to READ command delay for same bank group, to same bank group	$t_{CCD\_L\_WTR}$	$CWL + WBL/2 + \max(16nCK, 10ns)$						nCK, ns	29,31, 43
WRITE to READ command delay for different bank, to same bank group	$t_{CCD\_M\_WTR}$	$CWL + WBL/2 + \max(16nCK, 8.000ns)$	-	$CWL + WBL/2 + \max(16nCK, 7.619ns)$	-	$CWL + WBL/2 + \max(16nCK, 7.272ns)$	-	nCK, ns	29,31,43
READ to READ command delay for different bank group	t_{CCD_S}	$RBL/2$						nCK	43
WRITE to WRITE command delay for different bank group	$t_{CCD\_S\_WR}$	$WBL/2$						nCK	43
READ to WRITE command delay for different bank group	$t_{CCD\_S\_RTW}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, nsCK	29,30, 35,43
WRITE to READ command delay for different bank group	$t_{CCD\_S\_WTR}$	$CWL + WBL/2 + \max(4nCK, 2.000ns)$	-	$CWL + WBL/2 + \max(4nCK, 1.904ns)$	-	$CWL + WBL/2 + \max(4nCK, 1.818ns)$	-	nCK, ns	29,31,43
WRITE to READ with AUTO PRECHARGE command for same bank	t_{CCD_WTRA}	$CWL + WBL/2 + t_{WR} - t_{RTP}$						nCK, ns	29,31, 34,43
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	$t_{RRD\_L,1K}$	$\max(8nCK, 4.000ns)$	-	$\max(8nCK, 4.000ns)$	-	$\max(8nCK, 3.863ns)$	-	nCK, ns	43
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	$t_{RRD\_L,2K}$	$\max(8nCK, 4.000ns)$	-	$\max(8nCK, 4.000ns)$	-	$\max(8nCK, 3.863ns)$	-	nCK, ns	43
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	$t_{RRD\_S,1K}$	8						nCK	43
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	$t_{RRD\_S,2K}$	8						nCK	43
Four activate window for 2KB page size	$t_{FAW,2K}$	$\max(40nCK, 10.000ns)$	-	$\max(40nCK, 9.523ns)$	-	$\max(32nCK, 9.090ns)$	-	nCK, ns	
Four activate window for 1KB page size	$t_{FAW,1K}$	$\max(32nCK, 8.000ns)$	-	$\max(32nCK, 7.619ns)$	-	$\max(32nCK, 7.272ns)$	-	nCK, ns	

Table 494: DDR5 8000-8800: Command and Address Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
READ command to PRECHARGE command delay	t_{RTP}	max(12nCK, 7.5ns)						nCK, ns	43
PRECHARGE to PRECHARGE command delay	t_{PPD}	4						nCK	36,43
WRITE recovery time	t_{WR}	30						ns	1,43
DLL locking time	t_{DLLK}	2560	-	2560	-	2816	-	nCK	

Table 495: DDR5 8000-8800: Mode Register Read/Write Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Mode register READ command period	t_{MRR}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		2
Mode register READ pattern to mode register READ pattern command spacing	t_{MRR_p}	8	-	8	-	8	-	nCK	
Mode register WRITE command period	t_{MRW}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-		2
Mode register SET command delay	t_{MRD}	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-	max(14ns, 16nCK)	-		
DFE mode register WRITE update delay time	t_{DFE}	80	-	80	-	80	-	ns	3

Table 496: DDR5 8000-8800: Data Strobe Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ preamble (1tCK preamble)	t_{RPRE1}	-	-	-	-	-	-	tCK	47,48
DQS_t, DQS_c differential READ preamble (2tCK preamble)	t_{RPRE2}	1.800	-	1.800	-	1.800	-	tCK	37,47
DQS_t, DQS_c differential READ preamble DDR4 (2tCK preamble)	t_{RPRE2_D4}	-	-	-	-	-	-	tCK	37,47
DQS_t, DQS_c differential READ preamble (3tCK preamble)	t_{RPRE3}	-	-	-	-	-	-	tCK	38,47
DQS_t, DQS_c differential READ preamble (4tCK preamble)	t_{RPRE4}	3.600	-	3.600	-	3.600	-	tCK	39,47
DQS_t, DQS_c differential READ postamble - 0.5tCK	$t_{RPST0.5}$	0.450	-	0.450	-	0.450	-	tCK	41,47
DQS_t, DQS_c differential READ postamble - 1.5tCK	$t_{RPST1.5}$	1.300	-	1.300	-	1.300	-	tCK	42,47
DQS_t, DQS_c differential WRITE preamble (2tCK preamble)	t_{WPRE2}	-	-	-	-	-	-	tCK (avg)	37,47

Table 496: DDR5 8000-8800: Data Strobe Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential WRITE preamble (3tCK preamble)	t_{WPRES}	-	-	-	-	-	-	tCK (avg)	38,47
DQS_t, DQS_c differential WRITE preamble (4tCK preamble)	t_{WPRES}	3.600	-	3.600	-	3.600	-	tCK (avg)	40,47
DQS_t, DQS_c differential initial low pulse width during preamble (2tCK preamble)	$t_{DQSL2PRE}$	-	-	-	-	-	-	tCK (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (3tCK preamble)	$t_{DQSL3PRE}$	-	-	-	-	-	-	tCK (avg)	
DQS_t, DQS_c differential initial low pulse width during preamble (4tCK preamble)	$t_{DQSL4PRE}$	1.800	-	1.800	-	1.800	-	tCK (avg)	
DQS_t, DQS_c differential WRITE postamble - 0.5tCK	$t_{WPST0.5}$	-	-	-	-	-	-	tCK (avg)	41,47
DQS_t, DQS_c differential WRITE postamble - 1.5tCK	$t_{WPST1.5}$	1.200	-	1.200	-	1.200	-	tCK (avg)	42,47
DQS_t, DQS_c differential high toggle pulse width during DDR4 2tCK READ preamble	$t_{DQSH2PRE\_D4}$	-	-	-	-	-	-	tCK	
DQS_t, DQS_c differential high toggle pulse width during WRITE preamble	t_{DQSH_pre}	0.45	0.55	0.45	0.55	0.45	0.55	nCK	
DQS_t, DQS_c differential low toggle pulse width during WRITE preamble	t_{DQSL_pre}	0.45	0.55	0.45	0.55	0.45	0.55	nCK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	t_{DQSCK}	-0.390	0.390	-0.400	0.400	-0.410	0.410	tCK	6,9,16
DQS_t, DQS_c rising edge output variance window	t_{DQSCKi}	-	0.635	-	0.651	-	0.667	tCK	7,8,9,16,33

Table 497: DDR5 8000-8800: Write Enable Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
2-tCK WRITE preamble enable window	$t_{WPRES\_EN\_2tCK}$	1.5	-	1.5	-	1.5	-	tCK	
3-tCK WRITE preamble enable window	$t_{WPRES\_EN\_3tCK}$	2.5	-	2.5	-	2.5	-	tCK	
4-tCK WRITE preamble enable window	$t_{WPRES\_EN\_4tCK}$	2.5	-	2.5	-	2.5	-	tCK	
Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge	$t_{DQSoffset}$	-0.5	0.5	-0.5	0.5	-0.5	0.5	tCK	26
Write leveling setup time	t_{WLS}	-80	80	-80	80	-80	80	ps	

Table 497: DDR5 8000-8800: Write Enable Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling hold time	t_{WLH}	-80	80	-80	80	-80	80	ps	
DRAM Voltage/ temperature drift window of first rising DQS _t preamble edge relative to CWL CK _t -CK _c edge (x4/x8/ x16)	t_{DQSD}	-0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	-0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	-0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	t_{CK}	5
Host and system voltage/ temperature drift window of first rising DQS _t pre- amble edge relative to CWL CK _t -CK _c edge (x4/x8/x16)	t_{DQSS}	-0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	-0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	-0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	0.25 x t_{WPRE_E} N _n t_{CK} (MIN)	t_{CK}	5,32

Table 498: DDR5 8000-8800: Dynamic ODT Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RTT change skew timing - transitioning from onevalid RTT state to the nextvalid RTT state	t_{ADC}	0.08	0.92	0.06	0.94	0.04	0.96	t_{CK}	45,46

Table 499: DDR5 8000-8800: MPSM Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPSM exit to first valid command delay	t_{MPSMX}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	ns	

Table 500: DDR5 8000-8800: ZQ Calibration Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ZQ calibration time	t_{ZQCAL}	1		1		1		μs	
ZQ calibration latch time	t_{ZQLAT}	max(30ns, 8nCK)		max(30ns, 8nCK)		max(30ns, 8nCK)			

Table 501: DDR5 8000-8800: Reset Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
RESET _n low time for reset initialization with stable power	t_{PW_RESET}	1	-	1	-	1	-	μs	
Time after RESET _n assertion to ODT off	t_{RST_ADC}	-	50	-	50	-	50	ns	

Table 502: DDR5 8000-8800: Self Refresh Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t_{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	nCK, ns	
Self refresh CS _n low pulse width	t_{CSL}	10	-	10	-	10	-	ns	

Table 502: DDR5 8000-8800: Self Refresh Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Self refresh exit CS_n high pulse width	t_{CSH_SRexit}	13	200	13	200	13	200	ns	
Self refresh exit CS_n low pulse width	t_{CSL_SRexit}	3nCK	30ns	3nCK	30ns	3nCK	30ns	nCK, ns	11
Self refresh exit CS_n low pulse width with frequency change	$t_{CSL\_FreqChg}$	VREFCA_time	-	VREFCA_time	-	VREFCA_time	-	ns	12
Valid clock requirement before SRX	t_{CKSRX}	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-	max(3.5ns, 8nCK)	-	nCK, ns	
Valid clock requirement after SRE	t_{CKLCS}	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	$t_{CPDED} + 1nCK$	-	nCK, ns	
Self refresh exit CS_n HIGH	t_{CASRX}	0	-	0	-	0	-	ns	
Exit self refresh to commands not requiring a locked DLL	t_{XS}	t_{RFC1}	-	t_{RFC1}	-	t_{RFC1}	-	nCK	
Exit self refresh to commands requiring a locked DLL	t_{XS_DLL}	t_{DLLK}	-	t_{DLLK}	-	t_{DLLK}	-	ns	

Table 503: DDR5 8000-8800: Power-Down Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Command pass disable delay	t_{CPDED}	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	max(5ns, 8nCK)	-	ns	
Power-down duration	t_{PD}	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	max(7.5ns, 8nCK)	5* t_{REFI1} (normal) 9* t_{REFI2} (FGR)	ns	28,44
Power-down exit command to next valid command (excluding NT ODT commands when PDE with CA11=L)	t_{XP}	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-	ns	
ACTIVATE command to POWER-DOWN ENTRY command	$t_{ACTPDEN}$	2	-	2	-	2	-	nCK	13
PRECHARGE, PRECHARGE ALL, or PRECHARGE SAME BANK command to POWER-DOWN ENTRY command	t_{PRPDEN}	2	-	2	-	2	-	nCK	13
READ or READ w/ AUTO PRECHARGE command to POWER-DOWN ENTRY command	t_{RDPDEN}	CL+RBL/2+1	-	CL+RBL/2+1	-	CL+RBL/2+1	-	nCK	24, 30
WRITE command to POWER-DOWN ENTRY command	t_{WRPDEN}	CWL+WBL/2+($t_{WR}/t_{CK(avg)}$)+1	-	CWL+WBL/2+($t_{WR}/t_{CK(avg)}$)+1	-	CWL+WBL/2+($t_{WR}/t_{CK(avg)}$)+1	-	nCK	14, 24,31
WRITE w/ AUTO PRECHARGE command to POWER-DOWN ENTRY command	$t_{WRAPDEN}$	CWL+WBL/2+ $t_{WR}+1$	-	CWL+WBL/2+ $t_{WR}+1$	-	CWL+WBL/2+ $t_{WR}+1$	-	nCK	14, 15, 24,31
REFRESH ALL or REFRESH SAME BANK command to POWER-DOWN ENTRY command	$t_{REFPDEN}$	2	-	2	-	2	-	nCK	

Table 503: DDR5 8000-8800: Power-Down Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MRR command to POWER-DOWN ENTRY command	$t_{MRRPDEN}$	CL+8+1	-	CL+8+1	-	CL+8+1	-	nCK	24
MRW command to POWER-DOWN ENTRY command	$t_{MRWPDEN}$	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	t_{MRD} (MIN)	-	nCK	
MPC command to POWER-DOWN ENTRY command	$t_{MPCPDEN}$	t_{MPC_delay}	-	t_{MPC_delay}	-	t_{MPC_delay}	-	nCK	25

Table 504: DDR5 8000-8800: MPC Command Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MPC to any other valid command	t_{MPC_Delay}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time between stable MPC command and first falling CS edge (setup)	$t_{MC\_MPC\_Setup}$	3	-	3	-	3	-	nCK	21
Time between first rising CS edge and stable MPC command (HOLD)	$t_{MC\_MPC\_Hold}$	3	-	3	-	3	-	nCK	21
Time CS_n is held LOW to register MPC command	t_{MPC_CS}	3.5	8	3.5	8	3.5	8	nCK	20

Table 505: DDR5 8000-8800: PDA Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
PDA ENUMERATE ID command to any other command cycle time	$t_{PDA\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY}$ (MAX) + BL/2 + 19ns	-	$t_{PDA\_DQS\_DELAY}$ (MAX) + BL/2 + 19ns	-	$t_{PDA\_DQS\_DELAY}$ (MAX) + BL/2 + 19ns	-	nCK,ns	
PDA ENUMERATE ID command to any other command cycle time for multi-device continuous DQS toggle mode	$t_{PDA\_DELAY\_2}$	$t_{PDA\_DQS\_DELAY\_1}$ + t_{MPC_DELAY} (MIN)	-	$t_{PDA\_DQS\_DELAY\_1}$ + t_{MPC_DELAY} (MIN)	-	$t_{PDA\_DQS\_DELAY\_1}$ + t_{MPC_DELAY} (MIN)	-	nCK,ns	
Delay to rising strobe edge used for sampling DQ during PDA operation	$t_{PDA\_DQS\_DELAY}$	5	18	5	18	5	18	ns	4
Delay to falling DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_1}$	$t_{PDA\_DQS\_DELAY}$ (MIN) - $t_{PDA\_S\_FALL}$ (MIN)	$t_{PDA\_DQS\_DELAY}$ (MAX) - $t_{PDA\_S\_FALL}$ (MIN)	$t_{PDA\_DQS\_DELAY}$ (MIN) - $t_{PDA\_S\_FALL}$ (MIN)	$t_{PDA\_DQS\_DELAY}$ (MAX) - $t_{PDA\_S\_FALL}$ (MIN)	$t_{PDA\_DQS\_DELAY}$ (MIN) - $t_{PDA\_S\_FALL}$ (MIN)	$t_{PDA\_DQS\_DELAY}$ (MAX) - $t_{PDA\_S\_FALL}$ (MIN)	nCK,ns	
Delay to rising DQ edge during PDA operation	$t_{PDA\_DQ\_DELAY\_2}$	$t_{PDA\_DELAY\_1}$ (MIN)	-	$t_{PDA\_DELAY\_1}$ (MIN)	-	$t_{PDA\_DELAY\_1}$ (MIN)	-	nCK,ns	
Delay after last DQS toggle used for sampling DQ during PDA	$t_{PDA\_DQS\_STOP}$	t_{MPC_DELAY} (MIN) + $t_{PDA\_H\_RISE}$ (MIN)	-	t_{MPC_DELAY} (MIN) + $t_{PDA\_H\_RISE}$ (MIN)	-	t_{MPC_DELAY} (MIN) + $t_{PDA\_H\_RISE}$ (MIN)	-	nCK,ns	

Table 505: DDR5 8000-8800: PDA Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay after last DQ toggle used for sampling DQ during PDA	$t_{PDA\_DQ\_STOP}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	nCK,ns	
Falling DQ edge setup time during PDA operation	$t_{PDA\_S\_FALL}$	MAX(3nCK, 1.250ns)	-	MAX(3nCK, 1.250ns)	-	MAX(3nCK, 1.250ns)	-		
Rising DQ edge hold time during PDA operation	$t_{PDA\_H\_RISE}$	MAX(3nCK, 1.250ns)	-	MAX(3nCK, 1.250ns)	-	MAX(3nCK, 1.250ns)	-		
Rising DQ edge setup time during PDA operation	$t_{PDA\_S\_RISE}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-		
Falling DQ edge hold time during PDA operation	$t_{PDA\_H\_FALL}$	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-	$t_{MPC\_DELAY} (MIN)$	-		

Table 506: DDR5 8000-8800: Read Training Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of MRW continuous burst mode exit to next valid command delay	$t_{Cont\_Exit\_Delay}$	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	$t_{Cont\_Exit} + t_{MRD}$	-	-	
Registration of MRW continuous burst mode exit to end of training mode	t_{Cont_Exit}	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	CL+BL/2+10nCK	-	
Maximum delay between first exit continuous burst mode MRW command and the second exit continuous burst mode MRW command	t_{CBME}	-	CL-10nCK	-	CL-10nCK	-	CL-10nCK	-	

Table 507: DDR5 8000-8800: Read Preamble Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay from MRW command to DQS driven	t_{SDOn}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		
Delay from MRW command to DQS disabled	t_{SDOff}	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)	-	max(12nCK, 20ns)		

Table 508: DDR5 8000-8800: CA Training Mode Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CATM entry command to start of training samples time	t_{CATM_Entry}	20	-	20	-	20	-	ns	
Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device).	t_{CATM_Exit}	-	14	-	14	-	14	ns	
Registration of CATM exit to next valid command delay	$t_{CATM\_Exit\_Delay}$	20	-	20	-	20	-	ns	
Time from sample evaluation to output on DQ bus	t_{CATM_Valid}	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{CATM\_DQ\_Window}$	2	-	2	-	2	-	nCK	27
CS_n assertion duration to exit CATM	$t_{CATM\_CS\_Exit}$	2	8	2	8	2	8	nCK	

Table 509: DDR5 8000-8800: CS Training Mode Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Registration of CSTM entry command to start of training samples time	$t_{\text{CSTM\_Entry}}$	20	-	20	-	20	-	ns	
Min time between last CS _n pulse and first pulse of MPC command to exit CSTM	$t_{\text{CSTM\_Min\_to\_MPC\_exit}}$	4	-	4	-	4	-	nCK	
Registration of CSTM exit command to end of training mode	$t_{\text{CSTM\_Exit}}$	-	20	-	20	-	20	ns	
Time from sample evaluation to output on DQ bus	$t_{\text{CSTM\_Valid}}$	-	20	-	20	-	20	ns	
Time output is available on DQ bus	$t_{\text{CSTM\_DQ\_Window}}$	2	-	2	-	2	-	nCK	27
Registration of CSTM exit to next valid command delay	$t_{\text{CSTM\_Exit\_Delay}}$	20	-	20	-	20	-	ns	

Table 510: DDR5 8000-8800: Write Leveling Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid	t_{WLPEN}	-	15	-	15	-	15	ns	
Write leveling output delay	t_{WLO}	-	9.5	-	9.5	-	9.5	ns	
Width of write leveling internal pulse	$t_{\text{WL\_Pulse\_Width}}$	2	-	2	-	2	-	tCK	17
Write leveling write to subsequent command spacing	$t_{\text{WL\_Write}}$	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-	max(CWL, last DQS differential toggle) + t_{WLO} (MAX) + 2nCK	-	nCK	

Table 511: DDR5 8000-8800: $V_{\text{REFCA}}/V_{\text{REFCS}}$ Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
VREFCA command to any other valid command delay	$t_{\text{VREFCA\_Delay}}$	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time CS _n is held LOW to register VREFCA command	$t_{\text{VREFCS\_CS}}$	3.5	8	3.5	8	3.5	8	nCK	18,19
VREFCS command to any other valid command delay	$t_{\text{VREFCS\_Delay}}$	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	
Time CS _n is held LOW to register VREFCS command	$t_{\text{VREFCS\_CS}}$	3.5	8	3.5	8	3.5	8	nCK	18,19
MIN time between stable VREFCA command and first falling CS edge (SETUP)	$t_{\text{MC\_VREFCA\_Setup}}$	3	-	3	-	3	-	nCK	10
MIN time between first rising CS edge and stable VREFCA command (HOLD)	$t_{\text{MC\_VREFCA\_Hold}}$	3	-	3	-	3	-	nCK	10

Table 511: DDR5 8000-8800: VREFCA/VREFCS Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
MIN time between stable VREFCS command and first falling CS edge (SETUP)	$t_{MC\_VREFCS\_Setup}$	3	-	3	-	3	-	nCK	10
MIN time between first rising CS edge and stable VREFCS command (HOLD)	$t_{MC\_VREFCS\_Hold}$	3	-	3	-	3	-	nCK	10

Table 512: DDR5 8000-8800: hPPR/sPPR Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
hPPR programming time (x4/x8)	t_{PGM_hPPRa}	1000	-	1000	-	1000	-	ms	
hPPR programming time (x16)	t_{PGM_hPPRb}	2000	-	2000	-	2000	-	ms	
sPPR programming time	t_{PGM_sPPR}	$CWL+8t_{CK}+t_{WR}$		$CWL+8t_{CK}+t_{WR}$		$CWL+8t_{CK}+t_{WR}$		t_{CK}	
hPPR/sPPR exit recognition time	t_{PGM_Exit}	t_{RP}	-	t_{RP}	-	t_{RP}	-	ns	
hPPR program exit and new address setting time	t_{PGMPST}	50	-	50	-	50	-	μs	
sPPR program exit and new address setting time	t_{PGMPST_sPPR}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	ns	

Table 513: DDR5 8000-8800: DQS Interval Oscillator Readout Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Delay time from DQS interval oscillator stop to mode register readout in manual mode	t_{OSCOM}	t_{MPC_Delay}	-	t_{MPC_Delay}	-	t_{MPC_Delay}	-	nCK	23
Delay time from DQS interval oscillator stop to mode register readout in automatic mode	t_{OSCOA}	t_{MRD}	-	t_{MRD}	-	t_{MRD}	-	nCK	23
DQS interval oscillator start gap in automatic stop mode	t_{OSCS}	$t_{MPC\_Delay} + \text{DQS Interval Time Run Time}$						nCK	23, 43

Table 514: DDR5 8000-8800: ESC Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ECS operation time	t_{ECSc}	max(176nCK, 110ns)	-	max(176nCK, 110ns)	-	max(176nCK, 110ns)	-		

Table 515: DDR5 8000-8800: CRC Error Reporting Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
CRC error to ALERT_n latency	t_{CRC_ALERT}	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	12	20	12	20	12	20	nCK	

- Notes: 1. Start of internal write transaction is defined as follows: For BL16 (fixed by MRS and on-the-fly), rising clock edge 4-clock cycles after CWL. For BC8 (on-the-fly), rising clock edge 4 clock cycles after CWL.
2. MRR and MRW commands are not allowed with pages open.
3. Applies only to MRWs to DFE registers and is defined as the settling time before a new DFE setting is active.

4. $t_{PDA\_DQS\_DELAY}$ specifies when the beginning of a minimum one complete BL16 set of consecutive strobe edges (8 rising edges and 8 falling edges, plus 1 rising edge and 1 falling edge for the 2 tCK and 3 tCK preambles or 2 rising edges and 2 falling edges for the 4 tCK preamble) must be sent by the host controller after the associated MPC.
5. Measured relative to the write leveling feedback, after write leveling training has been completed.
6. Measured over full V_{DD} and temperature spec ranges.
7. Measured for a given part and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
8. These parameters are verified by design and characterization, and may not be subject to production test.
9. Assume no jitter on input clock signals to the DRAM device.
10. Applies only to multicycle VREFCS/VREFCA commands when MR2:OP[4]=0b.
11. While in 2N mode, t_{CSL_SRExit} is not statically held LOW, it pulses for each 2-cycle period for a min of 6nCK. See the 2N mode section for more details.
12. Since frequency can require VrefCA, VrefCS_ and CA/CK/CS ODT changes, the min time is longer than the traditional t_{CSL} when the SRE command with CA9=L is used.
13. POWER DOWN command can be sent while operations such as ACTIVATION, PRECHARGE, AUTO PRECHARGE or REFRESH are in progress; however, IDD spec is not applied until the operations are finished.
14. Write recovery (WR) is calculated from t_{WR} by using the Rounding Algorithm. Refer to the Rounding Definitions and Algorithm section for more information.
15. Write recovery (WR) in clock cycles, as programmed in MR6.
16. Refer to Read Timing definition.
17. There is no max limit for the $t_{WL\_Pulse\_Width}$; however, the write leveling internal pulse must begin at zero for each WRITE command.
18. Multiple cycles are used to avoid possible metastability of CS_n.
19. At the end of CSTM and CATM, it is assumed the host can place the CS_n and the CA signals appropriately.
20. The minimum t_{MPC_CS} constraint applies only when the CS assertion duration setting is 0. The CS assertion duration MR setting must be set (MR2:OP[4]=1b) to enable single-cycle MPC commands. The earliest time to set the CS assertion duration MR (MR2:OP[4]=b1) is after VREFCS, VREFCA, CS, and CA training is complete, when MRW commands can be sent to the device.
21. Applies only to multicycle MPC commands when MR2:OP[4] = 0b.
22. $t_{CK(AVG)}$ MIN listed for reference only; refer to Speed Bin tables and Operations section for valid $t_{CK(AVG)}$ values.
23. In manual stop mode, DQS OSC START command must be followed by DQS OSC STOP command (MPC). Otherwise, DQS OSC reset value (MR46,47) cannot be guaranteed.
24. READ/WRITE/MRR can refer to both target command and non-target command when CA11 = H during PDE command.
25. t_{MPC_delay} is a valid timing parameter for all MPC functions except:
 - Enter CS Training mode, Enter CA Training mode, PDA Enumerate ID, Enter PDA Enumerate Program mode because power-down entry is not supported for these MPC commands.
 - Apply VrefCA, VrefCS and RTT_CA/CS/CK because this MPC command requires waiting for VrefCA_time/VrefCS_time.
26. When measuring the $t_{DQsoffset}$, t_{WLS} and t_{WLH} are reflected in the $t_{DQsoffset}$ value.
27. This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.
28. Refresh to refresh max time interval limits $t_{PD(MAX)}$ to 5 x t_{REFI1} in normal refresh mode, 9 x t_{REFI2} in FGR mode.
29. CWL = CL-2.
30. RBL: Read burst length associated with READ command:
 - RBL = 32 (36 w/ RCRC on) for fixed 32 and BL32 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for fixed 16 and BL16 in BL32 OTF mode
 - RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
31. WBL: Write burst length associated with Write command:
 - WBL = 32 (36 w/ WCRC on) for fixed 32 and BL32 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for fixed 16 and BL16 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

32. DDR5-3200 timings apply for data rates <2933 MT/s. For example, at 2000 MT/s, $t_{DQSS}(\max) = (2000/2933) \cdot 0.25 \cdot t_{WPRE\_EN\_ntck}(\min) = 0.17 \cdot t_{WPRE\_EN\_ntck}(\min)$.
33. Measured at a fixed and constant V_{DD} and temperature condition.
34. $t_{CCD\_WRTA}(\min)$ must always greater than or equal to $CWL + WBL/2 + t_{WR}(\min) - t_{RTP}(\min)$. When using the appropriate rounding algorithms, $n_{CCD\_WTRA}(\min)$ must always be greater than or equal to $CWL + WBL/2 + n_{WR}(\min) - n_{RTP}(\min)$.
35. The following is considered for t_{RTW} equation:
 - 1 t_{CK} must be added due to t_{DQS2CK} .
 - Read DQS offset timing can pull in the t_{RTW} timing.
 - 1 t_{CK} must be added when 1.5 t_{CK} postamble.
36. t_{PPD} applies to any combination of precharge commands (PREab, PREsb, PREpb). t_{PPD} also applies to any combination of precharge commands to a different die in a 3DS device.
37. The 2 t_{CK} READ and WRITE preamble is valid for the 3200/3600/4000/4400/4800 speed grades.
38. The 3 t_{CK} READ and WRITE preamble is valid for the 4000/4400/4800/5200/5600/6000/6400 speed grades.
39. The 4 t_{CK} READ preamble is valid for the 5600/6000/6400/6800/7200/7600/8000/8400/8800 speed grades.
40. The 4 t_{CK} WRITE preamble is valid for the 4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800 speed grades.
41. The 0.5 t_{CK} READ and Write Postamble is valid for the 3200/3600/4000/4400/4800 speed grades.
42. The 1.5 t_{CK} READ Postamble is valid for the 3200/3600/4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800 speed grades.
43. The 1.5 t_{CK} WRITE Postamble is valid for the 4000/4400/4800/5200/5600/6000/6400/6800/7200/7600/8000/8400/8800 speed grades.
44. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.
45. $t_{PD}(\max)$ must always be less than or equal to $5 \cdot t_{REFI1}(\max)$ during normal refresh mode and less than or equal to $9 \cdot t_{REFI2}(\max)$ during fine granularity refresh mode, and when using the rounding algorithms, $n_{PD}(\max)$ must always be less than or equal to $5 \cdot n_{REFI1}(\max)$ during normal refresh mode and less than or equal to $9 \cdot n_{REFI2}(\max)$ during fine granularity refresh mode.
46. When transitioning from a value of RTT equal to RA , to a value of RTT equal to RB , the RTT termination resistance during the transition must be constrained for the minimum of (RA , RB) to the maximum of (RA , RB).
47. The t_{ADC} spec follows the operating frequency (so that faster speed bins are backward-compatible to slower speed bins).
48. The strobe preamble and postamble timing parameter values must follow the operating frequency.
49. The 1 t_{CK} READ preamble is valid for the DDR5-3200/3600 speed grades.

Timing Parameters by Speed Grade: 3DS

Timing Parameters for 2H and 4H 3DS DDR5 3200-4000

The analog timing parameters in this section have been defined based on nominal $t_{CK(avg)min}$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

All minimum timing parameters needing to be translated from the time domain (ns, ps, etc.) to the clock domain (nCK), must be guard banded by an additional 0.3% according to the rules in the Rounding Definitions and Algorithms section.

Table 516: 3DS DDR5 3200-4000: Clock Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.625	-	0.555	-	0.500	-	ns	23

Table 517: 3DS DDR5 3200-4000: Command and Address Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_slr}$	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-		47
Minimum WRITE to WRITE command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_WR\_slr}$	$\max(32nCK, 20ns)$	-	$\max(32nCK, 20ns)$		$\max(32nCK, 20ns)$			47
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	$t_{CCD\_L\_WR2\_slr}$	$\max(16nCK, 10ns)$	-	$\max(16nCK, 10ns)$	-	$\max(16nCK, 10ns)$	-		47
Minimum READ to WRITE command delay for same bank group in same logical rank	$t_{CCD\_L\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{READ DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31, 36
Minimum WRITE to READ command delay for same bank group in same logical rank	$t_{CCD\_L\_WTR\_slr}$	$CWL + WBL/2 + \max(16 nCK, 10ns)$						nCK, ns	24,32
Read to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_slr}$	$t_{CCD\_L\_slr}$						nCK, ns	47
Write to Write command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WR\_slr}$	$t_{CCD\_L\_WR\_slr}$						nCK, ns	47

Table 517: 3DS DDR5 3200-4000: Command and Address Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Write to Read command delay for different bank in same bank group in same logical rank	$t_{\text{CCD\_M\_WTR\_slr}}$	$t_{\text{CCD\_L\_WTR\_slr}}$						nCK, ns	47
Minimum READ to READ command delay for different bank group in same logical rank	$t_{\text{CCD\_S\_slr}}$	RBL/2						nCK	47
Minimum WRITE to WRITE command delay for different bank group in same logical rank	$t_{\text{CCD\_S\_WR\_slr}}$	WBL/2						nCK	47
Minimum READ to WRITE command delay for different bank group in same logical rank	$t_{\text{CCD\_S\_RTW\_slr}}$	CL - CWL + RBL/2 + 2 t_{CK} - (READ DQS offset) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}						nCK, ns	24,31,36
Minimum WRITE to READ command delay for different bank group in same logical rank	$t_{\text{CCD\_S\_WTR\_slr}}$	CWL + WBL/2 + max(4nCK, 2.5ns)						nCK, ns	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	$t_{\text{CCD\_WTRA\_slr}}$	CWL + WBL/2 + $t_{\text{WR\_slr}}$ - $t_{\text{RTP\_slr}}$						nCK, ns	24,32,35
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	$t_{\text{RRD\_L\_slr}}$ (1K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-		47
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	$t_{\text{RRD\_S\_slr}}$ (1K)	8	-	8	-	8	-	nCK	47
Four activate window to same logical rank	$t_{\text{FAW\_slr}}$ (1K)	max(32nCK, 20.000ns)	-	max(32nCK, 17.777ns)	-	max(32nCK, 16.000ns)	-		41
READ to PRECHARGE command delay in same logical rank	$t_{\text{RTP\_slr}}$	max(12nCK, 7ns)	-	max(12nCK, 7.5ns)	-	max(12nCK, 7.5ns)	-		47
PRECHARGE to PRECHARGE delay in same logical rank	$t_{\text{PPD\_slr}}$	2	-	2	-	2	-	nCK, ns	37,47
WRITE recovery time in same logical rank	$t_{\text{WR\_slr}}$	30	-	30	-	30	-	ns	47
Minimum READ to READ command delay in different logical ranks	$t_{\text{CCD\_dlr}}$	max(8nCK, 5.000ns)	-	max(8nCK, 4.444ns)	-	max(8nCK, 4.000ns)	-		

Table 517: 3DS DDR5 3200-4000: Command and Address Timing (Continued)

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to WRITE command delay in different logical ranks	$t_{CCD\_WR\_dlr}$	max(8nCK, 5.000ns)	-	max(8nCK, 4.444ns)	-	max(8nCK, 4.000ns)	-		44
Minimum READ to WRITE command delay for different logical ranks	$t_{CCD\_RTW\_dlr}$	CL - CWL + RBL/2 + 2 ^t CK - (READ DQS offset) + (tRPST - 0.5 ^t CK) + tWPRE						nCK, ns	24,31, 36
Minimum WRITE to READ command delay for different logical ranks	$t_{CCD\_WTR\_dlr}$	CWL + WBL/2 + max(4nCK, 2.5ns)						nCK, ns	24,32
ACTIVATE to ACTIVATE command delay to different logical ranks	t_{RRD_dlr}	max(4nCK, 2.500ns)	-	max(4nCK, 2.222ns)	-	max(4nCK, 2.000ns)	-		
Four activate window to different logical ranks	t_{FAW_dlr}	max(16nCK, 10.000ns)	-	max(16nCK, 8.888ns)	-	max(16nCK, 8.000ns)	-		
PRECHARGE to PRECHARGE delay in different logic rank	t_{PPD_dlr}	2	-	2	-	2	-	nCK	37,47
Minimum WRITE to WRITE command delay in different 3DS or DDP physical ranks	$t_{CCD\_WR\_dpr}$	8	-	8	-	8	-	nCK	44,45, 47
Activate window by DIMM channel	t_{DCAW}	128	-	128	-	128	-	nCK	42,43, 45,46 47
DIMM CHANNEL ACTIVATE command count in t_{DCAW}	n_{DCAC}	-	32	-	32	-	32	A	42,43, 45,46 47

Table 518: 3DS DDR5 3200-4000: Self-Refresh Timing

Parameter	Symbol	3200		3600		4000		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
3DS Exit Self-Refresh to next valid command not requiring a DLL	t_{XS_3ds}	$t_{RFC1\_slr} + 10ns$						ns	39,40,41,43

Timing Parameters for 2H and 4H 3DS DDR5 4400-5200

The analog timing parameters in this section have been defined based on nominal $t_{CK(avg)min}$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 519: 3DS DDR5 4400-5200: Clock Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.454	-	0.416	-	0.384	-	ns	23

Table 520: 3DS DDR5 4400-5200: Command and Address Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_slr}$	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-		47
Minimum WRITE to WRITE command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_WR\_slr}$	$\max(32nCK, 20ns)$	-	$\max(32nCK, 20ns)$	-	$\max(32nCK, 20ns)$	-		47
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	$t_{CCD\_L\_WR2\_slr}$	$16nCK, 10ns$ (MAX)	-	$16nCK, 10ns$ (MAX)	-	$16nCK, 10ns$ (MAX)	-		47
Minimum READ to WRITE command delay for same bank group in same logical rank	$t_{CCD\_L\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{READ DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31,36
Minimum WRITE to READ command delay for same bank group in same logical rank	$t_{CCD\_L\_WTR\_slr}$	$CWL + WBL/2 + \max(16nCK, 10ns)$						nCK, ns	24,32
Read to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_slr}$	$t_{CCD\_L\_slr}$						nCK, ns	47
Write to Write command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WR\_slr}$	$t_{CCD\_L\_WR\_slr}$						nCK, ns	47
Write to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WTR\_slr}$	$t_{CCD\_L\_WTR\_slr}$						nCK, ns	24,32,47
Minimum READ to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_slr}$	$RBL/2$						nCK	47
Minimum WRITE to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_WR\_slr}$	$WBL/2$						nCK	47
Minimum READ to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{READ DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31,36
Minimum WRITE to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_WTR\_slr}$	$CWL + WBL/2 + \max(4nCK, 2.5ns)$						nCK, ns	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	$t_{CCD\_WTRA\_slr}$	$CWL + WBL/2 + t_{WR\_slr} - t_{RTP\_slr}$						nCK, ns	24,32,35

Table 520: 3DS DDR5 4400-5200: Command and Address Timing (Continued)

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	$t_{RRD\_L\_slr}$ (1K)	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-	max(8nCK, 5ns)	-		47
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	$t_{RRD\_S\_slr}$ (1K)	8	-	8	-	8	-	nCK	47
Four activate window to same logical rank	t_{FAW_slr} (1K)	max(32nCK, 14.545ns)	-	max(32nCK, 13.333ns)	-	max(32nCK, 12.308ns)	-		41
READ to PRECHARGE command delay in same logical rank	t_{RTP_slr}	max(12nCK, 7.5ns)	-	max(12nCK, 7.5ns)	-	max(12nCK, 7.5ns)	-		47
PRECHARGE to PRECHARGE delay in same logical rank	t_{PPD_slr}	2	-	2	-	2	-	nCK	37,47
WRITE recovery time in same logical rank	t_{WR_slr}	30	-	30	-	30	-	ns	47
Minimum READ to READ command delay in different logical ranks	t_{CCD_dlr}	max(8nCK, 3.636ns)	-	max(8nCK, 3.333ns)	-	max(8nCK, 3.333ns)	-		
Minimum WRITE to WRITE command delay in different logical ranks	$t_{CCD\_WR\_dlr}$	max(8nCK, 3.636ns)	-	max(8nCK, 3.333ns)	-	max(8nCK, 3.333ns)	-		44
Minimum READ to WRITE command delay for different logical ranks	$t_{CCD\_RTW\_dlr}$	CL - CWL + RBL/2 + 2 ^t CK - (READ DQS offset) + (t _{RPST} - 0.5 ^t CK) + t _{WPRE}						nCK, ns	24,31,36
Minimum WRITE to READ command delay for different logical ranks	$t_{CCD\_WTR\_dlr}$	CWL + WBL/2 + max(4nCK, 2.5ns)						nCK, ns	24,32
ACTIVATE to ACTIVATE command delay in different logical ranks	t_{RRD_dlr}	max(4nCK, 1.818ns)	-	max(4nCK, 1.666ns)	-	max(4nCK, 1.666ns)	-		
Four activate window to different logical ranks	t_{FAW_dlr}	max(16nCK, 7.272ns)	-	max(16nCK, 6.666ns)	-	max(16nCK, 6.666ns)	-		
PRECHARGE to PRECHARGE delay in different logic rank	t_{PPD_dlr}	2	-	2	-	2	-	nCK	37,47
Minimum WRITE to WRITE command delay in different 3DS or DDP physical ranks	$t_{CCD\_WR\_dpr}$	8	-	8	-	8	-	nCK	42,45,47
Activate window by DIMM channel	t_{DCAW}	128	-	128	-	128		nCK	42,43,45,46,47
DIMM CHANNEL ACTIVATE command count in t_{DCAW}	n_{DCAC}	-	32	-	32	-	32	ACT	42,43,45,46,48

Table 521: 3DS DDR5 4400-5200: Self-Refresh Timing

Parameter	Symbol	4400		4800		5200		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
3DS Exit Self-Refresh to next valid command not requiring a DLL	t_{XS_3DS}	t_{RFC1_slr} +10ns	-	t_{RFC1_slr} +10ns	-	t_{RFC1_slr} +10ns	-	ns	39,40,41,43

Timing Parameters for 2H and 4H 3DS DDR5 5600-6400

The analog timing parameters in this section have been defined based on nominal $t_{CK(ave)}^{min}$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 522: 3DS DDR5 5600-6400: Clock Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.357		0.333		0.312		ns	23

Table 523: 3DS DDR5 5600-6400: Command and Address Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_slr}$	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-		47
Minimum WRITE to WRITE command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_WR\_slr}$	$\max(32nCK, 20ns)$		$\max(32nCK, 20ns)$		$\max(32nCK, 20ns)$			47
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	$t_{CCD\_L\_WR2\_slr}$	$\max(16nCK, 10ns)$		$\max(16nCK, 10ns)$		$\max(16nCK, 10ns)$			47
Minimum READ to WRITE command delay for same bank group in same logical rank	$t_{CCD\_L\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31, 36
Minimum WRITE to READ command delay for same bank group in same logical rank	$t_{CCD\_L\_WTR\_slr}$	$CWL + WBL/2 + \max(16nCK, 10ns)$						nCK, ns	24,32
Read to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_slr}$	$t_{CCD\_L\_slr}$						nCK, ns	47
Write to Write command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WR\_slr}$	$t_{CCD\_L\_WR\_slr}$						nCK, ns	47
Write to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WTR\_slr}$	$t_{CCD\_L\_WTR\_slr}$						nCK, ns	24,32, 47
Minimum READ to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_slr}$	RBL/2						nCK	47
Minimum WRITE to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_WR\_slr}$	WBL/2						nCK	47

Table 523: 3DS DDR5 5600-6400: Command and Address Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31, 36
Minimum WRITE to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_WTR\_slr}$	$CWL + WBL/2 + \max(4nCK, 2.5ns)$						nCK, ns	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	$t_{CCD\_WTRA\_slr}$	$CWL + WBL/2 + t_{WR\_slr} - t_{RTP\_slr}$						nCK, ns	24,32, 35
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	$t_{RRD\_L\_slr}$ (1K)	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-	$\max(8nCK, 5ns)$	-		47
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	$t_{RRD\_S\_slr}$ (1K)	8	-	8	-	TBD	-	nCK	47
Four activate window to same logical rank	t_{FAW_slr} (1K)	$\max(32nCK, 1.428ns)$	-	$32nCK, 10.666ns$ (MAX)	-	$\max(32nCK, 10.000ns)$	-	nCK, ns	41
READ to PRECHARGE command delay in same logical rank	t_{RTP_slr}	$\max(12nCK, 7.5ns)$	-	$\max(12nCK, 7.5ns)$	-	$\max(12nCK, 7.5ns)$	-		47
PRECHARGE to PRECHARGE delay in same logical rank	t_{PPD_slr}	2	-	2	-	2	-	nCK	37,47
WRITE recovery time in same logical rank	t_{WR_slr}	30	-	30	-	30	-	ns	47
Minimum READ to READ command delay in different logical ranks	t_{CCD_dlr}	$\max(8nCK, 3.214ns)$	-	$\max(8nCK, 3.214ns)$	-	$\max(8nCK, 3.215ns)$	-		
Minimum WRITE to WRITE command delay in different logical ranks	$t_{CCD\_S\_WR\_dlr}$	$\max(8nCK, 3.214ns)$	-	$\max(8nCK, 3.214ns)$	-	$\max(8nCK, 3.215ns)$	-		44
Minimum READ to WRITE command delay for different logical ranks	$t_{CDD\_RTW\_dlr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31, 36
Minimum WRITE to READ command delay for different logical ranks	$t_{CCD\_WTR\_dlr}$	$CWL + WBL/2 + \max(4nCK, 2.5ns)$						nCK, ns	24,32
ACTIVATE to ACTIVATE command delay in different logical ranks	t_{RRD_dlr}	$\max(4nCK, 1.666ns)$	-	$\max(4nCK, 1.666ns)$	-	$\max(4nCK, 1.666ns)$	-		
Four activate window to different logical ranks	t_{FAW_dlr}	$\max(16nCK, 6.666ns)$	-	$\max(16nCK, 6.666ns)$	-	$\max(16nCK, 6.666ns)$	-		
PRECHARGE to PRECHARGE delay in different logic rank	t_{PPD_dlr}	2	-	2	-	2	-	nCK	37,47

Table 523: 3DS DDR5 5600-6400: Command and Address Timing (Continued)

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum Write to Write command delay in different 3DS or DDP physical ranks	$t_{CCD\_S\_WR\_dpr}$	8	-	8	-	8	-	nCK	44,45,47
Activate window by DIMM channel	t_{DCAW}	128	-	128	-	128	-	nCK	42,43,45,46,47
DIMM channel ACTIVATE command count in t_{DCAW}	n_{DCAC}	-	32	-	32	-	32	ACT	42,43,45,46,48

Table 524: 3DS DDR5 5600-6400: Self-Refresh Timing

Parameter	Symbol	5600		6000		6400		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
3DS Exit Self-Refresh to next valid command not requiring DLL	t_{XS_3DS}	$t_{RFC1\_slr} + 10ns$	-	$t_{RFC1\_slr} + 10ns$	-	$t_{RFC1\_slr} + 10ns$	-	ns	39,40,41,43

Timing Parameters for 2H and 4H 3DS DDR5 6800-7600

The analog timing parameters in this section have been defined based on nominal $t_{CK(avg)min}$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 525: 3DS DDR5 6800-7600: Clock Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.294	-	0.277	-	0.263	-	ns	23

Table 526: 3DS DDR5 6800-7600: Command and Address Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_sir}$	$\max(8nCK, 5ns)$						nCK, ns	47
Minimum WRITE to WRITE command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_WR\_slr}$	$\max(32nCK, 20ns)$						nCK, ns	47
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	$t_{CCD\_L\_WR2\_slr}$	$\max(16nCK, 10ns)$						nCK	47
Minimum READ to WRITE command delay for same bank group in same logical rank	$t_{CCD\_L\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31,36

Table 526: 3DS DDR5 6800-7600: Command and Address Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum WRITE to READ command delay for same bank group in same logical rank	$t_{CCD\_L\_WTR\_slr}$	CWL + WBL/2 + max(16nCK, 10ns)						nCK, ns	24,32
Read to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_slr}$	max(8nCK, 4.705ns)	-	max(8nCK, 4.444ns)	-	max(8nCK, 4.210ns)	-	nCK, ns	
Write to Write command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WR\_slr}$	max(32nCK, 18.823ns)	-	max(32nCK, 17.777ns)	-	max(32nCK, 16.842ns)	-	nCK, ns	
Write to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WTR\_slr}$	CWL + WBL/2 + max(16nCK, 9.411ns)	-	CWL + WBL/2 + max(16nCK, 8.888ns)	-	CWL + WBL/2 + max(16nCK, 8.421ns)	-	nCK, ns	24,32
Minimum READ to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_slr}$	RBL/2						nCK	47
Minimum WRITE to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_WR\_slr}$	WBL/2						nCK	47
Minimum READ to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_RTW\_slr}$	CL - CWL + RBL/2 + 2 t_{CK} - (Read DQS offset) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}						nCK, nsCK	24,31, 36
Minimum WRITE to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_WTR\_slr}$	CWL + WBL/2 + max(4nCK, 2.352ns)	-	CWL + WBL/2 + max(4nCK, 2.222ns)	-	CWL + WBL/2 + max(4nCK, 2.105ns)	-	nCK, nsCK	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	$t_{CCD\_WTRA\_slr}$	CWL + WBL/2 + t_{WR_slr} - t_{RTP_slr}						nCK, ns	24,32, 35
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	$t_{RRD\_L\_slr}(1K)$	max(8nCK, 4.705ns)	-	max(8nCK, 4.444ns)	-	max(8nCK, 4.210ns)	-	nCK, ns	
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	$t_{RRD\_S\_slr}(1K)$	8						nCK	47
Four activate window to same logical rank	$t_{FAW\_slr}(1K)$	max(32nCK, 9.411ns)	-	max(32nCK, 8.888ns)	-	max(32nCK, 8.421ns)	-	nCK, ns	41
READ command to PRECHARGE command delay in same logical rank	t_{RTP_slr}	max(12nCK, 7.5ns)						nCK, ns	47
PRECHARGE to PRECHARGE delay in same logical rank	t_{PPD_slr}	2				4		nCK	37,47

Table 526: 3DS DDR5 6800-7600: Command and Address Timing (Continued)

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
WRITE recovery time in same logical rank	t_{WR_slr}	30						ns	47
Minimum READ to READ command delay in different logical ranks	t_{CCD_dlr}	max(8nCK, 3.125ns)	-	max(8nCK, 3.056ns)	-	max(8nCK, 3.056ns)	-	nCK	
Minimum WRITE to WRITE command delay in different logical ranks	$t_{CCD\_WR\_dlr}$	max(8nCK, 3.125ns)	-	max(8nCK, 3.056ns)	-	max(8nCK, 3.056ns)	-	nCK	44
Minimum READ to WRITE command delay for different logical ranks	$t_{CCD\_RTW\_dlr}$	CL - CWL + RBL/2 + 2 t_{CK} -(Read DQS offset) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}						nCK	24,31, 36
Minimum WRITE to READ command delay for different logical ranks	$t_{CCD\_WTR\_dlr}$	CWL + WBL/2 + max(4nCK, 2.5ns)						nCK	24,32
ACTIVATE to ACTIVATE command delay to different logical ranks	t_{RRD_dlr}	max(4nCK, 1.666ns)						nCK, ns	47
Four activate window to different logical ranks	t_{FAW_dlr}	max(16nCK, 6.666ns)						nCK, ns	47
PRECHARGE to PRECHARGE delay in different logic rank	t_{PPD_dlr}	2				4		nCK	37,47
Minimum WRITE to WRITE command delay in different 3DS or DDP physical ranks	$t_{CCD\_S\_WR\_dpr}$	8						nCK	44,45, 47
Activate window by DIMM channel	t_{DCAW}	128						nCK	42,43, 45,46, 47
DIMM channel ACTIVE command count in t_{DCAW}	n_{DCAW}	32						ACT	42,43, 45,46, 48

Table 527: 3DS DDR5 6800-7600: Self Refresh Timing

Parameter	Symbol	6800		7200		7600		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
3DS exit self refresh to next valid command not requiring a DLL	t_{XS_3DS}	$t_{RFC1\_slr} + 10ns$						ns	39,40,41, 43

Timing Parameters for 2H and 4H 3DS DDR5 8000-8800

The analog timing parameters in this section have been defined based on nominal $t_{CK(avg)min}$ according to the rounding rules which can be found in the Rounding Definitions and Algorithms section.

Table 528: 3DS DDR5 8000-8800: Clock Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Average clock period	$t_{CK,AVG}$	0.250	-	0.238	-	0.227	-	ns	23

Table 529: 3DS DDR5 8000-8800: Command and Address Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Minimum READ to READ command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_sir}$	$\max(8nCK, 5ns)$						nCK, ns	47
Minimum WRITE to WRITE command delay for same bank in same bank group in same logical rank	$t_{CCD\_L\_WR\_slr}$	$\max(32nCK, 20ns)$						nCK, ns	47
Minimum WRITE to WRITE command delay for same bank group, second WRITE not RMW, same logical rank	$t_{CCD\_L\_WR2\_slr}$	$\max(16nCK, 10ns)$						nCK	47
Minimum READ to WRITE command delay for same bank group in same logical rank	$t_{CCD\_L\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						nCK, ns	24,31, 36
Minimum WRITE to READ command delay for same bank group in same logical rank	$t_{CCD\_L\_WTR\_slr}$	$CWL + WBL/2 + \max(16nCK, 10ns)$						nCK, ns	24,32
Read to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_slr}$	$\max(8nCK, 4.000ns)$	-	$\max(8nCK, 4.000ns)$	-	$\max(8nCK, 3.863ns)$	-	nCK, ns	
Write to Write command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WR\_slr}$	$\max(32nCK, 16.000ns)$	-	$\max(32nCK, 15.238ns)$	-	$\max(32nCK, 14.545ns)$	-	nCK, ns	
Write to Read command delay for different bank in same bank group in same logical rank	$t_{CCD\_M\_WTR\_slr}$	$CWL + WBL/2 + \max(16nCK, 8.000ns)$	-	$CWL + WBL/2 + \max(16nCK, 7.619ns)$	-	$CWL + WBL/2 + \max(16nCK, 7.272ns)$	-	nCK, ns	24,32
Minimum READ to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_slr}$	$RBL/2$						nCK	47
Minimum WRITE to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_WR\_slr}$	$WBL/2$						nCK	47
Minimum READ to WRITE command delay for different bank group in same logical rank	$t_{CCD\_S\_RTW\_slr}$	$CL - CWL + RBL/2 + 2t_{CK} - (\text{Read DQS offset}) + (t_{RPST} - 0.5t_{CK}) + t_{WPRE}$						$nCK, nsCK$	24,31, 36
Minimum WRITE to READ command delay for different bank group in same logical rank	$t_{CCD\_S\_WTR\_slr}$	$CWL + WBL/2 + \max(4nCK, 2.000ns)$	-	$CWL + WBL/2 + \max(4nCK, 1.904ns)$	-	$CWL + WBL/2 + \max(4nCK, 1.818ns)$	-	$nCK, nsCK$	24,32
WRITE to READ with AUTO PRECHARGE command for same bank in same logic rank	$t_{CCD\_WTRA\_slr}$	$CWL + WBL/2 + t_{WR\_slr} - t_{RTP\_slr}$						nCK, ns	24,32, 35

Table 529: 3DS DDR5 8000-8800: Command and Address Timing (Continued)

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE command delay to same bank group in same logical rank	$t_{RRD\_L\_slr}(1K)$	max(8nCK, 4.000ns)	-	max(8nCK, 4.000ns)	-	max(8nCK, 3.863ns)	-	nCK, ns	
ACTIVATE to ACTIVATE command delay to different bank group in same logical rank	$t_{RRD\_S\_slr}(1K)$	8						nCK	47
Four activate window to same logical rank	$t_{FAW\_slr}(1K)$	max(32nCK, 8.000ns)	-	max(32nCK, 7.619ns)	-	max(32nCK, 7.272ns)	-	nCK, ns	41
READ command to PRECHARGE command delay in same logical rank	t_{RTP_slr}	max(12nCK, 7.5ns)						nCK, ns	47
PRECHARGE to PRECHARGE delay in same logical rank	t_{PPD_slr}	4						nCK	37,47
WRITE recovery time in same logical rank	t_{WR_slr}	30						ns	47
Minimum READ to READ command delay in different logical ranks	t_{CCD_dlr}	max(8nCK, 3.000ns)	-	max(8nCK, 3.000ns)	-	max(8nCK, 2.955ns)	TBD	nCK, ns	
Minimum WRITE to WRITE command delay in different logical ranks	$t_{CCD\_WR\_dlr}$	max(8nCK, 3.000ns)	-	max(8nCK, 3.000ns)	-	max(8nCK, 2.955ns)	TBD	nCK, ns	44
Minimum READ to WRITE command delay for different logical ranks	$t_{CCD\_RTW\_dlr}$	CL - CWL + RBL/2 + 2 t_{CK} -(Read DQS offset) + (t_{RPST} - 0.5 t_{CK}) + t_{WPRE}						nCK, ns	24,31,36
Minimum WRITE to READ command delay for different logical ranks	$t_{CCD\_WTR\_dlr}$	CWL + WBL/2 + max(4nCK, 2.5ns)						nCK, ns	24,32
ACTIVATE to ACTIVATE command delay to different logical ranks	t_{RRD_dlr}	max(4nCK, 1.666ns)						nCK, ns	47
Four activate window to different logical ranks	t_{FAW_dlr}	max(16nCK, 6.666ns)						nCK, ns	47
PRECHARGE to PRECHARGE delay in same logic rank	t_{PPD_dlr}	4						nCK	47
Minimum WRITE to WRITE command delay in different 3DS or DDP physical ranks	$t_{CCD\_S\_WR\_dpr}$	8						nCK	44,45,47
Activate window by DIMM channel	t_{DCAW}	128						nCK	42,43,45,46,47
DIMM channel ACTIVE command count in t_{DCAW}	n_{DCAW}	32						ACT	42,43,45,46,48

Table 530: 3DS DDR5 8000-8800: Self Refresh Timing

Parameter	Symbol	8000		8400		8800		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
3DS exit self refresh to next valid command not requiring a DLL	t_{XS_3DS}	$t_{RFC1\_slr}+10ns$						nCK	39,40,41, 43

Notes: 1. Start of internal write transaction is defined as:

- For BL16 (fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after CWL.
 - For BC8 (on-the-fly): Rising clock edge 4 clock cycles after CWL.
2. MRR and MRW commands are not allowed with pages open.
 3. This parameter applies only to MRWs to DFE registers and is defined as the settling time before a new DFE setting is active.
 4. The range of $t_{PDA\_DQS\_DELAY}$ specifies the full range of when the minimum of 16 strobe edges can be sent by the host controller.
 5. Measured relative to the write leveling feedback, after write leveling training has completed.
 6. Includes min DQS and CK timing terms TBD.
 7. Measured over full VDD and temperature spec ranges.
 8. Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
 9. These parameters are verified by design and characterization, and may not be subject to production test.
 10. Assume no jitter on input clock signals to the device.
 11. This applies only to multicycle VREFCS/VREFCA commands when MR2:OP[4]=0b.
 12. While in 2N mode, t_{CSL_SRExit} is not statically held LOW, as it will pulse for each 2-cycle period for a min of 6 nCK. Refer to the 2N mode section for more details.
 13. Since frequency can require VREFCA and CA/CK/CS ODT changes, the min time is longer than the traditional t_{CSL} when the SRE command with CA9=L is used.
 14. POWER DOWN command can be sent while operations such as row activation, precharge, auto-precharge or refresh are in progress; however, IDD spec is not applied until the operations are finished.
 15. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}/t_{CK} .
 16. WR in clock cycles as programmed in MR6.
 17. Refer to Read Timing Definition.
 18. There is no max limit for $t_{WL\_Pulse\_Width}$; however, the Write Leveling Internal Pulse must begin at zero for each WRITE command.
 19. Multiple cycles are used to avoid possible metastability of CS_n.
 20. At the end of CSTM, it is assumed the host should be able to place the CS_n appropriately and the VREFCA command could be issued as a single-cycle command.
 21. The minimum t_{MPC_CS} constraint only applies when the CS assertion duration setting is 0. The CS assertion duration MR setting must be set to enable single-cycle MPC commands. The earliest time to set the CS assertion duration MR is after CA training is complete, when MRW commands can be sent to the device.
 22. This applies only to multicycle MPC commands when MR2:OP[2]=0b.
 23. $t_{CK(AVG)}$, MIN listed for reference only, refer to the Speed Bins and Operations section which lists all valid $t_{CK(avg)}$ values.
 24. CWL=CL-2.
 25. In manual stop mode, DQS OSC START command should be followed by the DQS OSC STOP command (MPC). Otherwise, DQS OSC result value (MR46 and 47) cannot be guaranteed.
 26. RD/WR/MRR can refer to both target command and non-target command when CA11=HIGH during PDE command.
 27. t_{MPC_delay} is a valid timing parameter for all MPC commands except:
 - Enter CS Training mode, Enter CA Training mode, PDA Enumerate ID, Enter PDA Enumerate Program mode because POWER DOWN ENTRY is not supported for these MPC commands.
 - APPLY VREFCA, VREFCS and RTT_CA/CS/CK because this MPC command requires waiting for VREFCA_{time}/VREFCS_{time}.
 28. When measuring the $t_{DQSoffset}$, t_{WLS} and t_{WLH} are reflected in the $t_{DQSoffset}$ value.

29. This timing parameter is applied to each DQ independently, not all-DQs valid window perspective.
30. Refresh to refresh max time interval limits $t_{PD}(MAX)$ to $5X t_{REFI1}$ if in normal refresh mode and $9X t_{REFI2}$ if in FGR mode.
31. RBL: Read burst length associated with READ command:
 - RBL = 32 (36 with RCRC on) for fixed 32 and BL32 in BL32 OTF mode
 - RBL = 16 (18 with RCRC on) for fixed 16 and BL16 in BL32 OTF mode
 - RBL = 16 (18 with RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
32. WBL: Write burst length associated with Write command:
 - WBL = 32 (36 w/ WCRC on) for fixed 32 and BL32 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for fixed 16 and BL16 in BL32 OTF mode
 - WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode
33. DDR5-3200 timings apply for data rates <2933 MT/s. For example, at 2000 MT/s, $t_{DQSS}(max) = (2000/2933) * t_{WPRE\_EN\_ntck}(min) = 0.17 * t_{WPRE\_EN\_ntck}(min)$.
34. Measured at a fixed and constant VDD and temperature condition.
35. $t_{CCD\_WRTA}(min)$ must always be greater than or equal to $CWL + WBL/2 + t_{WR}(min) - t_{RTP}(min)$. When using the appropriate rounding algorithms, $t_{CCD\_WTRA}(min)$ must always be greater than or equal to $CWL + WBL/2 + t_{WR}(min) - t_{RTP}(min)$.
36. The following is considered for t_{RTW} equation:
 - 1 t_{CK} needs to be added due to t_{DQSK}
 - Read DQS offset timing can pull in the t_{RTW} timing
 - 1 t_{CK} needs to be added when 1.5 t_{CK} postamble
37. t_{PPD} applies to any combination of PRECHARGE commands (PREab, PREsb, PREpb). t_{PPD} also applies to any combination of PRECHARGE commands to a different die in a 3DS device.
38. For x4 devices only. x8 device timings are TBD.
39. Upon exit from self-refresh, the 3DS device requires a minimum of one extra REFRESH command to all logical ranks before it is put back into self-refresh mode.
40. This parameter utilizes a value that varies based on density. Refer to the 3DS Refresh section for more information.
41. The timings contained in this table are for x4 2H and 4H 3DS devices.
42. ACTIVATE commands to different channels on the same DIMM may be issued on the same cycle, not requiring any stagger.
43. ACTIVATE commands to the same channel on a DIMM are subject to t_{DCAW} . No more than t_{DCAC} ACTIVATE commands may be issued to the same channel on a DIMM within t_{DCAW} .
44. $t_{CCD\_WR\_dlr}$ and $t_{CCD\_WR\_dpr}$ also apply to the WRITE PATTERN command.
45. Parameter applies to all DDP or dual-physical-rank (36 and 40 placement) 3DS-based DIMMs built with JESD301-1 PMIC50x0 Specification, but may not apply to DIMMs built with higher current capacity PMICs.
46. ACTIVATE commands to a DIMM channel include all ACTIVATE commands to the same logical rank (SLR), all ACTIVATE commands to different logical ranks (DLR), and all ACTIVATE commands to different physical ranks (DPR).
47. This parameter only specifies minimum values (there is no maximum value). The maximum value cells have been merged in the table to improve legibility.
48. This parameter only specifies maximum values (there is no minimum value). The minimum value cells have been merged in the table to improve legibility.

Rounding Definition and Algorithm

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 2200 MHz (4400 MT/s) for the DDR5-4400 speed bin, which mathematically yields a nominal clock period of 0.454545... ns). In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be used. The device specification establishes a minimum granularity for timing parameters of 1ps.

Rules for rounding must be defined to enable optimization of device performance without violating device parameters. All timing parameters specified in the time domain (ns, ps, etc.) which must then be converted to the clock domain (nCK units) must be defined to align with these rules. The key point is, the minimum and maximum timing parameter values must generally use the same rounding rules used to define $t_{CK(AVG)min}$ and $t_{CK(AVG)max}$. The resulting rounding algorithms rely on results that are within correction factors of device testing and specification to avoid losing performance due to rounding errors. The rules are:

- **Defining timing parameter values:** Minimum and maximum timing parameter values, including $t_{CK(AVG)min}$ and $t_{CK(AVG)max}$, are to be rounded down and defined to 1ps of accuracy in the specification based on the non-rounded nominal $t_{CK(AVG)}$ for a given speed bin. If the nominal timing parameter values require more than 1ps of accuracy, they can be rounded down (faster) to the next 1ps according to the rounding algorithms. The device is responsible for absorbing the resulting small parameter extension. In other words, the device specification only lists the nominal parameter values rounded down to the next 1ps. For example, this extends the DDR5-4400 $t_{CK(AVG)min}$ definition to be exactly 0.454ns, which is slightly smaller (faster) than the nominal memory clock period of 0.454545...ns by less than 1ps.
- **Calculating the real minimum timing parameter values:** For minimum timing parameters (other than $t_{CK(AVG)min}$) to avoid losing performance due to additional erroneous nCKs, and to calculate the true real minimum values, their nominal values listed in this specification must be reduced (faster) by the maximum percentage error (correction factor) used to define $t_{CK(AVG)min}$. The device is responsible for absorbing the resulting small parameter extensions. For example, $t_{WR MIN}$ has a nominal value of 30.000ns; however, applying the 0.30% correction factor enables a more aggressive timing (for example, 29.910ns) to be supported, which enables the intended smaller (faster) nCK value to be maintained when rounding $t_{CK(AVG)min}$ down to the next 1ps. Note, parameter values defined to be 0ps do not need to be reduced by a correction factor, and therefore, do not require these rounding algorithms.
- **Calculating the real maximum timing parameter values:** For maximum timing parameters, including $t_{CK(AVG)max}$, to avoid losing performance due to excluding erroneous nCKs and to calculate the true real maximum values, their nominal values listed in the DDR5 SDRAM specification must be increased (slower) by the maximum percentage error caused by rounding $t_{CK(AVG)}$ down to the next 1ps. The device is responsible for absorbing the resulting small parameter extensions. For example, $t_{REFImax}$ has a nominal value of 3.9 μ s. The DDR5-8400 speed bin mathematically yields a nominal clock period $t_{CK(AVG)}$ of 0.238095... ns, resulting in a theoretical maximum percentage error of 0.42% (0.239ns/0.238ns-100%). So the true real $t_{REFImax}$ value is 3.916386... μ s (3.9 μ s*0.239ns/0.238ns) for the DDR5-8400 speed bin.
- **Rounding algorithm for minimum timing parameter values:** Round-down only integer number math is commonly used in the industry to calculate nCK values. This algorithm for minimum timing parameters uses scaling by 1000 to enable use of integer math. Nominal minimum timing parameters like t_{WRmin} , t_{RCDmin} , etc., which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (ps) are rounded down to the next 1ps, multiplied by the scaled inverse correction factor (1000-3=997) prior to division by the application memory clock period rounded down to the next 1ps, and adding 1 scaled by 1000 to that result effectively adds 1 nCK. Division by 1000 undoes the scaling effects, resulting in a number of clocks as the final answer, which has been effectively rounded up to the next 1 nCK by adding 1 nCK in the previous step and then

rounding down to the next 1 nCK. The caveat is, effectively adding 1 prior to rounding down is mostly equivalent to rounding up, except when the result is equal to an integer, in which case the result won't be rounded down as intended, and therefore, performance would be lost. To address this, the 0.28% correction factor needed for 3600 MHz (0.277ns/0.277777...ns-100%) operation has been increased slightly to 0.30% in this rounding algorithm. This accounts for all boundary conditions except for the specific case when the nominal minimum timing parameter value is defined to be 0ps. No rounding is required for parameter values equal to 0 ps. This rounding algorithm is not optimized for parameter values that are less than or equal to 0ps, and may result in unintended lost performance if used for parameter values that are less than or equal to 0ps.

$$nCK[\text{min\_parameter}] = \text{truncate} \left[\frac{\left(\frac{\text{truncate}[\text{nominal\_min\_parameter\_in\_ps}] \times 997}{\text{truncate}[\text{tCK(AVG)real\_in\_ps}]} + 1000 \right)}{1000} \right]$$

- **Rounding algorithm for maximum timing parameter values:** Round-down only integer number math is commonly used in the industry to calculate nCK values. This rounding algorithm is used for maximum timing parameters. Nominal maximum timing parameters like tREFI_{max}, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (ps), are rounded down to the next 1ps prior to division by the application memory clock period rounded down to the next 1ps, resulting in a number of clocks as the final answer, which is rounded down to the next 1 nCK. No rounding is required for parameter values equal to 0ps, but this rounding algorithm can still be used for parameter values equal to 0ps and no performance will be lost. This rounding algorithm is not optimized for parameter values that are less than 0ps (negative parameter values), and may result in violating the parameter specification if used for parameter values that are less than 0ps.

$$nCK[\text{max\_parameter}] = \text{truncate} \left(\frac{\text{truncate}[\text{nominal\_max\_parameter\_in\_ps}]}{\text{truncate}[\text{tCK(AVG)real\_in\_ps}]} \right)$$

- **CL algorithm for standard speed bins:** The rounding algorithms must be used for all timing parameters when converting from the time domain (ns, ps, etc.) to the clock domain (nCK units), except for when converting tAA to CL. If these rounding algorithms are used to convert tAA to CL, they will return invalid CLs for some cases when down clocking (the DIMM SPD CL mask does not protect against all of these cases). The proper setting of CL must be determined by the memory controller, either by using the speed bin tables or the CL algorithm, or by some other means. Refer to the Speed Bins and Operations section for more information. Note, the CL algorithm replaces the need to use the DIMM SPD CL Mask.
- **CL algorithm for custom speed bins:** If the device supports non-standard tCK, tAA, tRCD, and tRP speed bin timings, the CL algorithm will still only return valid CLs as defined in the speed bin tables, which may not be the intended CLs for non-standard speed bins. In these cases, the rounding algorithms may need to be used to convert tAA to CL, instead of the CL algorithm. The CL returned by the rounding algorithms must be incremented up to the next supported CL according to the DIMM SPD CL mask. Consult the memory vendor for more information.

Example: Using Round-Down Only Integer Number Math to Convert t_{WR} (MIN) from ps to nCK

// This algorithm reduces the nominal minimum timing parameter value by a 0.30%
// correction factor, rounds t_{CK} (avg) down, calculates nCK, adds 1nCK, and rounds nCK down to the next integer value.

```
int TwrMin, Correction, ClockPeriod, TempTwr, TempNck, TwrInNck;

TwrMin = 30000;                // tWRmin in ps
Correction = 3                  // 0.30% per the rounding algorithm
ClockPeriod = ApplicationTck;   // Clock period in ps is application-specific
TempTwr = TwrMin * (1000 - Correction); // Apply correction factor, scaled by 1000
TempNck = TempTwr / ClockPeriod; // Initial nCK calculation, scaled by 1000
TempNck = TempNck + 1000;       // Add 1, scaled by 1000, to effectively round up
TwrInNck = (int)(TempNck / 1000); // Truncate to next lower integer
```

Table 531: Example: Using Round-Down Only Integer Number Math

DDR5 Device Operating at Standard Application Frequencies Timing Parameter: $t_{WR}(\text{min}) = 30.00\text{ns}$					
Application Speed Grade	Device t_{WR}	Application t_{CK}	Device t_{WR} / Application t_{CK}	Device $t_{WR} * 1000 - \text{Correction}$ / Application $t_{CK} + 1000$	Truncate Corrected nCK / 1000
MT/s	ps	ps	nCK (Real)	Scaled nCK (Corrected)	nCK (Integer)
3200	30000	625	48.00	48856	48
3600	30000	555	54.05	54891	54
4000	30000	500	60.00	60820	60
4400	30000	454	66.08	66881	66
4800	30000	416	72.12	72899	72

Revision History

Rev. E – 10/2024

- Updates are to align with JEDEC spec JESD79.5C-v.1.31

Rev. D – 10/2022

- Updates are to align with JEDEC spec JESD79.5B-v1.20

Rev. C – 10/2021

- Removed Micron Confidential marking

Rev. B – 09/2021

- Updates are to align with JEDEC full draft spec Rev 2.0
- Added MBIST/mPPR section
- Added sPPR undo and lock features
- Updated sPPR and hPPR to only have to drive DQ0-3
- Added Adaptive RFM feature
- Added Directed RFM feature, details still pending in JEDEC
- Moved several items from the DDR5 Core data sheet into the DDR5 Die Revision specific data sheet addendum
 - Features and options page
 - Pinouts and ballouts section
 - pin description section
 - Package mechanical drawings section
- Updates to on-die ECC to cover the bounded fault improvements
- Added features like ECS scan mode to provide flexibility for controllers to better control ECS use cases.
- Added Refresh Interval Rate feature
- Updated Write leveling with the 1/2 step WICA feature to enhance WL training
- Added mode registers to account for authentication serial numbers on DRAMs
- Added MR4 wide refresh rate
- Updated and improved data sheet with many clarifications and editorial corrections.

Rev. A – 06/2020

- Initial release — based on JEDEC full draft specification Rev 1.0

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.