MSPM0C110x, MSPS003 Mixed-Signal Microcontrollers

1 Features

- **Core**
  - Arm® 32-bit Cortex®-M0+ CPU, frequency up to 24MHz
- **Operating characteristics**
  - Extended temperature: –40°C to 125°C
  - Wide supply voltage range: 1.62V to 3.6V
- **Memories**
  - Up to 16KB of flash
  - 1KB of SRAM
- **High-performance analog peripherals**
  - One analog-to-digital converter (ADC) with up to 10 total external channels, 1.7Msps at 10 bit or 1.5Msps at 12 bit with VDD as the voltage reference
  - Configurable 1.4V or 2.5V internal ADC voltage reference (VREF)
  - Integrated temperature sensor
  - Integrated supply monitor
- **Optimized low-power modes**
  - RUN: 87µA/MHz
  - STOP: 609µA at 4MHz, 311µA at 32kHz
  - STANDBY: 5µA with SRAM retention
  - SHUTDOWN: 200nA
- **Intelligent digital peripherals**
  - 1-channel DMA controller dedicated for ADC
  - Three timers supporting up to 14 PWM channels
    - One 16-bit advanced timers with deadband support up to 8 PWM channels
    - One 16-bit general purpose timer with 4 capture/compares
    - One 16-bit general purpose timer with 2 capture/compares
  - Windowed watchdog timer
  - BEEPER generating 1kHz, 2kHz, 4kHz, or 8kHz square wave to drive the external beeper
- **Enhanced communication interfaces**
  - One UART interface supporting LIN, IrDA, DALI, smart card, Manchester and low-power operation in STANDBY mode
  - One I^2C interface supporting FM+ (1Mbps), SMBus, PMBus, and wakeup from STOP mode
  - One SPI supporting up to 12Mbps
- **Clock system**
  - Internal 24MHz oscillator with an accuracy from -2% to +1.2% (SYSOSC)
  - Internal 32kHz low-frequency oscillator (LFOSC)
- **Data integrity**
  - Cyclic redundancy checker (CRC-16)
- **Flexible I/O features**
  - Up to 18 GPIOs
  - Two 5V-tolerant open-drain IOs
- **Development support**
  - 2-pin serial wire debug (SWD)
- **Package options**
  - 20-pin TSSOP (PW)
  - 20-pin VSSOP (DGS)
  - 20-pin WQFN (RUK)
  - 16-pin SOT (DYY)
  - 8-pin SOT (DDF)
  - 8-pin WSON (DSG)
  - 8-pin DSBGA (YCJ)
- **Family members** (also see *Device Comparison*)
  - MSPS003F4: 16KB of flash, 1KB of RAM
  - MSPS003F3: 8KB of flash, 1KB of RAM
  - MSPM0C1104: 16KB of flash, 1KB of RAM
  - MSPM0C1103: 8KB of flash, 1KB of RAM
- **Development kits and software** (also see *Tools and Software*)
  - LP-MSPM0C1104 LaunchPad™ development kit
  - MSP Software Development Kit (SDK)

2 Applications

- Battery charging and management
- Power supplies and power delivery
- Personal electronics
- Building security and fire safety
- Connected peripherals and printers
- Grid infrastructure
- Smart metering
- Communication modules
- Medical and healthcare
- Lighting

3 Description

MSPM0C110x microcontrollers (MCUs) are part of the MSP highly-integrated ultra-low-power 32-bit MCU family based on the enhanced Arm® Cortex®-M0+ core platform operating at up to 24MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 125°C, and operate with supply voltages from 1.62V to 3.6V.

The MSPM0C110x devices provide up to 16KB embedded flash program memory with 1KB SRAM. These MCUs incorporate a high-speed on-chip oscillator with an accuracy from -2% to +1.2%, eliminating the need for an external crystal. Additional features include a 1-channel DMA, CRC-16 accelerator, and a variety of high-performance analog peripherals such as one 12-bit 1.5Msps ADC with VDD as the voltage reference, and an on-chip temperature sensor. These devices also offer intelligent digital peripherals such as one 16-bit advanced timer, two 16-bit general purpose timer, one windowed watchdog timer, and a variety of communication peripherals including one UART, one SPI, and one I^2C. These communication peripherals offer protocol support for LIN, IrDA, DALI, Manchester, smart card, SMBus, and PMBus.

The TI MSPM0 family of low-power MCUs consists of devices with varying degrees of analog and digital integration let customers find the MCU that meets their project needs. The architecture combined with extensive low-power modes is optimized to achieve extended battery life in portable measurement applications.

MSPM0C110x MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. Development kits include a LaunchPad™ kit available for purchase and design files for a target-socket board. TI also provides a free MSP Software Development Kit (SDK), which is available as a component of Code Composer Studio™ IDE desktop and cloud version within the TI Resource Explorer. MSPM0 MCUs are also supported by extensive online collateral, training with MSP Academy, and online support through the TI E2E™ support forums.

For complete module descriptions, see the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

CAUTION

System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturbing of data or code memory. See MSP430™ System-Level ESD Considerations for more information, as the principles in that application note also apply to MSPM0 MCUs.

4 Functional Block Diagram

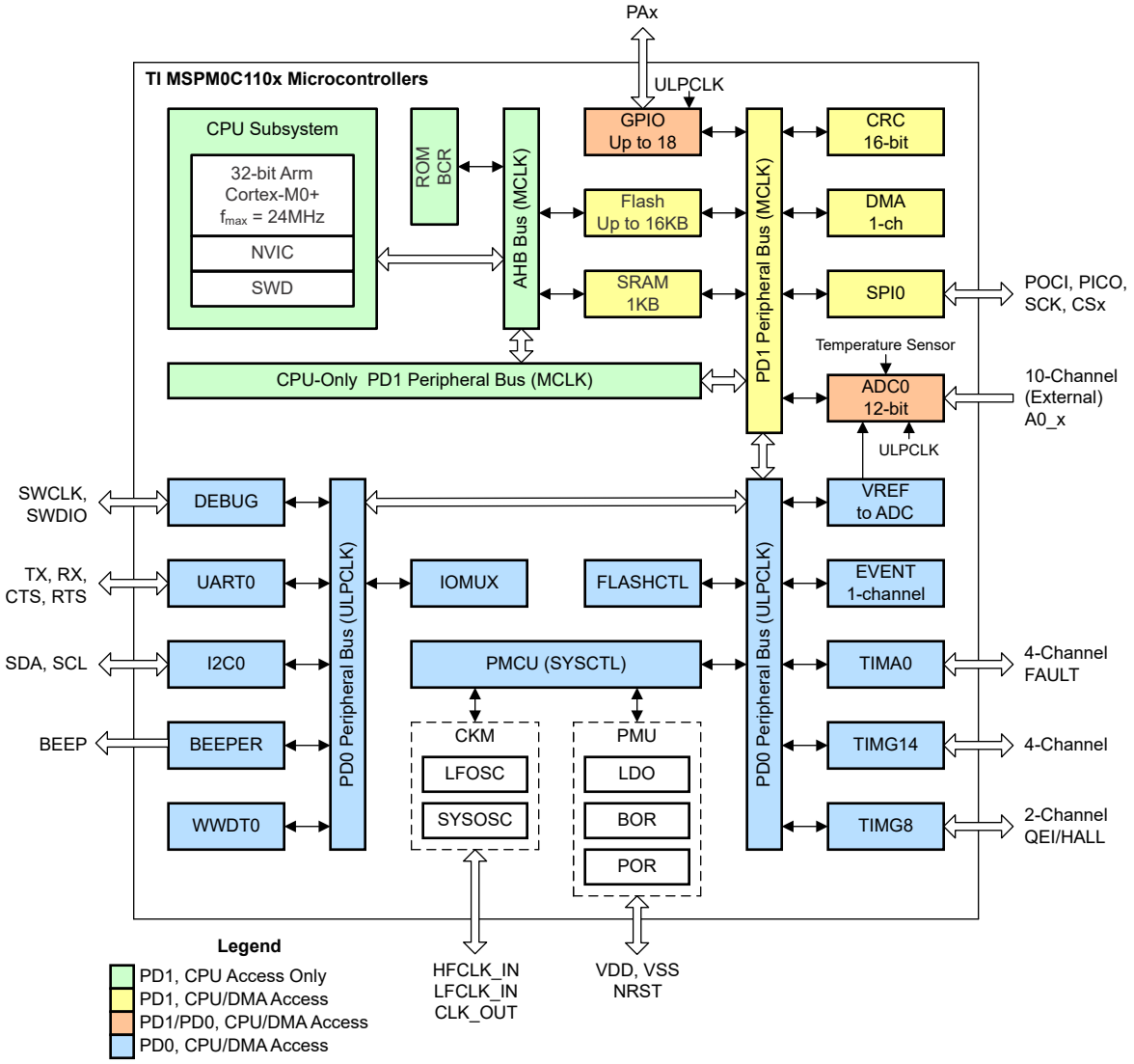

Figure 4-1. MSPM0C110x Functional Block Diagram

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5 Device Comparison

Table 5-1. Device Comparison

DEVICE NAME (1) (3)	FLASH / SRAM (KB)	ADC CHANNELS	UART / I2C / SPI	TIMG	TIMA	GPIOs	5V TOLERANT IO	PACKAGE [PACKAGE SIZE](2)
MSPS003F4SPW20R	16 / 1	9	1 / 1 / 1	2	1	17	2	20 TSSOP [6.5mm × 5.0mm]
MSPS003F3SPW20R	8 / 1							
MSPM0C1104SDGS20R	16 / 1	10	1 / 1 / 1	2	1	18	2	20 VSSOP [5.1mm × 4.9mm]
MSPM0C1103SDGS20R	8 / 1							
MSPM0C1104SRUKR	16/ 1	10	1 / 1 / 1	2	1	18	2	20 WQFN [3mm × 3mm]
MSPM0C1103SRUKR	8 / 1							
MSPM0C1104SDYYR	16 /1	8	1 / 1 / 1	2	1	14	2	16 SOT [4.2mm × 3.26mm]
MSPM0C1103SDYYR	8 / 1							
MSPM0C1104SDSGR	16 / 1	3	1 / 1 / 1	2	1	6	2	8 WSON [2mm × 2mm]
MSPM0C1103SDSGR	8 / 1							
MSPM0C1104SDDFR	16 / 1	3	1 / 1 / 1	2	1	6	2	8 SOT [2.9mm × 2.8mm]
MSPM0C1103SDDFR	8 / 1							
MSPM0C1104S8YCJR	16 / 1	3	1 / 1 / 1	2	1	6	2	8 DSBGA [1.6mm × 0.86mm]
MSPM0C1103S8YCJR	8 / 1							

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 12, or see the TI web site.
(2) The package size (length × width) is a nominal value and includes pins, where applicable. For package dimensions with tolerances, see the *Mechanical Data* in Section 12.
(3) For more information about the device name, see Section 10.1.

6 Pin Configuration and Functions

6.1 Pin Diagrams

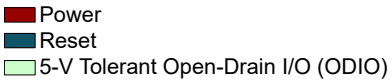


Figure 6-1. Pin Diagram Color Coding

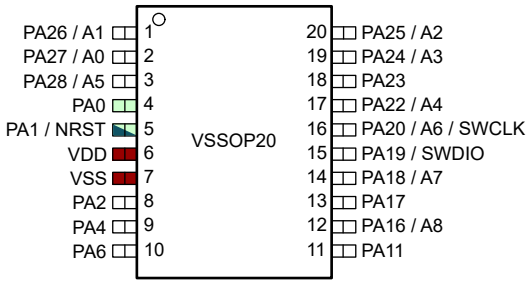


Figure 6-2. 20-Pin DGS20 (VSSOP) (Top View)

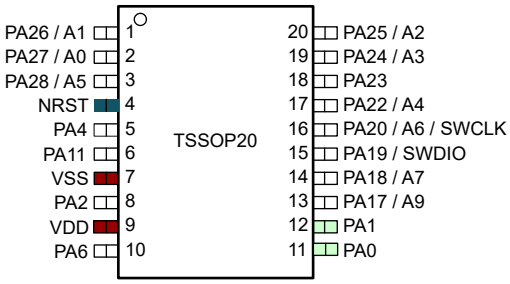


Figure 6-3. 20-Pin PW20 (TSSOP) (Top View)

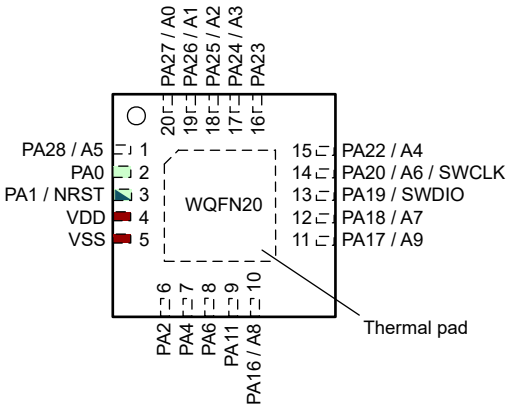


Figure 6-4. 20-Pin RUK (WQFN) (Top View)

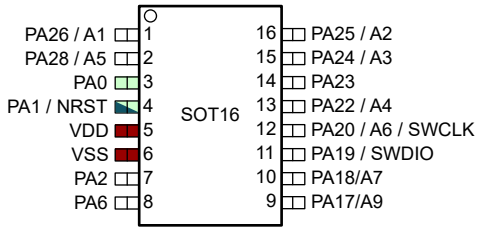


Figure 6-5. 16-Pin DYY (SOT) (Top View)

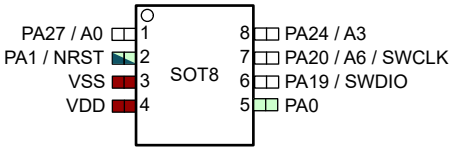


Figure 6-6. 8-Pin DDF (SOT) (Top View)

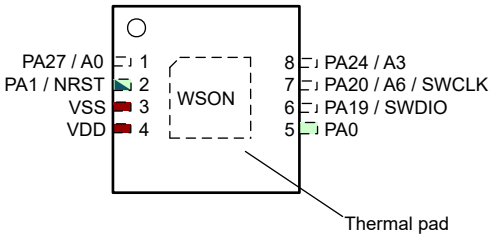


Figure 6-7. 8-Pin DSG (WSON) (Top View)

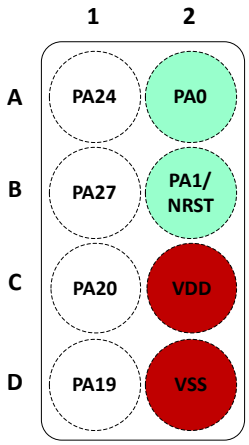


Figure 6-8. 8-Pin YCJ (DSBGA) (Bumps Down View)

6.2 Pin Attributes

The following table describes the functions available on every pin for each device package.

Note

Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Table 6-1. Pin Attributes

PINCMx	PIN FUNCTION			PIN NUMBER							I/O Structure
	PIN NAME	ANALOG	DIGITAL (1)	20 VSSOP	20 TSSOP	20 WQFN	16 SOT	8 SOT	8 WSON	8 DSBGA	
N/A	VDD			6	9	4	5	4	4	C2	Power
N/A	VSS			7	7	5	6	3	3	D2	Power
1	PA0		BEEP *[2]* / I2C0_SDA *[3]* / TIMG8_C0 *[4]* / SPI0_CS1 *[5]*/ FCC_IN *[6]*/ TIMA_FAL1 *[7]*	4	11	2	3	5	5	A2	5V Tolerant Open-Drain
2	PA1		I2C0_SCL *[2]* / TIM8_C0 *[3]* / HFCLK_IN *[4]*/ TIMA0_C1 *[5]*	5	12	3	4	2	2	B2	5V Tolerant Open-Drain
N/A		NRST			4						Reset
3	PA2		TIMG8_C1*[2]* / SPI0_CS0*[3]* / TIMA0_C0*[4]* / TIMG8_IDX*[5]*	8	8	6	7	-	-	-	Standard
5	PA4		TIMA0_C0N*[2]* / SPI0_POCI*[3]*/ LFCLK_IN*[4]*/ HFCLK_IN*[5]* / TIMA0_C1N*[6]*	9	5	7	-	-	-	-	Standard
7	PA6		TIMG14__C1*[2]* / SPI0_SCK*[3]* / TIMA0_C1*[4]* / TIMG14_C2*[5]* / SPI0_CS0*[6]* / TIMA_FAL0*[7]*	10	10	8	8	-	-	-	Standard
12	PA11		SPI0_SCK*[2]* / I2C0_SCL*[3]* / TIMA_FAL0*[4]*	11	6	9	-	-	-	-	Standard
17	PA16	A8	TIMA0_C1N*[2]* / SPI0_POCI*[3]* / TIMG14_C0*[4]* / FCC_IN*[5]*	12	-	10	-	-	-	-	Standard
18	PA17	A9	UART0_TX*[2]* / TIMA0_C0N*[3]* / SPI0_SCK*[4]* / TIMA0_C2*[5]* / SPI0_CS1*[6]* / TIMA0_C3*[7]*	13	13	11	9	-	-	-	Standard
19	PA18	A7	UART0_RX*[2]* / SPI0_PICO*[3]* / TIMA0_C1N*[4]* / CLK_OUT*[5]* / TIMA0_C3*[6]* / TIMA0_C3N*[7]*	14	14	12	10	-	-	-	Standard
20	PA19		SWDIO*[2]* / SPI0_SCK*[3]* / SPI0_POCI*[4]* / TIMA0_C2*[5]* / TIMG14_C0*[6]* / UART0_CTS*[7]*	15	15	13	11	6	6	D1	Standard
21	PA20	A6	SWCLK*[2]* / TIMA_FAL1*[3]* / SPI0_PICO*[4]* / TIMA0_C2N*[5]* / TIMA0_C0*[6]* / UART0_RTS*[7]*	16	16	14	12	7	7	C1	Standard
23	PA22	A4	UART0_RX*[2]* / SPI0_POCI*[3]* / UART0_RTS*[4]* / CLK_OUT*[5]* / TIMA0_C1*[6]*	17	17	15	13	-	-	-	Standard
24	PA23		UART0_TX*[2]* / SPI0_CS3*[3]* / TIMG14_C0*[4]* / UART0_CTS*[5]* / TIMA0_C3*[6]* / TIMG14_C1*[7]*	18	18	16	14	-	-	-	Standard
25	PA24	A3	SPI0_CS2*[2]* / TIMG14_C1*[3]* / UART0_RTS*[4]* / TIMG14_C2*[5]* / TIMA0_C3N*[6]* / UART0_RX*[7]*	19	19	17	15	8	8	A1	Standard
26	PA25	A2	TIMG14_C3*[2]* / UART0_TX*[3]* / SPI0_PICO*[4]* / TIMG14_C1*[5]* / TIMA_FAL2*[6]*	20	20	18	16	-	-	-	Standard
27	PA26	A1	TIMG8_C0*[2]* / UART0_RX*[3]* / SPI0_POCI*[4]* / BEEP*[5]* / TIMG14_C0*[6]* / TIMA_FAL0*[7]*	1	1	19	1	-	-	-	Standard
28	PA27	A0	TIMG8_C1*[2]* / SPI0_CS3*[3]* / TIMA0_C0N*[4]* / UART0_TX*[5]* / SPI0_POCI*[6]* / TIMA_FAL2*[7]*	2	2	20	-	1	1	B1	Standard

Table 6-1. Pin Attributes (continued)

PINCMx	PIN FUNCTION			PIN NUMBER							I/O Structure
	PIN NAME	ANALOG	DIGITAL (1)	20 VSSOP	20 TSSOP	20 WQFN	16 SOT	8 SOT	8 WSON	8 DSBGA	
29	PA28	A5	TIMA0_C0*[2]* / UART0_RX*[3]* / TIMG8_IDX*[4]*	3	3	1	2	-	-	-	Standard

(1) PINCM.PF and PINCM.PC in IOMUX must be set to 0 for analog functions like ADC inputs. Each digital I/O on a device is mapped to a specific Pin Control Management Register (PINCMx) that lets users configure the desired *Pin Function* using the PINCM.PF control bits.

Table 6-2. Digital IO Features by IO Type

IO Structure	INVERSION CONTROL	DRIVE STRENGTH CONTROL	HYSTERESIS CONTROL	PULLUP RESISTOR	PULLDOWN RESISTOR
Standard-drive	Y			Y	Y
5V tolerant open-drain	Y		Y		Y

6.3 Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO. (1)							PIN TYPE (2)	DESCRIPTION
		20 VSSOP	20 TSSOP	20 WQFN	16 SOT	8 SOT	8 WSON	8 DSBGA		
ADC	A0	2	2	20	-	1	1	B1	I	ADC0 analog input 0
	A1	1	1	19	1	-	-	-	I	ADC0 analog input 1
	A2	20	20	18	16	-	-	-	I	ADC0 analog input 2
	A3	19	19	17	15	8	8	A1	I	ADC0 analog input 3
	A4	17	17	15	13	-	-	-	I	ADC0 analog input 4
	A5	3	3	1	2	-	-	-	I	ADC0 analog input 5
	A6	16	16	14	12	7	7	C1	I	ADC0 analog input 6
	A7	14	14	12	10	-	-	-	I	ADC0 analog input 7
	A8	12	-	10	-	-	-	-	I	ADC0 analog input 8
	A9	13	13	11	9	-	-	-	I	ADC0 analog input 9
Clock	CLK_OUT	14, 17	14, 17	12, 15	10, 13	-	-	-	O	Configurable clock output
Debug	SWDIO	15	15	13	11	6	6	D1	I/O	Serial wire debug data input/output
	SWCLK	16	16	14	12	7	7	C1	I	Serial wire debug input clock

FUNCTION	SIGNAL NAME	PIN NO. (1)							PIN TYPE (2)	DESCRIPTION
		20 VSSOP	20 TSSOP	20 WQFN	16 SOT	8 SOT	8 WSON	8 DSBGA		
GPIO	PA0	4	11	2	3	5	5	A2	I/O	General-purpose digital I/O with open-drain capability
	PA1	5	12	3	4	2	2	B2	I/O	General-purpose digital I/O with open-drain capability
	PA2	8	8	6	7	-	-	-	I/O	General-purpose digital I/O
	PA4	9	5	7	-	-	-	-	I/O	General-purpose digital I/O
	PA6	10	10	8	8	-	-	-	I/O	General-purpose digital I/O
	PA11	11	6	9	-	-	-	-	I/O	General-purpose digital I/O
	PA16	12	-	10	-	-	-	-	I/O	General-purpose digital I/O
	PA17	13	13	11	9	-	-	-	I/O	General-purpose digital I/O
	PA18	14	14	12	10	-	-	-	I/O	General-purpose digital I/O
	PA19	15	15	13	11	6	6	D1	I/O	General-purpose digital I/O
	PA20	16	16	14	12	7	7	C1	I/O	General-purpose digital I/O
	PA22	17	17	15	13	-	-	-	I/O	General-purpose digital I/O
	PA23	18	18	16	14	-	-	-	I/O	General-purpose digital I/O
	PA24	19	19	17	15	8	8	A1	I/O	General-purpose digital I/O
	PA25	20	20	18	16	-	-	-	I/O	General-purpose digital I/O
	PA26	1	1	19	1	-	-	-	I/O	General-purpose digital I/O
	PA27	2	2	20	-	1	1	B1	I/O	General-purpose digital I/O
	PA28	3	3	1	2	-	-	-	I/O	General-purpose digital I/O
I^2C	I2C0_SCL	5, 11	6	3, 9	4	2	2	B2	I/O	I2C0 serial clock
	I2C0_SDA	4	11	2	3	5	5	A2	I/O	I2C0 serial data
Power	VSS	7	7	5	6	3	3	D2	P	Ground supply
	VDD	6	9	4	5	4	4	C2	P	Power supply
	QFN Pad	-	-	Pad	-	-	Pad	-	P	QFN package exposed thermal pad. TI recommends connection to V_{SS}.
SPI	SPI0_CS0	8	8	6	7	-	-	-	I/O	SPI0 chip-select 0
	SPI0_CS1	4, 13	11, 13	2, 11	3, 9	5	5	A2	I/O	SPI0 chip-select 1
	SPI0_CS2	19	19	17	15	8	8	A1	I/O	SPI0 chip-select 2
	SPI0_CS3	2, 18	2, 18	16, 20	14	1	1	B1	I/O	SPI0 chip-select 3
	SPI0_SCK	10, 11, 13, 15	6, 10, 13, 15	8, 9, 11, 13	8, 9, 11	6	6	D1	I/O	SPI0 clock signal input – SPI peripheral mode Clock signal output – SPI controller mode
	SPI0_POCI	1, 2, 9, 12, 15, 17	1, 2, 5, 15, 17	7, 10, 13, 15, 19, 20	1, 11, 13	1, 6	1, 6	D1, B1	I/O	SPI0 controller in/peripheral out
	SPI0_PICO	14, 16, 20	14, 16, 20	12, 14, 18	10, 12, 16	7	7	C1	I/O	SPI0 controller out/peripheral in
System	NRST	5	4	3	4	2	2	B2	I	Reset input active low

FUNCTION	SIGNAL NAME	PIN NO. (1)							PIN TYPE (2)	DESCRIPTION
		20 VSSOP	20 TSSOP	20 WQFN	16 SOT	8 SOT	8 WSON	8 DSBGA		
Timer	TIMA_FAL0	1, 10, 11	1, 6, 10	8, 9, 19	1, 8	-	-	-	I/O	Advanced control timer fault 0 handling input
	TIMA_FAL1	4, 16	11, 16	2, 14	3, 12	5, 7	5, 7	A2, C1	I/O	Advanced control timer fault 1 handling input
	TIMA_FAL2	2, 20	2, 20	18, 20	16	1	1	B1	I/O	Advanced control timer fault 2 handling input
	TIMA0_C0	2, 3, 8, 9, 13, 16	2, 3, 5, 8, 13, 16	1, 6, 7, 11, 14, 20	2, 7, 9, 12	1, 7	1, 7	B1, C1	I/O	Advanced control timer 0 CCR0 capture input/compare output
	TIMA0_C0N	2, 9, 13	2, 5, 13	7, 11, 20	9	1	1	B1	I/O	Advanced control timer 0 CCR0 capture input/compare output (inverting)
	TIMA0_C1	5, 9, 10, 12, 14, 17	5, 10, 12, 14, 17	3, 7, 8, 10, 12, 15	4, 8, 10, 13	2	2	B2	I/O	Advanced control timer 0 CCR1 capture input/compare output
	TIMA0_C1N	9, 12, 14	5, 14	7, 10, 12	10	-	-	-	I/O	Advanced control timer 0 CCR1 capture input/compare output (inverting)
	TIMA0_C2	13, 15, 16	13, 15, 16	11, 13, 14	9, 11, 12	6, 7	6, 7	C1, D1	I/O	Advanced control timer 0 CCR2 capture input/compare output
	TIMA0_C2N	16	16	14	12	7	7	C1	I/O	Advanced control timer 0 CCR2 capture input/compare output (inverting)
	TIMA0_C3	13, 14, 18, 19	13, 14, 18, 19	11, 12, 16, 17	9, 10, 14, 15	8	8	A1	I/O	Advanced control timer 0 CCR3 capture input/compare output
	TIMA0_C3N	14, 19	14, 19	12, 17	10, 15	8	8	A1	I/O	Advanced control timer 0 CCR3 capture input/compare output (inverting)
	TIMG14_C0	1, 12, 15, 18	1, 15, 18	10, 13, 16, 19	1, 11, 14	6	6	D1	I/O	General purpose timer 0 CCR0 capture input/compare output
	TIMG14_C1	10, 18, 19, 20	10, 18, 19, 20	8, 16, 17, 18	8, 14, 15, 16	8	8	A1	I/O	General purpose timer 0 CCR1 capture input/compare output
	TIMG14_C2	10, 19	10, 19	8, 17	8, 15	8	8	A1	I/O	General purpose timer 0 CCR2 capture input/compare output
	TIMG14_C3	20	20	18	16	-	-	-	I/O	General purpose timer 0 CCR3 capture input/ compare output
	TIMG8_C0	1, 4	1, 11	2, 19	1, 3	5	5	A2	I/O	General purpose timer 8 CCR0 capture input/compare output
	TIMG8_C1	2, 5, 8	2, 8, 12	3, 6, 20	4, 7	1, 2	1, 2	B1, B2	I/O	General purpose timer 8 CCR1 capture input/compare output
	TIMG8_IDX	3, 8	3, 8	1, 6	2, 7	-	-	-	I	General purpose timer 8 quadtrature encoder index pulse input

FUNCTION	SIGNAL NAME	PIN NO. (1)							PIN TYPE (2)	DESCRIPTION
		20 VSSOP	20 TSSOP	20 WQFN	16 SOT	8 SOT	8 WSON	8 DSBGA		
UART	UART0_TX	2, 13, 18, 20	2, 13, 18, 20	11, 16, 18, 20	9, 14, 16	1	1	B1	O	UART0 transmit data
	UART0_RX	1, 3, 14, 17, 19	1, 3, 14, 17, 19	1, 12, 15, 17, 19	1, 2, 10, 13, 15	8	8	A1	I	UART0 receive data
	UART0_CTS	15, 18	15, 18	13, 16	11, 14	6	6	D1	I	UART0 "clear to send" flow control input
	UART0_RTS	16, 17, 19	16, 17, 19	14, 15, 17	12, 13, 15	7, 8	7, 8	A1, C1	O	UART0 "request to send" flow control output
Beeper	BEEP	1, 4	1, 11	2, 19	1, 3	5	5	A2	O	Beep output
FCC	FCC_IN	4, 12	11	2, 10	3	5	6	A2	I	Frequency clock counter input

6.4 Connections for Unused Pins

Table 6-3 lists the correct termination of unused pins.

Table 6-3. Connection of Unused Pins

PIN (1)	POTENTIAL	COMMENT
PAx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.
NRST	VCC	NRST is an active-low reset signal. Pull high to VCC or the device cannot start. For more information, see Section 9.1.

(1) Any unused pin with a function that is shared with general-purpose I/O must follow the "PAx" unused pin connection guidelines.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
V_I	Input voltage	Applied to any 5-V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current of VDD pin	Current into VDD pin (source), -40 °C ≤ T_a ≤ 85 °C		80	mA
I_{VSS}	Current of VSS pin	Current out of VSS pin (sink), -40 °C ≤ T_a ≤ 85 °C		80	mA
I_{VDD}	Current of VDD pin	Current into VDD pin (source), -40 °C ≤ T_a ≤ 125 °C		48	mA
I_{VSS}	Current of VSS pin	Current out of VSS pin (sink), -40 °C ≤ T_a ≤ 125 °C		48	mA
I_{IO}	Current for SDIO pin	Current sunk or sourced by SDIO pin		6	mA
	Current for ODIO pin	Current sunk by ODIO pin		20	mA
I_D	Supported diode current	Diode current at any device pin except PA24		±2 (2)	mA
T_{stg}		Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) PA24 has an internal connection for the testing purpose, there is no injection current allowed on this pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage (2)	1.62 (3)		3.6	V
C_{VDD}	Capacitor placed between VDD and VSS (1)		10		uF
T_A	Ambient temperature	–40		125	°C
T_J	Max junction temperature			130	°C
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states			24	MHz

(1) Connect C_{VDD} between VDD/VSS, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD}.
(2) There is no dependency on MCLK frequency with respect to VDD recommended operating range.
(3) Functionality is guaranteed down to VBOR0-(min).

7.4 Thermal Information

THERMAL METRIC[1]		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	VSSOP-20 (DGS20)	91.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		29.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		48.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		47.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TSSOP-20 (PW20)	98.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		39.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		5.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		49.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	WQFN-20 (RUK)	52.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		55.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		26.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		12.0	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOT-16 (DYY)	117.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		54.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		54.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		54.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOT-8 (DDF)	142.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		65.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		62.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	WSON-8 (DSG)	70.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		85.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		37.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		37.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Supply Current Characteristics

7.5.1 RUN/SLEEP Modes

VDD=3.3V. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals are disabled.

PARAMETER		MCLK	-40°C		25°C		85°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
RUN Mode											
IDD_{RUN}	MCLK=SYSOSC, While(1), execute from flash	24MHz	2.06	2.20	2.08	2.35	2.09	2.40	2.21	2.45	mA
IDD_{RUN}, per MHz	MCLK=SYSOSC, While(1), execute from flash	24MHz	86	92	87	98	87	100	92	102	uA/Mhz
SLEEP Mode											
IDD_{SLEEP}	MCLK=SYSOSC, CPU is halted	24MHz	1115	1256	1132	1268	1149	1380	1214	1370	uA

7.5.2 STOP/STANDBY Modes

VDD=3.3V unless otherwise noted. All inputs tied to 0V or VDD. Outputs do not source or sink any current. All peripherals not noted are disabled.

PARAMETER		ULPCLK	-40°C		25°C		85°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
STOP Mode											
IDD_{STOP0}	SYSOSC=24MHz, DISABLESTOP=0	4MHz	598	640	609	646	622	710	662	733	uA
IDD_{STOP2}	SYSOSC off, DISABLESTOP=1, ULPCLK=LFCLK	32kHz	305	343	311	346	324	359	364	430	
STANDBY Mode											
IDD_{STBY0}	STOPCLKSTBY=0, TIMG8, TIMG14 and TIMA0 enabled	32kHz	3.8	8.3	5.1	14	17.8	35.4	57.4	93	uA
IDD_{STBY1}	STOPCLKSTBY=1, TIMG8, TIMG14 and TIMA0 enabled		3.4	8.5	5.1	14	17.5	35.1	57	93	
	STOPCLKSTBY=1, GPIOA enabled		3.4	8.5	5.0	14	17.5	35.2	57	93	

7.5.3 SHUTDOWN Mode

All inputs tied to 0V or VDD. Outputs do not source or sink any current. Core regulator is powered down.

PARAMETER		VDD	-40°C		25°C		85°C		125°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
IDD_{SHDN}	Supply current in SHUTDOWN mode	3.3V	140	320	200	350	428	932	1933	4680	nA

7.6 Power Supply Sequencing

7.6.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			0.1	V/us
		Falling (2)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising (1)	0.92	1.284	1.59	V
V_{POR-}		Falling (1)	0.87	1.236	1.54	V
$V_{HYS, POR}$	POR hysteresis	(1)	16	47	80	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	Cold start, rising (1)	1.48	1.54	1.615	V
V_{BOR0+}		Rising (1) (2)	1.57	1.59	1.61	
V_{BOR0-}		Falling (1) (2)	1.56	1.57	1.60	

7.6.1 POR and BOR (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR0, STBY}$	Brown-out reset voltage level 0 (default level)	STANDBY mode (1)	1.52	1.57	1.60	V
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1) (2)	2.15	2.17	2.23	V
V_{BOR1-}		Falling (1) (2)	2.11	2.14	2.19	
$V_{BOR1, STBY}$	Brown-out-reset voltage level 1	STANDBY mode (1)	2.07	2.14	2.19	V
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1) (2)	2.74	2.77	2.83	V
V_{BOR2-}		Falling (1) (2)	2.71	2.73	2.80	
$V_{BOR2, STBY}$	Brown-out-reset voltage level 2	STANDBY mode (1)	2.67	2.73	2.80	V
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1) (2)	2.88	2.96	3.04	V
V_{BOR3-}		Falling (1) (2)	2.85	2.93	3.01	
$V_{BOR3, STBY}$	Brown-out-reset voltage level 3	STANDBY mode (1)	2.83	2.92	3.00	V
$V_{HYS,BOR}$	Brown-out reset hysteresis	Level 0 (1)		14	18	mV
		Levels 1-3 (1)		34	41	
$T_{PD, BOR}$	BOR propagation delay	RUN/SLEEP/STOP mode			10	us
		STANDBY mode			100	us

(1) |dVDD/dt| ≤ 3V/s
(2) Device operating in RUN, SLEEP, or STOP mode.

7.6.2 Power Supply Ramp

Figure 7-1 gives the relationship of POR- POR+, BOR0-, and BOR0+ during power-up and power-down.

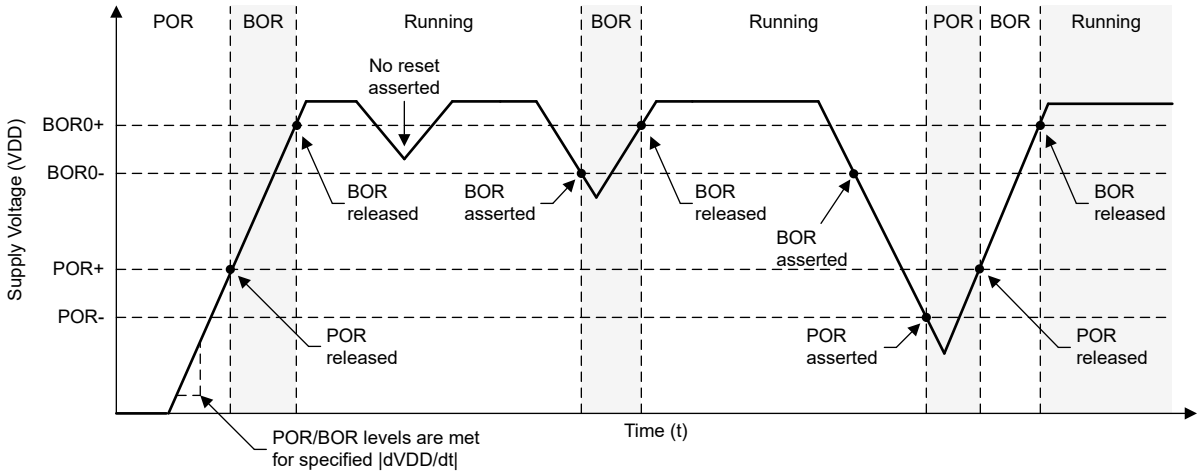


Figure 7-1. Power Cycle POR/BOR Conditions

7.7 Flash Memory Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
$VDD_{PGM/ERASE}$	Program and erase supply voltage		1.62		3.6	V
IDD_{ERASE}	Supply current from VDD during erase operation	Supply current delta		2		mA
IDD_{PGM}	Supply current from VDD during program operation	Supply current delta		2.5		mA
Endurance						

7.7 Flash Memory Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$NWEC_{(LOWER)}$	Erase/program cycle endurance		100			k cycles
$NE_{(MAX)}$	Total erase operations before failure (1)		802			k erase operations
$NW_{(MAX)}$	Write operations per word line before sector erase (1)				83	write operations
Retention						
t_{RET_85}	Flash memory data retention	-40°C <= Tj <= 85°C	60			years
t_{RET_105}	Flash memory data retention	-40°C <= Tj <= 105°C	11.4			years
t_{RET_130}	Flash memory data retention	-40°C <= Tj <= 130°C	2.4			years
Program and Erase Timing						
$t_{PROG\ (WORD,\ 64)}$	Program time for flash word (2)			40		µs
$t_{PROG\ (SEC,\ 64)}$	Program time for 1kB sector			5.1		ms
$t_{ERASE\ (SEC)}$	Sector erase time	<10k erase/program cycles		20	200	ms
$t_{ERASE\ (BANK)}$	Bank erase time	<10k erase/program cycles		22	220	ms

(1) Maximum number of write operations allowed per word line before the word line must be erased. If additional writes to the same word line are required, a sector erase is required once the maximum number of write operations per word line is reached.

(2) Sector program time is defined as the time from when the first word program command is triggered until the final word program command completes and the interrupt flag is set in the flash controller. This time includes the time needed for software to load each flash word (after the first flash word) into the flash controller during programming of the sector.

7.8 Timing Characteristics

VDD=3.3V, T_a=25 ℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wakeup Timing						
$t_{WAKE,\ SLEEP}$	Wakeup time from SLEEP to RUN			2		cycles
$t_{WAKE,\ STOP}$	Wakeup time from STOP0 to RUN (SYSOSC enabled)			14		us
	Wakeup time from STOP2 to RUN (SYSOSC disabled)			15		us
$t_{WAKE,\ STBY}$	Wakeup time from STANDBY to RUN			20		us
$t_{WAKE,\ SHDN}$	Wakeup time from SHUTDOWN to RUN			112		us
Asynchronous Fast Clock Request Timing						
t_{DELAY}	Delay time from edge of asynchronous request to first 24MHz MCLK edge	Mode is SLEEP2		1.2		us
		Mode is STOP2		1.2		us
		Mode is STANDBY1		5.0		us
Startup Timing						
$t_{START,\ RESET}$	Device cold start-up time from reset/ power-up (1)			210		us
NRST Timing						
$t_{RST,\ BOOTRST}$	Pulse length on NRST pin to generate BOOTRST	ULPCLK≥4MHz		2		us
		ULPCLK=32kHz		100		us
$t_{RST,\ POR}$	Pulse length on NRST pin to generate POR			1		s

(1) The start-up time is measured from the time that VDD crosses VBOR0+ (cold start-up) to the time that the first instruction of the user program is executed.

7.9 Clock Specifications

7.9.1 System Oscillator (SYSOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		24		MHz
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used (1)	SETUSEFCL=1, T_a = 25 ℃	-1.2		1.2	%
		SETUSEFCL=1, 0 ℃ ≤ T_a ≤ 85 ℃	-1.6		1.4	
		SETUSEFCL=1 -40 ℃ ≤ T_a ≤ 125 ℃	-2		1.4	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 24MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ ≤ T_a ≤ 125 ℃	-2.5		2.5	%
$t_{settle, SYSOSC}$	Settling time to target accuracy (2)	SETUSEFCL=1			30	us

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.

(2) When SYSOSC is enabled from a disabled state, the SYSOSC output will be released to the device within the time specified by $t_{start, SYSOSC}$. Once the output is released, the SYSOSC worst-case accuracy is specified by f_{settle}, SYSOSC. After the time specified by $t_{settle, SYSSOSC}$, the SYSOSC will have settled to the target f_{SYSOSC} accuracy.

7.9.2 Low Frequency Oscillator (LFOSC)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{LFOSC}	LFOSC frequency			32768		Hz
f_{LFOSC}	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 125 ℃	–5		5	%
f_{LFOSC}	LFOSC accuracy	-40 ℃ ≤ T_a ≤ 85 ℃	-3		3	%
I_{LFOSC}	LFOSC current consumption			300		nA
$t_{start, LFOSC}$	LFOSC start-up time			1.7		ms

7.10 Digital IO

7.10.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	ODIO (1)	VDD≥1.62V	0.7*VDD		5.5	V
		ODIO (1)	VDD≥2.7V	2		5.5	V
		All I/O except ODIO & Reset	VDD≥1.62V	0.7*VDD		VDD+0.3	V
V_{IL}	Low level input voltage	ODIO	VDD≥1.62V	-0.3		0.3*VDD	V
		ODIO	VDD≥2.7V	-0.3		0.8	V
		All I/O except ODIO & Reset	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	ODIO		0.05*VDD			V
		All I/O except ODIO		0.1*VDD			V
I_{lkg}	High-Z leakage current	SDIO(2) (3)	VDD = 3V			50	nA
R_{PU}	Pull up resistance	All I/O except ODIO	VIN = VSS		40		kΩ
R_{PD}	Pull down resistance		VIN = VDD		40		kΩ
C_I	Input capacitance		VDD = 3.3V		5		pF
V_{OH}	High level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA	VDD-0.5			V

7.10.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	SDIO	VDD ≥ 1.71V, $\|I_{IO}\|_{,max}$=2mA	VDD-0.4			V
V_{OL}	Low level output voltage	SDIO	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA			0.4	V
V_{OL}	Low level output voltage	ODIO	VDD≥2.7V, $I_{OL,max}$=8mA VDD≥1.71V, $I_{OL,max}$=4mA			0.5	V

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed
(2) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(3) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

7.10.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO (1)	VDD ≥ 1.71V, C_L= 20pF			24	MHz
f_{max}	Port output frequency	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF - 100pF			1	MHz
t_r,t_f	Output rise/fall time	All output ports except ODIO	VDD ≥ 1.71V			0.3*f_{max}	s
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM+, CL= 20pF-100pF	20*VDD/5.5		120	ns

(1) I/O Types: ODIO = 5V Tolerant Open-Drain , SDIO = Standard-Drive , HSIO = High-Speed , HDIO = High-Drive

7.11 ADC

7.11.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Vin_{(ADC)}$	Analog input voltage range(1)	Applies to all ADC analog input pins	0		VDD	V
V_{R+}	Positive ADC reference voltage	V_{R+} sourced from VDD		VDD		V
		V_{R+} sourced from internal reference (VREF)		VREF		V
V_{R-}	Negative ADC reference voltage			0		V
Fs	ADC sampling frequency	RES = 0x0 (12-bit mode), VDD Reference			1.5	Msps
		RES = 0x1 (10-bit mode), VDD Reference			1.7	
		RES = 0x2 (8-bit mode), VDD Reference			2	
F_S	ADC sampling frequency	RES = 0x0 (12-bit mode), Internal Reference			0.866	Msps
		RES = 0x1 (10-bit mode), Internal Reference			1	
		RES = 0x2 (8-bit mode), Internal Reference			1.2	
$I_{(ADC)}$	Operating supply current into VDD terminal	F_S = 1.5MSPS, V_{R+} = VDD		200	220	µA
		F_S = 0.856MSPS,V_{R+} = VREF = 2.5V (VREF power consumption included)		220	250	
$C_{S/H}$	ADC sample-and-hold capacitance			0.22		pF
Rin	ADC switch resistance			25		kΩ
ENOB	Effective number of bits	VDD reference (2)	9.3	10.4		bit
		VDD reference with over sampling		12.2		
		Internal reference, V_{R+} = VREF = 2.5V	9.4	9.8		
SNR	Signal-to-noise ratio	VDD reference (2)		64		dB
		VDD reference with over sampling		75		
		Internal reference, V_{R+} = VREF = 2.5V		61		
$PSRR_{DC}$	Power supply rejection ratio, DC	VDD = $VDD_{(min)}$ to $VDD_{(max)}$ Internal reference, V_{R+} = VREF = 2.5V		61		dB
T_{wakeup}	ADC Wakeup Time	Assumes internal reference is active			5	us

7.11.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all accuracy parameters are measured using 12-bit resolution mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SupplyMon}$	Supply Monitor voltage divider (VDD/3) accuracy	ADC input channel: Supply Monitor (3)	-0.6		+2.5	%
$I_{SupplyMon}$	Supply Monitor voltage divider current consumption	ADC input channel: Supply Monitor		10		uA

(1) The analog input voltage range must be within the selected ADC reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) VDD reference specifications are measured with V_{R+} = VDD = 3.3V and V_{R-} = VSS = 0V
(3) Analog power supply monitor. Analog input on channel 15 is disconnected and is internally connected to the voltage divider which is VDD/3.

7.11.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{ADCCLK}	ADC clock frequency		12		24	MHz
$t_{ADC\ trigger}$	Software trigger minimum width		3			ADCCLK cycles
t_{Sample_step}	Sampling time for step input	12-bit mode, R_S = 50Ω, C_{pext} = 10pF	0.166			µs
$t_{Sample\_SupplyMon}$	Sample time with Supply Monitor (VDD/3)		3			µs

7.11.3 Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted), all TYP values are measured at 25℃ and all linearity parameters are measured using 12-bit resolution mode (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (INL)	VDD reference, 10-bit (2)	-1.0		+1.0	LSB
		VDD reference, 12-bit (2)	-4.0		+4.0	LSB
E_D	Differential linearity error (DNL)	VDD reference, 10-bit (2)	-1.0		+1.0	LSB
		VDD reference, 12-bit (2)	-1.0		+4.0	LSB
E_O	Offset error	VDD reference, 10-bit (2)	-3		3	mV
		VDD reference, 12-bit (2)	-3		3	mV
E_G	Gain error	VDD reference, 10-bit (2)	-5		5	LSB
		VDD reference, 12-bit (2)	-25		25	LSB

(1) Total Unadjusted Error (TUE) can be calculated from E_I , E_O , and E_G using the following formula: TUE = $\sqrt{(E_I^2 + |E_O|^2 + E_G^2)}$
Note: You must convert all of the errors into the same unit, usually LSB, for the above equation to be accurate
(2) VDD reference specifications are measured with V_{R+} = VDD and V_{R-} = VSS = 0V.

7.11.4 Typical Connection Diagram

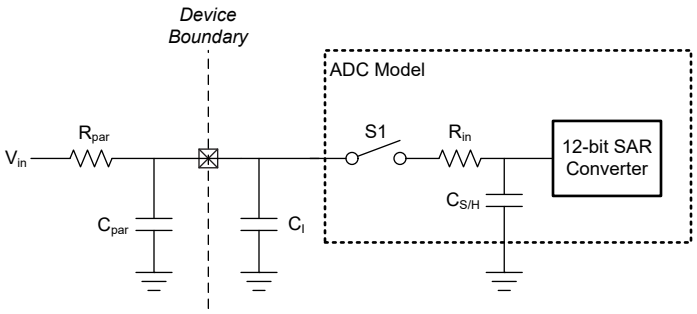


Figure 7-2. ADC Input Network

1. Refer to ADC Electrical Characteristics for the values of R_{in} and $C_{S/H}$
2. Refer to Digital IO Electrical Characteristics for the value of C_I

3. C_{par} and R_{par} represent the parasitic capacitance and resistance of the external ADC input circuitry

Use the following equations to solve for the minimum sampling time (T) required for an ADC conversion:

1. Tau = $(R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_I)$
2. K= $\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I)/C_{S/H})$
3. T (minimum sampling time) = K × Tau

7.12 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TS_{TRIM}	Factory trim temperature (1)		27	30	33	℃
TS_c	Temperature coefficient		-1.9	-1.8	-1.7	mV/℃
$t_{SET, TS}$	Temperature sensor settling time (2)	ADC and VREF configuration: RES=0 (12-bit mode), VRSEL=2h (VREF=1.4V), ADC CHANNEL=11		2.5	10	us

(1) Higher absolute accuracy may be achieved through user calibration.
(2) This is the minimum required ADC sampling time when measuring the temperature sensor.

7.13 VREF

7.13.1 Voltage Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum supply voltage needed for VREF operation	BUFCONFIG = 1	1.62			V
		BUFCONFIG = 0	2.7			
VREF	Voltage reference output voltage	BUFCONFIG = 1	1.378	1.4	1.421	V
		BUFCONFIG = 0	2.462	2.5	2.541	

7.13.2 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{VREF}	VREF operating supply current(this spec is an estimation and will be more reliable once the IP is further in the design phase)	BUFCONFIG = {0, 1}, No load	BUFCONFIG = {0, 1}, No load.		80	100	µA
TC_{VREF}	Temperature coefficient of VREF (1)	BUFCONFIG = {0, 1}	BUFCONFIG = {0, 1}			75	ppm/°C
TC_{drift}	Long term VREF drift	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25℃	Time = 1000 hours, BUFCONFIG = {0, 1}, T = 25℃			300	ppm
$T_{startup}$	VREF startup time	BUFCONFIG = {0, 1} , VDD = 2.7 V	BUFCONFIG = {0, 1} , VDD = 2.7 V			10	us

(1) The temperature coefficient of the VREF output is the sum of TC_{VRBUF} and the temperature coefficient of the internal bandgap reference.

7.14 I2C

7.14.1 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0		24		24		24	MHz
f_{SCL}	SCL clock frequency			100		400		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		ns
$t_{SU,DAT}$	Data setup time		250		100		50		ns
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	data valid acknowledge time			3.45		0.9		0.45	us

7.14.2 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		11	35	ns
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 1		14	35	ns
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 2		22	60	ns
f_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 3		35	90	ns

7.14.3 I²C Timing Diagram

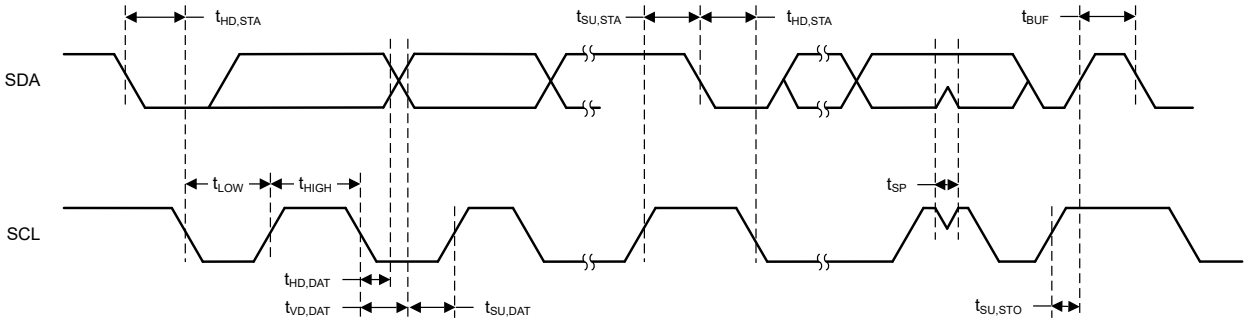


Figure 7-3. I2C Timing Diagram

7.15 SPI

7.15.1 SPI

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
f_{SPI}	SPI clock frequency	Clock max speed = 24MHz 1.62 < VDD < 3.6V Controller mode			12	MHz
f_{SPI}	SPI clock frequency	Clock max speed = 24MHz 1.62 < VDD < 3.6V Peripheral mode			12	MHz
DC_{SCK}	SCK Duty Cycle		40	50	60	%
Controller						
$t_{SCLK\_H/L}$	SCLK High or Low time		(tSPI/2) - 1	tSPI / 2	(tSPI/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		11			ns
$t_{CS.ACC}$	CS access time, CS active to PICO data out				93	ns
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				10	ns
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, delayed sampling enabled	1			ns
		1.62 < VDD < 2.7V, delayed sampling enabled	1			
$t_{SU.CI}$	POCI input data setup time (1)	2.7 < VDD < 3.6V, no delayed sampling	27			ns
		1.62 < VDD < 2.7V, no delayed sampling	35			
$t_{HD.CI}$	POCI input data hold time		9			ns
$t_{VALID.CO}$	PICO output data valid time (2)				10	ns
$t_{HD.CO}$	PICO output data hold time (3)		1			ns
Peripheral						
$t_{CS.LEAD}$	CS lead-time, CS active to clock		8			ns
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		0			ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out				50	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance				50	ns
$t_{SU.PI}$	PICO input data setup time		2			ns
$t_{HD.PI}$	PICO input data hold time		1			ns
$t_{VALID.PO}$	POCI output data valid time(2)	2.7 < VDD < 3.6V			34	ns
$t_{VALID.PO}$	POCI output data valid time(2)	1.62 < VDD < 2.7V			41	ns
$t_{HD.PO}$	POCI output data hold time(3)		5			ns

(1) The POCI input data setup time can be fully compensated when delayed sampling feature is enabled.
(2) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(3) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.15.2 SPI Timing Diagrams

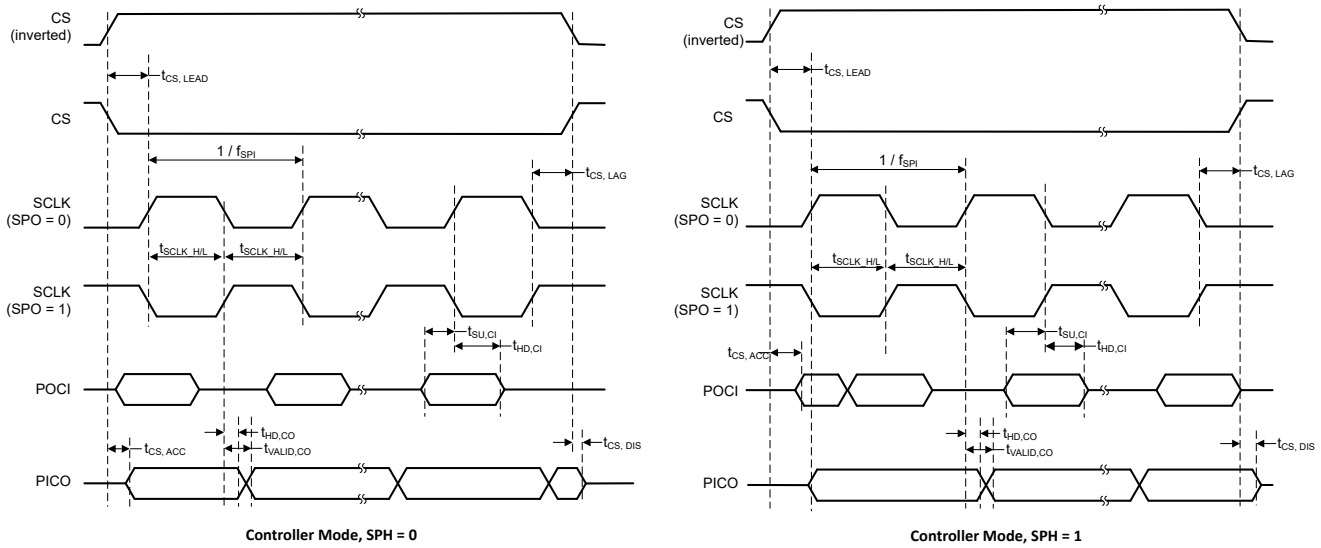


Figure 7-4. SPI Timing Diagram - Controller Mode

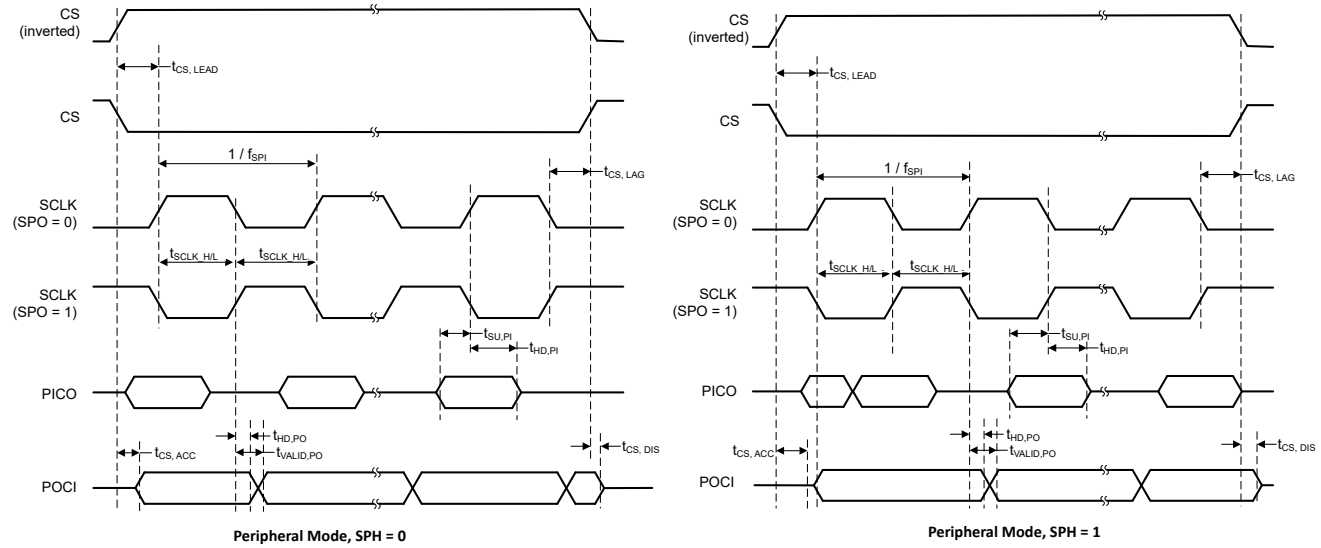


Figure 7-5. SPI Timing Diagram - Peripheral Mode

7.16 UART

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency				24	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				3	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		11	35	ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

7.17 TIMx

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{res}	Timer resolution time	$f_{TIMxCLK}$ = 24MHz	41.67			ns
			1			$t_{TIMxCLK}$
t_{res}	Timer resolution time	TIMx with 16bit counter			16	bit

7.18 Windowed Watchdog Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$WWDT_{FREQ}$	WWDT operating frequency			32.768		kHz
$WWDT_{Tstart}$	WWDT counter start time	Write to WWDTCTL0 until WWDT counter starts ($WWDT_{FREQ}$ = 32.768kHz)			30.5	µs
$WWDT_{Trestart}$	WWDT counter restart time	Write to WWDTCNTRST until WWDT counter restarts ($WWDT_{FREQ}$ = 32.768kHz)			30.5	µs

7.19 Emulation and Debug

7.19.1 SWD Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SWD}	SWD frequency				10	MHz

8 Detailed Description

The following sections describe all of the components that make up the devices in this data sheet. The peripherals integrated into these devices are configured by software through Memory Mapped Registers (MMRs). For more details, see the corresponding chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.1 CPU

The CPU subsystem (MCPUSS) implements an Arm Cortex-M0+ CPU, a system timer, and interrupt management features. The Arm Cortex-M0+ is a cost-optimized 32-bit CPU that delivers high performance and low power to embedded applications. Key features of the CPU Sub System include:

- Arm Cortex-M0+ CPU supports clock frequencies from 32kHz to 24MHz
  - ARMv6-M Thumb instruction set (little endian) with 32-cycle 32x32 slow multiply instruction
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail chaining

8.2 Operating Modes

MSPM0C MCUs provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. In order of decreasing power, the modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. The CPU is active executing code in RUN mode. Peripheral interrupt events can wake the device from SLEEP, STOP, or STANDBY mode to the RUN mode. SHUTDOWN mode completely disables the internal core regulator to minimize power consumption, and wake is only possible via NRST or SWD. RUN, SLEEP, STOP, and STANDBY modes also include several configurable policy options (for example, RUN.x) for balancing performance with power consumption.

To further balance performance and power consumption, MSPM0C devices implement two power domains: **PD1** (for the CPU, memories, and high performance peripherals), and **PD0** (for low speed, low power peripherals).

- **PD1** is always powered in RUN and SLEEP modes, but is disabled in all other modes.
- **PD0** is always powered in RUN, SLEEP, STOP, and STANDBY modes.
- PD1 and PD0 are both disabled in SHUTDOWN mode.

8.2.1 Functionality by Operating Mode (MSPM0C110x)

Table 8-1 lists the supported functionality in each operating mode.

Functional key:

- **EN**: The function is enabled in the specified mode.
- **DIS**: The function is disabled (either clock or power gated) in the specified mode, but the function's configuration is retained.
- **OPT**: The function is optional in the specified mode, and remains enabled if configured to be enabled.
- **NS**: The function is not automatically disabled in the specified mode, but use of the function is not supported.
- **OFF**: The function is fully powered off in the specified mode, and no configuration information is retained.

Table 8-1. Supported Functionality by Operating Mode

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT(1)	DIS	DIS	DIS	OFF
	LFOSC	EN										OFF

Table 8-1. Supported Functionality by Operating Mode (continued)

Operating Mode		RUN			SLEEP			STOP		STANDBY		SHUTDOWN
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP2	STANDBY0	STANDBY1	
Clocks	CPUCLK	24M	32k	32k	DIS							OFF
	MCLK to PD1	24M	32k	32k	24M	32k	32k	DIS				OFF
	ULPCLK to PD0	24M	32k	32k	24M	32k	32k	4M(1)	32k		DIS	OFF
	ULPCLK to TIMG14, TIMG8	24M	32k	32k	24M	32k	32k	4M(1)	32k			OFF
	MFCLK	OPT	DIS		OPT	DIS		OPT	DIS			OFF
	LFCLK	32k									DIS	OFF
	LFCLK to TIMG14, TIMG8	32k										OFF
	MCLK Monitor	OPT									DIS	OFF
PMU	POR Monitor	EN										
	BOR Monitor	EN										OFF
	Core Regulator	Full drive								Low drive		OFF
Core Functions	CPU	EN			DIS							OFF
	DMA	OPT						NS (triggers supported)				OFF
	Flash	EN						OPT		DIS		OFF
	SRAM	EN						OPT		DIS		OFF
PD1 Peripherals	SPI0	OPT						DIS				OFF
	CRC	OPT						DIS				OFF
PD0 Peripherals	TIMA0	OPT										OFF
	TIMG8	OPT										OFF
	TIMG14	OPT										OFF
	UART0	OPT									OPT(2)	OFF
	I2C0	OPT									OPT(2)	OFF
	GPIOA	OPT									OPT(2)	OFF
	WWDT0	OPT									DIS	OFF
Analog	ADC0	OPT							NS (triggers supported)			OFF
	VREF	OPT							NS			OFF
IOMUX and IO Wakeup		EN										DIS
Wake Sources		N/A			ANY IRQ			PD0 IRQ				NRST, SWD

(1) If STOP0 is entered from RUN1 (SYSOSC enabled but MCLK sourced from LFCLK), SYSOSC remains enabled as it was in RUN1, and ULPCLK remains at 32kHz as it was in RUN1. If STOP0 is entered from RUN2 (SYSOSC was disabled and MCLK was sourced from LFCLK), SYSOSC remains disabled as it was in RUN2, and ULPCLK remains at 32kHz as it was in RUN2.

(2) When using the STANDBY1 policy for STANDBY, only TIMG8, TIMG14 and TIMA0 are clocked. Other PD0 peripherals can generate an asynchronous fast clock request upon external activity but are not actively clocked.

8.3 Power Management Unit (PMU)

The power management unit (PMU) generates the internally regulated core supplies for the device and provides supervision of the external supply (VDD). The PMU also contains the bandgap voltage reference used by the PMU itself as well as analog peripherals. Key features of the PMU include:

- Power-on reset (POR) supply monitor
- Brown-out reset (BOR) supply monitor with early warning capability using three programmable thresholds
- Core regulator with support for RUN, SLEEP, STOP, and STANDBY operating modes to dynamically balance performance with power consumption

- Parity-protected trim to immediately generate a power-on reset (POR) in the event that a power management trim is corrupted

For more details, see the PMU chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.4 Clock Module (CKM)

The clock module provides the following oscillators:

- **LFOSC**: Internal low-frequency oscillator (32kHz)
- **SYSOSC**: Internal high-frequency oscillator (24MHz)
- **LFCKIN** : low-frequency digital clock input (32KHz)
- **HFCKIN**: high-frequency digital clock input (4 to 24MHz)

The following clocks are distributed by the clock module for use by the processor, bus, and peripherals:

- **MCLK**: Main system clock for PD1 peripherals, derived from SYSOSC or LFCLK, active in RUN and SLEEP modes
- **CPUCLK**: Clock for the processor (derived from MCLK), active in RUN mode
- **ULPCLK**: Ultra-low power clock for PD0 peripherals, active in RUN, SLEEP, STOP, and STANDBY modes
- **MFCLK**: 4MHz fixed mid-frequency clock for peripherals, available in RUN, SLEEP, and STOP modes
- **LFCLK**: 32kHz fixed low-frequency clock for peripherals or MCLK, active in RUN, SLEEP, STOP, and STANDBY modes
- **ADCCLK**: ADC clock, available in RUN, SLEEP and STOP modes
- **CLK_OUT**: Used to output a clock externally, available in RUN, SLEEP, STOP, and STANDBY modes

For more details, see the CKM chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.5 DMA

The direct memory access (DMA) controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA can be used to move data from ADC conversion memory to SRAM. The DMA reduces system power consumption by allowing the CPU to remain in low power mode, without having to awaken to move data to or from a peripheral.

The DMA in these devices support the following key features:

- 1 DMA transfer channel
- Direct peripheral to DMA trigger is supported only from ADC.
- Byte (8-bit), short word (16-bit), word (32-bit) and long word (64-bit) or mixed byte and word transfer capability
- Transfer counter block size supports up to 64k transfers of any data type
- Configurable DMA transfer trigger selection

Table 8-2 lists the available triggers for the DMA which are configured using the DMATCTL.DMATSEL control bits in the DMA memory mapped registers.

Table 8-2. DMA Trigger Mapping

TRIGGER 0:6	SOURCE
0	Software
1	Generic Subscriber 0 (FSUB_0)
2	Generic Subscriber 1 (FSUB_1)
3	ADC0 Publisher 2

8.6 Events

The event manager transfers digital events from one entity (for example, a peripheral) to another (for example, a second peripheral, the DMA or the CPU). The event manager implements event transfer through a defined

set of event publishers (generators) and subscribers (receivers) that are interconnected through an event fabric containing a combination of static and programmable routes.

Events that are transferred by the event manager include:

- Peripheral event transferred to the CPU as an interrupt request (IRQ) (Static Event)
  - Example: GPIO interrupt is sent to the CPU
- Peripheral event transferred to the DMA as a DMA trigger (DMA Event)
  - Example: ADC trigger to DMA to request a DMA transfer
- Peripheral event transferred to another peripheral to directly trigger an action in hardware (Generic Event)
  - Example: TIMx timer peripheral publishes a periodic event to the ADC subscriber port, and the ADC uses the event to trigger start-of-sampling

For more details, see the Event chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

Table 8-3. Generic Event Channels

A generic route is a point-to-point (1:1) route in which the peripheral publishing the event is configured to use the available generic route channel to publish the event to another entity. An entity can be another peripheral, a generic DMA trigger event, or a generic CPU event.

CHANID	Generic Route Channel Selection	Channel Type
0	No generic event channel selected	N/A
1	Generic event channel 1 selected	1 : 1

8.7 Memory

8.7.1 Memory Organization

Table 8-4 summarizes the memory map of the devices. For more information about the memory region detail, see the *Platform Memory Map* section in the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

Table 8-4. Memory Organization

Memory Region	Subregion	MSPM0C1103, MSPS003F3	MSPM0C1104, MSPS003F4
Code (Flash)	Flash	8KB(1) 0x0000.0000 to 0x0000.1FFF	16KB(1) 0x0000.0000 to 0x0000.3FFF
SRAM (SRAM)	SRAM	1KB 0x2000.0000 to 0x2000.03FF	1KB 0x2000.0000 to 0x2000.03FF
Peripheral	Peripherals	0x4000.0000 to 0x40FF.FFFF	0x4000.0000 to 0x40FF.FFFF
	Flash	0x0040.0000 to 0x0040.1FFF	0x0040.0000 to 0x0040.3FFF
	Configuration NVM	512 bytes 0x41C0.0000 to 0x41C0.0200	512 bytes 0x41C0.0000 to 0x41C0.0200
	FACTORY	0x41C4.0000 to 0x41C4.0080	0x41C4.0000 to 0x41C4.0080
Subsystem		0x6000.0000 to 0x7FFF.FFFF	0x6000.0000 to 0x7FFF.FFFF
System PPB		0xE000.0000 to 0xE00F.FFFF	0xE000.0000 to 0xE00F.FFFF

(1) Up to 100000 program and erase cycles.

8.7.2 Peripheral File Map

Table 8-5 lists the available peripherals and the register base address for each.

Table 8-5. Peripherals Summary

PERIPHERAL NAME	BASE ADDRESS	SIZE
VREF	0x40030000	0x2000
WWDT0	0x40080000	0x2000
TIMG14	0x40084000	0x2000

Table 8-5. Peripherals Summary (continued)

PERIPHERAL NAME	BASE ADDRESS	SIZE
TIMG8	0x40090000	0x2000
GPIO0	0x400A0000	0x2000
SYSCTL	0x400AF000	0x3000
DEBUGSS	0x400C7000	0x2000
EVENT	0x400C9000	0x3000
NVMNW	0x400CD000	0x2000
I2C0	0x400F0000	0x2000
UART0	0x40108000	0x2000
MCPUSS	0x40400000	0x2000
WUC	0x40424000	0x1000
IOMUX	0x40428000	0x2000
DMA	0x4042A000	0x2000
CRC	0x40440000	0x2000
SPI0	0x40468000	0x2000
ADC0	0x40004000	0x2000
TIMA0	0x40860000	0x2000
ADC0(1)	0x4055A000	0x2000

(1) Aliased region of ADC0 memory-mapped registers

8.7.3 Peripheral Interrupt Vector

Table 8-6 shows the IRQ number and the interrupt group number for each peripherals. There is only one group GROUP0 in this device.

Table 8-6. Interrupt Vector Number

PERIPHERAL NAME	NVIC IRQ	GROUP0 IIDX
WWDT0	0	0
DEBUGSS	0	2
NVMNW	0	3
SYSCTL	0	6
GPIO0	1	-
TIMG8	2	-
ADC	4	-
SPI0	9	-
UART0	15	-
TIMG14	16	-
TIMA0	18	-
I2C0	24	-
DMA	31	-

8.8 Flash Memory

A single bank of nonvolatile flash memory is provided for storing executable program code and application data.

Key features of the flash include:

- In-circuit program and erase operations supported across the entire recommended supply range
- Small 1KB sector sizes (minimum erase resolution of 1KB)
- Up to 100000 program and erase cycles

For a complete description of the flash memory, see the NVM chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.9 SRAM

MSPM0Cxx MCUs include a low-power high-performance SRAM memory with zero wait state access across the supported CPU frequency range of the device. SRAM memory can be used for storing volatile information such as the call stack, heap, global data, and code. The SRAM memory content is fully retained in RUN, SLEEP, STOP, and STANDBY operating modes and is lost in SHUTDOWN mode. A write protection mechanism is provided to allow the application to dynamically write protect the SRAM memory with 1KB resolution. Write protection is useful when placing executable code into SRAM to provide a level of protection against unintentional overwrites of code by either the CPU or DMA. Placing code in SRAM can improve performance of critical loops by enabling zero wait state operation and lower power consumption.

8.10 GPIO

The general purpose input/output (GPIO) peripheral lets the application write data out and read data in through the device pins. Through the use of the Port A GPIO peripheral, these devices support up to 18 GPIO pins.

The key features of the GPIO module include:

- 0 wait state MMR access from CPU
- Set, clear, or toggle multiple bits without the need of a read-modify-write construct in software
- "FastWake" feature enables low-power wakeup from STOP and STANDBY modes for any GPIO port
- User controlled input filtering

8.11 IOMUX

The IOMUX peripheral enables IO pad configuration and controls digital data flow to and from the device pins. The key features of the IOMUX include:

- IO pad configuration registers allow for programmable drive strength, speed, pullup or pulldown, and more
- Digital pin muxing allows for multiple peripheral signals to be routed to the same IO pad
- Pin functions and capabilities are user-configured using the PINCM register

For more details, see the IOMUX chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*..

8.12 ADC

The 12-bit analog-to-digital converter (ADC) module in these devices support fast 12-bit conversions with single-ended inputs.

ADC features include:

- 12-bit output resolution at up to 1.5-Msps with greater than 10-bit ENOB
- Up to 10 external input channels
- Internal channels for temperature sensing, supply monitoring, and analog signal chain
- Software selectable reference:
  - Configurable internal dedicated ADC reference voltage of 1.4V and 2.5V (VREF)
  - MCU supply voltage (VDD)
- Operates in RUN, SLEEP, and STOP modes and supports triggers from STANDBY mode

Table 8-7. ADC0 Channel Mapping

CHANNEL[0:7]	SIGNAL NAME	CHANNEL[8:15]	SIGNAL NAME
0	A0	8	A8
1	A1	9	A9
2	A2	10	-
3	A3	11	*Temperature Sensor*
4	A4	12	-
5	A5	13	-
6	A6	14	-
7	A7	15	*Supply/Battery Monitor*

Italicized signal names are internal to the SoC. These signals are used for internal peripheral interconnections.

For more details, see the ADC chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.13 Temperature Sensor

The temperature sensor provides a voltage output that changes linearly with device temperature. The temperature sensor output is internally connected to one of ADC input channels to enable a temperature-to-digital conversion.

A unit-specific single-point calibration value for the temperature sensor is provided in the factory constants memory region. This calibration value represents the ADC conversion result (in ADC code format) corresponding to the temperature sensor being measured in 12-bit mode with the 1.4V internal VREF at the factory trim temperature (TS_{TRIM}). This calibration value can be used with the temperature sensor temperature coefficient (TS_c) to estimate the device temperature. See the temperature sensor section of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual* for guidance on estimating the device temperature with the factory trim value.

8.14 VREF

The voltage reference module (VREF) in these devices contains a configurable voltage reference buffer dedicated for the on-board ADC.

VREF features include:

- 1.4V and 2.5V user-selectable internal references
- Internal reference supports ADC operation up to 1Msps at 10-bit mode

For more details, see the VREF chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.15 CRC

The cyclical redundancy check (CRC) module provides a signature for an input data sequence. Key features of the CRC module include:

- Support for 16-bit CRC based on CRC16-CCITT
- Support for bit reversal

For more details, see the CRC chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.16 UART

The UART peripherals provide the following key features:

- Standard asynchronous communication bits for start, stop, and parity
- Fully programmable serial interface
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation
  - Line-break detection
  - Glitch filter on the input signals
  - Programmable baud rate generation with oversampling by 16, 8, or 3
  - Local Interconnect Network (LIN) mode support
- Separated transmit and receive FIFOs
- Support transmit and receive loopback mode operation
- See Table 8-8 for detail information on supported protocols

Table 8-8. UART Features

UART FEATURES	UART0 (Extend)
Active in stop and standby modes	Yes
Separate transmit and receive FIFOs	Yes
Support hardware flow control	Yes
Support 9-bit configuration	Yes
Support LIN mode	Yes
Support DALI	Yes
Support IrDA	Yes
Support ISO7816 Smart Card	Yes
Support Manchester coding	Yes

For more details, see the UART chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.17 SPI

The serial peripheral interface (SPI) peripherals in these devices support the following key features:

- Support ULPCLK/2 bit rate and up to 12 Mbits/s in both controller and peripheral modes
- Configurable as a controller or a peripheral
- Configurable chip select for both controller and peripheral
- Programmable clock prescaler and bit rate
- Programmable data frame size from 4 bits to 16 bits (controller mode)
- Programmable data frame size from 7 bits to 16 bits (peripheral mode)
- Separated transmit and receive FIFOs
- Supports TI mode, Motorola mode, and National Microwire format

For more details, see the SPI chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.18 I2C

The inter-integrated circuit interface (I^2C) peripherals in these devices provide bidirectional data transfer with other I2C devices on the bus and support the following key features:

- 7-bit and 10-bit addressing mode with multiple 7-bit target addresses
- Multiple-controller transmitter or receiver mode
- Target receiver or transmitter mode with configurable clock stretching
- Support Standard-mode (Sm), with a bit rate up to 100 kbit/s
- Support Fast-mode (Fm), with a bit rate up to 400 kbit/s
- Support Fast-mode Plus (Fm+), with a bit rate up to 1 Mbit/s
- Separated transmit and receive FIFOs
- Support SMBus 3.0 with PEC, ARP, timeout detection, and host support
- Wakeup from low-power mode on address match
- Support analog and digital glitch filter for input signal glitch suppression

For more details, see the I2C chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.19 WWDT

The windowed watchdog timer (WWDT) can be used to supervise the operation of the device, specifically code execution. The WWDT can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of the WWDT include:

- 25-bit counter
- Programmable clock divider
- Eight software selectable watchdog timer periods
- Eight software selectable window sizes
- Support for stopping the WWDT automatically when entering a sleep mode
- Interval timer mode for applications which do not require watchdog functionality

For more details, see the WWDT chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*

8.20 Timers (TIMx)

The timer peripherals in these devices support the following key features. For specific configuration, see Table 8-9.

Specific features for the **general-purpose timer (TIMGx)** include:

- 16-bit down, up/down, or up counter with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Two independent channels for
  - Output compare
  - Input capture

  - PWM output
  - One-shot mode
- Support quadrature encoder interface (QEI) for positioning and movement sensing
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Cross-trigger event logic for Hall sensor inputs

Specific features for the **advanced timer (TIMAx)** include:

- 16-bit down or up-down counter, with repeat-reload mode
- Selectable and configurable clock source
- 8-bit programmable prescaler to divide the counter clock frequency
- Repeat counter to generate an interrupt or event only after a given number of cycles of the counter
- Up to four independent channels for
  - Output compare
  - Input capture
  - PWM output
  - One-shot mode
- Shadow register for load and CC register available
- Complementary output PWM
- Asymmetric PWM with programmable dead band insertion
- Fault handling mechanism to keep the output signals in a safe user-defined state when a fault condition is encountered
- Support synchronization and cross trigger among different TIMx instances in the same power domain
- Support interrupt trigger generation and cross peripherals (such as ADC) trigger capability
- Two additional capture/compare channels for internal events

Table 8-9. TIMx Configurations

TIMER NAME	POWER DOMAIN	RESOLUTION	PRESCALER	REPEAT COUNTER	CAPTURE / COMPARE CHANNELS	PHASE LOAD	SHADOW LOAD	SHADOW CC	DEAD-BAND	FAULT	QEI
TIMG14	PD0	16 bit	8 bit	–	4	–	–	–	–	–	–
TIMG8	PD0	16 bit	8 bit	–	2	–	–	–	–	–	Yes
TIMA0	PD1	16 bit	8 bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	–

For more details, see the timer chapters of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

8.21 Device Analog Connections

Figure 8-1 shows the internal analog connection of the device.

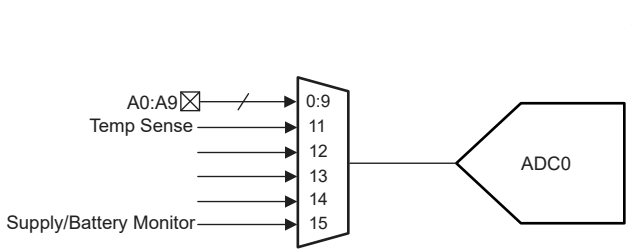


Figure 8-1. Analog Connections

8.22 Input/Output Diagrams

The IOMUX manages the selection of which peripheral function is to be used on a digital IO and provides the controls for the output driver and input path. For more information, see the IOMUX section of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

The mixed-signal IO pin slice diagram for a full featured IO pin is shown in Figure 8-2. Not all pins have analog functions, drive strength control, and pullup or pulldown resistors available.

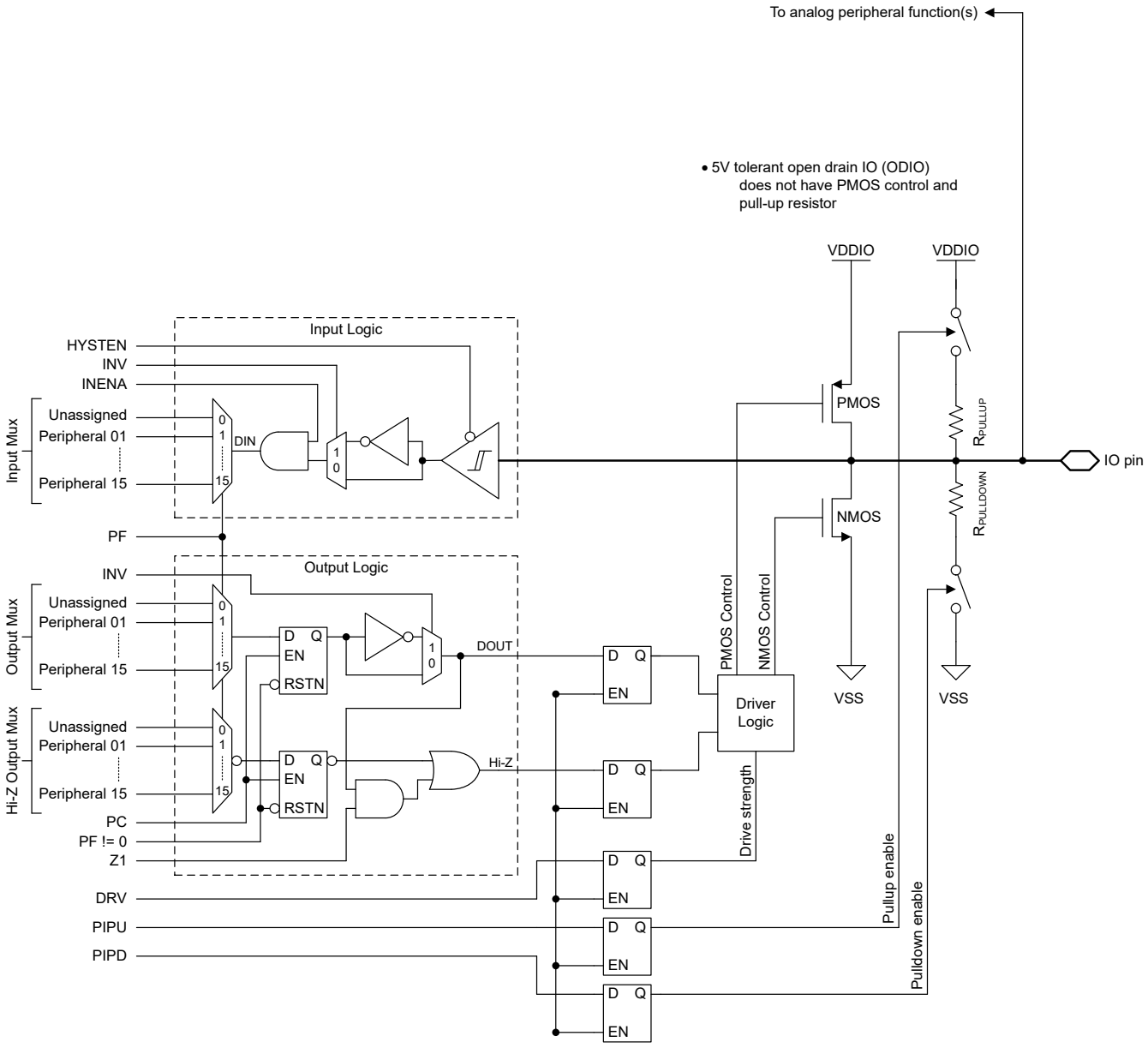


Figure 8-2. Superset Input/Output Diagram

8.23 Serial Wire Debug Interface

A serial wire debug (SWD) two-wire interface is provided via an Arm compatible serial wire debug port (SW-DP) to enable access to multiple debug functions within the device. For a complete description of the debug functionality offered on MSPM0 devices, see the debug chapter of the technical reference manual.

Table 8-10. Serial Wire Debug Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

8.24 Device Factory Constants

All devices include a memory-mapped FACTORY region which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. See the *Factory Constants* section of the MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual.

Table 8-11. DEVICEID

DEVICEID address is 0x41C4.0004, PARTNUM is bit 12 to 27, MANUFACTURER is bit 1 to 11.

Device	DEVICEID.PARTNUM	DEVICEID.MANUFACTURER
MSPM0C1103	0xBBA1	0x17
MSPM0C1104	0xBBA1	0x17

Table 8-12. USERID

USERID address is 0x41C4.0008, PART is bit 0 to 15, VARIANT is bit 16 to 23

Device	PART	VARIANT	Device	PART	VARIANT
MSPS003F4SPW20R	0x57B3	0x70	MSPS003F3SPW20R	0xD2B6	0x2
MSPM0C1104SDGS20R	0x57B3	0x71	MSPM0C1103SDGS20R	0xD2B6	0x4
MSPM0C1104SRUKR	0x57B3	0x73	MSPM0C1103SRUKR	0xD2B6	0x7
MSPM0C1104SDYYR	0x57B3	0x75	MSPM0C1103SDYYR	0xD2B6	0xA
MSPM0C1104SDDFR	0x57B3	0x77	MSPM0C1103SDDFR	0xD2B6	0xC
MSPM0C1104SDSGR	0x57B3	0x79	MSPM0C1103SDSGR	0xD2B6	0xE

8.25 Identification

Revision and Device Identification

The hardware revision and device identification values are stored in the memory-mapped FACTORY region (see the Device Factory Constants section) which provides read-only data describing the capabilities of a device as well as any factory-provided trim information for use by application software. For more information, see the *Factory Constants* chapter of the *MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual*.

The device revision and identification information are also included as part of the top-side marking on the device package. The device-specific errata describes these markings.

9 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 Schematic

TI recommends connecting a combination of a 10-µF and a 0.1-µF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used but can affect the supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins (within a few millimeters).

PA1 and NRST are double bonded for some variants. If it's used as a NRST, it must connect an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor.

For 5V-tolerant open drain (ODIO), a pullup resistor is required to output high for I2C and UART functions if the ODIO are used.

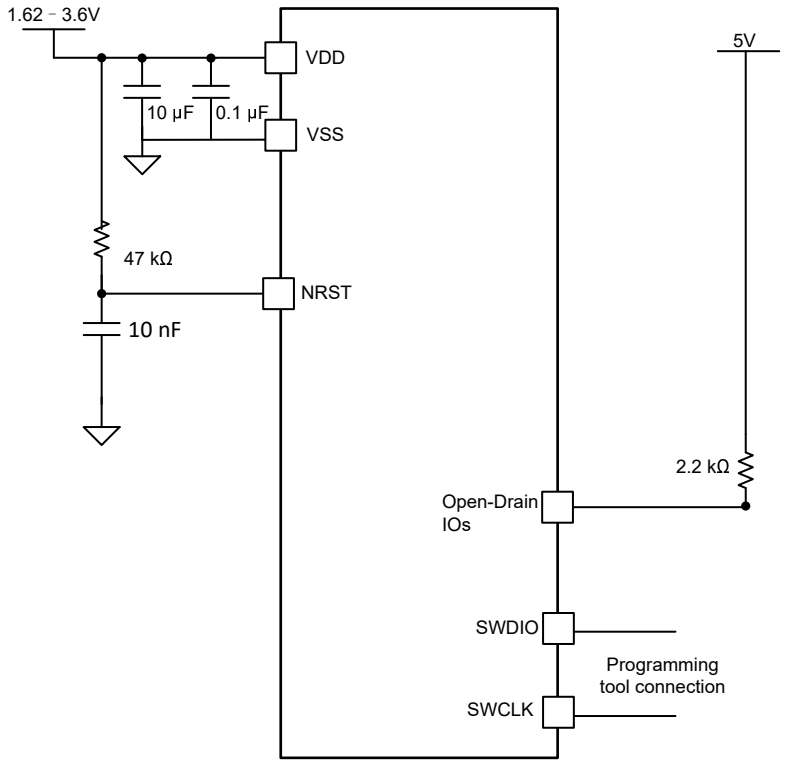


Figure 9-1. Typical Application Schematic

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices and support tools. . Each MSP MCU commercial family member has one of two prefixes: MSP or X. These prefixes represent evolutionary stages of product development from engineering prototypes (X) through fully qualified production devices (MSP).

X – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

X devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes." MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies. Predictions show that prototype devices (X) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 10-1 provides a legend for reading the complete device name.

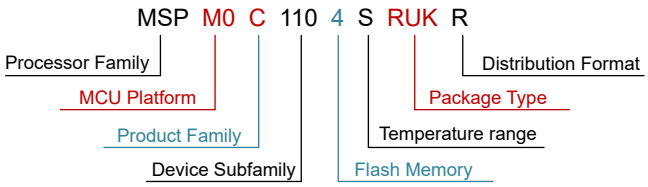


Figure 10-1. Device Nomenclature

Table 10-1. Device Nomenclature

Processor Family	MSP = Mixed-signal processor X= Experimental silicon
MCU Platform	M0 = Arm-based 32-bit M0+
Product Family	C = 24MHz frequency
Device Subfamily	110 = ADC
Flash Memory	3 = 8KB 4 = 16KB
Temperature Range	S = –40°C to 125°C
Package Type	See Table 5-1 and www.ti.com/packaging
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray

For orderable part numbers of MSP devices in different package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

10.2 Tools and Software

Design Kits and Evaluation Modules

MSPM0 LaunchPad (LP) Boards: LP-MSPM0C1104	Empowers you to immediately start developing on the industry's best integrated analog and most cost-optimized general purpose MSPM0 MCU family. Exposes all device pins and functionality; includes some built-in circuitry, out-of-box software demos, and on-board XDS110 debug probe for programming, debugging, and EnergyTrace™ technology. The LP ecosystem includes dozens of BoosterPack™ stackable plug-in modules to extend functionality.

Embedded Software

MSPM0 Software Development Kit (SDK)	Contains software drivers, middleware libraries, documentation, tools, and code examples that create a familiar and easy user experience for all MSPM0 devices.

Software Development Tools

TI Cloud Tools	Start your evaluation and development on a web browser without any installation. Cloud tools also have a downloadable, offline version.
TI Resource Explorer	Online portal to TI SDKs. Accessible in CCS IDE or in TI Cloud Tools.
SysConfig	Intuitive GUI to configure device and peripherals, resolve system conflicts, generate configuration code, and automate pin mux settings. Accessible in CCS IDE or in TI Cloud Tools. (offline version)
MSP Academy	Great starting point for all developers to learn about the MSPM0 MCU Platform with training modules that span a wide range of topics. Part of TIRex.
GUI Composer	GUIs that simplify evaluation of certain MSPM0 features, such as configuring and monitoring a fully integrated analog signal chain without any code needed.

IDE and compiler tool chains

Code Composer Studio™ (CCS)	Includes TI Arm-Clang compiler. Supports all TI Arm Cortex MCUs and boasts competitive code size performance advantages, fast compile time, code coverage support, safety certification support, and completely free to use.
IAR Embedded Workbench® IDE	
Keil® MDK IDE	
GNU Arm Embedded Tool Chain	

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

LaunchPad™, Code Composer Studio™, TI E2E™, EnergyTrace™, and BoosterPack™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2024) to Revision C (February 2025)	Page
• Added DSBGA package to Device Comparison	5
• Added DSBGA to Table 6-1	8
• Added DSBGA to Section 6.3	9

12 Mechanical, Packaging, and Orderable Information

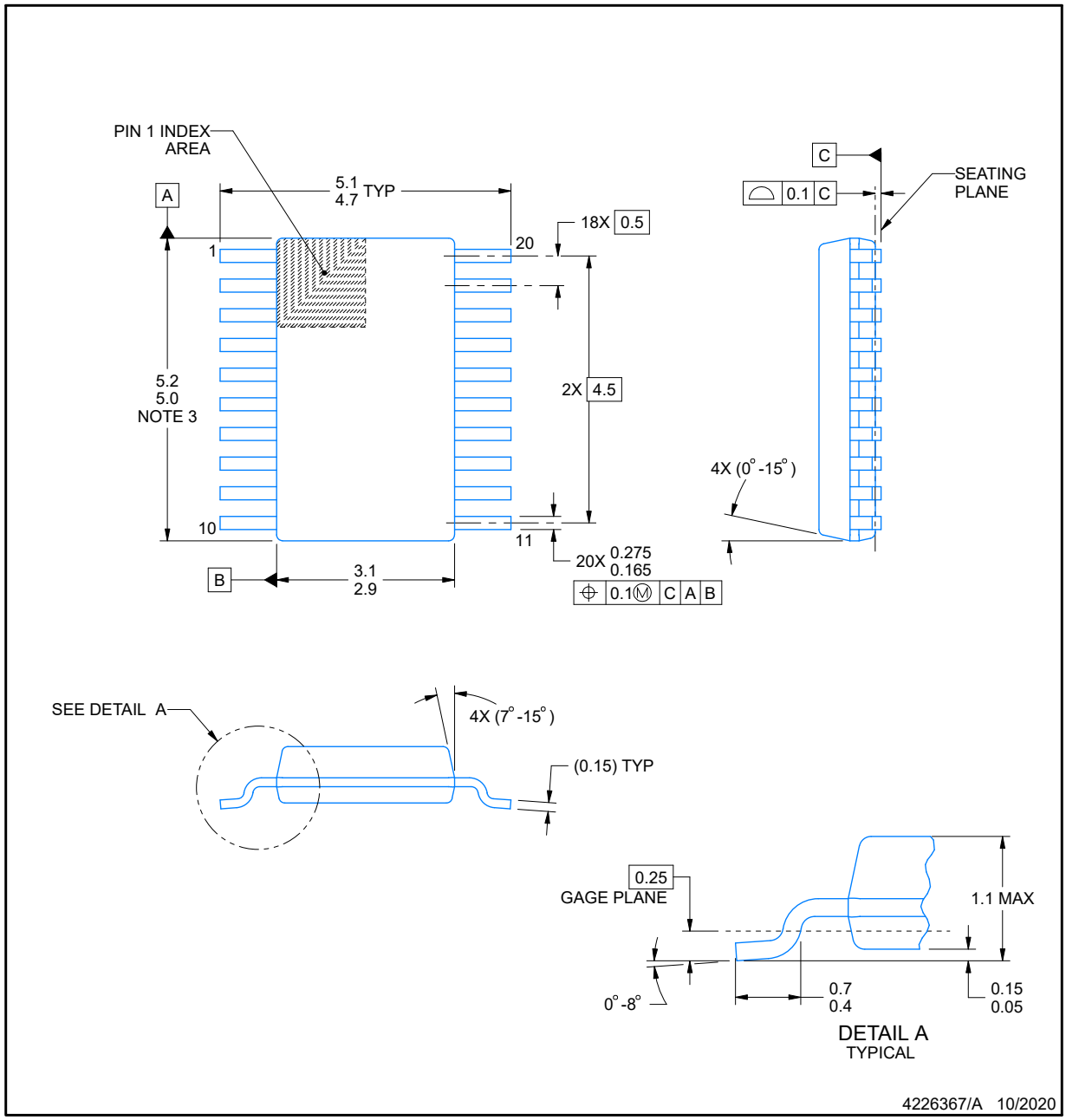
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

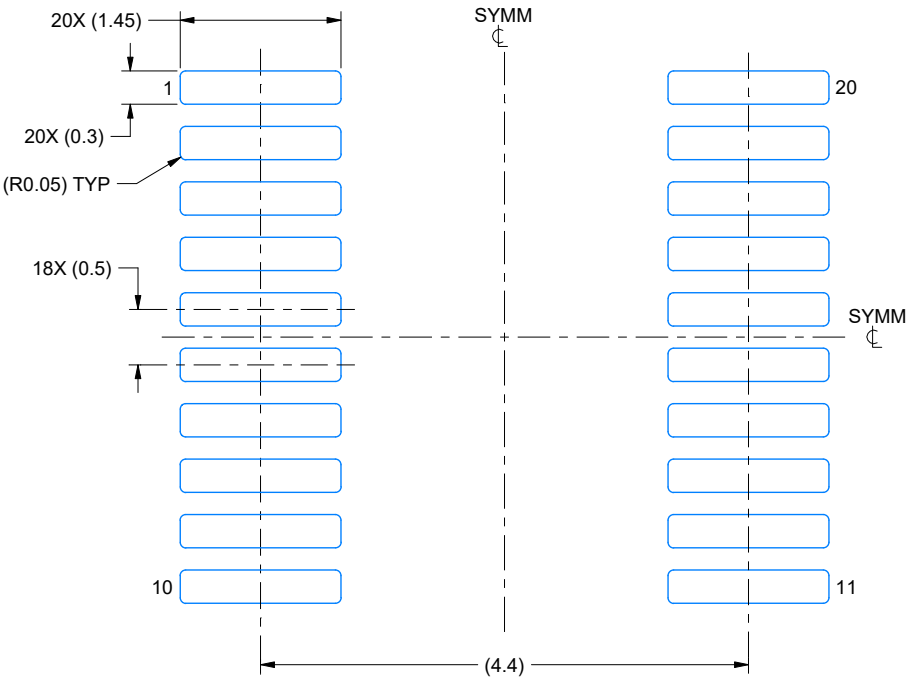
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

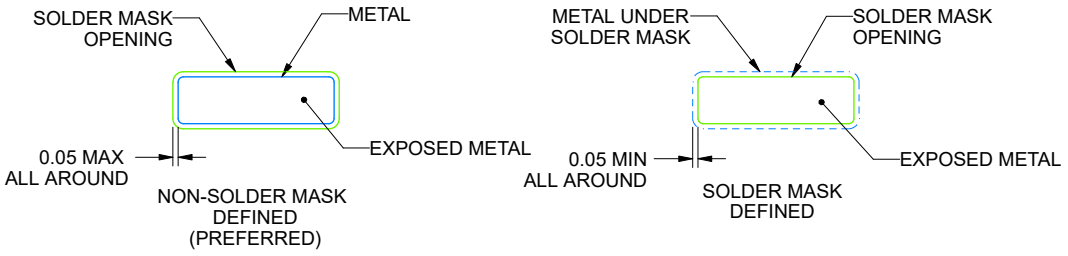
DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE: 16X



SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

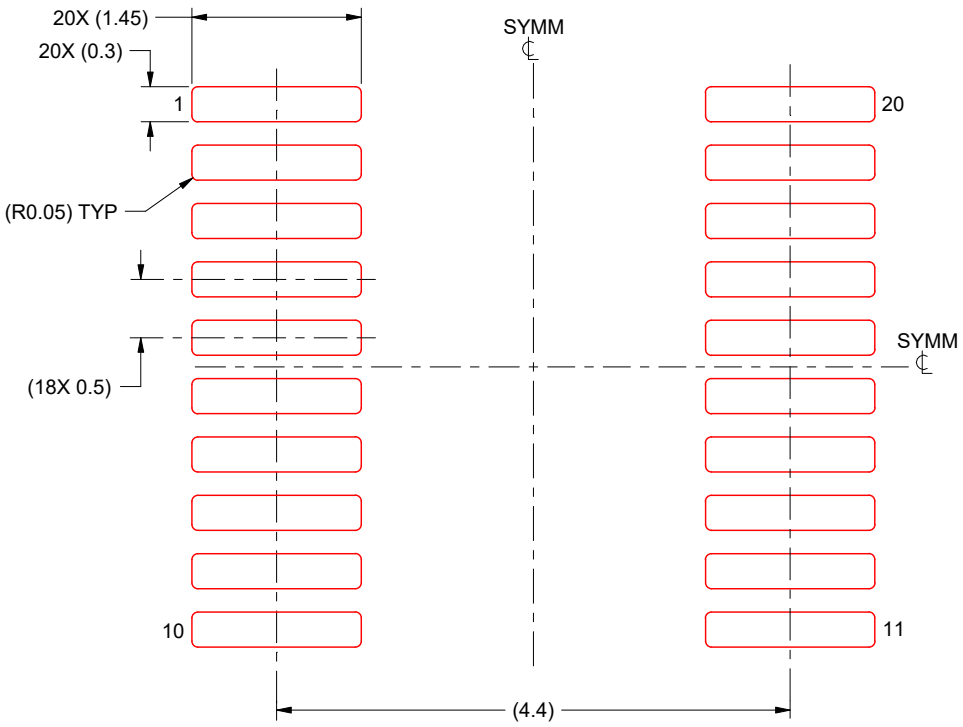
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

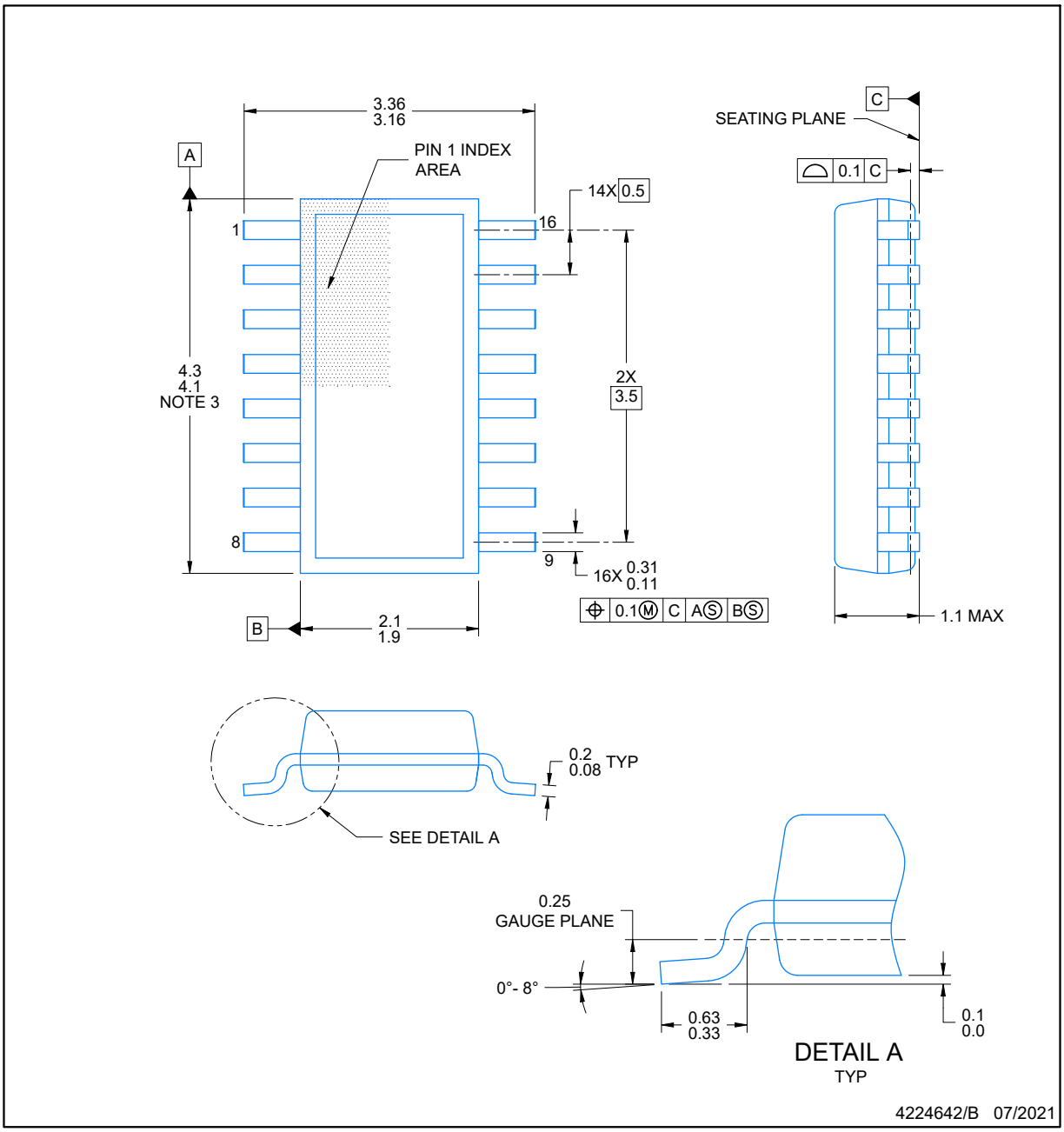
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0016A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

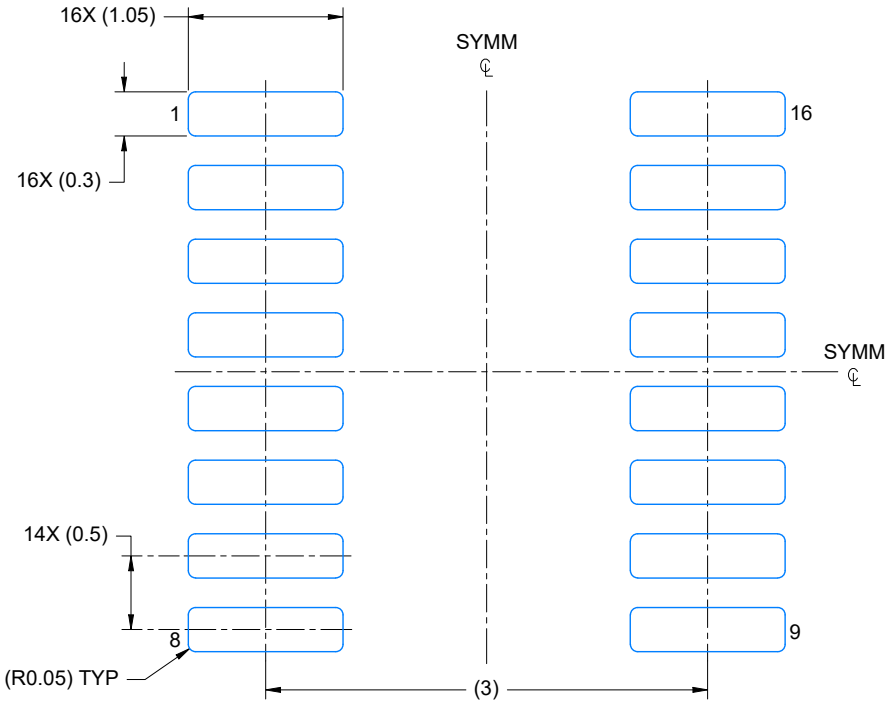
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA

EXAMPLE BOARD LAYOUT

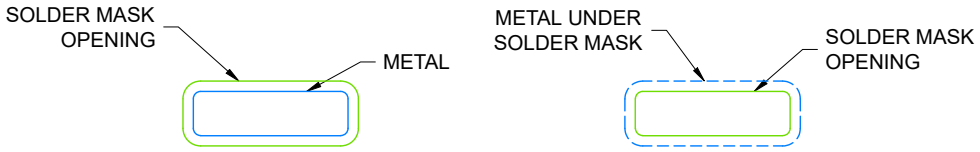
DYY0016A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224642/B 07/2021

NOTES: (continued)

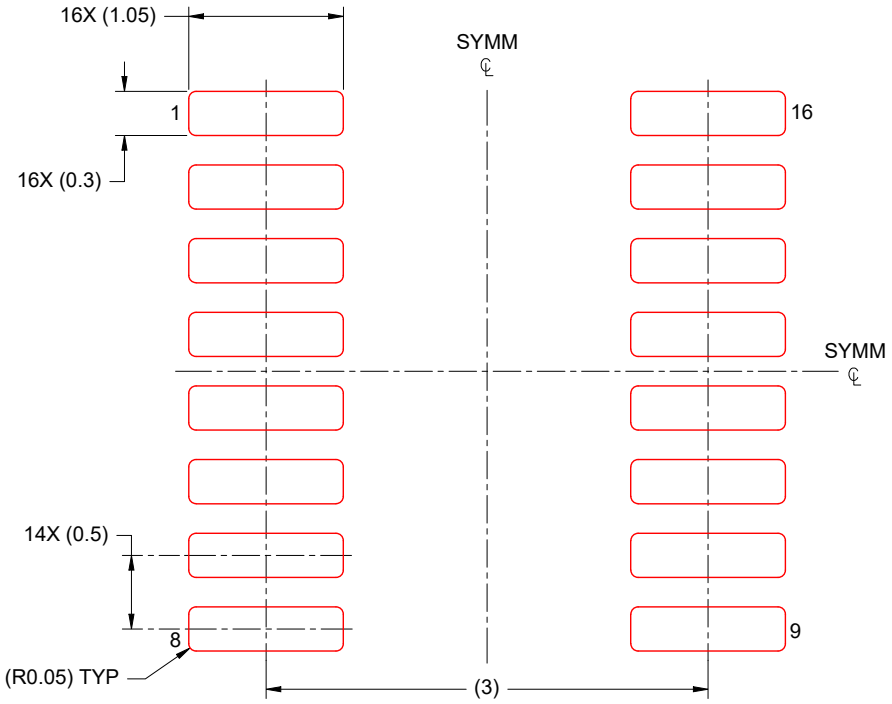
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYY0016A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/B 07/2021

NOTES: (continued)

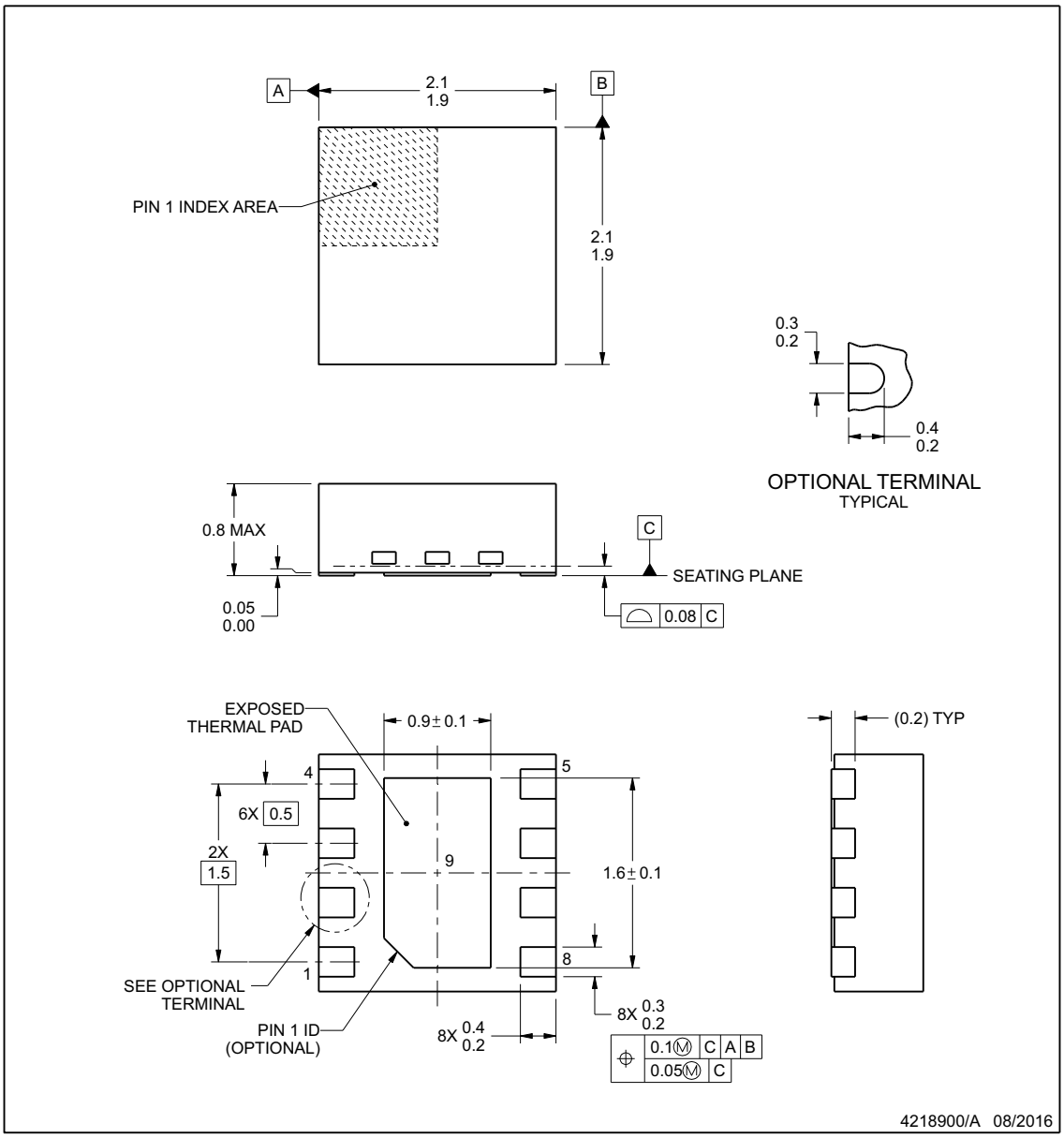
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

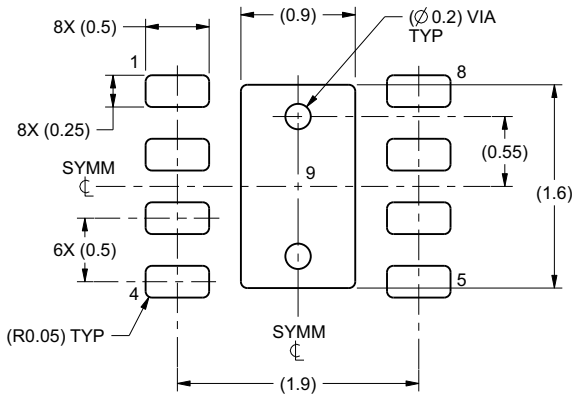
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

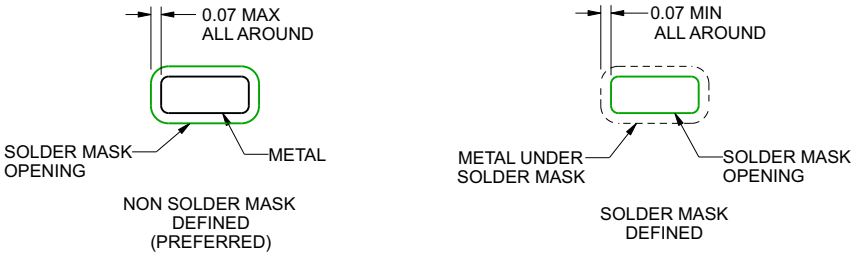
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/A 08/2016

NOTES: (continued)

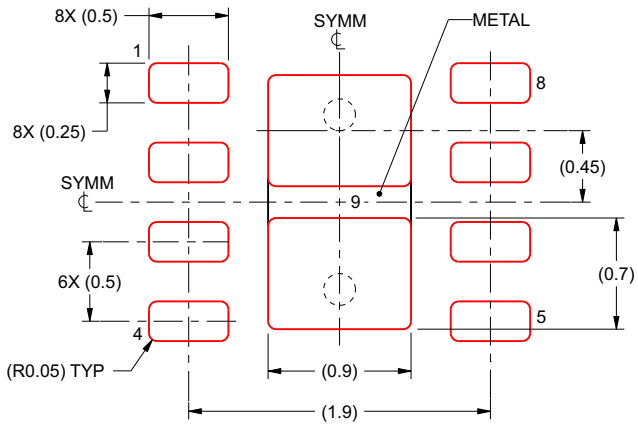
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/A 08/2016

NOTES: (continued)

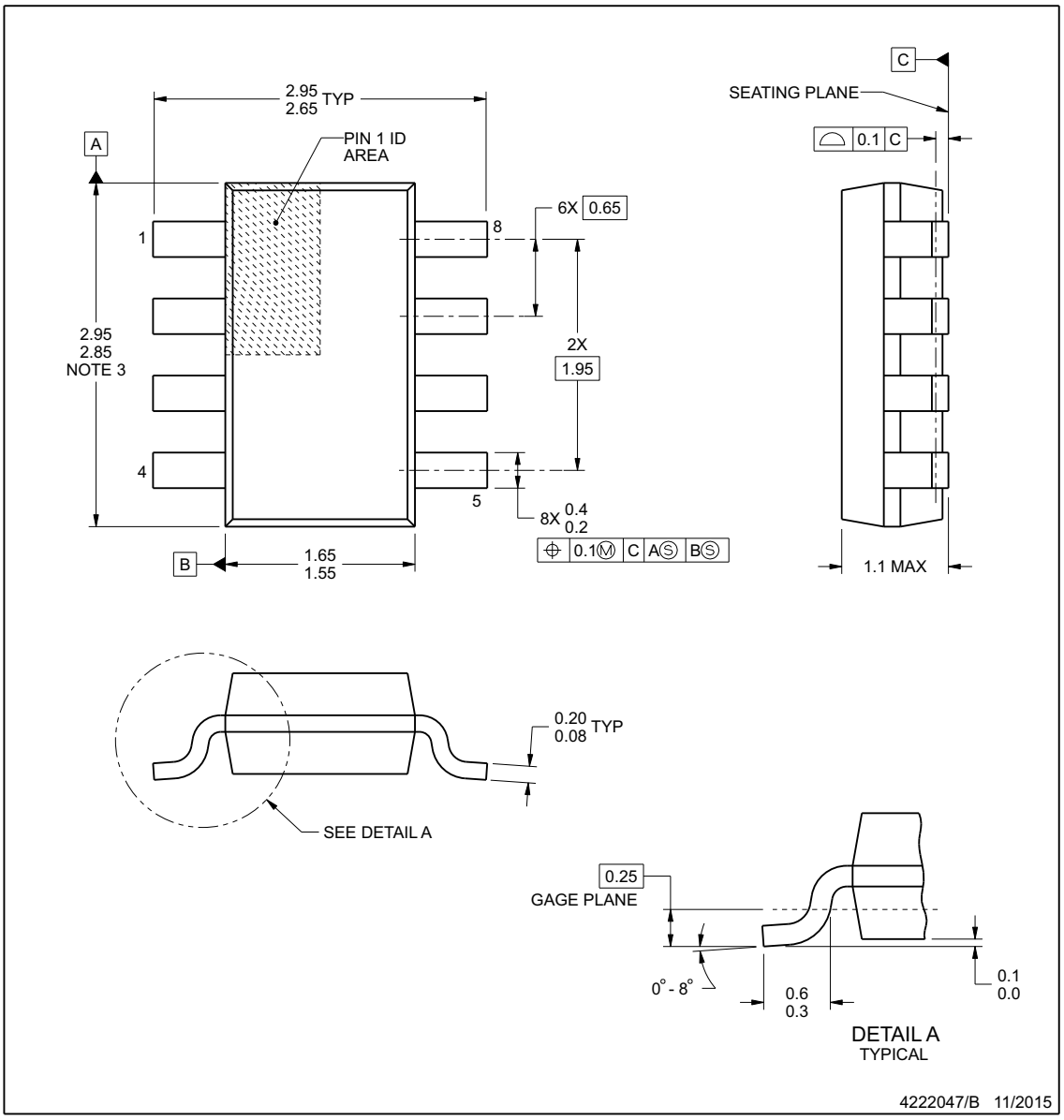
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

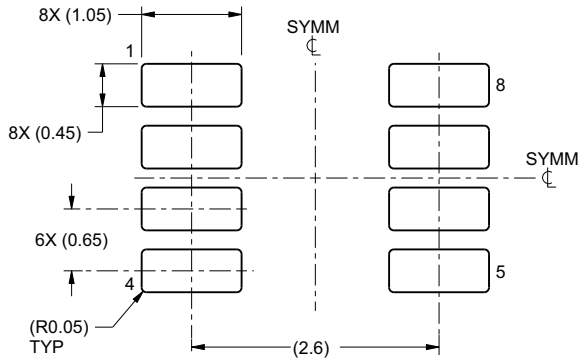
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

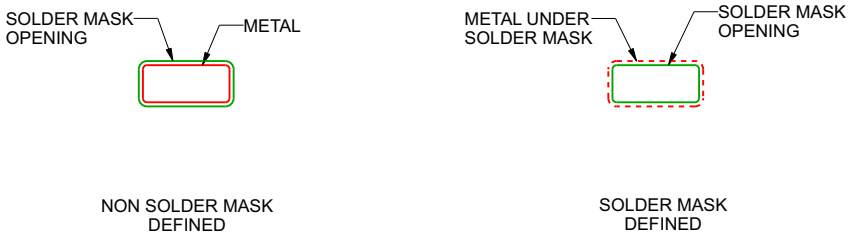
DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4222047/B 11/2015

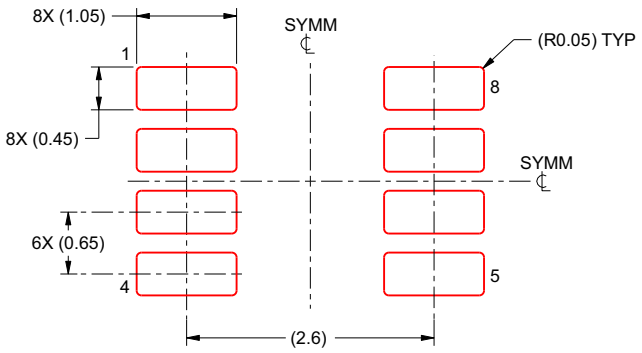
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A — **SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

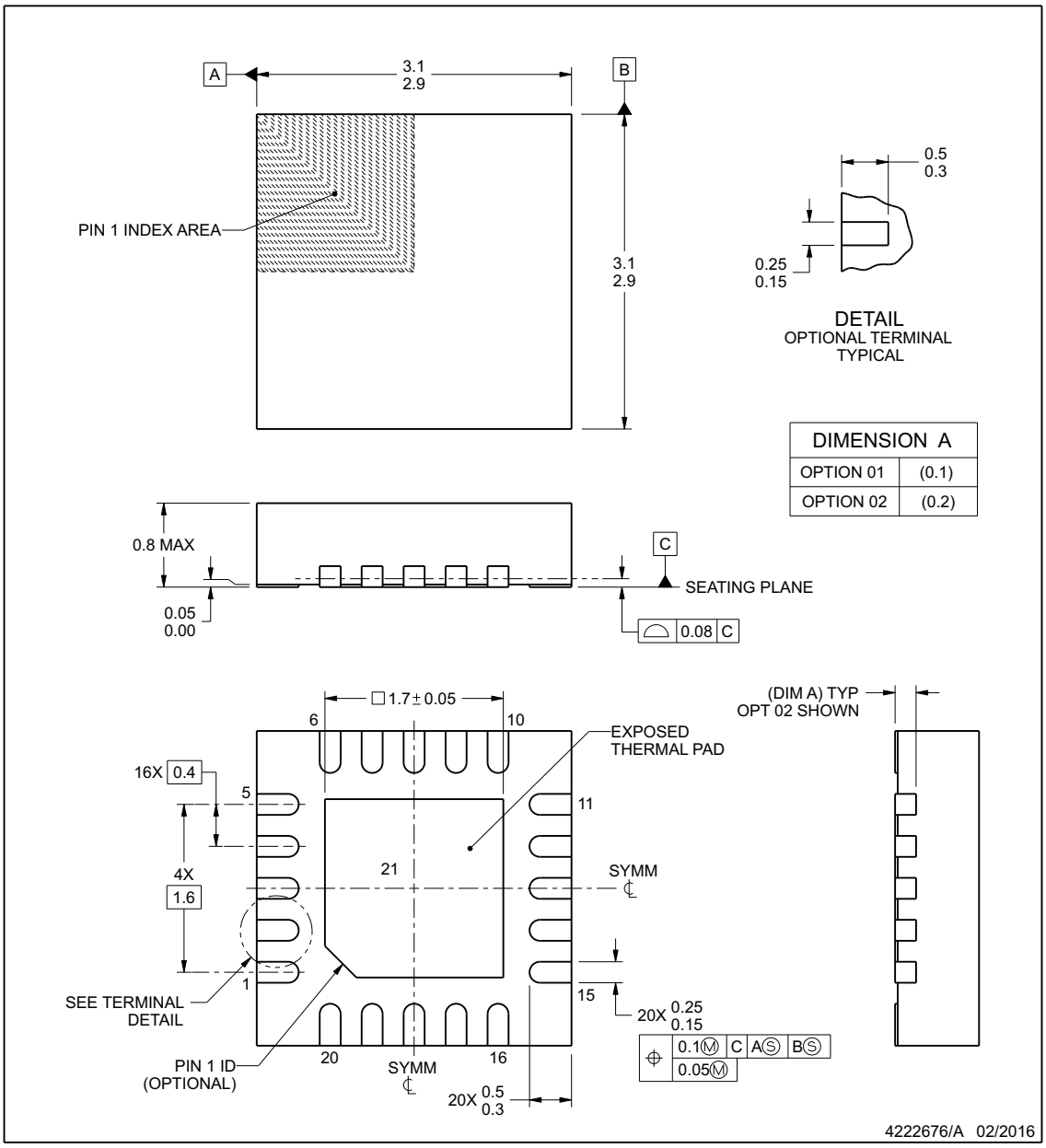
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

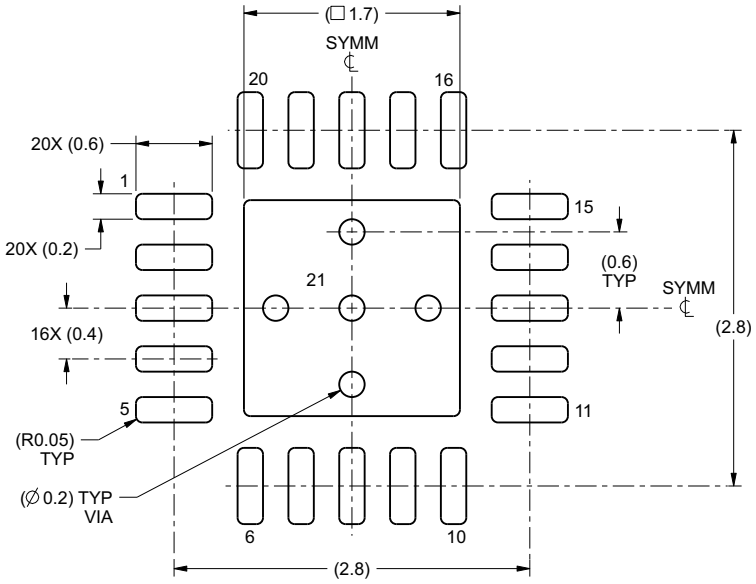
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

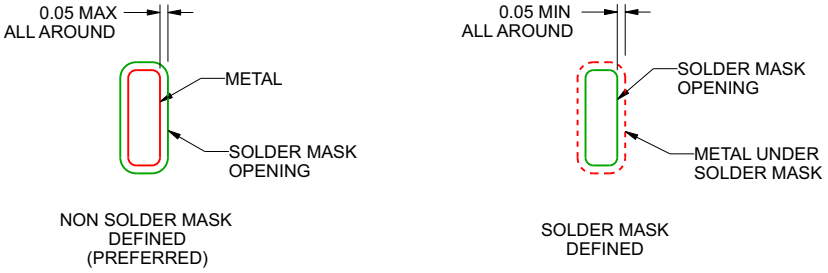
RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222676/A 02/2016

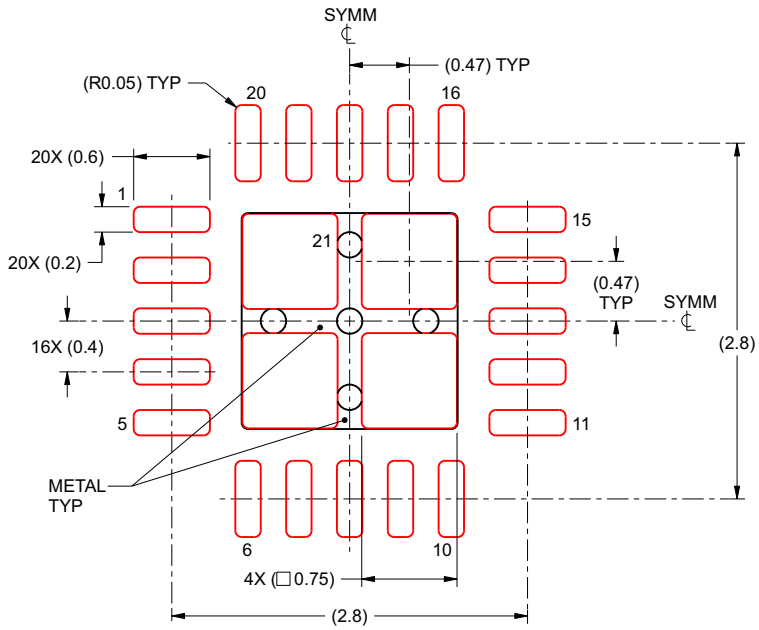
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUK0020B — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

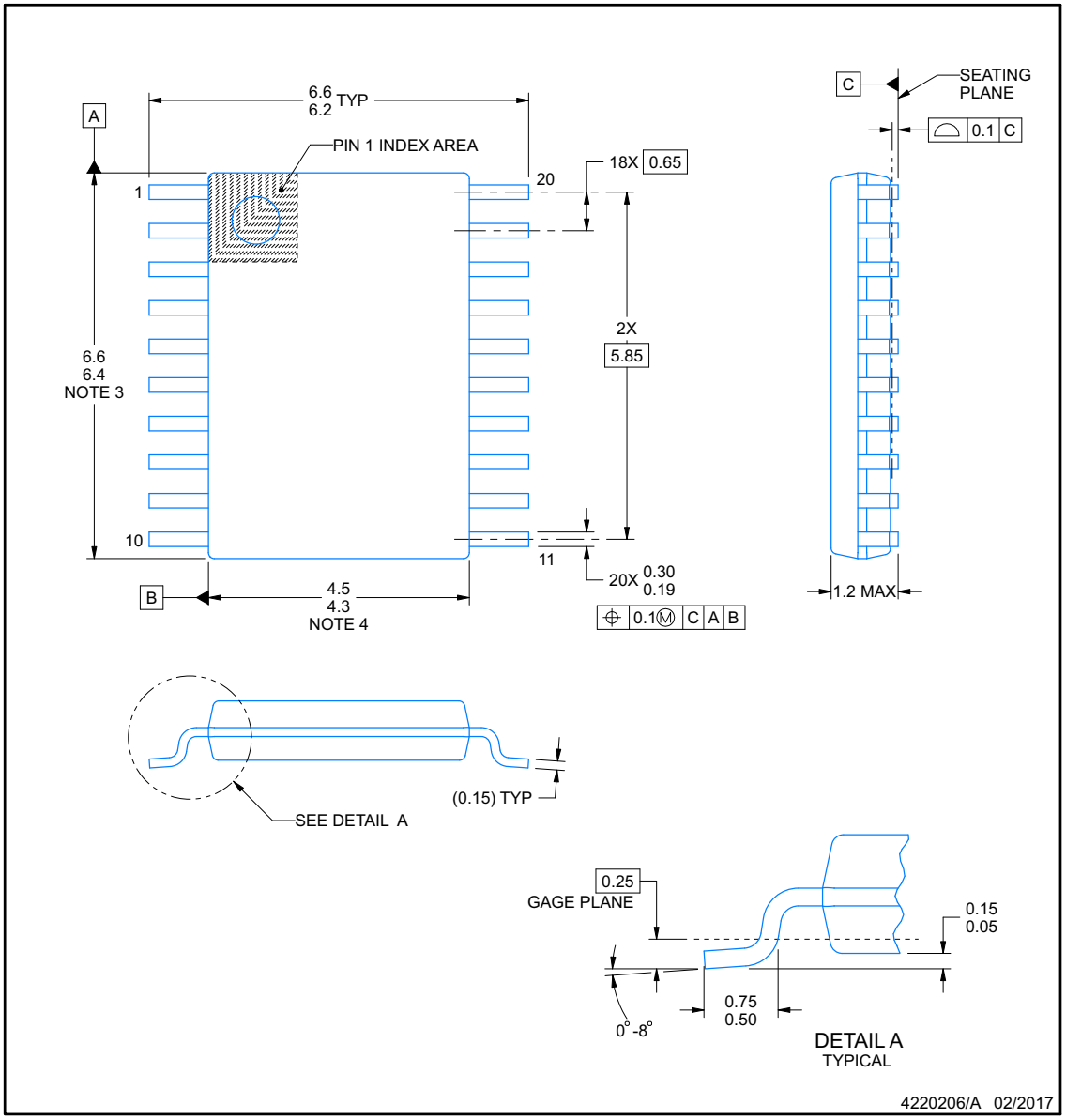
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

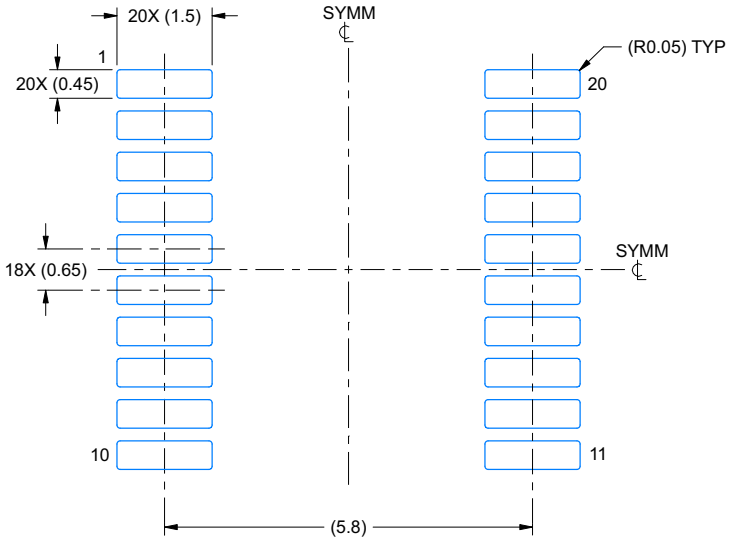
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

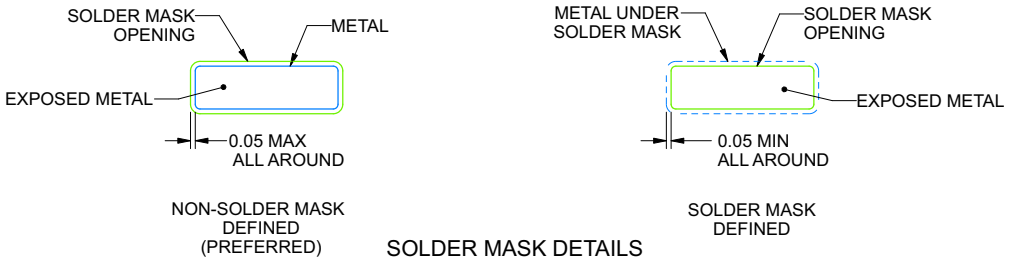
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

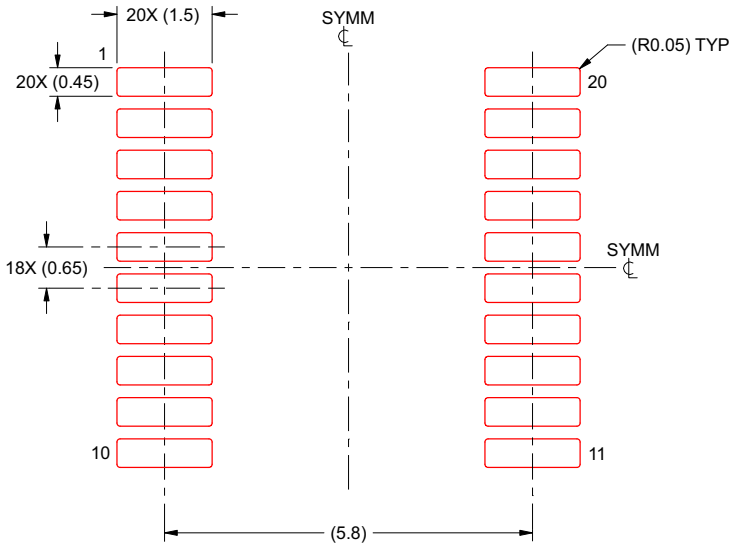
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



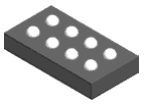
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

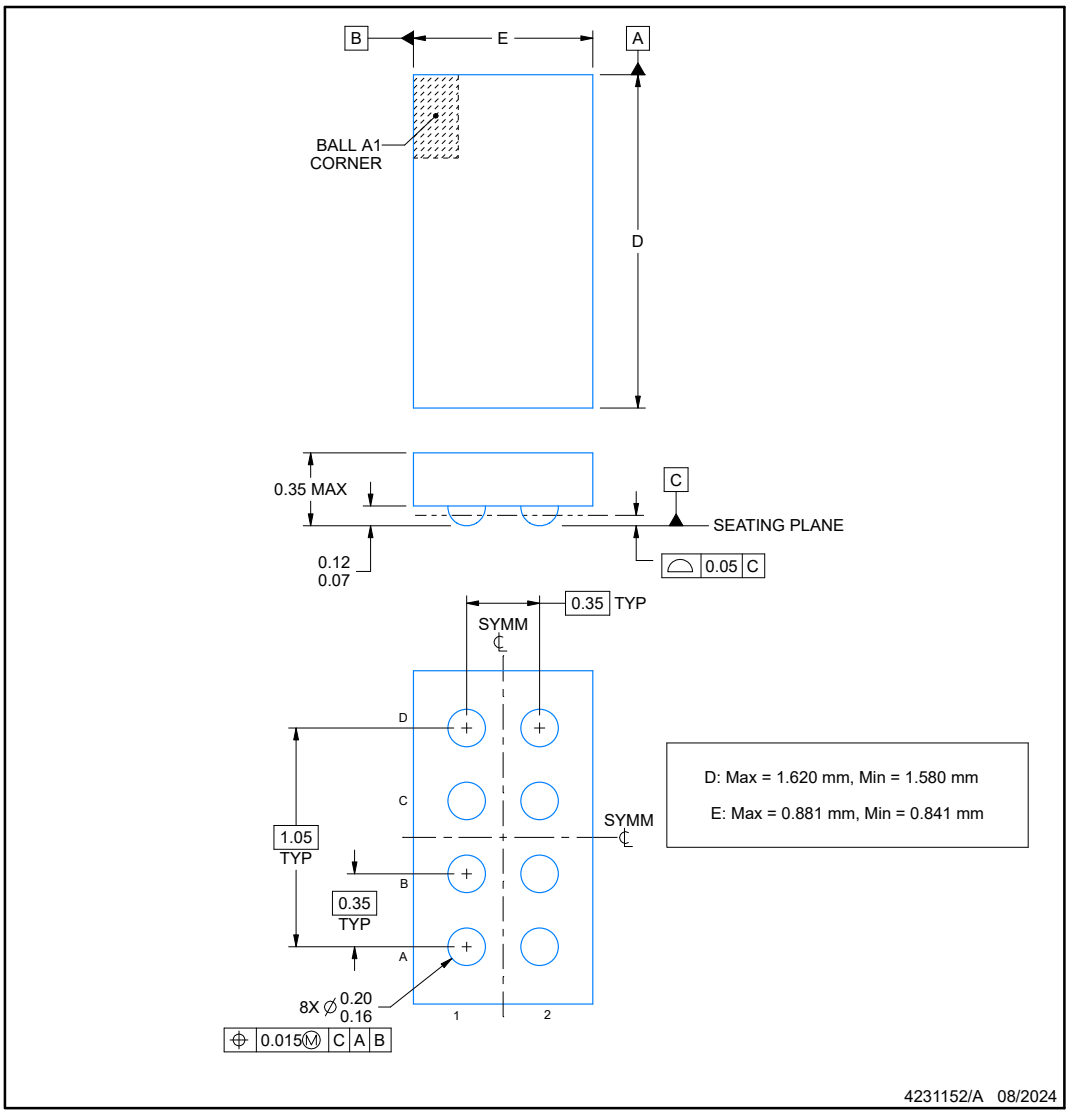
PACKAGE OUTLINE



YCJ0008-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

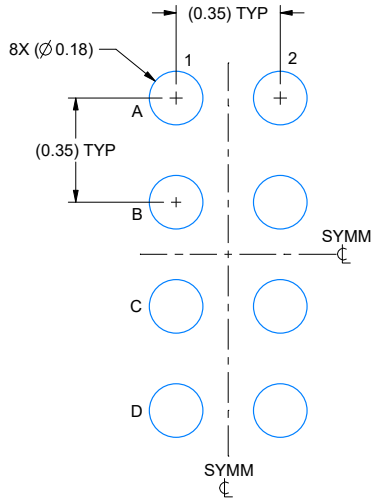
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

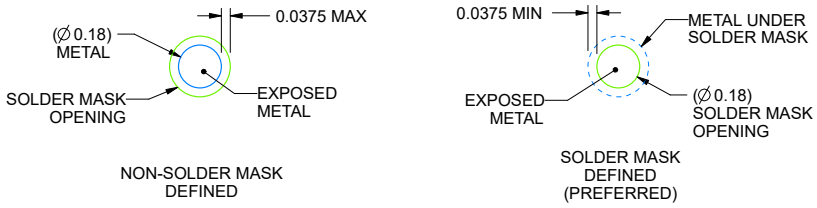
YCJ0008-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4231152/A 08/2024

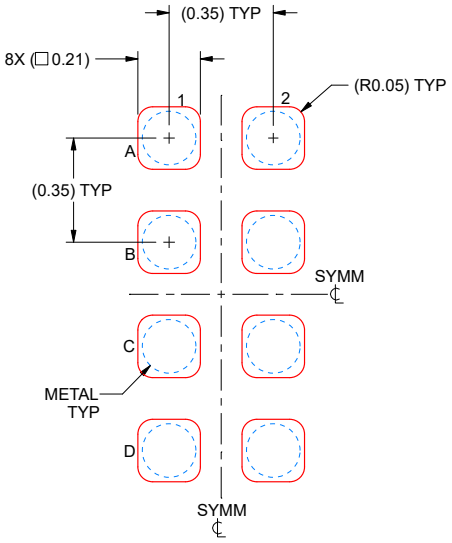
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCJ0008-C01 **DSBGA - 0.35 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4231152/A 08/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSPM0C1103SDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C03S
MSPM0C1103SDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C03S
MSPM0C1103SDDFR.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C03S
MSPM0C1103SDGS20R	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1103S
MSPM0C1103SDGS20R.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1103S
MSPM0C1103SDGS20R.B	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1103S
MSPM0C1103SDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C03S
MSPM0C1103SDSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C03S
MSPM0C1103SDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C03S
MSPM0C1103SDYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M0C1103S
MSPM0C1103SDYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M0C1103S
MSPM0C1103SDYYR.B	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M0C1103S
MSPM0C1103SRUKR	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1103S
MSPM0C1103SRUKR.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1103S
MSPM0C1103SRUKR.B	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1103S
MSPM0C1104SDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04S
MSPM0C1104SDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04S
MSPM0C1104SDDFR.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04S
MSPM0C1104SDGS20R	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104S
MSPM0C1104SDGS20R.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104S
MSPM0C1104SDGS20R.B	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104S
MSPM0C1104SDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04S
MSPM0C1104SDSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04S
MSPM0C1104SDSGR.B	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C04S
MSPM0C1104SDYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104S

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
MSPM0C1104SDYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104S
MSPM0C1104SDYYR.B	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	M0C1104S
MSPM0C1104SRUKR	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1104S
MSPM0C1104SRUKR.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1104S
MSPM0C1104SRUKR.B	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1104S
MSPS003F3SPW20R	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MS003F3
MSPS003F3SPW20R.A	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MS003F3
MSPS003F3SPW20R.B	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MS003F3
MSPS003F4SPW20R	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MS003F4
MSPS003F4SPW20R.A	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MS003F4
MSPS003F4SPW20R.B	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MS003F4
XMSM0C1104S8YCJR	Active	Preproduction	DSBGA (YCJ) | 8	12000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1104S8YCJR.B	Active	Preproduction	DSBGA (YCJ) | 8	12000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1104SDDFR.B	Active	Preproduction	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1104SDGS20R.B	Active	Preproduction	VSSOP (DGS) | 20	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1104SDSGR.B	Active	Preproduction	WSON (DSG) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1104SDYYR.B	Active	Preproduction	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1104SPW20R.B	Active	Preproduction	TSSOP (PW) | 20	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
XMSM0C1104SRUKR.B	Active	Preproduction	WQFN (RUK) | 20	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSPM0C1103, MSPM0C1104 :

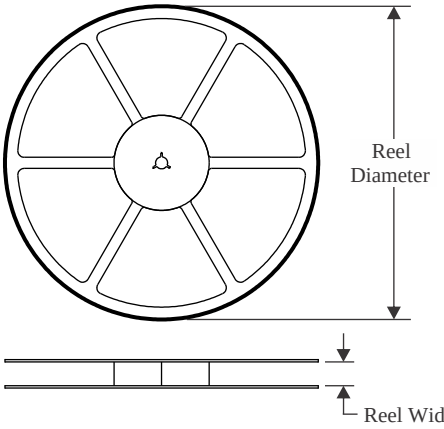
- Automotive : MSPM0C1103-Q1, MSPM0C1104-Q1

NOTE: Qualified Version Definitions:

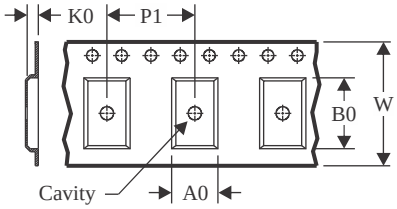
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

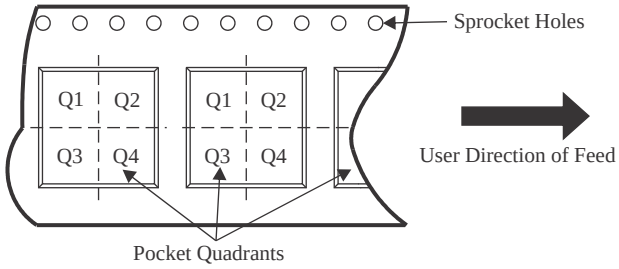


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

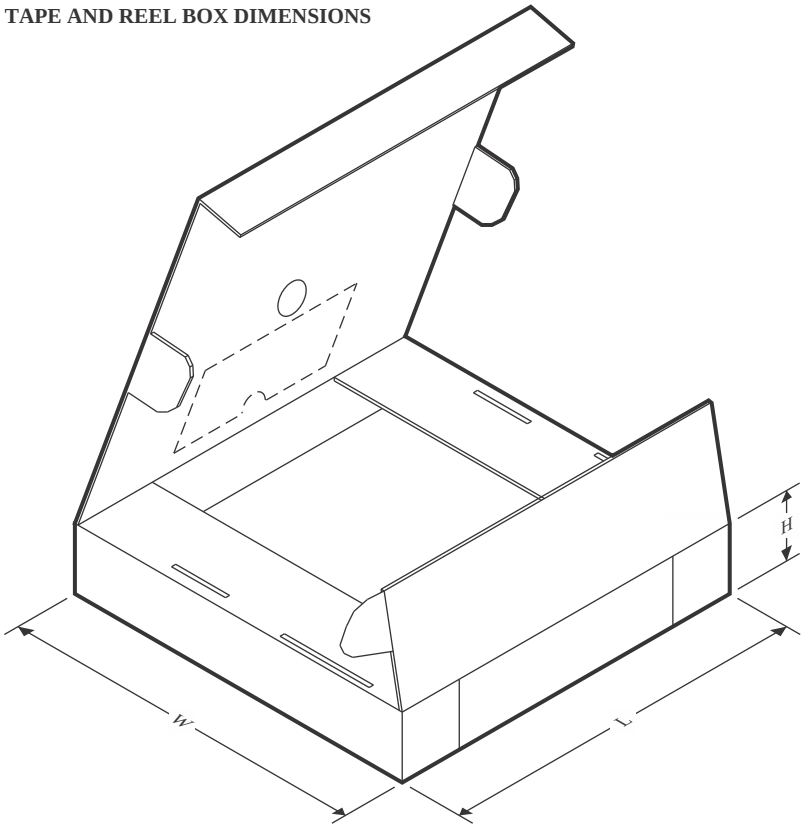
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSPM0C1103SDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MSPM0C1103SDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0C1103SDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
MSPM0C1103SDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0C1103SRUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSPM0C1104SDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
MSPM0C1104SDGS20R	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
MSPM0C1104SDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
MSPM0C1104SDYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
MSPM0C1104SRUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSPM0C1103SDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
MSPM0C1103SDGS20R	VSSOP	DGS	20	5000	353.0	353.0	32.0
MSPM0C1103SDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
MSPM0C1103SDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0C1103SRUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
MSPM0C1104SDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
MSPM0C1104SDGS20R	VSSOP	DGS	20	5000	353.0	353.0	32.0
MSPM0C1104SDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
MSPM0C1104SDYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
MSPM0C1104SRUKR	WQFN	RUK	20	3000	367.0	367.0	35.0

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