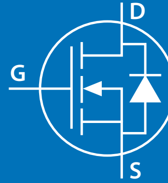
EPC2367 – Enhancement Mode Power Transistor

V_{DS}, 100 V
$R_{DS(on)}$, 1.2 mΩ typ
I_D, 78 A
Pulsed I_D, 309 A

PRELIMINARY



Revised February 3, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate
- Gate Drive ON = 5-5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

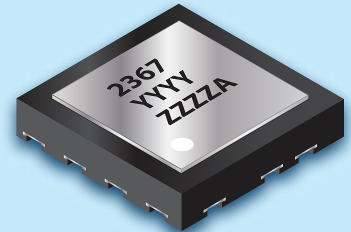
Maximum Ratings			
	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
I_D	Continuous (T_J = 125°C)(1)	78	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	309	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

(1) Electromigration current limit; See Reliability Report Phase 16, Section 3.3.4

Thermal Characteristics			
	PARAMETER	TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.5	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	2.4	

Static Characteristics (T_J = 25°C unless otherwise stated)						
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = TBD	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.01		mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.06		
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.15		
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.01		
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 10 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 30 A		1.2		mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.6		V

Defined by design. Not subject to production test.



Package size: 3.3 x 3.3 mm

Applications

- High frequency DC-DC conversion up to 80 V input
- High power density DC-DC modules up to 80 V input
- 24 V–60 V motor drives
- Synchronous rectification

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint
- Excellent thermal
- Lowest $R_{DS(on)}$ in 3.3 x 3.3 mm package, 100 V

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2367

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		2170		pF
C_{RSS}	Reverse Transfer Capacitance			8		
C_{OSS}	Output Capacitance			590		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		857		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1080		
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 30 A		17		nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 30 A		5.3		
Q_{GD}	Gate-to-Drain Charge			2.4		
$Q_{G(TH)}$	Gate Charge at Threshold			3.8		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		54		
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V.

Figure 1: Typical Output Characteristics at 25°C

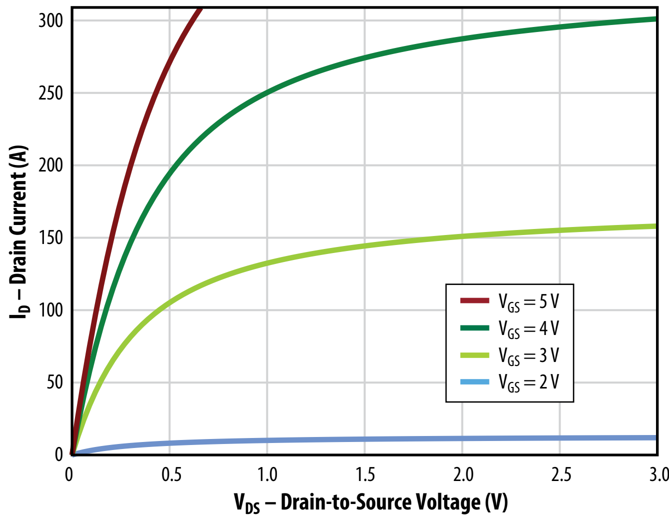


Figure 2: Typical Transfer Characteristics

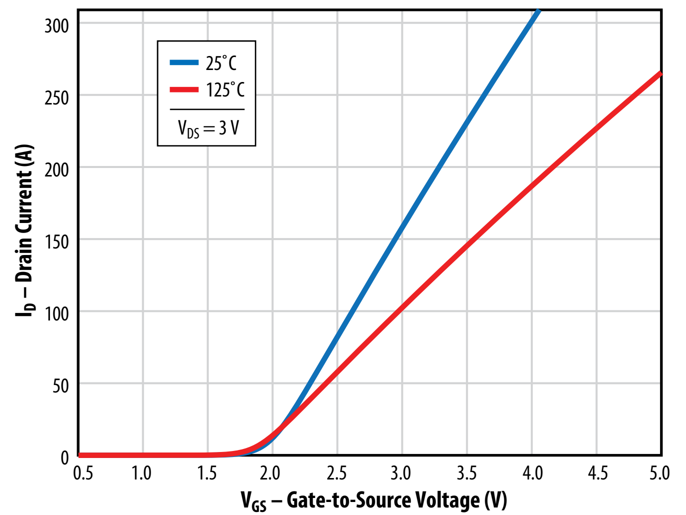


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

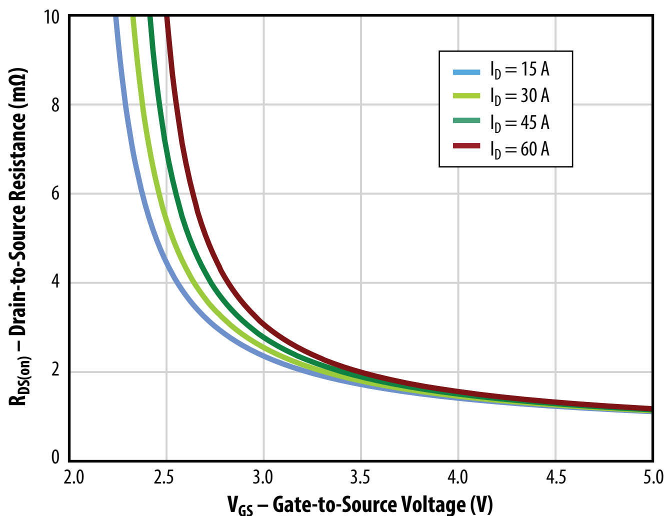
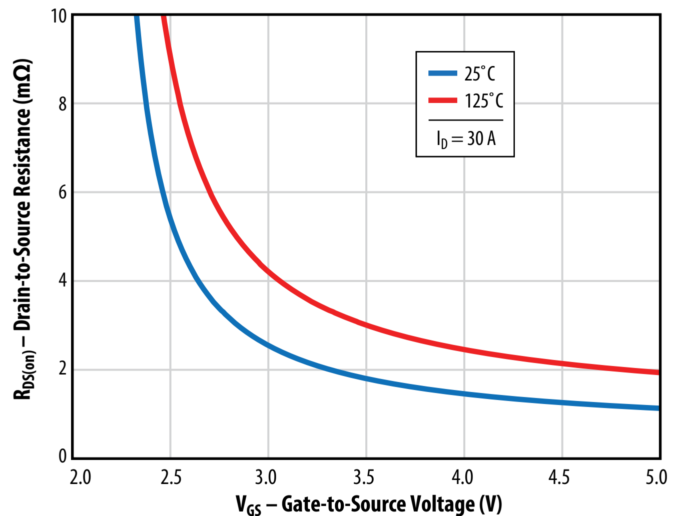
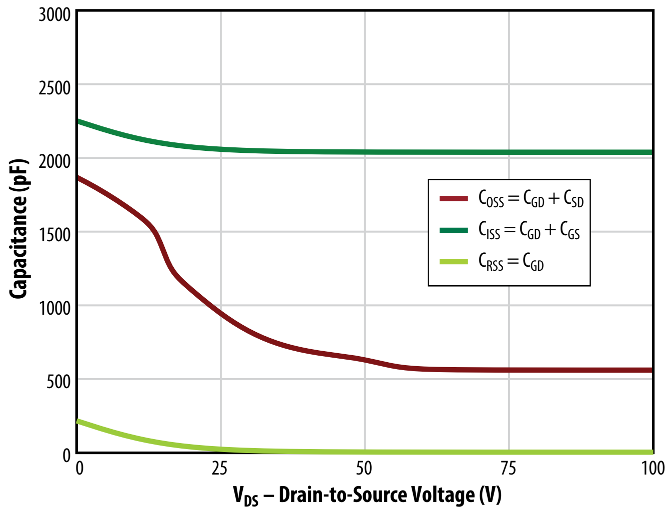
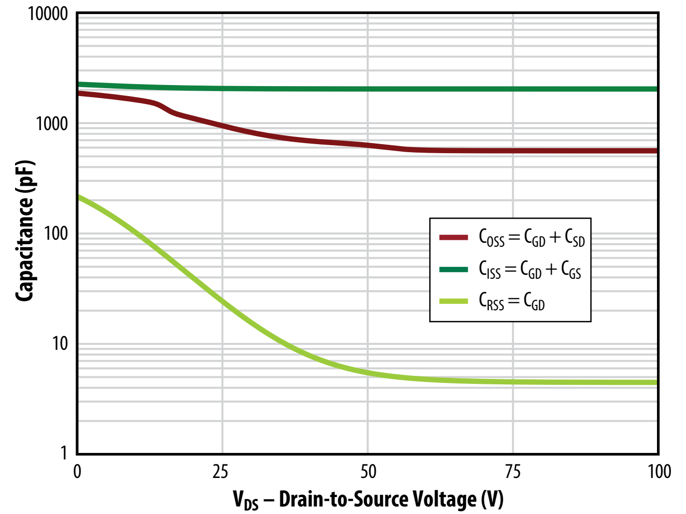
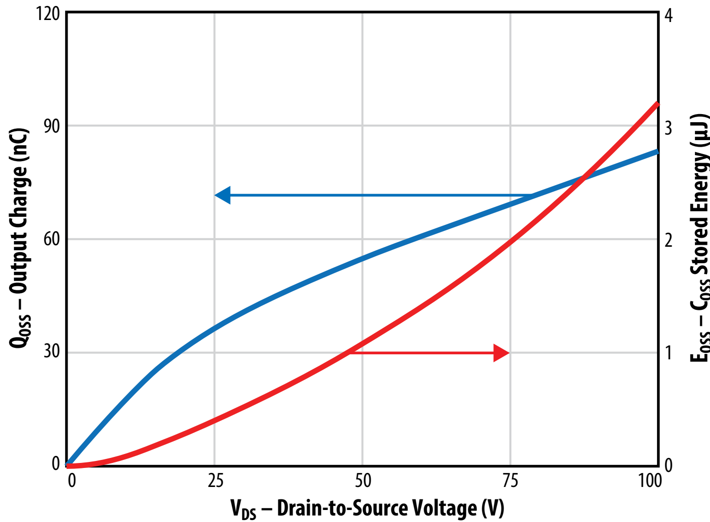


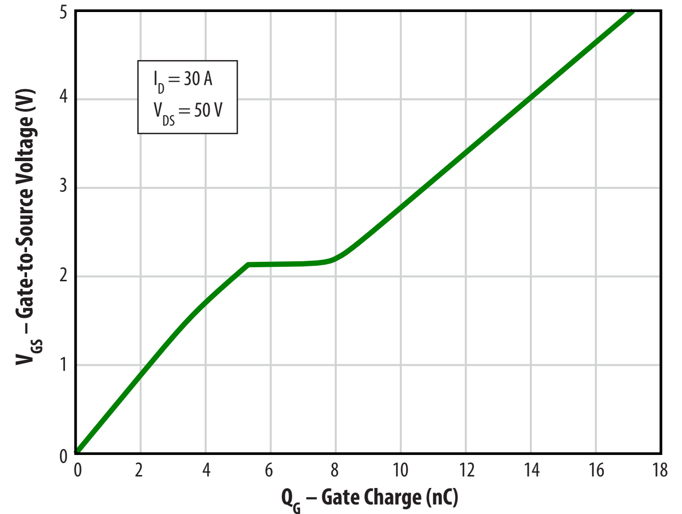
Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

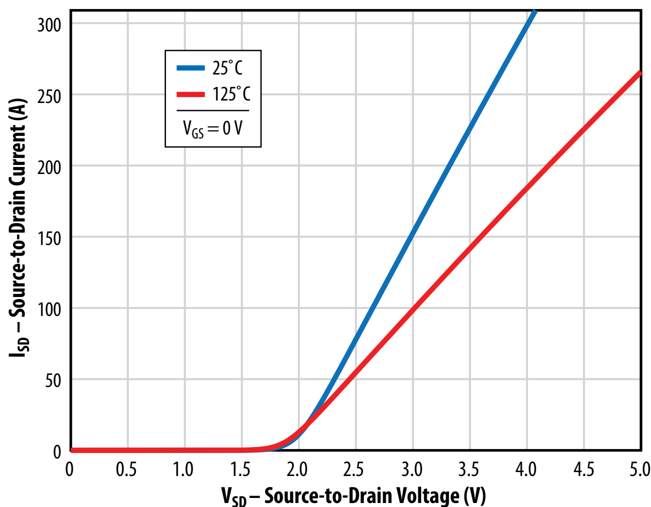












Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

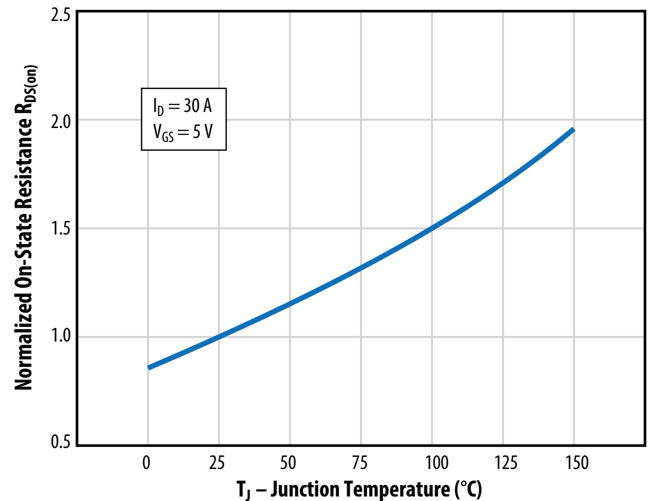


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

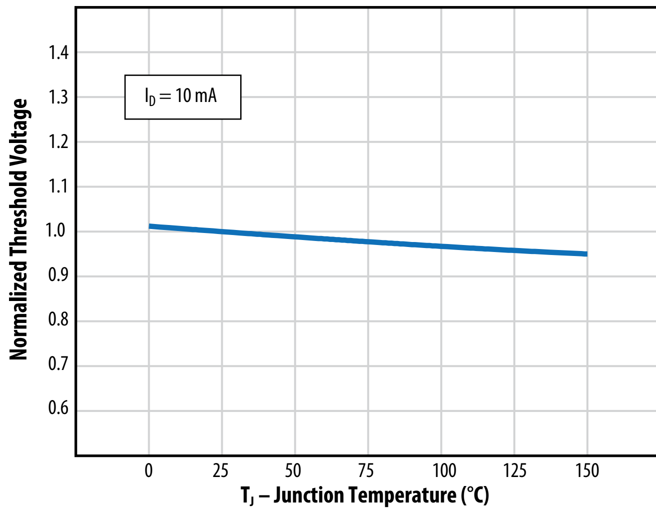
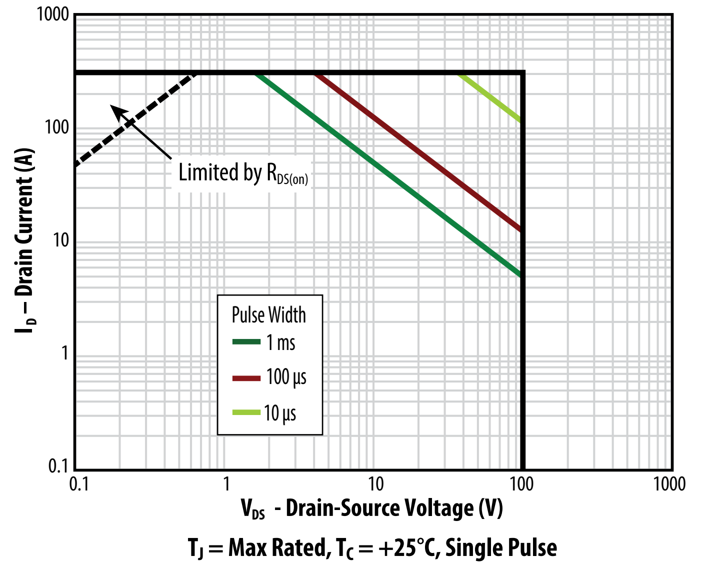
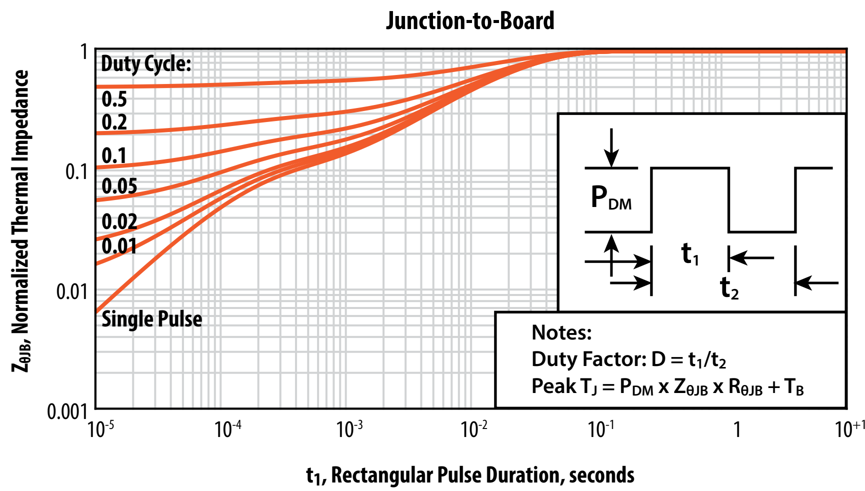


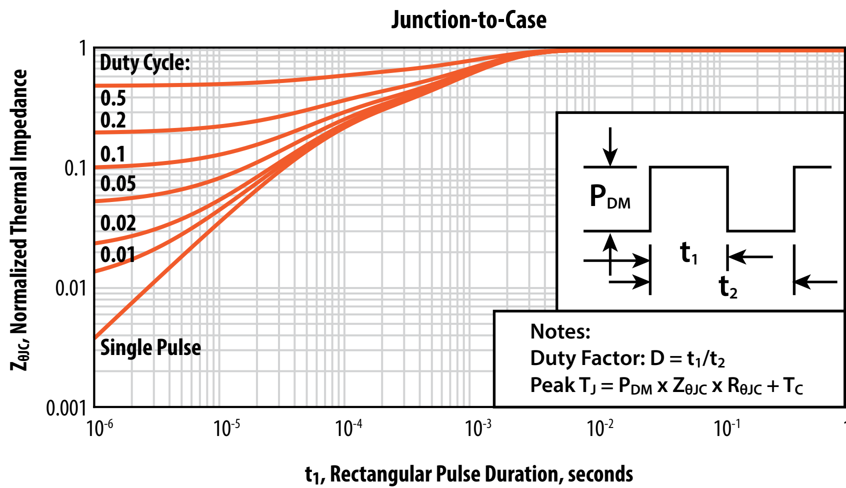
Figure 11: Safe Operating Area



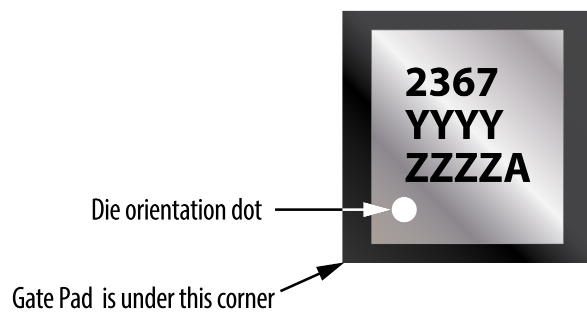
T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Transient Thermal Response Curves

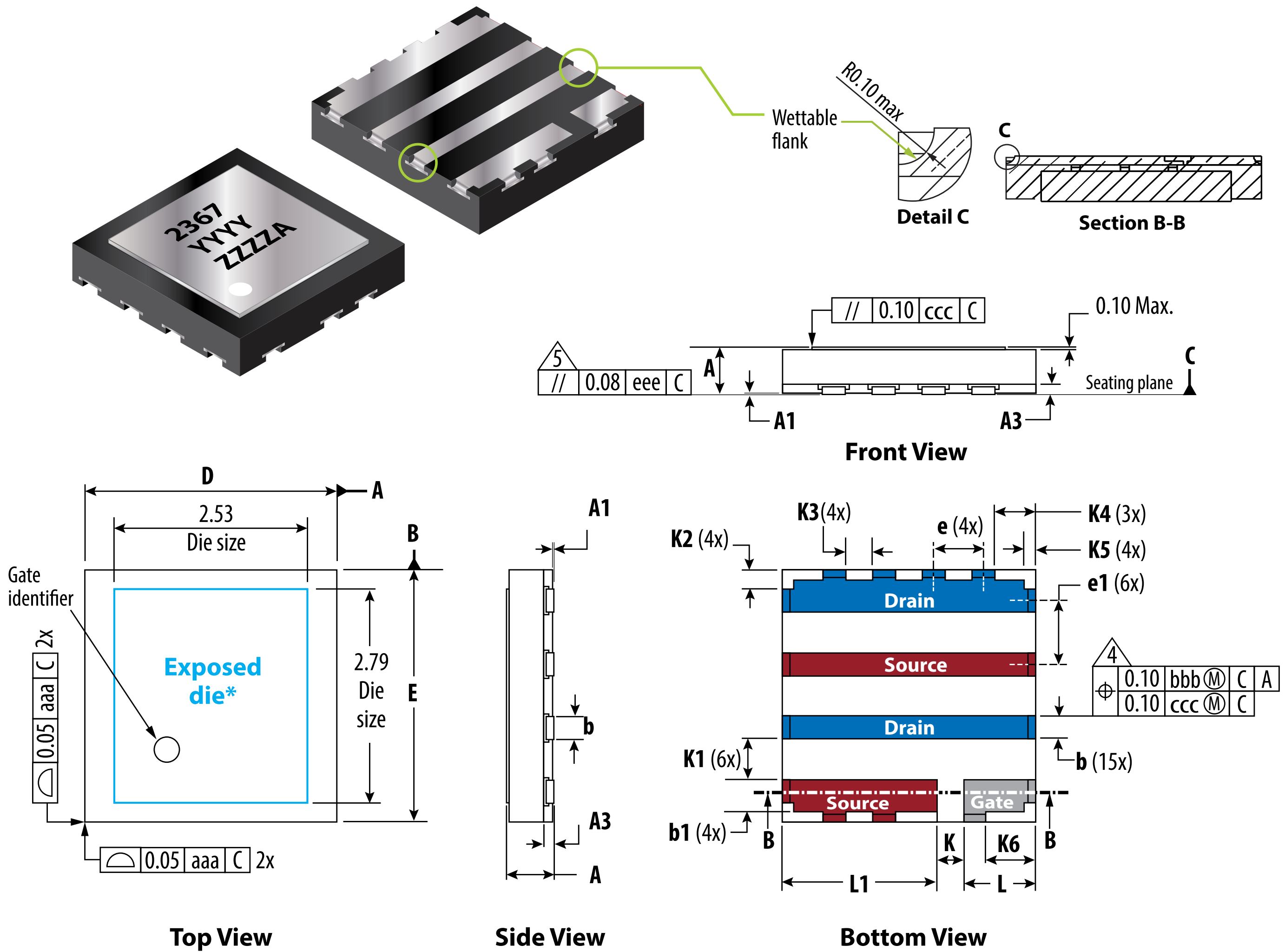




Part Marking



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2367	2367	YYYY	ZZZZA



*The exposed die is the silicon substrate that is internally connected to the source.
It is not recommended to use it as an electrical connection

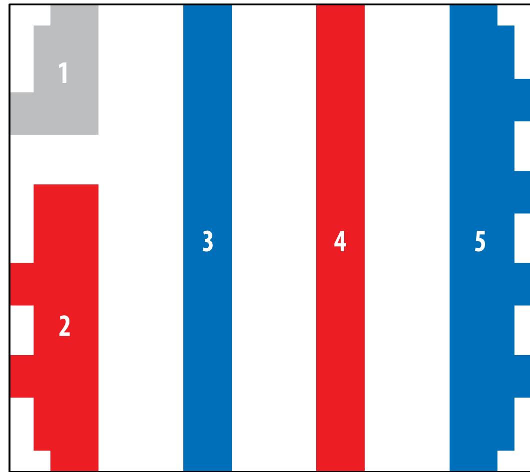
SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A			0.70	
A1	0.00	0.02	0.05	
A3			0.25	
b	0.22	0.30	0.35	4
b1	0.42 Ref			
D	3.20	3.30	3.40	
E	3.20	3.30	3.40	
e	0.65 BSC			
e1	0.83 BSC			
L	0.84	0.94	1.04	
L1	1.91	2.01	2.11	
K	0.350 Ref			
K1	0.530 Ref			

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
K2	0.255 Ref			
K3	0.350 Ref			
K4	0.525 Ref			
K5	0.150 Ref			
K6	0.621 Ref			
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	5			3
Notes	1.2			

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.

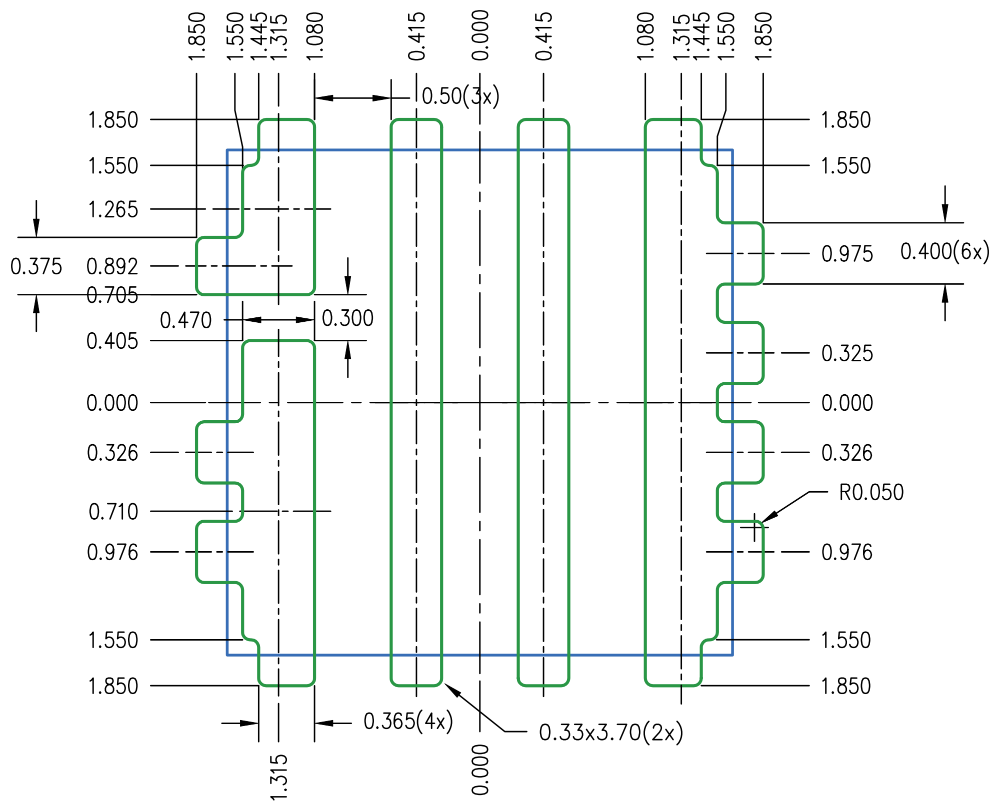
TRANSPARENT VIEW



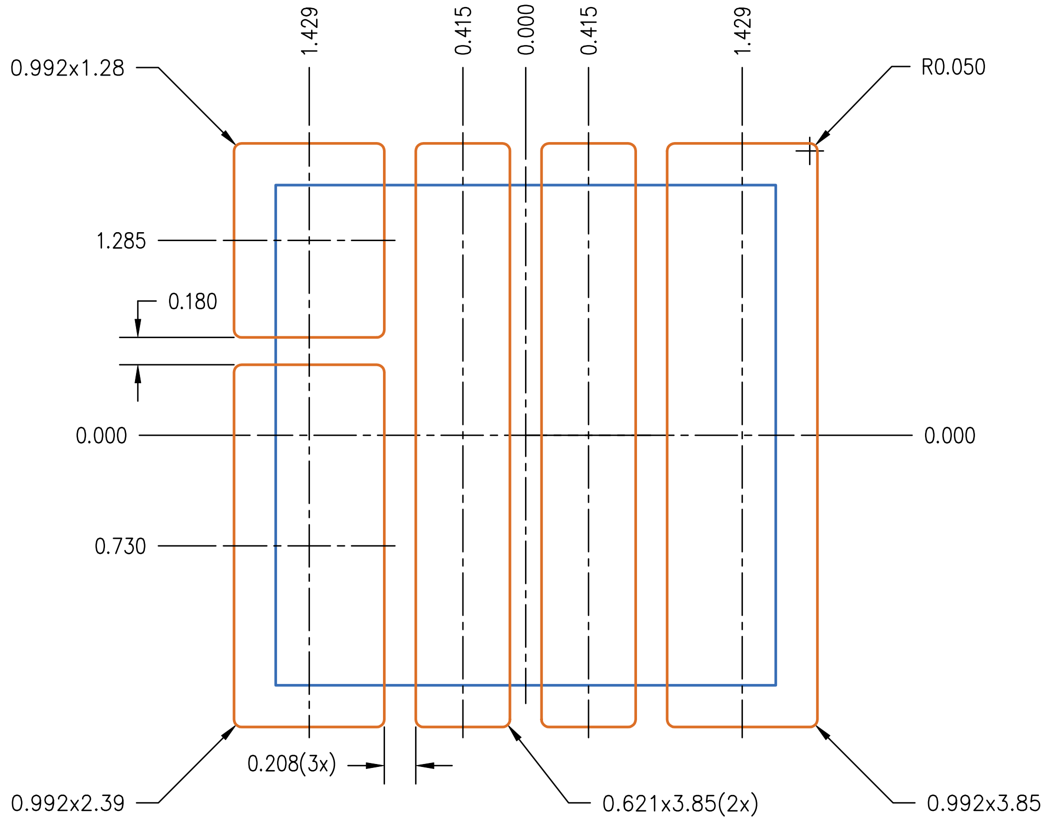
PIN	Description
1	Gate
2	Source
3	Drain
4	Source
5	Drain

RECOMMENDED LAND PATTERN
(units in mm)

Land pattern is solder mask defined



RECOMMENDED COPPER DRAWING *(units in mm)*



LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the first inner layer used as a reference fo the gate loop under the gate resistors and the relative pins of the gate driver: ground for the bottom FET and switch node for the top FET.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

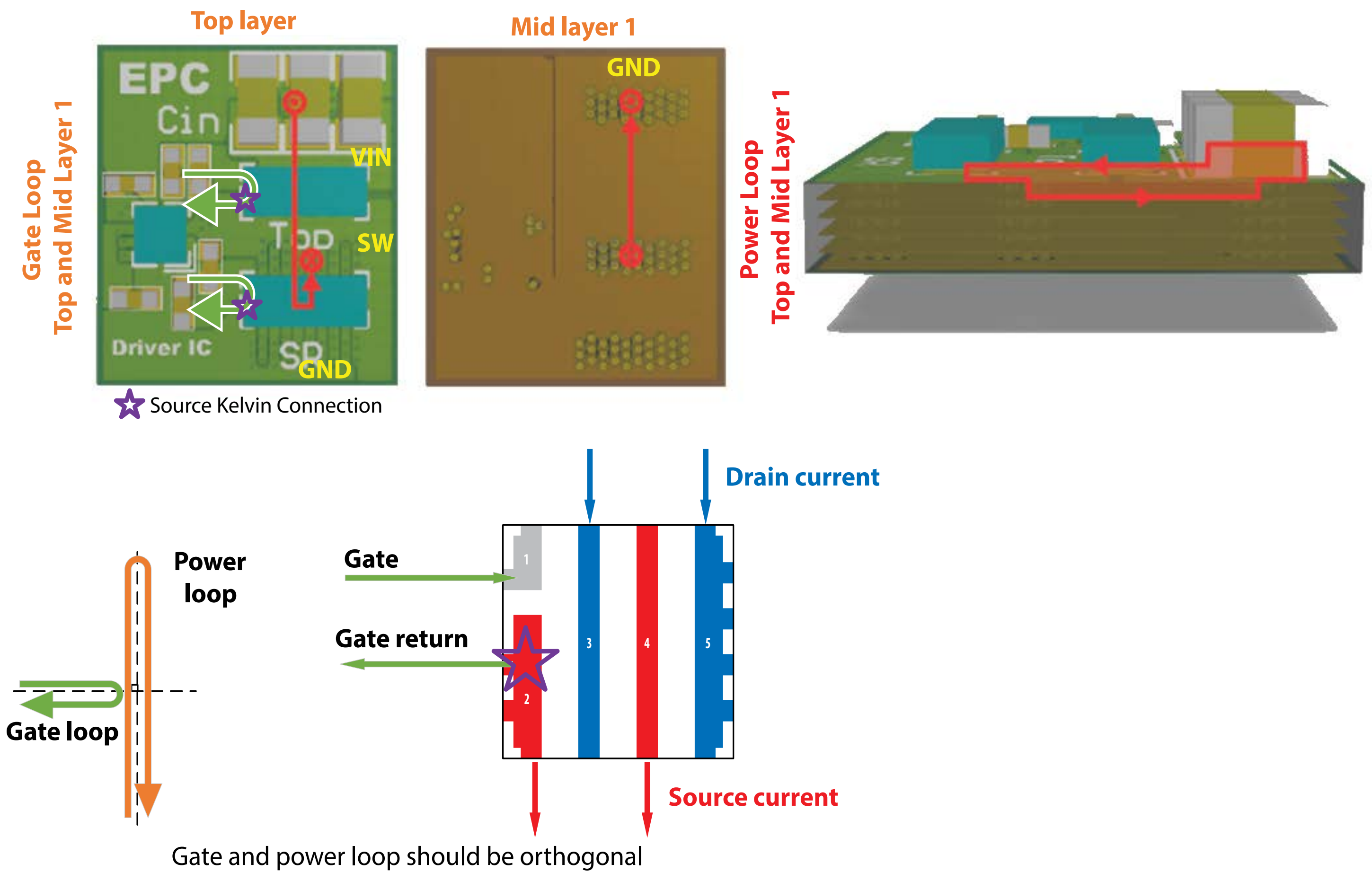


Figure 13: Inner vertical layout for power and gate loops

Detailed recommendations on layout can be found on EPC's website: **Optimizing PCB Layout with eGaN FETs.pdf**

TYPICAL THERMAL CONCEPT

The EPC2367 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

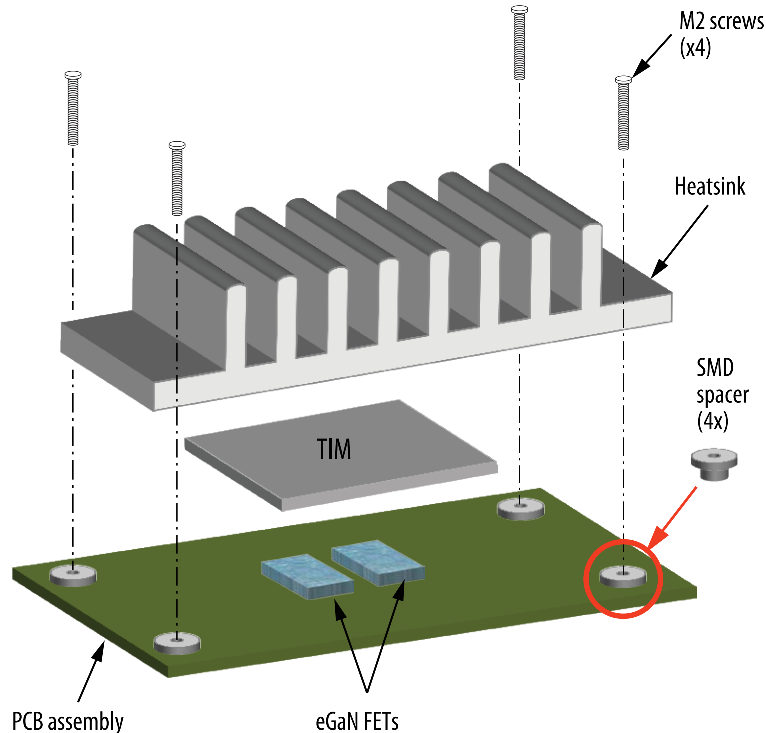


Figure 14: Exploded view of heatsink assembly using screws

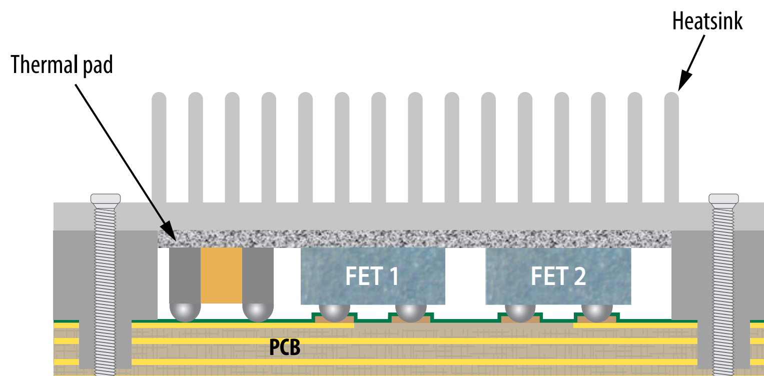


Figure 15: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

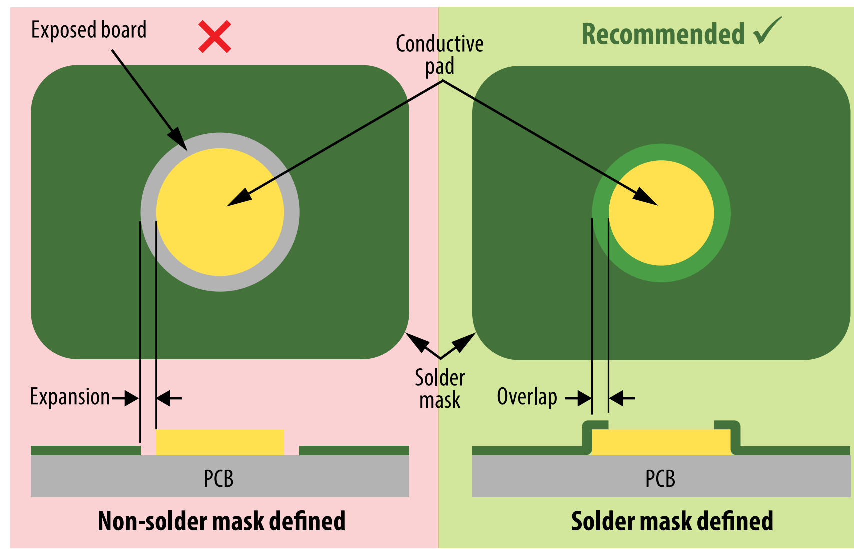


Figure 16: Solder mask defined versus non-solder mask defined pad

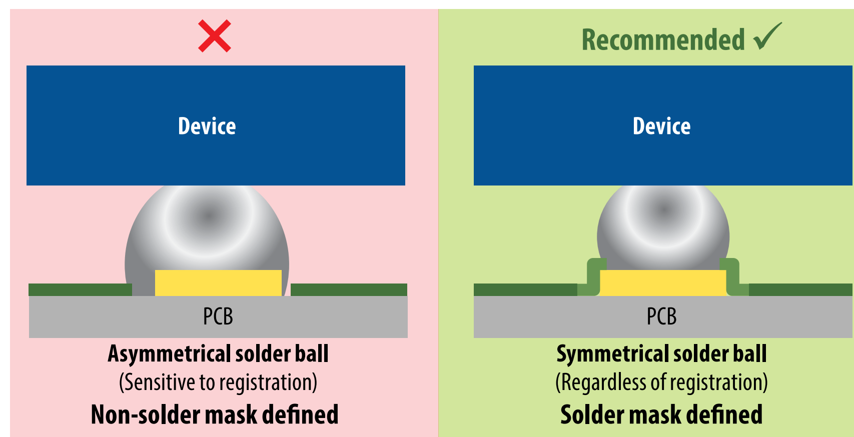


Figure 17: Effect of solder mask design on the solder ball symmetry

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip** (for preliminary device Altium footprints, contact EPC)

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