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Cyclone® V SoC Development Kit User Guide

Online Version
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Contents

1. Overview

Cyclone® V SoC Development Kit is a complete design environment that includes both hardware and software you need to develop the Cyclone V SoC designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of the Cyclone V designs.

Table 1. Ordering Information

Development Kit Version	Ordering Code	Device Part Number	Starting Serial Number
Cyclone V SoC Development Kit (Production 2) (Power Solution 2)	DK-DEV-5CSXC6N-B	5CSXFC6D6F31C6N	5CSXSoC0100014
Cyclone V SoC Development Kit (Production) (Power Solution 1)	DK-DEV-5CSXC6N	5CSXFC6D6F31C6N	5CSXSoC0060001

Figure 1. Cyclone V SoC Development Kit (Power Solution 2)—Top View

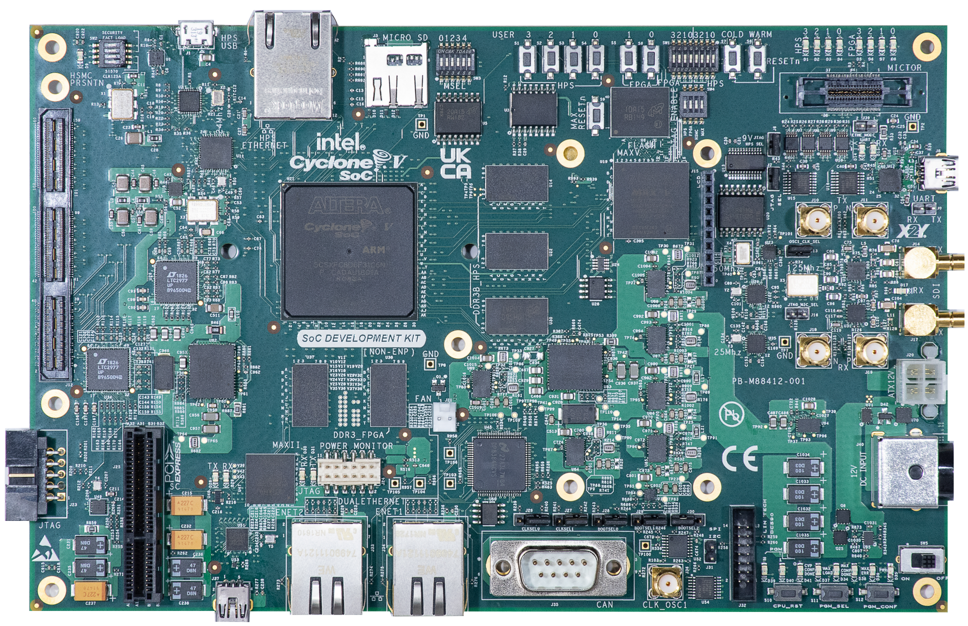
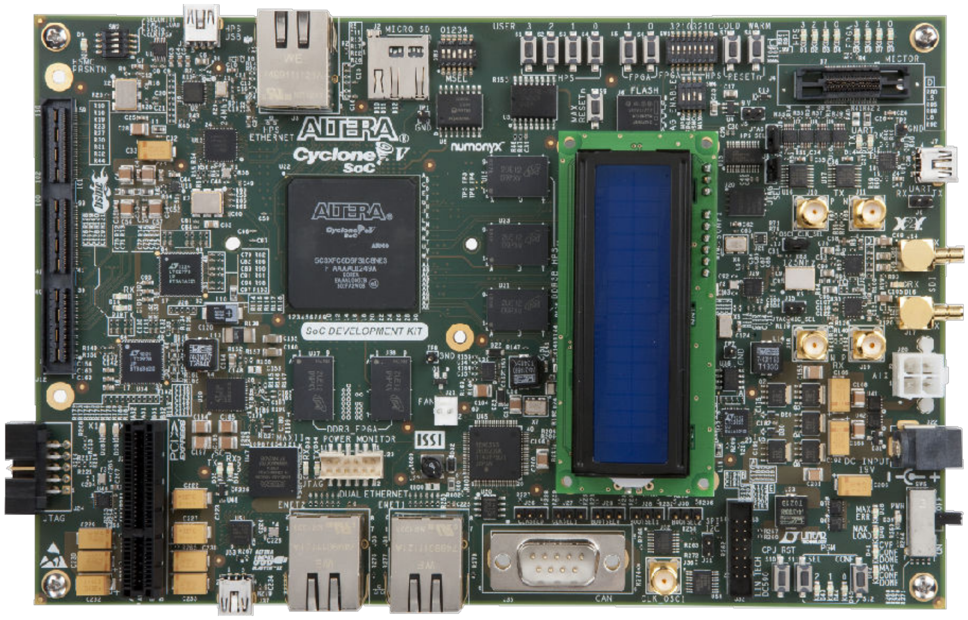


Figure 2. Cyclone V SoC Development Kit (Power Solution 1)—Top View



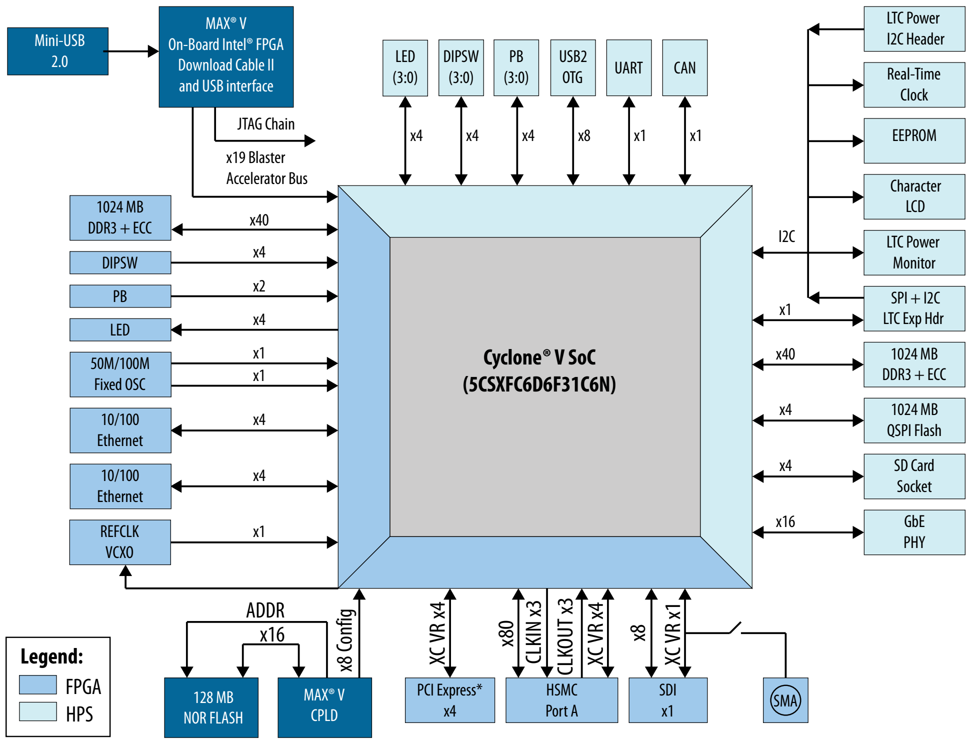
Refer to the *Appendix A—Development Kit Components* section for more details about the components on the Cyclone V SoC Development Kit.

Related Information

Development Kit Components on page 45

1.1. Block Diagram

Figure 3. Cyclone V SoC Development Kit Block Diagram



1.2. Feature Summary

Device

- Cyclone V SX SoC—5CSXFC6D6F31C6N (SoC)
- MAX® V CPLD—5M2210ZF256C4N (system controller)
- MAX II CPLD—EPM570GF100 (embedded Intel® FPGA Download Cable II)

FPGA I/O Interfaces

- 2 10/100 Megabit Ethernet PHYs (EtherCAT)
- PCIe* 1.0 x4 female connector
- Universal high-speed mezzanine card (HSMC)—x4 transceivers, x16 TX LVDS, x16 RX LVDS
- 1 serial digital interface (SDI) channel
- 4 SMAs for one transceiver channel
- 4 push buttons
- 2 switches
- 4 LEDs

HPS I/O Interfaces

- 1 USB 2.0 On-the-Go (OTG)
- 1 10/100/1000 Megabit Ethernet (10MbE/100MbE/1000MbE)
- 1 CAN
- 1 UART (UART to USB bridge)
- 1 real-time clock (with battery backup)
- 1 two-line text LCD
- 1-/2-channel, 20 bit delta-sigma analog-to-digital converter (Linear Technology LTC2422)
- 4 push buttons
- 4 switches
- 4 LEDs

HPS Boot Sources

- 1 GB DDR3 SDRAM (32 bit) with error correction code (ECC)
- 128 MB quad SPI flash memory
- Micro-SD card socket with 4 GB micro-SD card flash device

Memory

- HPS I/O Memory:
  - 1 GB DDR3 SDRAM (32 bit) with error correction code (ECC)
  - 128 MB quad SPI flash memory
  - Micro-SD card socket with 4 GB micro-SD card flash device
- FPGA Memory:
  - 1 GB DDR3 SDRAM (32 bit)

Cables and Adapters

- Power Solution 2 board—12 V AC adapter, PCIe edge connector
- Power Solution 1 board—Laptop DC Input 14 – 20 V adapter, PCIe edge connector

Software

A one-year license for the Quartus® Prime Pro Edition design software is included with the purchase of the kit. Refer to the *Intel FPGA Software Installation and Licensing* for more information.

Related Information

Intel FPGA Software Installation and Licensing

1.3. Box Contents

- Cyclone V development board—A development platform that allows you to develop and prototype hardware designs running on the Cyclone V SoC.
- MicroSD flash memory card
- Debug header breakout board high-speed mezzanine card (HSMC)
- Loopback daughtercard HSMC
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - USB cable
  - Ethernet cable
  - SMB cable

Related Information

Cyclone V SoC Development Kit Website

2. Getting Started

This section provides the initial guidelines to get you started using the development kit.

2.1. Before You Begin

You must check the kit contents and inspect the boards to verify that you received all of the items in the box before using the kit or installing the software.

In case any of the items are missing, you must contact Altera before you proceed.

Important: Read the Appendix B.1—Safety and Regulatory Information for safe operation and regulatory adherence.

2.2. Inspecting the Boards

To inspect each board, perform these steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Without proper anti-static handling, you may damage the board.
2. Verify that all components on the boards appear in place and intact.

In typical applications with the Cyclone V development board, a heat sink is not necessary. However, under extreme conditions or for engineering sample silicon, the board might require additional cooling to stay within operating temperature guidelines. The board has two holes near the FPGA that accommodate many different heat sinks, including the Dynatron V31G*. You can perform power consumption and thermal modeling to determine whether your application requires additional cooling. For information about measuring board and FPGA power in real time, refer to the *The Power Monitor* section.

Related Information

The Power Monitor on page 39

2.3. Software and Driver Installation

This section explains how to install the following software and driver:

- Quartus Prime Standard Edition software
- Intel SoC FPGA Embedded Development Software (EDS)
- Cyclone V SoC Development Kit software
- Intel FPGA Download Cable II driver

2.3.1. Installing the Quartus Prime Standard Edition Software

1. Download the Quartus Prime Standard Edition software from the *FPGA Software Download Center* webpage of the Intel website.
2. Follow the on-screen instructions to complete the installation process. Choose an installation directory that is relative to the Quartus Prime Standard Edition software installation directory.

If you have difficulty installing the Quartus Prime software, refer to the *Intel FPGA Software Installation and Licensing*.

Related Information

- Quartus Prime Standard Edition User Guide: Getting Started
- Intel FPGA Software Installation and Licensing
- Intel FPGA Download Center

2.3.2. Installing the Intel SoC EDS

The Intel SoC FPGA Embedded Development Software (EDS) is a comprehensive software tool suite for embedded software development on Altera® SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm* Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Altera's SoC FPGAs.

For more information and steps to install the Intel SoC EDS Tool Suite, refer to the links below.

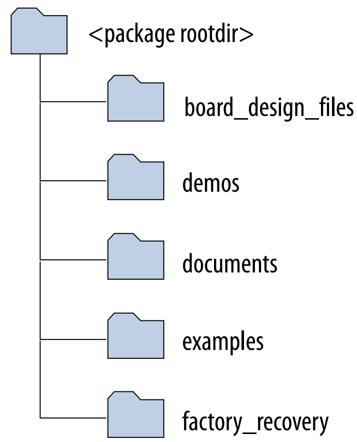
Related Information

- Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide
- Arm* Development Studio for Intel SoC FPGA

2.3.3. Installing the Development Kit

1. Download the Cyclone V SoC Development Kit installer package from the Cyclone V SoC Development Kit webpage of the Intel website.
2. Unzip the Cyclone V SoC Development Kit installer package. The package creates the directory structure shown in the figure below.

Figure 4. Cyclone V SoC Development Kit Directory Structure



3. For the latest issues and release notes, Altera recommends that you review the `readme.txt` located in the root directory of the kit installation.

Table 2. Installed Development Kit Directory Description

Lists the file directory names and a description of their contents.

Directory Name	Description of Directory Contents
`board_design_files`	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design.
`documents`	Contains the development kit documentation—quick start guides and user guide.
`examples`	Contains the sample design files for the Cyclone V SoC Development Kit: • Board Test System (BTS): BTS GUI, Power GUI, and Clock GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO PCIe 1.0 x4
`factory_recovery`	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Related Information

Cyclone V SoC Development Kit Website

2.3.4. Installing the Intel FPGA Download Cable II Driver

The Cyclone V SoC Development Kit includes onboard Intel FPGA Download Cable circuits for FPGA and system MAX V programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.

Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the *Cable and Adapter Drivers Information* link to locate the table entry for your configuration and click the link to access the instructions.

Related Information

Cable and Adapter Drivers Information

3. Development Kit Setup

The instructions in this section explain how to setup the Cyclone V SoC Development Kit for specific use cases.

3.1. Setting Up the Development Kit

To prepare the board, perform these steps:

1. The development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in the *Factory Default Switch and Jumper Settings* section to return the board to its factory settings before proceeding.

   The development board ships with the Golden System Reference Design (GSRD) binaries stored in the microSD card.

   The microSD card also includes the following:

   - Hardware reference design FPGA image, Raw Binary File (`.rbf`) file
   - HPS image preloader U-Boot and Linux images
   - File system and software examples

2. Power up the development board using the included power supply adapter. Make sure that the power supply is connected to J40 if you are using the Power Solution 2 board (MMID: 99C5L6), and to J22 if you are using the Power Solution 1 board (MMID: 979996).

   Caution: Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage, and a lower-rated power supply may not be able to provide enough power for the board.

   Alternatively, you can use the an ATX power from a PC by plugging a 4-pin output from that supply to J20 on the development board.

   Caution: Make sure that the ATX supply is off when connecting to the board. Hotswap is not supported and may damage the board's power supplies and other downstream devices.

When configuration is complete, the Config Done LED (D38) illuminates, signaling that the Cyclone V device configured successfully.

Related Information

- Factory Default Switch and Jumper Settings on page 15
- Restoring the MAX V CPLD to the Factory Setting on page 22

3.2. Factory Default Switch and Jumper Settings

Cyclone V SoC Development Kit (Power Solution 2) and Cyclone V SoC Development Kit (Power Solution 1) ship with their board switches preconfigured to support the design examples in the development kits. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the next sections to return to their factory default settings before proceeding ahead.

Attention: The SD card, MAX V system controller, and common flash interface (CFI) flash are already programmed with the factory default files. For more information, refer to the *Appendix A—Programming Flash Memory* section.

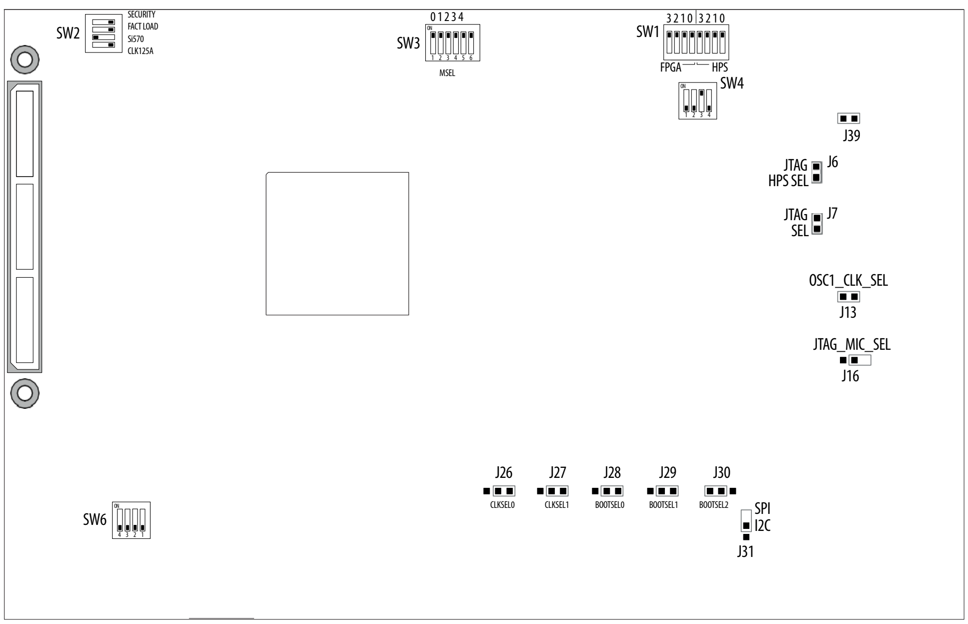
For more information about the FPGA board settings, refer to the *Cyclone V SoC Development Board Reference Manual*.

Related Information

- Programming Flash Memory on page 46
- Cyclone V SoC Development Board Reference Manual

3.2.1. Restoring the Default Settings for Power Solution 2 Board

Figure 5. Switch Locations and Default Settings for Power Solution 2 Board



To restore Cyclone V SoC Development Kit (Power Solution 2) board switches to their factory default settings, perform these steps:

1. Set the DIP switch bank (SW2) to match the *SW2 DIP Switch Settings* table.

   In the following table, ON indicates the switch is to the left according to the board orientation as shown in the *Switch Locations and Default Settings for Power Solution 2* figure.

Table 3. SW2 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	CLK125A	Switch 1 has the following options: • ON (0)—Onboard oscillator is disabled. • OFF (1)—Onboard oscillator is enabled.	OFF
2	Si570	Switch 2 has the following options: • ON (0)—Onboard programmable oscillator is enabled. • OFF (1)—Onboard programmable oscillator is disabled.	ON
3	FACT LOAD	Switch 4 has the following options: • ON (0)—Load the factory design starting at 0x20000 at power up. • OFF (1)—Parallel flash loader (PFL) disabled.	OFF
4	Security	Switch 4 has the following options: • ON (0)—Onboard Intel FPGA Download Cable II sends FACTORY command at power up. • OFF (1)—Onboard Intel FPGA Download Cable II does not send FACTORY command at power up.	OFF

2. Set the DIP switch bank (SW3) to match the *SW3 DIP Switch Settings* table.

   In the following table, *up* and *down* indicates the position of the switch with the board orientation as shown in the *Switch Locations and Default Settings for Power Solution 2* figure.

   Important: The default MSEL pin settings are set to all zeroes (ON) to select the fast passive parallel x16 mode. For power-up configuration from MAX V and CFI flash, ensure that the MAX V design uses this same mode as does in the design in the `cycloneVSX_5csxfc6df31_soc\examples\max5` directory.

Table 4. SW3 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	MSEL0	Switch 1 has the following options: • ON (*up*)—MSEL0 is 0. • OFF (*down*)—MSEL0 is 1.	ON
2	MSEL1	Switch 2 has the following options: • ON (*up*)—MSEL1 is 0. • OFF (*down*)—MSEL1 is 1.	ON
3	MSEL2	Switch 3 has the following options: • ON (*up*)—MSEL2 is 0. • OFF (*down*)—MSEL2 is 1.	ON
4	MSEL3	Switch 4 has the following options: • ON (*up*)—MSEL3 is 0. • OFF (*down*)—MSEL3 is 1.	ON
5	MSEL4	Switch 5 has the following options: • ON (*up*)—MSEL4 is 0. • OFF (*down*)—MSEL4 is 1.	ON

3. Set the DIP switch bank (SW4) to match the *SW4 JTAG DIP Switch Settings* table.

In the following table, *up* and *down* indicates the position of the switch with the board orientation as shown in the *Switch Locations and Default Settings for Power Solution 2* figure.

Table 5. SW4 JTAG DIP Switch Settings

Switch	Board Label	Function	Default Position
1	HPS	• ON (*up*)—Do not include HPS in the JTAG chain. • OFF (*down*)—Include HPS in the JTAG chain.	OFF
2	FPGA	• ON (*up*)—Do not include the FPGA in the JTAG chain. • OFF (*down*)—Include the FPGA in the JTAG chain.	OFF
3	HSMC	• ON (*up*)—Do not include the HSMC connector in the JTAG chain. • OFF (*down*)—Include the HSMC connector in the JTAG chain.	ON
4	MAX	• ON (*up*)—Do not include the MAX V system controller in the JTAG chain. • OFF (*down*)—Include the MAX V system controller in the JTAG chain.	OFF

4. Set the DIP switch bank (SW6) to match the *SW6 JTAG DIP Switch Settings* table.

   In the following table, *up* and *down* indicates the position of the switch with the board orientation as shown in the *Switch Locations and Default Settings for Power Solution 2* figure.

Table 6. SW6 JTAG DIP Switch Settings

Switch	Board Label	Function	Default Position
1	I2C_SDA_HPS	• ON (*down*)—Include HPS in the JTAG chain. • OFF (*up*)—Do not include HPS in the JTAG chain.	ON
2	I2C_SCL_HPS	• ON (*down*)—Include HPS in the JTAG chain. • OFF (*up*)—Do not include HPS in the JTAG chain.	ON
3	I2C_SCL	• ON (*down*)—Include the FPGA in the JTAG chain. • OFF (*up*)—Do not include the FPGA in the JTAG chain.	ON
4	I2C_SDA	• ON (*down*)—Include the FPGA in the JTAG chain. • OFF (*up*)—Do not include the FPGA in the JTAG chain.	ON

5. Set the following jumper blocks to match the *Default Jumper Settings for Power Solution 2 Board* table and the *Switch Locations and Default Settings for Power Solution 2 Board* figure.

Table 7. Default Jumper Settings for Power Solution 2 Board

Switch	Board Label	Function	Default Position
J6	JTAG HPS SEL	• SHORT—Controls the HPS from the onboard Intel FPGA Download Cable II JTAG master. • OPEN—Controls the HPS from Mictor-based JTAG master, such as DSTREAM* or Lauterbach* programming cables. Also, set SW4.1 to ON to remove the onboard Intel FPGA Download Cable II from driving the HPS JTAG input port in this mode.	SHORT
J7	JTAG SEL	• SHORT—The Intel FPGA Download Cable II is the source of the JTAG chain. • OPEN—The Mictor is the source of the JTAG chain.	SHORT
J13	OSC1_CLK_SEL	• SHORT—Selects the onboard 25 MHz clock. • OPEN—Selects SMA.	SHORT
J16	JTAG MIC SEL	• SHORT—JTAG TRST input to HPS driven from the JTAG chain. • OPEN—JTAG TRST input to HPS driven from the Mictor.	OPEN
J26	CLKSEL0	Selects the HPS clock settings.(1)	SHORT pins 2-3
J27	CLKSEL1	Selects the HPS clock settings.(1)	SHORT pins 2-3
J28	BOOTSEL0	Selects the boot mode and source for the HPS.(1)	SHORT pins 1-2
J29	BOOTSEL1	Selects the boot mode and source for the HPS.(1)	SHORT pins 2-3
J30	BOOTSEL2	Selects the boot mode and source for the HPS.(1)	SHORT pins 1-2
J31	SPI I2C	• SHORT—Select SPI bus access from HPS to Linear Tech daughter card interface through J32. • OPEN—Select I^2C bus access from HPS to Linear Tech daughter card interface through J32.(2)	OPEN
J39	—	• SHORT—External Mictor 38-pin connector's pin 14 is powered by 3.3 V rail. • OPEN—External Mictor 38-pin connector's pin 14 is floating.	SHORT

Related Information

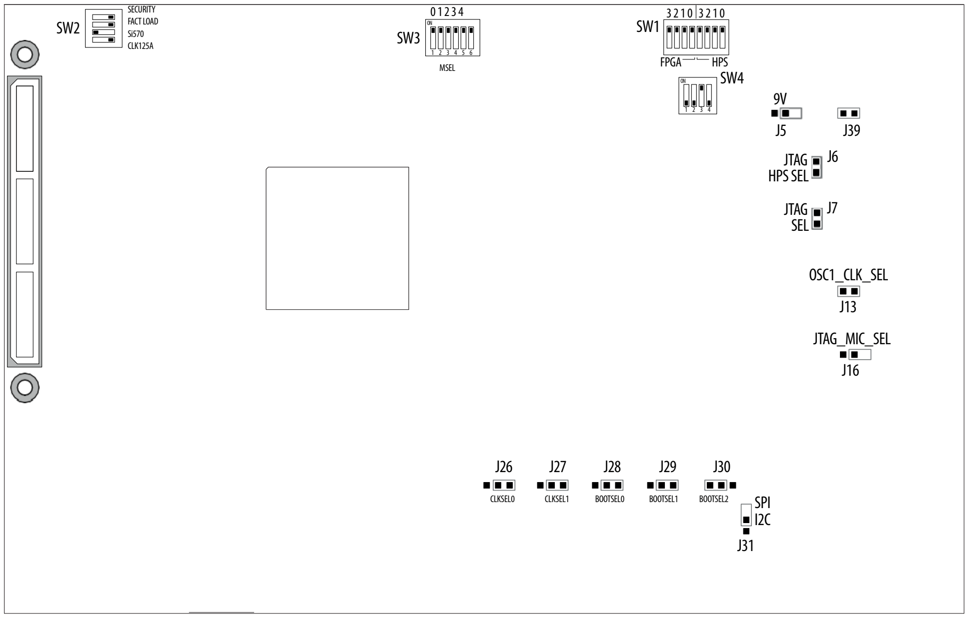
Cyclone V Device Handbook: Volume 1: Device Interfaces and Integration

(1) For more information, refer to the *Cyclone V Device Handbook Volume 1: Device Interfaces and Integration*.

(2) This connection can be software controlled from the HPS GPIO pin F16 on rev D and later boards.

3.2.2. Restoring the Default Settings for Power Solution 1 Board

Figure 6. Switch Locations and Default Settings for Power Solution 1 Board



To restore the Cyclone V SoC Development Kit (Power Solution 1) board switches to their factory default settings, perform these steps:

1. Set the DIP switch bank (SW2) to match the *SW2 DIP Switch Settings* table.

   In the following table, ON indicates the switch is to the left according to the board orientation as shown in the *Switch Locations and Default Settings for Power Solution 1* figure.

Table 8. SW2 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	CLK125A	Switch 1 has the following options: • ON (0)—Onboard oscillator is disabled. • OFF (1)—Onboard oscillator is enabled.	OFF
2	Si570	Switch 2 has the following options: • ON (0)—Onboard programmable oscillator is enabled. • OFF (1)—Onboard programmable oscillator is disabled.	ON
3	FACT LOAD	Switch 4 has the following options: • ON (0)—Load the factory design starting at 0x20000 at power up. • OFF (1)—Parallel flash loader (PFL) disabled.	OFF
4	Security	Switch 4 has the following options: • ON (0)—Onboard Intel FPGA Download Cable II sends FACTORY command at power up. • OFF (1)—Onboard Intel FPGA Download Cable II does not send FACTORY command at power up.	OFF

2. Set the DIP switch bank (SW3) to match the *SW3 DIP Switch Settings* table.

In the following table, *up* and *down* indicates the position of the switch with the board orientation as shown in the *Switch Locations and Default Settings for Power Solution 1* figure.

Important: The default MSEL pin settings are set to all zeroes (ON) to select the fast passive parallel x16 mode. For power-up configuration from MAX V and CFI flash, ensure that the MAX V design uses this same mode as does in the design in the `cycloneVSX_5csxfc6df31_soc\examples\max5` directory.

Table 9. SW3 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	MSEL0	Switch 1 has the following options: • ON (*up*)—MSEL0 is 0. • OFF (*down*)—MSEL0 is 1.	ON
2	MSEL1	Switch 2 has the following options: • ON (*up*)—MSEL1 is 0. • OFF (*down*)—MSEL1 is 1.	ON
3	MSEL2	Switch 3 has the following options: • ON (*up*)—MSEL2 is 0. • OFF (*down*)—MSEL2 is 1.	ON
4	MSEL3	Switch 4 has the following options: • ON (*up*)—MSEL3 is 0. • OFF (*down*)—MSEL3 is 1.	ON
5	MSEL4	Switch 5 has the following options: • ON (*up*)—MSEL4 is 0. • OFF (*down*)—MSEL4 is 1.	ON

3. Set the DIP switch bank (SW4) to match the *SW4 JTAG DIP Switch Settings* table.

   In the following table, *up* and *down* indicates the position of the switch with the board orientation as shown in the *Switch Locations and Default Settings for Power Solution 1* figure.

Table 10. SW4 JTAG DIP Switch Settings

Switch	Board Label	Function	Default Position
1	HPS	• ON (*up*)—Do not include HPS in the JTAG chain. • OFF (*down*)—Include HPS in the JTAG chain.	OFF
2	FPGA	• ON (*up*)—Do not include the FPGA in the JTAG chain. • OFF (*down*)—Include the FPGA in the JTAG chain.	OFF
3	HSMC	• ON (*up*)—Do not include the HSMC connector in the JTAG chain. • OFF (*down*)—Include the HSMC connector in the JTAG chain.	ON
4	MAX	• ON (*up*)—Do not include the MAX V system controller in the JTAG chain. • OFF (*down*)—Include the MAX V system controller in the JTAG chain.	OFF

4. Set the following jumper blocks to match the *Default Jumper Settings for Power Solution 1 Board* table and the *Switch Locations and Default Settings for Power Solution 1 Board* figure.

Table 11. Default Jumper Settings for Power Solution 1 Board

Switch	Board Label	Function	Default Position
J5	9V	• SHORT—Powers the CFI flash memory device using a 9 V supply for fast write in manufacturing. • OPEN—Powers CFI flash memory from the default 3 V supply.	OPEN
J6	JTAG HPS SEL	• SHORT—Controls the HPS from the onboard Intel FPGA Download Cable II JTAG master. • OPEN—Controls the HPS from Mictor-based JTAG master, such as DSTREAM* or Lauterbach* programming cables. Also, set SW4.1 to ON to remove the onboard Intel FPGA Download Cable II from driving the HPS JTAG input port in this mode.	SHORT
J7	JTAG SEL	• SHORT—The Intel FPGA Download Cable II is the source of the JTAG chain. • OPEN—The Mictor is the source of the JTAG chain.	SHORT
J13	OSC1_CLK_SEL	• SHORT—Selects the onboard 25 MHz clock. • OPEN—Selects SMA.	SHORT
J16	JTAG MIC SEL	• SHORT—JTAG TRST input to HPS driven from the JTAG chain. • OPEN—JTAG TRST input to HPS driven from the Mictor.	OPEN
J26	CLKSEL0	Selects the HPS clock settings.(3)	SHORT pins 2-3
J27	CLKSEL1	Selects the HPS clock settings.(3)	SHORT pins 2-3
J28	BOOTSEL0	Selects the boot mode and source for the HPS.(3)	SHORT pins 1-2
J29	BOOTSEL1	Selects the boot mode and source for the HPS.(3)	SHORT pins 2-3
J30	BOOTSEL2	Selects the boot mode and source for the HPS.(3)	SHORT pins 1-2
J31	SPI I2C	• SHORT—Select SPI bus access from HPS to Linear Tech daughter card interface through J32. • OPEN—Select I^2C bus access from HPS to Linear Tech daughter card interface through J32.(4)	OPEN
J39	—	• SHORT—External Mictor 38-pin connector's pin 14 is powered by 3.3 V rail. • OPEN—External Mictor 38-pin connector's pin 14 is floating.	SHORT

Related Information

Cyclone V Device Handbook: Volume 1: Device Interfaces and Integration

(3) For more information, refer to the *Cyclone V Device Handbook Volume 1: Device Interfaces and Integration*.

(4) This connection can be software controlled from the HPS GPIO pin F16 on rev D and later boards.

3.3. Restoring the MAX V CPLD to the Factory Setting

You can restore the original factory contents to the MAX V CPLD on the development board. Make sure you have the Quartus Prime software installed, and then perform these steps.

1. Set the board switches to the factory default settings described in the *Factory Default Switch and Jumper Settings* section.

   Attention: DIP switch SW4.4 includes the MAX V device in the JTAG chain.
2. Launch the Quartus Prime Programmer.
3. Click **Auto Detect**.
4. Click **Add File** and select `cycloneVSX_5csxfc6df31_soc\factory_recovery\max`<*no_ver*>`.pof`.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and product information, refer to the *Cyclone V SoC Development Kit* page of the Intel website.

Related Information

- Factory Default Switch and Jumper Settings on page 15
- Cyclone V SoC Development Kit Website

3.4. Restoring CFI Flash Device to the Factory Defaults

To program the factory image to the flash device in the Quartus Prime Programmer, do the following steps:

1. On the **Tools** menu in the Quartus Prime software, click **Programmer**.
2. In the Programmer window, click **Auto-Detect**.

   Note: If you do not see Intel FPGA Download Cable or the board's embedded Intel FPGA Download Cable II listed next to **Hardware Setup**, refer to the *Quartus Prime Software and Driver Installation* section.
3. Click **Add File** and open `cycloneVSX_5csxfc6df31_soc\factory_recovery\max2_PFL_writer.pof`.
4. Turn on the **Program/Configure** option for the `.pof` file.
5. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.
6. Click **Auto Detect** and a flash device should show up attached to the MAX V in the main window.
7. Double-click the graphic of the flash device in the device chain pane to display the **Device's Properties** dialog box.
8. Select the flash image `.pof` file: `cycloneVSX_5csxfc6df31_soc\factory_recovery\output_file.pof`.
9. Once the flash image `.pof` is attached in the Quartus Prime Programmer, turn on **Page_1** and **Option Bits**. (**Page_0** is reserved for the GSRD factory design.)

10. Click **Start**.
11. After the flash writing process has completed, power cycle the board and look for the MAX CONF DONE LED to turn ON if successful.
12. Altera recommends that you return to the MAX V System Controller factory design after completing the flash writing. To do so, program the MAX V with `cycloneVSX_5csxfc6df31_soc\factory_recovery\max<version>.pof`. For more information, refer to the *Restoring the MAX V CPLD to the Factory Settings* section.

    Note: The flash writer version blinks the SEL 2, 1, and 0 LEDs and does not support the Power Monitor, Clock Control, or other logic functions. Use the flash writer only for flash programming.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the *Cyclone V SoC Development Kit* webpage of the Intel website.

Related Information

- Restoring the MAX V CPLD to the Factory Setting on page 22
- Cyclone V SoC Development Kit Website

4. Board Update Portal

The Board Update Portal web page provides links to useful information on the Intel website. You can use this web page to interact with your board:

- Blinking LEDs
- Writing text messages to the LCD
- Mouse over the board photo to view features

The Board Update Portal web page is served by the web server application running on the HPS on your board.

4.1. Connecting to the Board Update Portal Web Page

Ensure that you have the following setup or installed:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. Keep the CSEL and BSEL jumpers and the DIP switch SW2.3 in the factory default positions.
2. Change J26 as Short1-2 and set SW as follows:
   - SW1: ALL OFF
   - SW2: ALL OFF
   - SW3: ON-OFF-ON-OFF-ON-ON
   - SW4: OFF-OFF-ON-ON
3. Download image to SD card and insert SD card to J3.
4. Connect J8 to your computer and power up the board.
5. Install the USB virtual COM port drivers to access the Linux system through a terminal window.
6. Type `ifconfig` to get the IP address as root.

   For more information, refer to the Cyclone V SOC GSRD page on RocketBoards.org.

Attention: There are several reasons why your board may fail to get and IP address in this step:

- Your port is not active or the cable is not plugged in.
- You do not have a DHCP server.
- Your DHCP server ran out of addresses.
- Your DHCP server was not allowed to respond to the board due to security filters, such as MAC address filtering.

7. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

   Attention: You can click Cyclone V SoC Development Kit on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

   You can also navigate directly to the Cyclone V SoC Development Kit webpage of the Intel website to determine if you have the latest kit software.

5. Board Test System

The Cyclone V SoC Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

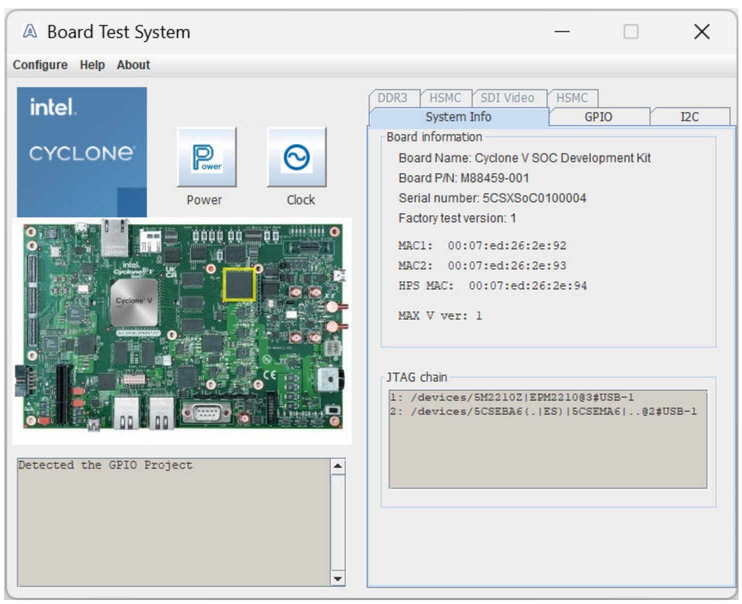
To install the BTS, follow the steps in the *Installing the Development Kit* section.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Cyclone V device.

The BTS checks for hardware faults before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

The following figure shows the GUI of a board that is in factory configuration.

Figure 7. BTS GUI



Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears that allows you to exercise the related board features.

The **Power Monitor** button starts the Power Monitor application that measures and reports current power information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs.

Attention: The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios® II debugger and the Signal Tap logic analyzer. Because the Quartus Prime programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus Prime Programmer.

5.1. Preparing the Board for the Board Test System

With the power to the board off, follow these steps:

1. Plug the included USB cable from J37 (Intel FPGA Download Cable II interface) to the host computer's USB port.
2. Ensure that the development board switches and jumpers are set to the default positions as shown in the *Factory Default Switch and Jumper Settings* section.

   For more information about the board’s DIP switch and jumper settings, refer to the *Cyclone V SoC Development Board Reference Manual*.

Caution: To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Related Information

- Factory Default Switch and Jumper Settings on page 15
- Cyclone V SoC Development Board Reference Manual

5.2. Running the Board Test System

Navigate to the `cycloneVSX_5csxfc6df31_soc\examples\board_test_system` directory and double click the `BoardTestSystem.bat`.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. Typically, the board is not pre-programmed with a BTS design. You must load using the Configure menu as described in the next section.

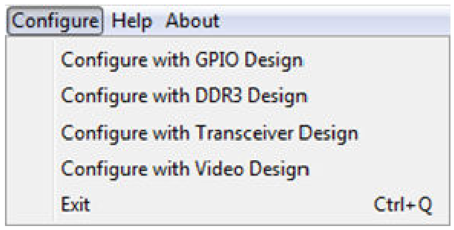
5.3. Using the Board Test System

This section describes each control in the BTS.

5.3.1. The Configure Menu

Use the Configure menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs. For example, if you select **Configure with GPIO Design**, the **System Info**, **GPIO**, and **I2C** tabs become active.

Figure 8. The Configure Menu



5.3.2. The System Info Tab

The **System Info** tab shows information about the board's current configuration. The tab displays the content of the MAX V registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

Figure 9. The System Info Tab

The following sections describe the controls on the **System Info** tab.

Board Information

The **Board information** control displays static information about your board.

- **Board Name**: Indicates the official name of the board.
- **Part number**: Indicates the part number of the board.
- **Serial number**: Indicates the serial number of the board.
- **Factory test version**: Indicates the version of the Board Test System currently running on the board.
- **MAC1**: Indicates the MAC address of the board's ENET1 10/100 port.
- **MAC2**: Indicates the MAC address of the board's ENET2 10/100 port.
- **HPS MAC1**: Indicates the MAC address of the board's HPS 10/100/1000 Ethernet port.
- **MAX V ver**: Indicates the version of MAX V code currently running on the board. The MAX V code resides in the `cycloneVSX_5csxfc6df31_soc\examples` directory. Newer revisions of this code might be available on the Cyclone V SoC Development Kit webpage of the Intel website.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Cyclone V device is always the first device in the chain. The JTAG chain is normally mastered by the onboard Intel FPGA Download Cable II.

Note: If you plug in an external onboard Intel FPGA Download Cable cable to the JTAG header (J23), the onboard Intel FPGA Download Cable II is disabled.

Note: JTAG DIP switch bank (SW4) selects which interfaces are in the chain. Refer to the *SW4 JTAG DIP Switch Settings* table in the *Factory Default Switch and Jumper Settings* section for detailed settings.

For details on the JTAG chain, refer to the *Cyclone V SoC Development Board Reference Manual*. For Intel FPGA Download Cable II configuration details, refer to the *Cable and Adapter Drivers Information* webpage of the Intel website.

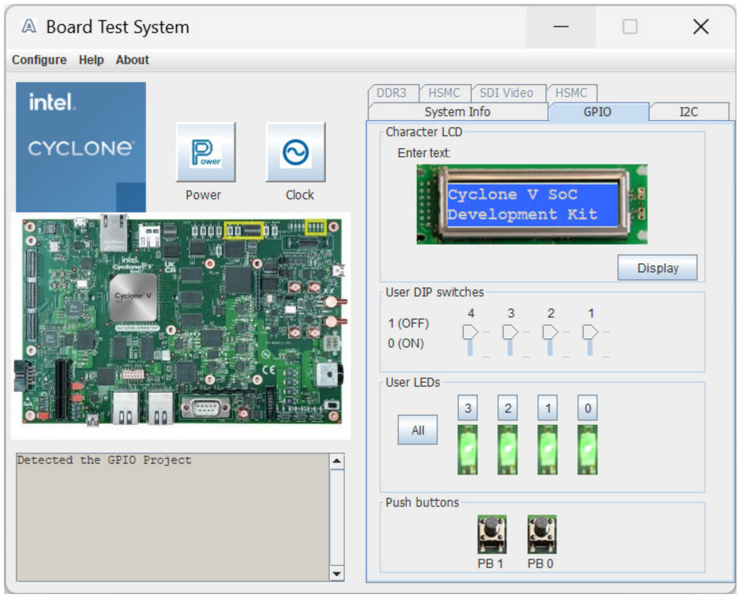
Related Information

- Factory Default Switch and Jumper Settings on page 15
- Cyclone V SoC Development Board Reference Manual

5.3.3. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses.

Figure 10. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

Attention: If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switches

The read-only **User DIP switches** control displays the current positions of the switches in the user DIP switch bank. Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Click the graphical representation of the LEDs to turn the board LEDs on and off. You can click **ALL** to turn on and off all of the user LEDs at once.

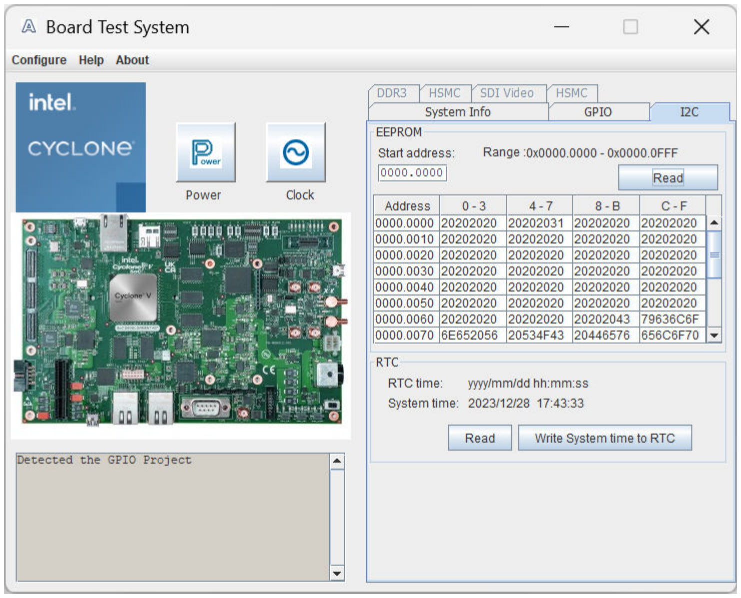
Push Buttons

The read-only **Push Buttons** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly

5.3.4. The I2C Tab

The **I2C** tab allows you to read and write 1 kilobit (Kb) to an I2C EEPROM located at U28 on the development board

Figure 11. The I2C Tab



The following sections describe the controls on the **I2C** tab.

EEPROM

The serial I^{2}C EEPROM is 32 Kilobits.

- **Start Address**: 0x0
- **Range**: 0x1000
- **Read**: Reads data from the I2C EEPROM.

For more information on the EEPROM, refer to the *Cyclone V SoC Development Board Reference Manual*.

RTC

Real time clock.

- **Current Time**: Displays current time stored in RTC memory when you click Read. It is not updated automatically.
- **System Time**: Displays current time from PC and is updated automatically.
- **Read**: Reads the time from the RTC device on the board.
- **Write System Time to RTC**: Writes the time to the RTC device on the board.

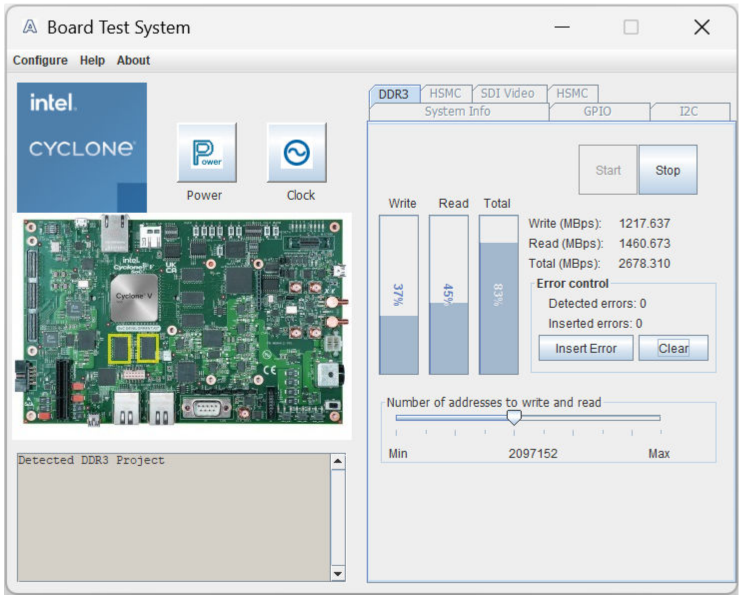
Related Information

Cyclone V SoC Development Board Reference Manual

5.3.5. The DDR3 Tab

The **DDR3** tab allows you to read and write the DDR3 memory on your board.

Figure 12. The DDR3 Tab



The following sections describe the controls on the **DDR3** tab.

Start

The **Start** control initiates DDR3 memory transaction performance analysis.

Stop

The **Stop** control terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write, Read, and Total performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps), Read (MBps), and Total (MBps)**: Show the number of bytes of data analyzed per second. The data bus is 72 bits wide and the frequency is 400 MHz double data rate (800 Mbps per pin), equating to a theoretical maximum bandwidth of 3200 Megabits per second or 400 MBps.

Error Control

The **Error control** control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**: Displays the number of data errors detected in the hardware.
- **Inserted errors**: Displays the number of errors inserted into the transaction stream.
- **Insert Error**: Inserts a one-word error into the transaction stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**: Resets the Detected errors and Inserted errors counters to zeros.

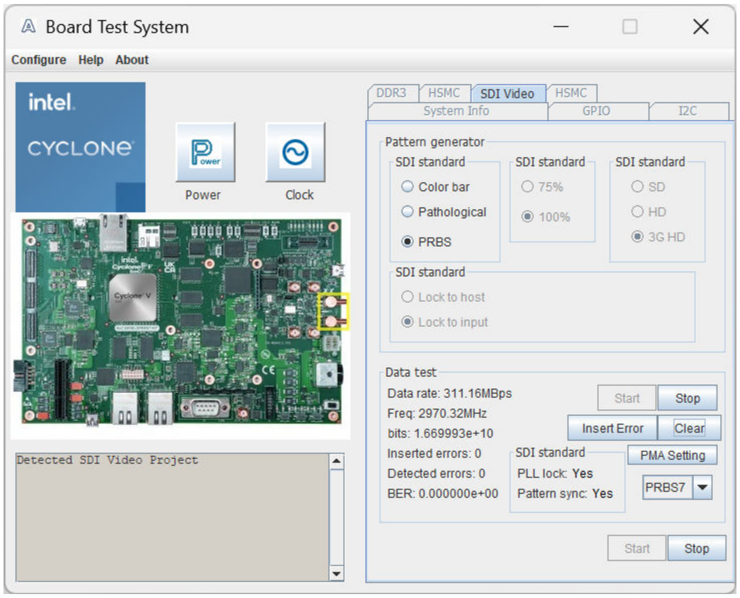
Number of Addresses to Write and Read

The **Number of addresses to write and read** control determines the number of addresses to use in each iteration of reads and writes.

5.3.6. The SDI Video Tab

The **SDI Video** tab allows you to test the SDI video interface on your board.

Figure 13. The SDI Video Tab



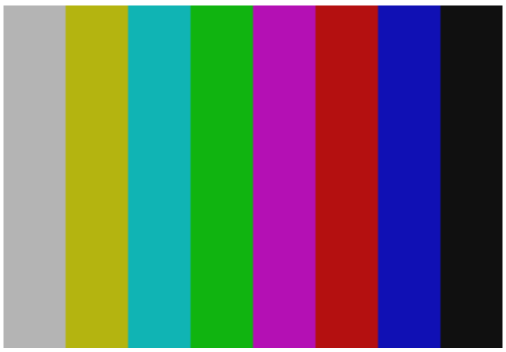
The following sections describe the controls on the **SDI Video** tab.

Pattern Generator

This control specifies the test pattern to output to the monitor. The following choices are available:

- **Color bar**: Specifies a video color bar pattern with eight vertical color bars as shown in table below.

Table 12. HDMI Color Bar Test Pattern

Color Bar	Color	RGB Values
	White/Grey	180,180,180
	Yellow	180,180,16
	Cyan	16,180,180
	Green	16,180,16
	Magenta	180,16,180
	Red	180,16,16
	Blue	16,16,180
	Black	16,16,16

- **Pathological**: Specifies a video color bar pattern with two horizontal color bars that stresses the receive PLL.
- **PRBS**: Specifies a pseudo-random bit sequence useful for electrical testing of the interface for data integrity.

Intensity

Specifies the color intensity of the transmitted color bar pattern. The following choices are available.

- **75%**: Specifies 75% intensity.
- **100%**: Specifies 100% intensity.

SDI Standard

Specifies the video standard used by the pattern generator on the SDI video stream. The following choices are available:

- **SD**: Specifies a 270 Mbps data rate.
- **HD**: Specifies a 1.485 Gbps data rate.
- **3G HD**: Specifies a 2.97 Gbps data rate.

Data Test

This group displays information about the SDI interface test when running in PRBS mode in the patter generator

- **Data rate**: Displays the current SDI data rate in megabytes per second (MBps).
- **Freq**: Displays the data rate frequency in MHz which is equivalent to Mbps.
- **Bits**:Displays the number of bits transmitted since clicking Start.

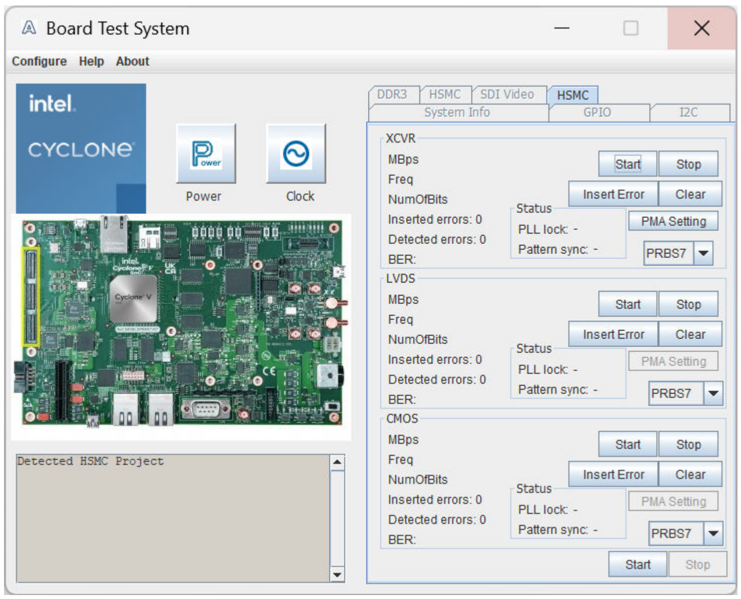
- **Inserted errors**: Displays the number of errors inserted by clicking Insert Error button.
- **Detected errors**: Displays the number of bit errors detected by the error checking circuitry.
- **BER**: Displays the bit error rate of the interface.
- **PLL lock**: Displays Yes if the SDI PLL is locked.
- **Pattern Sync**: Displays Yes if the receiver has detected the input data pattern.
- **Start**: Starts the PRBS data test and begins to monitor and update screen with live test results.
- **Stop**: Stops the PRBS data test.
- **Insert Error**: Inserts an error into an SDI data stream that is detected by the receiver when in loopback using the included video cable.
- **Clear**: Clears the Detected errors counter.
- **PMA Setting**: Opens the PMA settings window that allows for adjusting the analog transceiver settings, such as output voltage, loopback settings, and equalization.
- **PRBS (list)**: Selects the transmit pattern and sets the receive error detection circuitry to expect the same pattern for use in loopback testing.

5.3.7. The HSMC Tab

The HSMC tab allows you to perform loopback tests on the XCVR, LVDS, and CMOS ports.

Note: This tab requires that a `bts.ini` file with QTS=ON specified at the 1st line reside in the same directory as `BoardTestSystem.bat`. Removing or renaming this file runs an older version of this tab, which is grayed out by default. See the `readme.txt` in that same directory for more information.

Figure 14. The HSMC Tab



Attention: You must have the loopback HSMC installed on the HSMC Port A connector for this test to work correctly.

The following sections describe the controls on the HSMC tab.

Start, Stop

The **Start** and **Stop** controls at the bottom-right of this tab allow you to start and stop testing for all three ports.

XVCR, LVDS, CMOS

These groups displays the following XCVR, LVDS, and CMOS status information during the loopback test:

- **Data rate**: Displays the current XCVR data rate in megabytes per second (MBps).
- **Freq**: Displays the data rate frequency in MHz which is equivalent to Mbps.
- **Bits**: Displays the number of bits transmitted since clicking Start
- **Inserted errors**: Displays the number of errors inserted by clicking Insert Error button.

- **Detected errors**: Displays the number of bit errors detected by the error checking circuitry.
- **BER**: Displays the bit error rate of the interface.
- **PLL lock**: Displays Yes if the SDI PLL is locked.
- **Pattern Sync**: Displays Yes if the receiver has detected the input data pattern.
- **Start**: Starts the PRBS data test and begins to monitor and update screen with live test results.
- **Stop**: Stops the PRBS data test.
- **Insert Error**: Inserts an error into a data stream that is detected by the receiver when in loopback using the included video cable.

  With the **Insert Error**, there are differences among the three ports:
  - **XCVR**: inserts 4 errors at 1 click due to 4 test control blocks in the design.
  - **LVDS**: inserts 3 errors at 1 click due to 3 test control blocks in the design.
  - **CMOS**: inserts 1 error at 1 click.
- **Clear**: Clears the Detected errors counter.
- **PMA Setting**: Opens the PMA settings window that allows for adjusting the analog transceiver settings, such as output voltage, loopback settings, and equalization.

  The following settings are available for analysis:
  - **Serial Loopback**: Routes the selected TX output signal back to the RX input signal on-chip to verify operation without using an external loopback board.
  - **VOD**: Specifies the voltage output (differential) of the transmitter buffer.
  - **Pre-emphasis tap**
    - **Pre**: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
    - **First post**: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
    - **Second post**: Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.

      Attention: Support for this tap is device and software version dependent.
  - **Equalizer**: Specifies the setting for the receiver equalizer.
  - **DC gain**: Specifies the DC portion of the receiver equalizer.
- **PRBS**: Selects the transmit pattern and sets the receive error detection circuitry to expect the same pattern for use in loopback testing.

5.4. The Power Monitor

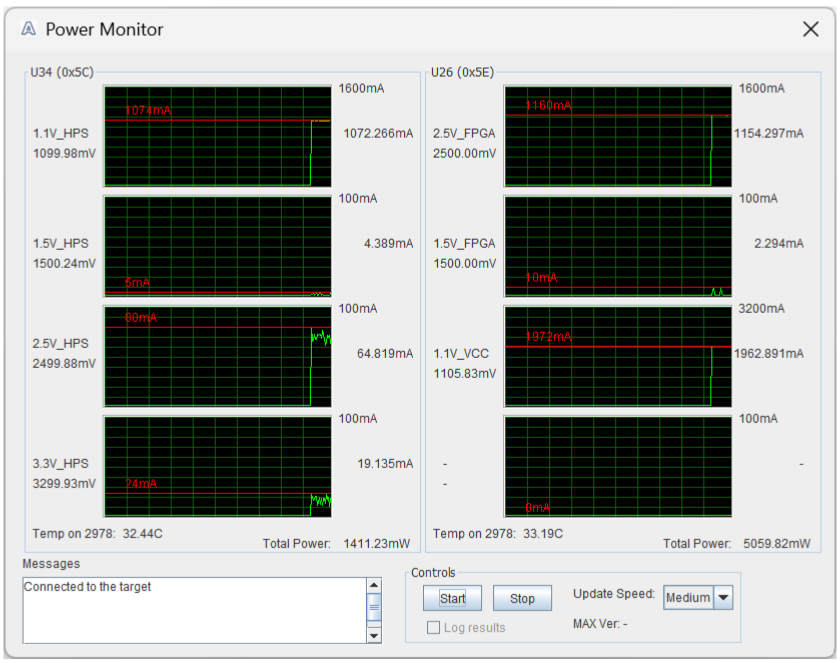
The Power Monitor measures and reports current power information. To start the application, click **Power Monitor** in the Board Test System application.

Attention: You can also run the Power Monitor as a stand-alone application. `PowerMonitor.bat` resides in the `cycloneVSX_5csxfc6df31_soc\examples\board_test_system` directory.

The Power Monitor communicates with the MAX V device on the board through the JTAG bus. A power monitor circuit attached to the MAX V device allows you to measure the power that the Cyclone V FPGA is consuming.

Attention: The Power Monitor measures power over an I^{2}C bus with multiple masters. You might see some glitches in the measurements if the HPS is booted. The GSRD and other Linux images access the I^{2}C bus periodically and cause inaccurate measurements for a cycle or two. These should go away and likely return to an accurate, steady state measurement for most designs.

Figure 15. The Power Monitor



The following sections describe the Power Monitor controls.

U34 and U26

The U34 and U26 groups show the power rail graphs. They display the mA power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset.

Attention: You can enlarge a graph by clicking on it. Click it again to restore the original size.

- **Temp on 2978**: The temperature controls display only the temperature from the power supply manager, not the FPGA.
- **Total Power**: These controls display the sum of all four rails for each group, U34 and for U26.

Controls

This group contains the following controls:

- **Start**: Starts the communication with the board to monitor power.
- **Stop**: Stops the communication with the board to monitor power.
- **Update** speed: Specifies how often to refresh the graph.
- **Log Results**: Specifies that a log file is saved to `cycloneVSX_5csxfc6df31_soc\examples\board_test_system`.
- **MAX V version**—Indicates the version of MAX V code currently running on the board. The MAX V code resides in the following directories:
  - `cycloneVSX_5csxfc6df31_soc\factory_recovery`
  - `cycloneVSX_5csxfc6df31_soc\examples\max5`

A table with the power rail information is available in the Cyclone V SoC Development Board Reference Manual.

Related Information

Cyclone V SoC Development Board Reference Manual

5.5. The Clock Control

The Clock Control application sets the Si570 or Si571 programmable oscillators to any frequency between 10 MHz and 810 MHz and Si5338. The frequencies support eight digits of precision to the right of the decimal point.

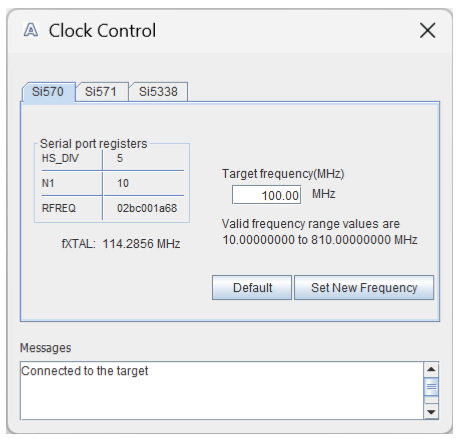
The Clock Control application runs as a stand-alone application. `ClockControl.bat` resides in the `cycloneVSX_5csxfc6df31_soc\examples\board_test_system` directory.

For more information about the Si570/Si571/Si5338 and the Cyclone V development board's clocking circuitry and clock input pins, refer to the *Cyclone V SoC Development Board Reference Manual*.

The Clock Control communicates with the MAX V device on the board through the JTAG bus. The Si570, Si571, and Si5338 programmable oscillators are connected to the MAX V device through a 2-wire serial bus.

The following figure shows the Clock Control Si570 tab.

Figure 16. The Clock Control—Si570



The following sections describe the Clock Control controls.

Serial Port Registers

The **Serial port registers** control shows the current values from the Si570 registers.

For more information about the Si570 registers, refer to the Si570/Si571 data sheet available on the Skyworks website.

fXTAL

The **fXTAL** control shows the calculated internal fixed-frequency crystal, based on the serial port register values. For more information about the f_{XTAL} value and how it is calculated, refer to the Si570/Si571 data sheet available on the Skyworks website.

Target Frequency

The **Target frequency** control allows you to specify the frequency of the clock. Legal values are between 10 and 810 MHz with eight digits of precision to the right of the decimal point. For example, 421.31259873 is possible within 100 parts per million (ppm). The **Target frequency** control works in conjunction with the **Set New Frequency** control.

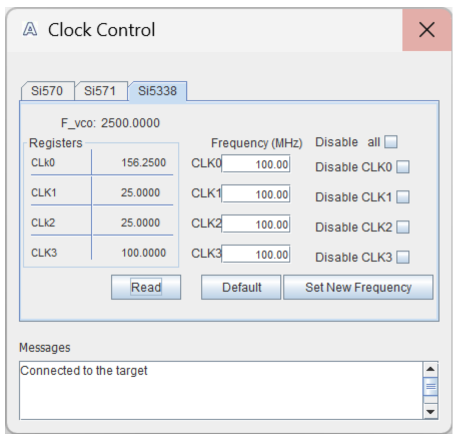
Default

This control sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set New Frequency

The **Set New Frequency** control sets the programmable oscillator frequency for the selected clock to the value in the **Target frequency** control for the Si570 and Si571. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends that you reset the FPGA logic after changing the frequencies.

Figure 17. The Clock Control—Si5338



Related Information

- Cyclone V SoC Development Board Reference Manual
- Skyworks Solutions

5.6. Configuring the FPGA Using the Quartus Prime Programmer

You can use the Quartus Prime Programmer to configure the FPGA with your SRAM Object File (`.sof`) file.

5.6.1. Before Configuring

Ensure the following:

- The Quartus Prime Programmer and the Intel FPGA Download Cable II driver are installed on the host computer.
- The USB cable is connected to the development board.
- Power to the board is on, and no other applications that use the JTAG chain are running.

If the Quartus Prime Programmer window is already open, and you power cycle the board, to detect the JTAG chain, do the following:

- Click **Hardware Setup** in the Quartus Prime Programmer window.
- Reselect Intel FPGA Download Cable II in order to properly detect the JTAG chain.

5.6.2. Configuring the FPGA

Perform these steps:

1. Start the Quartus Prime Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Add File** and select the path to the desired `.sof`.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Attention: Using the Quartus Prime Programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

6. Document Revision History for the Cyclone V SoC Development Kit User Guide

Document Version	Changes
2024.10.07	• Added new topics: — *Block Diagram* — *Feature Summary* — *Box Contents* — *Getting Started* — *Software and Driver Installation* — *Activating Your License* — *Restoring the Default Settings for Power Solution 2 Board* — *Restoring the Default Settings for Power Solution 1 Board* • Removed *References*. • Retitled topic *Software Installation* to *Software and Driver Installation*. • Retitled topic *Kit Features* to *Box Contents*. • Retitled topic *Inspect the Boards* to *Inspecting the Boards*. • Added information on Cyclone V SoC Development Kit (Power Solution 2) board. • Updated all figures in the document. • Added *Appendix—Development Kit Components* section. • Added *Appendix—Power* section. • Restructured the document to improve clarity and for ease of reference. • Updated the document for the latest branding standards.

Date	Version	Changes
September 2015	1.2	Updates for Rev. E PCB using Enpirion EN23x2 power products.
November 2013	1.1	Updates for production silicon and rev. D PCB using Enpirion power products.
May 2013	1.0	Initial release.

A. Development Kit Components

This chapter introduces all major components on the Cyclone V SoC Development Kit.

A.1. Board Overview

This section describes all the components on the development board. A complete set of schematics, a physical layout database, and Gerber files for the development board reside in the development kit document directory.

Figure 18. Components in Cyclone V SoC Development Kit (Power Solution 2)—Top View

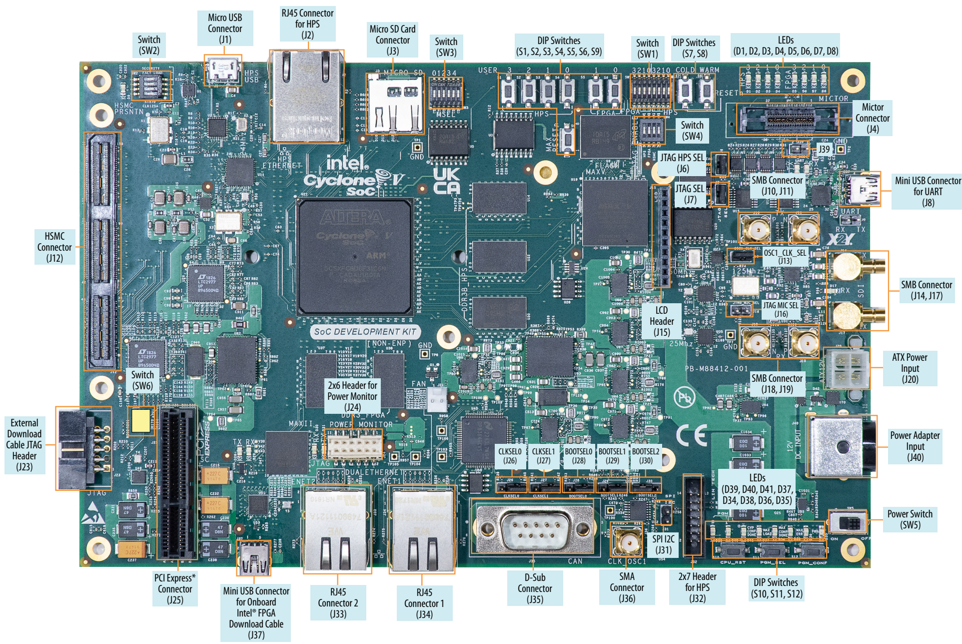
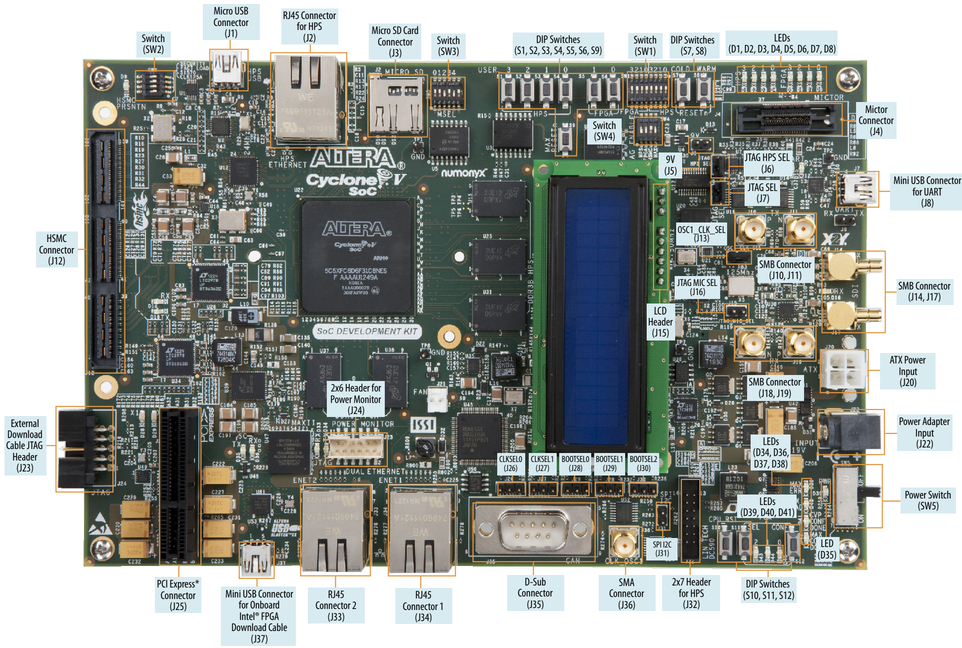


Figure 19. Components in Cyclone V SoC Development Kit (Power Solution 1)—Top View



A.2. Programming Flash Memory

This appendix describes programming information for the following memory devices:

- Common flash interface (CFI) flash memory
- Quad serial peripheral interface (quad SPI) flash memory
- SD card flash memory

The Cyclone V development board's flash memory ships preconfigured with the parallel flash loader (PFL) option bits to support FPGA designs to be written to any of the three locations as shown in the *Byte Address Flash Memory Map* table. The PFL is disabled by default. Set SW2.3 to ON to enable FPGA programming from CFI flash memory on power up.

There are several other factory software files written to flash memory to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus Prime software.

A.2.1. CFI Flash Memory

A.2.1.1. CFI Flash Memory Map

Table 13. Byte Address Flash Memory Map

This table shows the default memory contents of the 512 Mb CFI flash device.

Address Range	KB Size	Block Description
0x0145.635C – 03FF.FFFF	44,711	Unused
0x00DA.0000 – 0145.635B	6,872	User hardware 2
0x006E.0000 – 00D9.635B	6,872	User hardware 1
0x0002.0000 – 006D.635B	6,872	Factory hardware
0x0001.8000 – 0001.8080	32	PFL option bits

Caution: Altera recommends that you do not overwrite the factory hardware images unless you are an expert with Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to the *Restoring the CFI Flash Device to the Factory Defaults* section.

Related Information

Restoring CFI Flash Device to the Factory Defaults on page 22

A.2.1.2. Programming CFI Flash Using the Quartus Prime Programmer

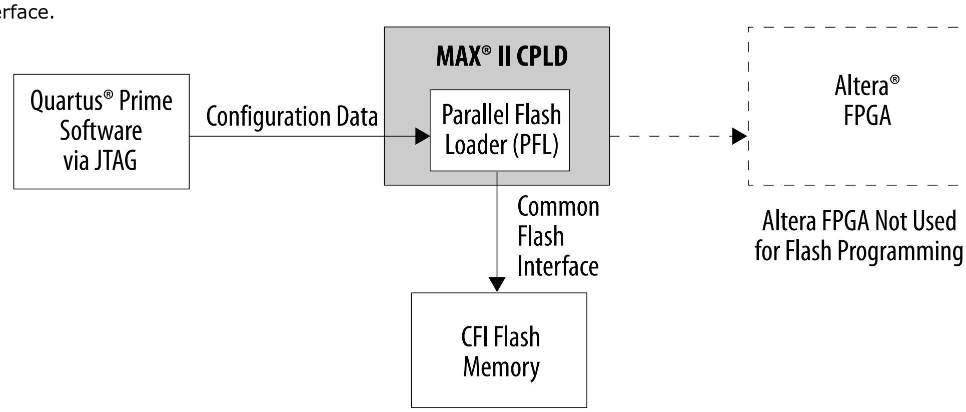
You can use the JTAG interface in Altera CPLDs to indirectly program the flash memory device. The Altera CPLD JTAG block interfaces directly with the logic array in a special JTAG mode.

This mode brings the JTAG chain through the logic array instead of the Altera CPLD boundary-scan cells (BSC). The Parallel Flash Loader Intel FPGA IP provides JTAG interface logic to do the following:

- Convert the JTAG stream provided by the Quartus Prime software.
- Program the CFI flash memory devices connected to the CPLD I/O pins.

Figure 20. Programming the CFI Flash Memory With the JTAG Interface

Shows an Altera CPLD configured as a bridge to program the CFI flash memory device through the JTAG interface.



Perform the following steps to program a user design to the flash device in the Quartus Prime Programmer:

Note: The following flash writing procedure blinks the SEL 2, 1, and 0 LEDs and does not support the Power Monitor, Clock Control, or other logic functions.

1. On the **Tools** menu in the Quartus Prime software, click **Programmer**.
2. In the **Programmer** window, click **Auto-Detect**.

   Note: If you do not see Intel FPGA Download Cable or the board's embedded Intel FPGA Download Cable II listed next to **Hardware Setup**, refer to the *Cable and Adapter Drivers Information* webpage in the Intel website.
3. Click **Add File** and open `cycloneVSX_5csxfc6df31_soc\factory_recovery\max2_PFL_writer.pof`.
4. Turn on the **Program/Configure** option for the `.pof` file.
5. Click **Start** to download the selected configuration file to the MAX V CPLD. Configuration is complete when the progress bar reaches 100%.
6. Click **Auto Detect** and a flash device should show up attached to the MAX V in the main window.
7. Double-click the graphic of the flash device in the device chain pane to display the **Device's Properties** dialog box.
8. Select the flash image `.pof` file generated from the Quartus Prime **Convert Programming Files** dialog box. The default file name is `output_file.pof`.
9. After the flash image `.pof` is attached in theQuartus Prime Programmer, turn on **Page_1** and **Option Bits**. (**Page_0** is reserved for the GSRD factory design.)
10. Click **Start**.
11. After the flash writing process has completed, power cycle the board and look for the MAX CONF DONE LED to turn ON if the writing process is successful.
12. Altera recommends that you return to the MAX V System Controller factory design after completing the flash writing. To do so, program the MAX V with `cycloneVSX_5csxfc6df31_soc\factory_recovery\max`<*version*>`.pof`. For more information refer to the *Restoring the MAX V CPLD to the Factory Settings* section.

    For more information on programming flash memory, refer to the *Parallel Flash Loader Intel FPGA IP User Guide* and *Using FPGA-Based Parallel Flash Loader with the Quartus Prime Software*.

Related Information

- Cyclone V SoC Development Board Reference Manual
- Restoring the MAX V CPLD to the Factory Setting on page 22
- Parallel Flash Loader Intel FPGA IP User Guide
- AN 478: Using FPGA-Based Parallel Flash Loader with the Quartus Prime Software

A.2.1.3. Converting `.sof` Files to a `.pof`

To generate a flash programming file, you must open the Quartus Prime software and convert the `.sof` files to `.pof`.

To convert the files, follow these steps:

1. On the File menu, click **Convert Programming Files**.
2. For **Programming file type**, specify **Programmer Object File (.pof)** and name the file.
3. For **Configuration device**, select **CFI_512Mb** for this kit's CFI device.
4. To add the configuration data, under **Input files to convert**, select **SOF Data**.
5. Click **Add File** and browse to the `.sof` files you want to add.

   If you want to store the data from other `.sof` files in a different page, click **Add SOF page**. Add the `.sof` files to the new page
6. Select **SOF Data** and click **Properties** to set the page number and name.
7. Under **Address mode for selected pages**, choose the User Hardware 1 offset as listed in the memory map in the *Byte Address Flash Memory Map* table in the *Appendix—CFI Flash Memory Map* section as 0x006E.0000.

Related Information

- Factory Default Switch and Jumper Settings on page 15
- CFI Flash Memory Map on page 47

A.2.2. quad SPI Flash Memory

A.2.2.1. Programming quad SPI Flash Using the Quartus Prime Programmer

Although the quad SPI flash is not programmed by factory default, you can program this device using `quartus_hps.exe` that resides in the `quartus/bin` directory.

1. To use this tool, open a command window and change directories to your 22.1std or later installation (for example, `c:\intelFPGA\22.1std\quartus\bin`).
2. To program an entire file to quad SPI flash starting at address 0, type the following command:

```
quartus_hps.exe -c <programming cable index> -o P <flash_boot_image.bin>
```

3. For a typical setup, where the Cyclone V SoC board is the only board connected to the PC, you can detect the quad SPI flash. To do so, run the following command:

```
quartus_hps.exe -o 1 -c1 <enter>
```

4. Using this tool requires that the board be placed into quad SPI boot mode. To do, set BOOTSEL1 (J29) shunt to the 1-2 position. The default position is 2-3 (SD card). You must power cycle the board after changing this jumper for the settings to take effect.
5. For help and more options, type the following command:

```
quartus_hps.exe --help
```

For more information, refer to the *SoC Board QSPI Boot* page on *RocketBoards.org*.

Related Information

SoC Board QSPI Boot, RocketBoard.org

A.2.3. SD Card Memory

A.2.3.1. Programming the SD Card Boot Image

The SD card is the default boot source for the HPS as selected by the BSEL jumpers. The socket is designed to accept microSD cards. The SoC development kit comes with a microSD card, micro-to-standard SD card adapter, and a USB programming adapter.

To program the SD card, perform the following steps:

1. Insert the SD card into the USB programming adapter and insert the programming adapter into a USB port on your PC.
2. In Windows, you should see a pop-up window asking what you would like to do with the flash device. Click **Cancel**, but note the drive letter it is mounted as.

   You cannot drag and drop files onto the SD card because the file system is different.
3. For Windows, use a disk imaging program such as Win32DiskImager.
4. For Linux, use the dd command. For example:

```
sudo dd if=<boot_image_filename.img> of=/dev/<sd_card_name> bs=<size>
```

   Attention: Be careful when using this programming command as it overwrites whatever that is found on the device pointed to in the of command.

For more information, refer to the *Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide* and *RocketBoards.org*.

Related Information

Intel SoC FPGA Embedded Development Suite (SoC EDS) User Guide

A.3. Power

Figure 21. Cyclone V SoC Development Kit (Power Solution 2) Power Tree

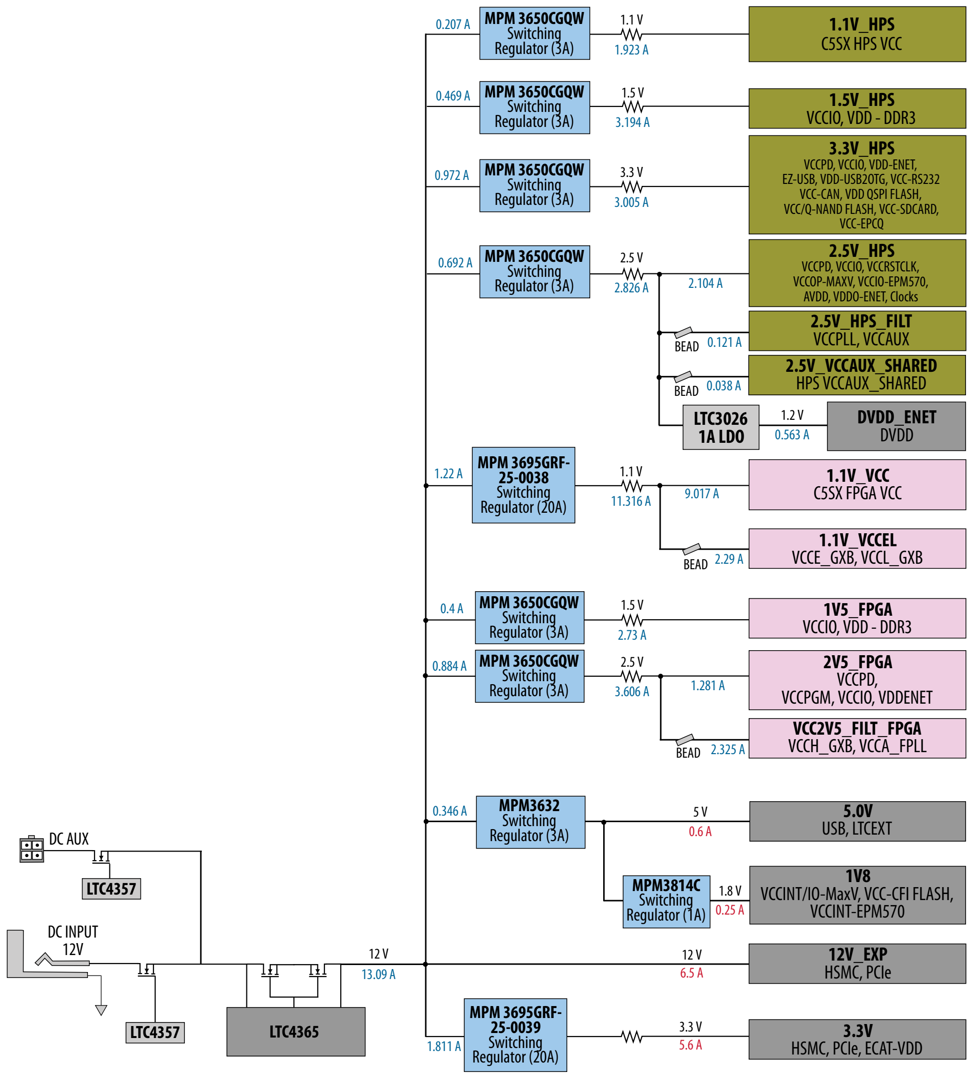
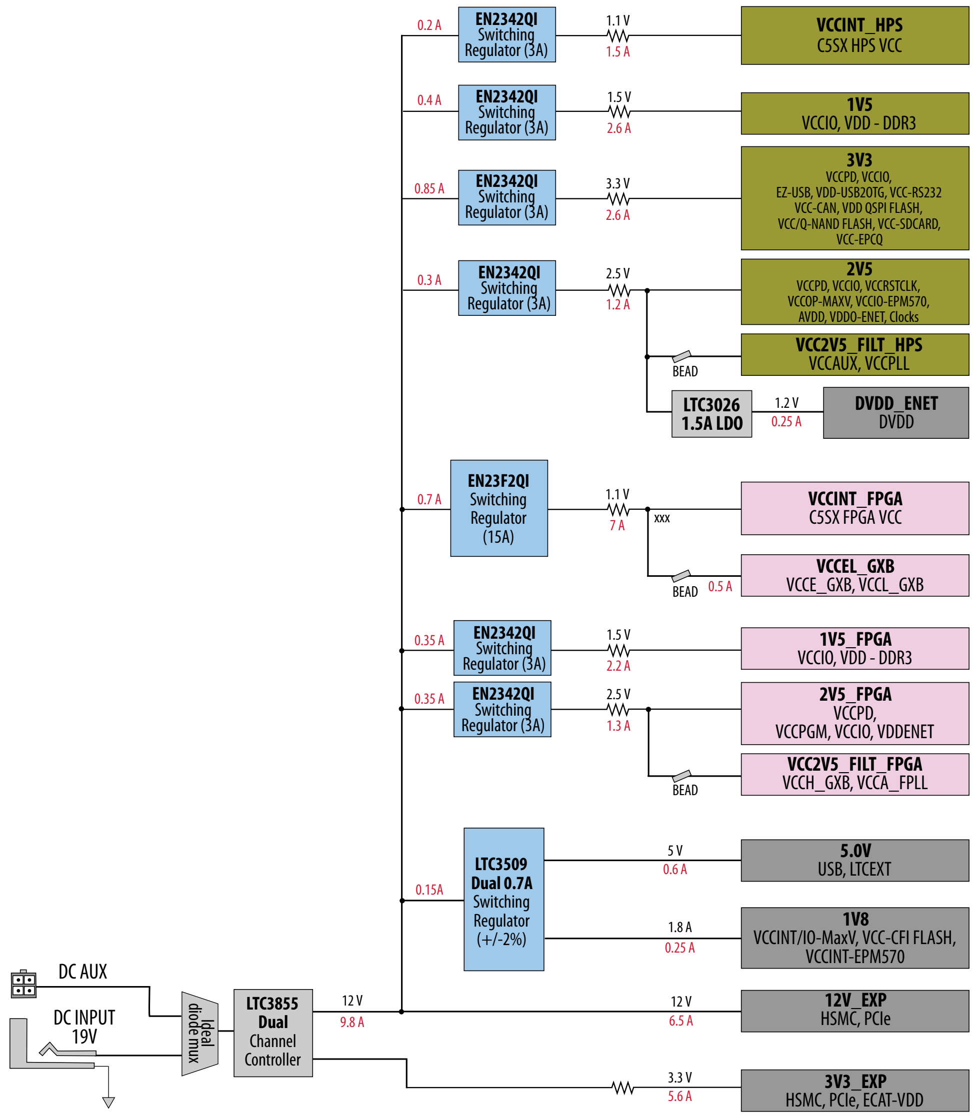


Figure 22. Cyclone V SoC Development Kit (Power Solution 1) Power Tree



B. Additional Information

B.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

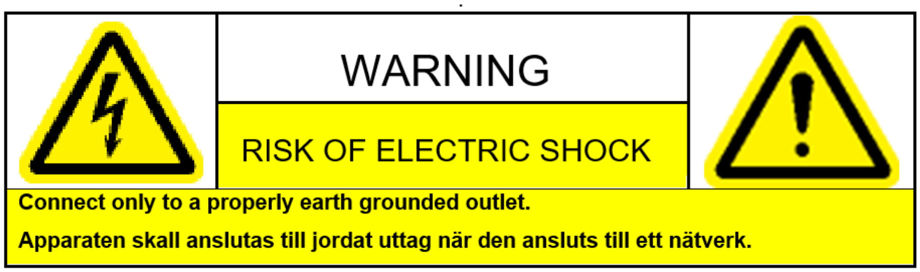
B.1.1. Safety Warnings

Power Supply Hazardous Voltage

AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

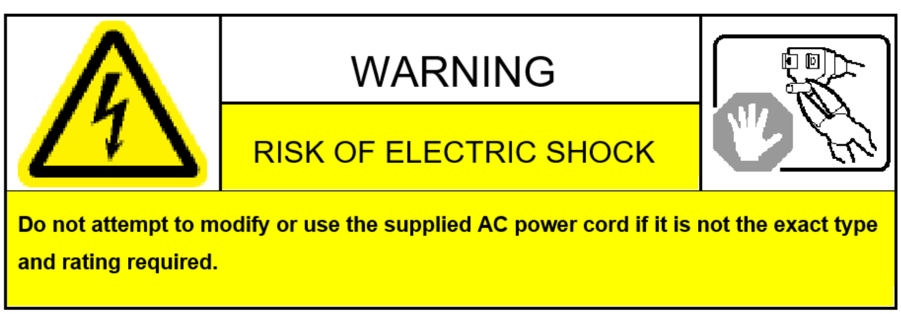
Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.



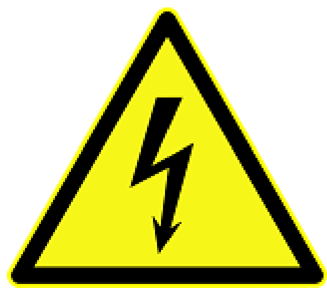
System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.



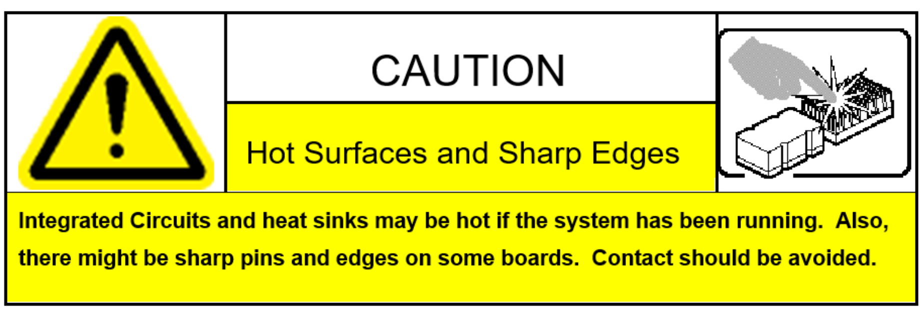
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

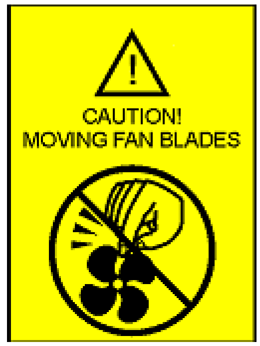
To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

B.1.2. Safety Cautions



Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.



Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

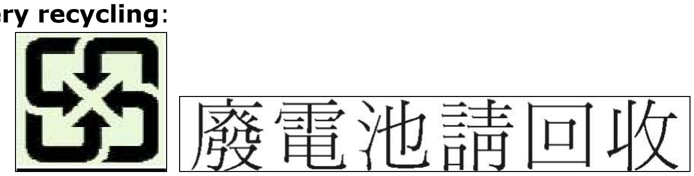
Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:



(Translation - please recycle batteries)

Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

B.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.