1. DESCRIPTION

XD40192 Presettable BCD Up/Down Counter Counter each consist of 4 synchronously clocked, gated “D” type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET}}$ $\overline{\text{ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the countdown mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

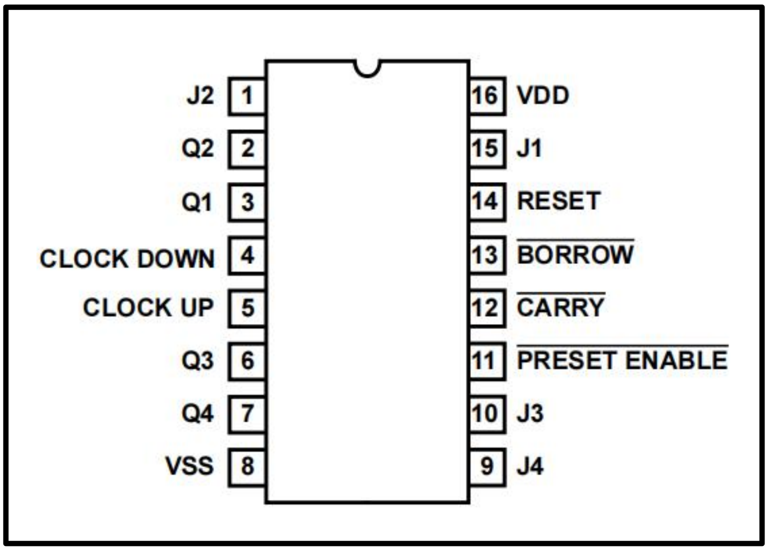
2. FEATURES

- High Voltage Type (20V Rating)
- Individual Clock Lines for Counting Up or Counting Down
- Synchronous High-Speed Carry and Borrow Propagation Delays for Cascading
- Asynchronous Reset and Preset Capability
- Medium Speed Operation - fCL = 8MHz (typ.) at 10V
- 5V, 10V and 15V Parametric Ratings
- Standardize Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Temperature Range)
  - 1V at VDD = 5V
  - 2V at VDD = 10V
  - 2.5V at VDD = 15V

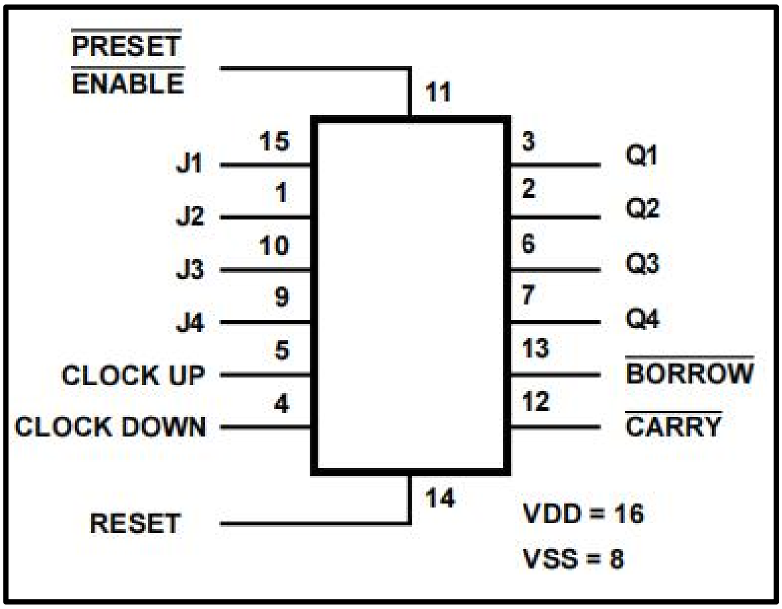
3. APPLICATIONS

- Up/Down Difference Counting
- Multistage Ripple Counting
- Synchronous Frequency Dividers
- A/D and D/A Conversion
- BCD Counting

4. PINOUT



5. FUNCTIONAL DIAGRAM



6. ABSOLUTE MAXIMUM RATINGS

- DC Supply Voltage Range, (VDD) . . . . -0.5V to +20V
- Input Voltage Range, All Inputs . . . .-0.5V to VDD +0.5V
- DC Input Current, Any One Input . . . .±10mA
- Operating Temperature Range. . . . . -40°C to +85°C
- Storage Temperature Range (TSTG) . . . . -65°C to +150°C
- Lead Temperature (During Soldering) . . . . +265°C

7. DC ELECTRICAL PERFORMANCE CHARACTERISTICS(TABLE 1)

(Ta = 25°C)

PARAMETER	SYMBOL	CONDITIONS(NOTE 1)	GROUP A SUBGROUPS	LIMITS		UNITS
				MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1	—	10	μA
Input Leakage Current	IIL	VIN = VDD or GND VDD = 20V	1	-100	—	nA
Input Leakage Curren	IIH	VIN = VDD or GND VDD = 20V	1	—	100	nA
Output Voltage	VOL 15	VDD = 15V, No Load	1	—	50	mV
Output Voltage	VOH 15	VDD = 15V, No Load (Note 3)	1	14.95	—	V
Output Current (Sink)	IOL 5	VDD = 5V, VOUT = 0.4V	1	0.53	—	mA
Output Current (Sink)	IOL 10	VDD = 10V, VOUT = 0.5V	1	1.4	—	mA
Output Current (Sink)	IOL 15	VDD = 15V, VOUT = 1.5V	1	3.5	—	mA
Output Current (Source)	IOH 5A	VDD = 5V, VOUT = 4.6V	1	—	-0.53	mA
Output Current (Source)	IOH 5B	VDD = 5V, VOUT = 2.5V	1	—	-1.8	mA
Output Current (Source)	IOH 10	VDD = 10V, VOUT = 9.5V	1	—	-1.4	mA
Output Current (Source)	IOH 15	VDD = 15V, VOUT = 13.5V	1	—	-3.5	mA
N Threshold Voltage	VNTH	VDD =10V,ISS =-10μA	1	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V,IDD =10μA	1	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND	7	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND	7			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1	—	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1	3.5	—	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V	1	—	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V ,VOL < 1.5V	1	11	—	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

8. AC ELECTRICAL PERFORMANCE CHARACTERISTICS(TABLE 2)

(Ta = 25°C)

PARAMETER	SYMBOL	CONDITIONS[NOTE 1]	GROUP A SUBGROUPS	LIMITS		UNITS
				MIN	MAX	
Propagation Delay Clock Up or Clock Down to Q	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	—	500	ns
Propagation Delay Reset to Q	TPHL2	VDD = 5V, VIN = VDD or GND	9	—	500	ns
Propagation Delay $\overline{\text{PE}}$ to Q	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	—	400	ns
Propagation Delay Clock Up to $\overline{\text{Carry}}$, Clock Down to $\overline{\text{Borrow}}$	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	—	320	ns
Propagation Delay $\overline{\text{PE}}$ to $\overline{\text{Borrow}}$or $\overline{\text{Carry}}$	TPHL5 TPLH5	VDD = 5V, VIN = VDD or GND	9	—	600	ns
Propagation Delay Reset to $\overline{\text{Borrow}}$ or $\overline{\text{Carry}}$	TPHL6 TPLH6	VDD = 5V, VIN = VDD or GND	9	—	600	ns
Transition Time	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	—	200	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	2	—	MHZ

NOTES: 1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

9. ELECTRICAL PERFORMANCE CHARACTERISTICS(TABLE 3)

PARAMETER	SYMBOL	CONDITIONS$^{\text{(NOTE 1)}}$	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1.2	+25°C	—	5	µA
		VDD = 10V, VIN = VDD or GND	1.2	+25°C	—	10	µA
		VDD = 15V, VIN = VDD or GND	1.2	+25°C	—	10	µA
Outout Voltage	VOL	VDD = 5V, No Load	1.2	+25°C	—	50	mV
Outout Voltage	VOL	VDD = 10V, No Load	1.2	+25°C	—	50	mV
Outout Voltage	VOH	DD = 5V, No Load	1.2	+25°C	4.95	—	V
Outout Voltage	VOH	VDD = 10V, No Load	1.2	+25°C	9.95	—	V
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1.2	+25°C	—	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1.2	+25°C	7	—	V
Propagation Delay Clock Up or Down to Q	TPHL1	VDD = 10V	1.2.3	+25°C	—	240	ns
	TPLH1	VDD = 15V	1.2.3	+25°C	—	180	ns
Propagation Delay Reset to Q	TPHL2	VDD = 10V	1.2.3	+25°C	—	240	ns
		VDD = 15V	1.2.3	+25°C	—	180	ns
Propagation Delay $\overline{\text{PE}}$ to Q	TPHL3	VDD = 10V	1.2.3	+25°C	—	200	ns
	TPLH3	VDD = 15V	1.2.3	+25°C	—	140	ns
Propagation Delay Clock Up to $\overline{\text{Carry}}$, Clock Down to $\overline{\text{Borrow}}$	TPHL4	VDD = 10V	1.2.3	+25°C	—	160	ns
	TPLH4	VDD = 15V	1.2.3	+25°C	—	120	ns
Propagation Delay $\overline{\text{PE}}$ to $\overline{\text{Borrow}}$ or $\overline{\text{Carry}}$	TPHL5	VDD = 10V	1.2.3	+25°C	—	300	ns
	TPLH5	VDD = 15V	1.2.3	+25°C	—	220	ns
Propagation Delay Reset to $\overline{\text{Borrow}}$ or $\overline{\text{Carry}}$	TPHL6	VDD = 10V	1.2.3	+25°C	—	300	ns
	TPLH6	VDD = 15V	1.2.3	+25°C	—	220	ns
Transition Time	TPHL1	VDD = 10V	1.2.3	+25°C	—	100	ns
	TPLH1	VDD = 15V	1.2.3	+25°C	—	80	ns
Maximum Clock Rise and Fall Time	TPCL	VDD = 5V	1.2.3.4	+25°C	—	15	µs
	TPCL	VDD = 10V	1.2.3.4	+25°C	—	15	µs
		VDD = 15V	1.2.3.4	+25°C	—	5	µs
Minimum Removal Time Reset or PE	TREM	VDD = 5V	1.2.3.5	+25°C	—	80	ns
		VDD = 10V	1.2.3.5	+25°C	—	40	ns
		VDD = 15V	1.2.3.5	+25°C	—	30	ns
Minimum Pulse Width Reset	TW	VDD = 5V	1.2.3	+25°C	—	480	ns
		VDD = 10V	1.2.3	+25°C	—	300	ns
		VDD = 15V	1.2.3	+25°C	—	260	ns
Minimum Pulse Width $\overline{\text{PE}}$	TW	VDD = 5V	1.2.3	+25°C	—	240	ns
		VDD = 10V	1.2.3	+25°C	—	170	ns
		VDD = 15V	1.2.3	+25°C	—	140	ns
Minimum Clock Pulse Width	TW	VDD = 5V	1.2.3	+25°C	—	180	ns
		VDD = 10V	1.2.3	+25°C	—	90	ns
		VDD = 15V	1.2.3	+25°C	—	60	ns
Input Capacitance	CIN	Reset	1.2	+25°C	—	15	pF
Input Capacitance	CIN	All Other Inputs	1.2	+25°C	—	7.5	pF

NOTES:

1.All voltages referenced to device GND.

2.The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.

3.CL = 50pF, RL = 200K, Input TR, TF < 20ns.

4.If more than one unit is cascaded, TRCL should be made less than or equal to the sumof the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

5.The time required for RESET or PRESET ENABLE control to be removed before clocking. See timing diagram defining TREM.

10. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS(TABLE 4)

PARAMETER	SYMBOL	CONDITIONS(NOTE 1)	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1.4	+25°C	—	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1.4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10μA	1.4	+25°C	—		V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10μA	1.4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10μA	1.4	+25°C	—		V
Functional	F	VDD = 18V, VIN = VDD or GND VDD = 3V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
Propagation Delay Time	TPHL TPLH	VDD = 5V	1.2.3.4	+25°C	—	1.35 x +25oC Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25oC limit.
4. Read and Record

11. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C(TABLE 5)

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	OOH5A	± 20% x Pre-Test Reading

12. APPLICABLE SUBGROUPS(TABLE 6)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1,7,9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1,7,9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1,7,9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1,7,9Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1,7,9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1,7,9Deltas	
Final Test		100% 5004	2,3,8A,8B,10,11	
Group A		Sample 5005	1,2,3,7,8A,8B,9,10,11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

13. TOTAL DOSE IRRADIATION(TABLE 7)

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	RE-IRRAD	POST-IRRA
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

14. BURN-IN AND IRRADIATION TEST CONNECTIONS(TABLE 8)

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
PART NUMBER XD40192						
Static Burn-In 1 (Note 1)	2,3,6,7,12,13	1, 4, 5, 8 - 11, 14, 15	16			
Static Burn-In 2 (Note 1)	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16			
Dynamic Burn In (Note 1)	—	8, 14	1, 5, 9 - 11, 15, 16	2, 3, 6, 7, 12, 13	4	—
Irradiation (Note 2)	2, 3, 6, 7, 12, 13	8	1, 4, 5, 9 - 11, 14 - 16			

NOTES: 1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V

2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

15. LOGIC DIAGRAMS

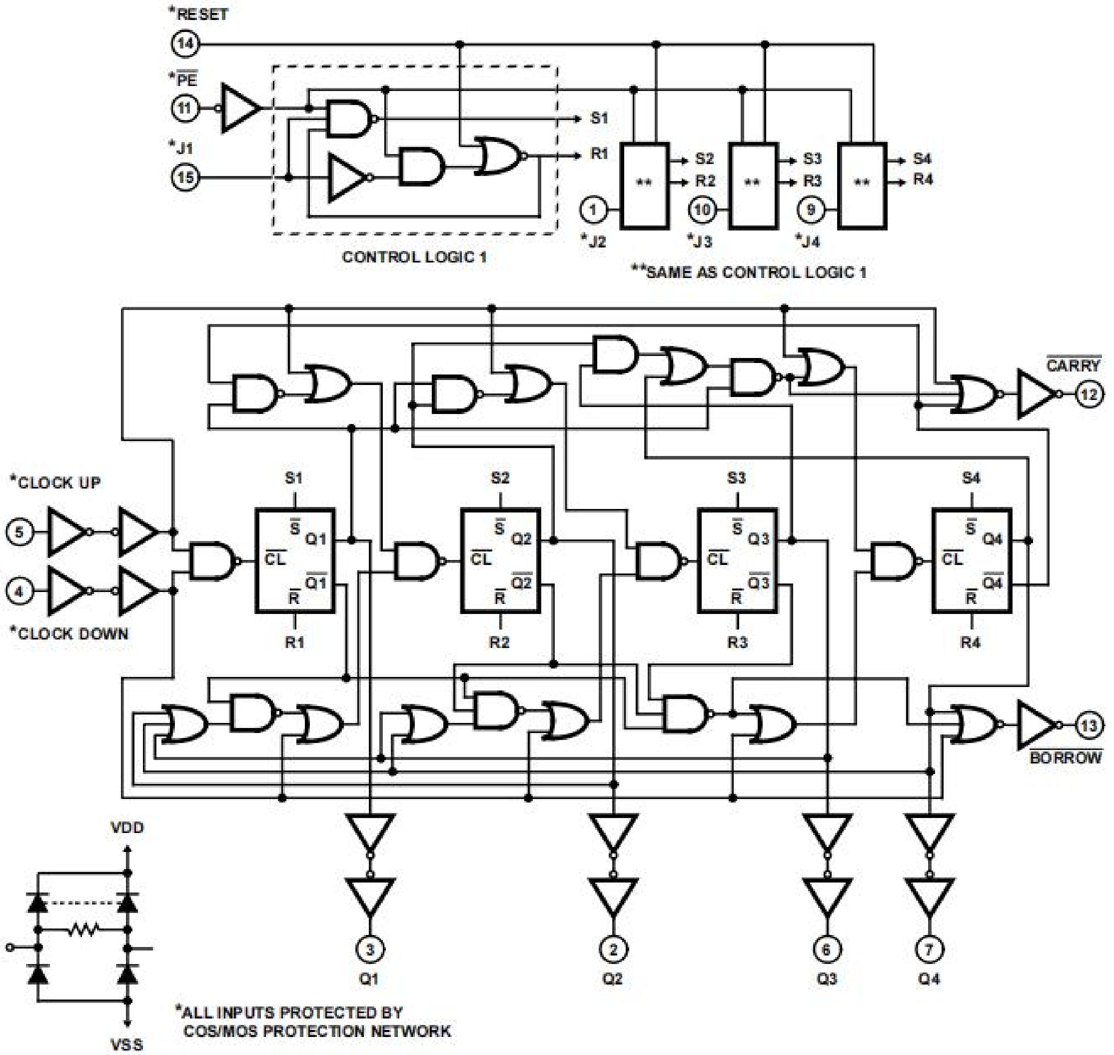


FIGURE 1. XD40192 LOGIC DIAGRAM

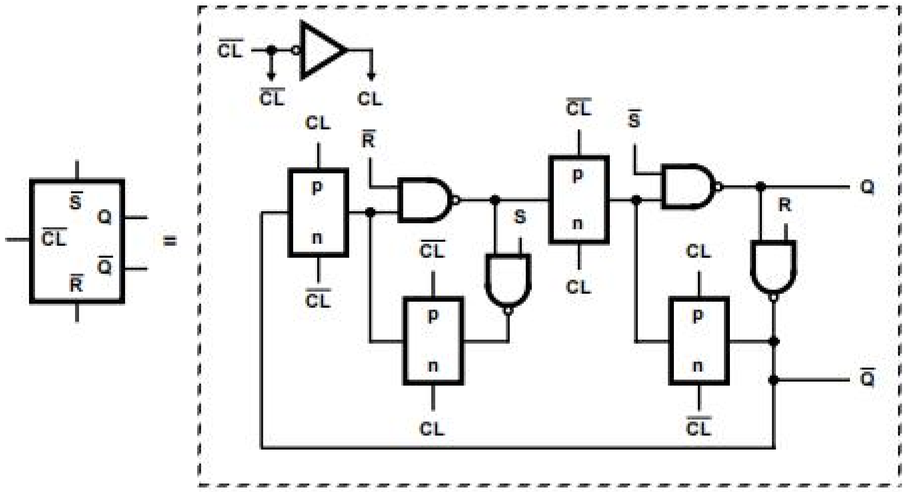


FIGURE 2. INTERNAL LOGIC OF FLIP-FLOP

TRUTH TABLE

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET ENABLE}}$	RESET	ACTION
_/‾	1	1	0	Count Up
‾_	1	1	0	No Count
1	_/‾	1	0	Count Down
1	‾_	1	0	No Count
X	X	0	0	Preset
X	X	X	1	Reset

1 = High Level 0 = Low Level X = Don't Care

16. TYPICAL PERFORMANCE CHARACTERISTICS

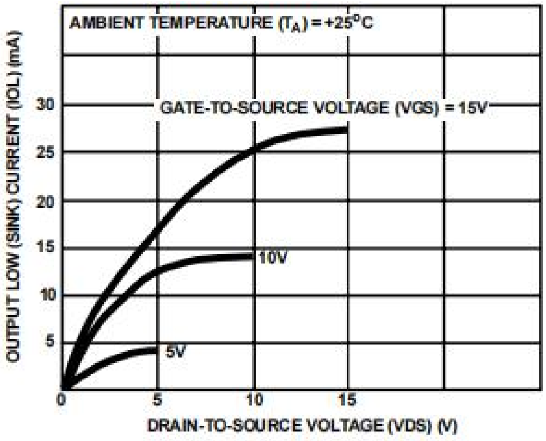


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

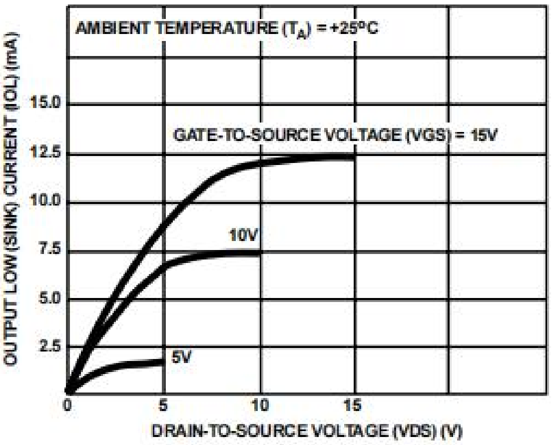


FIGURE 4. MIMIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

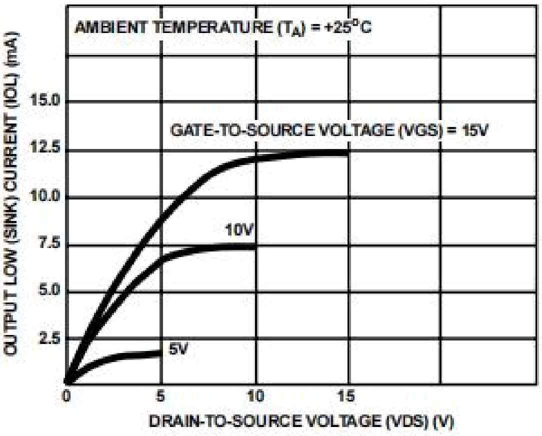


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

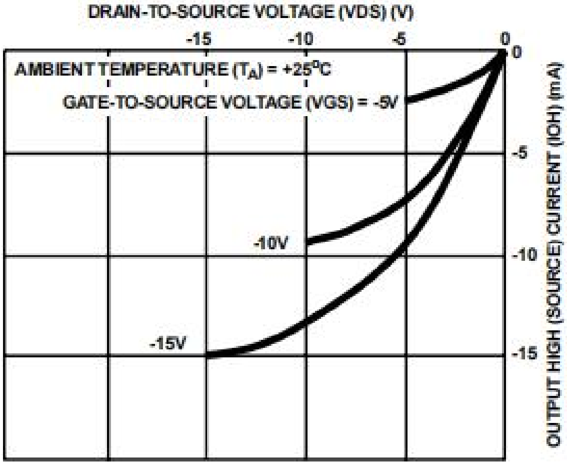


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

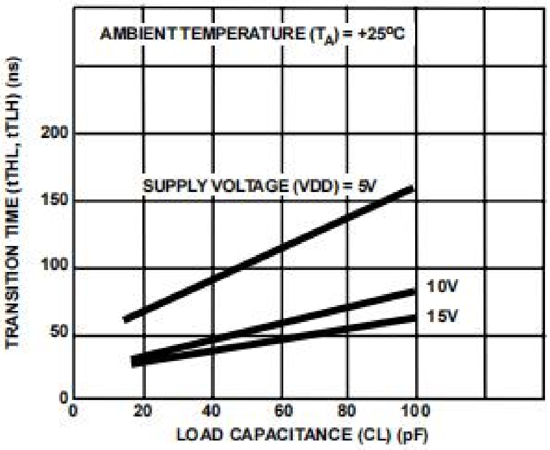


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

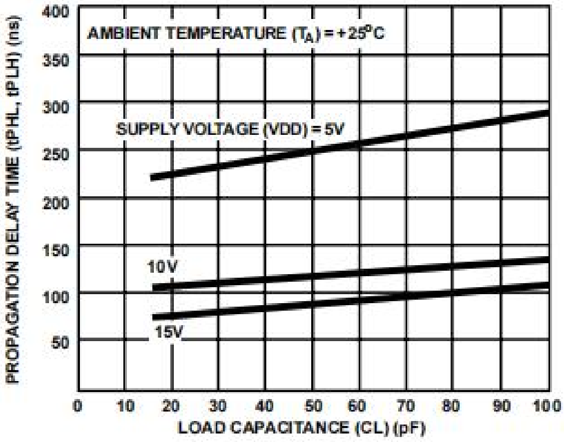


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

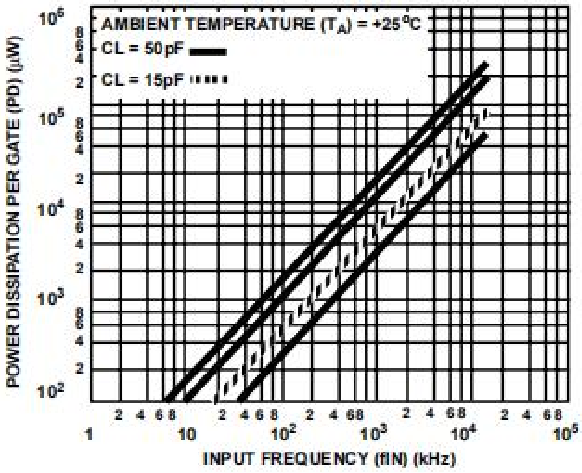


FIGURE 9. DYNAMIC POWER DISSIPATION

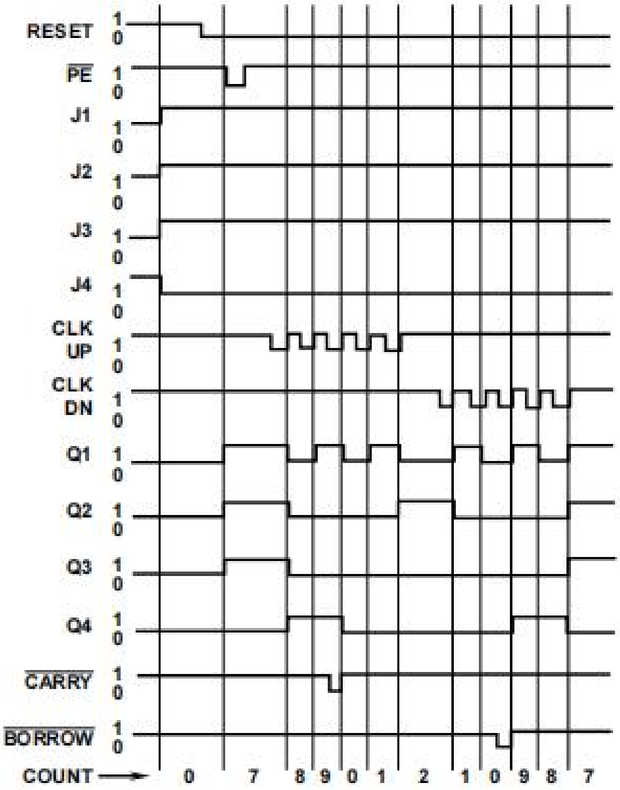


FIGURE 10. XD40192 TIMING DIAGRAM

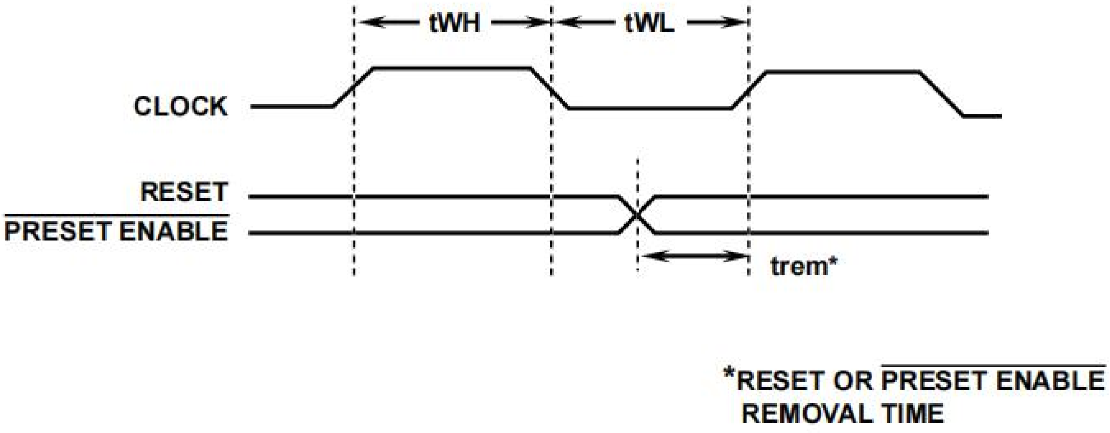


FIGURE 11. TIMING DIAGRAM DEFINING trem

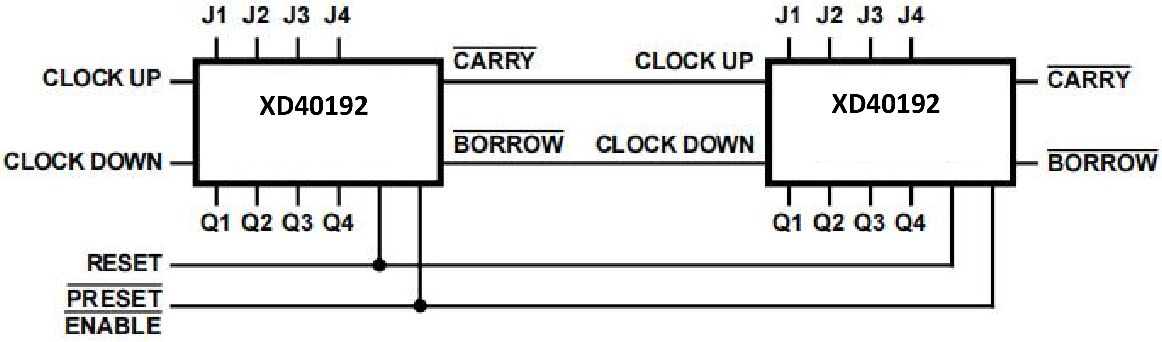


FIGURE 12. CASCADED COUNTER PACKAGES

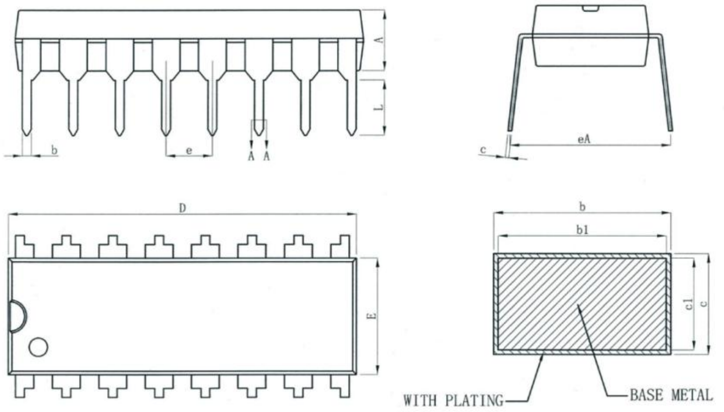
17. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (℃)	MSL	Transport Media	Package Quantity
XD40192	XD40192	DIP16	19.05*6.35	- 40 to 85	MSL3	Tube25	1000

18. DIMENSIONAL DRAWINGS

DIP16



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---