36 V, 4-/8-Channel, Fault-Protected Analog Multiplexers

Features

- Fault and Overvoltage Protection: ±50 V power on, ±30 V power off
- Latch-Up Proof Construction for all pins
- Break-Before-Make Construction
- Fast Switching Time: t_{ON} 166 nS； t_{OFF} 135 nS
- Low On Resistance: 270 Ω
- Off Leakage Current: 10 pA
- Charge Injection: 14.8 pC
- TTL and CMOS-Compatible Inputs
- Supply Voltage: ±5 V to ±18 V
- Specified Temperature Range: -40 °C to 125 °C

Applications

- Analog Input/Output Module
- Industrial and Process Control Systems
- Instruments
- ATE
- Communication Systems
- Relay Replacement

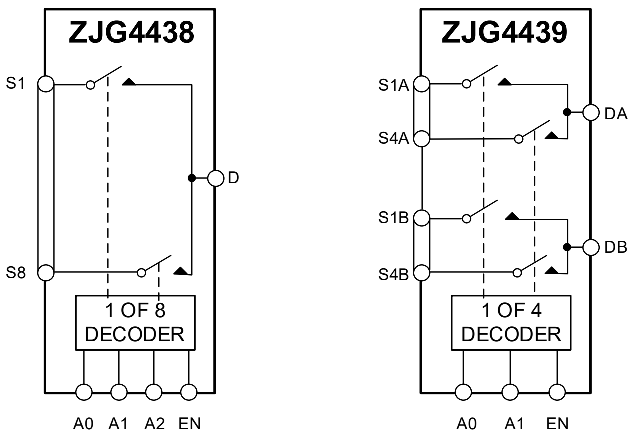
General Description

The ZJG4438 and ZJG4439 are analog multiplexers, with the ZJG4438 comprising eight single channels and the ZJG4439 comprising four differential channels. These multiplexers provide fault protection. Using optimized design, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from -50 V to +50 V. During fault conditions with power supplies off, the multiplexer input (or output) appears as an open circuit and only 2 nA of leakage current flows. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The ZJG4438 switches one of eight inputs to a common output as determined by the 3-bit binary address lines, A0, A1, and A2. The ZJG4439 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines, A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched off.

ZJG4438/ZJG4439 are available in SOIC-16 and TSSOP-16 packages and are pin compatible with industry standards.

Functional Block Diagram



Typical Application

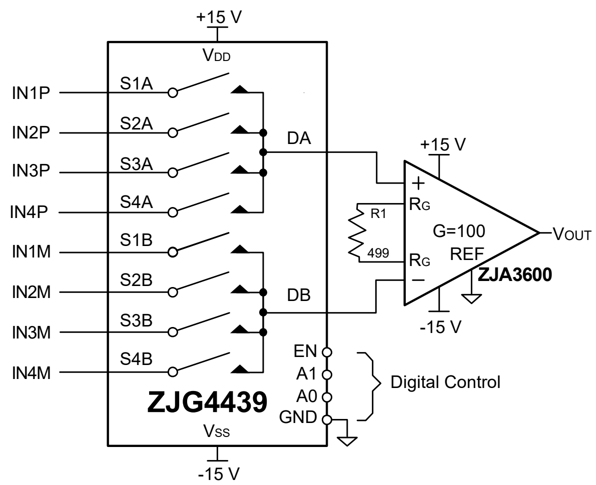


Table of Contents

Revision History (Release B) [1]

Jan. 2025 — Release B

English Version

Added TSSOP-16 Pin Configuration, Terminology and Test Circuits

Updated Specifications, Ordering Guide, Product Order Model and Related Parts

Apr. 2024

Added -40 °C < T_A < 85 °C specifications

Sep. 2023 — Release A

Mar. 2023 — Initial

Pin Configuration and Function Description

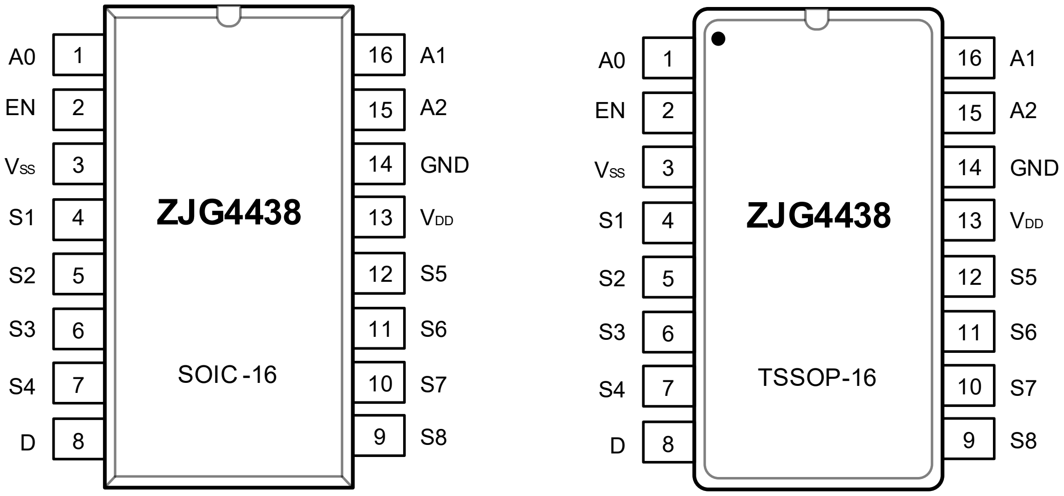


Figure 1. ZJG4438 Pin Configuration (SOIC-16 & TSSOP-16)

Mnemonic	Pin No.	Description
A0	1	Logic Control Input LSB.
EN	2	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
V_{SS}	3	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
S1	4	Source Terminal 1. This pin can be an input or an output.
S2	5	Source Terminal 2. This pin can be an input or an output.
S3	6	Source Terminal 3. This pin can be an input or an output.
S4	7	Source Terminal 4. This pin can be an input or an output.
D	8	Drain Terminal. This pin can be an input or an output.
S8	9	Source Terminal 8. This pin can be an input or an output.
S7	10	Source Terminal 7. This pin can be an input or an output.
S6	11	Source Terminal 6. This pin can be an input or an output.
S5	12	Source Terminal 5. This pin can be an input or an output.
V_{DD}	13	Most Positive Power Supply Potential.
GND	14	Ground (0 V) Reference.
A2	15	Logic Control Input MSB.
A1	16	Logic Control Input.

ZJG4438 Truth Table

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

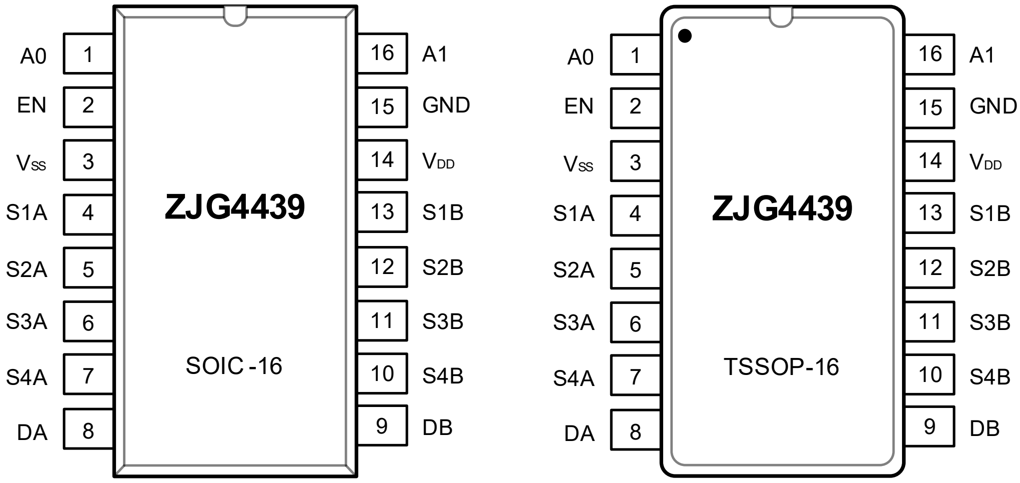


Figure 2. ZJG4439 Pin Configuration (SOIC-16 & TSSOP-16)

Mnemonic	Pin No.	Description
A0	1	Logic Control Input LSB.
EN	2	Active High Digital Input. When low, the device is disabled, and all switches are off. When high, Ax logic inputs determine on switches.
V_{SS}	3	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
S1A	4	Source Terminal 1A. This pin can be an input or an output.
S2A	5	Source Terminal 2A. This pin can be an input or an output.
S3A	6	Source Terminal 3A. This pin can be an input or an output.
S4A	7	Source Terminal 4A. This pin can be an input or an output.
DA	8	Drain Terminal A. This pin can be an input or an output.
DB	9	Drain Terminal B. This pin can be an input or an output.
S4B	10	Source Terminal 4B. This pin can be an input or an output.
S3B	11	Source Terminal 3B. This pin can be an input or an output.
S2B	12	Source Terminal 2B. This pin can be an input or an output.
S1B	13	Source Terminal 1B. This pin can be an input or an output.
V_{DD}	14	Most Positive Power Supply Potential.
GND	15	Ground (0 V) Reference.
A1	16	Logic Control Input MSB.

ZJG4439 Truth Table

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	40 V
Input Voltage	-50 V to +50 V
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	40 mA
Operating Temperature Range	-40 °C to 125 °C
Storage Temperature Range	-65 °C to 150 °C
Junction Temperature	-65 °C to 150 °C
Maximum Reflow Temperature [2]	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
Electrostatic Discharge (ESD) [3]	
Human Body Model (HBM) [4]	2 kV
Charged Device Model (CDM) [5]	1 kV

Thermal Resistance [6]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-16	94	23.5	°C/W
TSSOP-16	104	60	°C/W

1 These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2 IPC/JEDEC J-STD-020 Compliant.
3 Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
4 ANSI/ESDA/JEDEC JS-001 Compliant.
5 ANSI/ESDA/JEDEC JS-002 Compliant.
6 θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at V_{DD} = 15 V ± 10%, V_{SS} = -15 V ± 10%, GND = 0 V, T_A = 25 °C.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
ANALOG SWITCH							
Analog Signal High		Output open circuit			V_{DD} - 1.4		V
Analog Signal Low					V_{SS} + 1.4		V
Analog Signal High		Output loaded, 1 mA			V_{DD} - 2.2		V
Analog Signal Low					V_{SS} + 2.2		V
On Resistance	R_{ON}	-10 V ≤ V_S ≤ +10 V, I_S = 1 mA, V_{DD} = 15 V, V_{SS} = -15 V			270	320	Ω
			●			530	Ω
		-40 °C < T_A < 85 °C				430	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	-10 V ≤ V_S ≤ +10 V, I_S = 1 mA, V_{DD} = 15 V, V_{SS} = -15 V			5	7	%
			●			10	%
		-40 °C < T_A < 85 °C				10	%
On-Resistance Match Between Channels	ΔR_{ON}	V_S = ±10 V, I_S = 1 mA	●		0.5	3	%
LEAKAGE CURRENTS							
Source Off Leakage	I_S (Off)	V_S = ±10 V, V_D = ∓10 V		-0.5	±0.01	+0.5	nA
			●	-4		+4	nA
		-40 °C < T_A < 85 °C		-1		1	nA
Drain Off Leakage	I_D (Off)	V_S = ±10 V, V_D = ∓10 V		-0.5	±0.01	+0.5	nA
			●	-0.2		+0.2	μA
		-40 °C < T_A < 85 °C		-4		4	nA
Channel On Leakage	I_D,I_S(ON)	V_S = V_D = ±10 V		-0.5	±0.01	+0.5	nA
			●	-0.2		+0.2	μA
		-40 °C < T_A < 85 °C		-4		4	nA
FAULT							
Source Leakage Current	I_S (Fault)	V_S = +50 V or -50 V, V_D = 0 V		-2	±0.02	+2	nA
			●	-0.25		+0.25	μA
		-40 °C < T_A < 85 °C		-25		25	nA
Drain Leakage Current	I_D (Fault)	V_S = ±25 V, V_D = ∓10 V		-1	±0.01	+1	nA
			●	-0.2		+0.2	μA
		-40 °C < T_A < 85 °C		-10		10	nA
Source Leakage Current (Power Supply Off)	I_S (Fault)	V_S = ±30 V, V_{DD} = V_{SS} = V_D = V_{EN}, A0, A1, A2 = 0 V		-10	±0.1	+10	nA
			●	-0.25		+0.25	μA
		-40 °C < T_A < 85 °C		-25		25	nA

DIGITAL INPUTS

Input High Voltage	V_{INH}		•	2.4			V
Input Low Voltage	V_{INL}		•			0.8	V
Input Current	I_{INL}/I_{INH}	V_{EN} = 0 V or V_{DD}	•			1	μA

DYNAMIC CHARACTERISTICS [1]

$t_{TRANSITION}$		R_L = 1 MΩ, C_L = 35 pF, V_{S1} = ±10 V, V_{S8} = ±10 V			168		ns
			•			320	ns
t_{OPEN}		R_L = 1 KΩ, C_L = 35 pF, V_S = 5 V			139		ns
			•	50			ns
t_{ON}		R_L = 1 kΩ, C_L = 35 pF, V_S = 5 V			166		ns
			•			330	ns
t_{OFF}		R_L = 1 kΩ, C_L = 35 pF, V_S = 5 V			135		ns
			•			170	ns
Settling Time		t_{SETT} 0.1%, R_L = 1 kΩ, C_L = 35 pF, V_S = 5 V			0.25		μs
Charge Injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF			14.8		pC
Off Isolation		R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz, V_S = 7 Vrms			-93		dB
Channel-to-Channel Crosstalk		R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz, V_S = 7 Vrms			-104		dB
C_S (Off)					2.6		pF
C_D (Off)		ZJG4438			5.8		pF
		ZJG4439			3.2		pF

POWER SUPPLY

I_{DD_ON}, I_{SS_ON}		V_{DD} = 15 V, V_{SS} = -15 V, V_{EN} = 2.4 V			0.07	0.15	mA
			•			0.2	mA
I_{DD_OFF}, I_{SS_OFF}		V_{DD} = 15 V, V_{SS} = -15 V, V_{EN} = 0.8 V			0.05	0.15	mA
			•			0.2	mA
Power Supply Range				±5		±18	V

TEMPERATURE RANGE

Specified				-40		125	ºC

[1] Guaranteed by design, not subject to production test.

Typical Performance Characteristics

Unless otherwise stated, V_{DD} = 15 V, V_{SS} = -15 V, GND = 0 V, T_A = 25 °C.

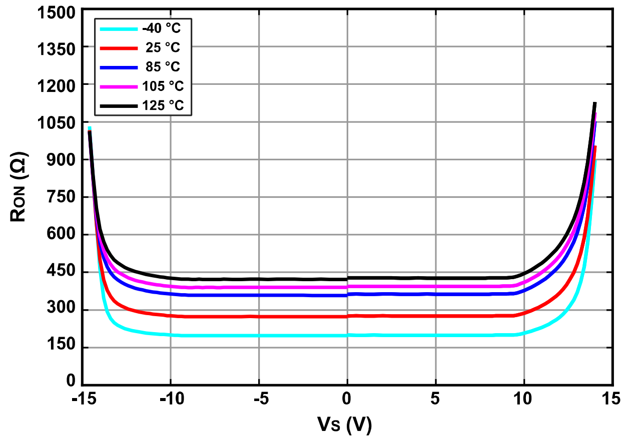


Figure 3. On Resistance as a Function of V_D (V_S)

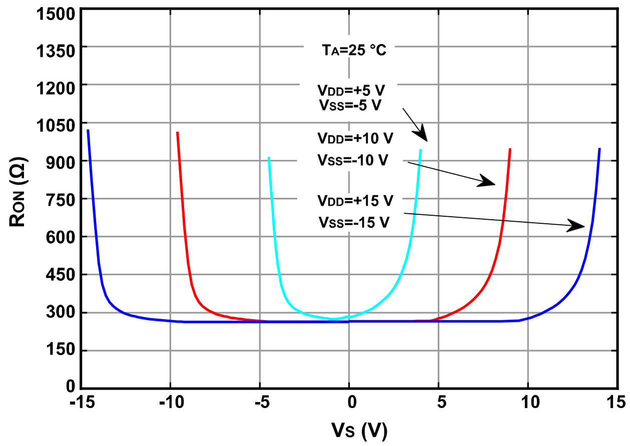


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures

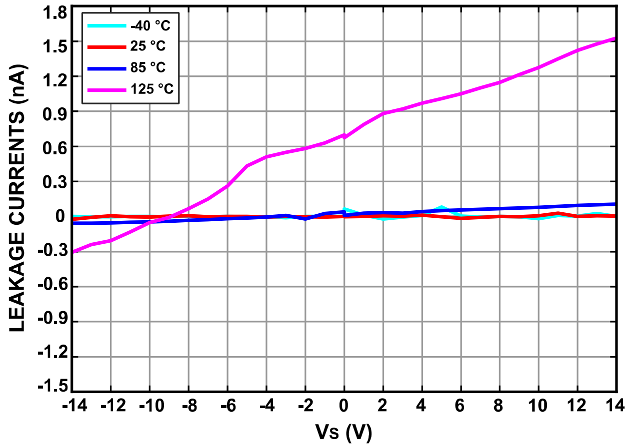


Figure 5. Source Input Leakage Current as a Function of V_S for Different Temperatures (Power Supplies On)

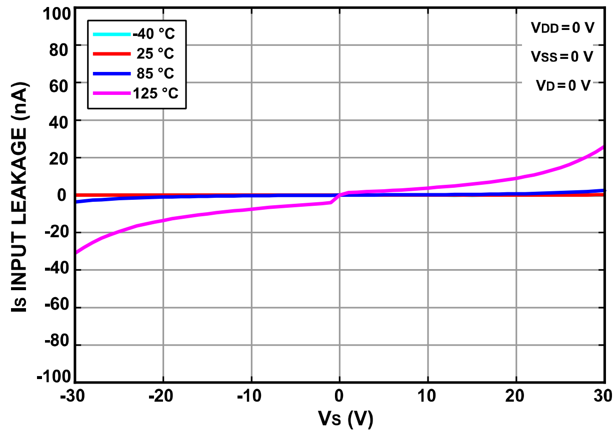


Figure 6. Source Input Leakage Current as a Function of V_S for Different Temperatures (Power Supplies Off)

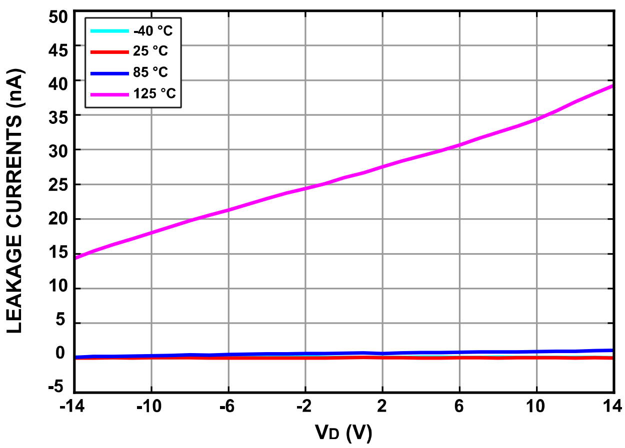


Figure 7. Leakage Current I_D (on) as a Function of V_D for Different Temperatures

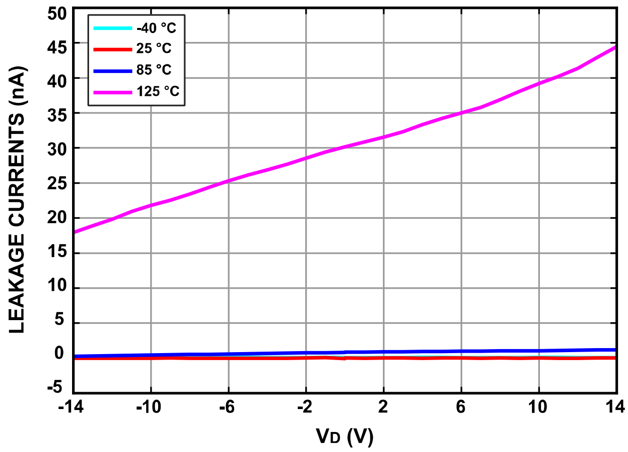


Figure 8. Leakage Current I_D (off) as a Function of V_D for Different Temperatures

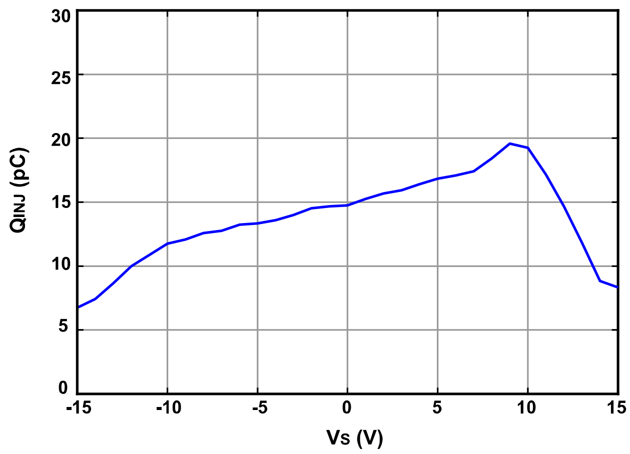


Figure 9. Charge Injection vs. Source Voltage

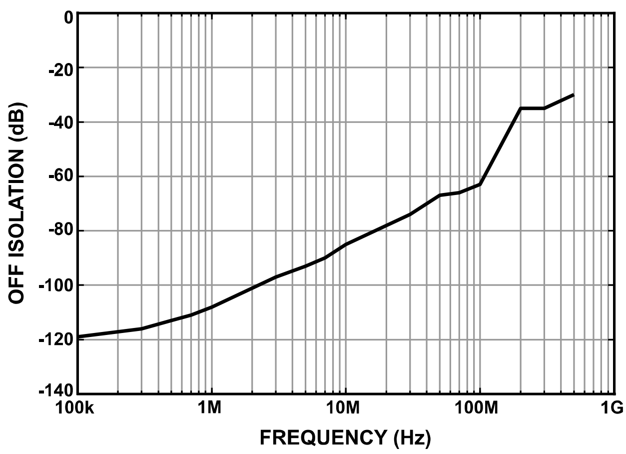


Figure 10. Off Isolation vs. Frequency

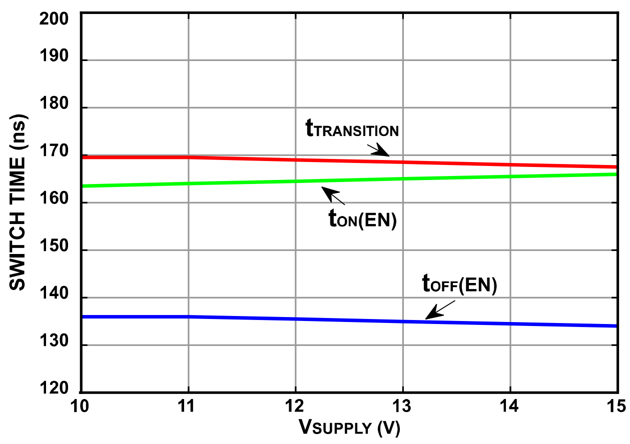


Figure 11. Switching Time vs. Dual Power Supply

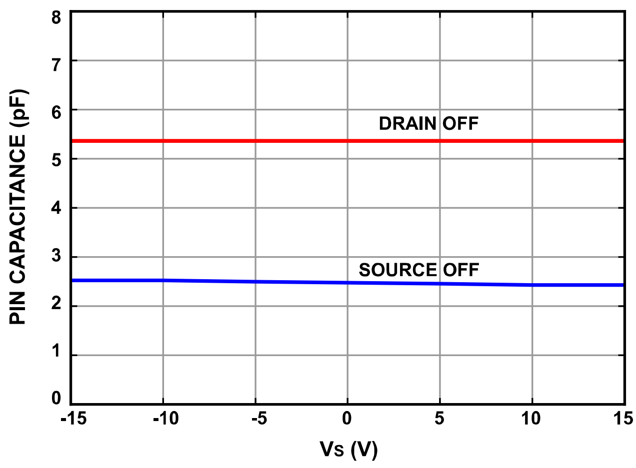


Figure 12. Capacitance vs. Source Voltage

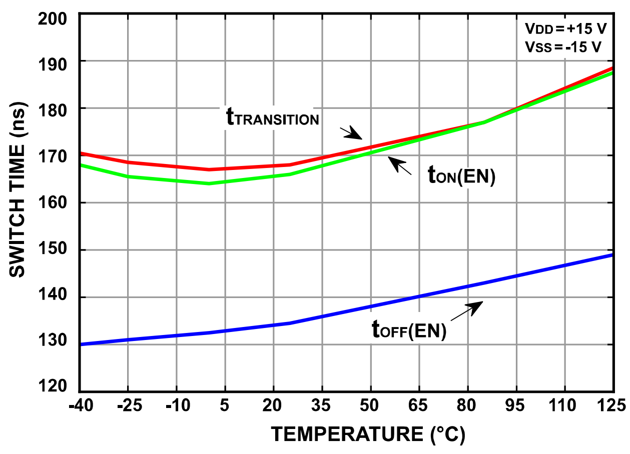


Figure 13. Switching Time vs. Temperature

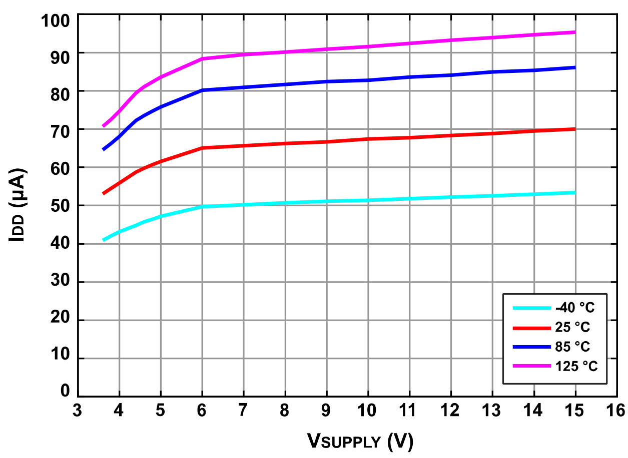


Figure 14. Supply Current vs Supply Voltage for Different Temperatures (EN = 1)

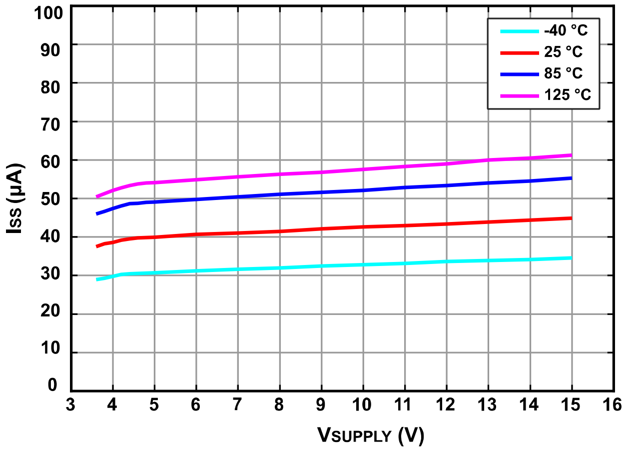


Figure 15. Supply Current vs Supply Voltage for Different Temperatures (EN = 0)

Terminology

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply potential.

GND
Ground (0 V) reference.

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels as a percentage of the maximum R_{ON} of those two channels.

$R_{FLAT\ (ON)}$
Flatness is defined as the difference between the maximum and minimum value of the on resistance measured over the specified analog signal range and is represented by $R_{FLAT\ (ON)}$.

Flatness is calculated by

$$\left((R_{MAX} - R_{MIN})/R_{MAX} \times 100\right)$$

R_{ON} Drift
Change in R_{ON} when temperature changes by one degree Celsius.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

I_S (Fault—Power Supplies On)
Source leakage current when exposed to an overvoltage condition.

I_D (Fault—Power Supplies On)
Drain leakage current when exposed to an overvoltage condition.

I_S (Fault—Power Supplies Off)
Source leakage current with power supplies off.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{OPEN}
Off time measured between 80% points of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Test Circuits

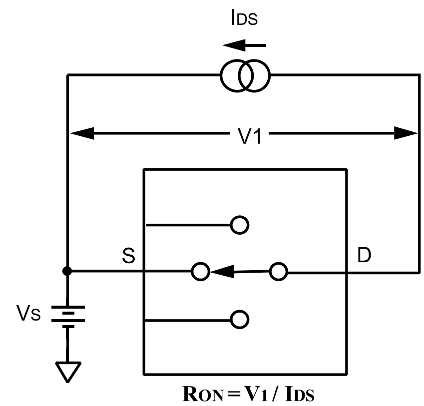


Figure 16. On Resistance

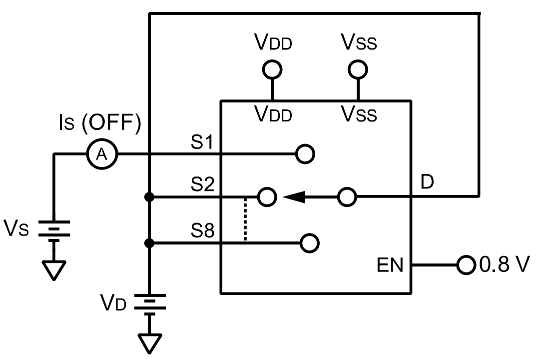


Figure 17. IS (Off)

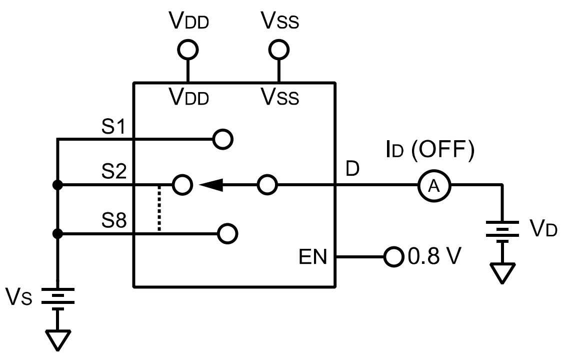


Figure 18. ID (Off)

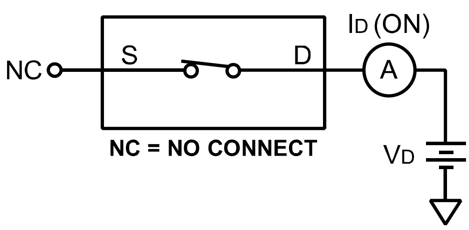


Figure 19. ID (On)

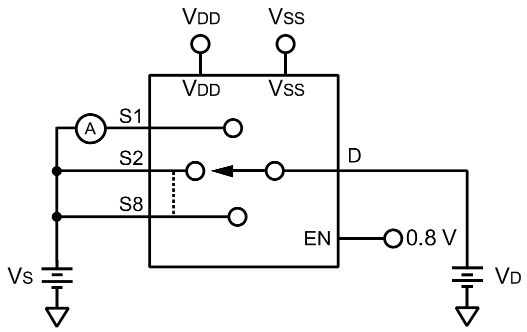


Figure 20. Input Leakage Current (with Overvoltage)

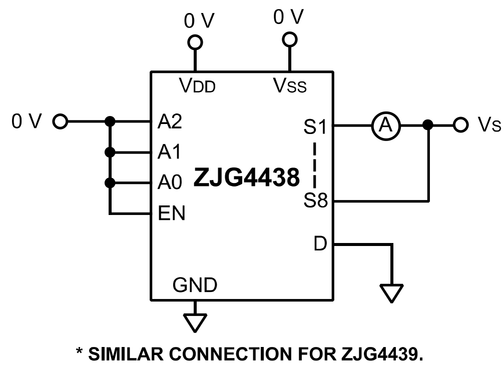


Figure 21. Input Leakage Current (with Power Supplies Off)

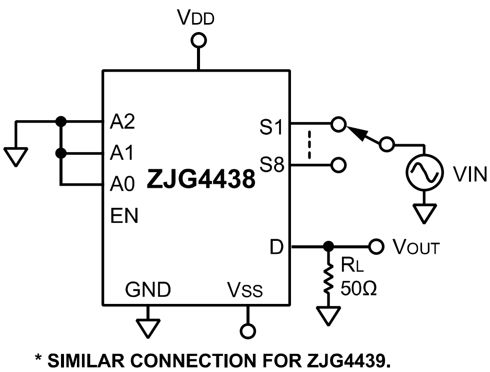
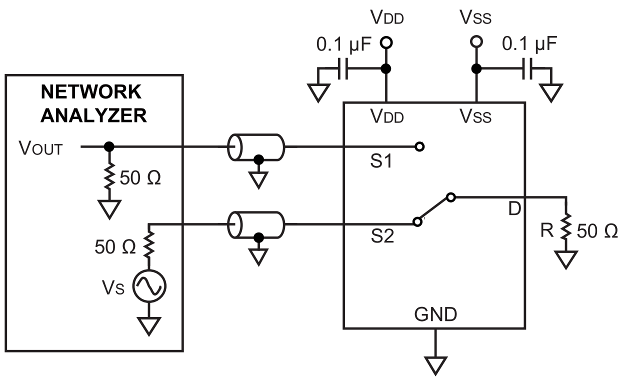


Figure 22. Off Isolation



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 23. Channel-to-Channel Crosstalk

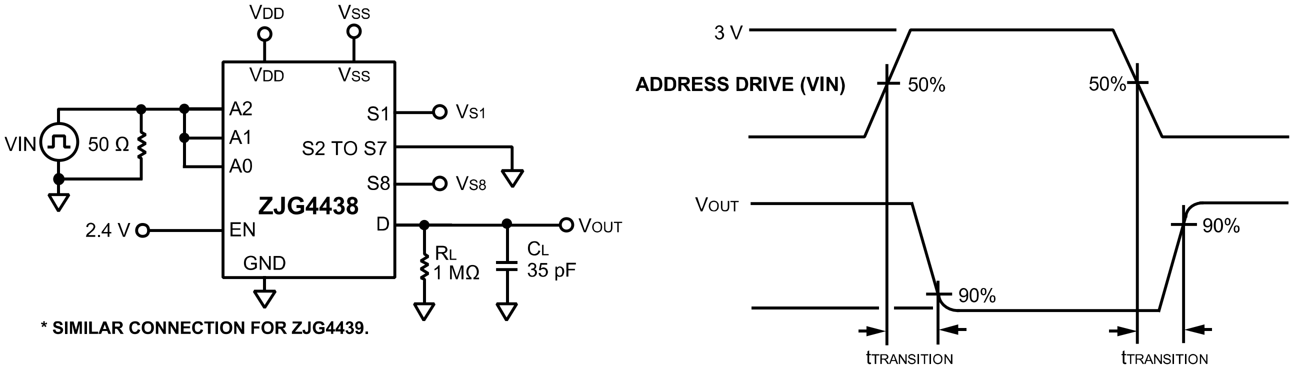


Figure 24. Switching Time of Multiplexer, $t_{TRANSITION}$

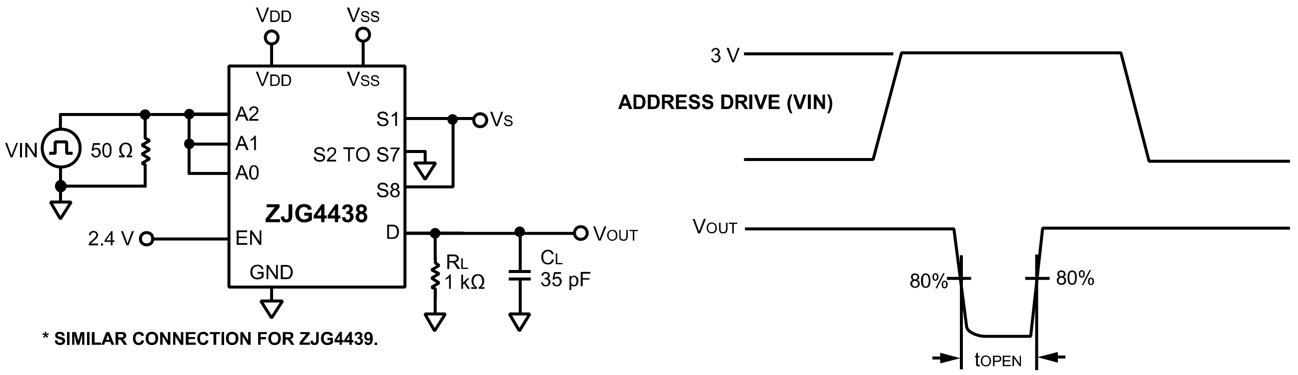


Figure 25. Break-Before-Make Delay, t_{OPEN}

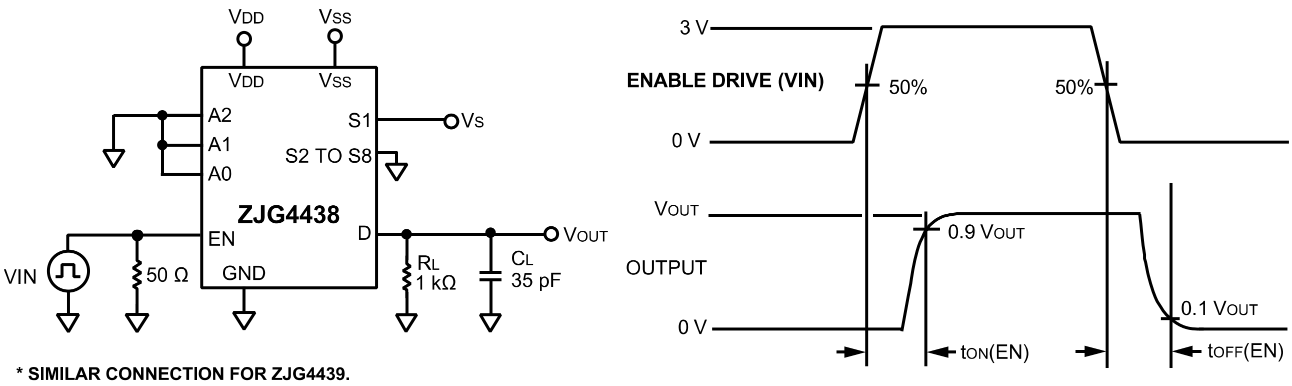


Figure 26. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

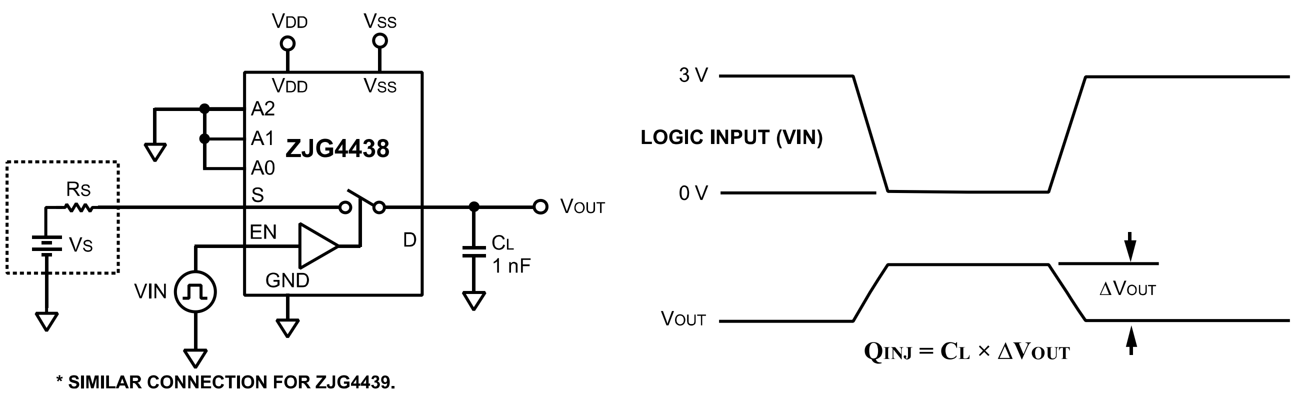


Figure 27. Charge Injection

Theory of Operation

The ZJG4438/ZJG4439 multiplexers are capable of withstanding overvoltages from -50 V to +50 V, irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an N-channel MOSFET, a P-channel MOSFET, and an N-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs saturates, limiting the current. The current during a fault condition is determined by the load on the output. The architecture enables these multiplexers to withstand continuous overvoltages.

When an analog input of (V_{SS}) + 2.2 V to (V_{DD}) – 2.2 V (output loaded, 1 mA) is applied to the ZJG4438/ZJG4439, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is 270 Ω typically. However, when an overvoltage is applied to the device, one of the three MOSFETs saturates.

Figure 28 to Figure 31 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an on channel approaches the positive power supply line, the N-channel MOSFET saturates because the voltage on the analog input exceeds the difference between V_{DD} and the N-channel threshold voltage (V_{TN}). When a voltage more negative than V_{SS} is applied to the multiplexer, the P-channel MOSFET saturates because the analog input is more negative than the difference between V_{SS} and the P-channel threshold voltage (V_{TP}). Because V_{TN} is nominally 1.4 V and (V_{TP}) − 1.4 V, the analog input range to the multiplexer is limited to (V_{SS}) + 1.4 V to (V_{DD}) − 1.4 V (output open circuit) when a ±15 V power supply is used.

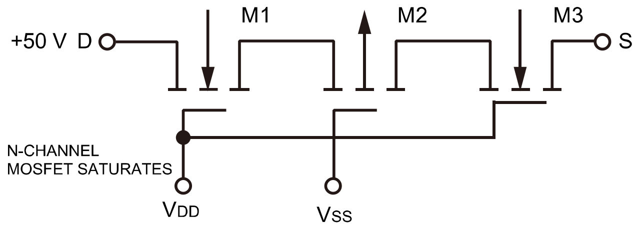


Figure 28. +50 V Overvoltage Input to the On Channel

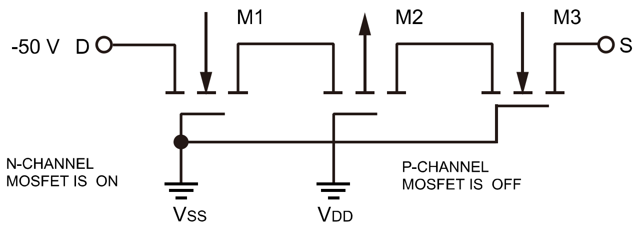


Figure 29. -50 V Overvoltage on an Off Channel with Multiplexer Power On

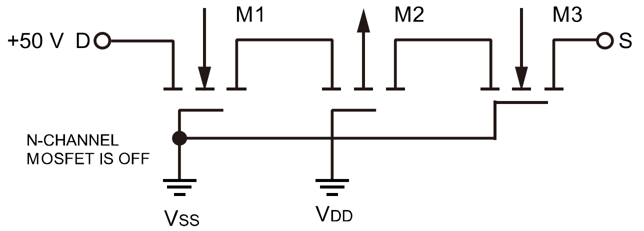


Figure 30. +50 V Overvoltage with Power Off

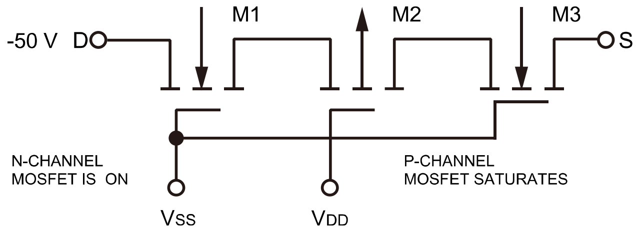


Figure 31. -50 V Overvoltage with Power Off

When the power supplies are present, but the channel is off, again either the P-channel MOSFET M2 or one of the N-channel MOSFET M1 remains off when an overvoltage occurs.

When the power supplies are off, the gate of each MOSFET is at ground. A negative overvoltage switches on the N-channel MOSFET M1, but the bias produced by the overvoltage causes the P-channel MOSFET M2 to remain turned off. With a positive overvoltage, the MOSFET M1 in the series remains off because the gate to source voltage applied to this MOSFET is negative.

During fault conditions (power supplies off), the leakage current into and out of the ZJG4438/ZJG4439 is limited to 10 nA. This limit protects both the multiplexer and subsequent circuitry from overstress as well as protects the signal sources that drive the multiplexer. Furthermore, the other channels of the multiplexer remain unaffected by the overvoltage and continue to operate normally.

Applications Information

High-voltage multiplexers are frequently used at the very front of a system's external interface, demanding high performance and exceptional safety and reliability. To protect expensive electronic devices, system designers demand that the multiplexer withstand fault signals significantly exceeding the supply voltages. Moreover, given the unpredictable power-on sequence of the system and external signals, the multiplexers must withstand these fault signals irrespective of their power-on or power-off state. Multiplexers incorporating over-voltage protection significantly streamline system design, resulting in smaller, more cost-effective, and more robust systems with shorter development cycles.

When ZJG4438 and ZJG4439 are powered off, the switch is automatically in the off state. In this state, the inputs can withstand voltages ranging from -30 V to +30 V with only nA-level leakage current. When powered by ±15 V and in the off state, the input voltage tolerance increases to -50 V to +50 V, while maintaining nanoampere-level input leakage current and the output remains clamped within the power rails.

As illustrated in Figure 32 and Figure 33, under identical fault conditions where the input voltage exceeds the power rail, ZJG4438 and ZJG4439 exhibit both lower leakage current and higher input voltage tolerance compared to competing parts, regardless of power state. This superior performance effectively protects systems from potential damage.

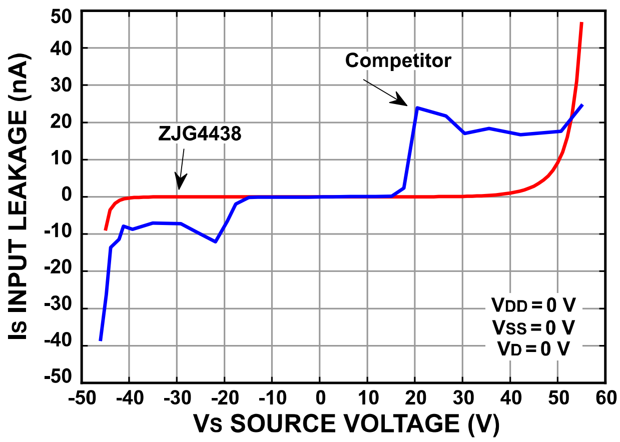


Figure 32. ZJG4438 Leakage Current I_S (Power off)

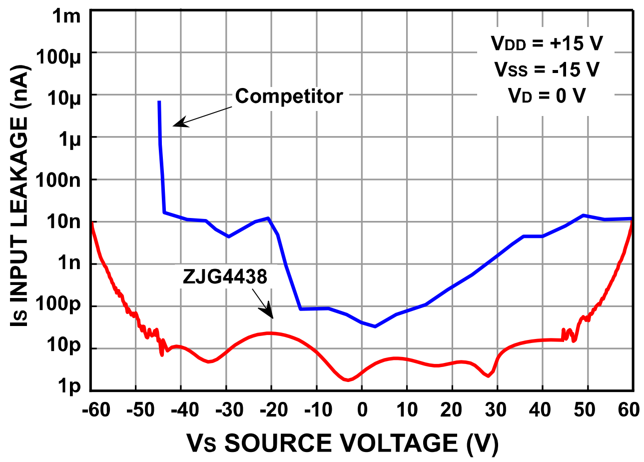


Figure 33. ZJG4438 Leakage Current I_S (Power on, switch off)

A latch-up happens at the system's front end can lead to severe consequences, often requires a full system reset or causes hardware damage. ZJG4438 and ZJG4439 mitigate this risk by ensuring that all pins—including input, output, and logic control pins—are inherently latch-up free. This key feature simplifies system design and maintenance while enhancing overall system reliability.

On-resistance (Ron) is a key parameter for analog switches and multiplexers. ZJG4438 and ZJG4439 offer a typical Ron of 270 Ω. Unlike many high-voltage analog switches and multiplexers, where Ron can significantly increase as the signal approaches the power rails, ZJG4438 and ZJG4439 exhibit superior Ron flatness over a wider voltage range, as shown in Figure 34. This characteristic makes them ideal for high-precision data acquisition systems requiring 16-bit or greater accuracy.

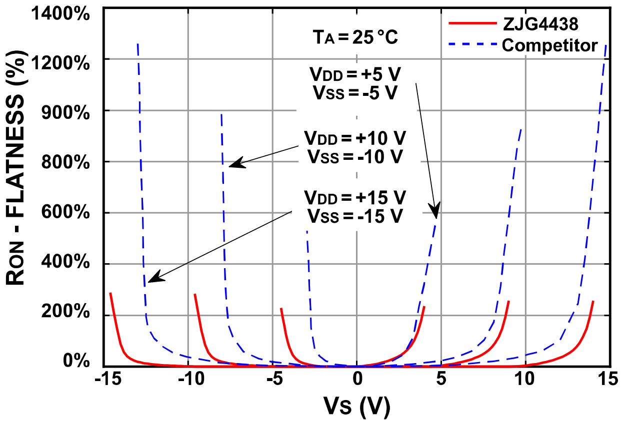


Figure 34. ZJG4438 On Resistance vs. Input Voltage

Leakage current when the switch is on is a critical DC specification for analog switches and multiplexers, as it decides system accuracy. Higher leakage current leads to increased measurement error, making the device less suitable for precision data acquisition systems. ZJG4438 and ZJG4439 exhibit excellent leakage current characteristics, as illustrated in Figure 35. When powered by ±15 V with a ±10 V input, they achieve a leakage current of 10 pA at room temperature. Over the temperature range of -40 °C to 85 °C, the leakage current remains below 4 nA, and even at -40 °C to 125 °C, it stays within 200 nA. These low leakage currents make them ideal for 14-bit or greater data acquisition systems.

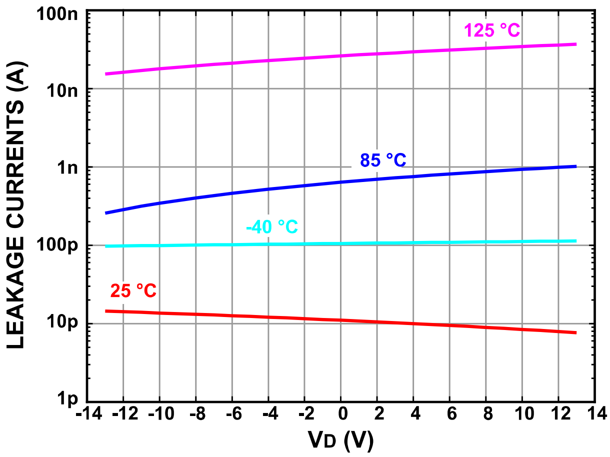


Figure 35. ZJG4438 Leakage Current when Turned On

Charge injection, which occurs during switching, can interfere with input signals and degrade system linearity. As shown in Figure 36, ZJG4438 exhibits a lower charge injection of 14.8 pC and maintains superior flatness across the entire input range compared to competing parts.

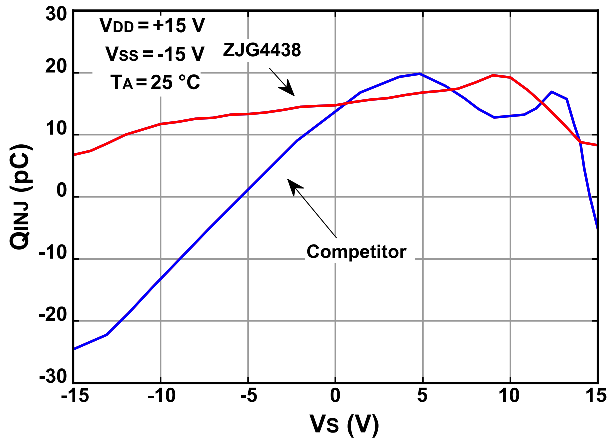


Figure 36. ZJG4438 Charge Injection vs. Source Voltage V_S

ZJG4438 and ZJG4439 offer fast switching times of 166 ns t_{ON} and 135 ns t_{OFF}. They are in break-before-make construction and the crosstalk between channels is just 104 dB. In the off state, they exhibit low input capacitance C_S of 2.6 pF and output capacitance C_D of 5.8 pF for ZJG4438 and 3.2 pF for ZJG4439. Their CMOS and TTL-compatible parallel interfaces simplify integration and ease of use.

Outline Dimensions

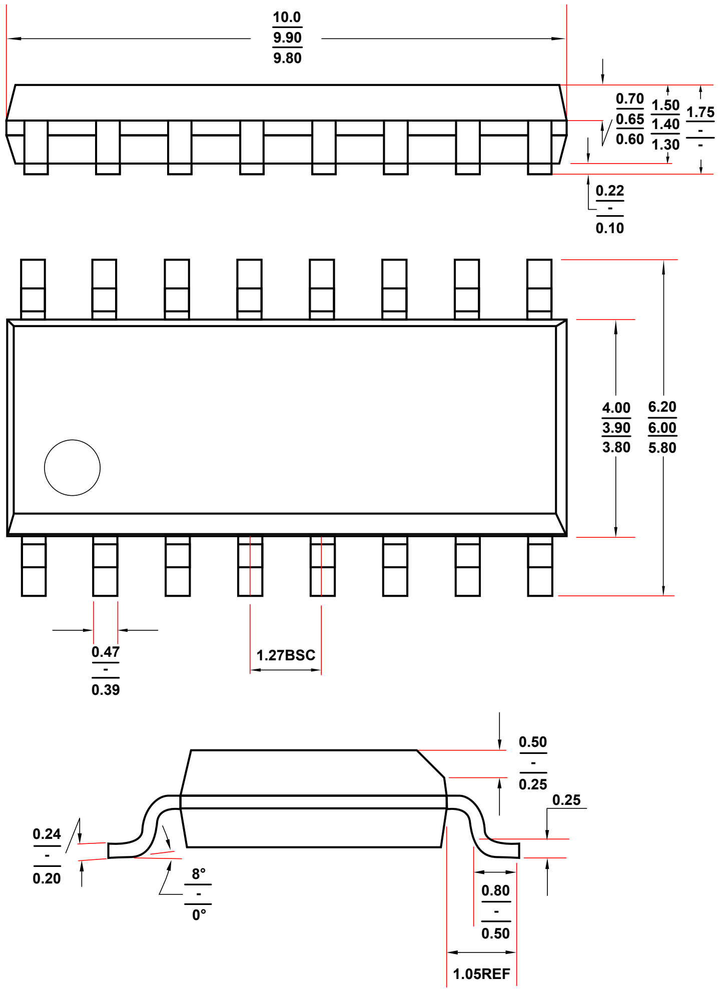


Figure 37. 16-Lead SOIC Package Dimensions Shown in Millimeters

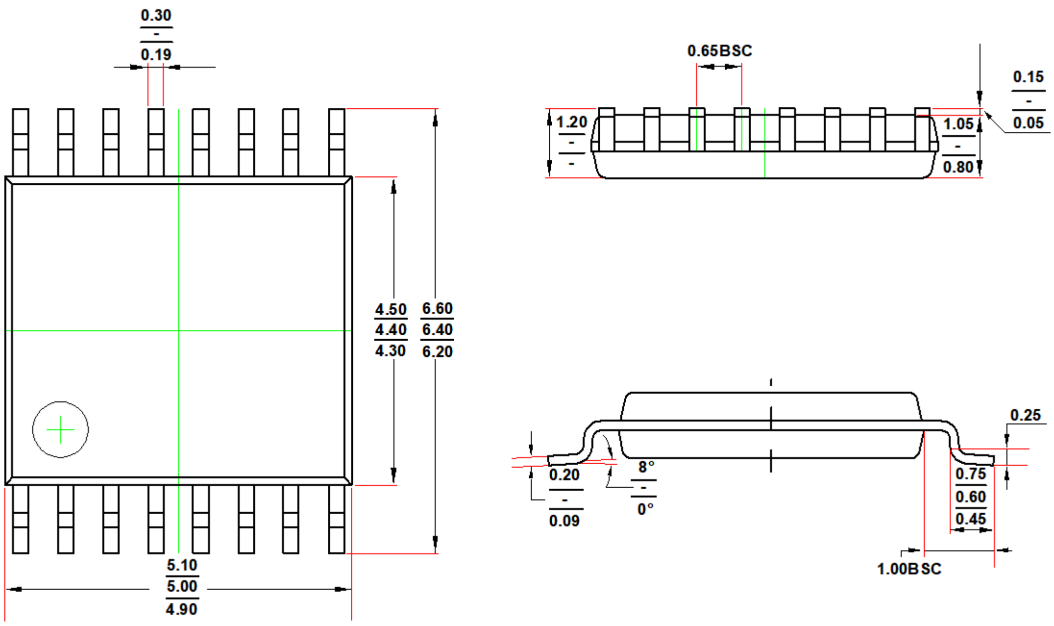


Figure 38. 16-Lead TSSOP Package Dimensions Shown in Millimeters

Ordering Guide

Model	Orderable Device	Function	Temperature Range (°C)	Package	External Package
ZJG4438	ZJG4438ASEBT	8:1 Multiplexer	-40 to +125	SOIC-16	Tube
	ZJG4438ASEBR			SOIC-16	13" Reel
	ZJG4438AUEBT			TSSOP-16	Tube
	ZJG4438AUEBR			TSSOP-16	13" Reel
ZJG4439	ZJG4439ASEBT	4:1 Differential Multiplexer	-40 to +125	SOIC-16	Tube
	ZJG4439ASEBR			SOIC-16	13" Reel
	ZJG4439AUEBT			TSSOP-16	Tube
	ZJG4439AUEBR			TSSOP-16	13" Reel

Product Order Model

ZJXXXXX X X X X X Q1

Q1: Automotive Grade
External package: T=Tube; R=Reel
Temperature range: A= -40°C to 125°C Automotive Grade 1; B= -40°C to 125°C; E= -40°C to 85°C
Number of pins: R=3; K=5; T=6, A=8; B=10; D=14; E=16; P=20
Package type: S=SOIC; U=MSOP, TSSOP, SOT (3 to 6 pins); T=DFN, QFN; K=SOT (8 pins)
Grade: B grade is better than A grade
Base: R=Voltage reference; A=Amplifier; C=Data Converter; G=Switches and Multiplexers, M=Others

Related Parts

Part Number	Description	Comments
ADC		
ZJC2020	20-bit 350 kSPS SAR ADC	Fully differential input, SINAD 101.4 dB, THD -118 dB
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2009	Small size, 12-bit 1 MSPS SAR ADC	Single-ended input, SOT23-6, 2.3 V to 5 V, SINAD 73 dB, THD -89 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8, MSOP-10/8, DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14, TSSOP-16, QFN-16 packages
Amplifier		
ZJA3000-1/2/4 ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz, 35 μV max Vos, 0.5 μV/°C max TCVos, 25 pA max Ibias, 1 mA/ch, input to V- (ZJA3000 only), RRO, 4.5 V to 36 V
ZJA3018-2 ZJA3008-2	OVP ±75 V, 36 V, Low Power, High Precision Op Amp 36 V, Low Power, High Precision Op Amp	1.3 MHz, 10 μV max Vos, 0.5 μV/°C max TCVos, 25 pA max Ibias, 0.5 mA/ch, OVP ±75 V (ZJA3018 only), RRO, 4.5 V to 36 V
ZJA3512-2	Dual 36 V 7 MHz precision JFET Op Amps	7 MHz, 35 V/μS, 50 μV max Vos, 1 μV/°C max TCVos, 2 mA/ch, RRO, 9 V to 36 V
ZJA3206/06/02-1/2	Precision 24/11.6/5.3 MHz CMOS RRIO Op Amps	24/11.6/5.3 MHz, RRIO, 30 μV max Vos, 1 μV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ib, 25 μV max Vosi, ±2.4 V to ±18 V, -40 °C to 125 °C
ZJA3611, ZJA3609	36 V precision wider bandwidth precision in-amp (G ≥ 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 μV max Vosi, 1.2 MHz BW (G = 10)
ZJA3676/7 ZJA3678/9	Low power, G = 1 Single/Dual 36 V difference amplifier Low power, G = 0.5/2 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min (G = 1), Vos 100 μV max, gain error 15 ppm max, 500 kHz BW (G = 1), 330 μA/channel, 2.7 V to 36 V
ZJA3669	High Common-Mode Voltage Difference Amplifier	±270 V CMV, 2.5 kV ESD, 96 dB min CMRR, 450 kHz BW, 4 V to 36 V, SOIC-8
ZJA3100	15 V precision fully differential amplifier	145 MHz, 447 V/μS, 50 nS to 16-bit, 50 μV max Vos, 4.6 mA Iq, SOIC/MSOP-8, QFN-16
ZJA3236/26/22-2	Low-cost 22/10/5 MHz CMOS RRIO Op Amps	22/11/5 MHz, RRIO, 2 mV max Vos, 6 μV/°C max TCVos, 0.6 pA Ib, 2.7 V to 5.5 V
ZJA3622/8	36 V low-cost precision in-amp	0.5 nA max Ibias, 125 μV max Vosi, 625 kHz BW (G = 10), 3.3 mA Iq, ±2.4 V to ±18 V
Voltage Reference		
ZJR1004	40 V supply precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096/5/10 V, 5 ppm/°C max drift -40 °C to 125 °C
ZJR1001/2 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.048/2.5/3/3.3/4.096/5 V, 5 ppm/°C max drift -40 °C to 125 °C, ±0.05% initial error, 130 μA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MSOP-8
ZJR1302	5.5 V low power compact precision voltage reference	V_{OUT} = 2.048/2.5/3/3.3/4.096 V, 30 ppm/°C max drift -40 °C to 125 °C, 130 μA, SOT23-3
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω, 14.8 pC, t_{ON} 166 nS
ZJG4428/4429	36 V 8:1/dual 4:1 multiplexer	Latch-up immune, Ron 270 Ω, 14.8 pC charge injection, t_{ON} 166 nS
Quad Matching Resistor		
ZJM5400	±75 V precision match resistors	Mismatch < 100 ppm, 10k:10k:10k:10k, 100k:100k:100k:100k, 100k:10k:10k:100k, 1k:1k:1k:1k, 1M:1M:1M:1M, 5k:1k:1k:5k, 5k:1.25k:1.25k:5k, 9k:1k:1k:9k, ESD: 3.5 kV

