PCI11414

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip PCI11414. These checklist items should be followed when utilizing the PCI11414 in a new design. A summary of these items is provided in Section 14.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power and Bypass Capacitance"
- Section 4.0, "PCIe Signals"
- Section 5.0, "USB Signals"
- Section 6.0, "Ethernet"
- Section 7.0, "UART"
- Section 8.0, "I^2C/SPI Controllers"
- Section 9.0, "GPIOs"
- Section 10.0, "Clock Circuit"
- Section 11.0, "Power and Startup"
- Section 12.0, "Configuration"
- Section 13.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The PCI11414 implementor should have the following documents on hand:

- *PCI11414 Data Sheet*
- *AN4754 Using Microchip Bridge Controllers with External Ethernet PHYs*
- *AN4255 PCI12000/PCI11xxx Register Map*
- *AN5213 Configuration and Programming Options for the PCI1XXXX*

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground flag, **GND**, must be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

3.0 POWER AND BYPASS CAPACITANCE

3.1 1.1V Supplies

- The analog supplies (**VDD11**) are located on pins 28, 67, 102, 135, and 147 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1 µF and one 0.1 µF shared bulk capacitance placed nearby the device IC.
- The PCIe upstream port 1.1V supplies for Lanes 0-1 (**VDD11PA**) are located on pins 14, 18, 19, 21, and 25 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. (Only one capacitor is necessary for pins that are adjacent and directly shorted together.) All pins should share one 1 µF and one 0.1 µF bulk capacitor placed nearby the device IC. A ferrite bead isolating these pins from the general 1.1V power plane is also highly recommended.
- The PCIe upstream port 1.1V supplies for Lanes 2-3 (**VDD11PB**) are located on pins 49, 53, 54, 56, and 60 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. (Only one capacitor is necessary for pins which are adjacent and directly shorted together.) All pins should share one 1 µF and one 0.1 µF bulk capacitor placed nearby the device IC. A ferrite bead isolating these pins from the general 1.1V power plane is also highly recommended.
- The PCIe downstream port 1.1V supplies (**VDD11PC**) are located on pins 138, 142, and 143 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. (Only one capacitor is necessary for pins which are adjacent and directly shorted together.) All pins should share one 0.1 µF bulk capacitor placed nearby the device IC. A ferrite bead isolating these pins from the general 1.1V power plane is also highly recommended.
- The Ethernet MAC power supply (**VDD11ENET**) is located on pin 79 and requires a connection to a regulated 1.1V power plane. It is recommended to place one 0.1 µF and one 1 nF capacitor as close to the pin as possible.
- The USB3 PHY core 1.1V supplies (**VD11ATX0/VD11ARX0/VD11ATX1/VD11A1RX1**) are located on pins 109, 110, 120, and 121 and require a connection to a regulated 1.1V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible (only 1 capacitor is necessary for pins which are adjacent and directly shorted together). All pins should share one 1 µF and one 0.1 µF bulk capacitor placed nearby the device IC.

3.2 Variable Voltage

- The variable voltage supplies (**VDDVARIO**) are located on pins 37, 46, and 98 and require a connection to a regulated 1.8V to 3.3V power supply. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1 µF and one 0.1 µF bulk capacitor placed nearby the device IC.

3.3 3.3V Supplies

- The general I/O 3.3V voltage supplies (**VDD33**) are located on pins 6, 154, 161, and 163 and require a connection to a regulated 3.3V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible (only 1 capacitor is necessary for pins which are adjacent and directly shorted together). All pins should share one 1 µF and one 0.1 µF bulk capacitor placed nearby the device IC.
- The general I/O (1) 3.3V voltage supplies (**VDD33A0/VDD33A1**) are located on pins 113 and 124 and require a connection to a regulated 3.3V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1 µF and one 0.1 µF bulk capacitor placed nearby the device IC.
- The Ethernet MAC/RGMII Interface 3.3V voltage supplies (**VDD33ENET/VDDRGMII**) are located on pins 68, 80, and 84 and require a connection to a regulated 3.3V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 0.1 µF bulk capacitor placed nearby the device IC.

3.4 2.5V Supplies

- The PCIe upstream port 2.5V voltage supplies for Lanes 0-1 (**VDD25PA**) are located on pins 15, 20, and 24 and require a connection to a regulated 2.5V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 1 µF and one 0.1 µF bulk capacitor placed nearby the device IC.
- The PCIe upstream port 2.5V voltage supplies for Lanes 2-3 (**VDD25PB**) are located on pins 50, 55, and 59 require a connection to a regulated 2.5V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 0.1 µF bulk capacitor placed nearby the device IC.

- The PCIe downstream port 2.5V voltage supplies (**VDD25PC**) are located on pins 139 and 144 and require a connection to a regulated 2.5V power plane. Each pin should have a dedicated 1 nF capacitor placed as closely to the pin as possible. All pins should share one 0.1 µF bulk capacitor placed nearby the device IC.

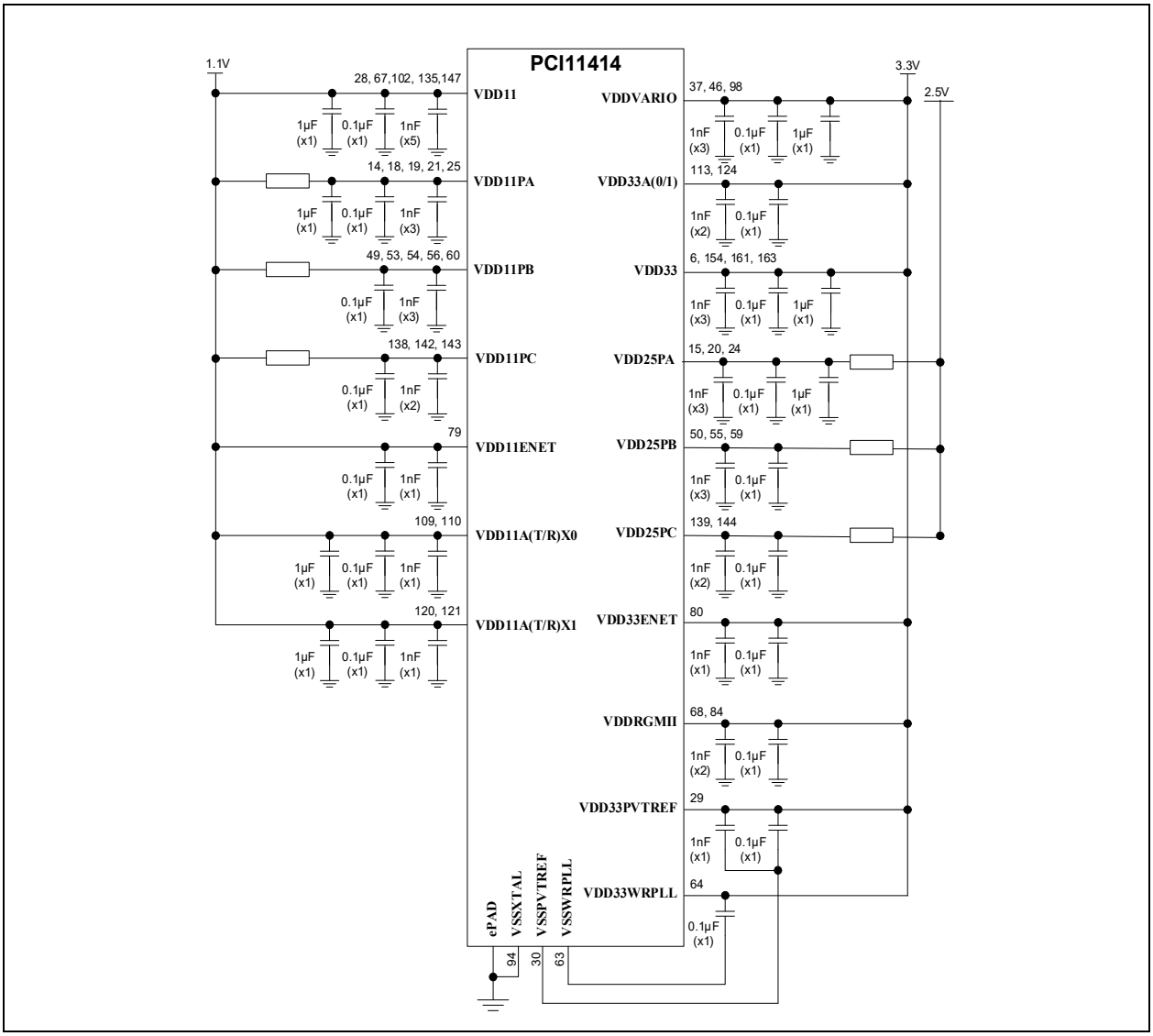
3.5 3.3V References

- The 3.3V reference for the internal PVT component (**VDD33PVTREF**) is located on pin 29 and requires a connection to a regulated 3.3V power plane. This pin should have dedicated 1 nF and 0.1 µF capacitors placed as closely to the pin as possible. The opposite end of these capacitors should be directly connected to the **VSSPVTREF** signal on pin 30 and should not be connected directly to the ground plane.
- The 3.3V reference for the internal PLL component (**VDD33WRPLL**) is located on pin 64 and requires a connection to a regulated 3.3V power plane. This pin should have a dedicated 0.1 µF capacitor placed as closely to the pin as possible. The opposite end of this capacitor should be directly connected to the **VSSWRPLL** signal on pin 63 and should not be connected directly to the ground plane.

3.6 Power Schematic

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 PCIE SIGNALS

4.1 Upstream Port PCIe Signals

The upstream port PCIe connections are shown in Figure 4-1 and Figure 4-2.

FIGURE 4-1: UPSTREAM PORT EDGE CONNECTOR PCIE CONNECTIONS

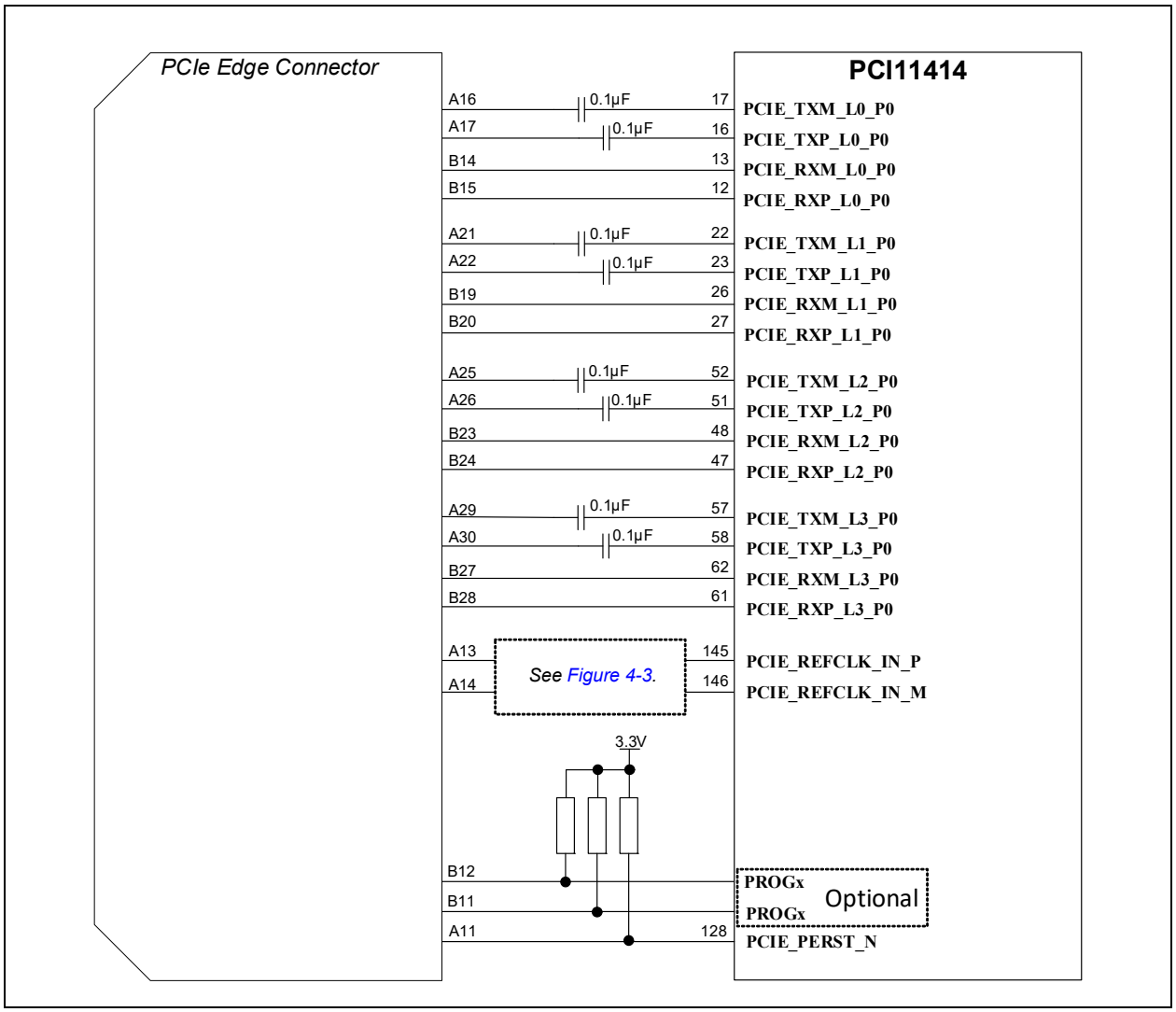
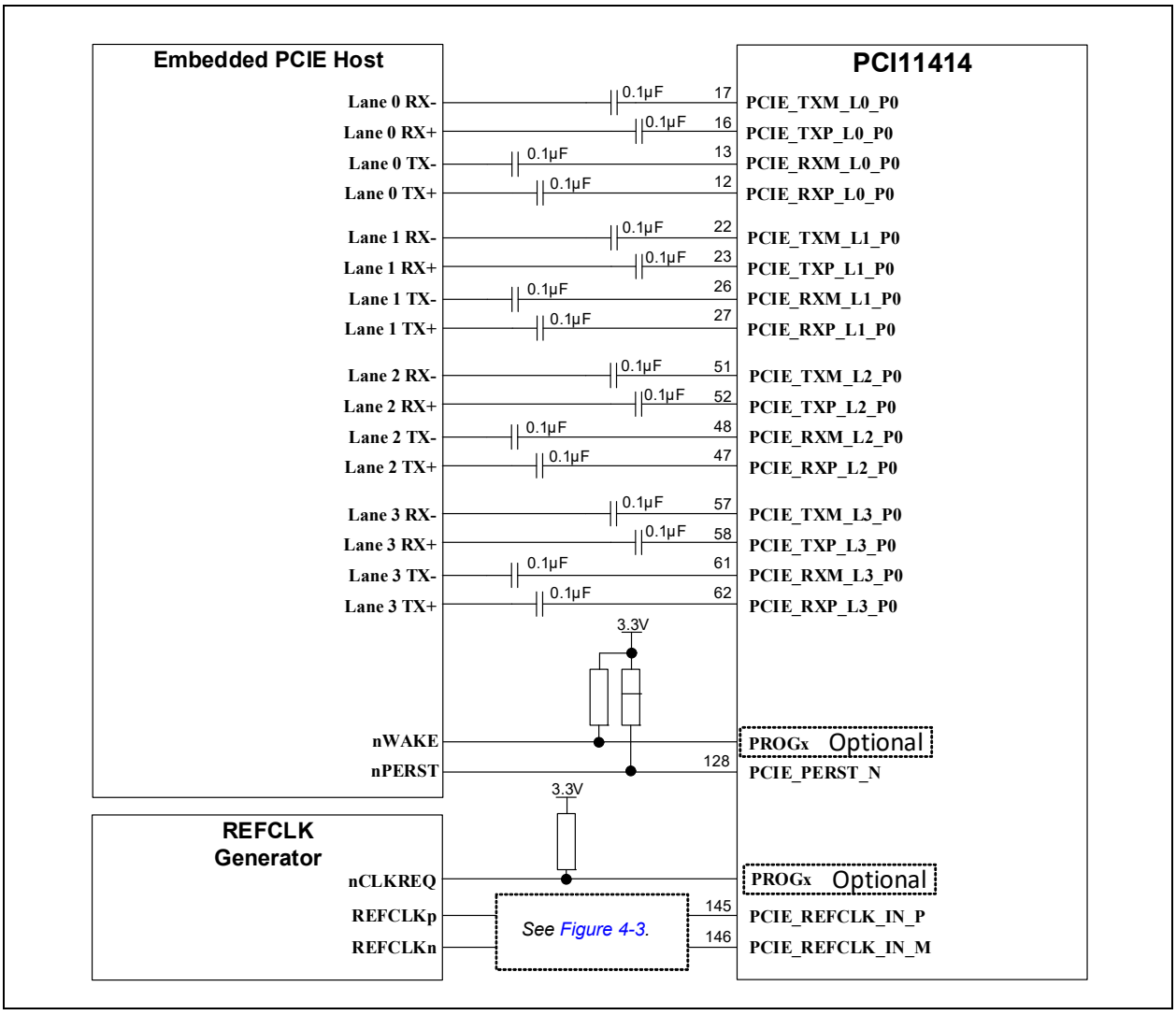


FIGURE 4-2: UPSTREAM PORT TO EMBEDDED HOST PCIE CONNECTIONS



4.1.1 PCIE PINS

- **PCIE_TXP_L0_P0/PCIE_TXM_L0_P0** (pins 16/17): These pins comprise the PCIe upstream Lane 0 transmitter differential pair. All necessary USB terminations and resistors are included in the IC. Both pins require a series of 0.1 µF decoupling (DC blocking) capacitors before being connected directly to the **PERp0/PERn0** pins of the PCIe edge connector, or the Lane 0 receiver pins of an embedded PCIe host.
- **PCIE_RXP_L0_P0/PCIE_RXM_L0_P0** (pins 12/13): These pins comprise the PCIe upstream Lane 0 receiver differential pair. All necessary USB terminations and resistors are included in the IC. The pins may be directly connected to the **PETp0/PETn0** pins of the PCIe edge connector, or connected to the Lane 0 transmitter pins of an embedded PCIe host through series 0.1 µF decoupling (DC blocking) capacitors.
- **PCIE_TXP_L1_P0/PCIE_TXM_L1_P0** (pins 22/23): These pins comprise the PCIe upstream Lane 1 transmitter differential pair. All necessary USB terminations and resistors are included in the IC. Both pins require a series of 0.1 µF decoupling (DC blocking) capacitors before being connected directly to the **PERp1/PERn1** pins of the PCIe edge connector, or the Lane 1 receiver pins of an embedded PCIe host.

Note: These pins may be left floating or unconnected if implementing a 1 Lane PCIe connection.

- **PCIE_RXP_L1_P0/PCIE_RXM_L1_P0** (pins 26/27): These pins comprise the PCIe upstream Lane 1 receiver differential pair. All necessary USB terminations and resistors are included in the IC. The pins may be directly connected to the **PETp1/PETn1** pins of the PCIe edge connector, or connected to the Lane 1 transmitter pins of an

embedded PCIe host through series 0.1 µF decoupling (DC blocking) capacitors.

Note: These pins may be left floating or unconnected if implementing a 1 Lane PCIe connection.

- **PCIE_TXP_L2_P0/PCIE_TXM_L2_P0** (pins 51/52): These pins comprise the PCIe upstream Lane 2 transmitter differential pair. All necessary USB terminations and resistors are included in the IC. Both pins require a series of 0.1 µF decoupling (DC blocking) capacitors before being connected directly to the **PERp2/PERn2** pins of the PCIe edge connector, or the Lane 2 receiver pins of an embedded PCIe host.

Note: These pins may be left floating/unconnected if implementing 1 or 2 Lane PCIe connections.

- **PCIE_RXP_L2_P0/PCIE_RXM_L2_P0** (pins 47/48): These pins comprise the PCIe upstream Lane 2 receiver differential pair. All necessary USB terminations and resistors are included in the IC. The pins may be directly connected to the **PETp2/PETn2** pins of the PCIe edge connector, or connected to the Lane 2 transmitter pins of an embedded PCIe host through series 0.1 µF decoupling (DC blocking) capacitors.

Note: These pins may be left floating/unconnected if implementing 1 or 2 Lane PCIe connections.

- **PCIE_TXP_L3_P0/PCIE_TXM_L3_P0** (pins 57/58): These pins comprise the PCIe upstream Lane 3 transmitter differential pair. All necessary USB terminations and resistors are included in the IC. Both pins require a series of 0.1 µF decoupling (DC blocking) capacitors before being connected directly to the **PERp3/PERn3** pins of the PCIe edge connector, or the Lane 3 receiver pins of an embedded PCIe host.

Note: These pins may be left floating/unconnected if implementing 1 or 2 Lane PCIe connections.

- **PCIE_RXP_L3_P0/PCIE_RXM_L3_P0** (pins 61/62): These pins comprise the PCIe upstream Lane 3 receiver differential pair. All necessary USB terminations and resistors are included in the IC. The pins may be directly connected to the **PETp3/PETn3** pins of the PCIe edge connector, or connected to the Lane 3 transmitter pins of an embedded PCIe host through series 0.1 µF decoupling (DC blocking) capacitors.

Note: These pins may be left floating/unconnected if implementing 1 or 2 Lane PCIe connections.

4.1.2 REFCLK

- **PCIE_REFCLK_IN_P/PCIE_REFCLK_IN_M** (pins 145/146): These pins comprise the 100 MHz PCIe Differential Reference Clock which is supplied by the PCIe Root Complex port. A PCIe REFCLK buffer device is used to buffer and supply the 100 MHz to the PCI11414 upstream port and PCIe downstream ports, as shown in Figure 4-3. If downstream PCI11414 ports are unused, the PCIe **REFCLK** pins of the PCIe Edge Connector can connect directly to the PCI11414 without the use of a buffer, as indicated in Figure 4-4.
- PCI11414 **REFCLK** pins are LVDS (Low-Voltage Differential Signaling) differential inputs, but PCIe REFCLK sources are normally differential HCSL (High-Speed Current Steering Logic). LVDS and HCSL have different nominal common-mode voltage and nominal voltage swing specifications. The LVDS standard requires a receiver to accept any common mode of 0V to 2.4V. The HCSL **TX** common mode is within the range of acceptable common mode voltages for LVDS, and the REFCLK receiver of PCI11414 is capable of recovering a clock which is transmitted with HCSL voltage swing. Figure 4-3 illustrates an implementation using a Microchip ZL40264 clock buffer, which implements HCSL outputs. Figure 4-4 shows an example of REFCLK being sourced directly from and edge connector, which is always expected to be an HCSL clock source.

FIGURE 4-3: REFCLK CONNECTIONS WITH REFCLK BUFFER

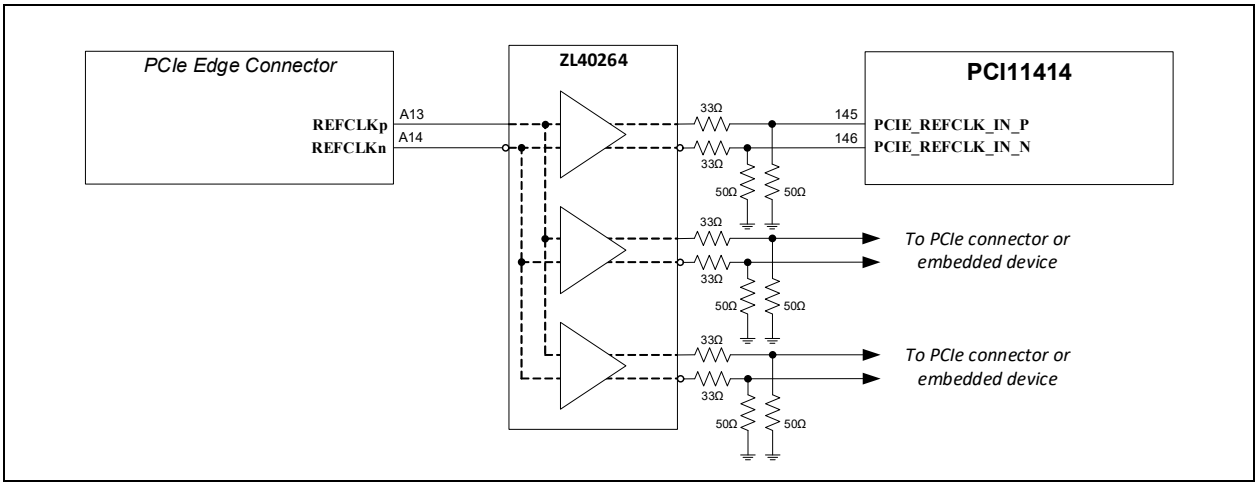
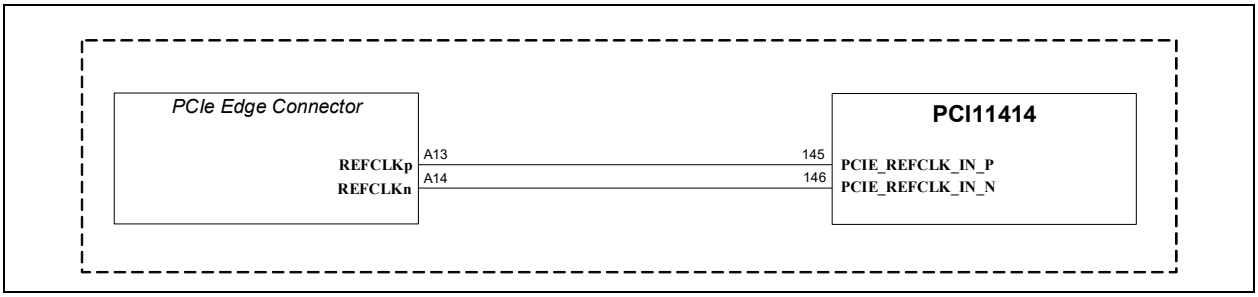


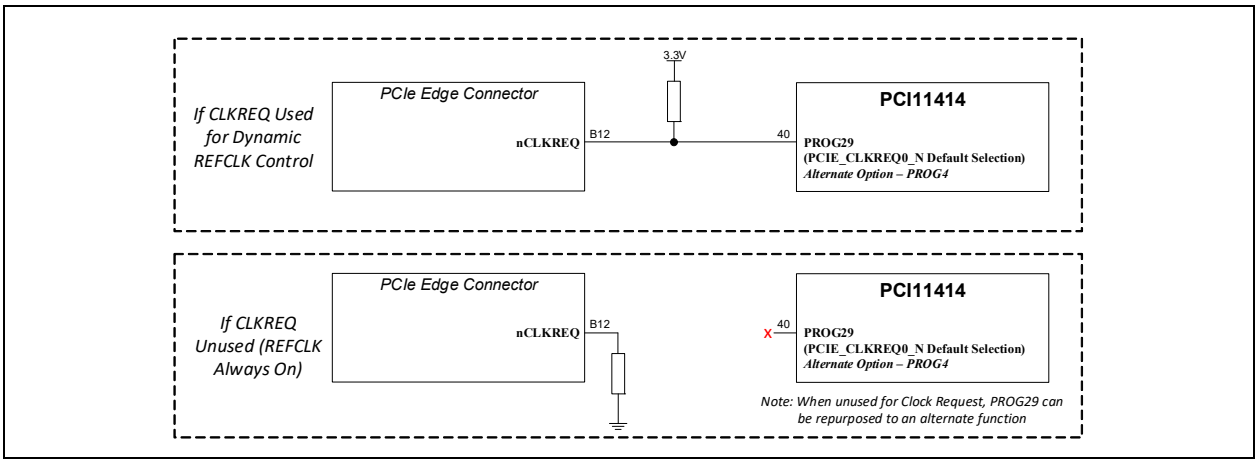
FIGURE 4-4: REFCLK CONNECTIONS WITH NO BUFFER AND NO DOWNSTREAM PCIE PORTS



4.1.3 CLOCK REQUEST

- The **PCIE_CLKREQ0_N** pin function (which is assigned to PROG29 in PCI11414 by default) is an optional pin function used to allow for dynamic REFCLK request. This functionality is necessary to support L1 substates (L1.1 and L1.2). If L1 substates are unsupported, this pin function can be left unused in the end application while pulling the **nCLKREQ** pin on the edge connector to **GND** to force the **REFCLK** output to always remain enabled. The Clock Request options are displayed graphically in Figure 4-5.

FIGURE 4-5: UPSTREAM PORT CLOCK REQUEST OPTIONS



If utilizing the dynamic Clock Request functionality:

- A programmable pin function must be selected and programmed into the PCI11414 device via the preferred method (EEPROM or OTP memory).
- The selected pin on the PCI11414 device must connect to the PCIe edge connector **nCLKREQ** (pin B12 of a standard PCIe Edge connector).
- An external pull-up resistor to 3.3V should be included.

If not utilizing the dynamic Clock Request functionality:

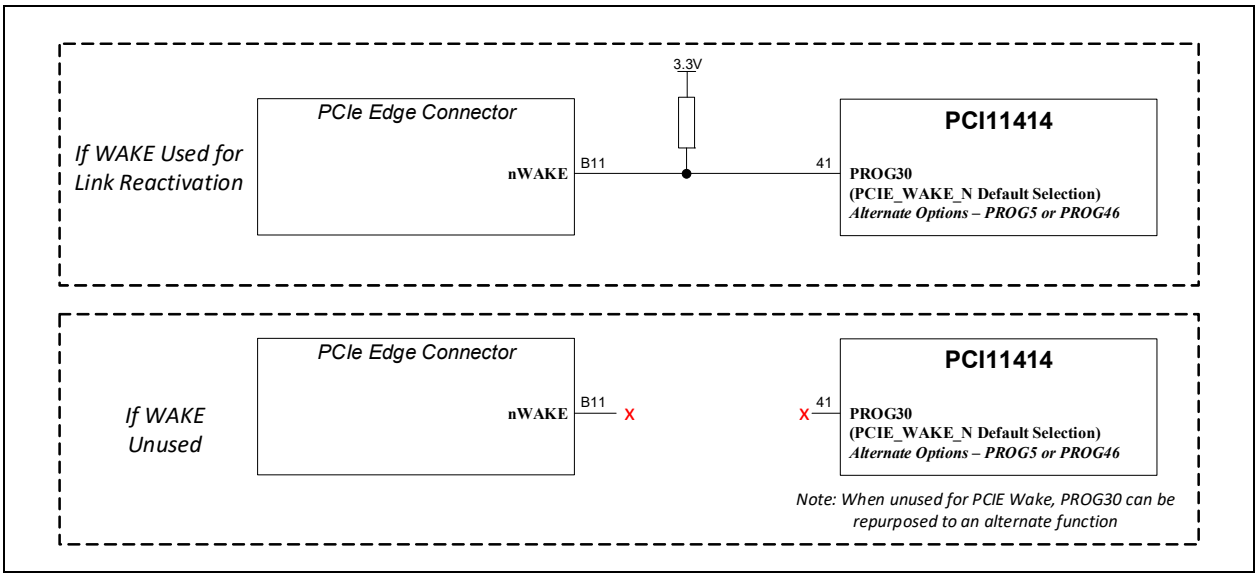
- The pin on PCI11414 may be left floating (if leaving the default selection of PROG29 unchanged) or left unassigned.
- The **nCLKREQ** pin on the PCIe Edge connector should be pulled low to ensure that the REFCLK is always output.

4.1.4 WAKE

- The **PCIE_WAKE_N** pin function (which is assigned to PROG30 in PCI11414 by default) is an optional pin function used to allow for link reactivation from the D3cold Low-power state. Support of the **PCIE_WAKE_N** is optional.

The Clock Request options are displayed graphically in Figure 4-6.

FIGURE 4-6: UPSTREAM PORT WAKE OPTIONS



If utilizing the Wakeup functionality:

- A programmable pin function must be selected and programmed into the PCI11414 device via the preferred method (EEPROM or OTP memory), or left with the default selection of PROG30.
- The selected pin on the PCI11414 device must connect to the PCIe edge connector **nWAKE** (pin B11 of a standard PCIe Edge connector).
- An external pull-up resistor to 3.3V should be included.

If not utilizing the Wakeup functionality:

- The pin on PCI11414 may be left floating (if leaving the default selection of PROG30 unchanged) or left unassigned.
- The **nCLKREQ** pin on the PCIe Edge connector should be pulled low to ensure that the **REFCLK** is always output.

4.1.5 PERST

- **PCIE_PERST_N** (pin 128): PERST should always be connected directly to the edge connector or directly to the PERST control output of the embedded host. An external pull-up resistor may be required for certain systems, such as when PCI11414 is directly connected to an embedded host. For standard PCIe edge card use-cases, it is assumed that the PCIe host board implements the PERST pull-up resistor.

4.2 Downstream Port PCIe Signals

The PCI11414 has a single, one-lane downstream PCIe port. This downstream port can be connected in a number of ways:

- To a standard PCIe slot, as shown in Figure 4-7.
- To an embedded PCIe device, as shown in Figure 4-8.
- To an alternate PCIe connector (i.e.: Mini PCIe, M.2, SD Express card, etc.). Consult relevant standard documents and reference designs for more details on how to implement these connections. Contact Microchip support for additional resources.

FIGURE 4-7: STANDARD DOWNSTREAM PCIE PORT SLOT IMPLEMENTATION

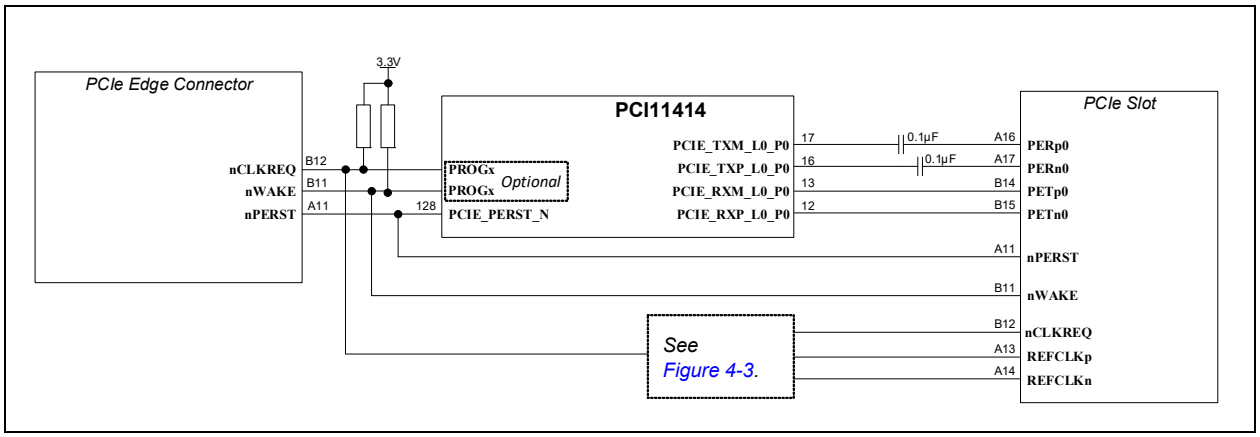
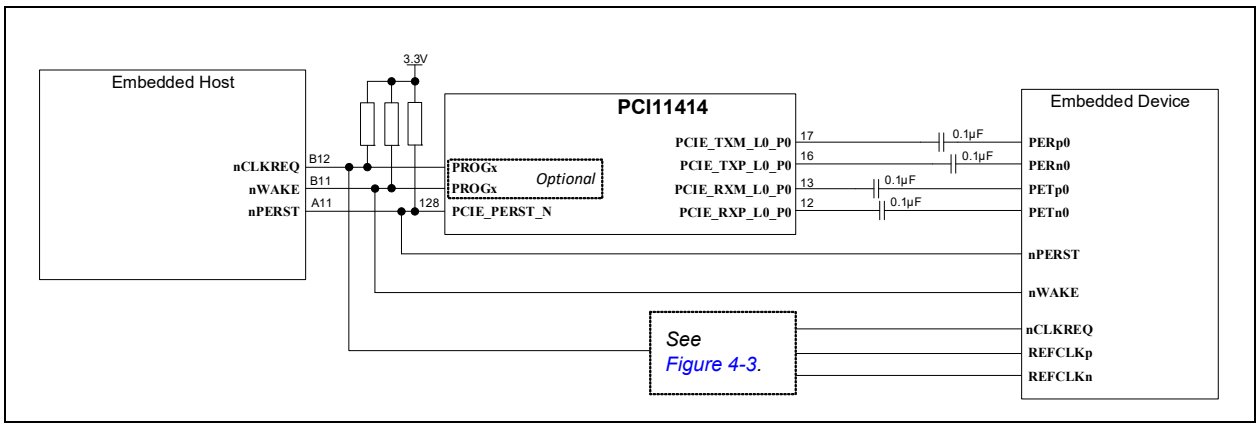


FIGURE 4-8: EMBEDDED DOWNSTREAM PCIE PORT IMPLEMENTATION



5.0 USB SIGNALS

5.1 USB Host Ports

5.1.1 USB DATA PINS

TABLE 5-1: USB DATA PIN MAPPING

Name ('x' is replaced by 1-4 to indicator associated port number.)	Pin				Description
	Port 1	Port 2	Port 3	Port 4	
USB2_DP_Px	116	105	130	133	This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the **D**+ pin of a USB connector. See **Note 1**.
USB2_DM_Px	117	106	131	134	This pin is the negative (–) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the **D**– pin of a USB connector. See **Note 1**.
USB3_TX1P_Px	118	107	—	—	This pin is the positive (+) signal of the downstream port USB3.1 transmitter (**TX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the **TX**+ (or **TX**–)[2] pin of the USB connector. See **Note 2** and **Note 3**.
USB3_TX1M_Px	119	108	—	—	This pin is the negative (–) signal of the downstream port USB3.1 transmitter (**TX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin requires a series of 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the **TX**– (or **TX**+)[2] pin of the USB connector. See **Note 2** and **Note 3**.
USB3_RX1P_Px	122	111	—	—	This pin is the positive (+) signal of the downstream port USB3.1 receiver (**RX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the **RX**+ (or **RX**–)[2] pin of the USB connector. See **Note 2** and **Note 3**.
USB3_RX1M_Px	123	112	—	—	This pin is the negative (–) signal of the downstream port USB3.1 receiver (**RX**) differential pair. All necessary USB terminations and resistors are included in the IC. This pin can be connected directly to the **RX**– (or **RX**+)[2] pin of the USB connector. See **Note 2** and **Note 3**.

Note 1: The USB2.0 positive and minus pins can be swapped by utilizing the Microchip PortSwap feature. This must be configured through the register settings in the PCI11414 device.

2: A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the **TX** lines are swapped, or if the positive and negative pins of the **RX** lines are swapped.

3: These pins have an alternate name when USB3 PHYs are grouped together to form a USB Type-C® port. The PHYs are grouped to allow for a USB Type-C implementation without the need of an external muxing device. The CC1_Px and CC2_Px pins determine which USB3 PHY to use for a given connection based on how the user inserted the reversible USB Type-C cable. In this case, USB3_TX1P_P2 is renamed to USB3_TX2P_P1, USB3_TX1M_P2 is renamed to USB3_TX2M_P1, USB3_RX1P_P2 is renamed to USB3_RX2P_P1, USB3_RX1M_P2 is renamed to USB3_RX2M_P1.

5.1.2 PORT CONTROL PINS CONTROL PINS

TABLE 5-2: TYPE-C CONTROL PIN MAPPING

Name ('x' is replaced by 1-4 to indicator associated port number)	Pin				Description
	Port 1	Port 2	Port 3	Port 4	
VB_PRT_CTL_Px/ VB_OCS_Px	Assignable **Note 1**				This pin is a hybrid input/output which is used to enable a VBUS power source to the USB connector and detect a VBUS Fault event when the VBUS power switch device pulls the pin low via an open-drain output. When VBUS is to be disabled, this pin operates as an output and drives the pin low. When VBUS is enabled, this pin enables an internal pull-up resistor and operates as an input to monitor for Fault events.
CC1_DPx	114	103	—	—	This pin is used to detect a USB Type-C® connection and insertion orientation. This should connect directly to the CC1 pin of the USB Type-C® connector.
CC2_DPx	115	104	—	—	This pin is used to detect a USB Type-C® connection and insertion orientation. This should connect directly to the CC2 pin of the USB Type-C® connector.
VBUS_MON_Px	129	132	—	—	This pin is used to sense the voltage on VBUS of the Type-C port. This allows the Type-C logic to detect when VBUS is enabled and when VBUS has been discharged (i.e.: after the connection is removed or a fault has occurred).
VCONN1_EN_Px	Assignable **Note 1**		—	—	This pin is used to enable the VCONN power supply to the CC1 pin of the Type-C port when a valid Ra resistor is detected inside of the cable through the CC1/CC2 lines.
VCONN2_EN_Px	Assignable **Note 1**		—	—	This pin is used to enable the VCONN power supply to the CC2 pin of the Type-C port when a valid Ra resistor is detected inside of the cable through the CC1/CC2 lines.
VBUS_DIS_Px	Assignable **Note 1**		—	—	This pin controls a VBUS discharge circuit to ensure that voltage on VBUS is discharged quickly following a USB Type-C cable detach or fault event.

Note 1: These pin roles can be assigned to a number of programmable function pins (PROGx). Consult the PCI11414 Data Sheet Programmable Pin Function table for available options for each pin role.

The USB ports of PCI11414 can be configured to form a number of port combinations. PCI11414 includes two USB3.2 Gen2 PHYs and four USB2 PHYs which can be arranged into one of the following:

- All Type-A ("AAAA")
- One Type-C + Three Type-A ("CAAA")
- Two Type-C + Two Type-A option 1 ("CCAA-1")
- Two Type-C + Two Type-A option 2 ("CCAA-2")

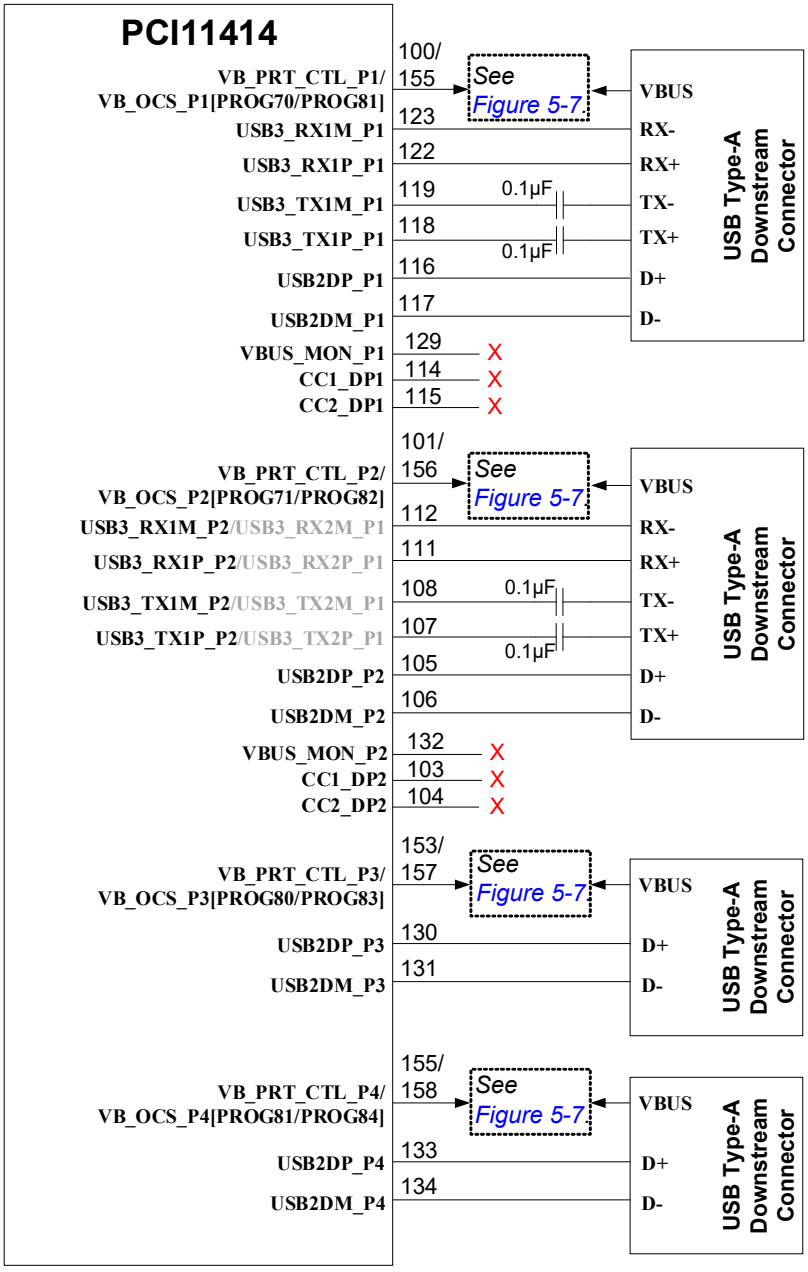
Other variations are also possible using one of the above configurations as a starting point by disabling entire ports or disabling just the USB3 channel of ports.

5.1.3 ALL TYPE-A (“AAAA”)

TABLE 5-3: AAAA COMBINATION

Port	Connector Type	Speed	PHYs
Port 1	Type-A	USB3.2	USB3.2 PHY1 + USB2.0 PHY1
Port 2	Type-A	USB3.2	USB3.2 PHY2 + USB2.0 PHY2
Port 3	Type-A	USB2.0	USB2.0 PHY3
Port 4	Type-A	USB2.0	USB2.0 PHY4

FIGURE 5-1: ALL TYPE-A OPTION (“AAAA”)

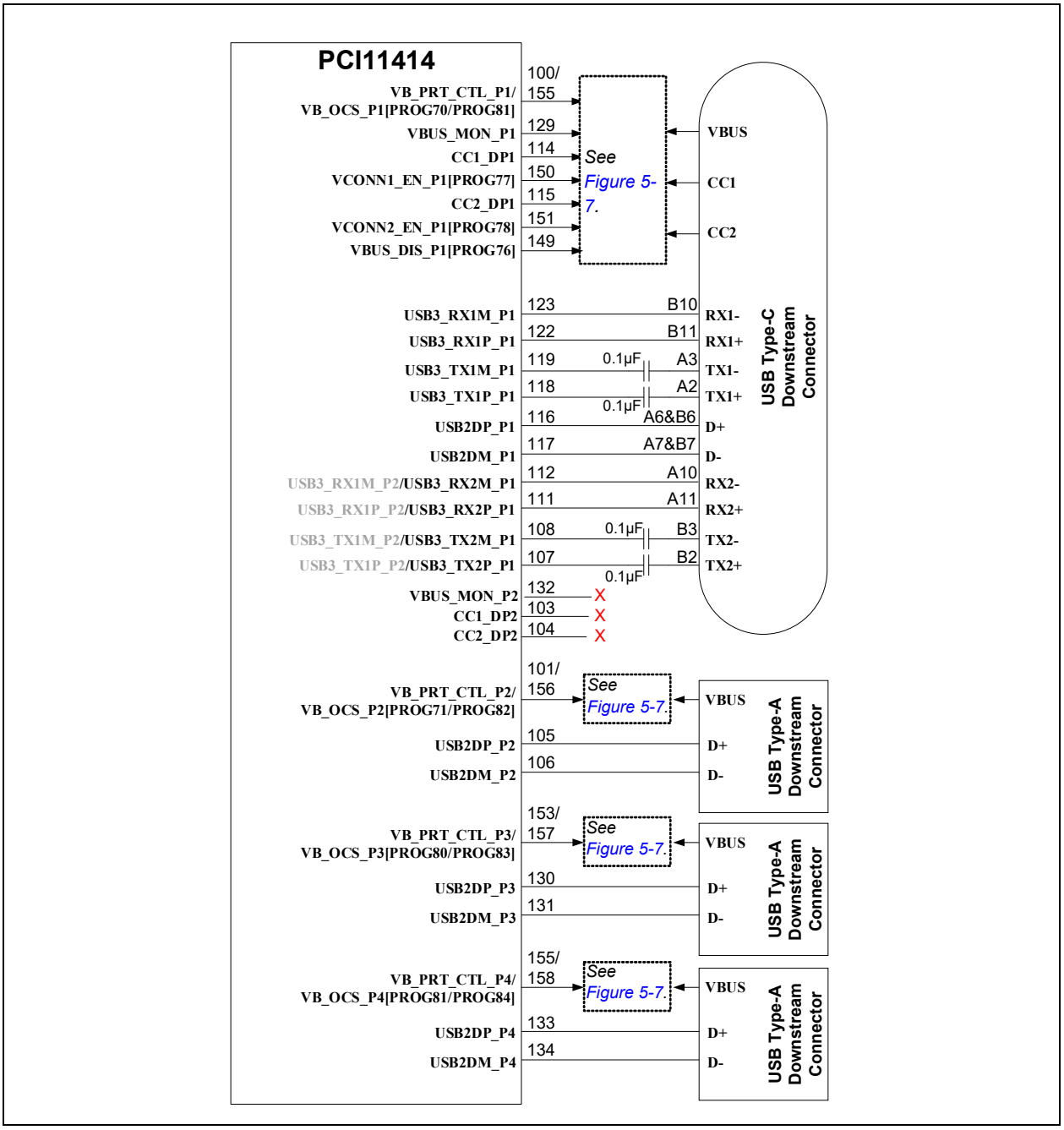


5.1.4 ONE TYPE-C + THREE TYPE-A (“CAAA”)

TABLE 5-4: CAAA COMBINATION

Port	Connector Type	Speed	PHYs
Port 1	Type-C	USB3.2	USB3.2 PHY1 + USB3.2 PHY2 + USB2.0 PHY1
Port 2	Type-A	USB2.0	USB2.0 PHY2
Port 3	Type-A	USB2.0	USB2.0 PHY3
Port 4	Type-A	USB2.0	USB2.0 PHY4

FIGURE 5-2: ONE TYPE-C + THREE TYPE-A OPTION 2 (“CAAA”)

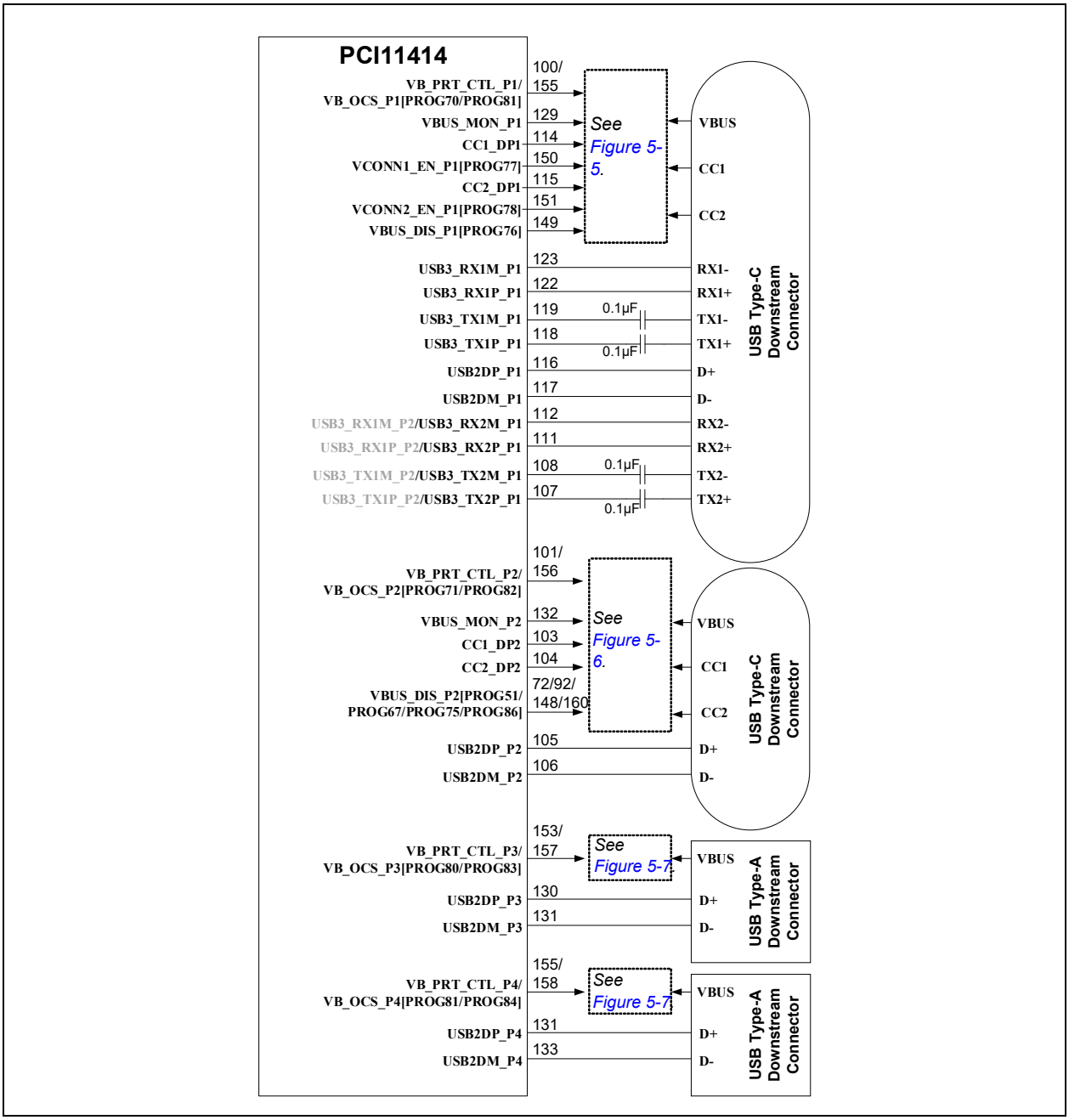


5.1.5 TWO TYPE-C + TWO TYPE-A OPTION 1 (“CCAA-1”)

TABLE 5-5: CCAA-1 COMBINATION

Port	Connector Type	Speed	PHYs
Port 1	Type-C	USB3.2	USB3.2 PHY1 + USB3.2 PHY2 + USB2.0 PHY1
Port 2	Type-A	USB2.0	USB2.0 PHY2
Port 3	Type-A	USB2.0	USB2.0 PHY3
Port 4	Type-A	USB2.0	USB2.0 PHY4

FIGURE 5-3: TWO TYPE-C + TWO TYPE-A OPTION 1(“CCAA-1”)

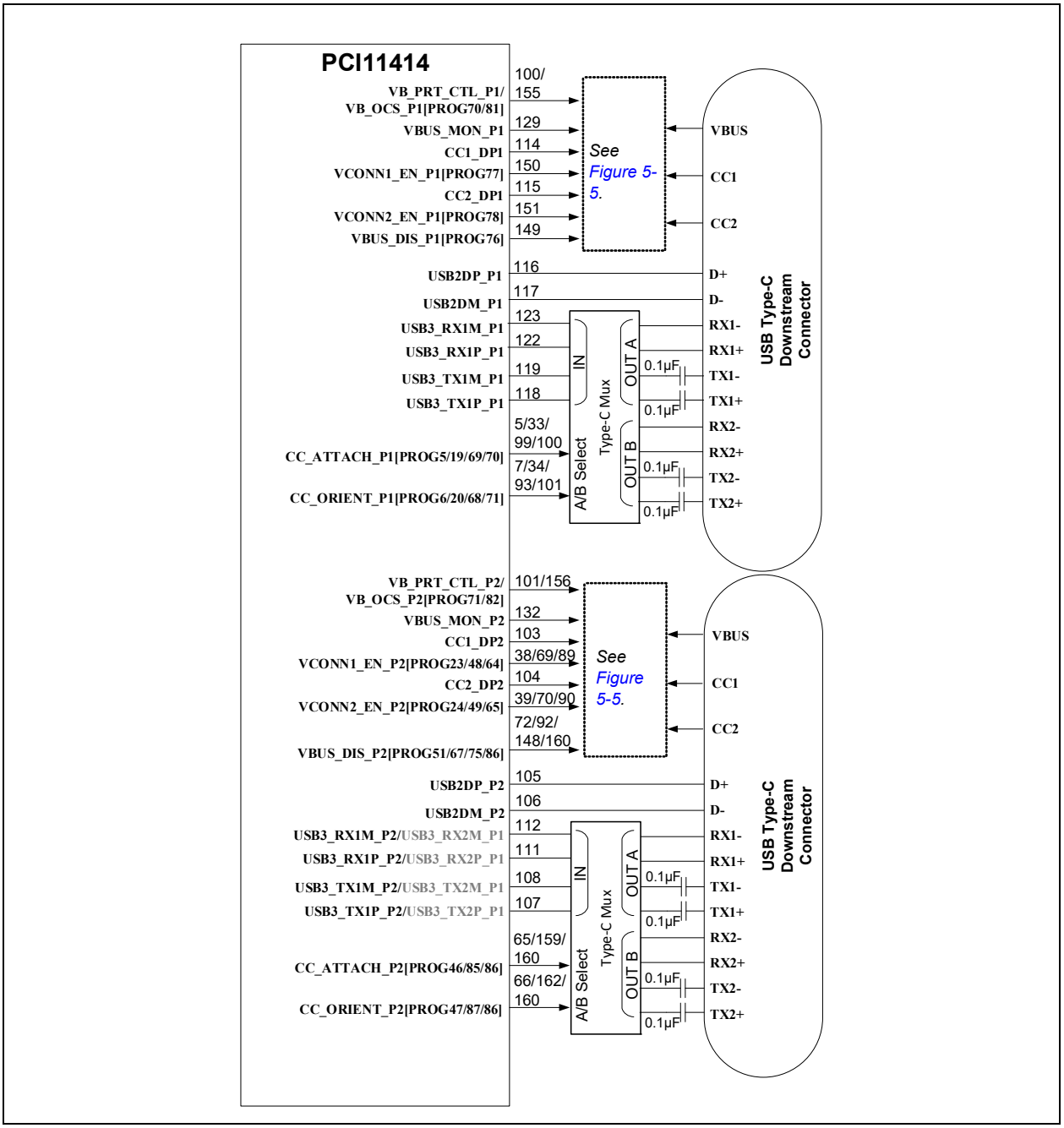


5.1.6 TWO TYPE-C + TWO TYPE-A OPTION 2 (“CCAA-2”)

TABLE 5-6: CCAA-2 COMBINATION

Port	Connector Type	Speed	PHYs
Port 1	Type-C	USB3.2	USB3.2 PHY1 (with External USB3 Mux) + USB2.0 PHY1
Port 2	Type-C	USB3.2	USB3.2 PHY2 (with External USB3 Mux) + USB2.0 PHY2
Port 3	Type-A	USB2.0	USB2.0 PHY3
Port 4	Type-A	USB2.0	USB2.0 PHY4

FIGURE 5-4: TWO TYPE-C + TWO TYPE-A OPTION 2 (“CCAA-2”)



5.2 Disabling Downstream Ports

- Disable downstream ports if unused.
- If a downstream port of the PCI11414 is unused, it should be disabled. This can be achieved through configuration (I^2C/SPI or EEPROM/OTP), or through a port disable strap option.
- If using the port disable strap option, the USB_DP2 and USB_DM2 signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net, or through a pull-up resistor. All other signals related to the associated port may be floated.

5.3 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These are generally grouped into three categories:

1. TVS protection diodes
   - ESD protection for IEC-61000-4-2 system-level tests
2. Application targeted protection ICs or galvanic isolation devices
   - DC overvoltage protection for short to battery protection
3. Common-mode chokes
   - For EMI reduction

The PCI11414 can be used in conjunction with these types of devices, but these devices may have a negative effect on USB signal integrity. Thus, it is important to select components accordingly and follow implementation guidelines from the device manufacturer. The following general guidelines for implementing these devices may also be implemented:

- Select only devices that are designed specifically for high-speed applications. Based on the USB2.0 specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry. In a USB3.1 Gen 1 system, ESD protection should add no more than 0.5 pF capacitance to the differential pairs.
- Place these devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- Always ensure a very low impedance path to a large ground plane. The effectiveness of TVS devices depends heavily on effective grounding.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

5.3.1 ADDITIONAL PROTECTION OPTIONS FOR USB3 PINS

In addition to TVS diodes, some or all of the following may be implemented:

- Use decoupling capacitors on both the **TX** and **RX** differential pairs. Decoupling capacitors on the **RX** pairs is not required for operation, but it adds some additional ESD immunity at a low cost.
- Use decoupling capacitors with high voltage ratings. 0.1 µF capacitors at 0402 sizes are widely available.
- A very small resistor of 0.3Ω to 0.5Ω may be placed in series with the decoupling capacitor (placed physically between the TVS diode and the decoupling capacitor) to help steer more of the ESD energy through the TVS diode. A resistor network (2-resistor/4-contact) in 0402 or 0201 size can be placed with very little impact on the differential routing of the signals.

Note:	Microchip PHYBoost, VariSense™, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help overcome marginal failures. It is simplest to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests, on physical hardware.

5.4 VBUS and PRT_CTLx Connections of Downstream Ports

The **VB_PRT_CTL_Px** pin is a hybrid I/O pin which has the following states:

- PORT OFF: **VB_PRT_CTL_Px** is an output and drives low. The **VB_PRT_CTL_Px** pin only transitions to the PORT ON state through a specific command from the USB host.
- PORT ON: **VB_PRT_CTL_Px** is an input with a weak internal pull-up enabled. The input buffer monitors overcur-

rent events, which are indicated by the port power controller by pulling the **VB_PRT_CTL_Px** line low. Once an overcurrent event is detected, the **VB_PRT_CTL_Px** automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

When connecting the **VB_PRT_CTL_Px** pin to a port power controller, the signal should be connected to both the Enable and the Fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

Note:	The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

The **VBUS_MON_Px** pin is an input with a preconfigured set of comparator banks. These comparator banks are used to monitor the voltage on the VBUS pin to ensure that the voltage is within the correct range while in the VBUS ON and OFF states ('vSafe5V' and 'vSafe0V', respectively). The recommended connection to VBUS is through a resistor divider of 43 kΩ over 49.9 kΩ. When the downstream port is used as a USB Type C® port, this pin must be connected per this guidance and may not be left floating or unused. When the downstream port is used as a Type A port, the VBUS_MON_Px pin can be left floating.

The **VBUS_DIS_Px** pin is an output that asserts whenever power to VBUS is transitioning from ON to OFF ('vSafe5V' to 'vSafe0V'). This pin can be connected to a transistor that should turn on and short VBUS to GND when this signal asserts to 3.3V. A series resistor in the 400Ω to 700Ω range is recommended to limit the current through the transistor and to add discharge slew rate controllability. When discharging the VBUS pin, the voltage must reach the vSafe0V voltage window within the discharge time as defined in the USB Type-C specification (see the latest revision for the most up-to-date timing and voltage requirements).

Some port power controllers have an automatic discharge function when they are shut off. In that case, the **VBUS_DIS_Px** pin may be left floating.

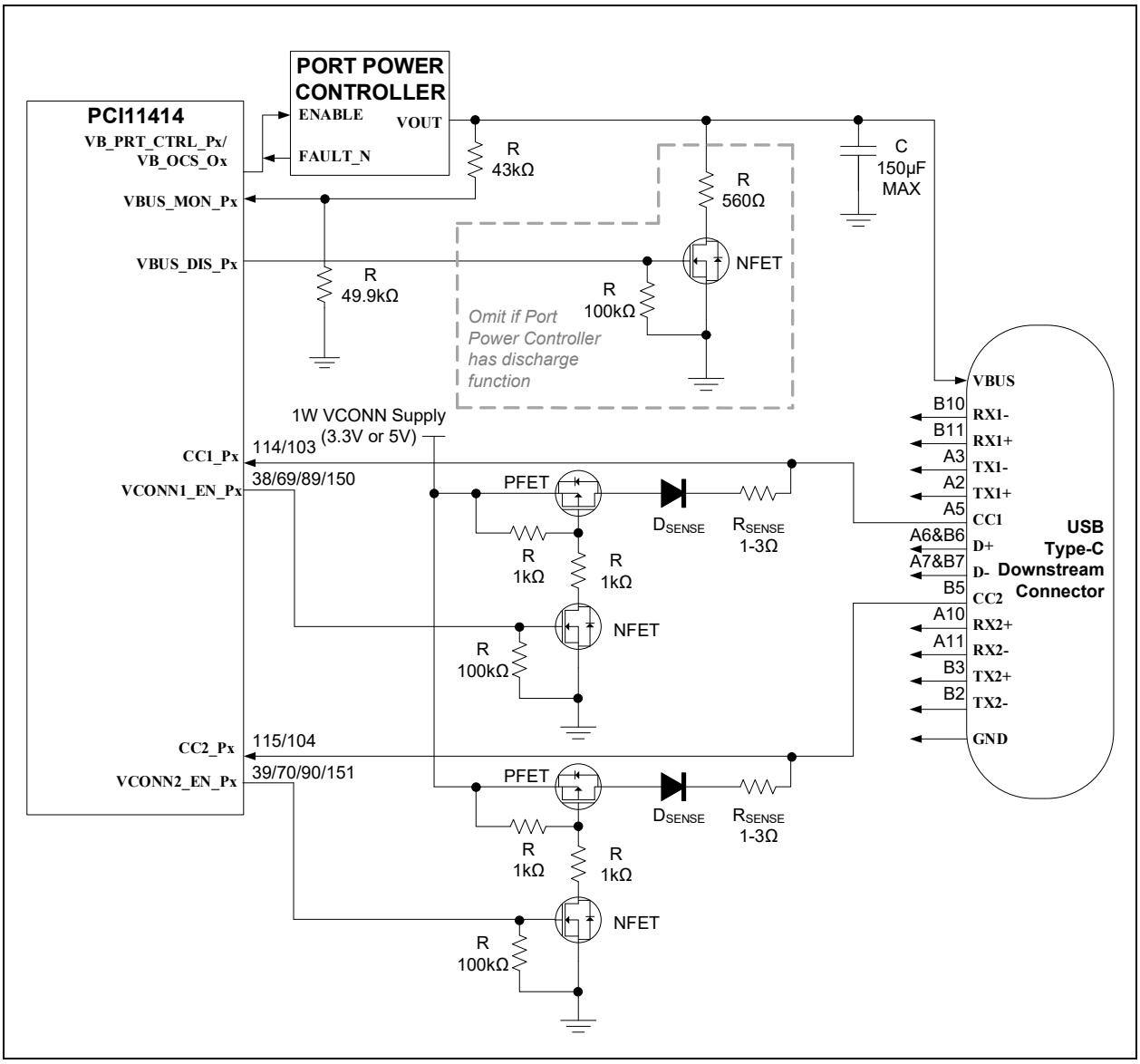
A typical Type-C implementation is shown in Figure 5-5.

CC1_Px and **DPx_CC2_Px** of downstream ports 1 and 2 of PCI11414 are designed to connect directly to the respective CC1 and CC2 pins of the Type-C connector.

VCONN1_EN_Px and **VCONN2_EN_Px** of downstream ports 1 and 2 of PCI11414 are active-high control signals that assert when the VCONN should be supplied to an active or electronically marked cable or to a VCONN powered accessory. The VCONN supply for a standard Type-C application must be capable of supplying 1W of VCONN power to each Type-C downstream port. For the VCONN power supply, 5V is recommended though lower voltages are also supported. The recommended arrangement is an NFET to invert the polarity of the control signal, and a PFET pass transistor for the VCONN voltage.

VCONN overcurrent is sensed by voltage drop on the **CCx** pin. A diode and a low-impedance series resistor may be necessary to ensure this voltage drop is achieved when VCONN current draw exceeds the desired overcurrent threshold. The diode and resistor characteristics should be tuned by the system designer to match the exact desired overcurrent setting.

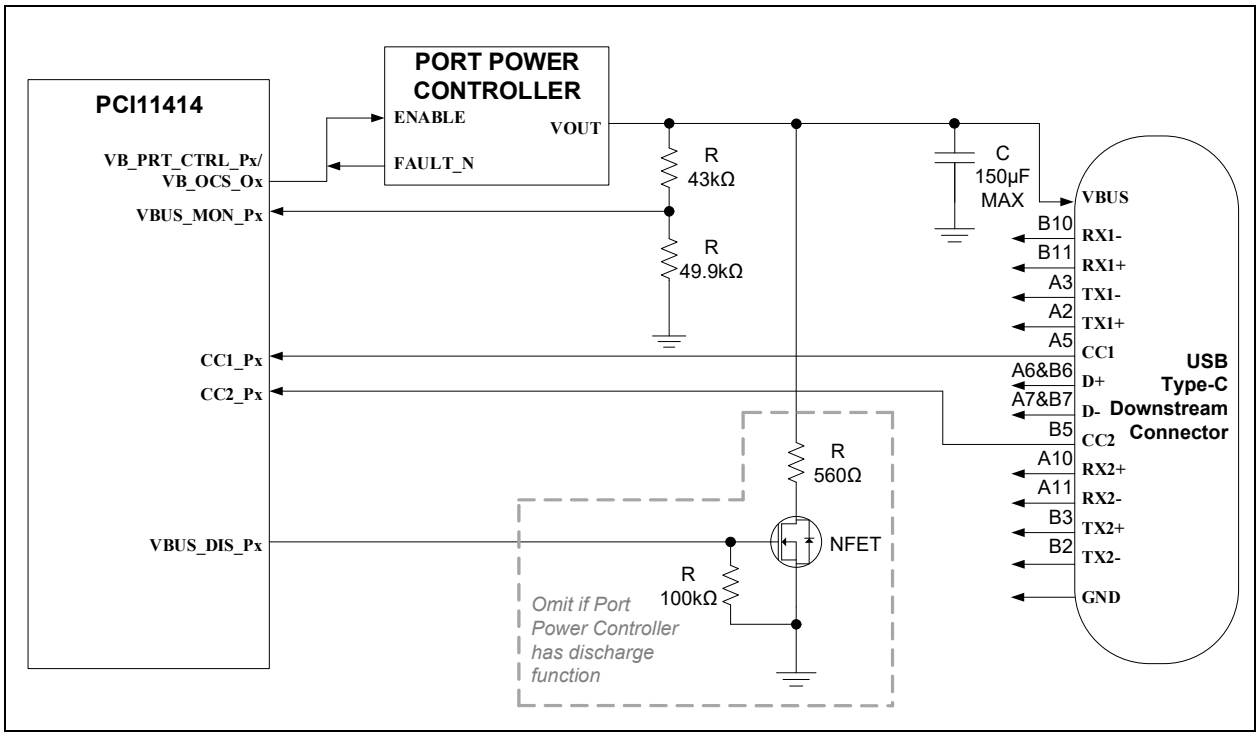
FIGURE 5-5: DOWNSTREAM TYPE-C PORT POWER CONTROL (WITH VCONN)



Note:	The implementation, as shown in Figure 5-5, assumes that the port power controller has an active-high Enable input, and an active-low, open-drain style Fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

A Type-C with VCONN implementation is shown in Figure 5-6. VCONN may only be omitted when a Type-C port is operating with USB2.0 Only speeds.

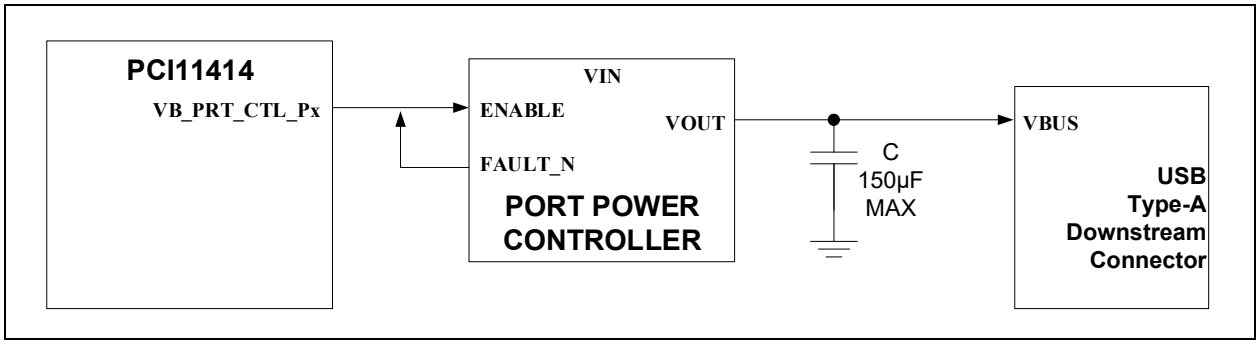
FIGURE 5-6: DOWNSTREAM TYPE-C PORT POWER CONTROL (WITHOUT VCONN)



Note: The implementation, as shown in Figure 5-6, assumes that the Type-C controller has an active-high Enable input, and the port power controller have an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the Type-C controller, port power controller, or both have different I/O characteristics.

A typical Type-A implementation is shown in Figure 5-7.

FIGURE 5-7: DOWNSTREAM TYPE-A PORT POWER CONTROL



5.5 GND and EARTH Recommendations

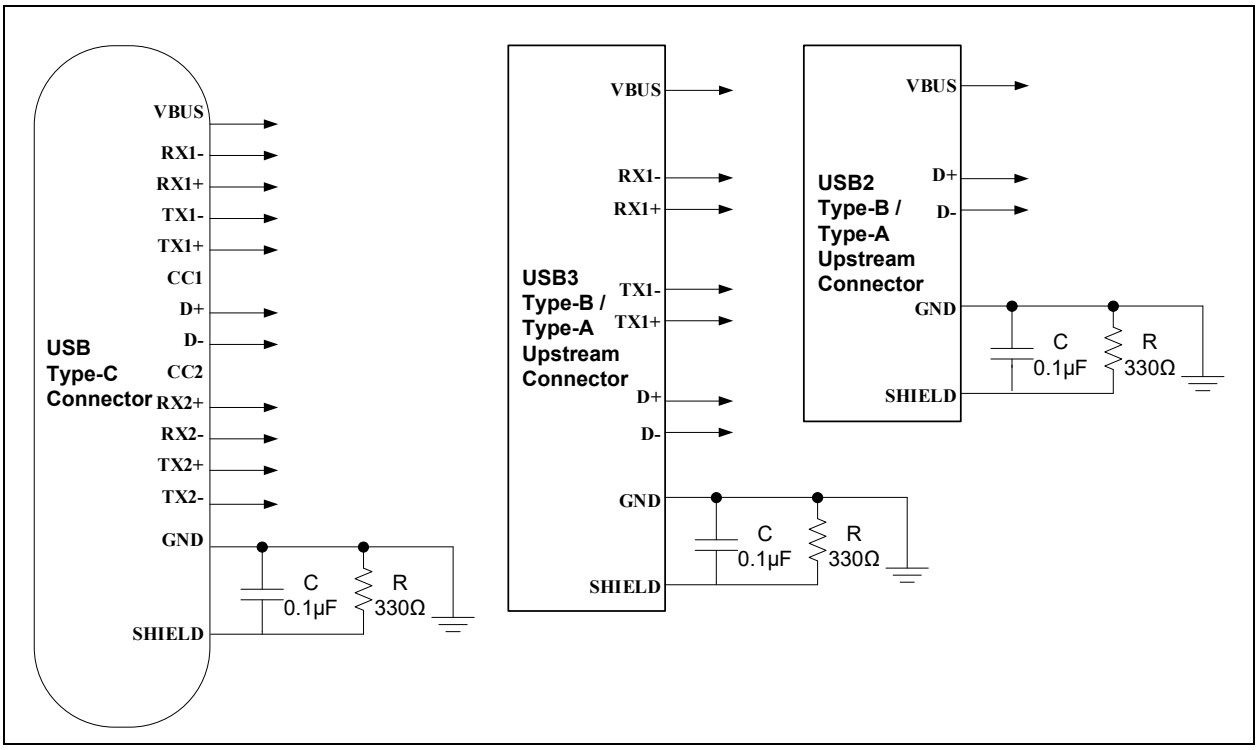
The GND pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (Recommended) Connect to GND through a resistor and capacitor in parallel. A resistor-capacitor (RC) filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Connect directly to the GND plane.

The recommended implementation is shown in Figure 5-8.

FIGURE 5-8: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 ETHERNET

The PCI11414 has an integrated Ethernet MAC capable of operating at supporting up to 2.5 Gbps. The following is a summary of key points:

- Either SGMII or RGMII operational modes may be used. MII, RMII, and GMII PHY interconnect standards are not supported.
- Selection of SGMII or RGMII modes occurs through PCI11414 configuration. This selection may be made via boot configuration or during runtime through Ethernet driver options. Boot configuration options include EEPROM, internal OTP configuration memory, I^2C/SMBus, or SPI configuration.
- The RGMII interface supports connections to Ethernet PHYs or to Ethernet MACs.
- The SGMII interface supports connections to Ethernet PHYs, Ethernet MACs, or Small form-factor pluggable (SFP) Modules.
- PCI11414 includes an MDIO sideband interface for Ethernet PHY configuration and management.
- The interface can support a wide range of PHYs, including (but not limited to) the following popular interface standards:
  - 10BASE-T
  - 10/100BASE-T
  - 10/1000/1000BASE-T
  - 2.5GBASE-T
  - 10BASE-T1S
  - 100BASE-T1
  - 1000BASE-T1

Note: Consult *AN4754 Using Microchip Bridge Controllers with External Ethernet PHYs* for additional details on the operation and software requirements of external PHY devices.

6.1 MDIO and Sideband Control/Indication

- The MDIO (Management Data Input/Output) interface is the PHY sideband management. It is strongly recommended to implement MDIO connections with the PHY whenever possible as it enables simple PHY reconfigurability and debug capability. Without MDIO implemented, alternate means must be used to configure and troubleshoot external PHY devices. Additional sideband control I/O for the PHY is also included. See Table 6-1.

TABLE 6-1: MDIO AND SIDEBAND CONTROL PIN MAPPING

Name	Pin		Description
	PROG	Pin	
ENET_MDC	46	65	Ethernet MDIO Clock (output) The clock rate is selectable: • 25 MHz (40 ns period) • 12.5 MHz (80 ns period) • 5 MHz (200 ns period) • 2.5 MHz (400 ns period) – Standard/default setting • 1.25 MHz (800 ns period) See **Note 1**.

Note 1: MDIO and PHY sideband control signals are not used for MAC-to-MAC connections or with SFP connections. If any of these pins are not used, these pins may be repurposed to perform any of the alternate functions available on the respective **PROGx** pin.

TABLE 6-1: MDIO AND SIDEBAND CONTROL PIN MAPPING (CONTINUED)

Name	Pin		Description
	PROG	Pin	
ENET_MDIO	47	66	Ethernet MDIO Data Input/Out (bidirectional signal). An external pull-up resistor to the I/O voltage is required to ensure the line stays high while idle. An external pull-up resistor value should be selected based on guidance from the PHY that is connected and the speed selected on MDC. 2.5 MHz is the typical speed selection for MDC. In that case, a pull-up resistor value of 1 kΩ is usually appropriate to balance signal edge rate and power consumption. See **Note 1**.
ENET_PHY_RESET	48	69	PHY Reset output. This pin is used to reset the PHY during initialization. It may also be used by the Ethernet driver to reset the PHY during operation (i.e.: in response to an error condition to reset the PHY into a known state). See **Note 1**.
ENET_PHY_INT_N	51	72	PHY Interrupt input. A pull-up resistor to the I/O voltage is required. See **Note 1**.
ENET_DUPLEX	49	70	Input pin which selects the Ethernet Duplex mode. This signal connects to the Duplex mode output from the partner PHY. The polarity of this pin is set via the Automatic Duplex Polarity (ADP) bit in the MAC Control Register (MAC_CR). By default: • Logic high = Partner PHY is in Full-duplex mode. • Logic low = Partner PHY is in Half-duplex mode. If the partner PHY does not have a Duplex output signal, then it is recommended that this signal should be tied high to force Full-duplex operation.
ENET_LINK	50	71	Link Status. This signal connects to the Link Status output from the external PHY. The polarity of this pin is set via the Link Status Polarity (LSP) bit in the MAC Control Register (MAC_CR). By default: • Logic high = Partner PHY has a valid Link. • Logic low = Partner PHY does not have a valid Link. If the partner PHY does not have a link output signal and no other means is used to determine the link status, then it is recommended that this signal be tied high or low to force a static “valid link” status.

Note 1: MDIO and PHY sideband control signals are not used for MAC-to-MAC connections or with SFP connections. If any of these pins are not used, these pins may be repurposed to perform any of the alternate functions available on the respective **PROGx** pin.

6.2 RGMII

TABLE 6-2: RGMII PIN MAPPING

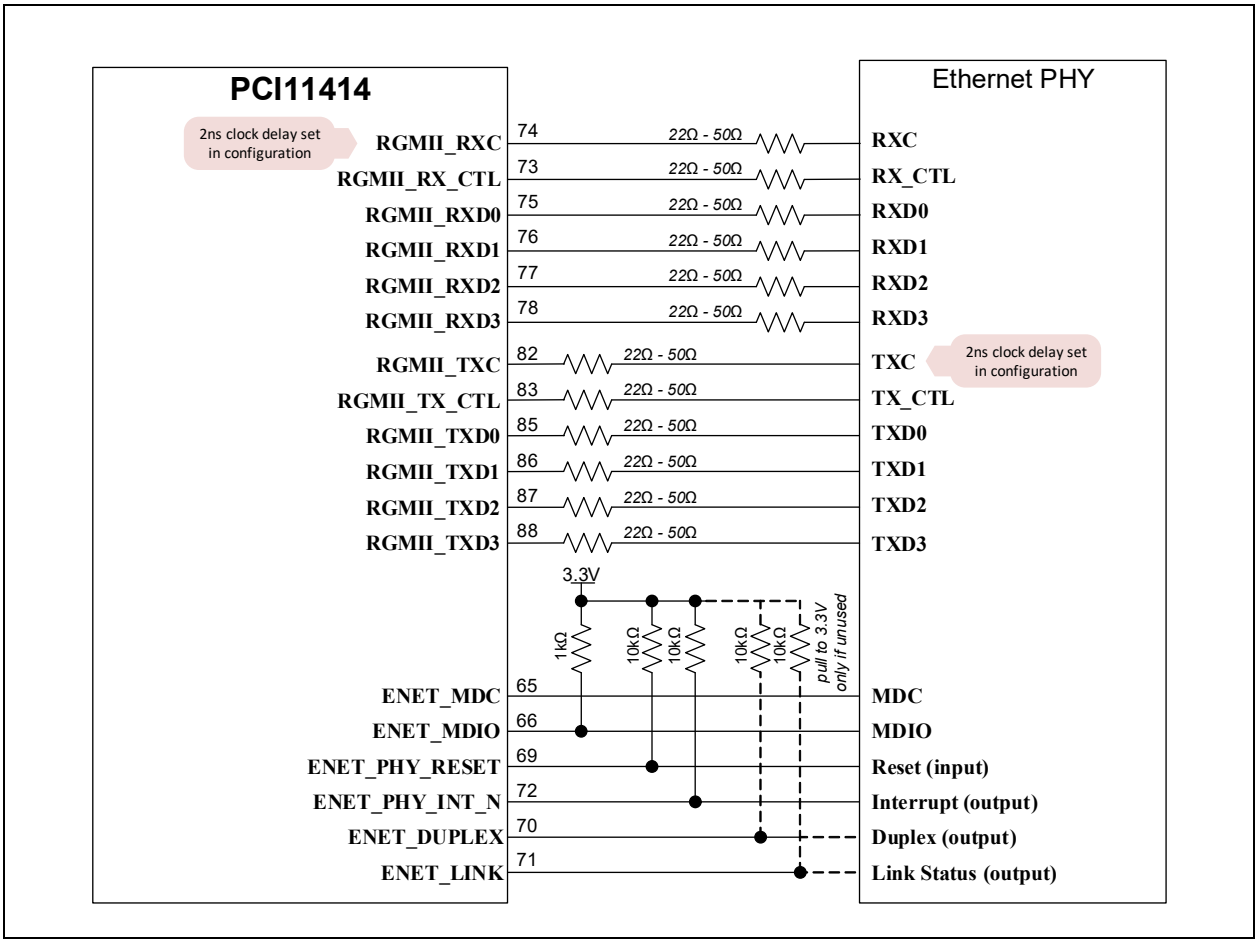
Name	Pin		Description
	PROG	Pin	
RGMII_RX_CTL	52	73	Multiplexing of Receive Data Valid and Receive Error Receive Data Valid • Asserts when received data is valid. Some preamble bits may be missed due to slight delay in assertion of the signal but must be asserted sufficiently fast to ensure that the start of frame delimiter byte is received by the MAC. Receive Error • Asserts to indicate that the received data was not properly decoded.
RGMII_RXC	53	74	Receive Signal Clock
RGMII_RXD0	54	75	Data received by MAC (transmitted by PHY) See **Note 1**.
RGMII_RXD1	55	76	
RGMII_RXD2	56	77	
RGMII_RXD3	57	78	
RGMII_TXC	58	82	Transmit Signal Clock
RGMII_TX_CTL	59	83	Multiplexing Transmit Enable and Transmit Error Transmit Enable • This signal is asserted during frame transmission. Transmit Error • This signal may be asserted during frame transmission to instruct the PHY to intentionally corrupt the frame. This is done so that the recipient of the frame will detect this packet as corrupted. This can be used as type of “frame abort” function in case a problem is detected in the midst of active frame transmission. This signal is optional per specification.
RGMII_TXD0	60	85	Data transmitted from MAC to PHY See **Note 1**.
RGMII_TXD1	61	86	
RGMII_TXD2	62	87	
RGMII_TXD3	63	88	

Note 1: It is recommended to place series termination resistors on all RGMII output pins. Refer to Figure 6-1 for output pin placement. Combined with the output pin impedance, these series resistors provide the means to tune and match the PCB trace impedance to minimize ringing, and thus improve signal integrity and reduce EMI. The typical resistor value ranges from 22Ω to 50Ω with the optimum value being dependent on the board layout. A resistor value of 33Ω can be used as the starting point for the schematic design.

6.2.1 RGMII TO ETHERNET PHY

- The most common RGMII connection is interfacing with an external Ethernet PHY device. An example is shown in Figure 6-1. Ethernet PHYs often have counter-intuitive pin naming schemes, so it is critical to closely check the pin descriptions for the selected PHY and the documentation for the PHY to ensure proper connection.
- RGMII also requires an intentional delay on the clock (relative to data) to be configured somewhere on the interconnection (typically about 2 ns). Delays can be enabled entirely within the PHY, entirely within the MAC, or through a hybrid approach with delay configured in both the PHY and the MAC. This does not impact hardware or layout design but is an important design consideration. Consult *AN4754 Using Microchip Bridge Controllers with External Ethernet PHYs* for additional detail and guidance on this topic.

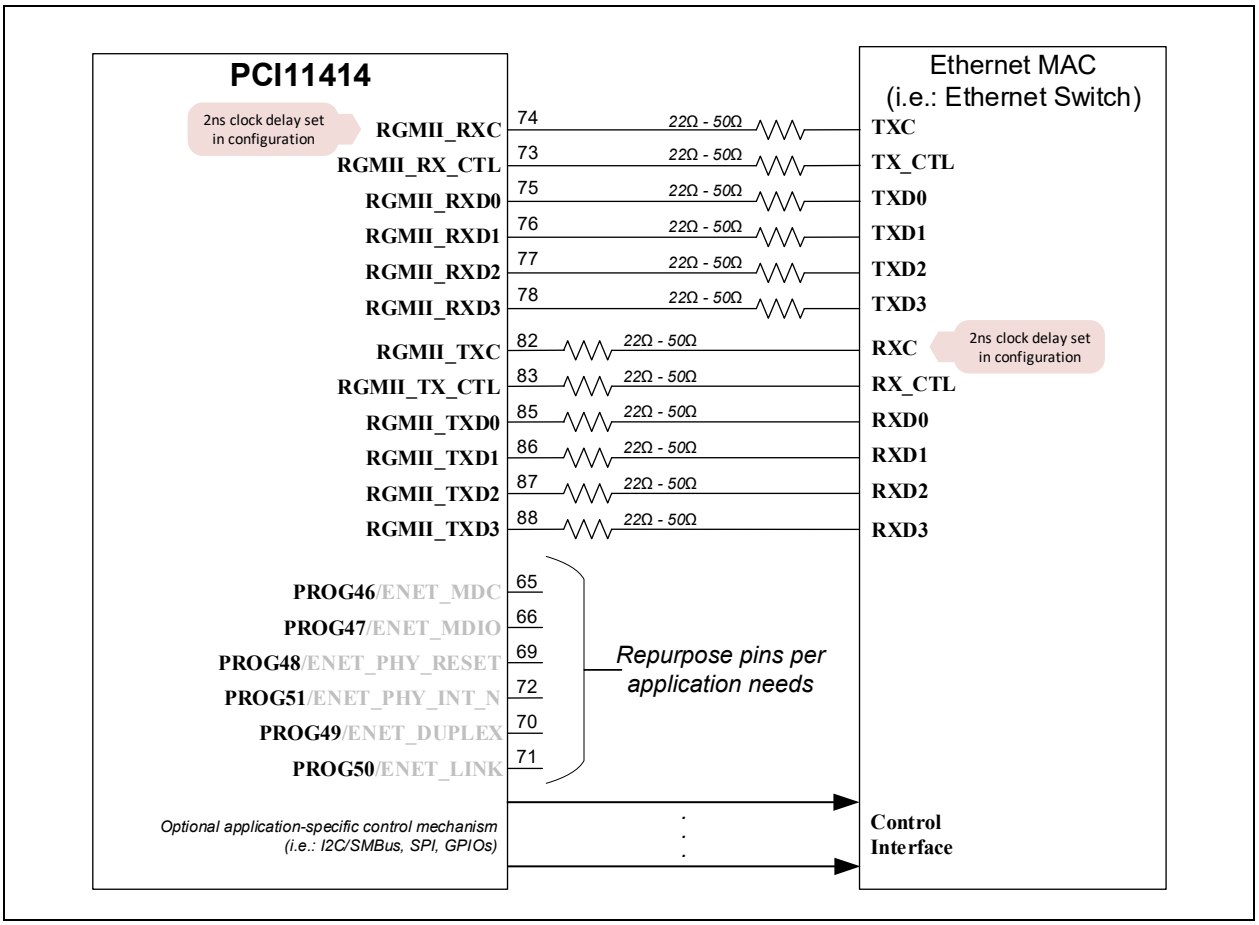
FIGURE 6-1: RGMII PHY CONNECTION



6.2.2 RGMII MAC-TO-MAC CONNECTION

- When connecting PCI11414 directly to an Ethernet switch for additional Ethernet port expansion, an Ethernet PHY is not used. Instead, the MAC of PCI11414 is connected directly to the MAC of one of the Ethernet switch ports.
- MDIO is not used for MAC-to-MAC communication. Switch configuration and management should be determined based on the options available for the selected switch (i.e.: an external memory device, via embedded processor, etc.). For simple switch configuration use-cases, a connection to one of the I^2C/SMBus or SPI interfaces of PCI11414 may be appropriate.
- RGMII also requires an intentional delay on the clock (relative to data) to be configured somewhere on the inter-connect (typically about 2 ns). In a MAC-to-MAC connection, these delay settings must be configured in one or both MACs. This does not impact hardware or layout design but is an important design consideration. Consult *AN4754 Using Microchip Bridge Controllers with External Ethernet PHYs* for additional details and guidance on this topic.
- Both MACs in the connection should be statically configured for the desired speed setting. Auto Negotiation should be disabled in both MACs for reliable operation. See Figure 6-2.

FIGURE 6-2: RGMII MAC-TO-MAC CONNECTION



6.3 SGMII

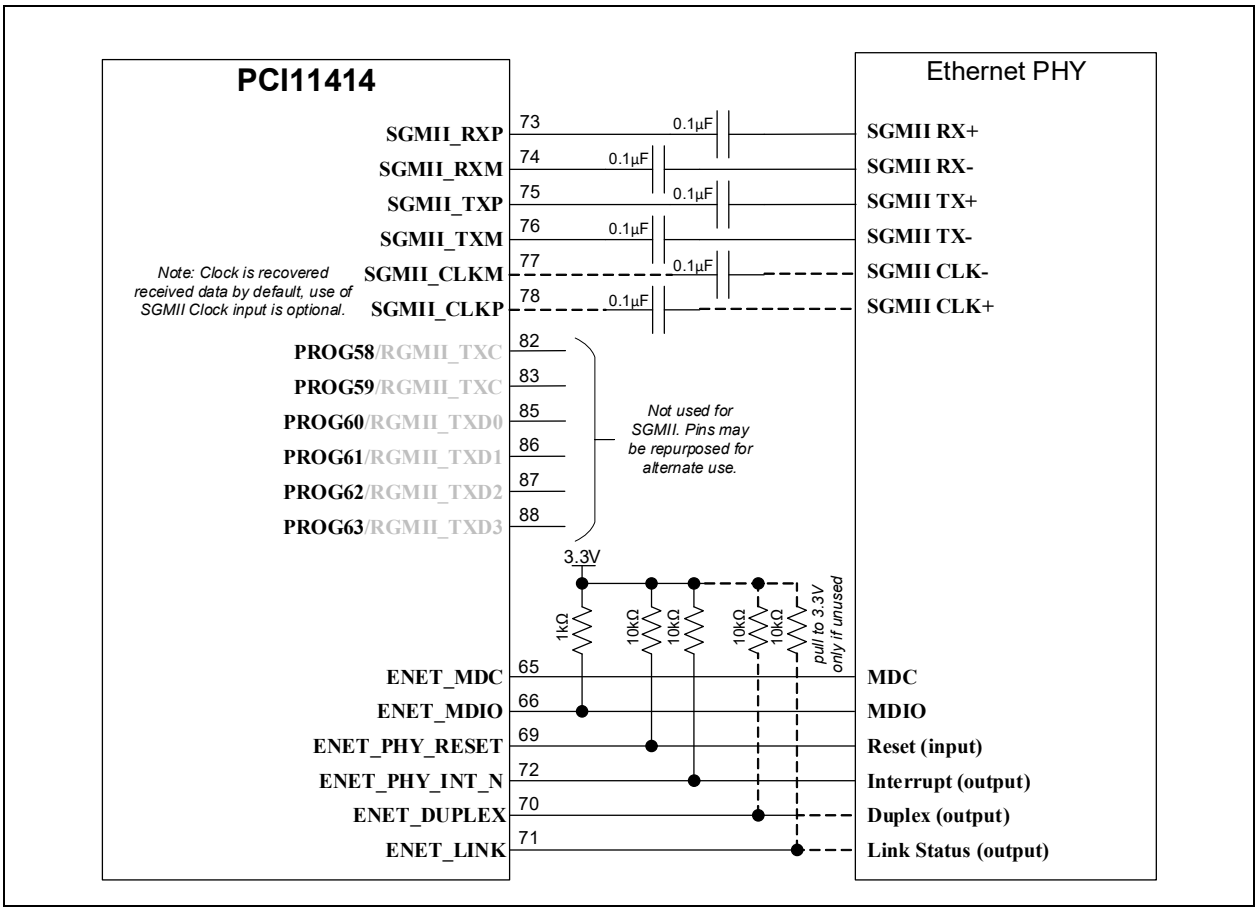
TABLE 6-3: SGMII PIN MAPPING

Name	Pin		Description
	PROG	Pin	
SGMII_RXP	52	73	SGMI Receiver Differential Pair (Data from PHY to MAC direction)
SGMII_RXM	53	74	
SGMII_TXP	54	75	SGMI Transmitter Differential Pair (Data from MAC to PHY direction)
SGMII_TXM	55	76	
SGMII_CLKM	56	77	SGMI Clock Differential Pair (Input). Using the SGMII Clock differential pair is optional, as the PCI11414 is capable of recovering the clock from the signal received on **RX**, and this is the default setting for the PCI11414 devices.
SGMII_CLKP	57	78	

6.3.1 SGMII CONNECTION TO ETHERNET PHY

- The most common SGMII connection is interfacing with an external Ethernet PHY device. An example is shown in Figure 6-3. Ethernet PHYs often have counter-intuitive pin naming schemes, so it is critical to closely check the pin descriptions for the selected PHY and the documentation for the PHY to ensure proper connection.
- SGMII signals require 0.1 µF DC blocking capacitors in series to eliminate the DC component of the signal before it arrives to the link partner's receiver pins.
- If operating at 2.5 Gbps, both the MAC and PHY should be statically configured for that speed as there is no standard mechanism to auto detect and select between 1 Gbps and 2.5 Gbps.
- If operating at 10/100/1000 Mbps speeds, auto-negotiation should be left enabled (typically the default setting) in both the MAC and PHY.

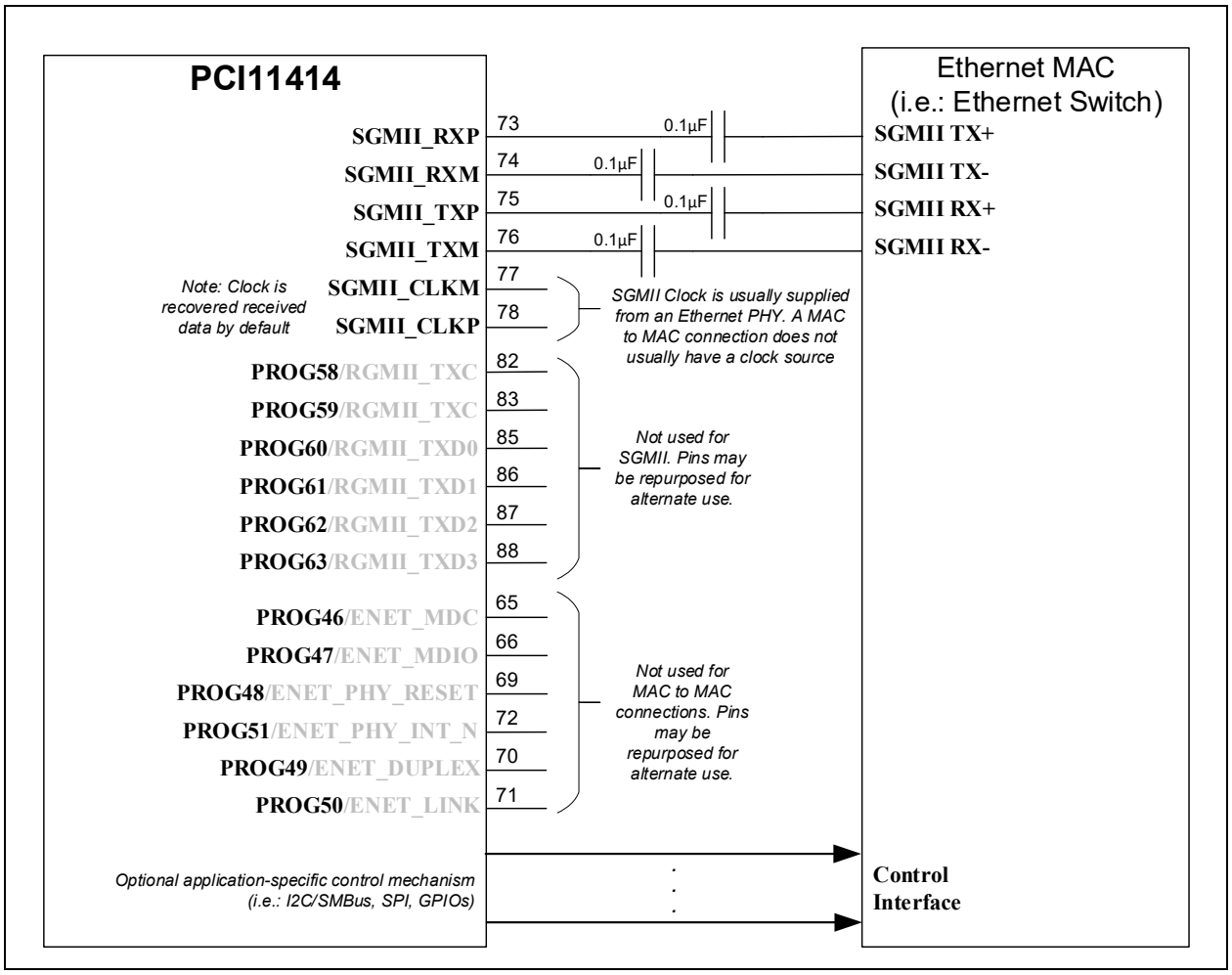
FIGURE 6-3: SGMII PHY CONNECTION



6.3.2 SGMII MAC-TO-MAC CONNECTION

- When connecting PCI11414 directly to an Ethernet switch for additional Ethernet port expansion, an Ethernet PHY is not used. Instead, the MAC of PCI11414 is connected directly to the MAC of one of the Ethernet switch ports. See Figure 6-4.
- SGMII signals require 0.1 µF DC blocking capacitors in series to eliminate the DC component of the signal before it arrives to the link partner's receiver pins.
- Switch configuration and management should be determined based on the options available for the selected switch (i.e.: an external memory device, via embedded processor, etc.). For simple switch configuration use cases, a connection to one of the I^2C/SMBus or SPI interfaces of PCI11414 may be appropriate.
- Both MACs in the connection should be statically configured for the desired speed setting. Auto Negotiation should be disabled in both MACs for reliable operation.

FIGURE 6-4: SGMII MAC-TO-MAC CONNECTION



6.3.3 SGMII CONNECTION TO SFP MODULE

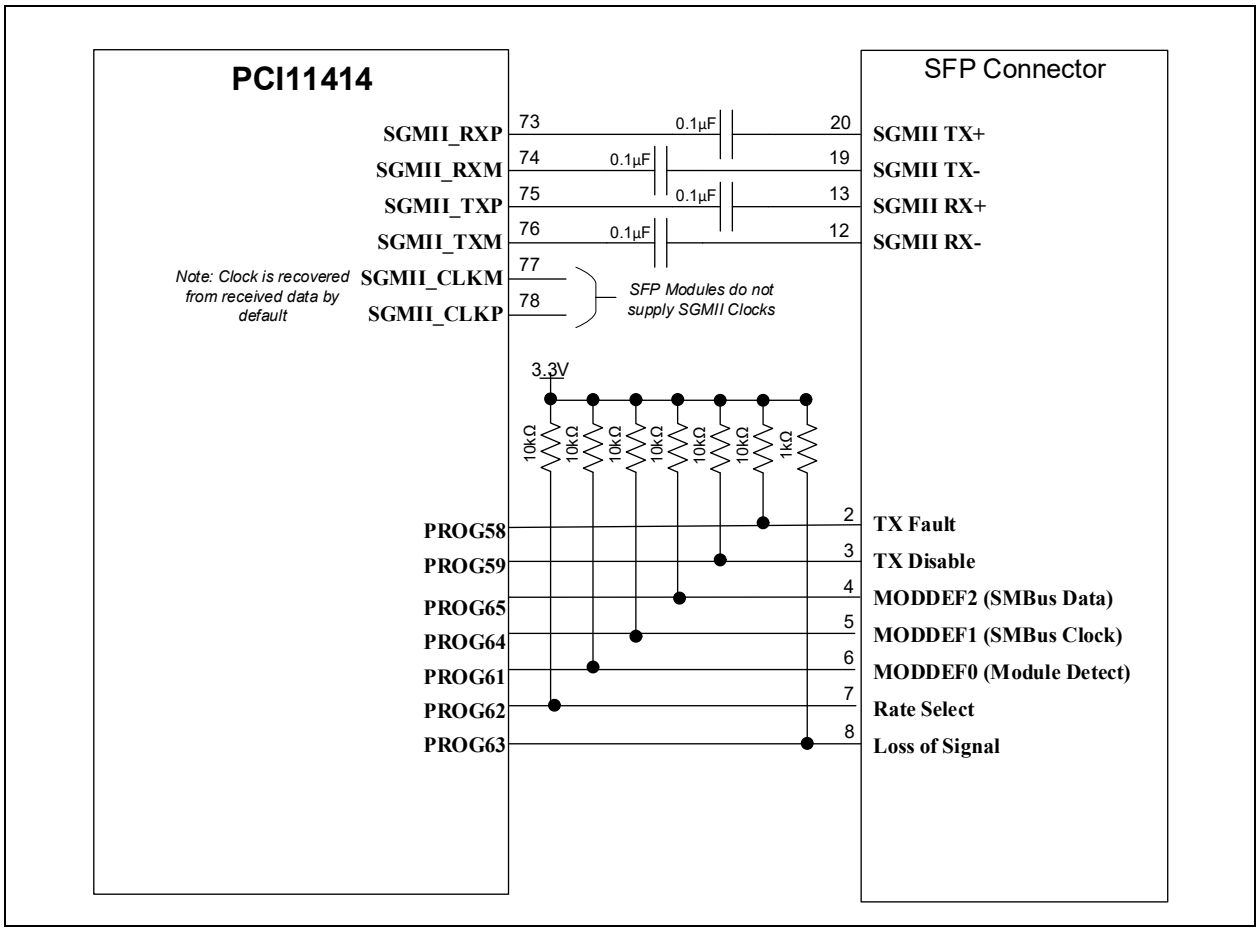
- An SFP module allows for the end user to select from a range of different speeds and media through insertion of different pluggable modules. This enables direct SERDES connections (DAC cables), copper Ethernet connections, or optical Ethernet connections to be supported by the same hardware via end-user-swappable modules.
- SFP uses SGMII, digital I/O, and a sideband SMBus/I^2C interface for management (MDIO is not used). Therefore, the PCI11414 must be configured appropriate to ensure the necessary additional I/O required for implementing SFP is configured properly. See Table 6-4.
- For SFP implementations, the PCI11414 should be statically configured for that speed aligns with the inserted module. This can be done during runtime via driver configuration options.

An example of an SFP implementation is shown in Figure 6-5.

TABLE 6-4: SFP CONNECTOR SIDEBAND I/O

Signal Name	Description	PCI11414 I/O Options
TX Fault	1 = Fault 0 = Normal Operation	Any available standard GPIO is capable of carrying out this role. Actual supported options depend on Ethernet driver implementation. Consult the latest driver release notes for the selected OS(es) to verify whether this I/O is supported natively in the driver and which pin options are supported.
TX Disable	1 = Transmitter Disabled 0 = Transmitter On	
Module Detect (MODDEF0)	This signal is definable by the SFP Module specification. However, the most common implementation is to use this pin as a module insertion detect function. 1 = Module Inserted 0 = Reduced Bandwidth	
Rate Select	1 = Full Bandwidth 0 = Reduced Bandwidth	
Loss of Signal	Used primarily by optical SFP modules to indicate that the signal has been lost. 1 = Optical Power below worst-case receiver 0 = Normal sensitivity	
SMBus Data (MODDEF1)	This signal is definable by the SFP Module specification. However, the most common implementation is to utilize this pin as a module insertion detect function. The SMBus interface connects to an EEPROM within the SFP module, which can read upon module initialization to discover the properties and capabilities of the module.	Any available SMBus/I^2C controller interface is capable of carrying out this role. Actual supported options depend on Ethernet driver implementation. Consult the latest driver release notes of the selected OS(es) to verify whether this I/O is supported natively in the driver and which pin options are supported.
SMBus Clock (MODDEF2)	This signal is definable by the SFP Module specification. However, the most common implementation is to use this pin as an SMBus Clock pin. The SMBus interface connects to an EEPROM with in the SFP module, which can read upon module initialization to discover the properties and capabilities of the module.	

FIGURE 6-5: SGMII SFP CONNECTION



7.0 UART

There are four UART interfaces available on the PCI11414. Each interface includes full flow control signals which may be optionally used, as well as an optional wake signal to allow for UART devices to wake the PCI11414.

Each interface can connect to one of the following:

- Direct to an embedded device
- An RS-232 Transceiver
- An RS-485 Transceiver
- An RS-422 Transceiver

In general, UART signals connect to the transceiver according to the Figure 7-1. Each transceiver may have additional requirements and connections.

Commonly, transceivers only make use of the UARTx_TXD (transmit), UARTx_RXD (receive), UARTx_RTS_N (ready to send), and UARTx_CTS_N (clear to send) signals. The other flow control and side band control signals are not as commonly used.

Consult the data sheet for the selected transceiver for additional guidance.

FIGURE 7-1: PCI11414 UART CONNECTIONS

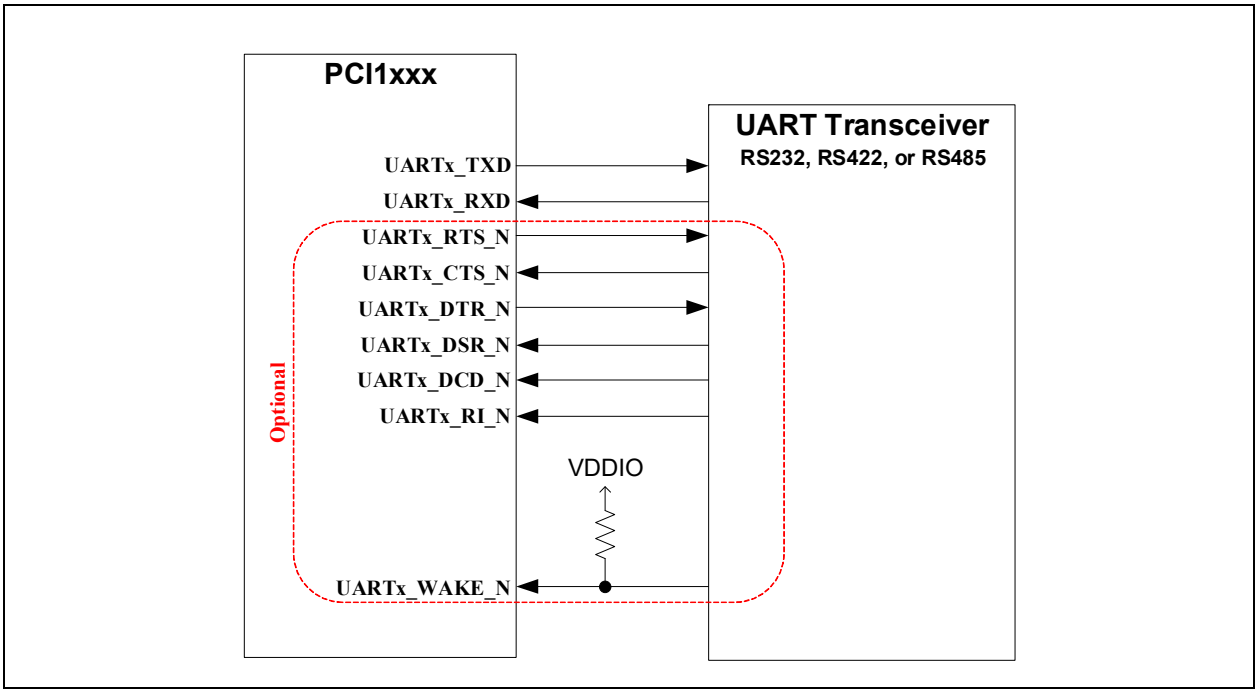


TABLE 7-1: UART0 INTERFACE PINS

Option	UART0_TXD		UART0_RXD		UART0_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	3	3	4	4	5	5
Option 2	4	4	18	32	17	31
Option 3	17	31	30	41	19	33
Option 4	29	40	70	100	31	42
Option 5	69	99	71	101	64	89
Option 6	70	100	—	—	75	148
Option 7	71	101	—	—	81	155
Option 8	—	—	—	—	83	157
Option	**UART0_CTS_N**		**UART0_DTR_N**		**UART0_DSR_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	6	7	31	42	8	9
Option 2	18	32	7	8	17	31
Option 3	20	34	17	31	18	32
Option 4	32	43	19	33	20	34
Option 5	65	90	21	35	29	40
Option 6	71	101	64	89	32	43
Option 7	76	149	75	148	65	90
Option 8	82	156	81	155	76	149
Option 9	—	—	83	157	82	156
Option	**UART0_DCD_N**		**UART0_RI_N**		**UART0_WAKE_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	9	10	10	11	6	7
Option 2	18	32	19	33	20	34
Option 3	30	41	31	42	31	42
Option 4	—	—	—	—	68	93
Option 5	—	—	—	—	69	99
Option 6	—	—	—	—	75	148
Option 7	—	—	—	—	78	151
Option 8	—	—	—	—	85	159

TABLE 7-2: UART1 INTERFACE PINS

Option	UART1_TXD		UART1_RXD		UART1_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	5	5	6	7	19	33
Option 2	31	42	32	43	33	44
Option 3	69	99	70	100	81	155
Option 4	77	150	78	151	—	—
Option 5	81	155	82	156	—	—
Option 6	86	160	87	162	—	—
Option	**UART1_CTS_N**		**UART1_DTR_N**		**UART1_DSR_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	20	34	19	33	20	34
Option 2	30	41	33	44	34	45
Option 3	34	45	46	65	47	66
Option 4	71	101	71	101	82	156
Option 5	82	156	81	155	—	—
Option	**UART1_DCD_N**		**UART1_RI_N**		**UART1_WAKE_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	48	69	49	70	29	40
Option 2	—	—	—	—	32	43
Option 3	—	—	—	—	50	71
Option 4	—	—	—	—	68	93
Option 5	—	—	—	—	69	99
Option 6	—	—	—	—	70	100
Option 7	—	—	—	—	83	157
Option 8	—	—	—	—	86	160

TABLE 7-3: UART2 INTERFACE PINS

Option	UART2_TXD		UART2_RXD		UART2_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	7	8	8	9	21	35
Option 2	17	31	18	32	31	42
Option 3	64	89	65	90	46	65
Option 4	86	160	87	162	—	—
Option	**UART2_CTS_N**		**UART2_DTR_N**		**UART2_DSR_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	22	36	21	35	22	36
Option 2	32	43	31	42	32	43
Option 3	47	66	46	65	47	66
Option	**UART2_DCD_N**		**UART2_RI_N**		**UART2_WAKE_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	0	164	2	2	64	89
Option 2	1	1	34	45	71	101
Option 3	33	44	62	87	79	152
Option 4	61	86	63	88	80	153
Option 5	60	85	87	162	87	162
Option 6	85	159	—	—	—	—
Option 7	86	160	—	—	—	—

TABLE 7-4: UART3 INTERFACE PINS

Option	UART3_TXD		UART3_RXD		UART3_RTS_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	9	10	10	11	23	38
Option 2	19	33	20	34	48	69
Option 3	66	91	67	92	—	—
Option	**UART3_CTS_N**		**UART3_DTR_N**		**UART3_DSR_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	24	39	23	38	24	39
Option 2	49	70	48	69	49	70
Option	**UART3_DCD_N**		**UART3_RI_N**		**UART3_WAKE_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**pin**
Option 1	0	164	2	2	79	152
Option 2	1	1	34	45	80	153
Option 3	34	45	62	87	85	159
Option 4	60	85	63	88	—	—
Option 5	61	86	87	162	—	—
Option 6	85	159	—	—	—	—
Option 7	86	160	—	—	—	—

8.0 I²C/SPI CONTROLLERS

PCI11414 has one I²C/SMBus and two SPI controller interfaces available for controlling embedded devices from the PCIe host. PCI11414 is capable of supporting all of the interfaces in parallel.

Note: For guidance on I²C/SMBus and SPI configuration interfaces, see *AN5213 Configuration and Programming Options for the PCI1XXXX*.

8.1 I²C/SMBus Controller Interface

- The PCI11414 has an I²C/SMBus controller interface that can bridge PCIe commands to I²C/SMBus.
- Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient, depending on the configured interface speed and total capacitance on I²C tree.
- A pull-up voltage of 1.8V to 3.3V is supported.
- Ensure that all I²C/SMBus target devices connected to the bus have unique addresses assigned.
- Ensure that the PCI11414 and all I²C/SMBus target devices connected to the bus can support the target bus speed. See Table 8-1.

TABLE 8-1: I²C/SMBUS CONTROLLER INTERFACE PINS

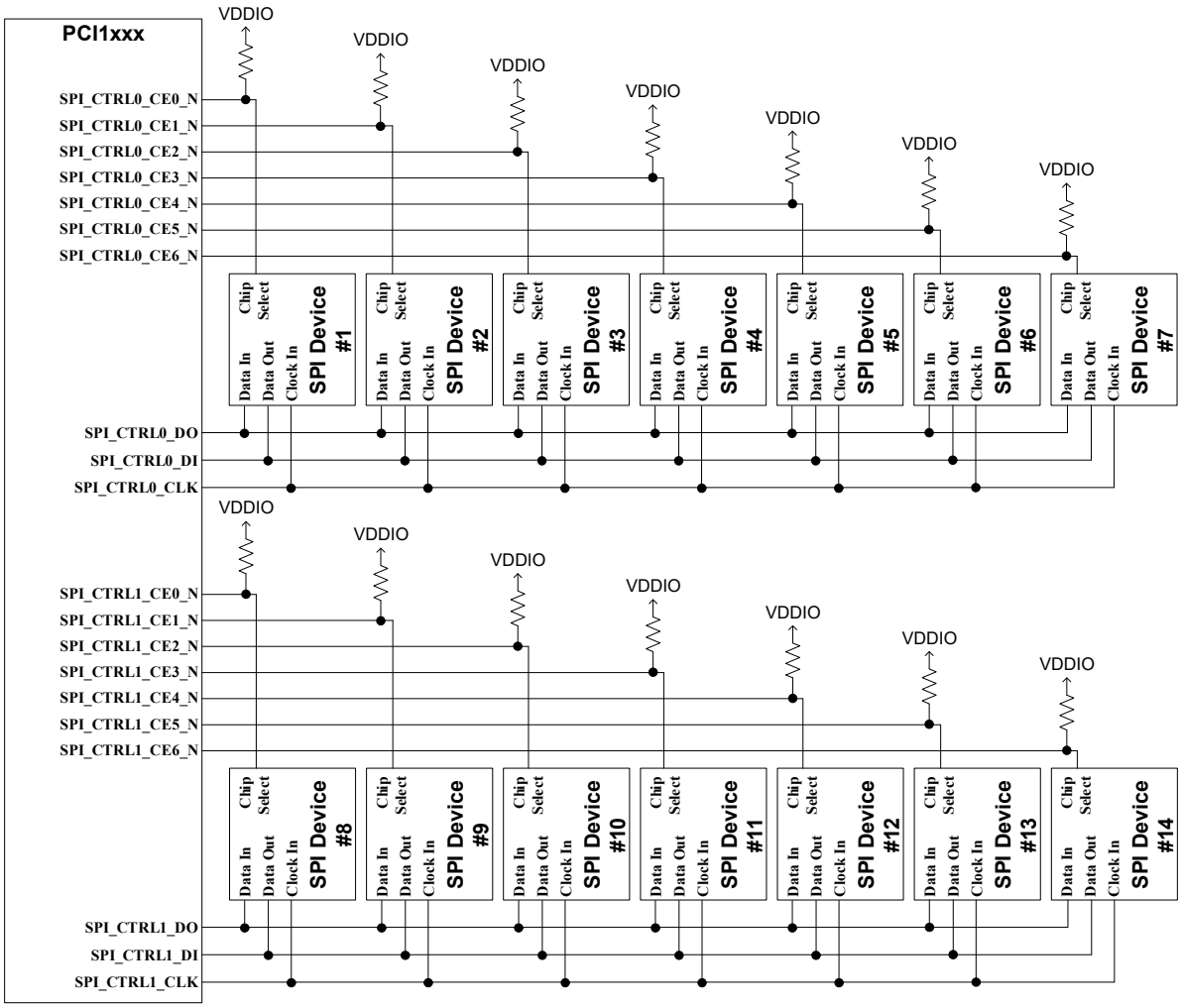
Option	SMBUS_CTLR_SCL		SMBUS_CTLR_SDA		SMBUS_CTLR_ALERT_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG0	164	PROG1	1	PROG2	2
Option 2	PROG17	31	PROG18	32	PROG3	3
Option 3	PROG32	43	PROG33	44	PROG34	45
Option 4	PROG50	71	PROG51	72	PROG66	91
Option 5	PROG64	89	PROG65	90	PROG70	100
Option 6	PROG68	93	PROG69	99	PROG78	151
Option 7	PROG76	149	PROG77	150	—	—
Option 8	PROG80	153	PROG81	155	—	—

8.2 SPI Controller Interface

- The PCI11414 has two SPI controller interfaces that can bridge PCIe commands to I^2C/SMBus. Each interface has seven separate chip select signals to support up to seven SPI devices per SPI bus.
- An I/O voltage of 1.8V to 3.3V is supported. I/O voltage is set via the **VDDVARIO** supply power pins.
- The PCI11414 SPI controller interface has a configurable signal rate and can support 2 MHz, 10 MHz, 12 MHz, 15 MHz, 20 MHz, 25 MHz, or 30 MHz operation.

A SPI controller implementation is shown in Figure 8-1.

FIGURE 8-1: PCI11414 SPI CONTROLLER



Note: The pin numbers are not reflected in the image due to the large number of pin mux options for these signals.

TABLE 8-2: SPI CONTROLLER 0 INTERFACE PINS

Option	SPI_CTRL0_DO		SPI_CTRL0_DI		SPI_CTRL0_CLK		SPI_CTRL0_CE0_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG4	4	PROG5	5	PROG3	3	PROG6	7
Option 2	PROG18	32	PROG19	33	PROG17	31	PROG7	8
Option 3	PROG47	66	PROG48	69	PROG46	65	PROG10	11
Option 4	PROG65	90	PROG66	91	PROG64	89	PROG20	34
Option 5	PROG69	99	PROG70	100	PROG71	101	PROG49	70
Option 6	PROG76	149	PROG77	150	PROG75	148	PROG67	92
Option 7	—	—	—	—	—	—	PROG68	93
Option 8	—	—	—	—	—	—	PROG78	151
Option	**SPI_CTRL0_CE1_N**		**SPI_CTRL0_CE2_N**		**SPI_CTRL0_CE3_N**		**SPI_CTRL0_CE4_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	PROG7	8	PROG0	164	PROG1	1	PROG32	43
Option 2	PROG17	31	PROG2	2	PROG24	39	PROG46	65
Option 3	PROG21	35	PROG23	38	PROG32	43	PROG60	85
Option 4	PROG31	42	PROG58	82	PROG33	44	PROG61	86
Option 5	PROG51	72	PROG59	83	PROG59	83	PROG62	87
Option 6	PROG58	82	PROG80	153	PROG60	85	PROG64	89
Option 7	PROG69	99	PROG81	155	PROG82	156	PROG68	93
Option 8	PROG79	152	PROG83	157	—	—	PROG83	157
Option 9	PROG80	153	—	—	—	—	—	—
Option	**SPI_CTRL0_CE5_N**		**SPI_CTRL0_CE6_N**					
	PROG	**Pin**	**PROG**	**Pin**				
Option 1	PROG33	44	PROG62	87				
Option 2	PROG46	65	PROG63	88				
Option 3	PROG61	86	PROG79	152				
Option 4	PROG62	87	—	—				
Option 5	PROG70	100	—	—				

TABLE 8-3: SPI CONTROLLER 1 INTERFACE PINS

Option	SPI_CTRL1_DO		SPI_CTRL1_DI		SPI_CTRL1_CLK		SPI_CTRL1_CE0_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG8	9	PROG9	10	PROG7	8	PROG32	43
Option 2	PROG30	41	PROG31	42	PROG29	40	PROG67	92
Option 3	PROG65	90	PROG66	91	PROG64	89	PROG78	151
Option 4	PROG76	149	PROG77	150	PROG75	148	—	—
Option	**SPI_CTRL1_CE1_N**		**SPI_CTRL1_CE2_N**		**SPI_CTRL1_CE3_N**		**SPI_CTRL1_CE4_N**	
	PROG	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**	**PROG**	**Pin**
Option 1	PROG18	32	PROG0	164	PROG1	1	PROG2	2
Option 2	PROG33	44	PROG24	39	PROG33	44	PROG47	66
Option 3	PROG51	72	PROG58	82	PROG59	83	PROG60	85
Option 4	PROG58	82	PROG59	83	PROG60	85	PROG61	86
Option 5	PROG79	152	PROG68	93	PROG61	86	PROG63	88
Option 6	—	—	PROG80	153	PROG69	99	PROG83	157
Option 7	—	—	—	—	PROG82	156	—	—
Option	**SPI_CTRL1_CE5_N**		**SPI_CTRL1_CE6_N**					
	PROG	**Pin**	**PROG**	**Pin**				
Option 1	PROG47	66	PROG62	87				
Option 2	PROG61	86	PROG63	88				
Option 3	PROG62	87	PROG64	89				
Option 4	—	—	PROG79	152				
Option 5	—	—	PROG80	153				

9.0 GPIOS

- Every **PROGx** pin (PROG0 to PROG 87) can be optionally configured as a GPIO for a custom application for the Host controller. For each **PROGx** pin, the “func0” pin mux option configures the pin for GPIO use. Other options, “func1” to “func15,” may also configure the pin for GPIO use, depending on the pin. Refer to the *PCI11414 Data Sheet* programmable pin function map for details.
- For each GPIO, it is recommended to configure a default state, which aligns with hardware requirements. Configuration options include:
  - Direction: Input or Output
  - (If Output) Output State: Drive High or Drive Low
  - Pull-up Resistor: Enable or Disable
  - Internal Pull-down Resistor: Enable or Disable
- For unused pins, it is acceptable to leave the pin as a floating input. You may optionally pull the pin down to ground via external resistor or by enabling the internal pull-down resistor.
- On PCI11414, the following **PROGx** pins are not bonded out and, therefore, unusable within an end application:
  - PROG11 – PROG16
  - PROG25 – PROG28
  - PROG35 – PROG45
  - PROG72 – PROG74

10.0 CLOCK CIRCUIT

10.1 Crystal and External Clock Connection

A 25.000 MHz (±50 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *PCI11414 Data Sheet*.

- **XTALI** (pin 95) is the clock circuit input for the PCI11414. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALO** (pin 96) is the clock circuit output for the PCI11414. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system-dependent, which are based on the total C_L specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:

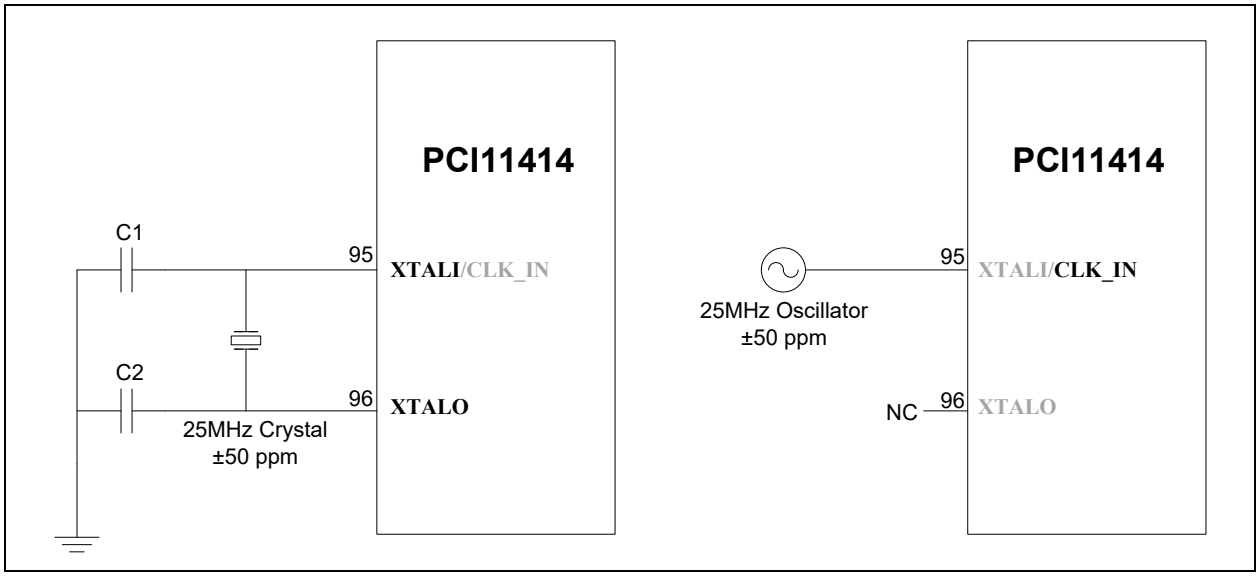
  $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$

Where, CL is the specification from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$.

Note:	C_{stray} is the stray or parasitic capacitance due to PCB layout. It can be assumed to be very small, within the 1 pF to 2 pF range, and verified by physical experiments in the laboratory if PCB simulation tools are not available.

- Alternatively, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the PCI11414. When using a single-ended clock source, **XTALO** (pin 96) should be left floating as a No Connect (NC).

FIGURE 10-1: CRYSTAL AND OSCILLATOR CONNECTIONS



11.0 POWER AND STARTUP

11.1 Board Power Supplies

11.1.1 POWER RISE TIME

- The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *PCI11414 Data Sheet*.
- If a monotonic or fast power rail rise cannot be assured, then the **RESET_N** signal should be controlled by a Reset supervisor and only released when the power rail has reached a stable level.

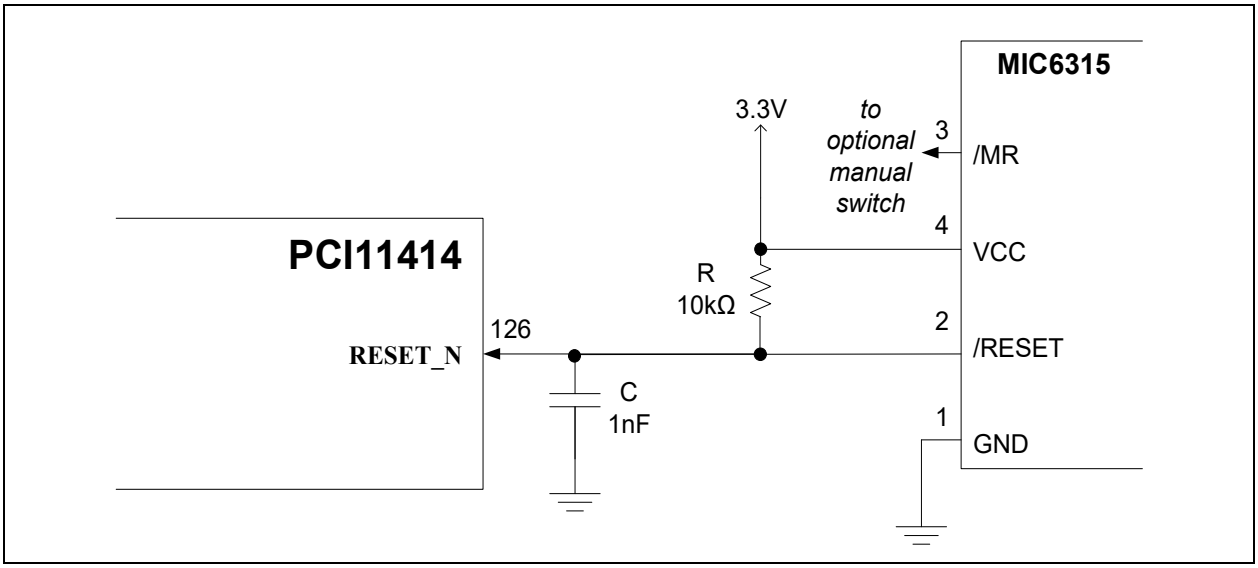
11.1.2 CURRENT CAPABILITY

- The 3.3V and 1.1V power supplies must be able to supply enough power to the USB hub IC. It is recommended that the 3.3V and 1.1V power rails be sized such that they are able to supply maximum power consumption specification as displayed in the *PCI11414 Data Sheet*.

11.2 Reset Circuit

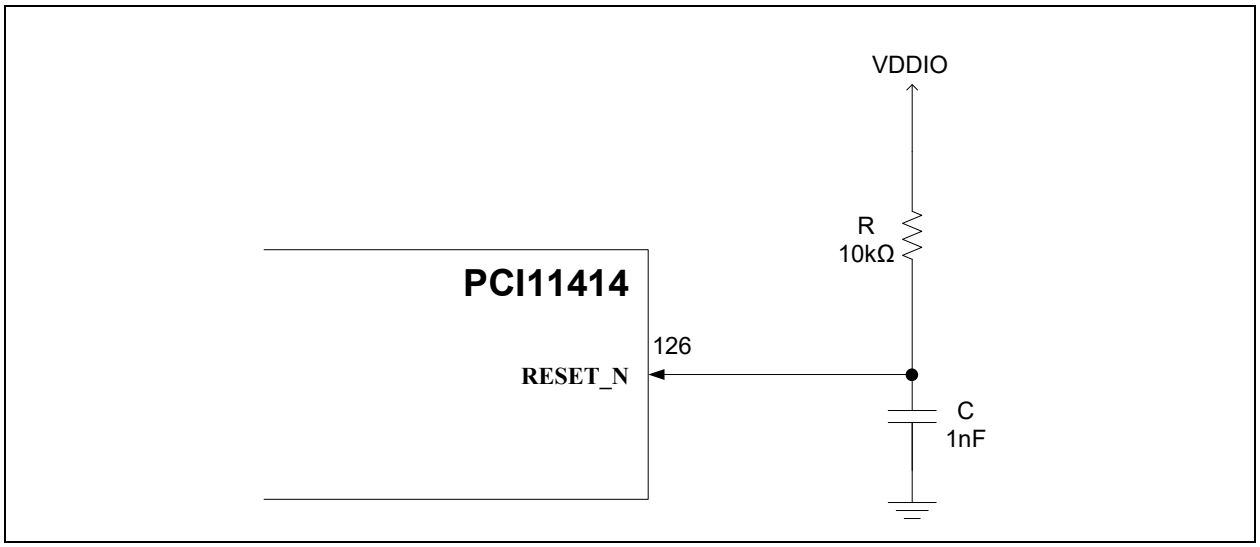
- **RESET_N** (pin126) is an active-low Reset input. This signal resets all logic and registers within the PCI11414. A hardware Reset (**RESET_N** assertion) is not required following power-up. Refer to the latest copy of the *PCI11414 Data Sheet* for Reset timing requirements.
- The best practice for managing **RESET_N** is to use an external Reset supervisor IC. A Reset supervisor can ensure that the entire system supporting the PCI11414 is properly reset following Fault and Brown-out conditions. See Figure 11-1.

FIGURE 11-1: RESET TRIGGERED BY RESET SUPERVISOR



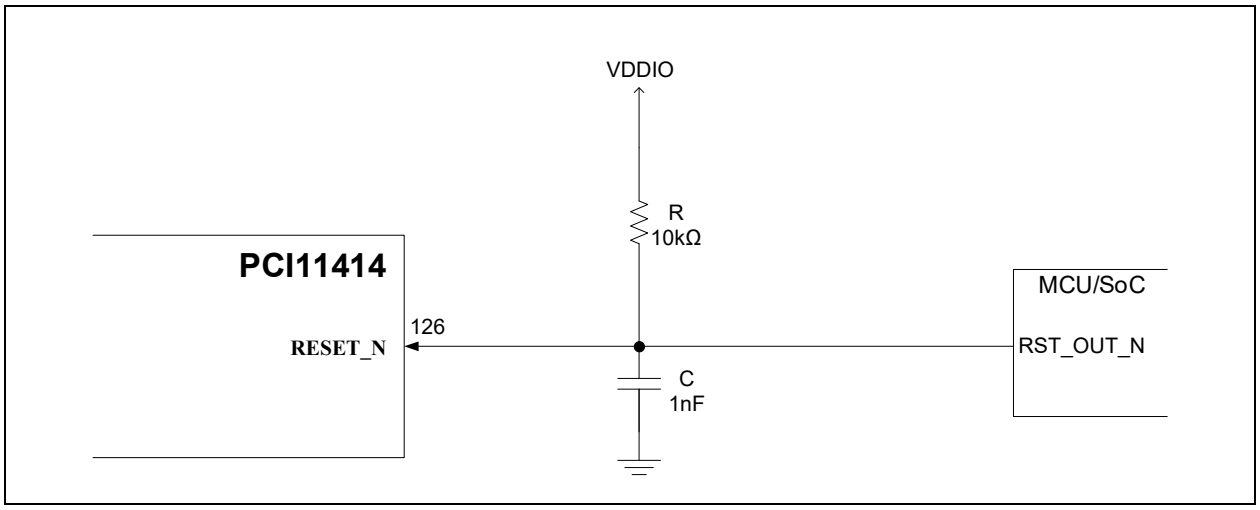
- Figure 11-2 shows a recommended Reset circuit for powering up the PCI11414 when Reset is triggered by the power supply. This implementation is lower-cost, but less robust and, therefore, may not be appropriate for many applications as it does not ensure that all system components experience a common Reset event following Fault and power brownout events.

FIGURE 11-2: RESET TRIGGERED BY POWER SUPPLY



- Figure 11-3 details the recommended Reset circuit for applications where Reset is driven by an external CPU/MCU or equivalent system management controller. The Reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm Reset after power-up.

FIGURE 11-3: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



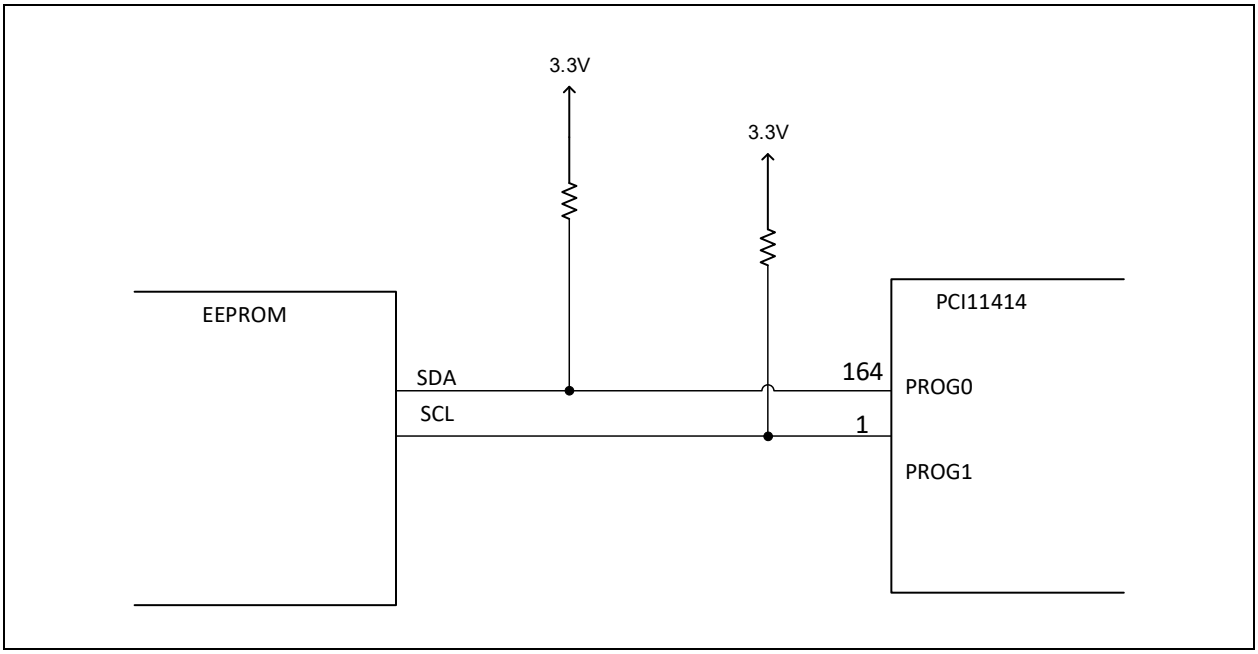
12.0 CONFIGURATION

- PCI11414 can be configured from the following sources:
  - EEPROM memory
  - External I2C/SMBus controller or SPI controller (PCI11414 cannot be configured via both interfaces.)
- PCI11414 can also be completely or partially configured via internal OTP memory.

12.1 EEPROM

- The *PCI11414 Data Sheet* maintains a list of approved compatible EEPROM memory devices. By default, the EEPROM interface expects a 32 Kbit, 1 MHz I2C EEPROM. The following strap pin detections are required at startup in order to enter I2C/SMBus Configuration mode:
  - EEPROM_STRAP_EN = 1
- If configuring via EEPROM, recommended schematic connections are shown in Figure 12-1.

FIGURE 12-1: EEPROM CONFIGURATION

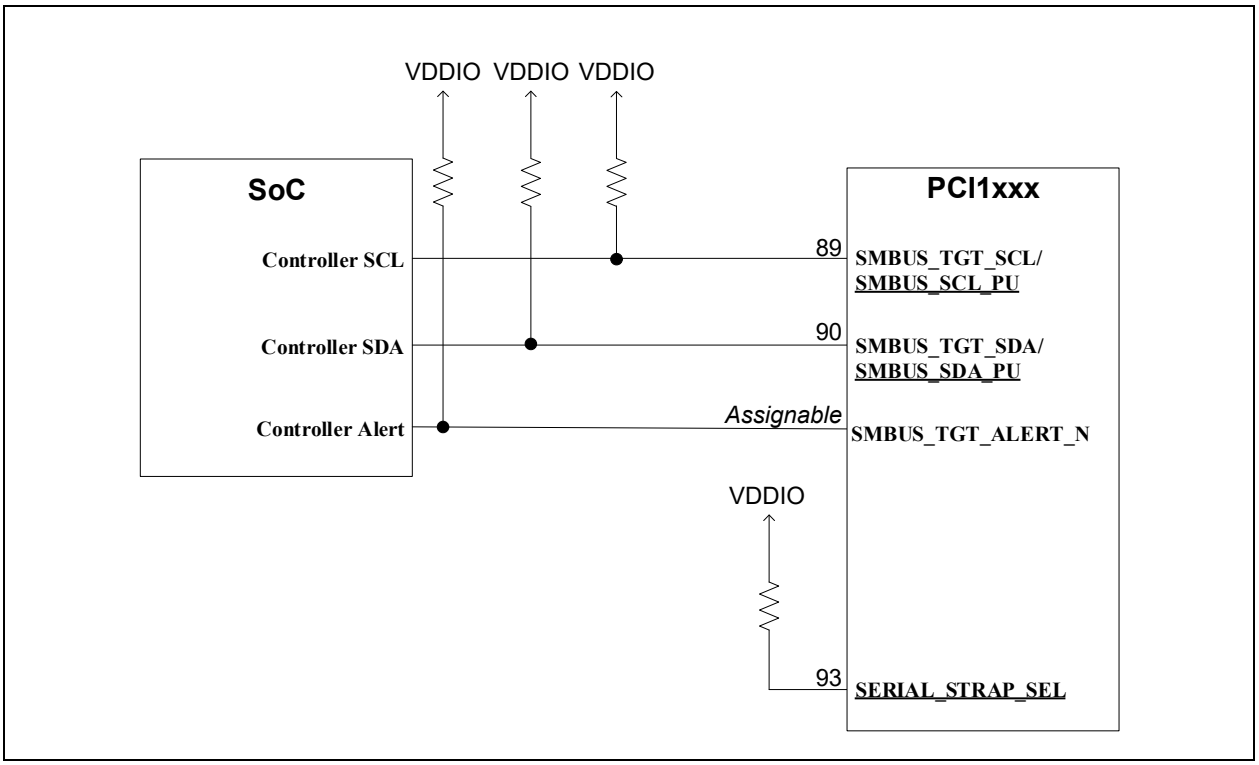


12.2 I2C/SMBus Configuration Interface

- The PCI11414 may be configured via I2C/SMBus by an embedded SoC/MCU during both the startup and runtime stages. The proper configuration straps must be detected by the PCI11414 at start-up for the I2C/SMBus interface to become active. The following strap pins detections are required at startup to enter the I2C/SMBus Configuration mode:
  - SERIAL_STRAP_EN = 1
  - SMBUS_SCL_PU = 1
  - SMBUS_SDA_PU = 1
- The interface command specification and configuration register set is described in full in the *AN4255 PCI12000/PCI11xxx Register Map* application note.
- Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient, depending on the interface speed and total capacitance on I2C tree.
- A pull-up voltage of 1.8V to 3.3V is supported.
- The target interface supports the Standard mode speed of up to 100 kHz and the Fast mode speed of 400 kHz.

A typical I2C/SMBus target implementation is shown in Figure 12-2.

FIGURE 12-2: TARGET INTERFACE



Note: If I²C/SMBus pull-up resistors are detected by the **SMBUS_SCL_PU** and **SMBUS_SDA_PU** pin straps at startup, the PCI11414 will be indefinitely configured by the attached I²C/SMBus controller. For early prototyping, it may be necessary to physically remove the pull-up resistors until the I²C/SMBus controller is fully operational and can properly configure the PCI11414 at startup.

The I²C/SMBus target clock and data pins, as well as the hardware configuration strap pins **SERIAL_STRAP_SEL**, **SMBUS_SCL_PU**, and **SMBUS_SDA_PU** are all fixed. The I²C/SMBus target alert pin is assignment to a number of **PROGx** pin options. See Table 12-1.

TABLE 12-1: I²C/SMBUS TARGET INTERFACE PINS

Option	SMBUS_TGT_SCL		SMBUS_TGT_SDA		SMBUS_TGT_ALERT_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG64	89	PROG65	90	PROG0	164
Option 2	—	—	—	—	PROG1	1
Option 3	—	—	—	—	PROG2	2
Option 4	—	—	—	—	PROG3	3
Option 5	—	—	—	—	PROG4	4
Option 6	—	—	—	—	PROG5	5
Option 7	—	—	—	—	PROG6	7
Option 8	—	—	—	—	PROG7	8
Option 9	—	—	—	—	PROG8	9
Option 10	—	—	—	—	PROG9	10
Option 11	—	—	—	—	PROG10	11
Option 12	—	—	—	—	PROG17	31

TABLE 12-1: I²C/SMBUS TARGET INTERFACE PINS (CONTINUED)

Option	SMBUS_TGT_SCL		SMBUS_TGT_SDA		SMBUS_TGT_ALERT_N	
	PROG	Pin	PROG	Pin	PROG	Pin
Option 13	—	—	—	—	PROG18	32
Option 14	—	—	—	—	PROG19	33
Option 15	—	—	—	—	PROG20	34
Option 16	—	—	—	—	PROG21	35
Option 17	—	—	—	—	PROG22	36
Option 18	—	—	—	—	PROG23	38
Option 19	—	—	—	—	PROG24	39
Option 20	—	—	—	—	PROG32	43
Option 21	—	—	—	—	PROG33	44
Option 22	—	—	—	—	PROG46	65
Option 23	—	—	—	—	PROG47	66
Option 24	—	—	—	—	PROG48	69
Option 25	—	—	—	—	PROG49	70
Option 26	—	—	—	—	PROG50	71
Option 27	—	—	—	—	PROG51	72
Option 28	—	—	—	—	PROG66	91
Option 29	—	—	—	—	PROG67	92
Option 30	—	—	—	—	PROG68	93
Option 31	—	—	—	—	PROG69	99
Option 32	—	—	—	—	PROG79	152
Option 33	—	—	—	—	PROG81	155
Option 34	—	—	—	—	PROG86	160
Option 35	—	—	—	—	PROG87	162

12.3 SPI Peripheral Interface

- The PCI11414 may be configured via SPI interface by an embedded SoC/MCU during both the startup and run-time stages. The proper configuration straps must be detected by the PCI11414 at startup for the I²C/SMBus interface to become active.
- The following strap pins detections are required at startup to enter the I²C/SMBus Configuration mode:
  - SERIAL_STRAP_EN = 1
  - SMBUS_SCL_PU = 0
  - SMBUS_SDA_PU = 0

Note: The SMBUS_SCL_PU and SMBUS_SDA_PU hardware straps share the same pins as the SPI data out and SPI clock lines. Hence, weak pull-down resistors (i.e.:100 kΩ) are recommended to minimize the effect on SPI communication.

- The interface command specification and configuration register set is described in full in *AN5213 Configuration and Programming Options for the PCI1XXXX.*
- An I/O voltage of 1.8V to 3.3V is supported. I/O voltage is set via the **VDDVARIO** supply power pins.
- The SPI Peripheral interface supports clock rate of up to 30 MHz.

A typical SPI peripheral target implementation is shown in Figure 12-3.

FIGURE 12-3: SPI PERIPHERAL INTERFACE

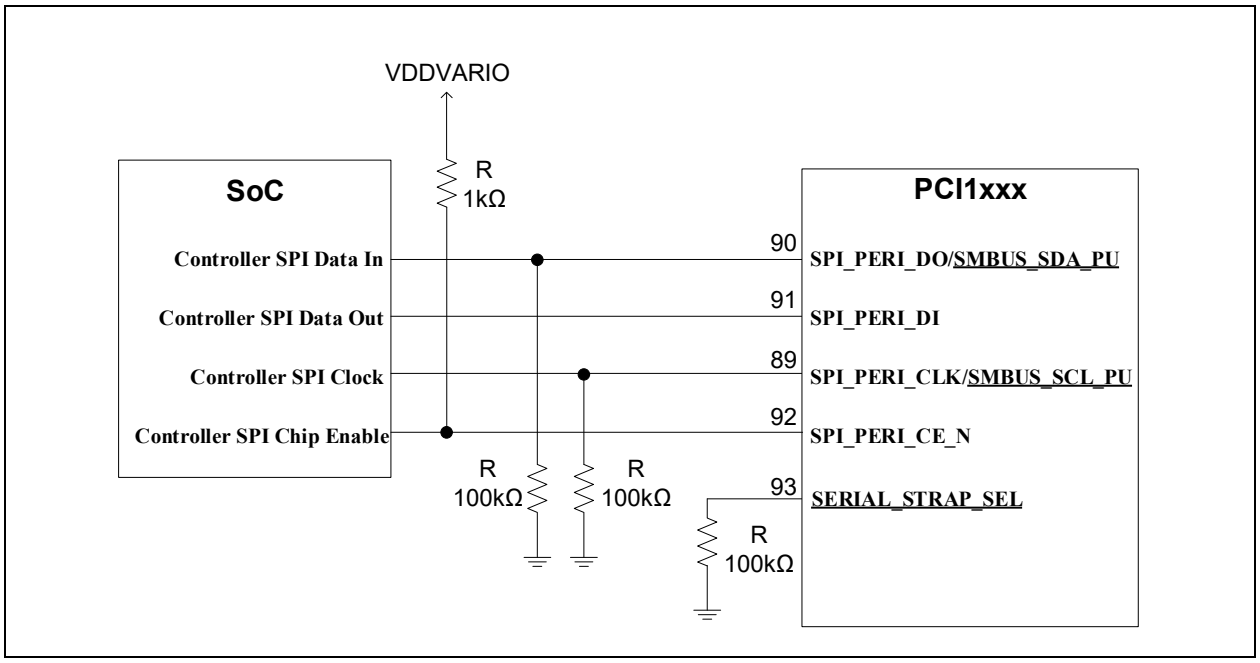


TABLE 12-2: SPI TARGET INTERFACE PINS

Option	SPI_PERI_DO		SPI_PERI_DI		SPI_PERI_CLK		SPI_PERI_CE_N	
	PROG	Pin	PROG	Pin	PROG	Pin	PROG	Pin
Option 1	PROG65	90	PROG66	91	PROG64	89	PROG67	92

13.0 MISCELLANEOUS

The PCI11414 includes several pins that are in place for manufacturing purposes. These pins are not intended for customer use but must be connected properly for reliable operation of the PCI11414. See Table 13-1 for more details.

TABLE 13-1: TEST PIN DETAILS

Pin Name	Required Connections
TESTEN	Default: Pull down to ground with a 100 kΩ resistor. JTAG enable: Pull up to 3.3V with a 10 kΩ resistor.
ENET_RESREF	Pull down to ground with a 200Ω resistor.

14.0 HARDWARE CHECKLIST SUMMARY

TABLE 14-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify that the grounds are tied together.		
Section 3.0, "Power and Bypass Capacitance"	Section 3.1, "1.1V Supplies"	Ensure all 1.1V supplies are in the range 1.08V to 1.32V, and they share one 1 µF and one 0.1 µF bulk capacitor each.		
	Section 3.2, "Variable Voltage"	Ensure **VDDVARIO** is in the range 1.8V to 3.3V, and they share one 1 µF and one 0.1 µF bulk capacitor.		
	Section 3.3, "3.3V Supplies"	Ensure **VDD33** is within the range of 3.0V to 3.6V, and a 0.1 µF capacitor is on each pin.		
	Section 3.4, "2.5V Supplies"	Ensure **VDD25** is within the range of 2.2V to 2.8V, and each pin has dedicated 1 nF capacitor.		
	Section 3.5, "3.3V References"	Ensure **VDD33PVTREF** and **VDD33WRPLL** are within the range of 3.0V to 3.6V with dedicated 1 nF and 0.1 µF capacitors on **VDD33PVTREF** and a dedicated 0.1 µF capacitor on **VDD33WRPLL**.		
Section 4.0, "PCIe Signals"	Section 4.1, "Upstream Port PCIe Signals"	Verify that the PCIe upstream data pins are correctly routed to the PCIe connector and the host. Pay special attention to the 0.1 µF decoupling capacitor series connecting to the corresponding transmitter and receiver pins.		
	Section 4.2, "Downstream Port PCIe Signals"	Verify that the PCIe downstream data pins of the two ports are correctly routed to the PCIe connector and host as shown in Figure 4-7 and Figure 4-8.		
Section 5.0, "USB Signals"	Section 5.1, "USB Host Ports"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 **D**+ and **D**– data lines, and do not cross the USB3 **TX** and **RX** differential pairs. If connected to a Type-C port, pay special attention to the "Side A" and "Side B" connections and ensure the routing is not crossed between the two.		
	Section 5.2, "Disabling Downstream Ports"	If any of the USB ports are unused, ensure they are properly disabled via pin strap. If pin strapping is not used, other methods may be used such as I^2C/SMBus configuration or OTP configuration.		
	Section 5.3, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance of the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB2 trace. Protection devices on USB3 traces should not add more than 0.5 pF on each line.		

TABLE 14-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
	Section 5.4, "VBUS and PRT_CTLx Connections of Downstream Ports"	Verify that **PRT_CTL1** and **PRT_CTL2** are properly connected to both the Enable pin of the downstream port power controller and the Fault indicator output of the port power controller. Ensure the port power controller current capability is sized appropriately (500 mA, 900 mA, 1.5A, or 3A) and the overcurrent threshold is set appropriately.		
		If downstream port 1, downstream port 2, or both are standard Type-C ports, verify that **DP1_CC1** and **DP1_CC2** are properly connected to the Type-C port **CC1** and **CC2** pins. The VCONN supplies must also be designed such that 1W of VCONN power can be delivered to the **CC1** or **CC2** pin when enabled by the DP1_VCONN1, DP1_VCONN2, DP2_VCONN1, and DP2_VCONN2 active-high Enable signals.		
	Section 5.5, "GND and EARTH Recommendations"	Ensure that the GND pin is connected with a low impedance path to the ground plane and the EARTH pin is connected to the GND through a 0.1 µs capacitor and a 330Ω resistor.		
Section 6.0, "Ethernet"	Section 6.1, "MDIO and Sideband Control/Indication"	Ensure all the MDIO pin connections are correct when configuring with PHY. Refer Figure 6.1 for correct pin mapping.		
	Section 6.2, "RGMII"	Verify that RGMII pin connections are correct.		
		Provide provision for the series termination resistors.		
	Section 6.3, "SGMII"	Verify that SGMII pin connections are correct. Ensure a series of 0.1 µF DC blocking capacitors are connected to the pins.		
Section 7.0, "UART"		Verify proper pin configuration. Make sure they are routed correctly to the transceiver. Refer to Figure 7-1.		
Section 8.0, "I²C/SPI Controllers"	Section 8.1, "I²C/SMBus Controller Interface"	Ensure **PROG** pins are connected correctly and pulled up to the supported pull-up voltage, 1.8V to 3.3V.		
	Section 8.2, "SPI Controller Interface"	Ensure **PROG** pins are connected correctly and pulled up to the supported pull-up voltage, 1.8V to 3.3V. Verify that the signal rate is one of the eight supported speeds (Refer to this section for the supported speeds.)		
Section 9.0, "GPIOs"		Verify that any **GPIO** pins that will be used as **GPIO**s within the application are connected properly, and never exceed the voltage maximum/minimum values, or overload the current source/sink maximum values as defined in the data sheet.		
Section 10.0, "Clock Circuit"	Section 10.1, "Crystal and External Clock Connection"	Confirm whether the crystal or clock is 25.000 MHz (±50 ppm).		
		If a single-ended clock is used, ensure it is connected to **XTALI** while leaving **XTALO** floating.		
		If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		

TABLE 14-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 11.0, "Power and Startup"	Section 11.1, "Board Power Supplies"	Verify that the board power supplies deliver 3.0 to 3.6V, and 1.08V to 1.32V to the switch power rails, and that the power-on rise time meets the requirement of the switch as defined in the data sheet.		
		If the rise time requirement cannot be met, ensure that the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 11.2, "Reset Circuit"	Ensure that the **RESET_N** signal has an external pull-up resistor, or is otherwise properly controlled by an external SoC, MCU, or Reset supervisor device.		
Section 12.0, "Configuration"	Section 12.1, "EEPROM"	Ensure that an approved compatible EEPROM device is used.		
		Verify if the following strap configuration is made at startup to enter Configuration mode: EEPROM_STRAP_EN = 1.		
	Section 12.2, "I^{2}C/SMBus Configuration Interface"	Verify if the following strap configuration is made at startup to enter Configuration mode: 1.SERIAL_STRAP_EN = 1 2.SMBUS_SCL_PU = 1 3.SMBUS_SDA_PU = 1		
	Section 12.3, "SPI Peripheral Interface"	Verify if the following strap configuration is made at startup to enter Configuration mode: 1.SERIAL_STRAP_EN = 1 2.SMBUS_SCL_PU = 0 3.SMBUS_SDA_PU = 0		
Section 13.0, "Miscellaneous"		Verify if **TESTEN** is pulled to **GND**.		
		Verify if **ENET_RESREF** is pulled to GND.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005196B (01-15-25)	Figure 3-1, Figure 4-1, Figure 4-2, Figure 4-7, Figure 4-8, Figure 5-1, Figure 5-2, Figure 5-3, Figure 5-4, Figure 5-5, Figure 6-1, Figure 6-2, Figure 6-4, Figure 6-5, and Figure 12-1	Corrected pin numbers.
	Section 5.4, "VBUS and PRT_CTLx Connections of Downstream Ports"	Changed the statement, “This pin must be connected per this guidance and may not be left floating or unused,” to “When the downstream port is used as a USB Type C® port, this pin must be connected per this guidance and may not be left floating or unused. When the downstream port is used as a Type A port, the VBUS_MON_Px pin can be left floating.”
	Section 12.1, "EEPROM"	Changed “SERIAL_STRAP_EN” to “EEPROM_STRAP_EN.”
	Table 5-2, Table 7-2, and Table 7-4	Updated pin information.
	All	Updated pin numbers in figures and their respective descriptions. Made minor updates and formatting changes throughout the document.
DS00005196A (12-19-23)	Initial release	

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