AN6029

PCB Layout Guidelines for Microchip PCI1xxxx PCIe® Switches

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1.0 INTRODUCTION

This application note is intended to provide general guidance for printed circuit board (PCB) layout suitable for Microchip's PCI12000/PCI11414/PCI11400/PCI11101/PCI11010 Peripheral Component Interface Express or PCIe® switches with integrated USB 3.2 Gen 2 Host Controller, Ethernet MAC, and Programmable I/O.

The topics outlined in this document are aimed towards PCB designers and developers who have the appropriate understanding of PCB design rules, such as component placement, signal routing, power and ground filtering and bypassing, as well as thermal management.

The material presented in this document was created to assist designers by detailing reference documentation and links that support the demands of Microchip's highly flexible PCIe switch, USB, Ethernet, and other related interfaces.

1.1 Sections

This document covers the following topics:

- Section 3.0, PCB Layout Guidelines
- Section 4.0, Component Placement
- Section 5.0, Power and Ground Distribution
- Section 6.0, Skew-Compensating Footprints
- Section 7.0, Miscellaneous

1.2 References

The following documents should be referenced when using this application note:

- *PCI11414 PCIe Switch with Integrated USB 3.2 Gen 2 Host Controller + Ethernet MAC & Programmable I/O*
- *PCI12000 3-Port PCIe Switch with Integrated Programmable I/O*
- *PCI11010 PCIe Switch with Integrated Ethernet MAC & Programmable I/O*
- *PCI11101 PCIe Switch with Integrated USB 3.2 Gen 2 Host Controller & Programmable I/O*
- *PCI11400 PCIe Switch with Integrated USB 3.2 Gen 2 Host Controller & Programmable I/O*
- *AN 26.2 Implementation Guidelines for Microchip USB 2.0 and 3.1 Gen 1 Hub Devices Application Note*
- *AN 18.15 PCB Design Guidelines for QFN and DQFN Packages Application Note*

2.0 OVERVIEW

Microchip's PCIe switches require a robust PCB platform to ensure reliable operation. All switches contain a mix of sensitive analog circuitry, digital core logic, and high-speed I/O circuitry.

General recommendations and guidelines, such as component placement and layer stack-up, are covered in *AN 26.2 Implementation Guidelines for Microchip USB 2.0 and 3.1 Gen 1 Hub Devices Application Note*. In addition, the document details additional subsystem issues, such as high-speed signaling/impedance, crystal connections, and other critical circuits. Moreover, controlling EMI, system power distribution, and signal return path management are addressed in the document. Design guidelines and packages are discussed in *AN1815 PCB Design Guidelines for QFN and DQFN Packages Application Note*.

3.0 PCB LAYOUT GUIDELINES

Design, placement, routing recommendations, and techniques depend on the high-speed interfaces selected for the user's application.

3.1 Supported Interfaces

The interfaces supported by Microchip PCIe Gen 4 switches and the approximate length matching and length and width limits for those interfaces are outlined in Table 1.

TABLE 1: APPROXIMATE LIMITS FOR SUPPORTED INTERFACES

Interface	Impedance Zdiff or Z0	Typical Line Width (w) / Spacing (s)	Approximate Length Limit (on 370HR)	Within-Pair Length Matching	Within-Group Length Matching
High-Speed					
PCIe® Gen 4	85Ω	8/6	3 inches/75 mm	5 mil/0.125 mm	N/A
USB3.2 Gen 2	85Ω	8/6	4 inches/100 mm	5 mil/0.125 mm	N/A
Mid-Speed					
RGMII	50Ω	7 width	6 inches/150 mm	N/A	100 mil/2.5 mm
SGMII	100Ω	7/5	3 inches/75 mm	25 mil/0.6 mm	100 mil /2.5 mm
USB2	85Ω	8/6	10 inches/250 mm	200 mil/5 mm	N/A
Low-Speed					
UART	50Ω	7 width	12 inches/300 mm	N/A	1 in/25 mm
JTAG	50Ω	7 width	6 inches/150 mm	N/A	200 mil/5 mm
SPI	50Ω	7 width	6 inches/150 mm	N/A	200 mil/5 mm
EEPROM	50Ω	7 width	12 inches/300 mm	N/A	500 mil/12 mm

Note 1: The shorter the line lengths for high-speed interfaces, the better. The approximate limits provided in this table are based on a PCB fabricated using a 370HR FR-4 material. The use of lower-loss PCB materials, such as FR408HR or I-Tera MT40, allows for longer trace lengths.

4.0 COMPONENT PLACEMENT

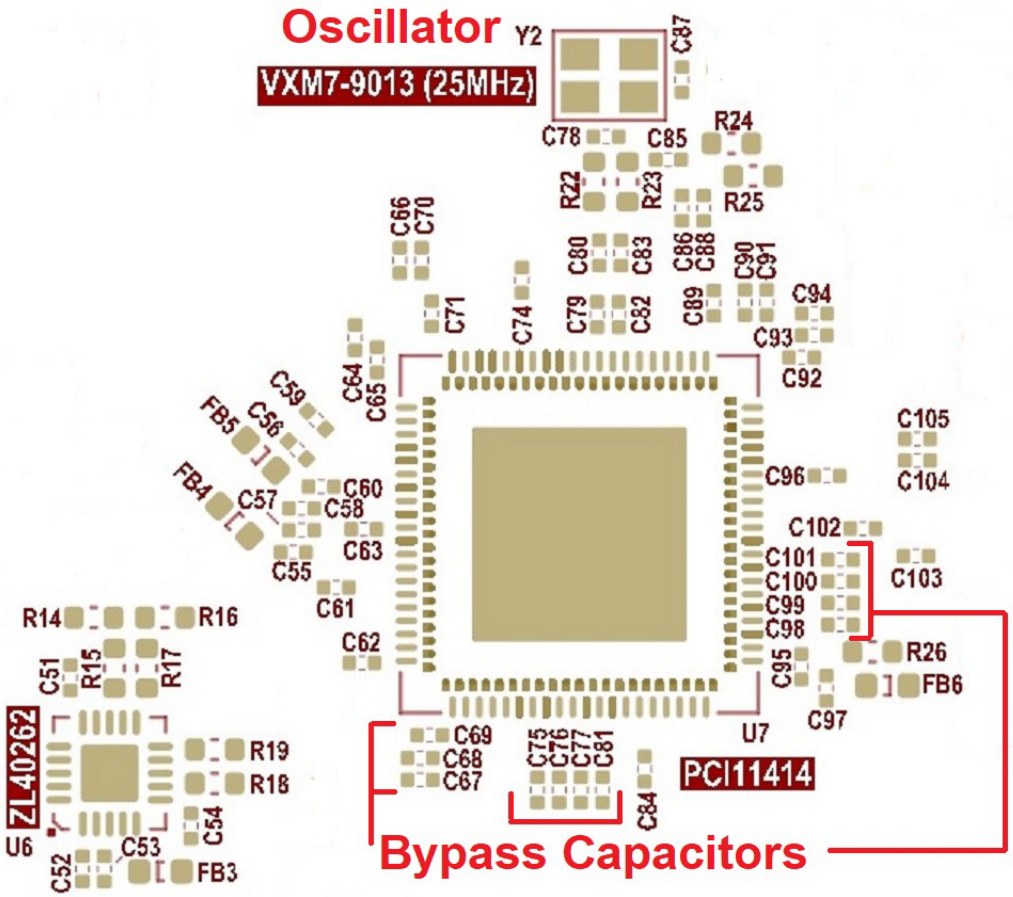
Component placement is key to a reliable PCB design. The PCB designer should strive to group components based on their function. The designer should also make a reasonable effort to separate noisy components and their return paths from sensitive analog circuits. Power supply bypassing is especially important for high-speed circuitry. Keep in mind that placement has an impact on signal routing.

General placement considerations:

- Place bypass capacitors close to their respective power pins.
- Place any series termination extremely close to the driving source.
- Place any DC blocking capacitors based on the applicable specification or device guidelines.

Figure 1 shows an example of a component placement design.

FIGURE 1: SAMPLE PLACEMENT CONSIDERATIONS



Note: Refer to *AN 26.2 Implementation Guidelines for Microchip USB 2.0 and 3.1 Gen 1 Hub Devices Application Note* for more detailed placement guidelines.

5.0 POWER AND GROUND DISTRIBUTION

Adequate power and ground distribution is critical to the success of any high-speed PCB design. Figure 2 shows examples of inner layer power and ground floods. For more detailed suggestions for filtering local voltage switcher outputs and methods for bypassing the power rails and general guidelines for power distribution, refer to Section 3.4 of the *AN 26.2 Implementation Guidelines for Microchip USB 2.0 and 3.1 Gen 1 Hub Devices Application Note*.

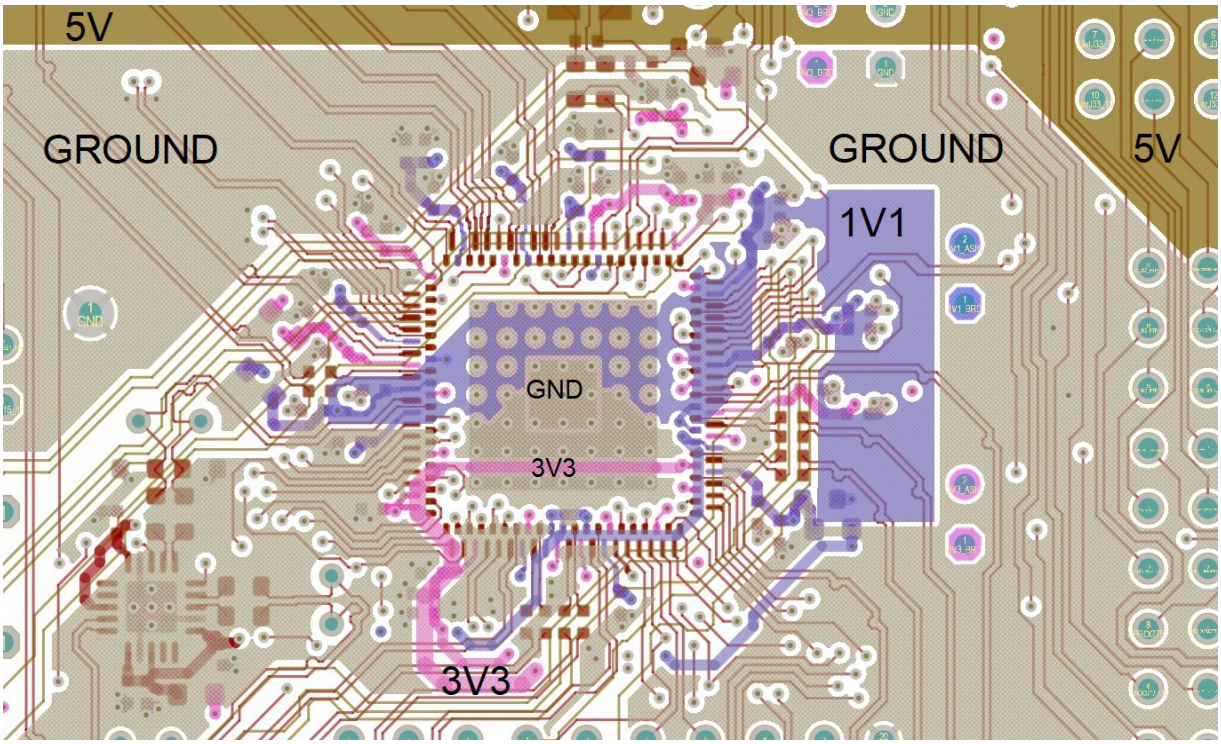
5.1 Power Supplies

The Microchip PCIe Switch products require multiple power supplies for internal core logic, AFE, and I/O.

The Microchip PCIe Switch power supply requirements are:

- VDD33 – Input provides +3.3V (3V3) supply voltage to the I/O rail and the AFE.
- VDD11 – Input provides +1.1V (1V1) supply voltage to the core logic and the AFE.
- VDDVARIO – Input provides +1.8V to +3.3V supply voltage to the variable I/O.

FIGURE 2: EXAMPLE OF INNER LAYER WITH POWER AND GROUND FLOOD



Note 1: All +1.1V power supplies must be powered from a common +1.1V source and cannot be powered separately.

2: All +3.3V power supplies must be powered from a common +3.3V source and cannot be powered separately.

3: A +5V power rail is depicted in Figure 1 to demonstrate an example of how power can be routed to the USB connectors.

5.2 Digital Ground and Shield Ground

USB cables and connectors use a shield ground or chassis ground. Refer to *AN 26.2* Figure 1 for an example of how to implement the digital ground to the shield (or chassis) ground connection. See *AN 26.2* Figure 10 for an example of chassis-ground treatment.

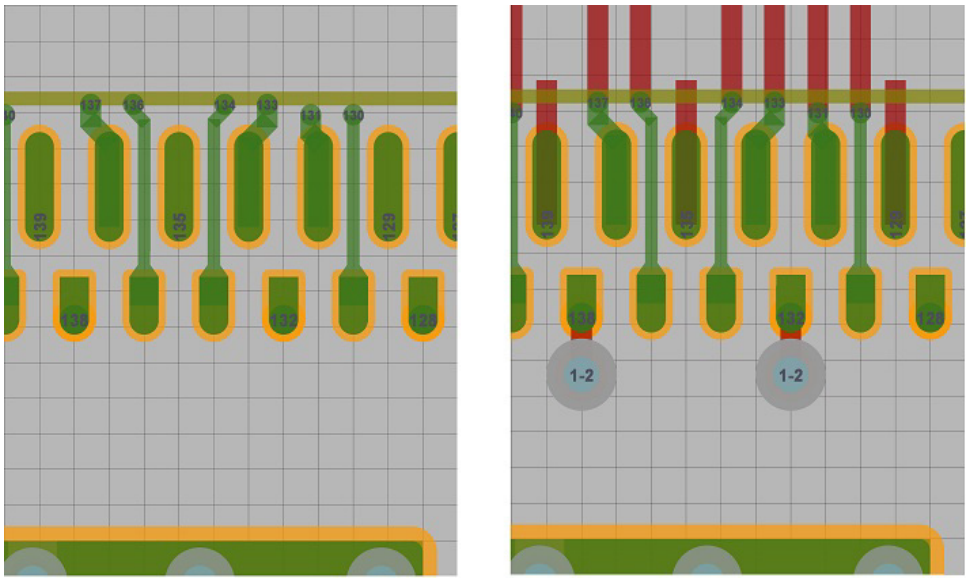
6.0 SKEW-COMPENSATING FOOTPRINTS

The Microchip PCIe Switch DQFN package **can** use a specially designed footprint that has skew compensation built into the breakout pattern. This physical skew compensation is **not** needed when the schematic symbol includes signal length skew offsets. Conventional single-row QFN packages do not require skew compensation since the differential-pair elements are in the same row as their differential-pair partners.

DQFN packages have shorter electrical paths to their inner-row pins than the adjacent outer-row pins. This imparts propagation delay skew between an inner-row pin and the outer-row pins adjacent to it about equal to the center length difference from the die to the pins.

A typical footprint does not compensate for the package skew between adjacent pins that contain high-speed differential-pair members, but the skew compensating footprint from Microchip for the PCIe controller does. The PCB design only needs to route the matched length differential pair to the terminations. The terminations have been designed to perform all the required skew compensation for the critical differential-pairs and still allow for breakout pads next to them. Figure 3 shows an example of skew compensation for a DQFN package footprint.

FIGURE 3: SKEW COMPENSATING FOOTPRINT SAMPLE



Note 1: Note how the differential pair routing is executed from the breakout terminations rather than the pads.

7.0 MISCELLANEOUS

The following section is dedicated to miscellaneous PCB layout topics related to Microchip's PCIe Switches. Refer to the Microchip product-specific *PCI1xxxx Data Sheet* for detailed operational characteristics, thermal ratings, power requirements, DC specifications, and timing parameters.

7.1 Pin Descriptions

The pin assignments and pin description tables from the product-specific data sheet describe the pin functions, pin states, and pin connections for normal operation. Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip Reset). Configuration straps are identified by an underlined symbol name.

Note:	Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

7.2 PCB Materials

The use of different PCB dielectric materials can impact the signal integrity of PCIe and USB 3 transmission lines. The use of lower-loss materials, such as 370HR, NP-175, and FR408HR, allows for longer trace lengths with a reduced effect on the high-speed transmission lines. Even lower-loss materials, such as I-Tera MT40, Megtron6, or RO4350, may be needed for PCIe 4 or faster designs. For more detailed information on PCB construction, PCB Materials, Stack-up, and Impedance Control, refer to Section 3.2 of *AN 26.2*.

7.3 PCB Stack-up

The pinouts of Microchip's PCIe Switch products make it difficult to implement a PCB using only two (2) layers. Using more than two layers provides greater control of impedances, return paths, and thermal management. An example of a four-layer PCB stack-up is illustrated in *AN 26.2* Figure 8.

7.4 Operational Characteristics

Absolute maximum ratings and operating conditions can be found in the product-specific data sheet.

7.5 Thermal Ratings

The PCIe switch thermal limits can be found in the package thermal parameters table in the product-specific data sheet.

7.6 Power Requirements

The PCIe switch power requirements can be found in the device power consumption in the product-specific data sheet.

7.7 DC Specifications

Specific pin input and output impedance parameters as well as various input and/or output capacitance characteristics are available in the DC specifications section of the product-specific data sheet.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00006029A (06-18-25)	Initial release	

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