AN5907

PCI1xxxx PCIe IBIS AMI Evaluation and Usage

1.0 INTRODUCTION

This application note provides an outline and usage model for the PCI1xxxx IBIS AMI models. The PCI11414, PCI11400, PCI11010, and PCI11101 have one (1) PCIe PHY upstream connector and one (1) PCIe PHY downstream connector. The PCI12000 has one (1) PCIe PHY upstream connector and two (2) PCIe PHY downstream connectors.

This document is written for engineers who are familiar with IBIS simulation models. The goal of this application note is to outline the configuration and usage of the IBIS models.

1.1 Sections

This document includes the following topics:

- Section 2.0, PCI1xxxx IBIS Folder Contents
- Section 3.0, AMI Model Parameters
- Section Appendix A:, TX Model Evaluation
- Section Appendix B:, RX Model Evaluation

1.2 References

The following documents should be referenced when using this application note:

- *PCI11414 Data Sheet*
- *PCI11400 Data Sheet*
- *PCI11101 Data Sheet*
- *PCI11010 Data Sheet*
- *PCI12000 Data Sheet*

2.0 PCI1XXXX IBIS FOLDER CONTENTS

This section provides an overview of the files within the PCI1xxxx IBIS .zip folder.

1. PMATS40LPCLXEB2_TX.ibs

This is a top-level IBIS-AMI model file containing the IBIS buffer and reference to the AMI model for TX.

2. PMATS40LPCLXEB2_RX.ibs

This is a top-level IBIS-AMI model file containing the IBIS buffer and reference to the AMI model for RX.

3. PMATS40LPCLXEB2_TX.ami

This is the algorithmic model interface to the DLL for TX. This file specifies the AMI parameters which can be modified or defined by the user for any channel simulation.

4. PMATS40LPCLXEB2_RX.ami

This is the algorithmic model interface to the DLL for RX. This file specifies the AMI parameters which can be modified or defined by the user for any channel simulation.

5. PMATS40LPCLXEB2_TX_x64.dll

This a Windows® 64-bit dynamic-linked library (DLL) file. This file contains all algorithmic models for the transmitter.

6. PMATS40LPCLXEB2_RX_x64.dll

This is a Windows 64-bit dynamic-linked library (DLL) file. This file contains all algorithmic models for the receiver.

7. PMATS40LPCLXEB2_TX_x64.so

This is a Linux® 64-bit shared object compiled library file. This is the Linux equivalent of a Windows DLL.

8. PMATS40LPCLXEB2_RX_x64.so

This is a Linux 64-bit shared object compiled library file. This is the Linux equivalent of a Windows DLL.

9. *ANXXXX - PCI1xxxx PCIe IBIS AMI Evaluation and Usage*

This application note.

All files should be placed in the same working directory as that of the channel simulator tool being used.

Note:	**Files that are NOT `.ami` should NOT be modified in any way.** Changes to the file contents could result in unexpected behavior and generate simulation results not indicative of actual SERDES performance. If it is suspected that any of the files above needs to be modified, please contact Microchip Technology Inc.

3.0 AMI MODEL PARAMETERS

The following AMI parameters can be seen in the file PMATS40LPCLKEB2_TX.ami and PMATS40LPCLKEB2_RX.ami files. Model-specific parameters can be modified in a channel simulator, while other parameters should not be altered by users. See Table 1 and Table 2 for the parameter details.

TABLE 1: PMATS40LPCLKEB2 TRANSMITTER IBIS-AMI MODEL AMI

Parameter	Type	Description
Model-Specific Parameters		
Corner Case	Int	0 – Typical (TT silicon, 40°C operating temperature, VDDATX = 1.1V) 1 – Slow (SS silicon, –40°C operating temperature, VDDATX = 0.99V) 2 – Fast (FF silicon, 125°C operating temperature, VDDATX = 1.21V)
AutoInitFFE	Int	0 – Does not automatically initialize the FFE taps for optimal emphasis based on the channel impulse response. 1 – Automatically initializes the FFE taps for optimal emphasis based on the channel impulse response.
TXDRV	Int	[0-7] Represents the number of 8 active register segments. The number of active elements is TXDRV + 1. Elements are activated from element 0 up to 7, in order. Example: TXDRV = 0 sets only element 0 active. TXDRV = 3 would activate elements 0, 1, 2, and 3, and so forth. Used if AutoInitAFE=0
TXDRVTRIM	String	Array of TXDRV+1 integers with range [0, 7]. Each represents the level for the associated TXDRV segment. This is a string indicating element drive strength from element 0 (at the LSBs) up to element 7 (at the MSBs). Example: TXDRVTRIM = ‘01234567’ would indicate drive strength 7 for element 0, drive strength 0 for element 7, etc. Used if AutoInitFFE=0
TXDATA_INV	String	Array of TXDRV+1 integers, [0 or 1] This is a string indicating TXDRVTRIM element from element 0 (at the LSBs) up to element 7 (at the MSBs). A value of 1 will invert the value. Example: TXDATA_INV = '01000010' would invert elements 1 and 6. Used if AutoInitFFE=0
TXDEL	String	This is a string setting delay for each driver segment from element 0 (at the LSBs) up to element 7 (at the MSBs). Where: 1 = Assigns segment to pre-cursor 2 = Assigns main cursor 3 = Assigns post cursor Example: TXDEL='10020030' would indicate a precursor assignment to element 7 Used if AutoInitFFE=0
AutoSetSwingLevel	Int	0 – Does not automatically set the FFE voltage swing level. (Not recommended to set.) 1 – Automatically sets the FFE voltage swing level. (Recommended to leave at default value 1.)

TABLE 1: PMATS40LPCLKEB2 TRANSMITTER IBIS-AMI MODEL AMI (CONTINUED)

Parameter	Type	Description
Model-Specific Parameters		
SwingLevel	Float	FFE voltage swing level (in Volts). Used if AutoSetSwingLevel=0
Constant Parameters		
Init_Returns_Impulse	—	Recommended to be left at default.
GetWave_Exists	—	Recommended to be left at default.
Max_init_Aggressors	—	Recommended to be left at default.

TABLE 2: PMATS40LPCLKEB2 RECEIVER IBIS-AMI MODEL AMI

Parameter	Type	Description
Model-Specific Parameters		
Corner Case	Int	0 – Typical (TT silicon, 40°C operating temperature, VDDATX = 1.1V) 1 – Slow (SS silicon, –40°C operating temperature, VDDATX = 0.99V) 2 – Fast (FF silicon, 125°C operating temperature, VDDATX = 1.21V)
CTLE_AutoInit	Int	0 – Does not automatically select the best CDR CTLE state based on the channel impulse response. 1 – Automatically selects the best CDR CTLE state based on the channel impulse response.
CTLE_State	Int	[1 to 8] Set the CTLE peaking and degeneration. Only used when CTLE_AutoInit=0. See Table 3 for more mapping information.
CDR_Stability_Factor	Float	[100-200;1] CDR error gain factor used in the calculation of the sampling error gain. This parameter should remain set to its default state.
CDR_BB_Step	Float	[0.3125-10.0;0.01] CDR error gain factor numerator in the calculation of the sampling error gain. This parameter should remain set to its default state.
CDR_SamplerUIDelay	Float	[–0.5-0.5; 0.05] CDR sampler offset in UI.
DFE_Adapt	Int	0 – DFE tap coefficients will **NOT** be dynamically modified during runtime. 1 – DFE tap coefficients will be dynamically modified during runtime to determine the best set for optimal eye height.
DFE_Alpha	Float	[0.002-0.2;0.0002] A scalar gain applied to the slicer error and is used to modify the DFE tap values. This parameter should remain set to its default state. However, in situations where the channel loss is high and the received waveforms require significant equalization, this value can be increased.
DFE1 – DFE5	Int	[0-15] DFE tap coefficients applied when DFE_AutoInitTaps = 0
DFE_OutputGain	Float	[1.0-10.0;0.1] Scalar gain applied to the RX model output after the DFE. This parameter should remain set to its default state.
DFE_OverrideCDRClock	Int	0 – Does not override the CDR clock. (For normal operation, recommend leaving set to 0.) 1 – Switch from the input CDR clock to an internal clock synced with the CDR clock, but with phase held constant thereafter and no longer tracking the CDR clock phase. This effectively forces the clock to have a constant UI time as defined by the nominal bit rate.
DFE_ClockOffsetDeg	Float	[–90-90;1] When DFE_OverrideCDRClock=1, add this additional phase to the internal clock in degrees.
DFE_OutputUIDelay	Float	[–0.5-0.5; 0.05] Adds a delay to the DFE output relative to the DFE output clock_times. This effectively causes the center of the output eye to shift in either the positive or negative direction.

TABLE 2: PMATS40LPCLKEB2 RECEIVER IBIS-AMI MODEL AMI (CONTINUED)

Parameter	Type	Description
Model-Specific Parameters		
RXOutputOption	Int	Selects the data path to view in the simulator output. 0 – CTLE 1 – CTLE with clock_times 2 – CTLE+CDR+DFE with clock_times
Constant Parameters		
Init_Returns_Impulse	—	Recommended to be left at default
GetWave_Exists	—	Recommended to be left at default
Ignore_Bits	—	Recommended to be left at default

Table 3 maps the parameter CTLE_State to its respective CST and RST values. CTLE peaking and degeneration are set via PMA parameter CST1, CST2, RST1, and RST2. In the IBIS-AMI model, the parameter CTLE_State controls the available CST and RST values.

TABLE 3: RX IBIS-AMI MODEL AMI PARAMETER CTLE_STATE MAPPING

IBIS-AMI CTLE_State	CST1/2	RST1	RST2
1	0	0	0
2	0	1	2
3	0	2	2
4	0	3	3
5	1	0	0
6	1	1	2
7	1	2	2
8	1	3	3

APPENDIX A: TX MODEL EVALUATION

This appendix provides information on using the PMATS40LPCLXEB2_TX IBIS-AMI models.

A.1 Output Level vs. TXDRV and DR-Corner

The following data is the result on a parametric sweep of the TX parameters data rate (DR) and TXDRV across their respective specified range. Refer to Figure A-1.

- RX IBIS component acts as an ideal 100Ω differential load
- TXDEL = “22222222”
- TXDATA_INV = “00000000”
- TXDRVTRIM = “77777777”

Note:	Deemphasis was not active during testing.

FIGURE A-1: KEYSIGHT ADS TESTBENCH FOR TRANSMITTER PEAK-TO-PEAK DIFFERENTIAL VOLTAGE SWING EVALUATION

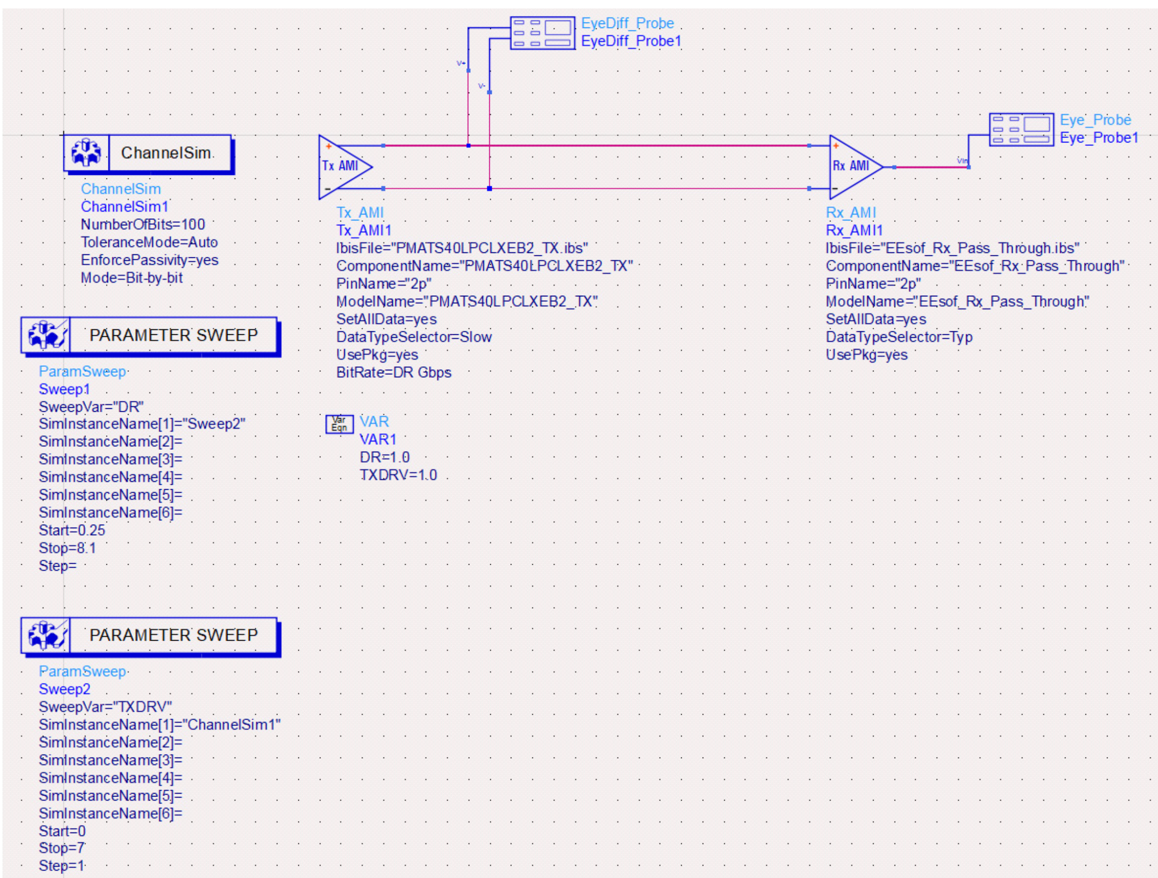
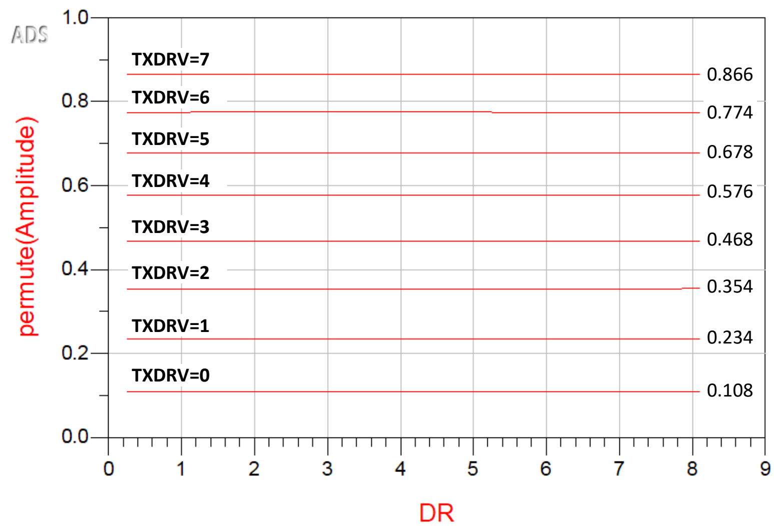


FIGURE A-2: DRIVE STRENGTH TESTBENCH RESULTS FOR TT OPERATING CONDITION



The same test was run for slow and fast splits. See Figure A-3 and Figure A-4.

FIGURE A-3: DRIVE STRENGTH TESTBENCH RESULTS FOR SS OPERATING CONDITION

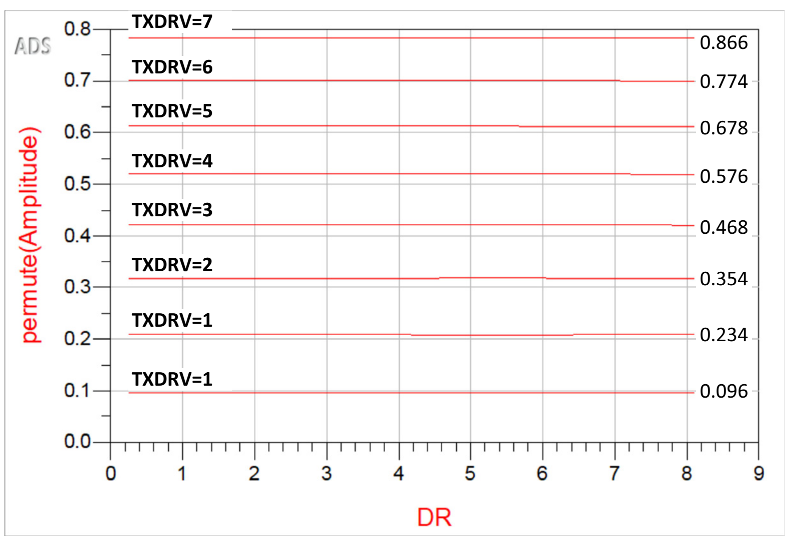
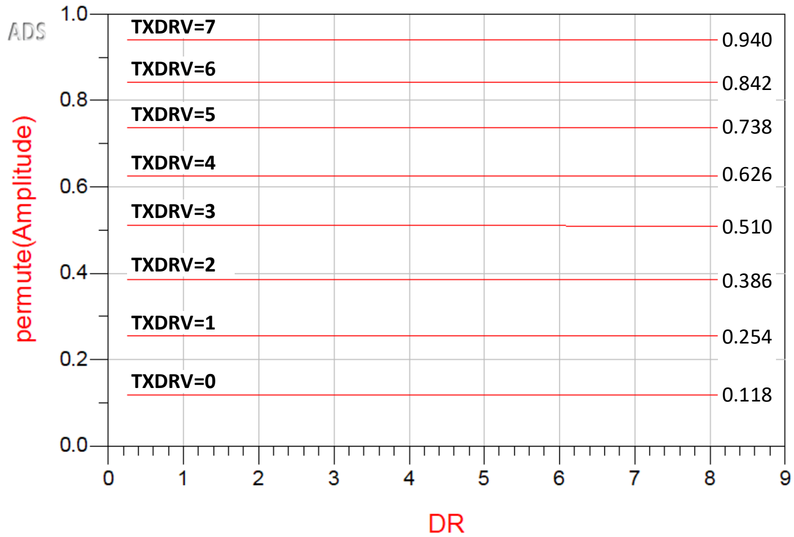


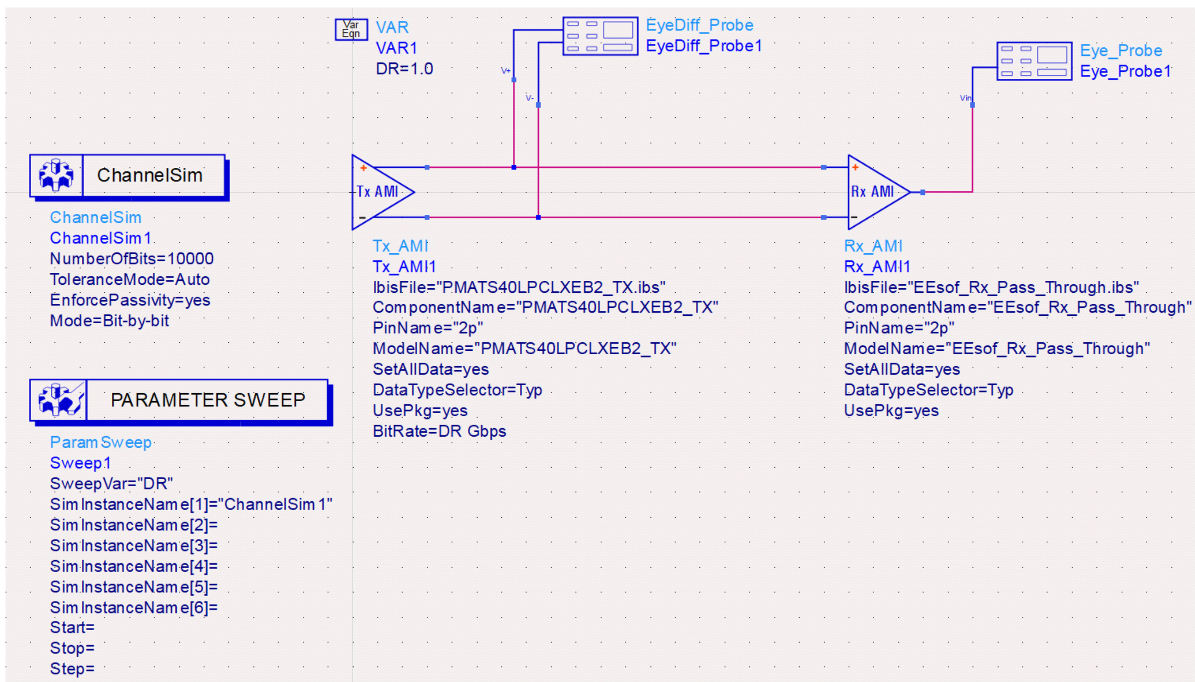
FIGURE A-4: DRIVE STRENGTH TESTBENCH RESULTS FOR FF OPERATING CONDITION



A.2 Deemphasis

Using the same ADS test setup in Section A.1, Output Level vs. TXDRV and DR-Corner, the transmitter deemphasis was characterized and compared against the calculated expectation. The parameter sweep module was used to make the available variable DR in the data display window. In actuality, DR is nor being permuted, and the controller is set to single-point sweep.

FIGURE A-5: KEYSIGHT ADS TESTBENCH FOR TRANSMITTER 3-TAP FIR FUNCTIONALITY (EMPHASIS) EVALUATION ACROSS OPERATING CONDITION



Two tested cases were checked. In both test cases, the data rate was held constant at 1 Gbps.

1. 3 dB
2. 6 dB

See Figure A-6.

FIGURE A-6: DATA DISPLAY EQUATIONS FOR MEASURING POSTCURSOR EMPHASIS IN THE TRANSMITTED WAVEFORM

```
Eqn DR=Eye.Eye_Probe1.DR

Eqn UI=1/(1e9*DR)

Eqn stopTime=EyeDiff_Probe1.time[0]+30*UI

Eqn idx=find_index(EyeDiff_Probe1.time[0][::], stopTime)

Eqn Deemphasis=20*log10(m1/m2)
```

A.2.1 3 DB

FIGURE A-7: TRANSMITTER 3 DB EMPHASIS AT TT OPERATING CONDITIONS

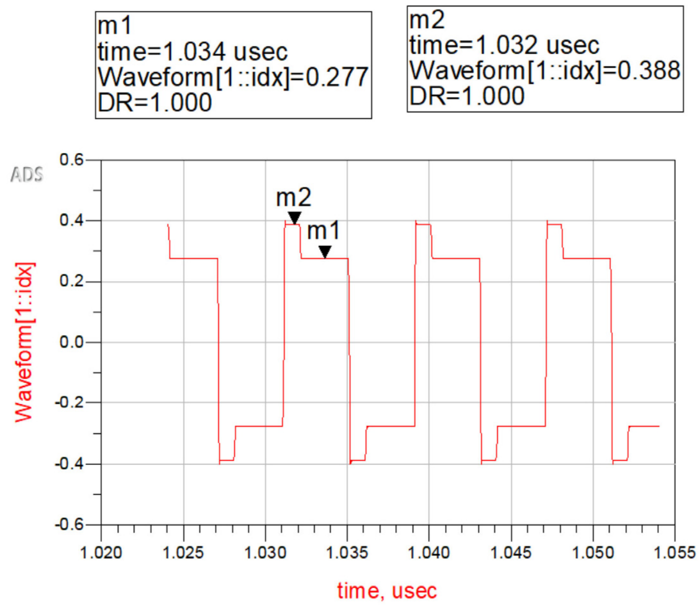


FIGURE A-8: TRANSMITTER 3 DB EMPHASIS AT SS OPERATING CONDITIONS

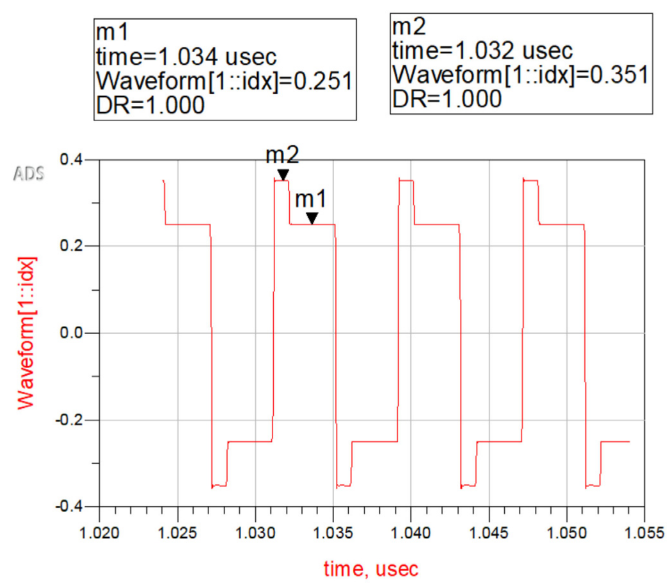
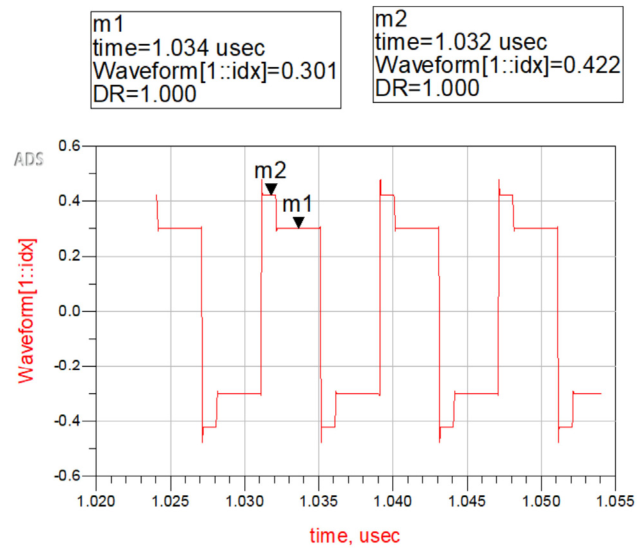


FIGURE A-9: TRANSMITTER 3 DB EMPHASIS AT FF OPERATING CONDITIONS



A.2.2 6 DB

FIGURE A-10: TRANSMITTER 6 DB EMPHASIS AT TT OPERATING CONDITIONS

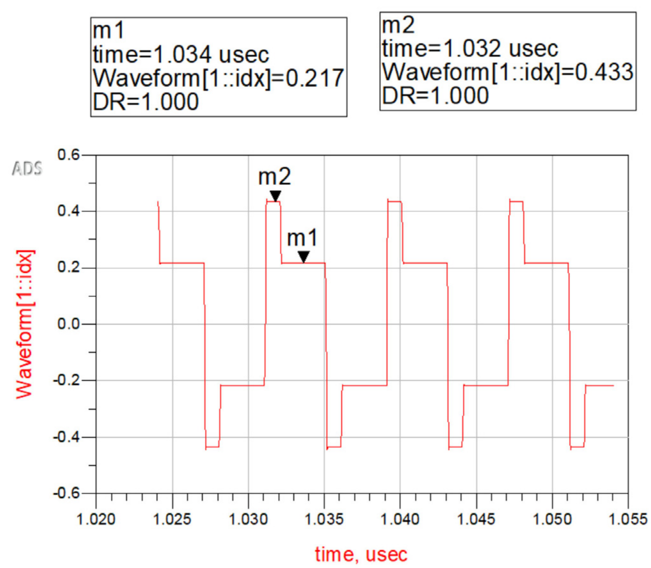


FIGURE A-11: TRANSMITTER 6 DB EMPHASIS AT SS OPERATING CONDITIONS

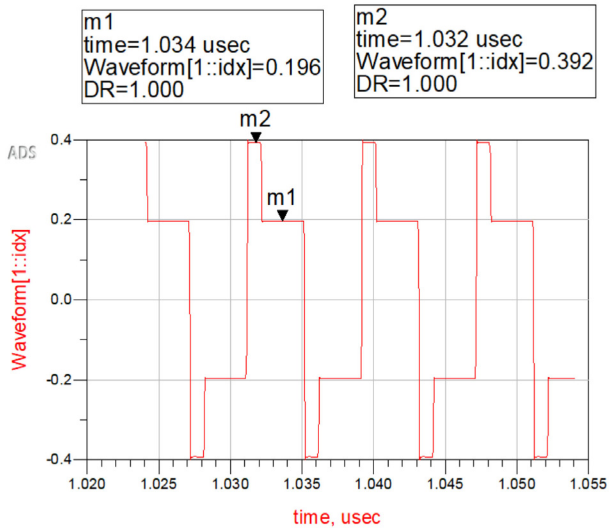
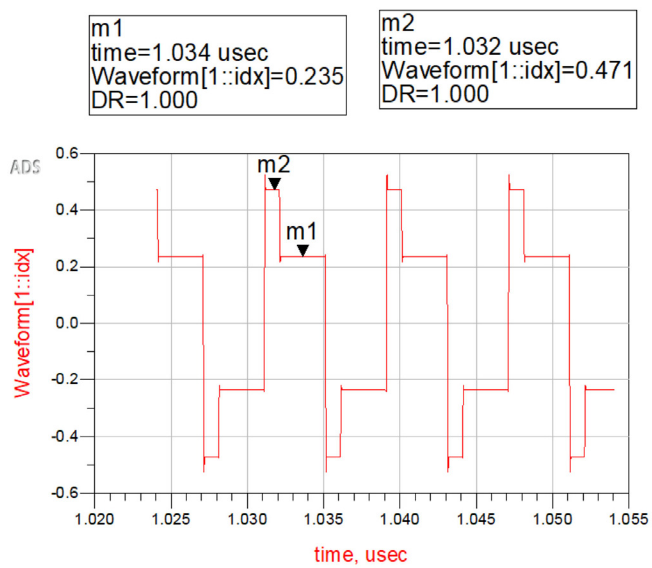


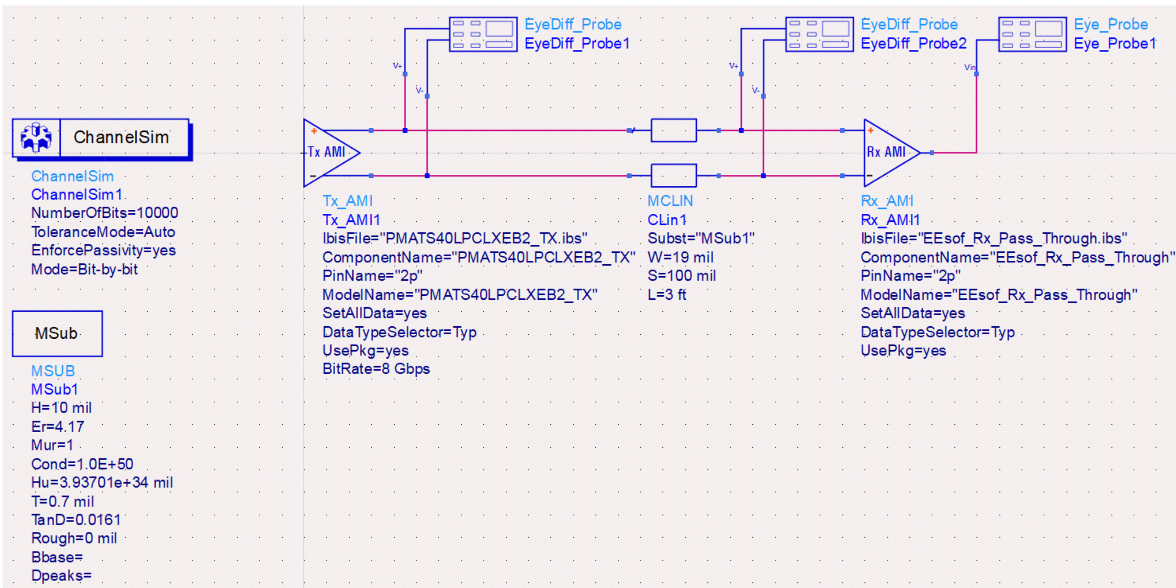
FIGURE A-12: TRANSMITTER 6 DB EMPHASIS AT FF OPERATING CONDITIONS



A.2.3 EYE DIAGRAMS

To highlight the impact of transmitter deemphasis on eye quality, a differential transmission line channel was introduced.

FIGURE A-13: KEYSIGHT ADS TESTBENCH FOR EVALUATING TRANSMITTER EMPHASIS ON CHANNEL ISI EQUALIZATION

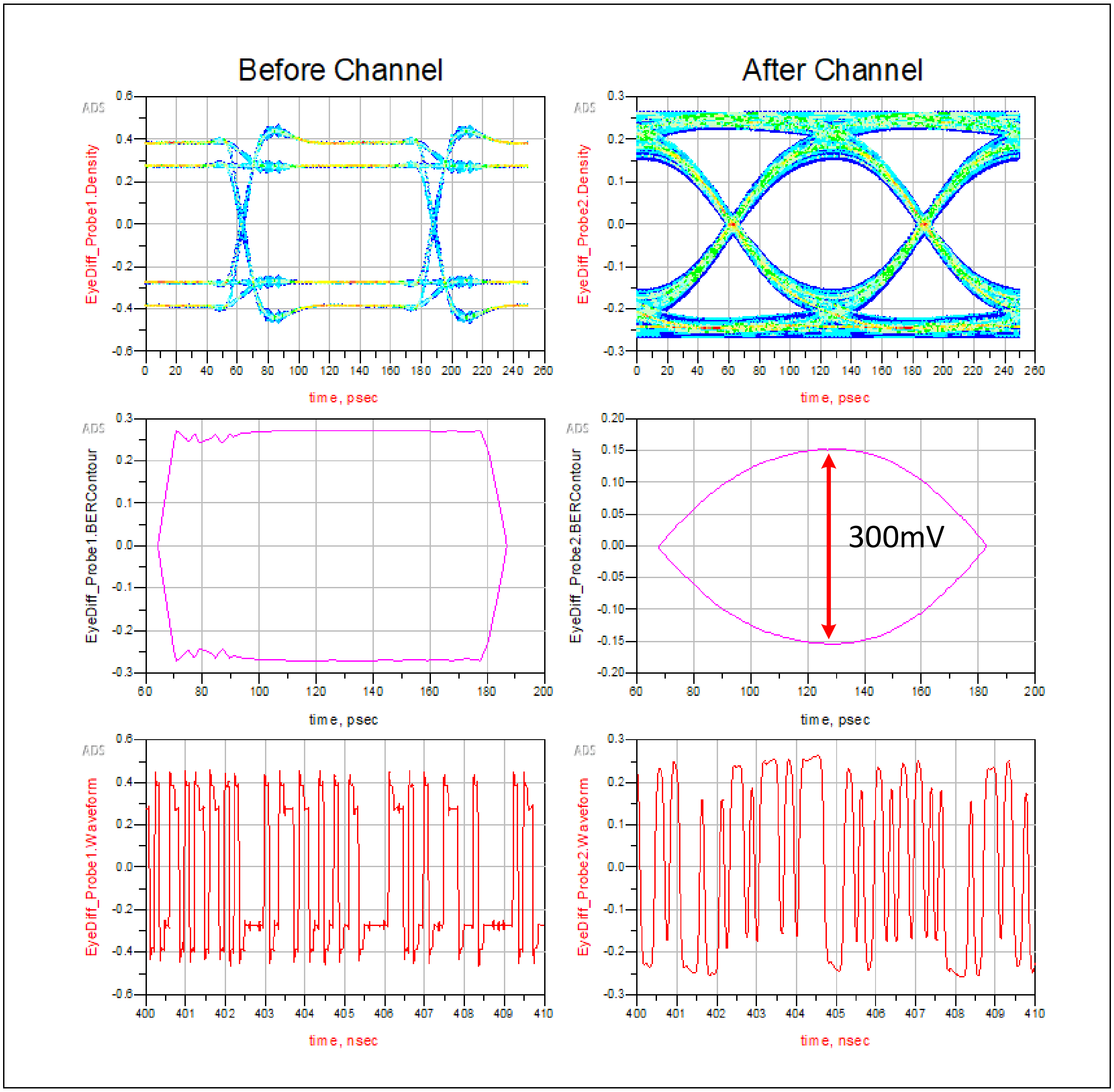


At 3 feet in length, the channel has approximately 8.5 dB of loss at 4 GHz.

The simulations were performed at 8 Gbps and the transmitter was set to 3 dB deemphasis.

- TXDRV = 6
- TXDATA_INV = “00000001”
- TXDEL = “22222223”
- TXDRVTRIM = “77777777”

FIGURE A-14: TRANSMITTER 8 GBPS EYE AFTER APPLYING 3 DB POST-CURSOR EMPHASIS TO A CHANNEL WITH 8.5 DB LOSS AT 4 GHZ



A.3 PCIe De-Emphasis Table

For PCIe Gen3, specific preset values are decoded to driver settings during compliance tests. Table A-1 shows the mappings of each of those presets to driver settings which may be used with the IBIS-AMI model.

TABLE A-1: IBIS-AMI Transmitter AMI Parameter Settings for PCIe Emphasis Presets

Preset	p_TxDeemph [17:0]	Post-Cursor Elements	Main-Cursor Elements	Pre-Cursor Elements	TXDRV	TXDRVTRIM	TXDATA_INV	TXDEL
0	0x00010BC0	16	47	0	7	0xFF7FFF	0xC0	0xFAAA
1	0x00006B00	6	44	0	6	0xF5FFFF	0xC0	0xFAAA
2	0x0000BD00	11	52	0	7	0x3FFFFF	0xC0	0xFAAA
3	0x00003B00	3	44	0	6	0xE9FFFF	0xC0	0xFAAA
4	0x00000000	0	64	0	7	0xDFFFFF	0xC0	0xAAAA
5	0x00000B02	0	44	2	6	0xE5FFFF	0xC0	0xCAAA
6	0x00000B03	0	44	3	6	0xE9FFFF	0xC0	0xCAAA
7	0x0000ED09	14	52	9	7	0x3EEFFFF	0xE0	0xF2AA
8	0x00006B06	6	44	6	7	0xB5FFFF	0xC0	0xCAAA
9	0x00000B06	0	44	6	6	0xF5FFFF	0xC0	0xCAAA

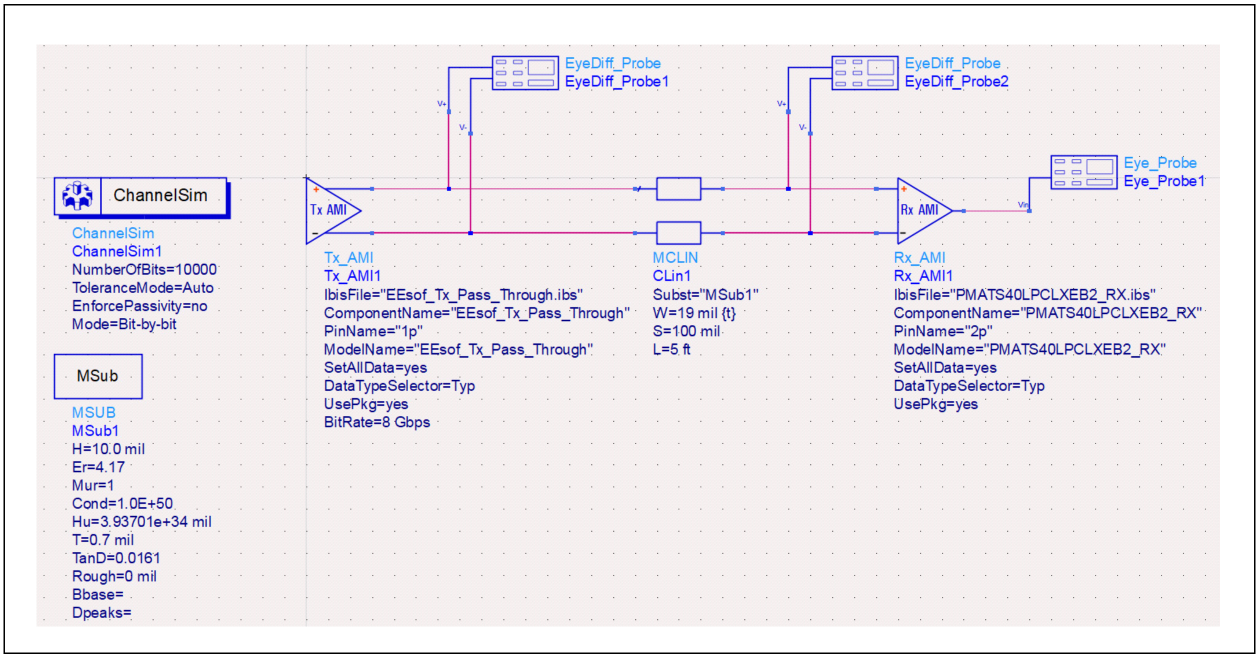
APPENDIX B: RX MODEL EVALUATION

This appendix provides information about using the PMATS40LPCLXEB2_RX IBIS-AMI models.

B.1 CTLE Performance

To evaluate RX CTLE performance, a differential transmission line was added between a golden TX and the IBIS-AMI RX model. See Figure B-1.

FIGURE B-1: KEYSIGHT ADS TESTBENCH FOR EVALUATING IBIS-AMI RX CTLE EQUALIZATION



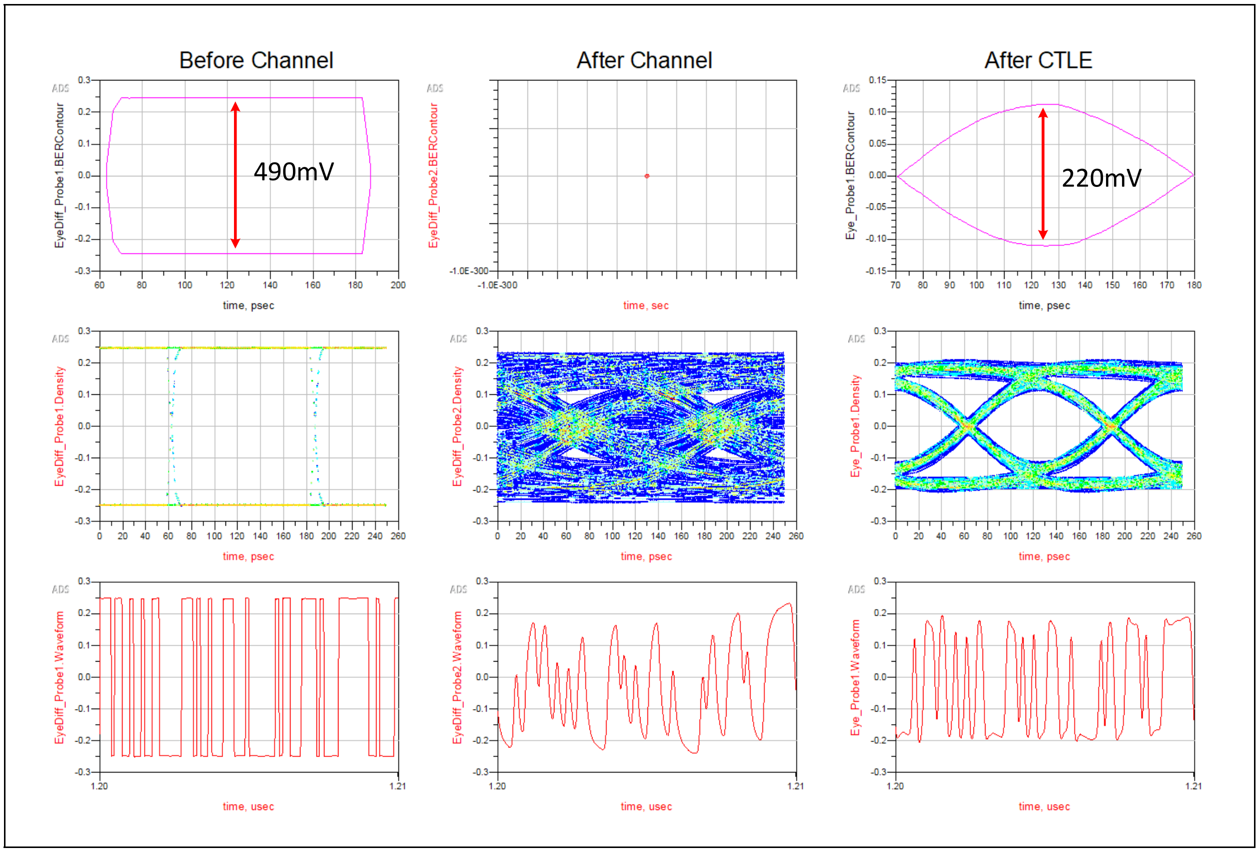
At 8 Gbps and 5 feet in length, the loss at Nyquist (4 GHz) of the transmission line is approximately 14 dB.

In the following measurements, transmitter deemphasis is not active during the test. This only allows the observation of the impact of the CTLE on equalizing the channel loss. Three probes were placed in the design as follows:

1. Before the channel (to observe the data before being possibly corrupted)
2. After the channel but before the receiver
3. At the receiver output

The CTLE was set to autodetermine the best settings for maximizing eye height. In all the plots below, typical corner was simulated. In this simulation, the receiver chose CST = 1, RST1 = 3, and RST2 = 3 as the best settings to improve eye opening.

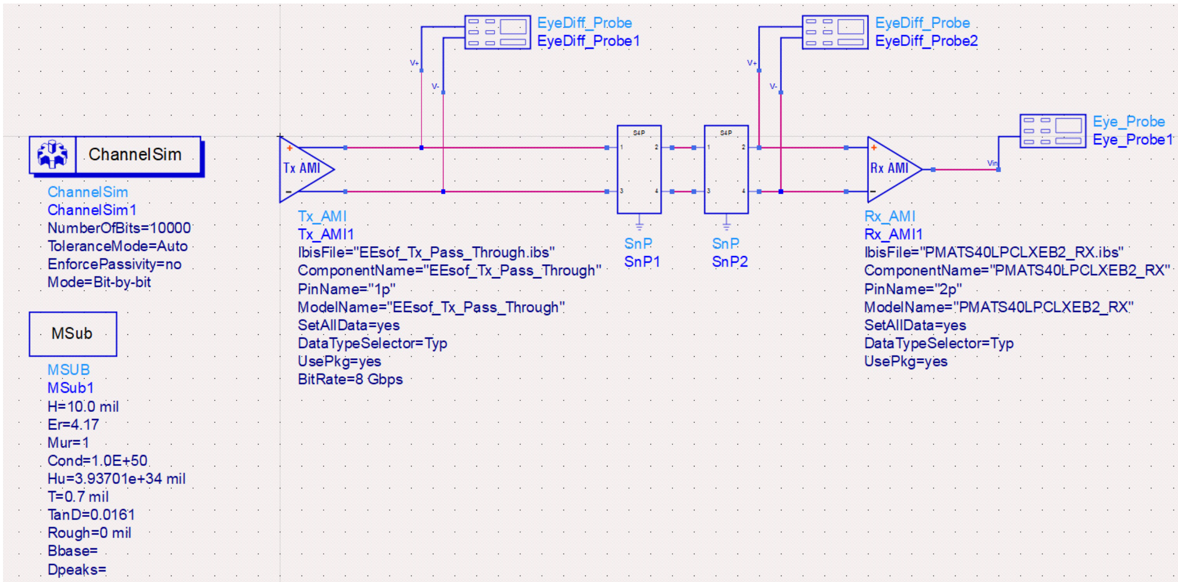
FIGURE B-2: DATA INNER EYE QUALITY BEFORE AND AFTER A LOSSY CHANNEL AND AFTER APPLYING CTLE-ONLY EQUALIZATION



B.2 CTLE + DFE Response

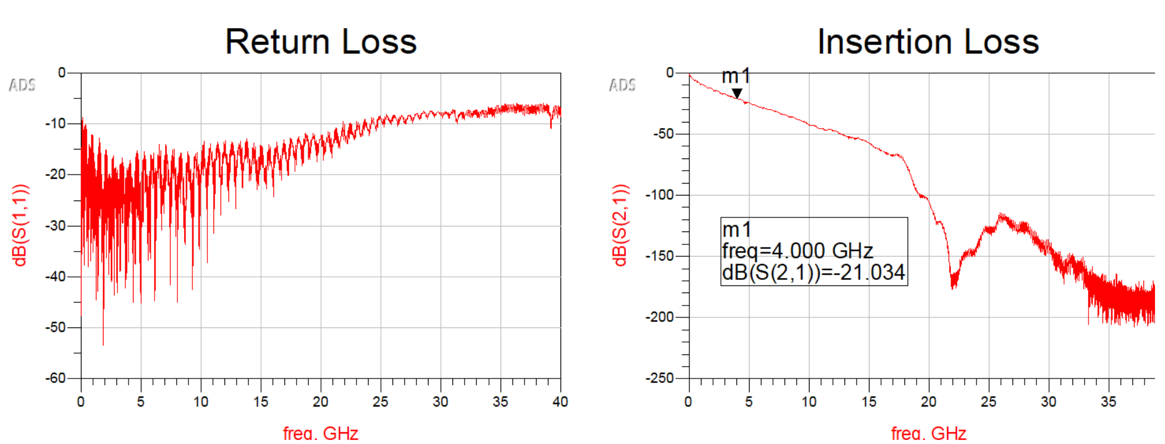
To exercise the CTLE + DFE data path, a new lossy channel was placed between the TX and RX. See Figure B-3.

FIGURE B-3: KEYSIGHT ADS TESTBENCH TO EVALUATE IBIS-AMI RX CTLE + DFE EQUALIZATION



In the return and insertion loss plots, Figure B-4, the S4P represents a real-world lossy channel that was used in Figure B-3. Insertion loss is 21 dB at Nyquist for 8 Gbps data transmission.

FIGURE B-4: RETURN AND INSERTION LOSS CURVES FOR THE LOSSY CHANNEL DEPLOYED IN THE TESTBENCH SEEN IN FIGURE B-3

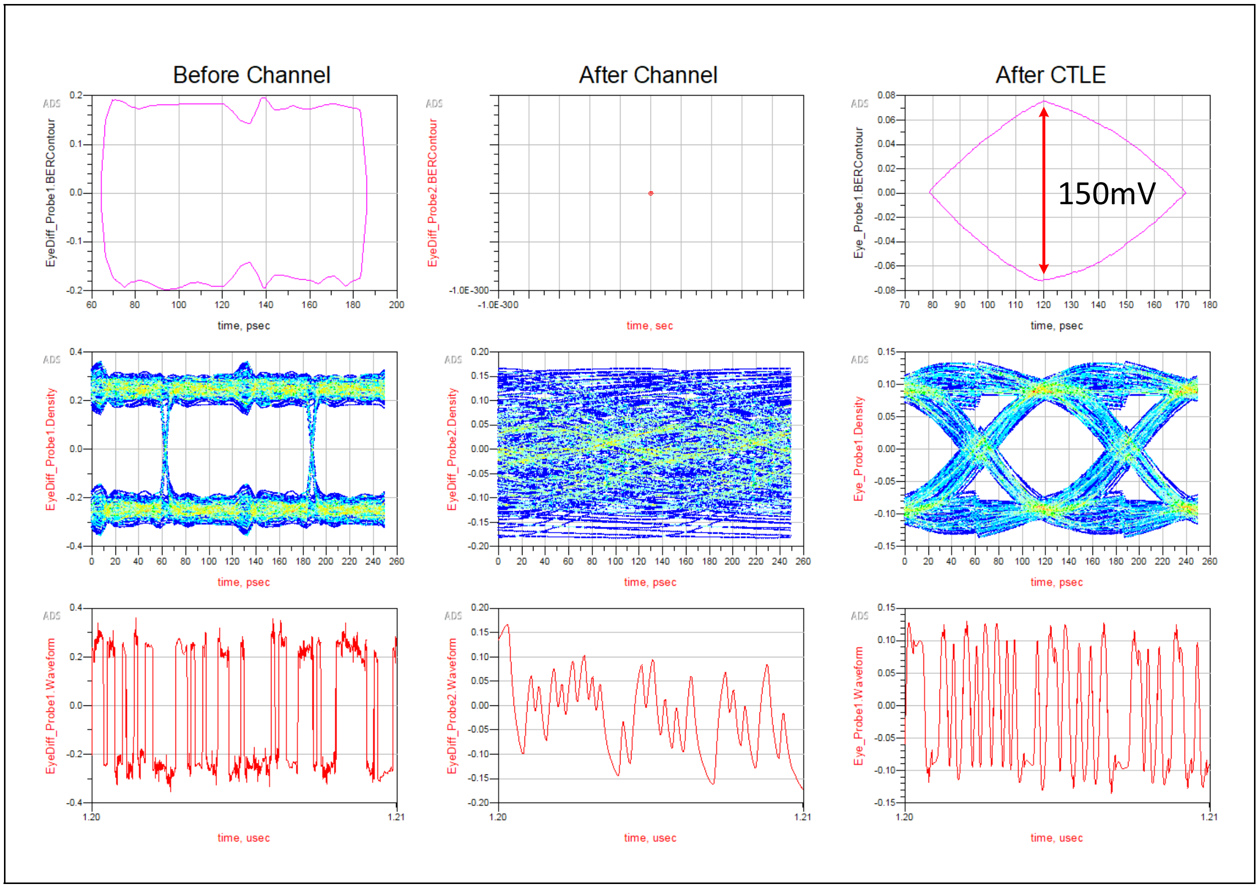


Now, the same measurements were performed but with this new lossy channel inserted. Again, transmitter deemphasis is not active. The same three probes were placed:

1. Before the channel (to observe the data before being possibly corrupted)
2. After the channel but before the receiver
3. At the receiver output

The CTLE and DFE were set to autodetermine the best settings to maximize eye height. Plots are still simulated using typical corners. In the simulation, the receiver chose CST = 1, RST1 = 3, RST2 = 3 with H-coefficients = [1, 2, 0, 0, 0].

FIGURE B-5: DATA INNER EYE QUALITY BEFORE AND AFTER A LOSSY CHANNEL AND AFTER APPLYING CTLE + DFE EQUALIZATION



APPENDIX C: REVISION HISTORY

TABLE C-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005907A (04-22-25)	Initial release	

NOTES:

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