

## Introduction

This application note provides detailed information and circuit design guidelines for the implementation of a Power over Ethernet (PoE) Power Source Equipment (PSE) system, based on Microchip's PD77718T4, PD77718T3, or PD77714T4 PoE Manager. This document enables designers to integrate PoE capabilities (as specified in the IEEE® 802.3bt standard) into an Ethernet switch.

To maintain simplicity, the term PD77718 will be used throughout this document to refer to all three managers, except where a specific characteristic applies to only one of the managers.

The PD77718T4 and PD77714T4 PoE Managers support up to Type 4, 90W output power per port. The PD77718T3 PoE Manager supports up to Type 3, 60W output power per port. Any combination of 2-pair and 4-pair in the same system is possible and supported. Up to 12 devices can be cascaded to provide up to 48, 4-pair ports.

The devices support PoE Powered Device (PD) detection, classification, power-up and protection according to the IEEE 802.3bt standard, and legacy/pre-standard PD detection. They provide real-time protection against fault conditions such as overload, under-load, over-voltage, over temperature and short-circuit.

Microchip offers complete Evaluation Board (EVB)s. For an Evaluation Board recommendation or access to device data sheets or related application notes, consult your regional Microchip Client Engagement Manager or visit [www.microchip.com/poe](http://www.microchip.com/poe).

Firmware (without the boot section) and GUI are available on [Microchip's Software Library](#).

For technical support, consult your local Embedded Solutions Engineers or go to [www.Microchip.com/support](http://www.Microchip.com/support).

## Features

The PD77718T4, PD77718T3, and PD77714T4 devices and the PSE systems based on them have the following key features:

- IEEE 802.3 bt/at compliant
  - PD77718T4/PD77714T4 - Type 4
  - PD77718T3 - Type 3
- Supported PD Types
  - Type 1, Type 2 PDs (IEEE 802.3af, IEEE 802.3at)
  - Single-Signature PDs
    - PD77718T4/PD77714T4 Type 3 and 4
    - PD77718T3 Type 3
  - Dual-Signature PDs
    - PD77718T4/PD77714T4 Type 3 and 4
    - PD77718T3 Type 3
  - Pre-Standard (Legacy) 4-pair PDs
  - Supports non-compliant and legacy PDs

- Operational Modes
  - Controller mode in conjunction with PD77010 PoE PSE Controller
- Cascade up to 12 devices
  - PD77718T4/PD77718T3 to support 96 × 2-pair ports or 48 × 4-pair ports and any 4-pair/2-pair combination
  - PD77714T4 to support 48 × 2-pair ports or 24 × 4-pair ports and any 4-pair/2-pair combination
- Device Features
  - Per-port integrated Field Effect Transistor (FET), sense resistor, and port diode
  - Total port resistance of 160 mΩ
  - Device power dissipation ≤ 2W at full load
  - Two power rails (55V and 3.3V) for maximum power efficiency
  - 4-pair output power
    - 90W PD77718T4/PD77714T4
    - 60W PD77718T3
  - Over Supply Signal (OSS) support
  - AutoClass support
  - Supports Fast and Perpetual PoE
  - Communication Interfaces
    - I<sup>2</sup>C communication interface between PD77718 and PD77010
    - I<sup>2</sup>C communication interface between PD77010 and host
- Real-Time Protection (RTP)
- Measurements
  - Per-port voltage and current measurement
  - Accurate main power measurement
- Surge
  - Surge upto 2 kV per IEC61000-4-5-2014 without additional components
  - Compliance to ITU-T K.21, GR1089, IEC61000-4-5-2014, EN55024 with suggested protection circuitry<sup>1</sup>
    - Up to 10 kV per IEC61000-4-5-2014
    - Up to 6 kV per ITU-T K21
- Physical Characteristics
  - PD77718
    - Ambient temperature range –40°C to 85°C
    - 56-pin 8 mm × 8 mm QFN package with thermal pad
  - PD77010
    - Ambient temperature range –40°C to 85°C
    - 32-pin 5 mm × 5 mm QFN package

<sup>1</sup> Request AN4813 Surge Protection for Systems Based on PD777xx PSE PoE Manager

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# 1. Operational Modes

This section provides a high-level description of the operational mode:

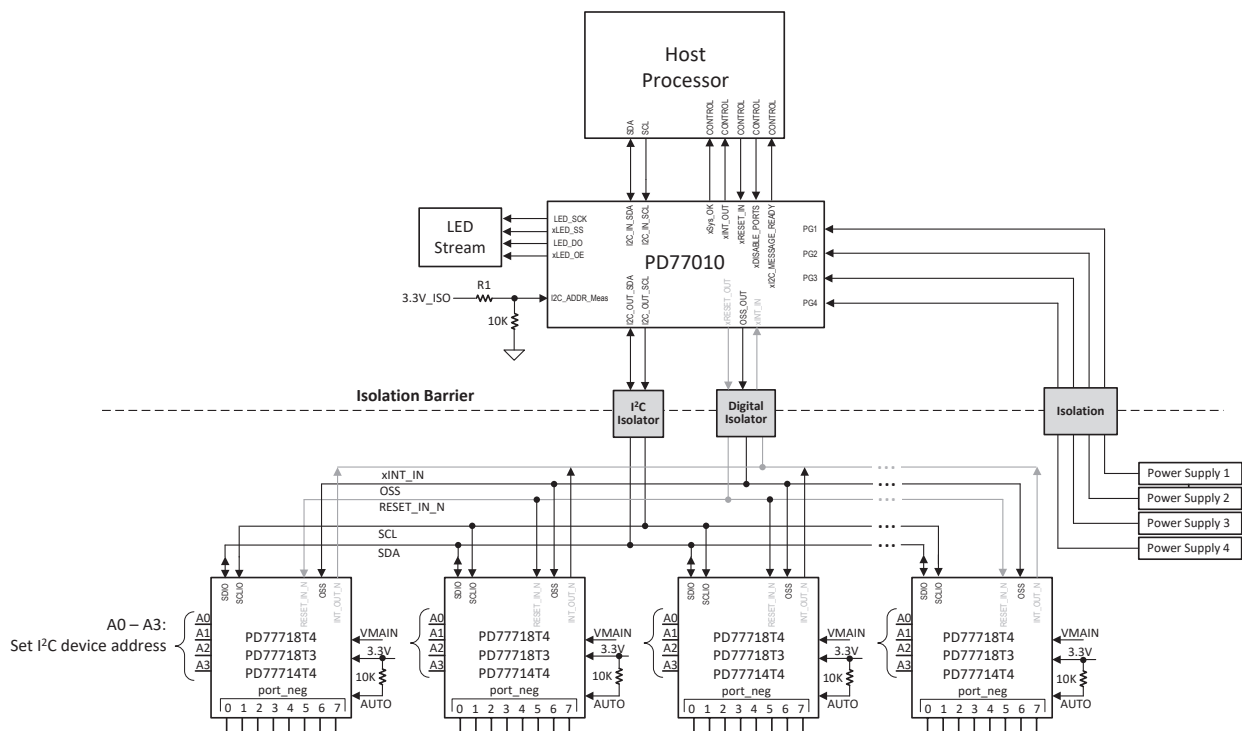
- Controller mode (with PD77010)

## 1.1 Controller Mode

This section describes the chipset operation with PD77010 PoE PSE Controller. The PD77010 device is used in conjunction with the PD77718T4, PD77718T3 or PD77714T4 devices, where the PD77010 provides multi-port PoE functions, such as port mapping (Port Matrix), port priority, port status, and system power management.

The following figure shows the Controller mode application.

**Figure 1-1.** Controller Mode Application



**Note:** The Reset and Interrupt functions (shown in grey) are reserved. For potential future use, it is recommended that the PCB design route these functions; however, the isolator may be a “do not populate” option.

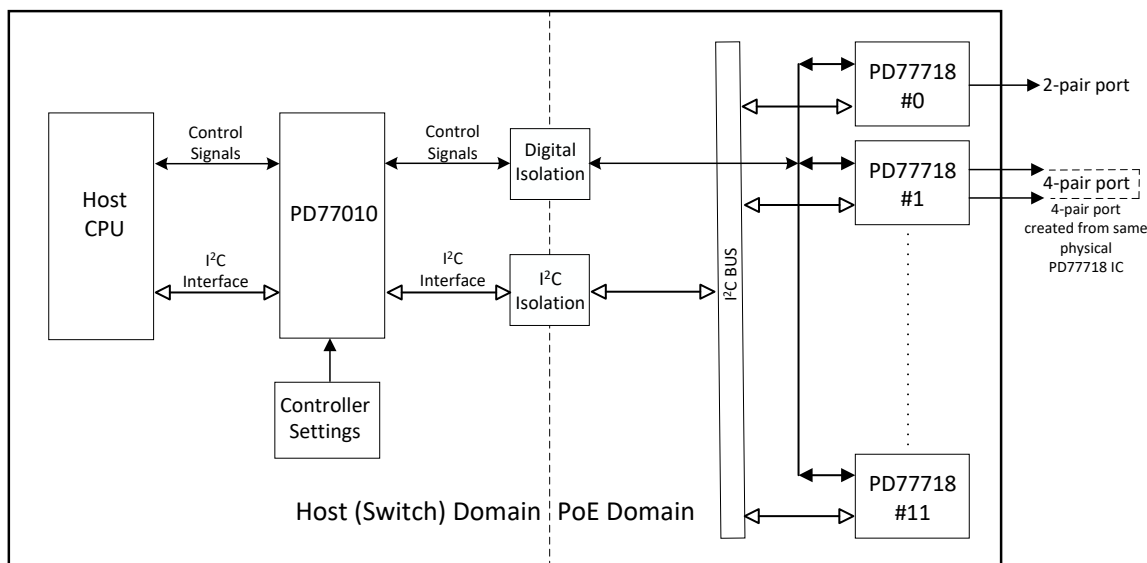
## 2. Functional Descriptions - Controller Mode

A typical application using the PD77010 Controller includes the following blocks:

- PD77718T4/PD77718T3 supports up to  $96 \times 2$ -pair ports or  $48 \times 4$ -pair ports and any 4-pair/2-pair combination. PD77714T4 supports up to  $48 \times 2$ -pair ports or  $24 \times 4$ -pair ports and any 4-pair/2-pair combination
- PD77010 Controller used to initialize, control, and monitor each PD77718T4, PD77718T3, or PD77714T4 through an isolated I<sup>2</sup>C bus.
- Isolation circuit for control signals between PD77010 and PD77718T4, PD77718T3, or PD77714T4 devices

These blocks are shown in the following figure.

**Figure 2-1.** Controller Mode Block Diagram



### 2.1 Communication Interfaces

Two communication interfaces are available: an interface between the Host CPU and the PD77010 Controller and an interface between the PD77010 Controller and the PD77718T4, PD77718T3, or PD77714T4 PoE Managers.

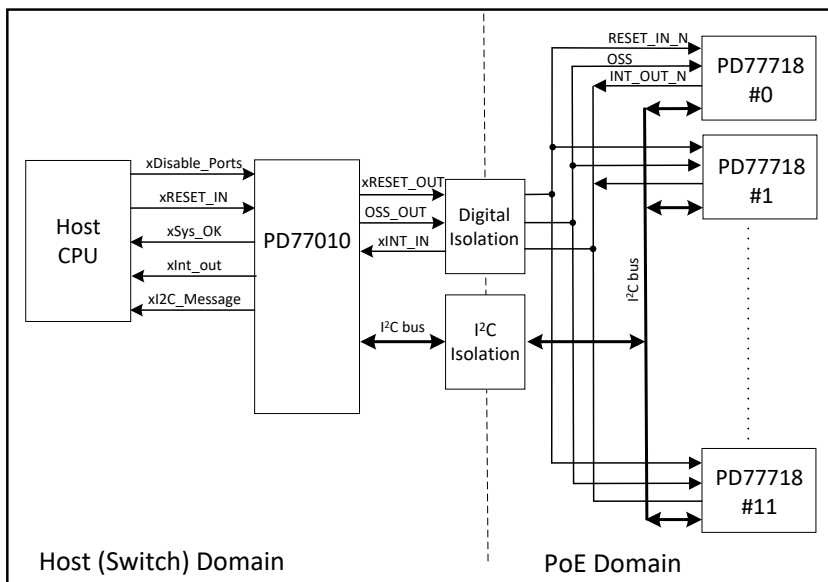
Communication between the Host CPU and the PD77010 is performed through a non-isolated I<sup>2</sup>C interface. Clock speed at this interface is up to 400kHz. The Host CPU issues commands utilizing a dedicated serial communication protocol to the PoE controller. For more information, see the *PD77010 Serial Communication Protocol User Guide*.

Communication between the PD77010 and the PD77718T4, PD77718T3, or PD77714T4 device is through an I<sup>2</sup>C interface with  $1500 V_{RMS}$  isolation. Isolation is a basic requirement of IEEE 802.3bt PoE standards. Each side of the isolator circuitry is fed by a separate power supply.

The I<sup>2</sup>C clock (SCL) signal is bidirectional and clock stretch is required. The PD77718T4, PD77718T3, or PD77714T4 has a typical I<sup>2</sup>C clock frequency of 600 KHz, but up to 1 MHz is supported.

There are additional control signals between the PD77010 Controller and the PD77718 Managers. This is shown in the following figure.

**Figure 2-2.** Communication Interfaces



### 2.1.1 Control Signals between the Host CPU and PD77010 Controller

**xDISABLE\_PORTS:** Active-low signal driven by the Host CPU disables all the PoE ports. When the PD77010 Controller detects a low level voltage at xDISABLE\_PORTS, it sends a disable command through the I<sup>2</sup>C bus to all the PD77718T4, PD77718T3, or PD77714T4 PoE Manager ports.

**xRESET\_IN:** Active-low signal driven by the Host CPU resets the PD77010 PoE Controller and all the PD77718T4, PD77718T3, or PD77714T4 PoE Managers. When the PD77010 device detects a low-level voltage at xRESET\_IN, it enters the reset mode and all of its output pins switch to tri-state mode. When the Reset returns to high, the PoE controller initializes and sends a RESET command to the PD77718T4, PD77718T3, or PD77714T4 PoE managers through the I<sup>2</sup>C bus. Connect a 10 K $\Omega$  pull-up resistor to xRESET\_OUT on the PD77010 controller and to xRESET\_IN\_N on the PD77718 managers. A 47 nF filter capacitor must be connected between this pin and GND and located close to the device.

**xSYS\_OK:** Signal is generated by the PD77010 PoE Controller, indicating that the main input voltage is within range. This pin's function is determined by a 15-byte serial communication protocol. This pin is active-low.

**xINT\_OUT:** Interrupt output indication. This line is asserted low when a preconfigured event is in progress. The Host configures the events that generate an interrupt through the 15-byte protocol. When this event occurs, the xINT\_OUT pin is asserted. This pin is active-low.

**xI2C\_MESSAGE:** I<sup>2</sup>C message ready for reading by the host. The PD77010 Controller asserts this line low to indicate a message is ready to be read by the host. Therefore, the host can poll this line and initiate I<sup>2</sup>C read cycle only when the message is ready. This pin is active-low. After the host reads the data from the controller, this pin is asserted high.

### 2.1.2 Control Signals/Buses between the PD77010 Controller and PD77718 Managers

**OSS:** OSS is used to implement two functions as follows:

1. Fast Dynamic system Over Budget disconnect.
2. Fast Disconnect code in case of PD77010 power good change.

OSS is used to turn off the lower priority ports due to live removal or failure of one of the power supplies, or when dynamic over power is above the active budget by more than 5%.

The power budget and reallocation of the power based on priority (if there is a loss of a power supply) is defined through the Power Good pins.

The bus is always operational even when using a single power supply. The OSS pin of the PD7771x devices must be connected to the OSS\_OUT of the PD77010 device through high frequency digital isolation.

**INTERRUPT:** The INTERRUPT bus is xINT\_IN to the PD77010 and INT\_OUT\_N from the PD77718. The signal must be connected between all PD7771x devices and isolated from the PD77010. For future use. It is recommended that the PCB design route these functions, however the isolator may be a “do not populate” option.

**RESET:** The RESET bus is xRESET\_OUT from the PD77010 and RESET\_IN\_N to the PD77718. The signal must be connected between all PD7771x devices and isolated from the PD77010. For future use. It is recommended that the PCB design route these functions, however the isolator may be a “do not populate” option.

## 2.2 Emergency Power Management

PoE circuits can be powered by up to four separate power supplies. It is recommended that each power supply is capable of generating a logic signal, indicating its operate/fail status.

The following table lists the PD77010 pins used for emergency power management.

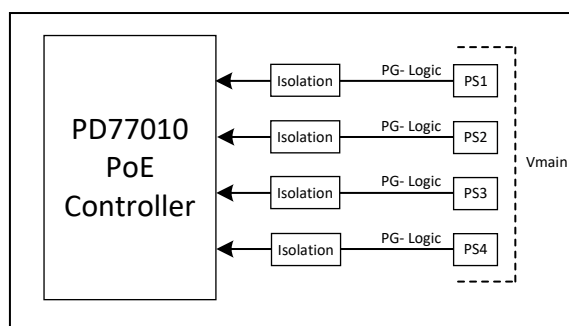
**Table 2-1.** Emergency Power Management Pins

PD77010 Pin Number	Signal	Description
17	PG1	Power Good 1
18	PG2	Power Good 2
19	PG3	Power Good 3
20	PG4	Power Good 4

The PoE circuit allocates power to the system in four programmed power levels (power banks). Power bank values are based on each supplies' available power and on the state of the logic signals PG[1..4] coming from power supplies. If PG is not used, the pins should be tied to GND.

The following figure shows the connections between the logic signals of the power supplies and the PoE Controller.

**Figure 2-3.** Power Good



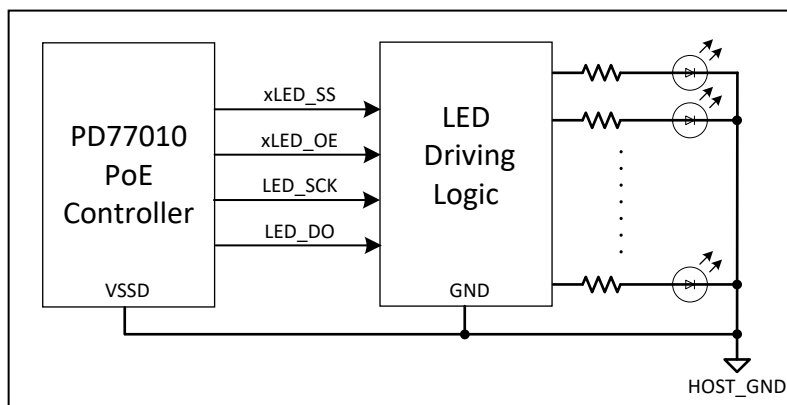
**Note:** The system  $V_{MAIN}$  capacitor must hold the voltage from dropping for 70  $\mu$ s until the emergency power management reacts.

## 2.3 LED Support

LED support for port status indication is accomplished by utilizing the LED\_SCK, xLED\_SS, LED\_DO, and xLED\_OE signals on the PD77010 controller. Bus behavior is 1 MHz synchronous serial communication (clock and data) in one direction (write only) that transmits the status up to 48 logical ports. The LED driving logic for two PD77718T4 or PD77718T3 devices is shown in Figure 6-5 and Table 7-3.

The following figure shows the LED support.

Figure 2-4. LED Support



## 2.4 Powering

The following sections describe powering.

### 2.4.1 PD77010 Supply

The PD77010 PoE Controller requires a regulated and filtered power for its operation coming from the system 3.3V supply in the Host Domain (3\_3V\_iso), so a number of decoupling capacitors are included in the design. The typical current consumption of the PD77010 PoE controller circuitry is below 20 mA.

Additionally, the PD77010 internal 1.2V VDD\_CORE voltage requires decoupling capacitors. These decoupling capacitors must be layout close to pin 29 VDD\_CORE.

### 2.4.2 PD77718T4, PD77718T3, or PD77714T4 Supply

The PD77718T4, PD77718T3, or PD77714T4 requires a regulated 3.3V and filtered power supply in the PoE domain for operation. Connect this power supply to VDD, pin 43. The VDDA, pin 22 must be connected with a single point connection to VDD close to pin 43 and not to PCB VDD general plane, see Figure 8-6. There must be decoupling capacitors placed close to both VDD and VDDA pins. The typical current consumption is below 30 mA.

Additionally, the PD77718T4, PD77718T3, or PD77714T4 1.8V (VREG1P8) and 1.2V (VDDCORE) internal voltage regulators require decoupling capacitors. These decoupling capacitors must be placed close to the respective pins.

### 2.4.3 Main Supply

The PoE system operates within a range of 44 V<sub>DC</sub> – 57 V<sub>DC</sub> (IEEE 802.3at/bt V<sub>MAIN</sub> range is 50 V<sub>DC</sub>–57 V<sub>DC</sub>). To comply with the UL SELV regulations, the maximum output voltage must not exceed 60 V<sub>DC</sub>.

The main PoE power supply is connected at V<sub>MAIN</sub> pin 17. For basic levels of surge protection (<math>\leq 2\text{kV}</math>), connect the PoE power supply to both VMAIN\_7 pin 7 and VMAIN\_36 pin 36. For Enhanced levels of surge protection (>2 kV), leave pin 7 and 36 floating. For more information, request for AN4813 *Surge Protection for Systems Based on PD777xx PSE PoE Manager*.

## 2.4.4 Hot-Swap Circuit

The hot-swap circuit is crucial for applications where DC hot plug is present because absence of such a circuit causes the DC voltage to oscillate (ring), which may lead to application malfunctions.

The hot-swap circuit based on [MIC2587](#) for a system with 12 PD77718T4, PD77718T3, or PD77714T4 devices is shown in [Figure 6-8](#) and [Table 7-6](#). Consult Microchip for an option based on a discrete solution.

## 2.4.5 Grounds

Several grounds are utilized in the system: PoE domain analog (AGND) and local analog (LAGND), PoE domain digital (DGND) and local digital (LDGND), chassis, and host domain floating. See [Figure 8-6](#) and [Figure 8-9](#).

**AGND:** The negative rail of input PoE is termed as AGND. Connect the PD77718T4, PD77718T3, or PD77714T4 device EPAD to AGND.

**LAGND:** Quiet local AGND use for each individual PD77718T4, PD77718T3, or PD77714T4 to have a low current quiet connection to IREF (pin 14), VMAIN (pin 17), and VDDA (pin 22) decoupling capacitors. To avoid current loops, LAGND must be connected in a single point to AGND near the PD77718T4, PD77718T3, or PD77714T4 EPAD. LAGND must be connected to DGND through a 470 nF and 1 nF capacitor and optional back to back diodes. See [Figure 8-6](#).

**DGND:** The ground connection used for PD77718T4, PD77718T3, or PD77714T4 digital signals (pins 43 to 56) is DGND. The decoupling capacitors connected to VDD and VDDCORE pins are connected to DGND.

**LDGND:** The ground connection for VREG1P8 decoupling capacitors is LDGND. Connect LDGND and DGND at single point.

All these grounds—AGND, LAGND, DGND, and LDGND—are the same ground, electrically. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

The power supplies AGND ground connector enables a current path back to the power supply. The ground connection must be capable of carrying all current back to power supplies.

**Host Domain Floating:** The PD77010 PoE controller relates to the host domain floating ground, which is isolated from the PoE domain grounds.

**Chassis Ground:** The chassis ground is connected to the chassis ground of the switch. This ground plane must be 1500 V<sub>RMS</sub> isolated from PoE circuitry.

### 3. PoE Manager Circuitry

This section describes the PoE Manager circuitry.

#### 3.1 PD77718T4, PD77718T3, or PD77714T4 Circuitry

The PD77718T4, PD77718T3, or PD77714T4 performs a variety of internal operations and PoE functions, requiring a minimal number of external components. For PD77718T4, PD77718T3, or PD77714T4 device configuration in Controller mode, see [Controller Mode](#).

##### 3.1.1 Reference Current Source

The reference for internal voltages within the PD77718T4, PD77718T3, or PD77714T4 is set by a precision resistor, 10 k $\Omega$ . The resistor precision must be 0.1%.

##### 3.1.2 Port Channel Resistance

The total channel resistance of a PD77718T4, PD77718T3, or PD77714T4 port is 160 m $\Omega$  (typical). This resistance includes sense resistor and MOSFET  $R_{DS(on)}$ .

##### 3.1.3 Front-End Components

A front-end, per-line capacitor is required. The capacitor is a 100V capacitor with a value between 47 nF and 220 nF. All other components such as reverse diode, port protection, sense resistor, and switching MOSFET are internal.

#### 3.2 Line Transformer

A line transformer that is dedicated to PoE (with consideration to the desired PoE current for the specific applications) must be used.

## 4. PoE Manager I<sup>2</sup>C

The port I<sup>2</sup>C address is programmed through pins A0, A1, A2, A3 (pins 48–51). Tie each pin to VDD or DGND to set the I<sup>2</sup>C address, as listed in the following table.

**Note:** The I<sup>2</sup>C address is a 7-bit address.

**Table 4-1.** PD77718T4, PD77718T3, and PD77714T4 I<sup>2</sup>C Address Select

A3	A2	A1	A0	I <sup>2</sup> C Address
0	0	0	0	0x20
0	0	0	1	0x21
0	0	1	0	0x22
0	0	1	1	0x23
0	1	0	0	0x24
0	1	0	1	0x25
0	1	1	0	0x26
0	1	1	1	0x27
1	0	0	0	0x28
1	0	0	1	0x29
1	0	1	0	0x2A
1	0	1	1	0x2B
1	1	0	0	0x2C
1	1	0	1	0x2D
1	1	1	0	0x2E
1	1	1	1	0x2F

## 5. 4-Pair Ports for IEEE 802.3bt

This section describes the basic steps to configure PSE systems to support IEEE 802.3bt 4-pair applications based on the PD77718T4, PD77718T3, or PD77714T4 device.

### 5.1 Background

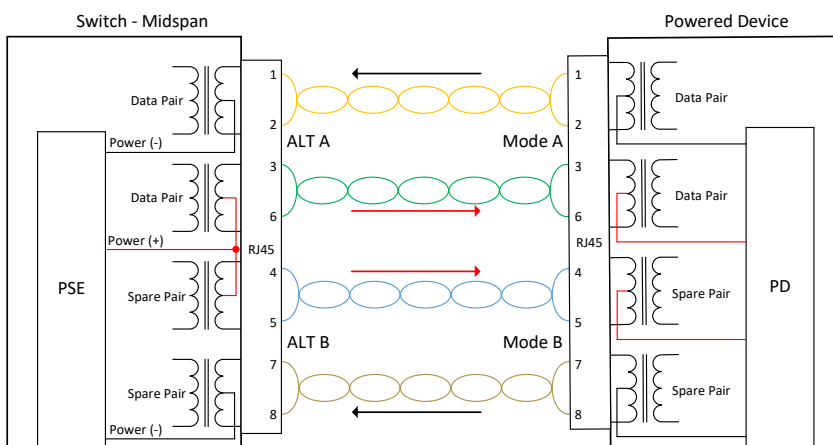
The IEEE 802.3af standard describes Power Source Equipment (PSE) power of 15W over 2-pair and the IEEE 802.3at standard describes PSE power of 30W over 2-pair. The IEEE 802.3bt-2018 standard, introduced the Type 3 and Type 4 PSE/PD capable of supporting 60W/90W output power.

To support this increase in the maximum PoE power supplied by the PSE to the Powered Device (PD), the IEEE 802.3bt-2018 standard defines 4-pair ports, which utilize all four pairs of the structured RJ45 wires.

The PD77718T4 or PD77714T4 supports up to 30W per 2-pair or 90W per 4-pair (Type 3 or Type 4). The PD77718T3 supports up to 30W per 2-pair or 60W per 4-pair (Type 3).

The Data Pair is defined as **Alternative A** at the PSE side and **Mode A** at the PD side. The Spare Pair is defined as **Alternative B** at the PSE side and **Mode B** at the PD side. This is illustrated in the following figure.

Figure 5-1. PoE 4-Pair Architecture



### 5.2 Hardware Setup

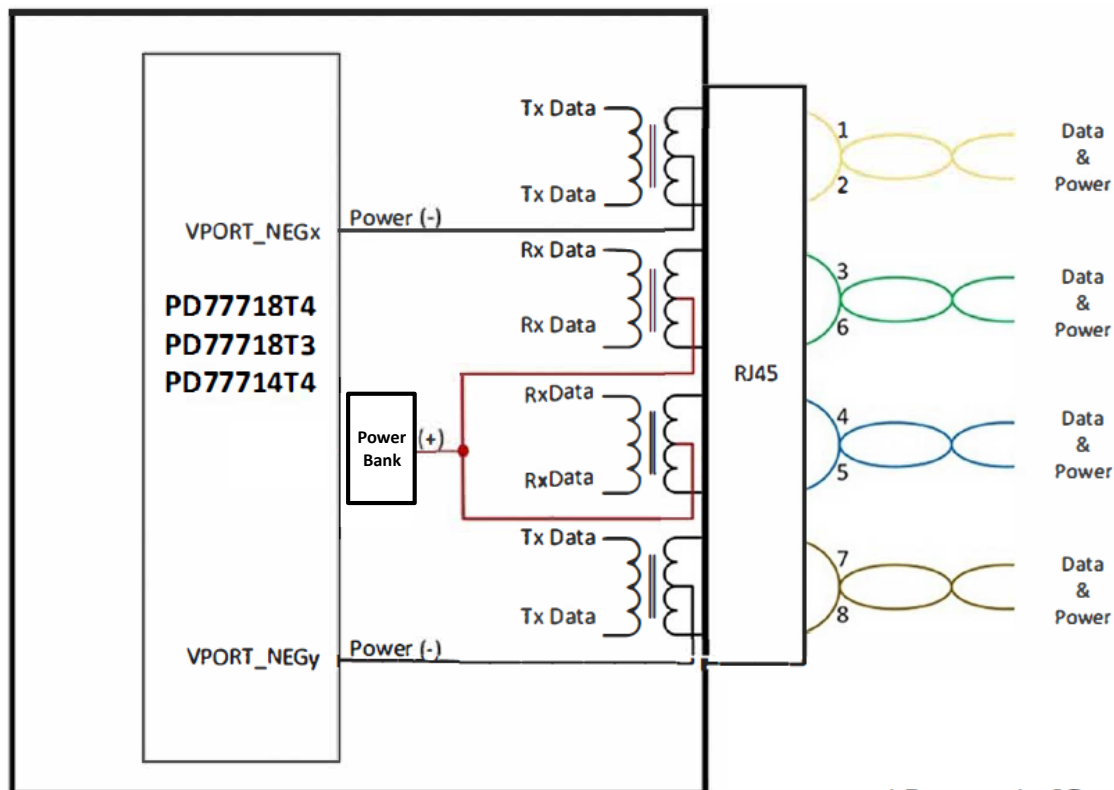
The following sections describe how to set up the hardware.

#### 5.2.1 PSE

When operating in 4-pair, power is delivered to the PD on both pair sets (ALT-A and ALT-B), that is, two physical ports are combined to create a single logical 4-pair port required for the 4-pair operation. When operating in 4-pair mode, the two physical ports that create the one logical four pair port must be chosen from the same physical PD77718T4, PD77718T3, or PD77714T4 IC.

This configuration is shown in the following figure.

**Figure 5-2.** 4-Pair Implementation



**Note:** VPORT\_NEG<sub>x,y</sub> should be from the same physical PD77718T4, PD77718T3 or PD77714T4 IC.

### 5.2.2 Polarity

Type 4 is limited to a “fixed polarity”, that is the IEEE 802.3bt strictly defines the connection of the positive  $V_{MAIN}$  voltage and return (PORT\_NEG) paths to the physical pairs. For Type 3 applications, the standard is flexible, allowing a variety of connection options. See the following table.

**Table 5-1.** Allowed Polarity

Pair Set	TIA/EIA 568-A	TIA/EIA 568-B	Alternative	Type 3			Type 3 or Type 4
				Option 1	Option 2	Option 3	
1-2	Green	Orange	Data (Alt A)	PORT_NEGx	VMAIN	VMAIN	PORT_NEGx
3-6	Orange	Green		VMAIN	PORT_NEGx	PORT_NEGx	VMAIN
4-5	Blue	Blue	Spare (Alt B)	PORT_NEGy	PORT_NEGy	VMAIN	VMAIN
7-8	Brown	Brown		VMAIN	VMAIN	PORT_NEGy	PORT_NEGy

### 5.2.3 PD Side

The following figures describe how to physically connect 4-pair ports to a Signal Signature PD and how to physically connect to a Dual Signature PD.

Figure 5-3. PD 4-Pair SSPD Implementation

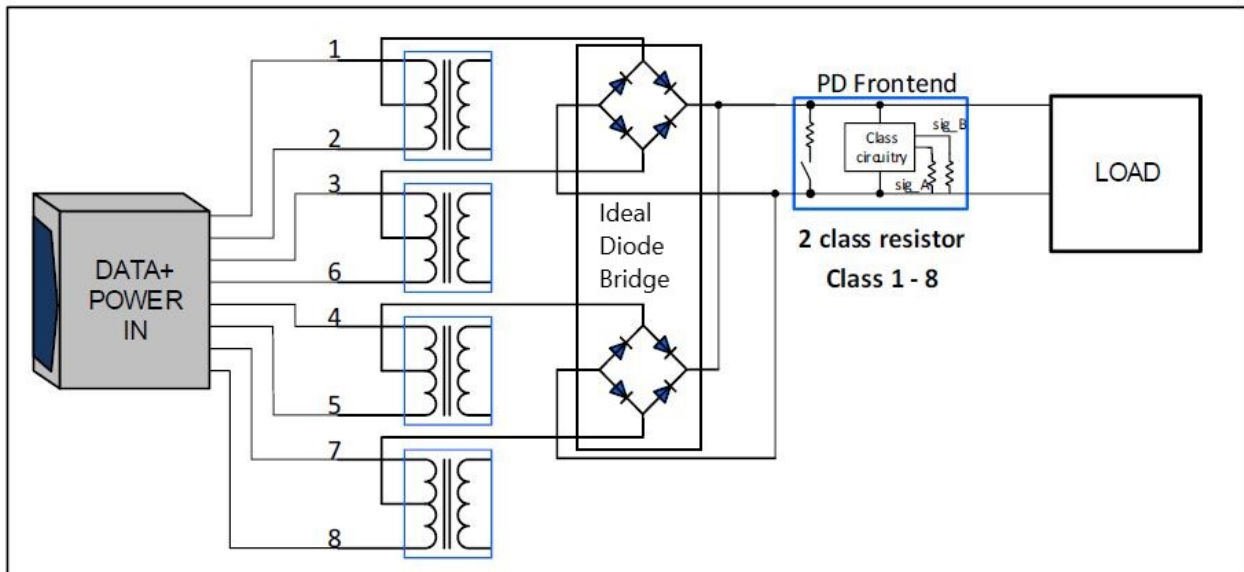
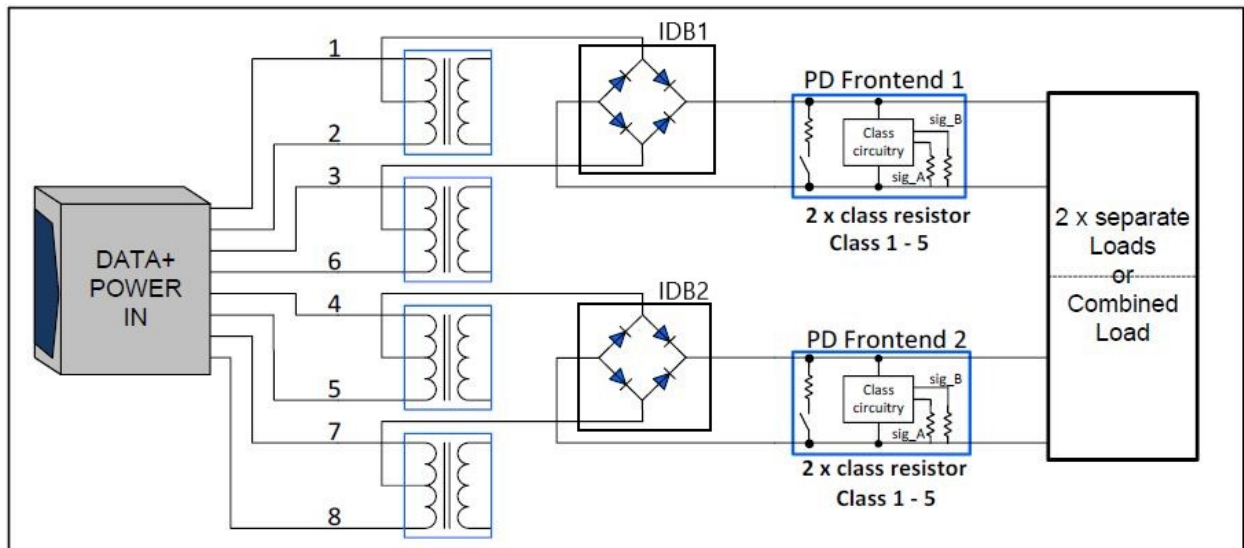


Figure 5-4. PD 4-Pair DSPD Implementation



## 6. Schematics

The following section shows the detailed device-level schematic.

### 6.1 Controller Mode

The following section shows the detailed device-level schematic of a 8-physical port system based on two PD77718T4 or PD77718T3 devices, operating in Controller Mode. This schematic meets 2 kV basic surge requirements as defined in EN 61000-4-5:2014. For a higher level of surge protection, request for *AN4813: Surge Protection for Systems Based on PD777xx 8-Port PSE PoE Manager*.

Figure 6-1. System Main Blocks – Controller Mode

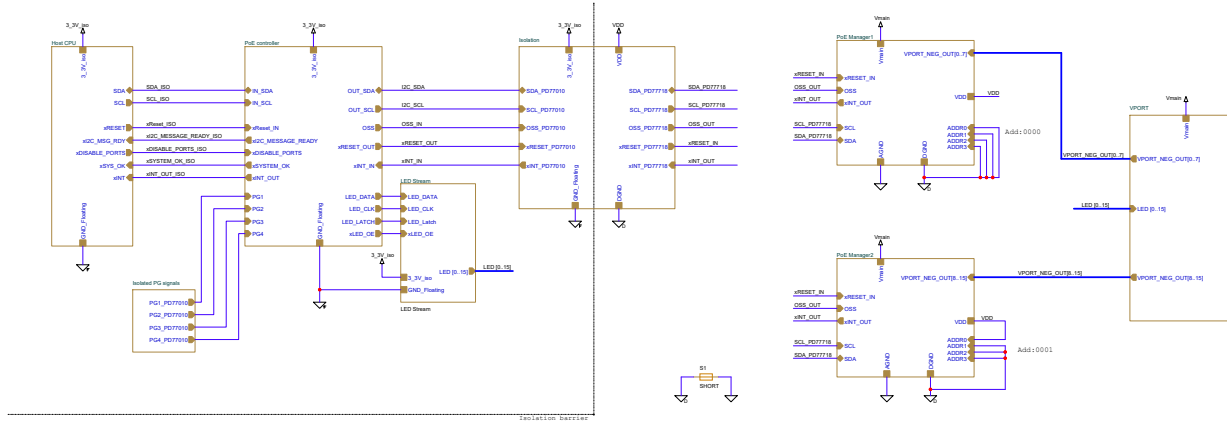
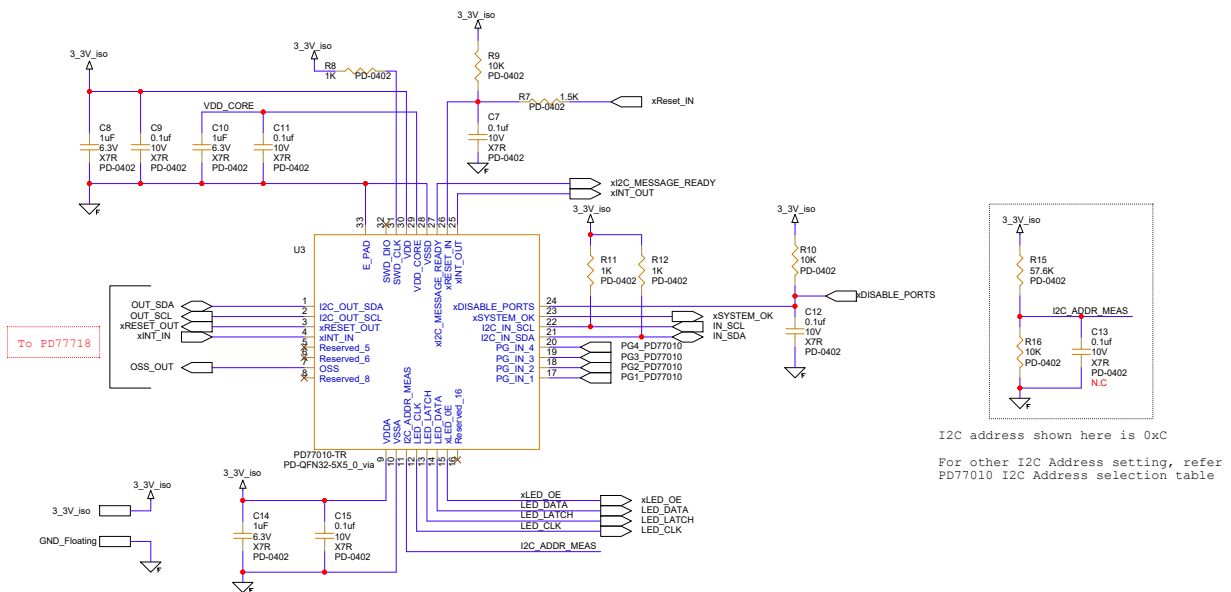
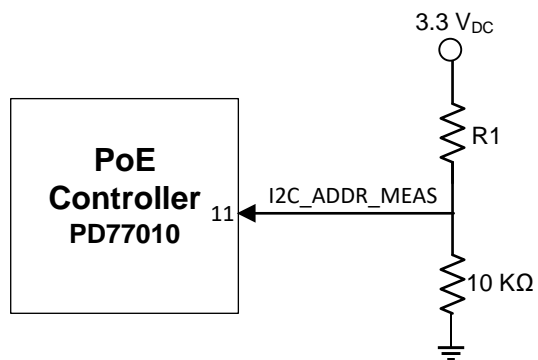


Figure 6-2. PD77010 Controller Circuitry - Controller Mode



**Figure 6-3.** PD77010 I<sup>2</sup>C Address Selection

The following table lists the specific value of R1 to set the I<sup>2</sup>C address.

**Table 6-1.** PD77010 I<sup>2</sup>C Address Selection

I <sup>2</sup> C Address (Hexadecimal)	R1-KΩ
0x4	147
0x8	86.6
0xC	57.6
0x10	43.2
0x14	34
0x18	26.7
0x1C	22.1
0x20	18.2
0x24	15.4
0x28	13
0x2C	11
0x30	9.31
0x34	7.87
0x38	6.49
0x3C	5.49

Figure 6-4. PD77718T4 or PD77718T3 Manager Circuitry - Controller Mode

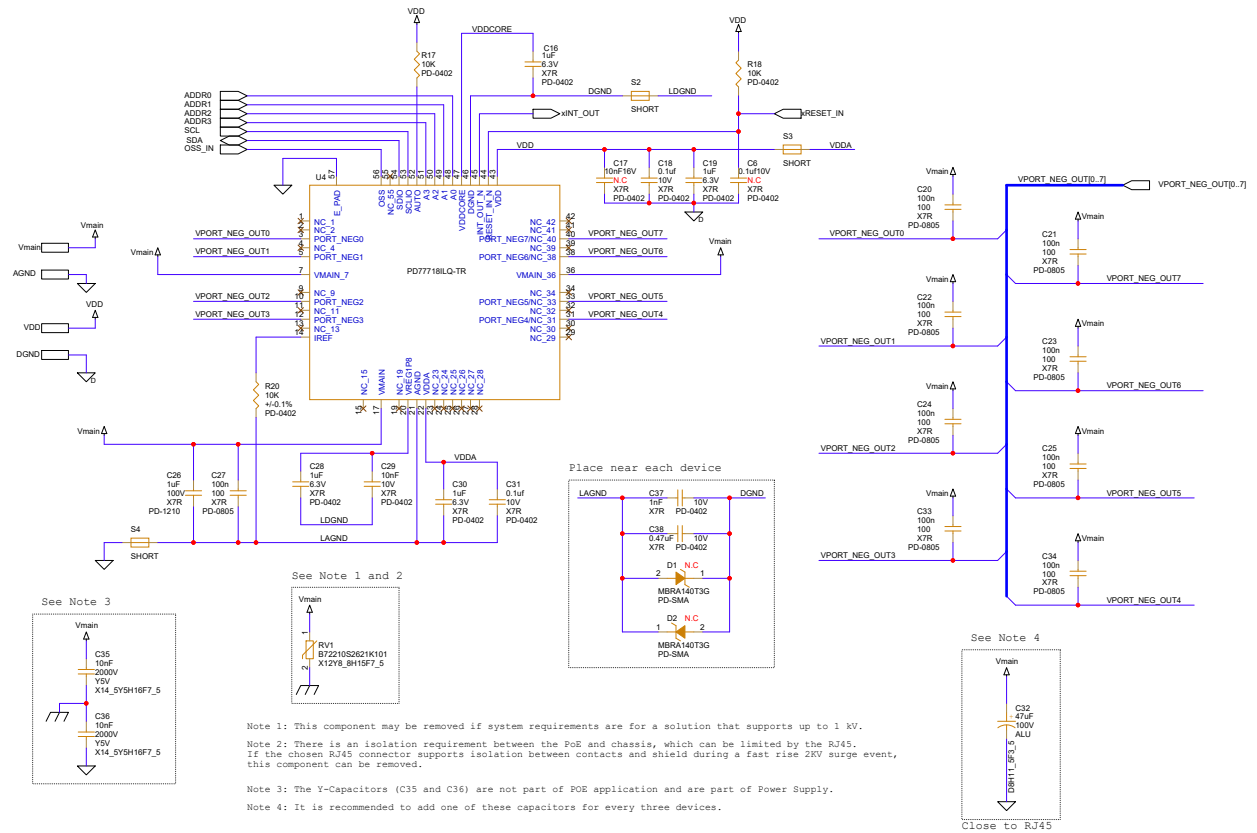


Figure 6-5. LED Stream Circuitry

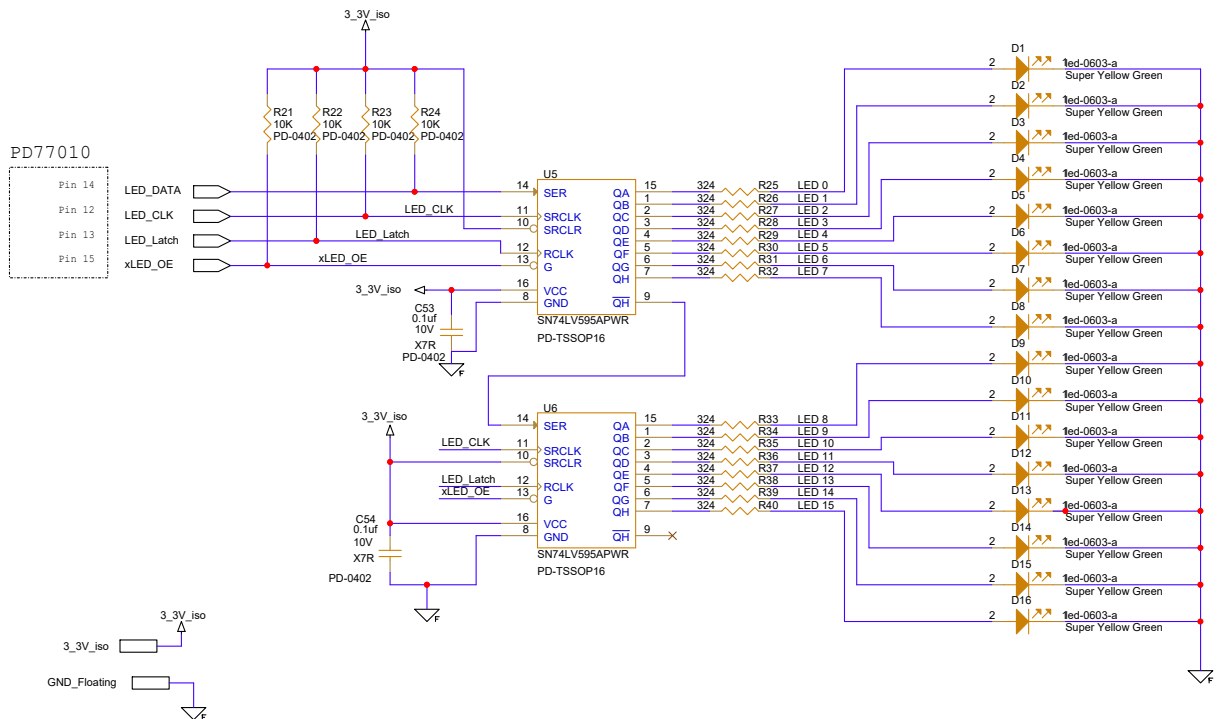


Figure 6-6. Digital Isolation Circuitry - Controller Mode

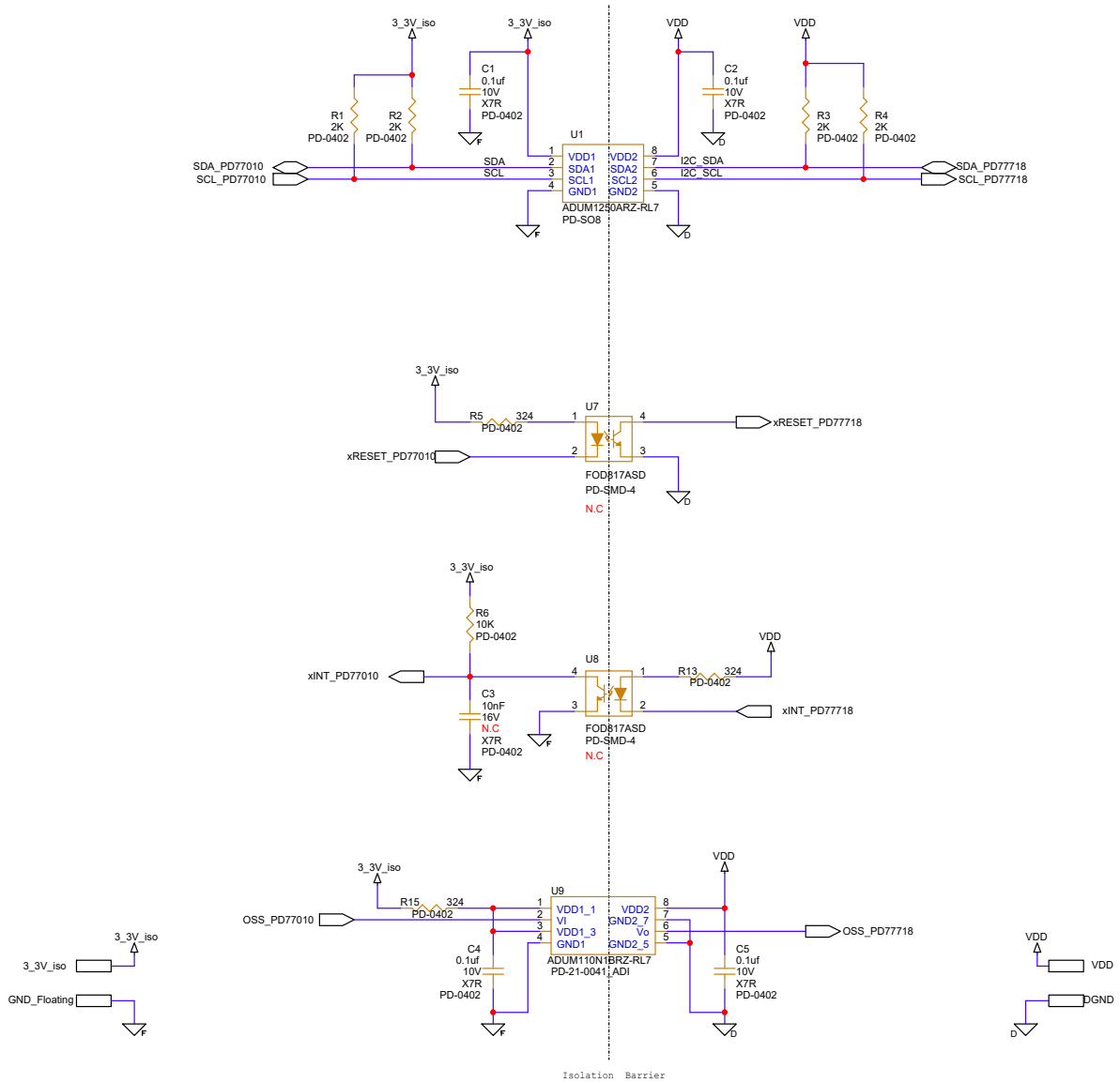


Figure 6-7. Power Good Isolation Circuitry

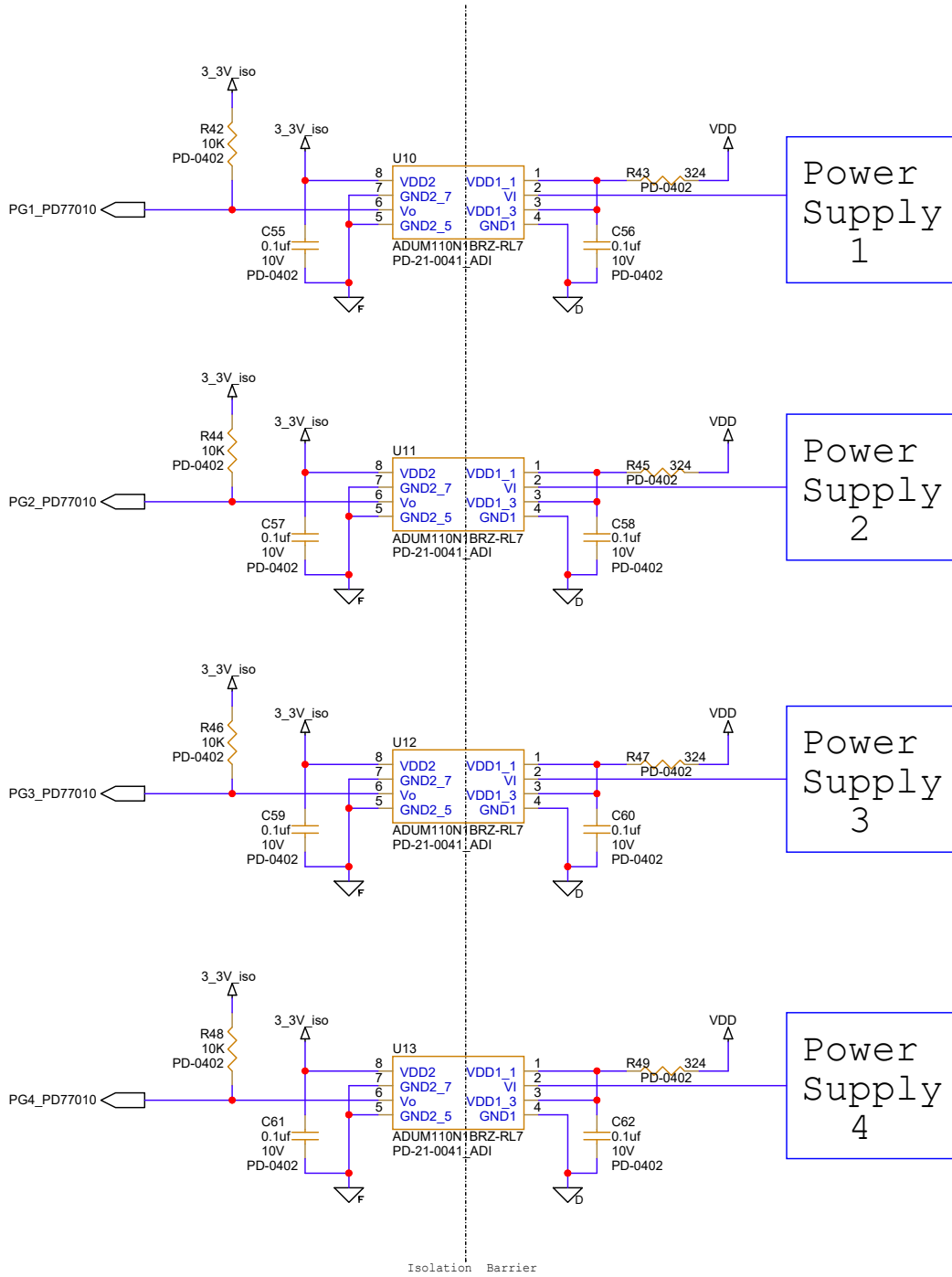
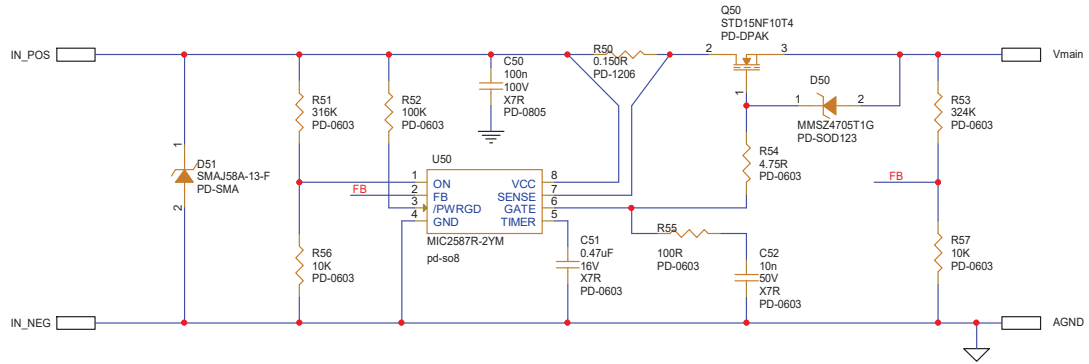


Figure 6-8. Hot-swap Circuit Based on MIC2587



## 7. Bill of Materials

The following section shows the detailed bill of materials.

### 7.1 Controller Mode

The following section shows the Bill of Material (BOM) for Controller Mode.

**Table 7-1.** PD77010 Controller Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
5	C7, C9, C11, C12, C15	0.1 uF	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Nic Components	NMC0402X7R104K10TRP
3	C8, C10, C14	1 uF	CAP CER 1 uF 6.3V X7R 0402	Yageo	CC0402KRX7R5BB105
3	R9, R10, R16	10K	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-1002GLF
3	R8, R11, R12	1K	RES TCK FLM 1K 1% 62.5 mW 0402 SMT 100 PPM	Royal Electronic Factory Co.,Ltd.	0402WGF1001TCE
1	R7	1.5K	RES TCK FLM 1.5K 1% 62.5mW 0402 SMT 100 PPM	Walsin	WR04X1501FTL
1	R15	57.6K	Resistor, 57.6K, 1%, 1/16W 0402	Rohm	MCR01MZPF5762
1	U3	PD77010	PD77010 PoE PSE Controller	Microchip	PD77010-VVVV-SSSS-TR <sup>(1,2)</sup>

#### Notes:

1. Firmware revision.
2. Firmware parameters options.

**Table 7-2.** PD77718T4, PD77718T3, or PD77714T4 Manager Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C16, C19, C28, C30	1 uF	CAP CER 1 uF 6.3V X7R 0402	Samsung	CL05B105KQ5NQNCC
2	C18, C31	0.1 uF	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Walsin	0402B104K100CT
9	C20, C21, C22, C23, C24, C25, C27, C33, C34	100n	Capacitor, X7R, 100 nF 100V 10% 0805	Samsung	CL21B104KCF5FNE
1	C26	1 uF	CAP CER 1 uF 100V 10% X7R 1210 SMT	AVX	12101C105KAT2A
1	C29	10 nF	Capacitor, CER, X7R, 10 nF 10V 10% 0402 SMT	Yageo	CC0402KRX7R6BB103
1	C32	47 uF	CAP ALU 47 uF 100V 20% 8X11.5 105C P = 3.5 mm T/H	Rubycon	100PX47MEFC T7 8X11.5
2	C35, C36*	10 nF	CAP CER 10 nF 2KV +80-20% P =7.5, D = 14.5	TDK	CK45-E3DD103ZYGNA
1	C37	1 nF	Capacitor, CER, X7R, 1 nF 10V 10% 0402 SMT	Walsin	0402B102K100CT
1	C38	0.47 uF	CAP CER 0.47UF 10V X7R 0402 SMT	Yageo	CC0402KRX7R6BB474
1	RV1	B72210S2621K101	VARISTOR 625 VRMS, 825 VDC 3.5KA 10 MM	EPCOS	B72210S2621K101

**Table 7-2.** PD77718T4, PD77718T3, or PD77714T4 Manager Circuitry Components (continued)

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
2	R17, R18	10K	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-1002GLF
1	R20	10K	RES 10 KΩ 0.1% 1/16W 0402 SMT	Stackpole Electronics Inc	RNCF0402BTE10K0
1	U4	PD77718T4, PD77718T3, or PD77714T4,	IC PSE Manager	Microchip	PD77718T4ILQ-VVVV-SSSS-TR, PD77718T3ILQ-VVVV-SSSS-TR, or PD77714T4ILQ-VVVV-SSSS-TR

**Notes:**

- \*The Y-capacitors (C35 and C36) are not part of PoE application and are part of Power Supply.
- \*\* Use one capacitor per three PD77718 devices

**Table 7-3.** LED Stream Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
2	C53, C54	0.1 uF	CAP CER 0.1uF 10V X7R 10% 0402 SMT	Kemet	C0402C104K8RAC
4	R21, R22, R23, R24	10 KΩ	RES TCK FLM 10K 1% 62.5mW 0402 SMT	Bourns	CR0402-FX-1002GLF
16	R25-R40	324Ω	RES 324R 62.5mW 1% 0402 SMT Thick Film	Yageo	RC0402FR-07324RL
16	D1-D16	19-21SY GC/S530-E3/4T	LED SuperYelGrn 100-130o 20-40mcd h=1 0603 SMD	Everlight	19-21SYGC/S530-E3/4T
2	U5, U6	SN74LV595APWR	IC 8-BIT SHFT REG TRI-ST16-TSSOP	Texas Instruments	SN74LV595APWR

**Table 7-4.** Digital Isolation Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C1, C2, C4, C5	0.1 uF	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Nic Components	NMC0402X7R104K10TRP
4	R1, R2, R3, R4	2K	RES TCK FLM 2K 1% 62.5 mW 0402 SMT	Yageo	RC0402FR-072KL
1	R6	10K	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-1002GLF
2	R5, R13, R15	324	RES 324R 62.5mW 1% 0402 SMT Thick Film	Yageo	RC0402FR-07324RL
1	U1	ADUM1250ARZ-RL7	IC Hot-Swap I <sup>2</sup> C Isolator 2Ch Bi-Direct SO-8	Analog Devices	ADUM1250ARZ-RL7
1	U1 [Alternative]	ADUM1254ASA+	Bidirectional I <sup>2</sup> C Isolator with Idle-Bus Hot-Swap and Low VOL SOIC-8	Analog Devices	ADUM1254ASA+
1	U9	ADUM110N1BRZ-RL7	Single-Channel Digital Isolator, 1.7V-5.5V, 3KV Fail-Safe Output State High SOIC-86	Analog Devices	ADUM110N1BRZ-RL7

**Table 7-5.** Power Good Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
8	C55-C62	0.1 uF	CAP CER 0.1 uF 10V X7R 10% 0402 SMT	Nic Components	NMC0402X7R104K10TRP
4	R43, R45, R47, R49	324	RES 324R 62.5 mW 1% 0402 SMT Thick Film	Yageo	RC0402FR-07324RL

**Table 7-5. Power Good Circuitry Components (continued)**

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	R42, R44, R46, R48	10K	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	Bourns	CR0402-FX-1002GLF
4	U10-U13	ADUM110N1BRZ-RL7	Single-Channel Digital Isolator, 1.7V-5.5V, 3KV Fail-Safe Output State High SOIC-8	Analog Devices	ADUM110N1BRZ-RL7

**Notes:** Optional components for isolation, depending on hardware configuration:

- ADUM1200 dual channel
- ADUM1300 triple channel
- ADUM1400 quad channel

**Table 7-6. Hot-Swap Circuit Based on MIC2587**

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	C50	100n	Capacitor, X7R, 100 nF 100V 10% 0805	Vishay	VJ0805Y104KXBAT
1	C51*	0.47 uF	Capacitor, X7R, 0.47 μF, 16V, 10% 0603	Samsung	CL10B474KO8NNNC
1	C52	10n	CAP CRM 10 nF 50V 10% X7R 0603 SMT	Samsung	CL10B103KB8NNNC
1	D50	MMSZ4705T1G	DIODE ZENER 18V 500MW SOD-123	ON-Semiconductor	MMSZ4705T1G
1	D51	SMAJ58A-13-F	DIO TVS 58V 40A SRG400WPK SMA SMT	Diodes Inc.	SMAJ58A-13-F
1	Q50	STD15NF10T4	TRN FET NCH 100V 23A0.065R D-PAK	ST Microelectronics	STD15NF10T4
1	R50*	0.150R	RES 0.15 OHM 1/4W 1% 75 ppm 1206 SMT	Vishay	WSL1206R1500FEA
1	R51	316K	Resistor, 316K, 1%, 1/16W 0603	ASJ	CR16-3163FL
1	R52	100K	RES 100K 62.5 mW 1% 0603 SMT MTL FLM	Panasonic	ERJ3EKF1003V
1	R53	324K	RES TCK FLM 324K 62.5 mW 1% 0603 SMT	Samsung	RC1608F3243CS
1	R54	4.75R	RES 4.75R 0.1W 1% 0603 SMT MTL FLM	Samsung	RC1608F4R75CS
1	R55	100R	RES TCK FLM 100R 62.5 mW 1% 0603 SMT	Yageo	RC0603FR-07100RL
2	R56, R57	10K	RES 10K 62.5 mW 1% 0603 SMT MTL FLM	Yageo	RC0603FR-0710KL
1	U50	MIC2587R-2YM	IC HOT SWAP CTRLR GP 8SOIC	Microchip	MIC2587R-2YM

**Note:** \*The resistor and capacitor value must be tuned as per the application current limit. A system with 12 PSE Managers is considered as an example here. Contact Microchip for design guidance.

## 8. Layout Guidelines

This section provides detailed information and PCB design guidelines for the implementation of a PoE system based on Microchip's PD77718T4, PD77718T3, or PD77714T4 PoE Manager.

### 8.1 Isolation and Termination

According to PoE standards, certain isolation requirements need to be met in all the PoE equipment. In addition, EMI limitations must be considered, as specified in the FCC and European EN regulations. These requirements are considered by the PoE switch vendors while designing the switch circuitry. However, when a PoE manager is integrated into a switch, special design considerations must be met because of the unique combination of data and power circuitries.

The following sections define the requirements and provide recommendations for their implementation to assist designers in meeting those requirements, while also integrating Microchip's PoE chipset.

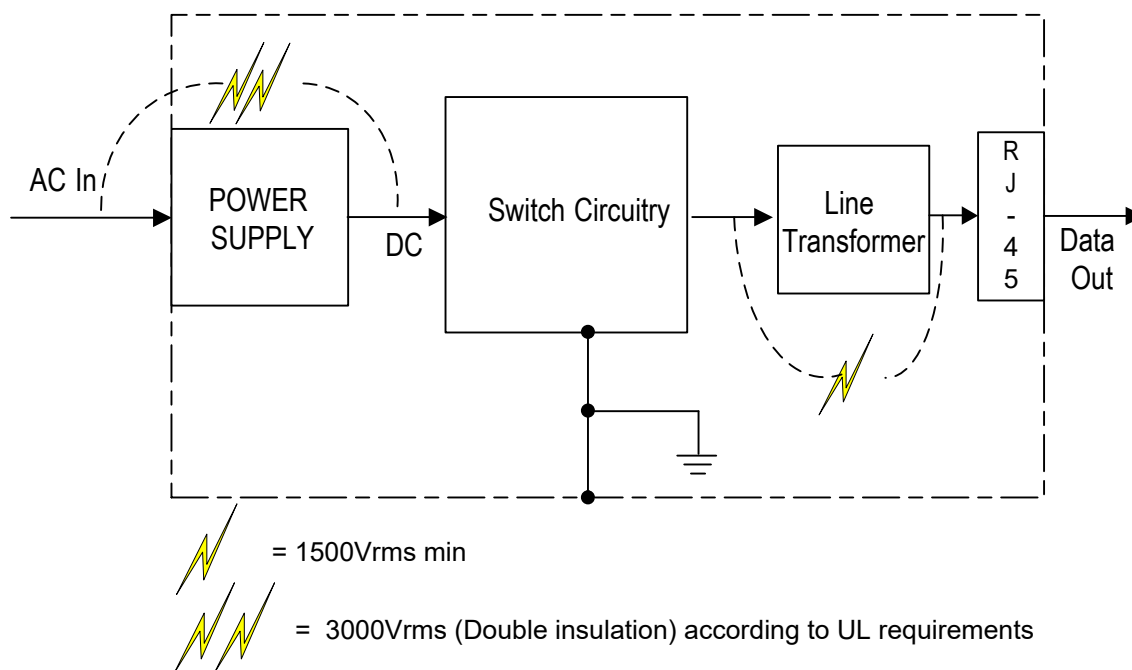
#### 8.1.1 Isolation

As specified in the IEEE PoE standards, 1500 V<sub>RMS</sub> isolation is required between the switch's main board circuitry (including protective and frame ground) and the Media Dependent Interface (MDI).

#### 8.1.2 High-Voltage Isolation

For a switch with no PoE circuitry, isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated line transformers, as shown in the following figure.

Figure 8-1. Standard Switch Circuitry

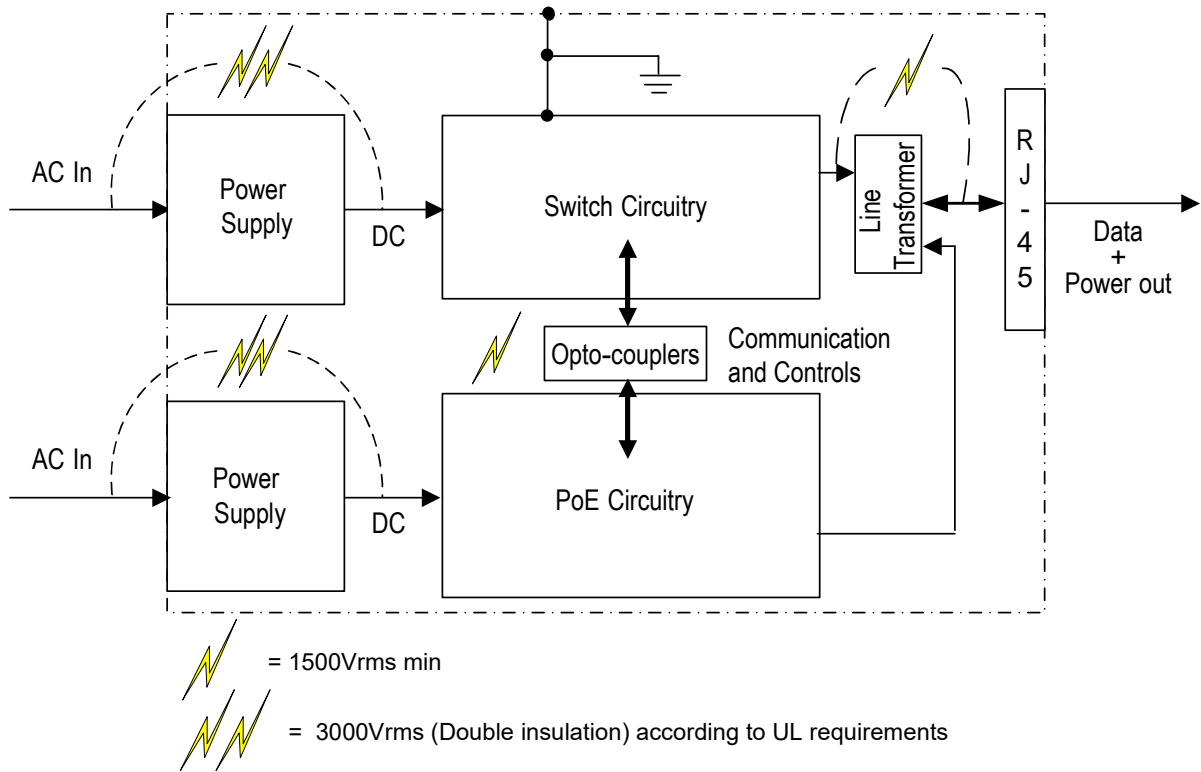


When integrating PoE circuitry into a switch, the output power can be supplied through the central tap of the line transformer's secondary side. This connectivity can bypass the line transformer's isolation if the PoE ground or DC input is connected to the switch's circuitry/ground.

To comply with these isolation requirements, the PoE managers must be isolated in regard to all other switch circuitries. Use one of the following two methods.

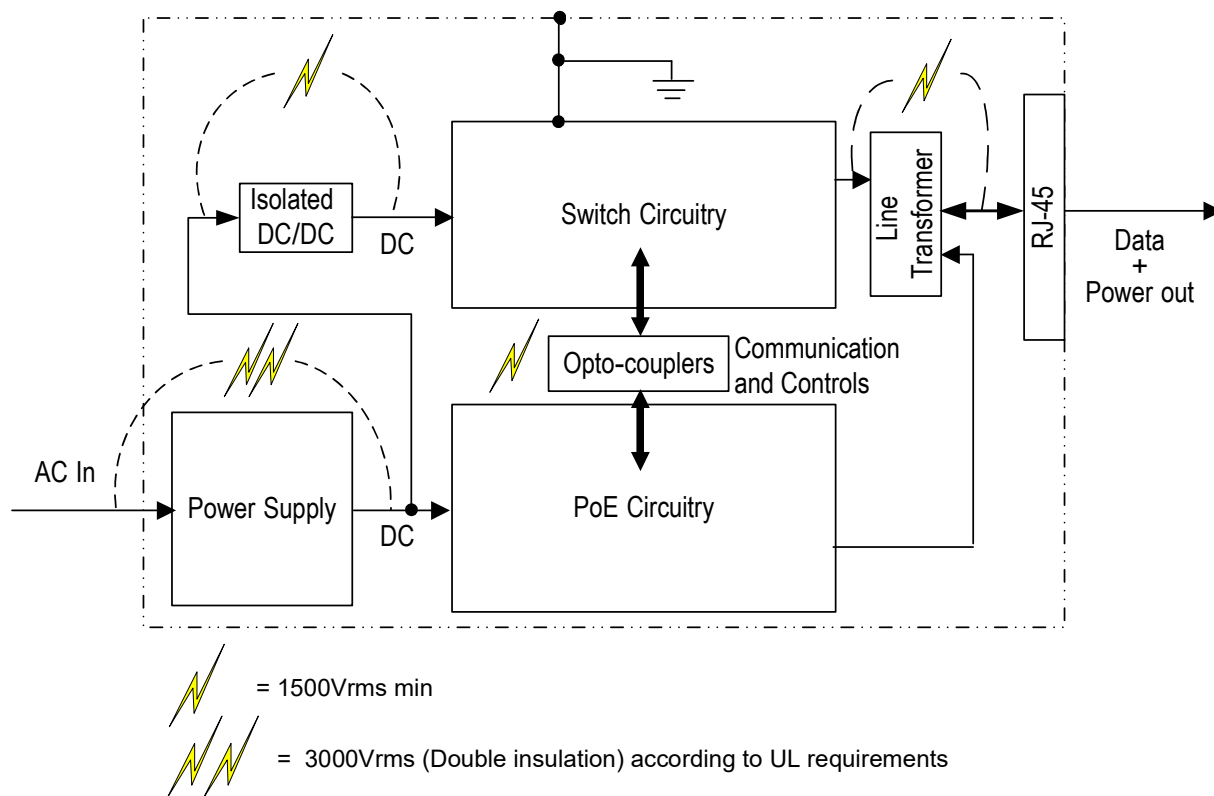
**Method 1:** Use a separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry, as shown in the following figure.

**Figure 8-2.** Switch Circuitry with Two DC Source



**Method 2:** Use a single system AC/DC PSU for the switch and PoE circuit while isolating the switch with additional isolated DC/DC circuitry. Use isolated serial communication port between the PoE circuitry, and the switch's circuitry, as shown in the following figure.

**Figure 8-3.** Switch Circuitry with Single DC Source

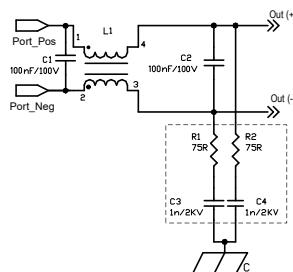


To maintain 1500  $V_{RMS}$  isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended to provide a safe margin for hi-pot requirements.

### 8.1.3 PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet the EMI requirements, high filtering and line terminations are needed when connecting the PoE circuit outputs to the switch circuitry, as shown in the following figure.

**Figure 8-4.** Recommended EMI Filter



**Note:** In most PoE systems, it is recommended to use 0Ω resistors for R1 and R2. However, certain systems may benefit from 75Ω resistors. Filtering provisions must be made. In quiet PoE systems, the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes the following:

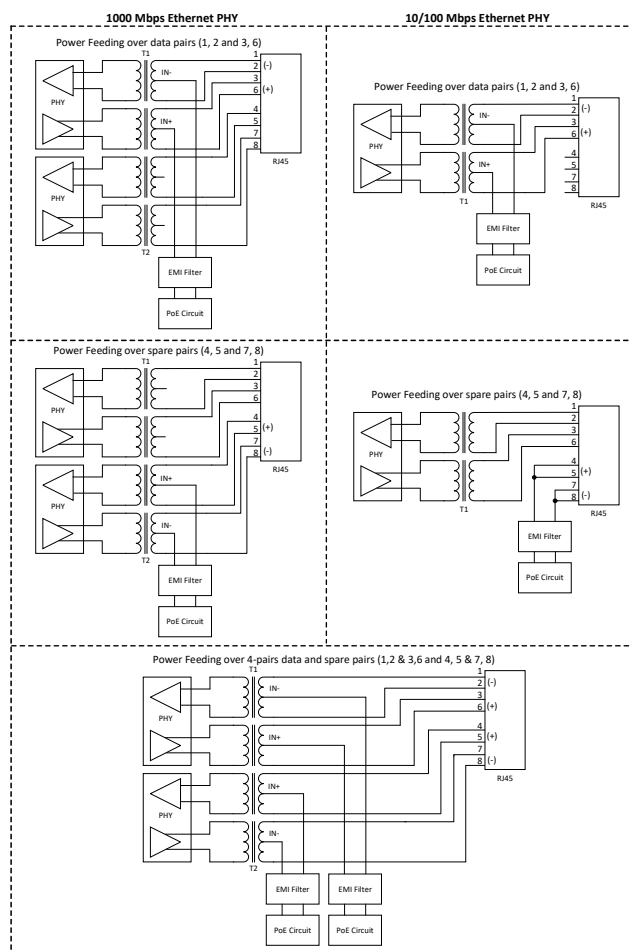
- A common mode choke for conducted EMI performances (such as, ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

As each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

**Note:** For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs, the spare pairs, or both the data and spare pairs. All methods are shown in the following figure where an MDI-X (or Auto MDI-X) connection is associated with the switch.

**Figure 8-5. Output Ports Design Details**



### 8.1.4 Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500  $V_{RMS}$  isolation between PoE voltages and frame ground (EGND). The RJ45 jack assemblies have a metal cover of 80 mils that almost reaches the PCB surface. Maintain an 80 mils traces clearance between EGND traces for the RJ45 modular jack assembly metal cover and adjacent circuit paths/components. To prevent 1500  $V_{RMS}$  isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ45 connector assemblies.

PoE technology involves voltages as high as 57  $V_{DC}$ . Therefore, plan adjacent traces for 100  $V_{DC}$  operational creepage. Operational creepage must be maintained to prevent breakdown between traces carrying these potentials.

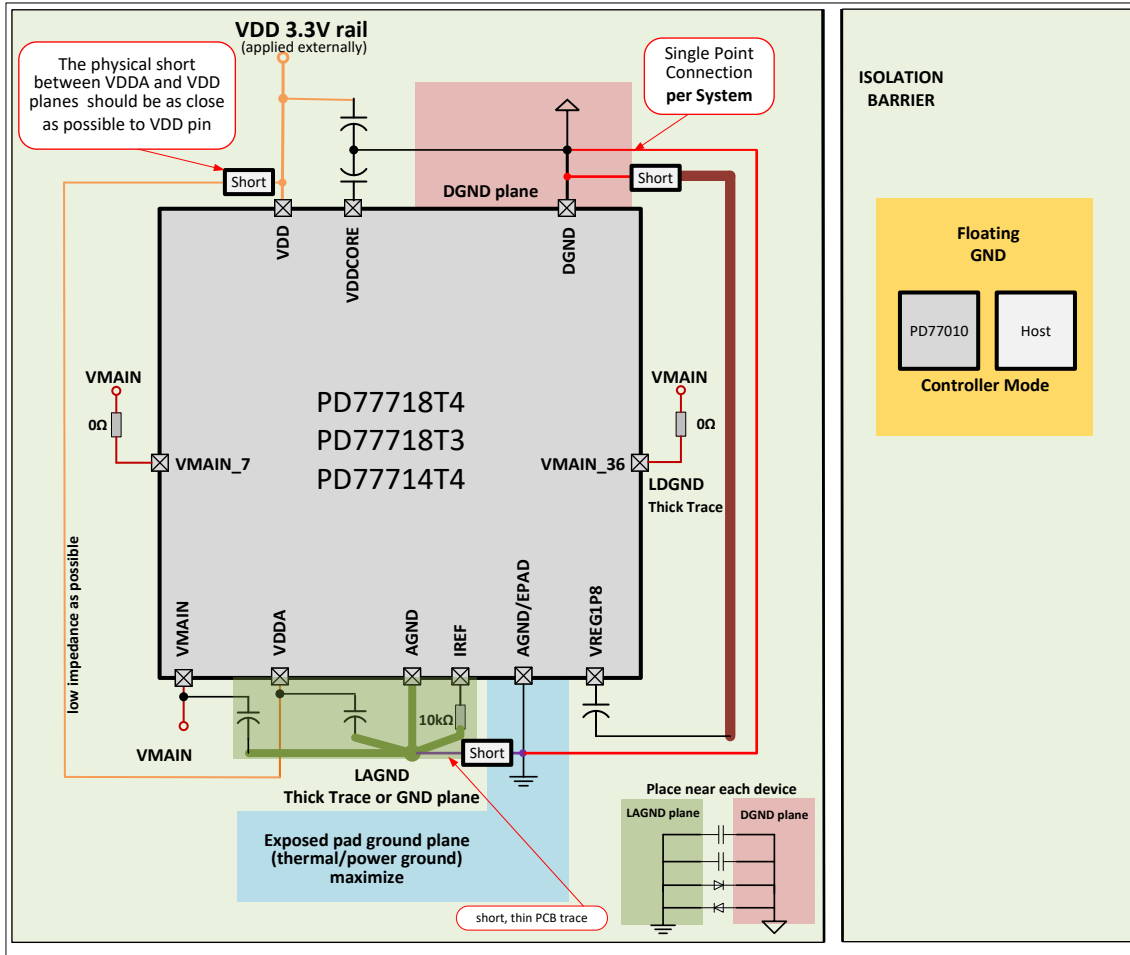
## 8.2 Guidelines

Microchip's PD77718T4, PD77718T3, or PD77714T4 PoE Manager is designed to simplify the integration of PoE circuitry into switches based on the IEEE PoE standards. The pinout arrangement has been configured for optimal PCB routing.

The following block diagram shows the various circuits and elements surrounding the PD77718T4, PD77718T3, or PD77714T4 PoE manager. This block diagram includes the following peripheral elements:

- **$V_{MAIN}$  7 and 36 pins:** Connect to  $V_{MAIN}$  (pin 17) through PCB trace or 0 $\Omega$  resistor for basic level protection. Leave unconnected for enhanced surge protection. See *AN4813: Surge Protection for Systems Based on PD777xx 8-Port PSE PoE Controller/Manager*.
- **$V_{DD}$ , pin43:** Connect VDD to main 3.3V power supply on the board. Connect VDD decoupling capacitors to DGND
- **$V_{DDCORE}$ , pin47:** Internal 1.2V regulator, connect 1.0  $\mu$ F low ESR capacitor to DGND
- **$V_{REG1P8}$ , pin20:** Internal 1.8V regulator, connect 1.0  $\mu$ F low ESR capacitor to LDGND
- **$V_{MAIN}$ , pin17:** Connect VMAIN to positive rail of input PoE. Connect 1  $\mu$ F (100V, X7R) capacitor to LAGND
- **$V_{DDA}$ , pin22:** Connect VDDA to VDD using a single point connection, preferably the PCB shorting point placed close to VDD trace. Connect VDDA decoupling capacitors to LAGND
- **AGND, pin21:** Connect to LAGND
- **IREF, pin14:** Connect IREF resistor to LAGND
- **EPAD:** Connect EPAD to AGND
- **DGND and LAGND capacitor:** Requires a 1 nF and 470 nF per IC between LAGND and DGND. Leave a population option for two back-to-back diodes to improve EMC/EMI immunity, if required.
- **Per port connection:** See [Front-End Components](#)
- **LAGND and AGND short:** LAGND and AGND need to have a single connection near the EPAD
- **LDGND and DGND short:** LDGND and DGND need to have a single connection

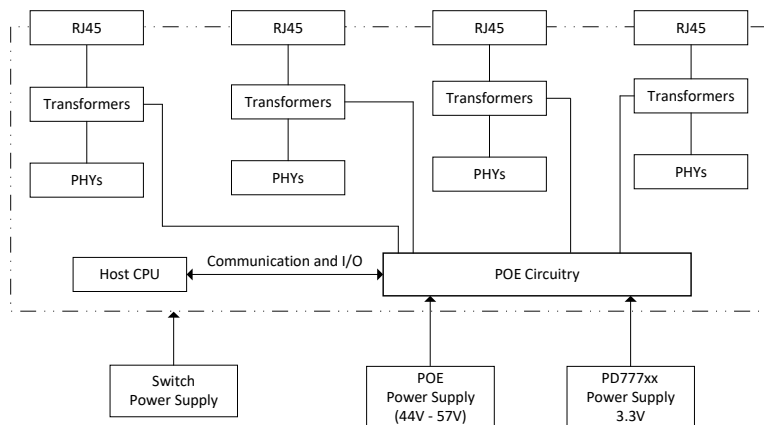
Figure 8-6. Component Identification for PD77718T4, PD77718T3, or PD77714T4 Circuitry



### 8.2.1 Locating PoE Circuitry in a Switch

To minimize the length of high current traces as well as RFI pick-up, place the PoE circuitry as close as possible to the line transformers of the switch. The circuit can be fully integrated into the switch's PCB or can be easily placed on top of the switch using a daughter board. Typical integration of PoE modules inside a switch is shown in the following figure.

Figure 8-7. PoE Circuitry Inside the Switch



## 8.2.2 Ground and Power Planes

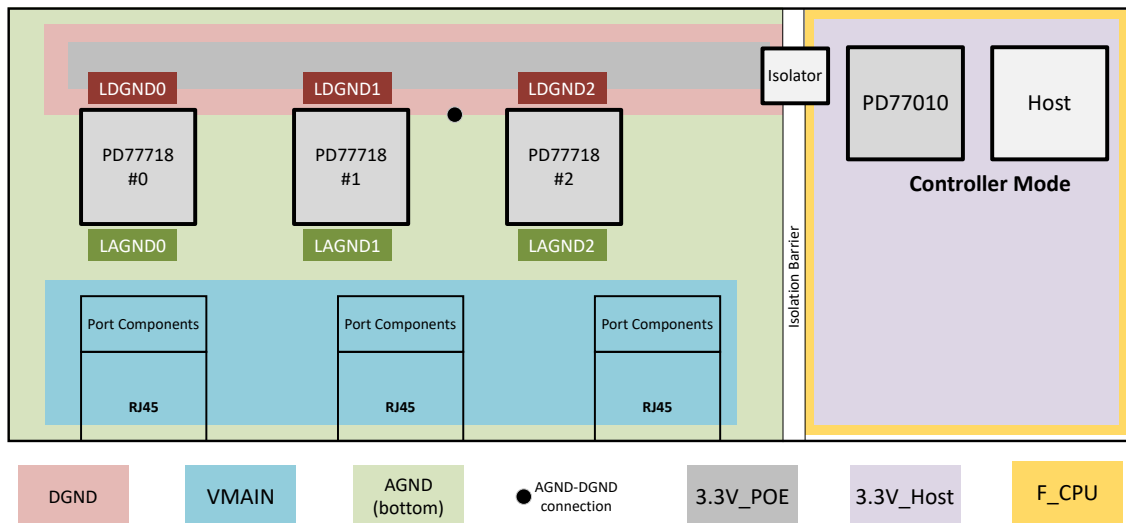
As the PoE solution is a mixed-signal (analog and digital) circuitry, care must be taken when routing the ground and power signal lines.

The reference design assumes a four-layer board such as, top, mid1, mid2, and bottom. The main planes are VMAIN/AGND and DGND.

Ground planes are crucial for proper operation and must be designed in accordance with the following guidelines:

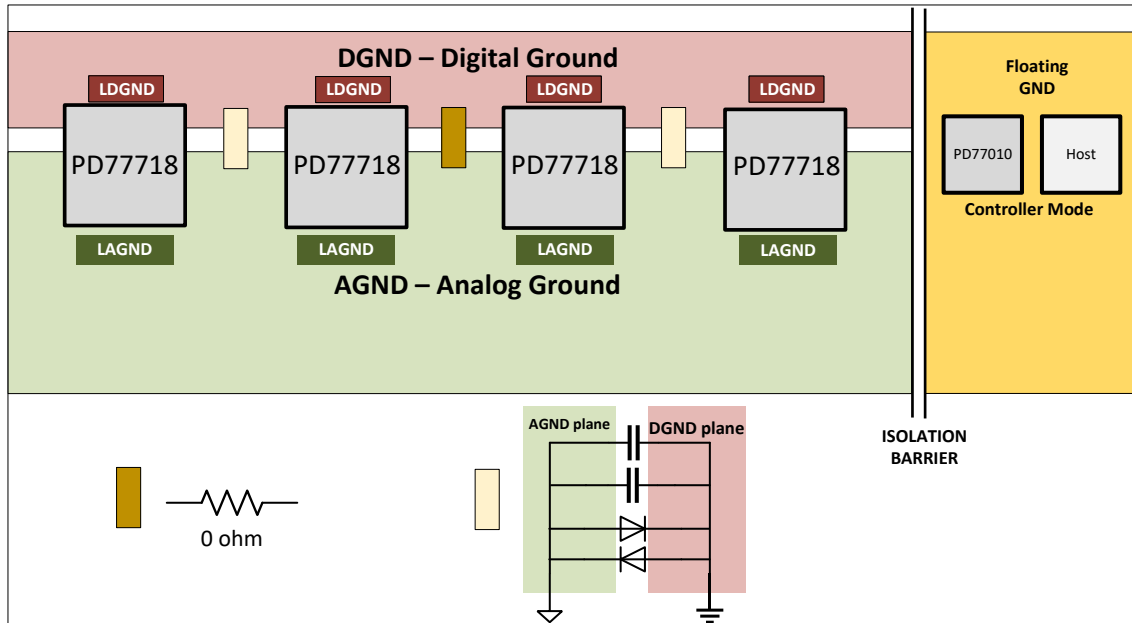
- Separate analog ground (AGND) and digital ground (DGND), with a gap of at least 40 mils
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD77718T4, PD77718T3, or PD77714T4. The AGND must be located on external layer.
- Separate local grounds (LAGND/LDGND) and system grounds (AGND/DGND), with a gap of at least 20 mils
- Connect LDGND to DGND using a single point connection, preferably the PCB shorting point placed close to DGND trace
- Connect all LAGND connections at single point using star connection. The LAGND is connected to EPAD using a short, thin PCB trace under IC for equipotential with AGND.
- Earth ground is used to tie in the metal frame of the RJ45 connectors. This ground must be routed separately and connected to the switch's metal chassis/enclosure.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds, as shown in the following figure.

Figure 8-8. Ground and Power Planes



- To connect various digital ground (DGND) points extend the DGND surface under pins 43–56 of the PD77718T4, PD77718T3, or PD77714T4 Managers.
- A focal interconnection point for the digital and analog grounds must be located at about the middle of the overlapping section, as shown in the following figure

Figure 8-9. Single-Point Connection Between DGND and AGND



- Leave spacing for a ceramic 1 nF bypass capacitor and two parallel and inverted Schottky diodes near each PoE manager between the analog and digital layers, as shown in the preceding figure. The capacitors form low impedance paths for digital driving signals.
- The power and return (ground) planes for the  $V_{MAIN}$  supply must be designed to carry the system maximum continuous current, based on the design capacity. Minimize DC power losses on these planes by using wide copper lands.

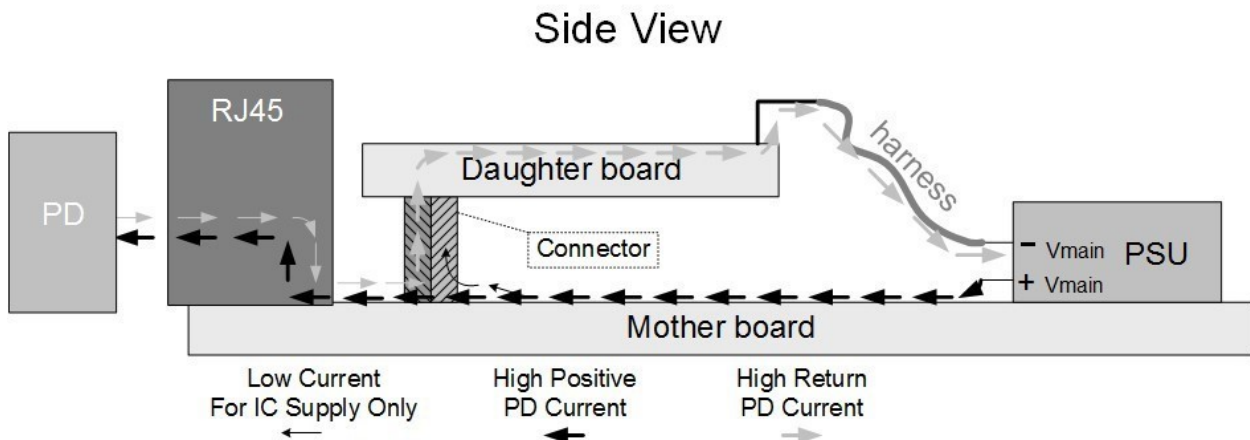
Use the following design guidelines while routing the Power planes:

- Separate  $V_{MAIN}$  and VDD signals, with a gap of at least 20 mils
- Separate PORT\_NEGx and VDD signals, with a gap of at least 20 mils

### 8.2.3 Current Flow Through the PoE Application Utilizing a Daughter Board

When implementing the PoE circuitry on a daughter board, the high current path to the load (PD) does not have to be routed through the daughter board but only the return path, as shown in the following figure.

Figure 8-10. Blocks Identification for PD77718T4, PD77718T3, or PD77714T4 Circuitry (Side View)



The port's DC current flows in an application utilizing a PoE DB as follows:

1. Coming from the switch's power supply positive to the center taps of the line transformer through a mother board wide trace (not through the DB)
2. From the center tap of the line transformer through the RJ45 of the switch to the PD side
3. The return current from the PD flows through RJ45 and the line transformer to the DB PoE circuitry
4. From the DB analog ground (AGND), the current flows back to the switch's power supply negative through harness

**Note:** The heavy current of the positive port flows directly to the PD side without going through the PoE managers on the DB.

## 8.2.4 Conductor Routing

The following sections describe the conductor routing guidelines.

### 8.2.4.1 General Guidelines

The conductor (or printed lands) routing is performed as practiced in the general layout guidelines, specifically listed as follows:

- Conductors that deliver a digital signal are routed between the analog and the digital ground planes
- Avoid routing analog signals above the digital ground

### 8.2.4.2 Port Outputs

For robust design, the port output traces are 45-mil wide to handle maximum current and port power. However, to obtain a 10 °C (maximum) copper rise under 1A per port, set the minimum width for traces in accordance with the layer location and copper thickness, listed as follows:

- For two-ounce copper, external layer: 15 mils
- For two-ounce copper, internal layer: 20 mils
- For one-ounce copper, external layer: 25 mils
- For one-ounce copper, internal layer: 40 mils
- For ½ ounce copper, external layer: 30 mils
- For ½ ounce copper, internal layer: 55 mils (20 °C copper rise)

Additionally, the following port output guidelines must be considered:

- The port output traces must be short and parallel to each other to reduce RFI pickup and keep the series resistance low
- The PoE port outputs must be connected to the switch's pulse transformers as shown in [Figure 8-5](#). The common mode choke and Bob Smith termination (resistor-capacitor) to chassis ground are optional and used to reduce RFI noise. The circuit is located as close as possible to the pulse transformer.
- Route the I<sup>2</sup>C communication clock (SCK) line coming from the PoE controller carefully so that it does not disturb the other lines. Two ground lines (connected to DGND) can be routed alongside the clock line to isolate it from the rest of the lines.

## 8.3 Specific Component Placement

The following section provides placement details for specific components.

### 8.3.1 Peripheral Components

To minimize heat transfer among various components, a gap between them must be maintained. The system designer must monitor the thermal performance during the designing phase and ensure that the maximum temperatures of the various components meet all requirements specified in the data sheet.

### 8.3.2 PD77010 Controller and Peripherals

For PD77010, see the Microchip *SAM D21 Family Datasheet* for recommendations related to the PoE controller layout guidelines. Locate the filtering capacitors for  $V_{DD}$  and for  $V_{DDA}$  close to the power and ground pins.

### 8.3.3 PD77718T4, PD77718T3, or PD77714T4 PoE Manager and Peripherals

The side of the PoE manager that includes pins 43–56 must face the DGND plane. These pins function as communication and control pins for the manager; connect between the PoE manager and the PD77010 PoE controller through isolation circuitry.

Locate the bypass capacitors for the PoE manager supply input close to the relevant pin. If two bypass capacitors are placed on the same line, then locate the lower valued capacitor closer to the pin on the same layer, and place the higher valued capacitor at a more distant location.

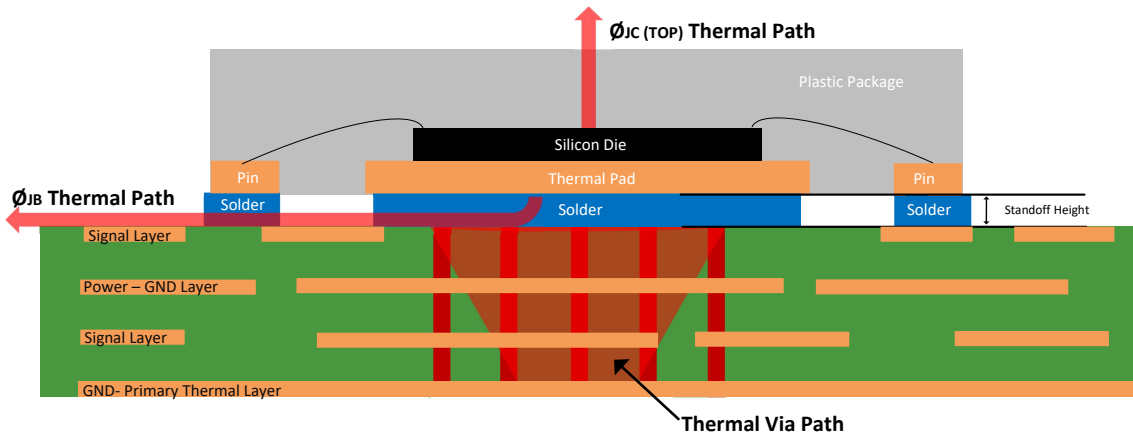
### 8.3.4 $V_{MAIN}$ Capacitors

It is a good design practice to have 47  $\mu\text{F}$  capacitors near each RJ45 gang over  $V_{MAIN}$ , to prevent noise and spikes events to penetrate the  $V_{MAIN}$  rail.

## 9. Thermal Pad Design

For proper heat dissipation, the recommended footprint/layout guidelines must be followed.

Figure 9-1. Heat Dissipation in PCB



Three thermal paths are available for heat to flow from the IC:

- Heat flow from the junction to the package side and pins. This parameter is a package parameter and is defined by  $\varnothing_{JB}$  in the device datasheet.
- Heat flow from the junction to the package top surface. This parameter is a package parameter and is defined by  $\varnothing_{JC}$  (TOP) in the device datasheet.
- Heat flow from the junction to the package bottom surface (the thermal pad) through the thermal vias to the various thermal ground planes. This is the most significant thermal path. The thermal resistance of this path is determined by the package e-pad design and the PCB construction: Number of PCB layers, number of thermal vias, construction of thermal vias, and size and location of the copper thermal plane. This is the primary heat flow path and it is important to follow footprint recommendations.

The footprint that details the solder mask, copper layers, and recommended paste mask is detailed in the PD77718T4, PD77718T3, or PD77714T4 datasheet.

- As per IPC7093 standard, standoff must be minimum of 2 mil (0.050 mm), with a Microchip recommended target of 2.5 mil (0.0635 mm). For this reason, a paste mask stencil thickness of 5 mils must be considered.
- Thermal vias must be unplugged with a diameter approximately 0.33 mm. Microchip recommends a 6 × 6 via array and no solder paste covering on the bottom PCB layer.
- Thermal pad solder paste is a 3 × 3 array with “streets” in-between the array

**➔ Important:** It is important to have streets to allow for outgassing during the reflow process to help achieve a uniform standoff height.

The PCB copper thermal planes must be of maximum practical area on as many PCB layers as possible. See the device datasheet for package footprint guidelines.

## 10. References

The following documents can be obtained from Microchip Power over Ethernet.

- *PD77718T4, PD77718T3, and PD77714T4 8-Port and 4-Port PoE PSE Manager data sheet*
- *PD77010 PoE PSE Controller*

Consult Microchip for *Surge Protection 8-Port PSE Manager PD777xx*.

The following are available on [Microchip's Software Library](#).

- *Firmware (without the boot section) and GUI*
- *PD77010 Communication Protocol User Guide*

In addition, the following non-Microchip documents can be consulted.

- *IEEE Std 802.3-2018 Clause 33 Power over Ethernet over 2-Pair and Clause 145 Power over Ethernet*
- *IEEE802.3af-2003 Standard, DTE Power via MDI*
- *IEEE802.3at-2009 Standard, DTE Power via MDI*

Technical support for Microchip PoE products is available at the [Microchip Technical Support Portal](#).

## 11. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

**Table 11-1.** Revision History

Revision	Date	Description
B	03/2025	Updated <a href="#">Communication Interfaces</a>
A	03/2025	Initial Revision

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