8-Port and 4-Port PoE PSE Manager

PD77718T4, PD77718T3, and PD77714T4

Introduction

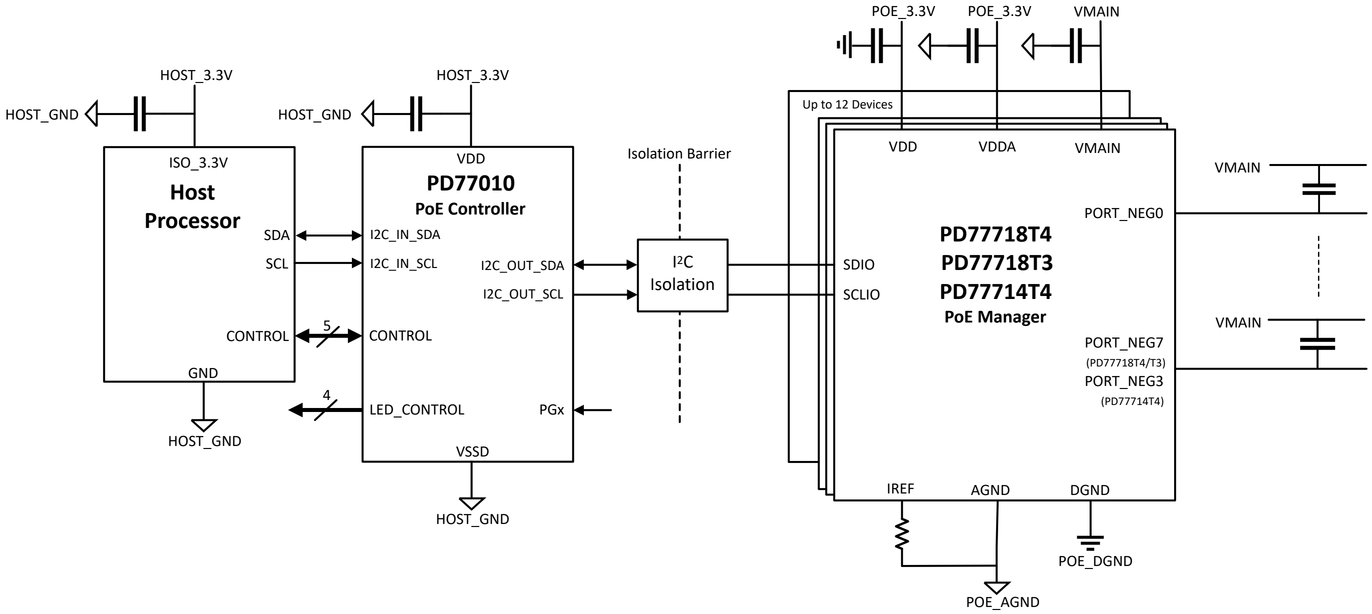
The PD77718T4, PD77718T3, and PD77714T4 devices are part of Microchip's seventh generation IEEE®802.3bt compliant Power over Ethernet (PoE) Power Sourcing Equipment (PSE) family. These devices are fully integrated PoE managers with integrated Field Effect Transistor (FET) switches and current sense resistors. Up to 12 devices can be cascaded to provide 48 4-pair ports. The device is available in a 56-pin 8 mm × 8 mm QFN package.

The devices are IEEE802.3bt compliant

- PD77718T4 8-port Type 4 (90W)
- PD77718T3 8-port Type 3 (60W)
- PD77714T4 4-port Type 4 (90W)

The following figure shows the typical PoE application of the PD77718T4, PD77718T3, and PD77714T4 devices.

Figure 1. Typical PoE Application



Features

The PD77718T4, PD77718T3, and PD77714T4 devices and PSE based systems have the following key features:

- IEEE802.3bt Compliant
  - PD77718T4/PD77714T4 - Type 4
  - PD77718T3 - Type 3
- Supported PD Types
  - Type 1, Type 2 PDs (802.3af, 802.3at)
  - Single-Signature PDs
    - PD77718T4/PD77714T4 Type 3 and 4
    - PD77718T3 Type 3
  - Dual-Signature PDs
    - PD77718T4/PD77714T4 Type 3 and 4
    - PD77718T3 Type 3
  - Legacy PDs powered as 4P
  - Supports non-compliant and legacy PDs
- Operational Modes
  - Controller mode in conjunction with PD77010 PSE Controller
- Cascade up to 12 devices
  - Systems based on PD77718T4/PD77718T3 support 96 × 2-pair ports or 48 × 4-pair ports in any 4-pair/2-pair combination
  - Systems based on PD77714T4 support 48 × 2-pair ports or 24 × 4-pair ports in any 4-pair/2-pair combination
- Any combination of PD77718T4, PD77718T3 or PD77714T4 may be used in a system
- Device Features
  - Per-port integrated FET, sense resistor, and port diode
  - Total port resistance of 160 mΩ
  - Device power dissipation ≤ 2W at full load
  - Two power rails (55V and 3.3V) for maximum power efficiency
  - Guaranteed 4-pair output power
    - 90W PD77718T4/PD77714T4
    - 60W PD77718T3
  - Over Supply Signal (OSS) support
  - AutoClass support
  - Supports Fast and Perpetual PoE
  - PD77010 interface through I^2C Communication

- Real-Time Protection (RTP)
- Measurements
  - Per-port voltage and current measurement
  - Accurate main power measurement
  - Voltage measurement and total device dynamic power consumption calculations
  - Per-port power calculations
- PD77718 field up-gradable firmware through PD77010.
- Surge
  - Surge up to 2 kV without additional components per IEC61000-4-5-2014
  - Surge compliance, ITU-T K.21, GR1089, IE61000-4-5-2014, EN55024
    - Up to 10 kV per IEC61000-4-5-2014
    - Up to 6 kV per ITU-T K.21
- Physical Characteristics
  - Ambient temperature range –40 °C to 85 °C
  - 56-pin 8 mm × 8 mm QFN package with thermal pad
  - MSL3, RoHS compliant

Applications

The PD77718T4, PD77718T3, or PD77714T4 based PSE has the following typical applications:

- Campus switches
- Switches and routers for enterprise, small and medium businesses, Small Office/Home Office (SOHO), and commercial markets
- Switches for lighting markets
- PoE injectors

Table of Contents

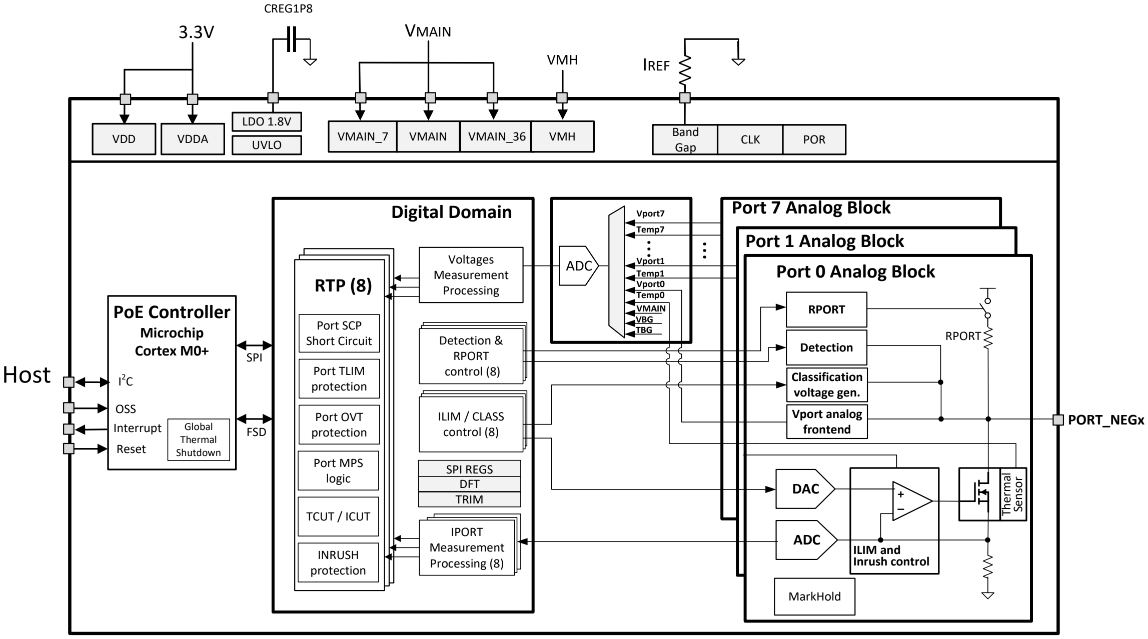
1. Functional Descriptions

This section describes the following four main blocks of the PD77718T4, PD77718T3, and PD77714T4 devices:

- Analog front-end block (x8 for PD77718T3/T4 or x4 for PD77714T4)
- Voltage and temperature measurement module
- Digital processing and control block
- PoE controller (based on the Cortex®-M0+ device)

The following figure shows a high-level block diagram of the PD77718T4 or PD77718T3 devices.

Figure 1-1. PD77718T4/PD77718T3 Block Diagram



1.1 Analog Front-End Block

The analog front-end block of each port contains the following components:

- Current-limiting block—fast-acting, current-limiting loop
- Classification voltage regulation
- V_{PORT} measurement analog interface
- Detection module
- Current measurement module

This structure allows efficient and flexible port control. It also supports simultaneous power-up/power-on 8-ports control.

1.2 Voltage and Temperature Measurement Module

The module measures port voltages, V_{MAIN} voltage, and temperature.

1.3 Digital Processing and Control Block

The digital block communicates with the integrated PoE controller and controls the analog front-end block. It consists of the following blocks:

- Ports on/off control block
- I_{LIM} and I_{CLASS} control blocks
- I_{INRUSH} control and protection block
- Detection and R_{PORT} control block
- Port voltage and temperature measurement post-processing module
- Port current post-processing module
- RTP module

1.4 Integrated PoE Controller

The PD77718/14 has an integrated device level PoE Controller. The integrated PoE controller controls both port-level and device-level PoE tasks. The firmware is pre-programmed into the integrated controller with field-upgradable capability through the I^2C PD77010 interface.

The integrated PoE controller provides the following features:

- PD77010 communication interface (Fast-Mode Plus I^2C interface, INT_OUT signal)
- OSS fast shut-down control
- Device-level data processing
- Supports PoE firmware download capability from the PD77010
- Local management of device 2p and 4p port configuration

1.5 Power

The PD77718T4, PD77718T3, and PD77714T4 devices are designed for low-power consumption and low-power dissipation, using the cutting-edge process technology and the port's proprietary MOSFET design.

The following two parameters allow for a total power dissipation up to 2W at T_J = 125 °C:

- Very low channel (port) resistance (typically, 160 mΩ at 25 °C)
- Very low V_{MAIN} quiescent current

The PD77718T4, PD77718T3, and PD77714T4 devices support any power rail sequencing of the V_{MAIN} and V_{DD} rails.

1.6 Real-Time Protection (RTP)

This section describes the RTP blocks included in the PD77718T4, PD77718T3, or PD77714T4 devices. These devices contain multi-level and real-time support mechanisms. All RTP mechanisms are configured by the PoE controller, implemented in the digital domain, and directly controls the port analog front-end. Each port has its own RTP protection blocks. This type of design ensures fast-acting protection under all conditions.

1.6.1 Current Overload (T_{LIM}/I_{LIM}) Protection

The configurable I_{LIM} and T_{LIM} parameters are based on the IEEE 802.3bt standard. T_{LIM} and I_{LIM} threshold levels are selected by firmware based on the assigned class. The port shuts down if it enters the current limit (I_{LIM}) and maintains the I_{LIM} for a period of T_{LIM}. Current overload RTP also protects against repetitive overload conditions, where the port repetitively enters the current limit for a duration less than T_{LIM}, which might result in device damage due to accumulated overheating. The overload protection mechanism disconnects the port if the accumulated power poses a danger to the Safe Operating Area (SOA) of the MOSFET.

1.6.2 Short-Circuit Protection

If the port enters the current limit and the port voltage (V_{PORT}) drops below a configurable value, the port is considered to be in a short-circuit condition. In this case, the port is turned off within 100 µs (typical) to minimize the power dissipation on the MOSFET during such a harsh condition. The voltage below which the port is considered to be in a short-circuit condition is also configurable.

1.6.3 Inrush (Power-Up) Protection

During the port inrush phase, the PD capacitor is charged with a constant current for up to 65 ms. If the PD is not limiting the current, the PSE uses its current limit to limit the capacitor inrush current (for most cases, I_{LIM} is 0.425A). Inrush current is also configurable. A failed PD capacitor, or too large a capacitor value, might result in either a true short-circuit condition on the port during inrush (leads to very high-power dissipation, equal to 0.425A × V_{MAIN}), or a very high-power dissipation due to the slow increase in the capacitor voltage. A dedicated inrush protection mechanism is provided to protect the device from such events, assuring that the port's MOSFET does not exceed its SOA under any condition.

1.6.4 Over-Temperature (OVT) Protection

OVT protection adds a layer of protection to the device, and protects the device from overheating and damaging in parallel to the other protection mechanisms. An example of OVT protection is a slow increase in ambient temperature (for example, a failed fan), resulting in an elevated junction temperature which exceeds the maximum operating junction temperature. In this case, OVT real-time protection either limits the number of ports that can be turned ON at such temperature, or turns off the port (s) that exceeds the highest junction temperature.

1.6.5 T_{CUT}/I_{CUT} Protection

The firmware selects T_{CUT} and I_{CUT} threshold levels based on the assigned class. The port is turned off if the port current exceeds I_{CUT} for a cumulative time of T_{CUT} (typical 65 ms). Both T_{CUT} and I_{CUT} values are configurable.

1.6.6 Maintain Power Signature

The Maintain Power Signature (MPS) is required to keep a PD powered and to disconnect its power if PD is removed. MPS protection, as defined in the IEEE 802.3bt standard, is incorporated, in which the port is turned off if the PD current does not comply with the required hold current and time. Both the hold current (I_{HOLD}/$I_{HOLD-2P}$) and the duration (T_{MPS}, T_{MPDO}) are configurable parameters.

1.7 Over Supply Shutdown (OSS)

OSS is a control pin required to turn off ports of a certain priority due to live removal or failure in one of the power supplies and when dynamic over power is above the active budget by more than 5%.

When used with the PD77010 device, the PD77010 device controls this pin to implement the correct code to be sent to the PD77718 device when either of the four power good pins is activated.

1.8 Power Good

The power budget and reallocation of the power based on priority (if there is a loss of a power supply) is defined through the Power Good pins. These pins associated with this function are on the PD77010. It is mentioned in this document for completeness.

1.9 V_{MAIN} Under-Voltage Lockout (V_{MAIN_UVLO})

V_{MAIN} under-voltage lockout (V_{MAIN_UVLO}) turns off ports when V_{MAIN} drops below a set threshold.

1.10 Surge

The PD77718T4/PD77718T3 and PD77714T4 devices support up to 2 kV per IEC-61000-4-5-2014 without external protection components.

For a higher level of surge, request the *AN4813 Surge Protection for Systems Based on PD777xx PSE PoE Controller/Manager* Application note.

1.11 PSE System Modes of Operation

The device supports the following PSE system modes of operation:

- Controller mode (with PD77010 PSE Controller)

For more details, see Application Information.

2. PD77010 PSE Controller

The PD77010 PSE Controller is used in conjunction with the PD77718T4, PD77718T3, or PD77714T4 PoE Manager. The PD77010 provides multi-port PoE functions, such as port mapping (Port Matrix), port priority, port status, system power management, fast dynamic over power disconnect and fast power good change disconnect. The PD77010 is based on Microchip SAM D21, and is packaged in a 5 mm × 5 mm 32-pin QFN package.

For more details, see the *PD77010 Data Sheet and Communications Protocol* documents.

3. Electrical Specifications

This section describes the electrical specifications of the device.

3.1 Absolute Maximum Ratings

PoE performance is not guaranteed when it exceeds the recommended rating. Exposure to any stress in the range between the recommended rating and the absolute maximum rating must be limited to a short time. Exceeding these ratings might impact the long-term operating reliability. The following table lists the absolute maximum ratings.

Table 3-1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD}	–0.3	3.8	V
V_{DDA}	–0.3	3.8	V
V_{DDA} to V_{DD}	–0.3	0.3	V
V_{MAIN}	–0.3	80	V
V_{MAIN_7}, V_{MAIN_36}	V_{MAIN}	80	V
PORT_NEGx to AGND	–0.3	Lower of V_{MAIN_x} + 0.5 or 80	V
DGND to AGND	–0.3	0.3	V
Digital I/O	–0.3	3.6	V
AUTO	–0.3	Lower of V_{DDA} + 0.3 or 3.8	V
Junction Temperature	–40	Self Protected	°C
Storage	–55	150	°C
Solder 10 Seconds	—	260	°C

3.2 Immunity

The following tables list the device immunity.

Table 3-2. ESD

Model	Pins	Minimum Rating	Test Method
Human Body Model (HBM)	All	±2000V	JS-001-2017
Charge Device Model (CDM)	All	±1000V	JESD22-C101F

Table 3-3. Surge Protection

Standard	Application	Minimum Rating
IEC61000-4-5 Ed3	Common mode	1 kV, 2 kV, 4 kV, 6 kV, and 10 kV
ITU-T K.21 2019	Common mode	2.5 kV, 4 kV, and 6 kV
	Differential mode	2.5 kV and 6 kV
EN55024 2010	Common mode	1 kV and 4 kV
GR1089 Issue 6	Common mode	1 kV and 2.5 kV
	Differential mode	1 kV

Note: The device meets 2 kV per IEC-61000-4-5 without the need for additional surge protection components. Consult Microchip for recommended protection circuitry for enhanced surge capability.

3.3 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 3-4. Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Junction temperature	—	–40	—	125	°C
Ambient temperature	—	–40	—	85	°C
V_{MAIN}	Type 1: Reference to AGND	44	—	57	V
	Type 2, 3: Reference to AGND	50	—	57	V
	Type 4: Reference to AGND	52	—	57	V
V_{MAIN_7}/V_{MAIN_36}	Reference to AGND	—	V_{MAIN}	—	V
V_{MAIN} slew rate	V_{MAIN} = 0V to 57V V_{DD} may be either present or absent	—	—	1.0	V/µs
V_{DD}	Reference to DGND	3.0	3.3	3.6	V
V_{DDA}	Reference to AGND	3.0	3.3	3.6	V
DGND–AGND voltage difference	—	–0.3	—	0.3	V

3.4 Electrical Characteristics

If not specified under conditions, the minimum and maximum ratings listed in the following table apply to the entire specified operating ratings of the device. Typical values stated are either by design or by production testing at 25 °C ambient.

The following tables list the electrical characteristics of the device.

Table 3-5. Current and Power Consumption

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
V_{MAIN} current	I_{MAIN}	Power on Reset (POR) threshold exceeded, $V_{MAIN} > 12V$	—	—	1.5	mA
		$0V < V_{MAIN} \leq 8V$, V_{DD}, V_{DDA} not present V_{MAIN}< POR threshold IC is non-operational	—	—	100	µA
V_{DD} rail + V_{DDA} rail current	$I_{VDD} + I_{VDDA}$	V_{MAIN} = 55V, $V_{DD} = V_{DDA}$ = 3.6V	—	—	30	mA

Table 3-6. Port Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Port-supported continuous current	I_{PORT_CONT}	• Single-Signature PD • V_{MAIN} = 52V, port not in current limit • Class 8 with P_{CLASS_PD} = 99.7W • Maximum unbalance	1.185	—	—	A
Power dissipation PD77718T4	P_{DISS}	All ports 4P Class 8 power (90W) V_{MAIN} = 52V $V_{DD} = V_{DDA}$ = 3.3V	—	—	2.0	W
Power dissipation PD77718T3	P_{DISS}	All ports 4P Class 6 power (60W) V_{MAIN} = 50V $V_{DD} = V_{DDA}$ = 3.3V	—	—	0.900	W
Total channel resistance	R_{CH_ON}	T_A = 25 °C	—	0.160	—	Ω
Port resistance	R_{CH_OFF}	R_{PORT} connected, T_J = 25 °C V_{PORT} < 30V	50	60	70	kΩ
		R_{PORT} disconnected, T_J = 25 °C	—	1.8	—	MΩ

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
V_{PORT} leakage	$I_{LEAKAGE}$	V_{PORT_NEGx} to AGND	—	—	5	µA
Port capacitance	C_{PSE}	**Required:** External X7R port capacitance (typical capacitor values)	47	100	220	nF
	C_{PD}	Supported PD capacitance for IEEE® 802.3bt compliant detection	50	—	150	nF
		Supported PD capacitance, non-compliant PD detection	0.05	—	12.8	µF
		Supported PD capacitance, inrush phase, IEEE® 802.3bt compliant	5	—	180	µF
		Supported PD capacitance, inrush phase, not IEEE® 802.3bt compliant	—	—	432	µF
Supported output power PD77718T4/ PD77714T4	P_{PORT4P}	2 ports power, connected to a single-signature PD, V_{MAIN} = 52V	—	—	100	W
Supported output power PD77718T3	P_{PORT4P}	2 ports power, connected to a single-signature PD, V_{MAIN} = 52V	—	—	68	W

Table 3-7. Current Limit (I_{LIM})

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Port current limit	I_{LIM}	Class 0–Class 3, 2-pair single signature	—	0.720	—	A
		Class 4, 2-pair single signature	—	0.850	—	A
		Class 4, 4-pair dual signature	—	0.850	—	A
		Class 5, 4-pair single signature	—	0.850	—	A
		Class 6, 4-pair single signature	—	0.890	—	A
		Class 7, 4-pair single signature (PD77718T4/PD77714T4 only)	—	1.000	—	A
		Class 8, 4-pair single signature Class 5, 4-pair dual signature (PD77718T4/PD77714T4 only)	—	1.200	—	A
Inrush current limit	I_{INRUSH}	I_{LIM} setting I_{LIM_2P}	0.400	0.425	0.450	A

Table 3-8. Power Accuracy

Parameter	Conditions	Min.	Typ.	Max.
Single port (2 pairs) power accuracy	Port power: 5W to 15W	−5.0%	—	5.0%
	Port power: 15W to 55W	−2.5%	—	2.5%
2 ports (4 pairs) power accuracy	Total 4-pair power: 5W to 30W	−5.0%	—	5.0%
	Total 4-pair power: 30W to 100W PD77718T4/PD77714T4 Total 4-pair power: 30W to 60W PD77718T3	−2.5%	—	2.5%

Table 3-9. Detection and Connection Check

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Accept signature resistance	R_{DET}	—	19	25	26.5	kΩ
Accept signature capacitance	C_{DET}	—	—	—	0.15	µF
Reject signature resistance (low)	R_{REJ}	—	—	—	15	kΩ
Reject signature resistance (high)	R_{REJ}	—	33	—	—	kΩ
Reject signature capacitance	C_{REJ}	—	10	—	—	µF
Detection open circuit resistance	R_{OC}	—	0.5	—	—	MΩ
Valid detection test voltage	V_{VALID}	—	2.8	—	10	V
Detection open circuit voltage	V_{OC}	—	—	—	30	V
Total detection timing	T_{DET}	—	—	—	400	ms

Table 3-10. Classification

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Measured I_{CLASS} at PSE	I_{CLASS}	Class Signature 0	0	—	5	mA
		Class Signature 1	8	—	13	mA
		Class Signature 2	16	—	21	mA
		Class Signature 3	25	—	31	mA
		Class Signature 4	35	—	45	mA
Invalid Class Signature	I_{CLASS_LIM}	—	51	—	—	mA

Table 3-11. Real-Time Protection

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Short Circuit Protection (SCP) disconnection time	T_{SCP}	Port in current limit, $V_{PORT} < 40V$, no bouncing	—	100	—	µs
Overload protection (T_{LIM})	T_{LIM_2P}	Port in current limit, $V_{PORT} \geq 40V$ Class 1 to Class 6	—	11	—	ms
		Port in current limit, $V_{PORT} \geq 40V$ Class 7 and Class 8 PD77718T4/PD77714T4 only	—	7	—	ms
Port MPS current threshold	I_{MPS}	SSPD, Class 1–4, 4P operation	2.0	3.5	5.0	mA
		SSPD, Class 1–4, 2P operation	5.0	7.0	9.0	mA
		SSPD, Class 5–8, 4P operation Class 7, 8 4P operation PD77718T4/ PD77714T4 only	2.0	4.5	7.0	mA
		DSPD	2.0	4.5	7.0	mA
MPS on-time detection	T_{MPS}	—	—	—	6	ms
MPS off time	T_{MPDO}	—	340	356	372	ms
Port OVT protection	Reference temperature	Temperature above which the OVT protection is active	—	—	150	°C

Table 3-12. I_{CUT} and T_{CUT} Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
I_{CUT} threshold	I_{CUT_2P}	44V < V_{MAIN} < 57V Class 0–3	—	0.375	—	A
		50V < V_{MAIN} < 57V Class 4 SSPD 2P operation	—	0.644	—	A
		50V < V_{MAIN} < 57V Class 5 SSPD 4P operation	—	0.700	—	A
		52V < V_{MAIN} < 57V Class 6 SSPD 4P operation	—	0.800	—	A
		52V < V_{MAIN} < 57V Class 7 SSPD 4P operation (PD77718T4/PD77714T4 only)	—	0.900	—	A
		52V < V_{MAIN} < 57V Class 8 SSPD 4P operation Class 5 DSPD 4P operation (PD77718T4/PD77714T4 only)	—	1.090	—	A
T_{CUT} disconnect time	T_{CUT_2P}	—	—	65	—	ms
P_{CUT} disconnect time	P_{CUT_2P}	$I_{PORT} \geq P_{CUT}/V_{MAIN}$	—	132	—	ms

Table 3-13. Inrush (Power-Up) Phase

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Inrush time	T_{INRUSH}	Per port V_{MAIN} = 57V I_{INRUSH_2P} = 0.425A	—	65	—	ms
Number ports for simultaneous power-up	N_{PORT}	Power-up to maximum capacitor of 360 µF + 20%	—	—	8	Ports

Table 3-14. UVLO

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VMAIN_UVLO Threshold voltage	$V_{MAIN\_UVLO\_F}$	Threshold level below which ports are turned OFF. V_{MAIN} falling.	29.5	30	30.5	V
	$V_{MAIN\_UVLO\_R}$	Threshold level above which ports are operational. V_{MAIN} rising.	39.4	40	40.6	V
VMAIN_UVLO ports off response time	$t_{VMAIN\_UVLO\_F}$	Time between V_{MAIN} falling below VMAIN_UVLO_F and ports turned off. V_{MAIN} falling.	8	—	24	ms

Table 3-15. External Current Reference Resistor I_{REF}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
I_{REF} resistor value	I_{REF}	External 0402 reference resistor value	—	10	—	kΩ
	$I_{REF\%}$	External 0402 reference resistor accuracy	–0.1	—	0.1	%
	I_{REF_TEMPCO}	Resistor temperature coefficient	—	25	50	ppm/°C

Table 3-16. I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{PULL}	Internal Pull-up/Pull-down resistance	—	20	40	60	kΩ
V_{IL}	Input low-level voltage	V_{DD} = 3.0V–3.6V	—	—	0.3 × V_{DD}	V
V_{IH}	Input high-level voltage	V_{DD} = 3.0V–3.6V	0.55 × V_{DD}	—	—	
V_{OL}	Output low-level voltage	V_{DD} > 3.0V, I_{OL} at max	—	0.1 × V_{DD}	0.2 × V_{DD}	
V_{OH}	Output high-level voltage	V_{DD} > 3.0V, I_{OH} at max	0.8 × V_{DD}	0.9 × V_{DD}	—	
I_{OL}	Output low-level current	V_{DD} = 3V–3.63V	—	—	10	mA
I_{OH}	Output high-level current	V_{DD} = 3V–3.63V	—	—	7	mA
t_{RISE}	Rise time[1]	load = 20 pF, V_{DD} = 3.3V	—	—	15	ns
t_{FALL}	Fall time[1]	load = 20 pF, V_{DD} = 3.3V	—	—	15	ns
I_{LEAK}	Input leakage current	Pull-up resistors disabled	−1	±0.015	1	μA

Note:

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

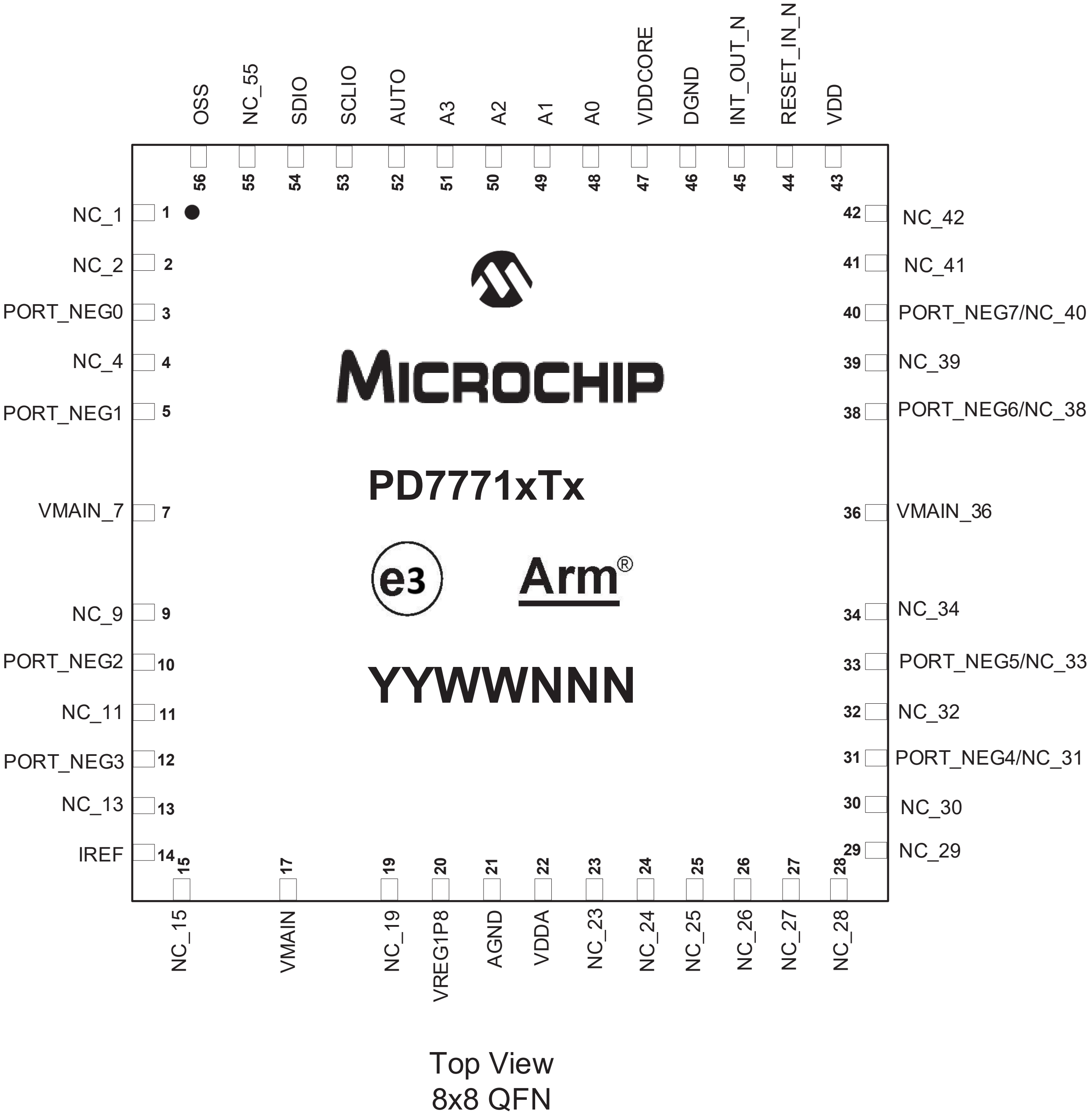
Table 3-17. I^2C Pins Characteristics in I^2C Configuration

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input low-level voltage	V_{DD} = 3.0V–3.6V	—	—	0.3 × V_{DD}	V
V_{IH}	Input high-level voltage	V_{DD} = 3.0V–3.6V	0.55 × V_{DD}	—	—	
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.08 × V_{DD}	—	—	
V_{OL}	Output low-level voltage	V_{DD} > 3.0V, I_{OL} = 3 mA	—	—	0.4	
I_{OL}	Output low-level current	V_{OL} = 0.4V Fast Plus Mode	20	—	—	mA
f_{SCL}	SCL clock frequency		—	600	1000	KHz

4. Pin Descriptions

The following figure shows the device pinout.

Figure 4-1. Pinout



The following table lists the pin descriptions of the PD77718T4, PD77718T3, or PD77714T4 devices.

Table 4-1. Pin Descriptions

Pin	Designator	Type	Description
1, 2, 4, 9, 11, 13, 15, 19, 23, 24, 25, 26, 27, 28, 29, 30, 32, 34, 39, 41, 42, 55	Not Connected (NC)	N/A	NC. Leave floating.
3	VPORT_NEG0	Power	Negative port 0 output
5	VPORT_NEG1	Power	Negative port 1 output
6, 8, 16, 18, 35, 37	N/A	N/A	Pin removed
7	VMAIN_7	Power	Connect to V_{MAIN} through PCB trace or 0Ω resistor for basic level protection. Leave unconnected for enhanced surge protection. See *PD777xx Surge Protection Application Note* for more details.
10	VPORT_NEG2	Power	Negative port 2 output
12	VPORT_NEG3	Power	Negative port 3 output
14	IREF	Analog Input	Current reference resistor. Connect through 10K 0.1% to AGND.
17	VMAIN	Power	Connect to V_{MAIN}. Connect a 1 µF, 100V, X7R capacitor near the V_{MAIN} pin of each device.
20	VREG1P8	Power	Internal 1.8V regulator output capacitor connection. Connect a low-ESR, 1 µF capacitor to DGND.
21	AGND	GND	Analog Ground. Connect to DGND through a single point connection.
22	VDDA	Power	Analog 3.3V supply. Connect a capacitor to AGND. Connected to main 3.3V supply on the board.
31	VPORT_NEG4	Power	PD77718T4/PD77718T3: Negative port 4 output PD77714T4: No connect, leave floating
33	VPORT_NEG5	Power	PD77718T4/PD77718T3: Negative port 5 output PD77714T4: No connect, leave floating
36	VMAIN_36	Power	Connect to V_{MAIN} through PCB trace or 0Ω resistor for basic level protection. Leave unconnected for enhanced surge protection. For more details, see *PD777xx Surge Protection Application Note*.
38	VPORT_NEG6	Power	PD77718T4/PD77718T3: Negative port 6 output PD77714T4: No connect, leave floating
40	VPORT_NEG7	Power	PD77718T4/PD77718T3: Negative port 7 output PD77714T4: No connect, leave floating
43	VDD	Power	Digital 3.3V supply. Connect a capacitor to DGND. Connected to main 3.3V supply on the board.
44	RESET_IN_N	Input	Device Reset. Connect a pull-up resistor to V_{DD}. This functionality depends on firmware version. It is recommended to route this connection and DNI the Isolator.
45	INT_OUT_N	Output	Interrupt output pin (open drain). Leave open if not used. This functionality depends on firmware version. It is recommended to route this connection and DNI the Isolator.
46	DGND	GND	Digital Ground. Connect to AGND through a single point connection.
47	VDDCORE	Power	Internal 1.2V regulator output capacitor pin. Connect 1.0 µF low ESR capacitor to DGND.

...........continued

Pin	Designator	Type	Description
48	A0	Input	I^2C device address. Connect to V_{DD} or DGND. See Table 5-1
49	A1	Input	I^2C device address. Connect to V_{DD} or DGND.
50	A2	Input	I^2C device address. Connect to V_{DD} or DGND.
51	A3	Input	I^2C device address. Connect to V_{DD} or DGND.
52	AUTO	Input	Connect a 10 kΩ resistor from VDD to AUTO pin.
53	SCLIO	Bidirectional	I^2C clock
54	SDIO	Bidirectional	I^2C data input/output
56	OSS	Input	OSS shuts down ports based on priority settings. Connect to Pin 7, OSS_OUT, of the PD77010 through isolation.
EPAD	EPAD	Analog	Exposed Pad. Connect to AGND through short trace on PCB underneath device. AGND must have enough copper masks to ensure adequate thermal performance.

5. Application Information

This section provides practical operation information for the PD77718T4/ PD77718T3 and PD77714T4 devices.

5.1 Operational Modes

This section provides a high level description of the available operational modes. These are listed as follows:

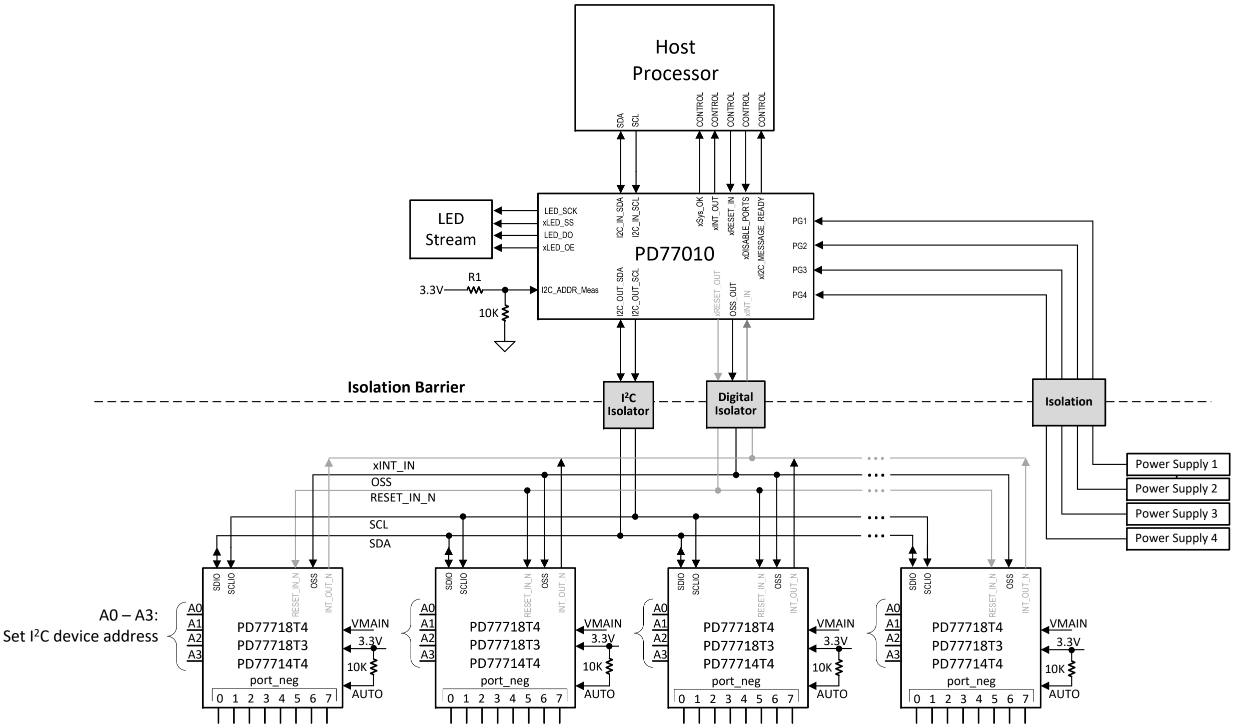
- Controller mode

5.1.1 Controller Mode

This section describes the chipset operation with PD77010 PSE Controller. The PD77010 device is used in conjunction with the PD77718T4, PD77718T3, or PD77714T4 devices, where the PD77010 PSE Controller provides multi-port PoE functions, such as port mapping (Port Matrix), port priority, port status, and system power management.

The following figure shows the Controller Mode application.

Figure 5-1. Controller Mode Application



Notes:

- Alternatively, the isolation may be placed between the PD77010 and the Host Processor. For additional details, consult Microchip.
- The Reset and Interrupt functions (shown in grey) are reserved. The use of these functions depend on firmware revision. To mitigate against the possibility that some firmware versions may require these functions, it is recommended that the PCB design route these functions, however the isolator may be a "do not populate" option.

5.2 I^{2}C

The port I^{2}C address is programmed through pins A0, A1, A2, A3 (pins 48–51). Tie each pin to V_{DD} or DGND to set the I^{2}C address, as listed in the following table.

Note: The I^{2}C address is a 7-bit address.

Table 5-1. PD77718T4, PD77718T3, and PD77714T4 I^{2}C Address Select

A3	A2	A1	A0	I^{2}C Address
0	0	0	0	0x20
0	0	0	1	0x21
0	0	1	0	0x22
0	0	1	1	0x23
0	1	0	0	0x24
0	1	0	1	0x25
0	1	1	0	0x26
0	1	1	1	0x27
1	0	0	0	0x28
1	0	0	1	0x29
1	0	1	0	0x2A
1	0	1	1	0x2B
1	1	0	0	0x2C
1	1	0	1	0x2D
1	1	1	0	0x2E
1	1	1	1	0x2F

5.3 2-Pair and 4-Pair (2P/4P) Operation

The IEEE 802.3bt standard introduces the ability to drive a PD (that supports this mode) by using four pairs and allowing higher PD power support. The IEEE 802.3bt standard discusses the 4P definition from a logical port point of view. That is, a port in the IEEE 802.3bt standard can operate either in 2P mode or in 4P mode. A PD that can accept power on both ALT-A and ALT-B at the same time is regarded as a 4P-capable PD.

5.3.1 2P Operation

PSE port can operate over two pairs, that is, only two pairs are used to actively deliver power to the PD, either on ALT-A or ALT-B, but not both. This is allowed when the assigned class is 0 to 4. A 2P operation uses a single physical port that is considered a logical port.

5.3.2 4P Operation

When the assigned class is 5 to 8, the PSE port must deliver the power over four pairs. When operating in 4P, power is delivered to the PD on both pair sets (ALT-A and ALT-B), that is, two physical ports are combined to create a single logical 4P port required for the 4P operation.

When operating in the 4P mode, the two physical ports that create the one logical four pair port must be chosen from the same physical PD77718T4, PD77718T3, or PD77714T4 IC.

5.4 Communication Interface

The Communication interface between the PD77718T4, PD77718T3, or PD77714T4 and the PD77010 is through the I^{2}C interface. For more detailed information, see *PD77718T4, PD77718T3, and PD77714T4 Register Map*.

5.5 OSS Pin Behavior

A dedicated fast shut-down bus is located between the PD77010 and the PD7771x devices. OSS pin is used as the fast communication interface between the PD7771x and PD77010 for implementing the Power Good Functionality. The OSS output control pin is used to turn off ports of a certain priority due to live removal or failure in one of the power supplies and when dynamic over power is above the active budget by more than 5%.

The bus is always operational even when using a single power supply. The OSS pin of the PD7771x devices must be connected to the OSS_OUT of the PD77010 device through digital isolation. The power budget and reallocation of the power based on priority (if there is a loss of a power supply) is defined through the Power Good pins.

5.6 Compliance to Limited Power Source Requirements

The Microchip PD77718T4, PD77718T3, and PD77714T4 PoE managers fulfill the Limited Power Source (LPS) requirements per IEC/UL/EN62368-1. In other words, the PD77718T4, PD77718T3, and PD77714T4 are IC current limiters that are used for current limiting the output of the power source in accordance with the requirements of an LPS.

As per IEC62368-1 Ed2, if the system power supply exceeds 250 VA, then the PD77718T4, PD77718T3, or PD77714T4 devices are shorted during compliance testing. Therefore, an external current limiter or per-port fuse is required. If the total system power is less than 250 VA, then the PD77718T4, PD77718T3, or PD77714T4 device is not shorted during compliance testing and LPS requirements are met by virtue of the PD77718T4, PD77718T3, or PD77714T4 device being an IC current limiter.

As per IEC62368-1 Ed3, the IC current limiters used for current limiting in power sources are not shorted from input to output if they comply with all of the following:

- The IC current limiters limit the current to the value defined by the manufacturer, which must be less than 5A under normal operating conditions with any specified drift accounted for
- The IC current limiters are entirely electronic and have no means of manual operation or reset
- The IC current limiters output current is limited to 5A or less (specified maximum load)

This implies that per port fuses might not be required to meet IEC62368-1 Ed3. The compliance requirements are as follows:

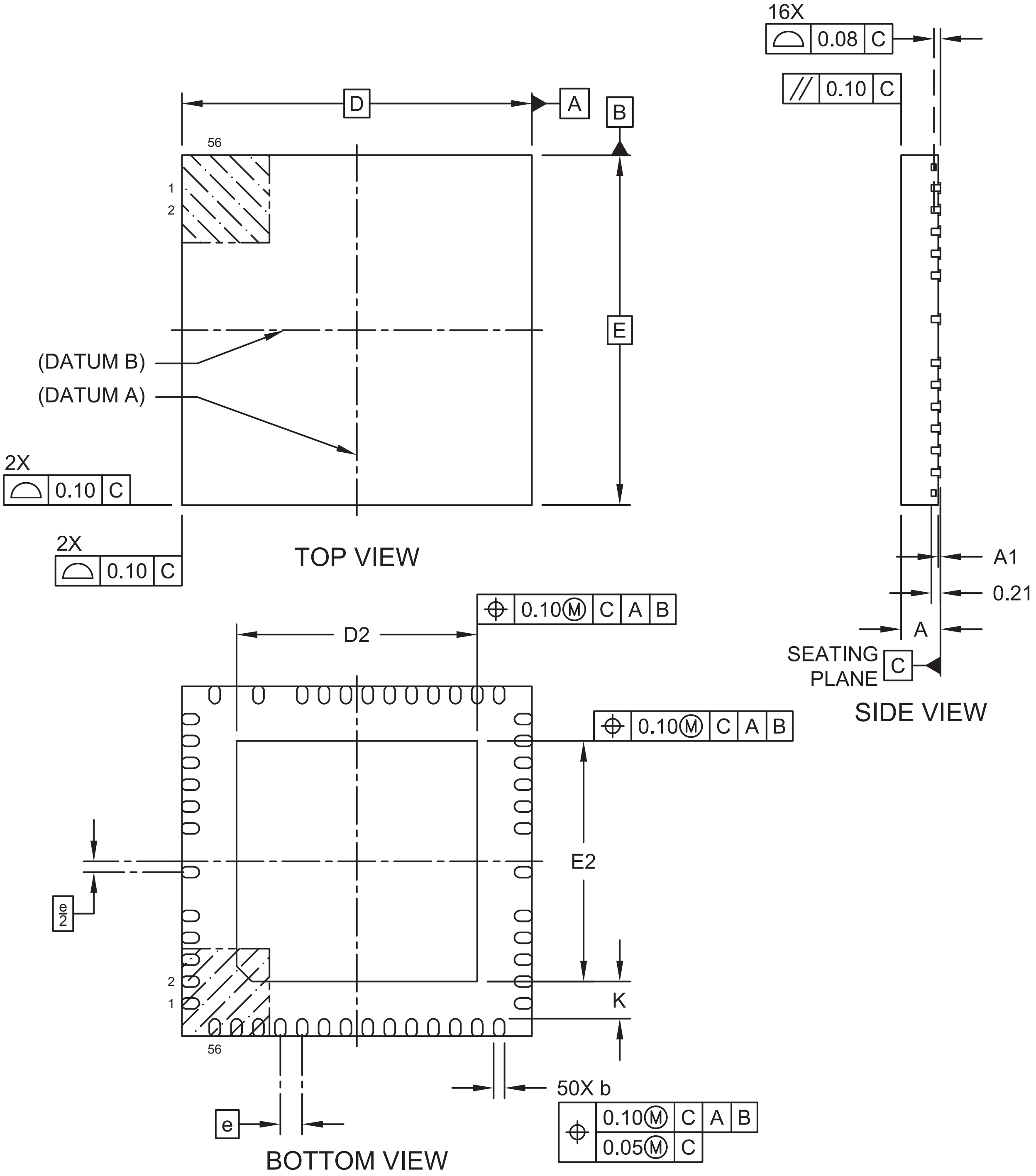
- If a system is intended to meet IEC62368-1Ed2: Per port fuse is required if the total system power > 250 VA
- If a system is intended to meet IEC62368-1Ed2: Per port fuse is not required if the total system power is < 250 VA
- If a system is intended to meet IEC62368-1Ed3: Per port fuse may not be required

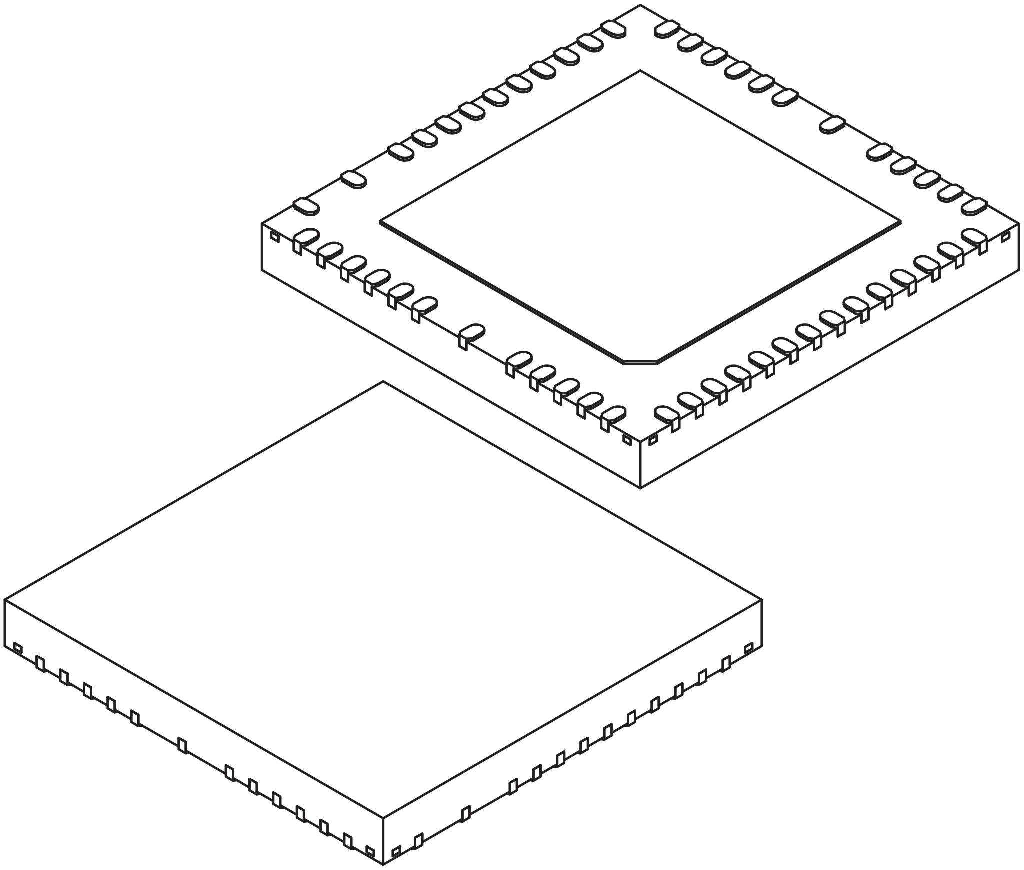
For additional details, request for Microchip *AN3527 Compliance to Limited Power Source Requirements*. These statements are Microchip's good faith interpretation of the IED62368-1 standard. Consult IEC or equivalent agency and the IEC62368-1 Ed2/Ed3 standards for official positions with respect to this topic.

6. Package Specifications

This device is a 56-lead very thin plastic quad flat, no lead package (KDC), 8 mm x 8 mm x 0.9 mm body [VQFN] with depopulated terminals and a 5.5 mm^2 exposed pad. For latest package drawings, see Microchip Package Drawings.

Figure 6-1. Package Outline Drawing (POD)





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	56		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	5.40	5.50	5.60
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	5.40	5.50	5.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.70	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

6.1 Recommended PCB Layout

The following figures show the recommended PCB layout of the PD77718T4, PD77718T3, or PD77714T4 device.

Note: All figure dimensions are in mm.

Figure 6-2. Solder Mask (Component Side)

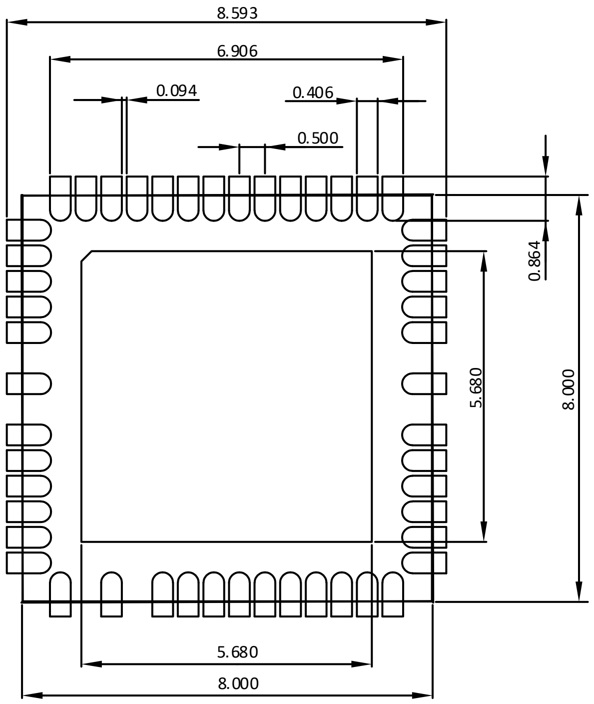


Figure 6-3. Solder Mask (Print Side)

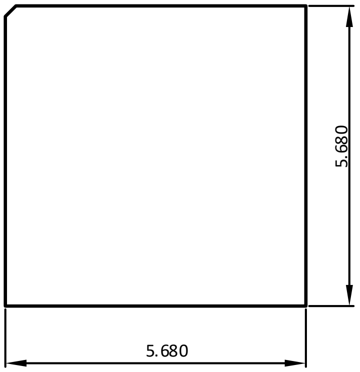


Figure 6-4. Copper Layer (Component Side)

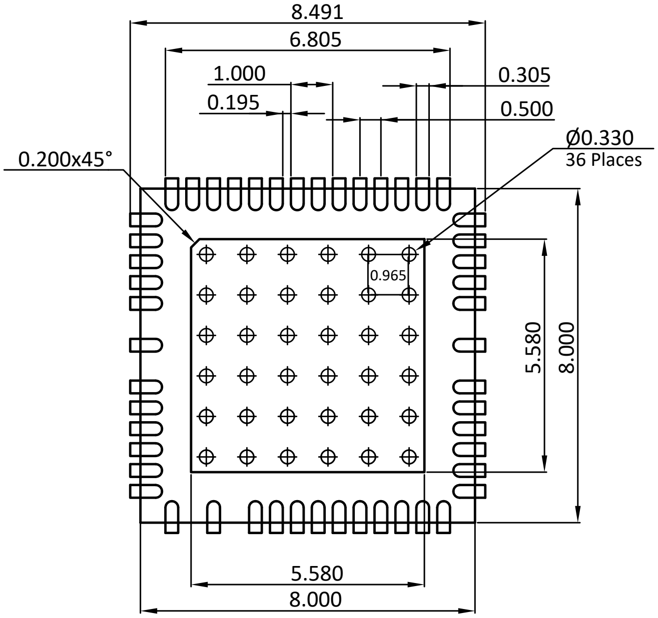
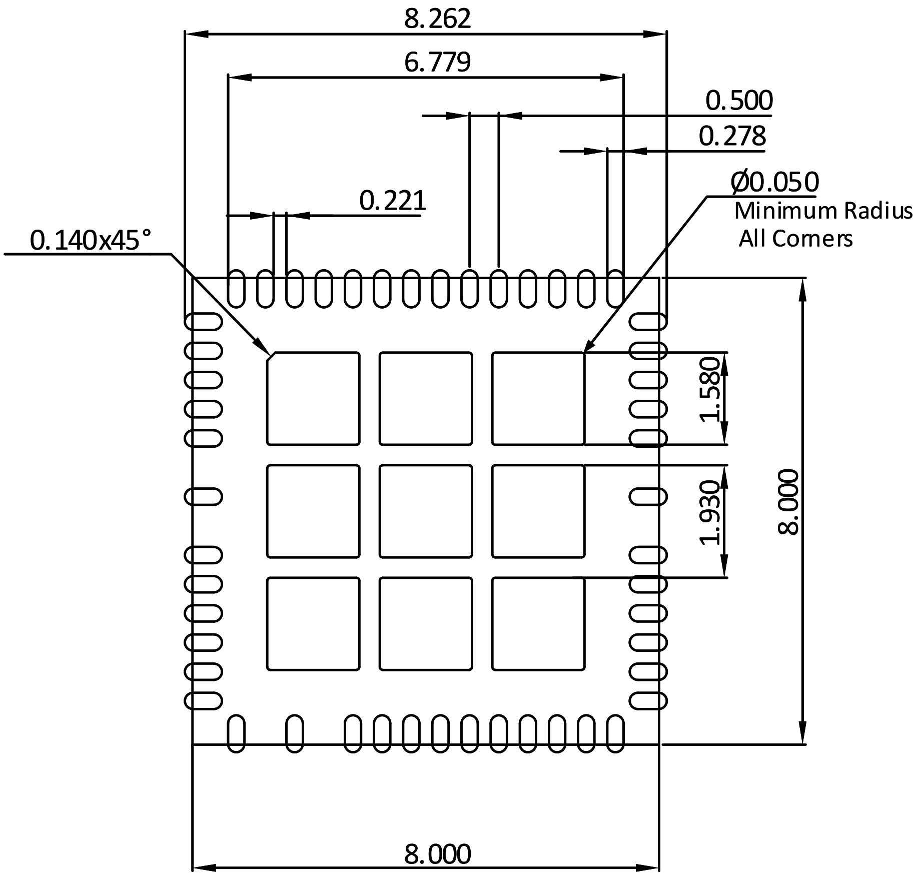
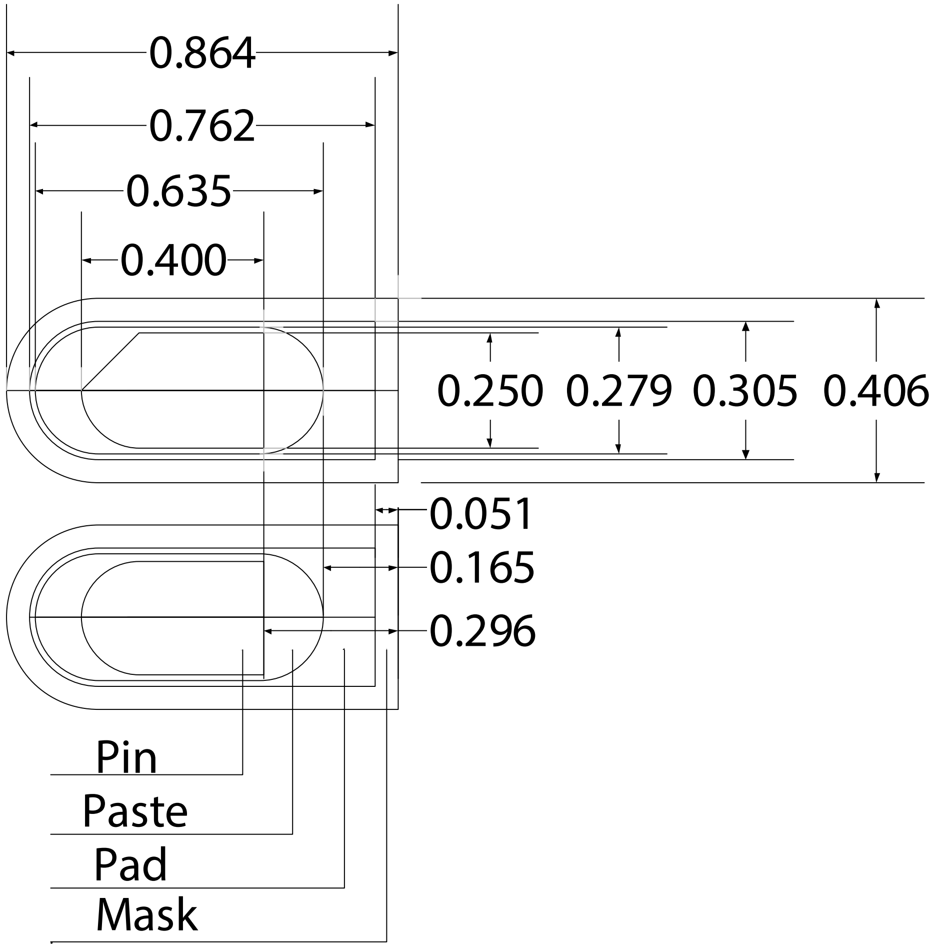


Figure 6-5. Paste Mask (Component Side)



Note: Use a 5 mil stencil.

Figure 6-6. Pin Geometry (Component Side)



6.2 Thermal Properties

The following table lists the thermal properties of the device.

Table 6-1. Thermal Properties[1]

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	θ_{JA}	21.03	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$	10.04	°C/W
Junction-to-board thermal resistance	θ_{JB}	4.12	°C/W
Junction-to-top characterization parameter	ψ_{JT}	0.334	°C/W

Note:

1. Using the JESD51-7 test board.

6.3 Recommended Solder Reflow Information

The following list shows the solder reflow information:

- RoHS 6/6
- Pb-free 100% Matte Tin Finish
- Package Peak Temperature for Solder Reflow (40s maximum exposure)—260 °C (0 °C, –5 °C)

The following tables list the classification reflow profile and Pb-Free Process—package classification reflow temperature details.

Table 6-2. Classification Reflow Profile

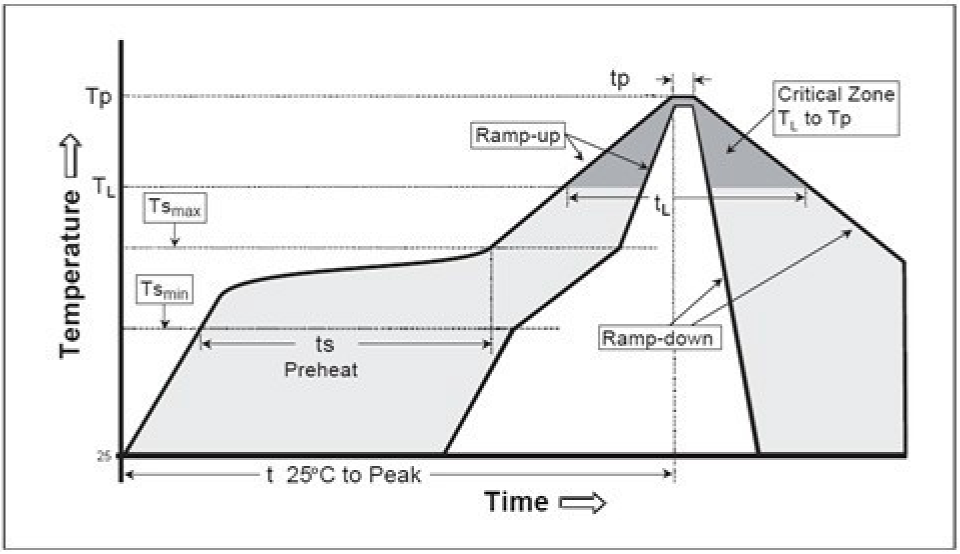
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TS_{MAX} to T_P)	3 °C/s maximum	3 °C/s maximum
Preheat		
Temperature min (TS_{MIN})	100 °C	150 °C
Temperature max (TS_{MAX})	150 °C	200 °C
Time (ts_{MIN} to ts_{MAX})	60s to 120s	60s to 180s
Time Maintained		
Temperature (T_L)	183 °C	217 °C
Time (t_L)	60s to 150s	60s to 150s
Peak classification temperature (T_P)	210 °C to 235 °C	240 ℃ to 255 °C
Time within 5 °C of actual peak temperature (t_P)	10s to 30s	20s to 40s
Ramp-down rate	6 °C/s maximum	6 °C/s maximum
Time 25 °C to peak temperature	6 minutes maximum	8 minutes maximum

Table 6-3. Pb-Free Process—Package Classification Reflow Temperatures

Package Thickness	Volume < 350 mm^3	Volume 350–2000 mm^3	Volume > 2000 mm^3
Less than 1.6 mm	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6 mm to 2.5 mm	260 + 0 °C	250 + 0 °C	245 + 0 °C

The following figure shows the classification reflow profile.

Figure 6-7. Classification Reflow Profile



7. Tape and Reel Specifications

This section provides the tape and reel specifications.

The following figures show the tape and reel pin 1 orientation and tape specifications of the PD77718T4, PD77718T3, and PD77714T4 devices.

Figure 7-1. Tape and Reel Pin 1 Orientation

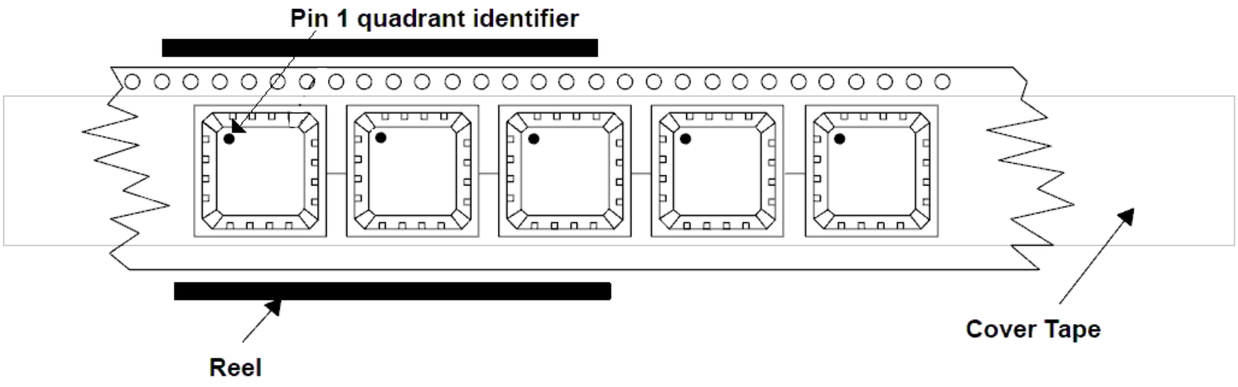
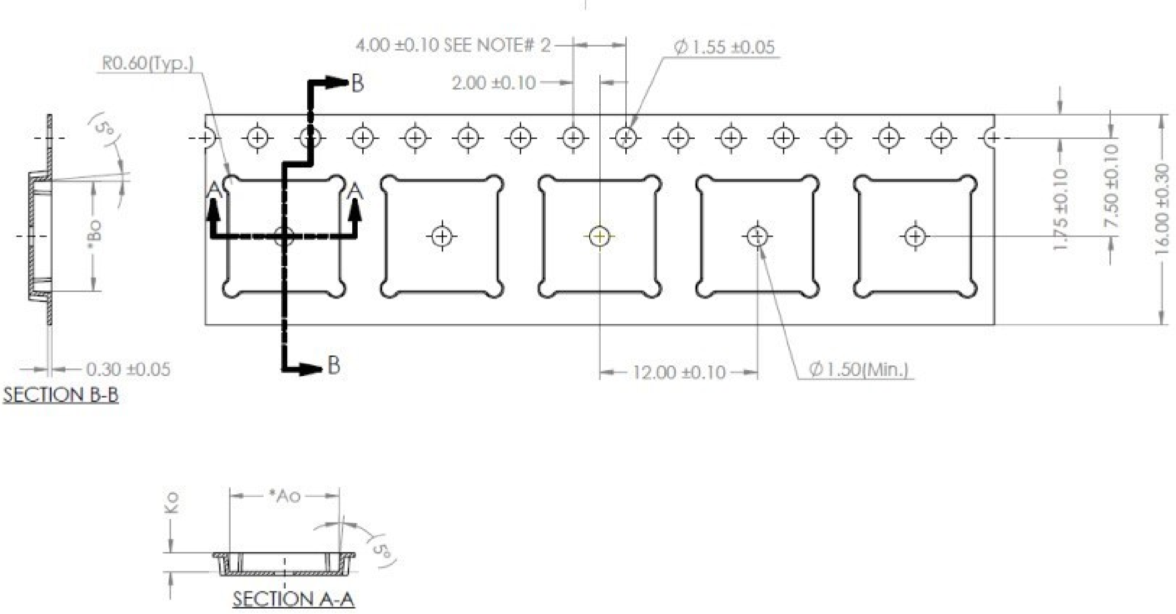


Figure 7-2. Tape Specifications



The following table lists the tape mechanical data details of the PD77718T4, PD77718T3, and PD77714T4 devices.

Table 7-1. Tape Mechanical Data

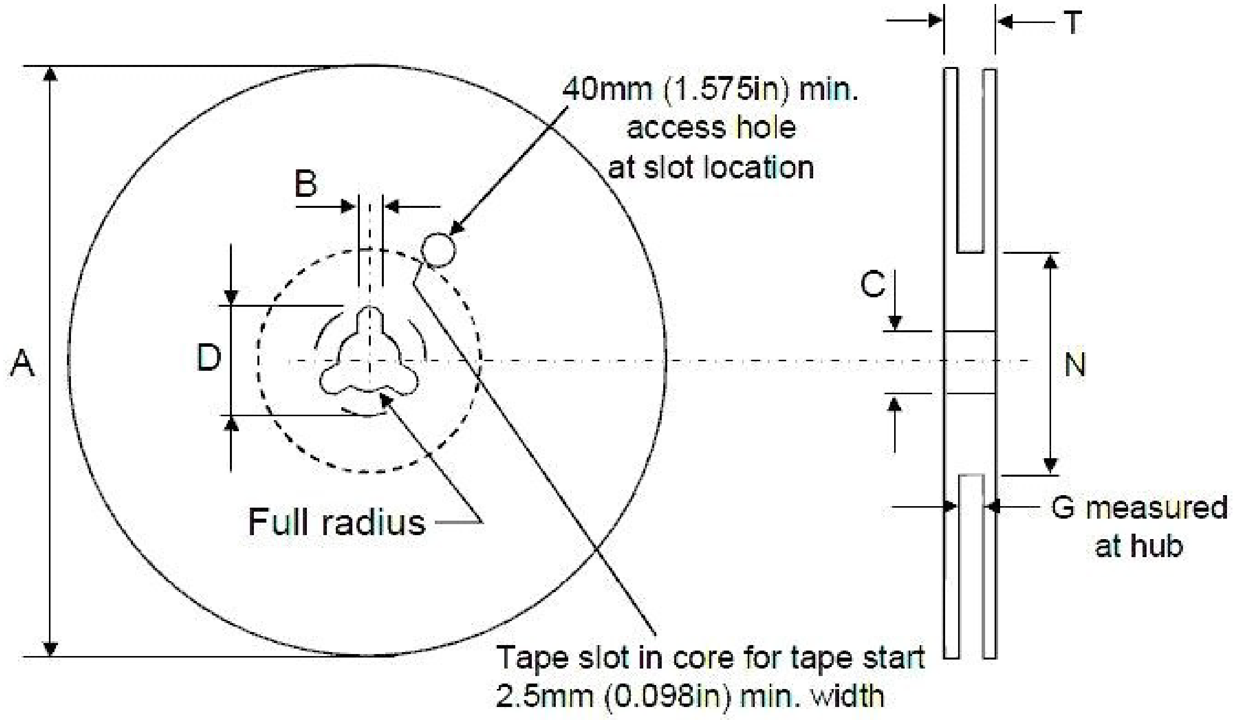
Dimension	Value (mm)
A0	8.35 ±0.10
B0	8.35 ±0.10
K0	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10

...........continued

Dimension	Value (mm)
Width	16.00 ±0.30

The following figure shows the reel specifications of the PD77718T4, PD77718T3, and PD77714T4 devices.

Figure 7-3. Reel Specification



The following table lists the reel mechanical data details of the PD77718T4, PD77718T3, and PD77714T4 devices.

Table 7-2. Reel Mechanical Data

Dimensions	Value (mm)	Value (inch)
Tape size	16.00 ±0.3	0.630 ±0.012
A maximum	330	13
B maximum	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D minimum	20.2	0.795
N minimum	50	1.968
G	16.4 +2.0/−0.0	0.724 to 0.645
T maximum	29	1.142

Note: Base quantity: 2000 pieces

8. Ordering Information

The following table lists the part ordering information of the device.

Table 8-1. Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking
PD77718T4ILQ-VVVV-SSSS-TR(2,3)	Plastic QFN 8 mm × 8 mm (56 lead)	Tape and Reel	−40 °C to 85 °C	Microchip Logo PD77718T4 e3 Arm® YYWWNNN[1]
PD77718T3ILQ-VVVV-SSSS-TR(2,3)	Plastic QFN 8 mm × 8 mm (56 lead)	Tape and Reel	−40 °C to 85 °C	Microchip Logo PD77718T3 e3 Arm® YYWWNNN[1]
PD77714T4ILQ-VVVV-SSSS-TR(2, 3)	Plastic QFN 8 mm × 8 mm (56 lead)	Tape and Reel	−40 °C to 85 °C	Microchip Logo PD77714T4 e3 Arm® YYWWNNN[1]

Notes:

1. YY= Year; WW= Week; and NNN= Trace code
2. VVVV = Firmware version
3. SSSS = Firmware parameters options

9. Reference Documents

This document has the following reference documents:

- *PD77010 PoE PSE Controller Data Sheet*
- *AN5347 Designing an IEEE® 802.3bt PoE System With PD77718T4, PD77718T3, and PD77714T4*
- *AN4813 Surge Protection for Systems Based on PD777xx 8-Port PSE PoE Controller/Manager*
- *AN4952 PD777xx PSE Firmware Download and Replace Flow*

10. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 10-1. Revision History

Revision	Date	Description
B	02/2025	The following is the summary of changes made in this revision: • Updated Figure 1 • Updated Table 8-1. Ordering Information • Updated Figure 6-4. Copper Layer (Component Side)
A	12/2024	Initial revision

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