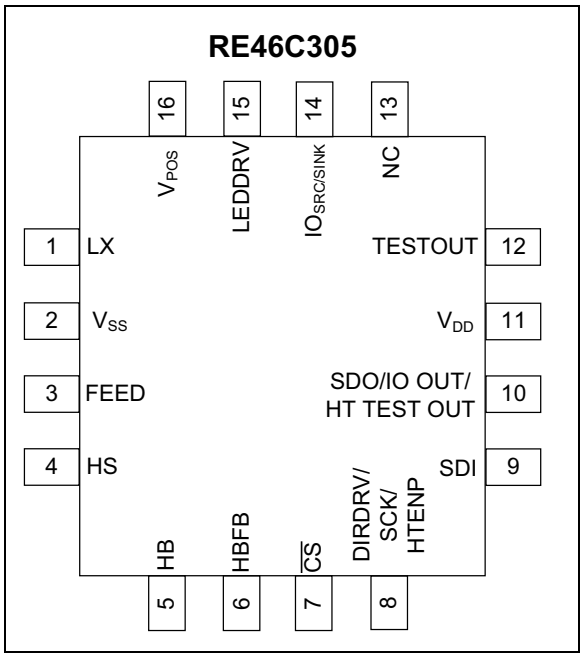
RE46C305

Piezoelectric Horn Driver with Boost IO and Built-In Horn Fault Testing

Features

- 2 and 3 Terminal Piezoelectric Horn Driver with Direct Drive Capability
- 8.5V and 10 V Boost Converter
- IO Interconnect with Current Source/Sink Feature
- Low Quiescent Current
- Operation from two AA or Single Lithium Battery
- Horn Fault Detection Circuit
- Serial Interface Controlled
- LED Driver
- Packaging:
  - 4 x 4 mm, 16-Lead VQFN

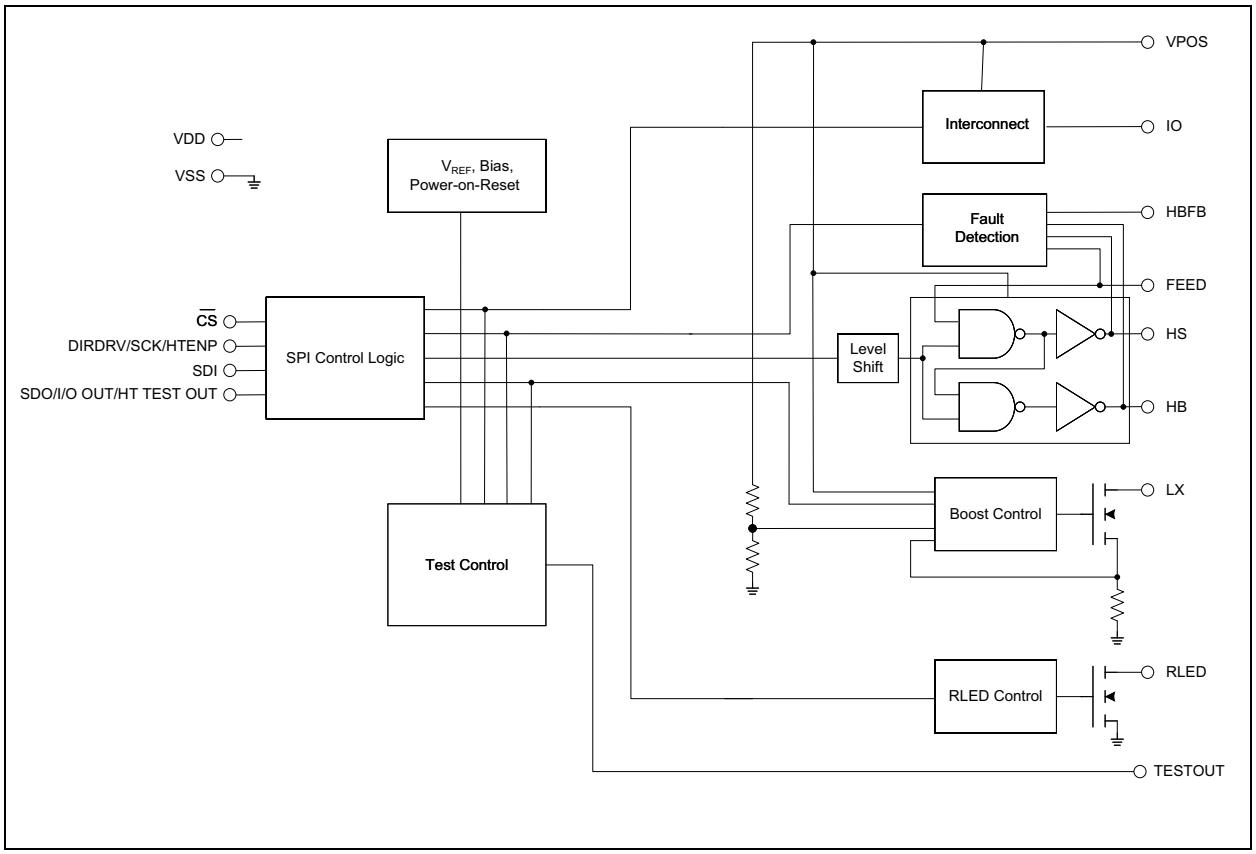
Package Type 4 x 4 mm, 16-Lead VQFN



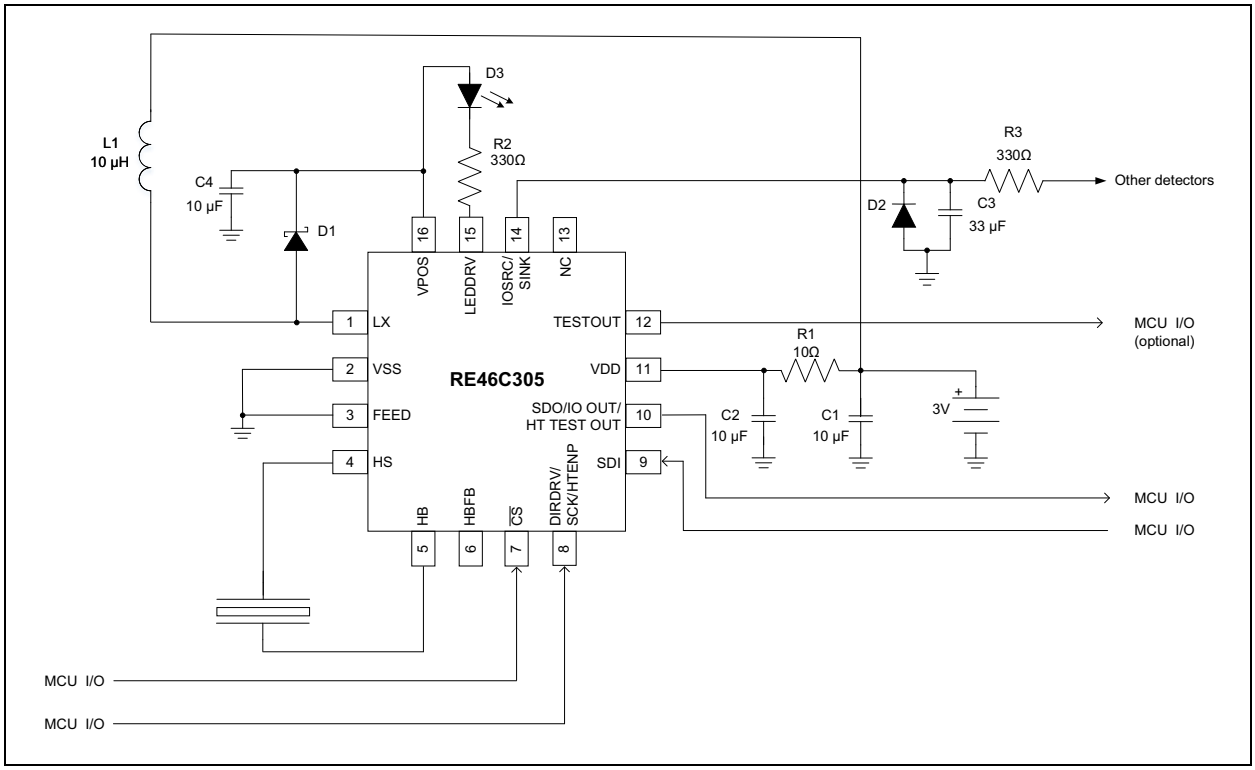
Description

RE46C305 is an advanced CMOS piezoelectric horn driver IC, equipped with a built in boost converter and controlled through a serial interface. It is designed for 3V battery or battery-backed applications. The circuit includes a boost converter and a driver suitable for powering a two or three-terminal piezoelectric horn. RE46C305 supports horn fault testing, enabling the detection of broken or shorted horn connections. An IO interface facilitates communication with interconnected units, offering both source and sink capabilities. Additionally, a visual LED driver provides signaling and can be used as a load for low battery checks.

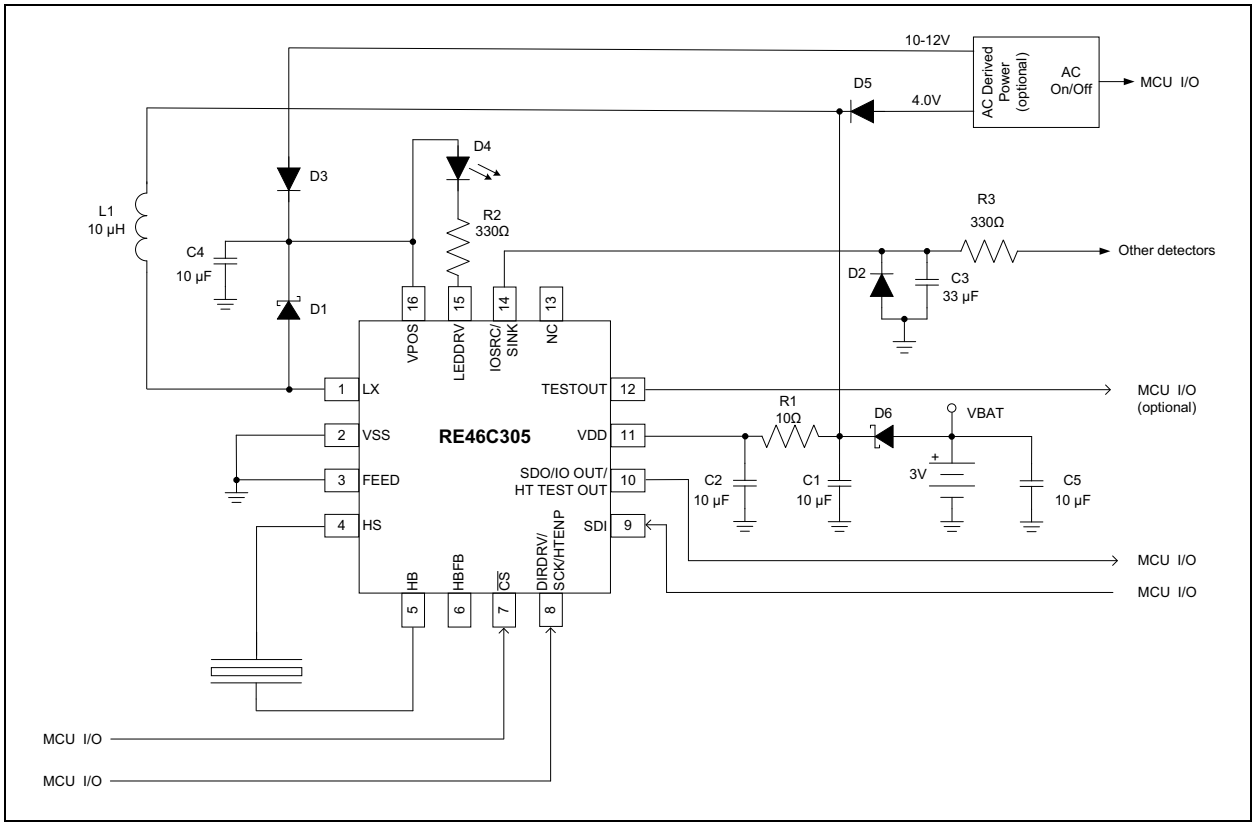
Functional Block Diagram



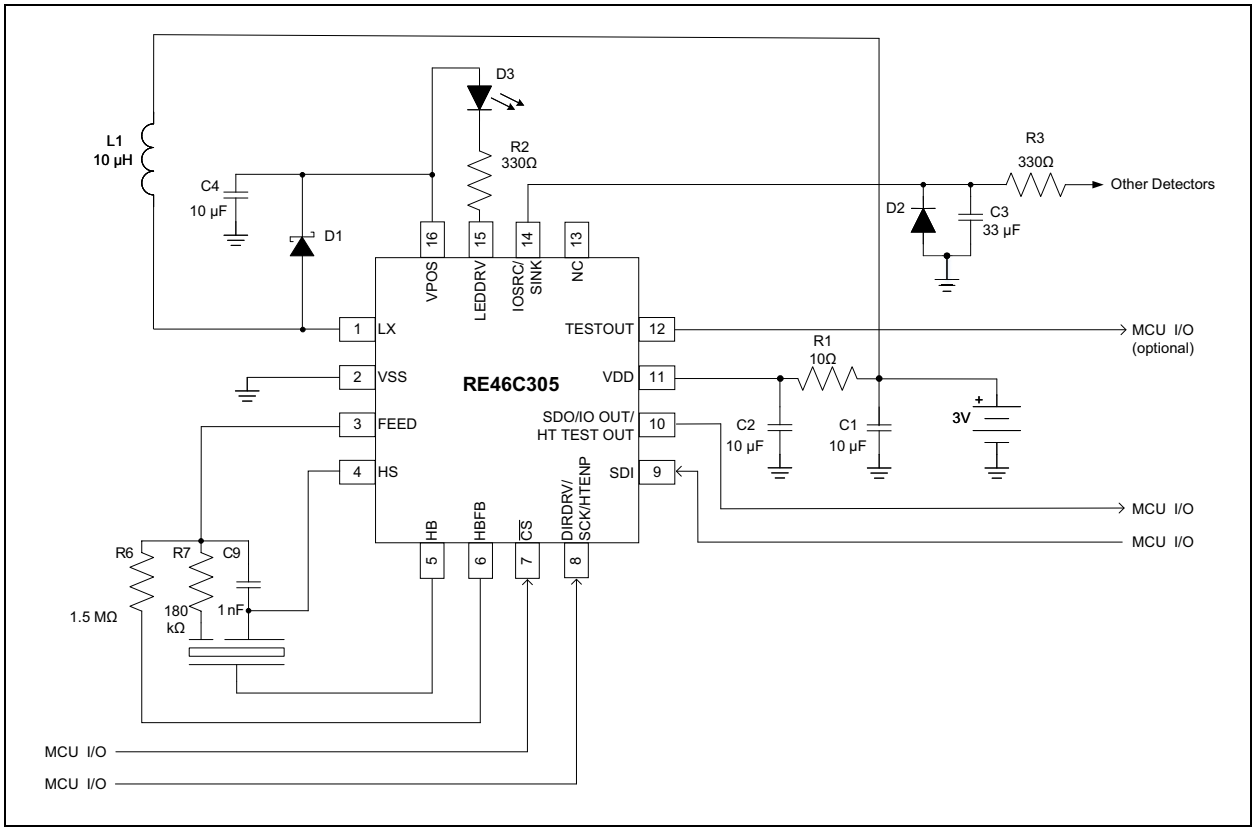
Typical Application - 3V with 2 Terminal Horn



Typical Application - 3V with 2 Terminal Horn AC and Battery Backup



Typical Application - 3V with Three-Terminal Horn



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings†

V_{DD} ..... +5.0V
V_{POS} ..... +15V
LX ..... -0.3V to V_{POS} + 0.6V
$IO_{src/sink}$ ..... -0.3V to +18.0V
FEED Input Voltage Range ..... -10V to +22V
Input Voltage Range ($\overline{CS}$, DIRDRV/SCK, SDI) ..... -0.3V to VDD + 0.3V
Output Voltage Range (SDO/IO OUT/HT TEST OUT, TESTOUT) ..... -0.3V to VDD + 0.3V
HB, HS, HBFB, LEDDRV Output Voltage Range ..... -0.3V to V_{POS}
Input Current ..... 10 mA
Output Current ..... 10 mA
Output Current (HBFB) ..... 1 mA
Continuous Output Current (HB, HS, VPOS, LEDDRV) ..... 40 mA
Continuous Output Current (IO_{src}) ..... 15 mA
Continuous Output Current (IO_{sink}) ..... 30 mA
Storage Temperature (T_{STG}) ..... -55°C to +125°C
Operating Temperature Range ..... -20°C to +85°C
Maximum Junction Temperature (T_J) ..... +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -20°C to +85°C, V_{DD} = 3V, V_{SS} = 0V, C_{Vpos} = 10 µF

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Power Supply							
Supply Voltage	V_{DD}	11	2.0	—	3.6	V	Operating, battery only operation
	V_{POS}	16	8.0	—	14.0	V	
POR	V_{POR}	—	—	1.5	—	V	
Standby I_{DD}	$I_{DDSTBY1}$	11	—	0.2	1.0	µA	Inputs low, no loads, boost regulator not running
	$I_{DDSTBY2}$		—	1.0	3.0	µA	IO input high, other inputs low, no loads, boost regulator not running
Quiescent I_{DD}	I_{DDQ}	11	—	35	60	µA	Inputs low, no loads, V_{POS} = 13V, LX=0.5V, boost enabled
Quiescent I_{Vpos}	I_{VposQ1}	16	—	20	75	µA	Inputs low, no loads, V_{POS} = 13V, LX=0.5V, boost enabled
	I_{VposQ2}		—	300	400	µA	Inputs low, no loads, V_{POS} = 13V, LX=0.5V, IO source enabled

Note 1: Warranted by functional test.
2: Typical values are for design information only and apply at +25°C.
3: The limits shown are 100% tested at +25°C only. Test limits are guard-banded based on temperature characterization to warrant compliance at temperature extremes.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -20°C to +85°C, V_{DD} = 3V, V_{SS} = 0V, C_{Vpos} = 10 µF

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Power Supply							
Input Leakage Low	I_{IL}	7, 8, 9	-100	—	—	nA	CS,DIRDRV/SCK, SDI
	I_{ILF}	3	-50	-15	—	µA	FEED pin = -10V, V_{POS} = 10V
Input Leakage High	I_{IH}	7, 8, 9	—	—	100	nA	$\overline{CS}$, DIRDRV/SCK, SDI
	I_{IHF}	3	—	20	50	µA	FEED pin = 22V, V_{POS} = 10V
Output Off Leakage High	I_{IHOZLX}	1	—	0.1	1	µA	LX = V_{POS} = 14V, boost disabled
	$I_{IHOZLED}$	15	—	0.1	1	µA	LEDDRV = V_{POS} = 14V, boost disabled
Input Voltage Low	V_{IL1}	7, 8, 9	—	—	1	V	$\overline{CS}$, DIRDRV/SCK, SDI
	V_{ILIO1}	14	—	—	2.1	V	Serial interface selected
	V_{ILIO2}	14	—	—	1.35	V	Serial interface selected
	V_{ILF}	3	—	—	3	V	V_{POS} = 10V
Input Voltage High	V_{IH1}	7, 8, 9	2.5	—	—	V	$\overline{CS}$, DIRDRV/SCK, SDI
	V_{IHIO1}	14	2.7	—	—	V	Serial interface selected
	V_{IHIO2}	14	1.75	—	—	V	Serial interface selected
	V_{IHF}	3	7	—	—	V	V_{POS} = 10V
Input Voltage Hysteresis	V_{IOHYS1}	14	—	200	—	mV	V_{ILIO1}, V_{IHIO1} selected
	V_{IOHYS2}		—	100	—	mV	V_{ILIO1}, V_{IHIO1} selected
	V_{INHYS}	7, 8, 9	—	500	—	mV	
Output Voltage Low	V_{OL}	10, 12	—	0.1	0.5	V	I_{LOAD} = 1 mA
	V_{OLH}	4, 5	—	0.3	0.6	V	HS or HB, I_{OUT} = 16 mA, V_{POS} = 10V, horn disabled
	V_{OLHBFB}	6	—	0.1	0.5	V	HBFB, I_{OUT} = 100 uA
	V_{OLLED1}	15	—	—	0.5	V	10 mA load, V_{POS} = 10V
	V_{OLLED2}	15	—	—	1.0	V	30mA load, V_{POS} = 10V
Output Voltage High	V_{OH}	10, 12	2.4	2.6	—	V	I_{LOAD} = -1 mA
	V_{OHHS}	4	9.4	9.7	—	V	HORNS, I_{OUT} = -16mA, V_{POS} = 10V, horn enabled, DIRDRV = 1
	V_{OHHB}	5	9.4	9.7	—	V	HORNB, I_{OUT} = 16 mA, V_{POS} = 10V, horn enabled, DIRDRV = 0
	V_{OHHBFB}	6	9.5	9.7	—	V	HBFB, I_{OUT} = -100 µA
V_{POS} Output Voltage	V_{VPOS1}	16	10	11.5	13	V	Boost enabled, I_{OUT} = 10 mA
	V_{VPOS2}	16	8.5	10	11.5	V	Boost enabled, I_{OUT} = 10 mA
V_{POS} Efficiency	V_{EFF}	—	—	85	—	%	I_{LOAD} = 10 mA, horn enabled
V_{POS} Divider	$V_{VOPSx10}$	12	—	1	—	V	VPOSBuf - Register 3 bit 5 = 1
LX On Resistance	LXron	1	—	0.5	—	Ω	Force 500 mA and measure voltage on pin and calculate LXron.

Note 1: Warranted by functional test.

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -20°C to +85°C, V_{DD} = 3V, V_{SS} = 0V, C_{Vpos} = 10 µF

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
Power Supply							
LX Peak Current	LXpk0	1	375	500	625	mA	VPOSISel = 0; V_{VPOSx} - 0.100V
	LXpk1		—	800		mA	VPOSISel = 1; V_{VPOSx} - 0.100V
	LXpkSS		—	180		mA	VPOSISel = x; V_{VPOSx} = 3V, SS enabled, Reg0[2] = 0
IO Output Current	I_{OIH1}	14	25	—	60	µA	IO disabled, IO = 1V, V_{POS} = 10V (either VT selected)
	I_{OIH2}	14	—	—	90	µA	IO disabled, IO = 15V, V_{POS} = 10V (high VT selected)
	I_{OIH3}	14	—	—	110	µA	IO disabled, IO = 15V, V_{POS} = 10V (low VT selected)
	I_{OIOH1}	14	-4	-5	—	mA	IO enabled, IO = 5.8V; V_{POS} = 10V
		14	-4	-5	—	mA	IO enabled, IO = 4V; V_{POS} = 8.5V
	I_{OIOH2}	14	—	-5	-10	mA	IO enabled, IO = V_{SS}; V_{POS} = 8.5V, 10V
	I_{O1IOL1}	14	10	—	—	mA	IO Dump Current, IO source disabled, IO = 1V; V_{POS} = 10V
		14	—	15	—	mA	IO Dump Current, IO source disabled, IO = 1V; V_{POS} = 8.5V
Horn Default Detection							
I_{DD}	I_{DDHT}	11	—	50	120	µA	No shorts present
I_{POS}	I_{VPOSHT}	16	—	5	10	µA	No shorts present
HTVsrc	VHTVsrc1hb	5	0.825	0.9	0.975	V	Reg1[6:5] = Reg2[6] = HTENP = 1; Reg2[7] = Reg3[0] = 0; IHB < 100 nA
	VHTVsrc2hb	5	0.925	1.0	1.075	V	Reg1[6:5] = Reg2[6] = Reg3[0] = HTENP = 1; Reg2[7] = 0; IHB < 100 nA
	VHTVsrc1hs	4	—	0.9	—	V	Reg1[6:5] = Reg2[7] = HTENP = 1; Reg2[6] = Reg3[0] = 0; IHS < 100 nA
	VHTVsrc1fb	3	—	0.9	—	V	Reg1[6:5] = Reg2[7:6] = Reg3[4] = HTENP = 1; Reg3[0] = 0; IFB < 100 nA

Note 1: Warranted by functional test.

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -20°C to +85°C, V_{DD} = 3V, V_{SS} = 0V, C_{Vpos} = 10 µF

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
HTIsnk	IHTIsnk1hb	5	1	2	3	µA	Reg1[6:5] = Reg2[6] = Reg2[0] = 1; HTENP = Reg2[7] = 0; HB = 1V
	IHTIsnk2hb	5	—	2	—	µA	Reg1[6:5] = Reg2[6] = HTENP = 1; Reg2[7] = Reg2[0] = 0; HB = 1V
	IHTIsnk1hs	4	1	2	3	µA	Reg1[6:5] = Reg2[7] = Reg3[0] = HTENP = 1, Reg2[0] = 0, Reg2[6] = 0; HS = 1V
HTIsnk	IHTIsnk2hs	4	—	2	—	µA	Reg1[6:5] = Reg2[7] = 1; Reg2[0] = 1, Reg2[6] = Reg3[0] = HTENP = 0; HS = 1V
	IHTIsnk1fb	3	1	2	3	µA	Reg1[6:5] = Reg2[7:6] = Reg3[4] = 1; Reg3[0] = HTENP = 1; Reg2[0] = 0; FEED = 2V
HTIpd	IHTIpd1hb	5	1	2	3	µA	Reg1[6:5] = 1; Reg2[7:6] = HTENP = 0; HB = 1V
	IHTIpd2hb	5	—	2	—	µA	Reg1[6:5] = Reg2[2] = 1; Reg2[3] = HTENP = 0; HB = 1V
	IHTIpd3hb	5	—	2	—	µA	Reg1[6:5] = 1; Reg3[4] = HTENP = 0V; HB = 1V
	IHTIpd1hs	4	1	2	3	µA	Reg1[6:5] = 1; Reg2[7:6] = HTENP = 0; HS = 1V
	IHTIpd2hs	4	—	2	—	µA	Reg1[6:5] = 1; Reg2[3:2] = HTENP = 0; HS = 1V
	IHTIpd3hs	4	—	2	—	µA	Reg1[6:5] = 1; Reg3[4] = HTENP = 0; HS = 1V
	IHTIpd4hs	4	—	2	—	µA	Reg1[6:5] = Reg2[1] = Reg3[4] = 1; HTENP = 0; HS = 1V
	IHTIpd1fb	3	1	2	3	µA	Reg1[6:5] = 1; Reg3[4] = HTENP = 0; FEED = 1V
	IHTIpd2fb	3	—	2	—	µA	Reg1[6:5] = Reg2[1] = Reg3[4] = 1; HTENP = 0; FEED = 1V
	IHTIpd3fb	3	—	2	—	µA	Reg1[6:5] = Reg2[1] = Reg3[4] = HTENP = 1; FEED = 1V
	IHTIpd4fb	3	—	2	—	µA	Reg1[6:5] = HFT3T = 1; Reg2[1] = HTENP = 0; FEED = 1V

Note 1: Warranted by functional test.

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3: The limits shown are 100% tested at +25°C only. Test limits are guard-banded based on temperature characterization to warrant compliance at temperature extremes.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -20°C to +85°C, V_{DD} = 3V, V_{SS} = 0V, C_{Vpos} = 10 µF

Parameter	Symbol	Test Pin	Min.	Typ.	Max.	Units	Conditions
HTdrv	VHTDvol1hb	5	—	0.4	1	V	Reg1[6:5] = 1; Reg2[3:2] = 0; IHB = 100 uA
	VHTDvol1hs	4	—	0.4	1	V	Reg1[6:5] = Reg2[2] = 1; Reg2[3] = 0; IHS = 100 uA
HTMeasVT	VHTM1hb	10	0.3	—	0.4	V	Reg1[6:5] = Reg3[1] = 1; Reg3[3] = 1; Reg2[5:4] = 0; HB Swept 0.1 - 1.0V; HTOut Measured (SDO)
	VHTM2hb	10	0.17	—	0.23	V	Reg1<6:5>=Reg3<3> 1; Reg2<5:4>=Reg3<1>=0; HB Swept; HTOut Measured (SDO)
	VHTM1hs	10	0.3	—	0.4	V	Reg1[6:5] = Reg2[4] = Reg3[1] = Reg3[3] =1; Reg2[5] = 0; HS Driven; HTOut Measured (SDO)
	VHTM1fb	10	0.3	—	0.4	V	Reg1[6:5] = Reg2[5:4] = Reg3[1] = Reg3[3] = HFT3T = 1; FEED Driven; HTOut Measured (SDO)
	VHTM1hbfb	10	0.3	—	0.4	V	Reg1[6:5] = Reg2[5] = Reg3[1]= Reg3[1] = HFT3T = 1; Reg2[4] = 0; HBFB Driven; HTOut Measured (SDO)
HTMeasOut Ratio	RHTM1hb	12	—	1	—	V/V	Reg1[6:5] = 1; Reg2[5:4] = 0; HB 0.1 - 1.0V; HTOut Measured (Test Out)
	RHTM1hs	12	—	1	—	V/V	Reg1[6:5] = Reg2[4] = 1; Reg2[5] = 0; HS 0.1 - 1.0V; HTOut Measured (Test Out)
	RHTM1fb	12	—	1	—	V/V	Reg1[6:5] = Reg2[5:4] = HFT3T = 1; FEED 0.1 - 1.0V; HTOut Measured (Test Out)
	RHTM1hbfb	12	—	1	—	V/V	Reg1[6:5] = Reg2[5] = HFT3T = 1; Reg2[4] = 0; HBFB 0.1 - 1.0V; HTOut Measured (Test Out)

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DC ELECTRICAL CHARACTERISTICS (CONTINUED)

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at T_A = -20°C to +85°C, V_{DD} = 3V, V_{SS} = 0V, C_{Vpos} = 10 µF							
Parameter	**Symbol**	**Test Pin**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
HTMPd	IHTMPD1hs	4	5	20	35	nA	Reg1[6:5] = Reg2[4] = 1; Reg2[5] = 0; Reg3[2] = 0; VHS = 1V; 27C
	IHTMPD2hs	4	10	30	45	nA	Reg1[6:5] = Reg2[4] = 1; Reg2[5] = 0; Reg3[2] = 1; VHS = 1V; 27C
	IHTMPD1hb	5	—	20	—	nA	Reg1[6:5] = 1; Reg2[5,4] = 0; Reg3[2] = 0; VHB = 1V; 27C
	IHTMPD1fb	4	—	20	—	nA	Reg1[6:5] = 1; Reg2[5,4] = 1; Reg3[2] = 0; VFB = 1V; 27C
	IHT-MPD1hbfb	10	—	20	—	nA	Reg1[6:5] = 1; Reg2[5] = 1; Reg2[4] = 0; Reg3[2] = 0; VHBFB = 1V; 27C
Serial Interface Timing (Diagram 1-1)							
Digital Pin Capacitance	CIN, COUT	7, 8, 9, 10	—	10	—	pF	(All logic inputs/outputs)
MAX. Clock Frequency	FCLK	8	—	10	—	MHz	C_{load} = 50 pF, Note 1
Min. Clock High Time	tHI	8	—	50	—	ns	C_{load} = 50 pF, Note 1
Min. Clock Low Time	tLO	8	—	50	—	ns	C_{load} = 50 pF, Note 1
Min. $\overline{CS}$ to First Rising Clock Edge	tCSSR	7, 8	—	50	—	ns	C_{load} = 50 pF, Note 1
Min. Data Input Setup Time	tSU	9	—	20	—	ns	C_{load} = 50 pF, Note 1
Min. Data Input Hold Time	tHD	9	—	40	—	ns	C_{load} = 50 pF, Note 1
Min. SCK to $\overline{CS}$ Rise Hold Time	tCHS	7, 8	—	50	—	ns	C_{load} = 50 pF, Note 1
Min. $\overline{CS}$ High Time	tCSH	7	—	100	—	ns	C_{load} = 50 pF, Note 1

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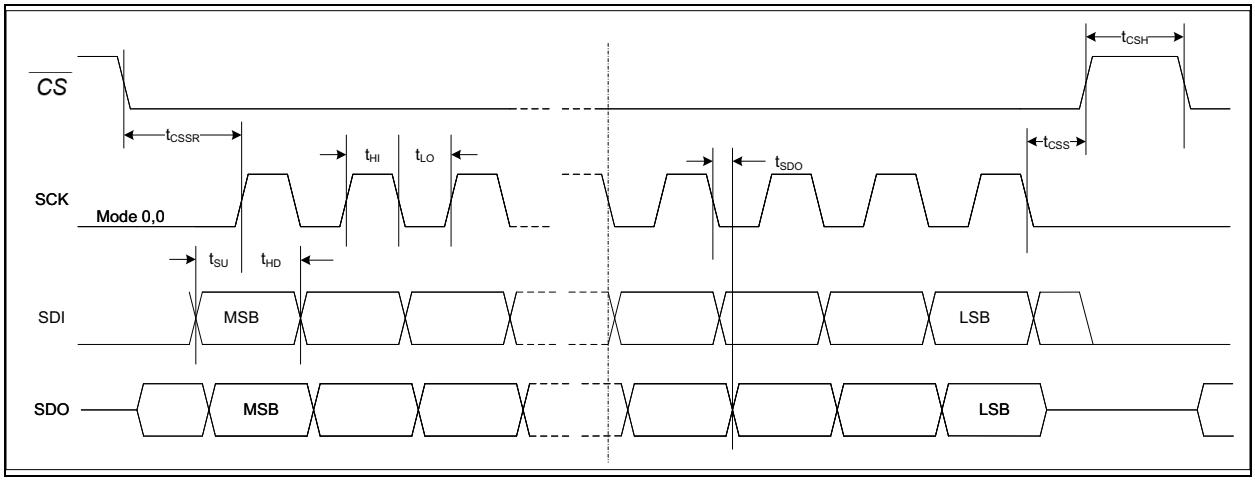


FIGURE 1-1: *Serial Interface Timing Mode 0,0.*

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated.						
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-20	—	+85	°C	
Storage Temperature Range	T_{STG}	-55	—	+125	°C	
Thermal Package Resistances						
Thermal Resistance, 16-Lead VQFN	θ_{JA}	—	35	—	°C/W	

2.0 PIN DESCRIPTION

TABLE 2-1: RE46C305 PIN FUNCTION

Pin Number	Type	Symbol	Description
1	Input/Output	LX	Open drain NMOS output used to drive the boost converter inductor. The inductor should be connected from this pin to the positive supply through a low resistance path.
2	GND	VSS	Connect to the negative supply voltage.
3	Input/Output	FEED	Usually connected to the FEEDBACK electrode of a three terminal piezoelectric horn through a resistor. For two terminal horn operation this pin must be tied low.
4	Input/Output	HS	HS is a complementary output to HB and connects to the ceramic electrode (S) of the piezoelectric transducer.
5	Input/Output	HB	HB is a complementary output to HS and connects to the metal electrode (B) of the piezoelectric transducer.
6	Input/Output	HBFB	Connect to the FEEDBACK pin through resistor - used during three terminal horn fault testing. When using two-terminal horn this pin should float.
7	Input	$\overline{CS}$	Chip Select Bar - used to enable serial interface as well as the multiplexing of the MCU pins 8, 9, 10.
8	Input	DIRDRV/SCK/HTENP	When $\overline{CS}$ = high, Horn Test is disabled through register setting (default operation) and two-terminal horn function is enabled through register setting. Then, this pin is the direct drive logic input to drive the piezoelectric horn. When $\overline{CS}$ = high and Horn Test is enabled through register setting this pin is the Horn Test enable and needs to be pulsed 25 ms for each horn test. When $\overline{CS}$ = low, this pin is the logic input to drive the serial interface clock.
9	Input	SDI	Serial Data input to write registers to control device operation. Needs to be driven low whenever $\overline{CS}$ = high.
10	Output	SDO/IO OUT/HT TEST OUT	When $\overline{CS}$ = high and Horn Test is disabled through register setting (default operation) this pin is the IO out to the MCU signaling a valid interconnect signal on the IO line. When $\overline{CS}$ = high and Horn Test is enabled through register setting this pin is the Horn test output reporting the result of the horn test performed. When $\overline{CS}$ = low, this pin is the logic output for the serial data.
11	Supply	VDD	Connect to the positive supply voltage.
12	Output	TESTOUT	Manufacturing test pin - optional: capability to bring MaxLD (goes high when boost is overloaded), HTMeas (analog Horn Fault Test signal) and V_{POSDiv} (divided V_{POS}) to that pin. V_{POSDiv} is nominally 1V regardless of which V_{POS} level is set.
13	NA	NC	Not connected.
14	Input/Output	IOSRC/SINK	IO interconnect source/sink driver to drive IO line (source) or to pull IO line low (sink). When source/sink disable pin will function as an input with a weak pull down
15	Open Drain	LEDDRV	LED Driver output.
16	Power	VPOS	Boosted voltage produced by DC-DC converter, Selectable 8.5V or 10V minimum.

TABLE 2-2: HORN MAPPING BASED ON $\overline{CS}$ AND SERIAL INTERFACE SETTINGS

Pin Number	Pin Name	Pin Function when			Pin Function - Mode
		$\overline{CS}$ is low	$\overline{CS}$ is high with Horn Test disabled	$\overline{CS}$ is high with Horn Test enabled	
1	LX	LX	LX	LX	
2	V_{SS}	V_{SS}	V_{SS}	V_{SS}	
3	FEED	FEED	FEED	FEED	Tie to V_{SS} for two terminal horn
4	HS	HS	HS	HS	
5	HB	HB	HB	HB	
6	HBFB	HBFB	HBFB	HBFB	NC for two-terminal horn
7	$\overline{CS}$	Low	High	High	To MCU
8	DIRDRV/SCK/HTENP	SCK	DIRDRV	HT Test Enable Pulse	To MCU
9	SDI	SDI	SDI (drive to V_{SS})	SDI (drive to V_{SS})	To MCU
10	SDO/IO OUT/ HT TEST OUT	SDO	IO OUT to MCU	HT Test Output	To MCU
11	V_{DD}	V_{DD}	V_{DD}	V_{DD}	
12	TEST OUT	Test Output	Test Output	Test Output	Optional to MCU
13	NC	NC	NC	NC	
14	IO Source/Sink to Line	IO Source/ Sink to Line	IO Source/Sink to Line	IO Source/Sink to Line	
15	LED Driver Output	LED Driver Output	LED Driver Output	LED Driver Output	
16	V_{POS}	V_{POS}	V_{POS}	V_{POS}	

TABLE 2-3: CONSIDERATIONS FOR TWO VS THREE TERMINAL CONFIGURATIONS

Horn Type	Horn Mode	Horn Test	FSSsel	HFT3T	HBFB
Three Terminal	FEED Input	Three Terminal	1	1	Enabled
Three Terminal	FEED Input	No Horn Test	1	0	Disabled
Three Terminal	Direct Drive	Three Terminal	0	1	Enabled
Three Terminal	Direct Drive	No Horn Test	0	0	Disabled
Two Terminal	Direct Drive	Two Terminal	0	0	Disabled

Note: If a three terminal horn is used and Horn Fault Test is not required (HFT3T = 0), R6 in Typical Application - 3V with Three-Terminal Horn should be connected to HB rather than HBFB.

3.0 DEVICE OVERVIEW

3.1 Introduction

The RE46C305 provides the necessary analog functions to build a microcontroller-based piezoelectric horn driver, interconnect and visual LED driver for use in smoke and CO detection products. This includes a horn driver with a fault detection feature. The RE46C305 supports three-terminal self-resonating horns with feedback or can be configured to operate a two-terminal horn in direct drive mode. The serial interface enables the microcontroller to have full control over the RE46C305 operation.

3.2 Power Control System

In a 3V battery-only system, the 3V battery connects to the V_{DD} pin through the RC filter shown in Typical Application - 3V with 2 Terminal Horn. The filter minimizes any boost regulator switching noise that may be present at the V_{DD} pin. In this setup, the microcontroller is powered directly from the battery, as is most of the internal circuitry of the RE46C305.

3.3 Boost Regulator

The boost regulator is an adjustable, fixed-off-time boost converter with peak current limiting. It operates at two voltage levels: 10.0V and 11.5V. The boost voltage selection is controlled by Register 0, bit 0 (VPOSVSel).

In boost operation, the peak LX current can be set to either 500 mA or 800 mA nominally. For systems that operate with input voltages less than 3V, the 800 mA peak current is recommended. The boost peak LX current selection is controlled by Register 0, bit 1 (VPOSISel). The boost regulator powers the horn driver and IO circuit or it can be used as a standalone boost. It is enabled by Register 1, bit 0 (BEn).

Although the boost regulator is intended for battery operation, it also features a low peak current mode of 500 mA if V_{DD} pin is supplied from a source other than a battery, such as a regulator. Register 0, bit 1, controls the peak boost LX current selection.

The boost regulator also supports a soft-start feature for boost operation, which limits the LX peak current to typically 180 mA. Once V_{POS} reaches its regulation point for the first time, the LX peak current level is determined by the VPOSISel setting in Register 0, bit 1. Soft start is controlled via Register 0, bit 2 (SSDis) and the default operation has soft start enabled.

Note: Using MaxLD is the preferred method to ensure proper boost operation. Sufficient time shall be allowed for soft start before loading the boost regulator i.e. horn or IO operation.

The basic equation governing boost operation is:

$$IDD = \frac{VBST}{VDD \times Eff} \times IBST$$

Eff represents the boost regulator's efficiency. When practical, selecting the lower boost voltage for a given operating mode helps minimize battery drain.

The health and status of the boost regulator are monitored through the TESTOUT or SDO pin. This can assist with development debugging or serve as a way to monitor the boost regulator's health. The selection of these signals and pins is controlled by Register 3, bits 7-5 and 3.

3.4 Horn Driver with Fault Detection

The horn driver drives a standard three-terminal piezoelectric horn connected to the pins HB, HS and FEED, or a two-terminal horn using the direct drive capability of the part. The microcontroller sets and resets the HRNEn bit with the required horn modulation pattern to sound the alarm. In low voltage applications, before asserting HRNEn high, the serial interface enables BEn for boost operation. This ensures sufficient horn drive capability to achieve the necessary sound pressure levels.

For two-terminal horns, the DIRDRV pin toggles the HB and HS pins at the desired operating frequency of the horn.

The operation of two or three-terminal horns is selected through Register 0, bit 3 (FDDSel).

In addition to the driver circuitry, serial interface controls (register 2[7:0]) test the HB, HS and FEED connections to the piezo. This testing covers all combinations of opens and shorts of these pins.

All opens/shorts occur at the horn disc, not at the DUT or feedback network.

The RE46C305 includes several selectable circuit configurations for Horn Fault Testing, which include:

- Tristating the HB and HS horn drivers (HRNEn, Register 1[4]).
- Driving HB, HS and/or FEED pins with an internal current-limited source to 0.9V or 1.0V (HTVsrc) or ground. The nominal current limit is 2 µA (HTIsnk).
- Connecting an internal comparator to the HB, HS, FEED or HBFB pins, with a selectable comparator reference of 0.2V or 0.35V (HTMeasVT). The measured node has a selectable pull-down current of 20 nA or 30 nA (HTMPd) to counter weak parasitic leakages.

- Monitoring the analog voltage at HB, HS, FEED, or HBFB pins during horn fault testing (HTMeasOut).
- Connecting a pull-down resistor of approximately 500 kΩ to HB and HS pins (HTIpd).
- Connecting an open-drain NMOS pull-down to HB, HS (HTdrv).

The parametric table outlines the register settings for each scenario mentioned above.

Horn Fault Test selection is controlled through the serial interface and test initiation occurs with a pulse on pin 8, configured as the HTENP pin ($\overline{CS}$ = high). Horn Fault Test is enabled through register 1, bit 5 (HFTEn). A pulse width of 25 ms is recommended and the HTENP pin must be pulsed for each horn test.

The test response becomes available after the negative edge of the HTENP pulse. After the HTENP pin goes low, read the HT test output result on pin 10 ($\overline{CS}$ = high). Horn Fault Test remains enabled through register 1, bit 5 (HFTEn).

Suggested configurations for two and three terminal horns appear in Table 2-3. Table 3-1 and Table 3-2 show the mapping of the horn test to each pin and its condition either open or shorted. The test code reflects the register 2 data written to perform each particular test.

During the test, there should be no noticeable sound emitted from the buzzer if it is properly configured.

TABLE 3-1: MAP OF THREE-TERMINAL HORN TESTS

	FB	HB	HS	Test Code
Opens	open	x	x	75
Opens	x	open	x	75
Opens	x	x	open	5B
Shorts	to V_{SS}	x	x	75
Shorts	to V_{DD}	x	x	74
Shorts	to HB	x	x	E1
Shorts	to HS	x	x	75
Shorts	x	to V_{SS}	x	75
Shorts	x	to V_{DD}	x	4A
Shorts	x	to HS	x	75
Shorts	x	x	to V_{SS}	5B
Shorts	x	x	to V_{DD}	5A

TABLE 3-2: MAP OF TWO-TERMINAL HORN TESTS

	HB	HS	Test Code
Opens	open	x	5B
Opens	x	open	8B
Shorts	to V_{SS}	x	47
Shorts	to V_{DD}	x	46
Shorts	to HS	to HB	47
Shorts	x	to V_{SS}	93
Shorts	x	to V_{DD}	92

3.5 RLED Driver

The RLED driver powers a red LED using a nominal 10V supplied by V_{POS}. This provides a means to perform a low battery test or provide a visual signal. The RLED driver current should be set to match the horn driver load current using the external resistor. The RLED driver is enabled or disabled via the serial interface register 1 bit 1, LEDEn.

3.6 Interconnect Operation

The interconnect circuit provides a communication interface to other compatible modules to signal an alarm condition. The $IO_{src/sink}$ pin functions as an input with a weak pull-down when the src/sink drivers are disabled, which is the default operation. An input trip selection setting of either 1.4V or 2.2V is available through register 0, bit 4 (IOinSel).

To signal an alarm, the IO interconnect source driver is enabled by setting register 1, bit 2 (IOsrcEn). The source driver is biased from V_{POS}. After clearing the alarm condition, the IO line discharges when IOdmpEn is activated by setting register 1, bit 3, which provides a sink current to the IO pin.

When $\overline{CS}$ is high and Horn Fault Test is disabled through register settings (default operation), pin 10 is the IO Out signal to the MCU used to signal a valid interconnect signal on the IO line.

3.7 Serial Interface Control

The RE46C305 devices are designed to interface with a Serial Peripheral Interface (SPI) port, available on many microcontrollers and supports Mode 0,0. To keep device pin count low, SDO and SCK are multiplexed with other pin functions. Table 2-2 describes the pin mapping and is based upon the register settings as well as the state of $\overline{CS}$.

All the digital input pins are Schmitt triggered to avoid system noise perturbations during communications.

Each serial interface communication starts with a $\overline{CS}$ falling edge and stops with the $\overline{CS}$ rising edge. Each serial interface communication is independent. When $\overline{CS}$ is logic high, SDO is in a high-impedance state, transitions on SCK and SDI have no effect. Any CS rising edge clears the communication and resets the serial digital interface. If $\overline{CS}$ is at a logic low at power up, then $\overline{CS}$ must be driven high and then low before communications can start.

Refer to Figure 1-1 for detailed input and output timing. The serial interface provides complete control of the RE46C305 operation. Serial interface registers can be programmed with setup information for each of the functions and they can also control the operation of certain functions as well as power each function on or off with an enable bit.

3.8 Serial Interface Registers

The RE46C305 interface has a simple command structure. Every command is either a WRITE command to a register or a READ command from a register. The READ command is intended to verify the WRITE command results.

Each register command consists of two bytes. The upper byte is the register address which includes the READ WRITE bit and the lower byte is the register data. Alternatively, the data for a byte address can be readout when a second 16-bit clock cycle is completed. The RE46C305 device includes four user registers defined in the Register 3-1. Unused data bits read back as 0. Data bits for nonexistent registers read back as 1's.

REGISTER 3-1: REGISTER CONFIGURATION AND CALIBRATION SETTINGS

Register 4:0 Address Byte							
R/W	U	U	U	U	R/W	R/W	R/W
RW	—	—	—	—	AD2	AD1	AD0
bit 15							bit 8

Register 0 Data Byte							**Setup**
U	U	U	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	IOinSel	FDDSel	SSDis	VPOSISel	VPOSVSel
bit 7							bit 0

Register 1 Data Byte							**Enables**
U	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RefEn	HFTEn	HRNEn	IOdmpEn	IOsrcEn	LEDEn	BEn
bit 7							bit 0

Register 2 Data Byte							**Horn Fault Test Codes**
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HTB7	HTB6	HTB5	HTB4	HTB3	HTB2	HTB1	HTB0
bit 7							bit 0

Register 3 Data Byte							**Horn Test Options**
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BstOvrLd	iBstOvrLd	VposBuf	HFT3T	HTEnOut	HTpdSel	HTrefSel	HTsrcSel
bit 7							bit 0

Register 4 Data Byte							**Open**
U	U	U	U	U	U	U	U
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as indeterminate	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	X = Bit is unknown

Register#	Bit#	POR Value	Description
4:0	11:8	—	**AD[3:0] Address Select** 0000 = Register 0: Setup 0001 = Register 1: Enables 0010 = Register 2: Horn Fault Test Code 0011 = Register 3: Horn Test Options 0100 = Register 4: Open XXXX = Don't Care Except
4:0	14:12	—	Not Used
4:0	15		**RW: Read / Write Select** 1 = Read contents of the specified register 0 = Write data to the specified register
Register 0 - Setup			
0	0	0	**VPOSVSel: V_{POS} Voltage Select** 1 = 11.5V 0 = 10.0V

0	1	0	**VPOSISel - V_{POS} Peak Current Select** 1 = 800 mA 0 = 500 mA
0	2	0	**SSDis - Soft Start Control** 1 = Immediate 0 = Soft start
0	3	0	**FDDSel - FEED/Direct Drive Select** 1 = FDBAK 0 = iDIRDRV
0	4	0	**IOinSel - IO Input Trip Select** 1 = 2.2V Maximum trip point 0 = 1.4V Maximum trip point
0	7:5	x	Not Used
Register 1 - Enables			
1	0	0	**BEn - Boost Operation Enable** 1 = Boost Enable 0 = Boost Disable
1	1	0	**LEDEn - LED Enable** 1 = Enable 0 = Disable
1	2	0	**IOsrcEn - IO Source Enable** 1 = IO Source Enable 0 = IO Source Disable
1	3	0	**IOdmpEn - IO Dump Enable** 1 = IO Dump Enable 0 = IO Dump Disable
1	4	0	**HRNEn - Horn Enable** 1 = Enable 0 = Disable
1	5	0	**HFTEn - Horn Fault Test Enable** 1 = Enable 0 = Disable
1	6	0	**RefEn - References Enable** 1 = Enable 0 = Disable
1	7		Not Used
Register 2 - Horn Fault Test Code			
2	7:0	0	Refer to **Section 3.4** for applicable codes
Register 3 - Horn Test Options & TestOut Options			
3	0	0	**HTsrcSel - Vsrc** 1 = 1V 0 = 0.9V
3	1	0	**HtRefSel - Vtrip selection** 1 = 0.35V 0 = 0.2V
3	2	0	**HtPdSel - Select Meas. pull down** 1 = 30 nA 0 = 20 nA
3	3	0	**HtEnOut - Enable Test Out → HT Meas. (analog) & SDO → HTStat** 1 = Enable horn test outputs 0 = Normal Outputs, SDO = HTSet
3	4	0	**HFT3T - 3/2 Terminal Horn Test Selection** 1 = Three-terminal 0 = Two-Terminal

3	5	0	**VposBuf - Enable Test Out → V_{POS} ÷ 10 (analog)** 1 = TESTOUT = VPOS ÷ 10 0 = TESTOUT = Normal (POR)
3	6	0	**iBstOvrLd - Serial Data Out → MaxLD** 1 = Enable - SDO as MaxLD interupt 0 = Disable - Normal SDO output
3	7	0	**BstOvrLd - Enable Test Out → MaxLD (digital)** 1 = Enable - MaxLD output on TESTOUT 0 = Disable - Normal TESTOUT (POR) output
Register 4 - Open			
4	7:0	0	Reserved

4.0 APPLICATION NOTES

4.1 Definitions and terms

MaxLD – The voltage increases when the boost converter is overloaded. Overload is defined as two consecutive boost cycles where regulation is not achieved, causing V_{POS} to remain below the minimum operating level. MaxLD is active during the boost startup ramp and is used to determine when the boost converter reaches regulation. This is available on TESTOUT or SDO, depending on the setup.

HTMeas - Analog horn fault test signal, the input to the horn fault comparator. Can be used for test and debug, either to drive the comparator or to observe the actual horn test response signal. This is available on TESTOUT.

HTStat – Unlatched output of horn fault comparator. This is available on TESTOUT or SDO, depending on the setup.

HTSet – The horn fault comparator output is latched on the falling edge of SCK. It is automatically presented on the HT TEST OUT pin. Any serial communication or edge of SCK clears the latch, meaning the first failure terminates the horn fault testing.

HTVsrc – An internal current limited source of 0.9V or 1.0V.

HTIsnk – Nominal current limit of 2 uA generated by HTVsrc.

HTIpd – Ability to control a pull-down resistor with a nominal value of 500k, which can be directed to either HB or HS.

HTdrv – Ability to connect an open-drain NMOS pull-down to either HB or HS.

HTMeasVT – Ability to connect an internal comparator to HB, HS, FEED or HBFB pins with selectable comparator reference of 0.2 or 0.35V.

HTMeasOut Ratio – The ratio of the analog voltage at TESTOUT to the selected signal voltage (HB, HS, HBFB, or FEED) during the Horn Fault Test. This is valid when HTMeas is selected for TESTOUT.

HTMPd – A selectable pull-down current of 20 nA or 30 nA to counter any weak parasitic leakages on the HB/HS/FEED/HBFB.

VPOSBuf – A divided V_{POS} with a nominal value of 1V, independent of the V_{POS} voltage selection, is available on TESTOUT.

LXpk – Measure of LX peak current based upon a transition of LX Current Sense Comparator (Vc2bb); typical values are 500 mA and 800 mA.

POR – Power on Reset in normal operation is available on the TESTOUT pin during power up.

4.2 Boost Converter

The boost converter in active mode draws LX current pulses greater than 800 mA when VPOSISel is set high, making it highly sensitive to series resistance. Key components contributing to this resistance include the inductor's DC resistance, the battery's internal resistance and the resistance in the connections between the inductor and the battery, the inductor and the LX pin, the inductor through the boost capacitor and the VSS pin to the battery. For proper functioning under full load at V_{DD} = 2V, the total resistance from the inductor and interconnects should not exceed 0.3Ω. The battery's internal resistance should be no more than 0.5 Ω. Additionally, a low ESR capacitor of 10 µF or more should be connected in parallel with the battery to smooth out the current draw during the boost converter's switching cycle. The Schottky diode and inductor should be rated for a maximum operating current of 1A or higher and the boost capacitor should have a low ESR.

There is an internal signal called MaxLD that reports the health of the boost converter. This signal can be output on either the TESTOUT pin or the SDO pin. When the boost is below regulation for two or more consecutive pulses, the selected output goes high.

This can be used as an interrupt to indicate a potential overload condition. When the signal is low, it indicates that the boost is in regulation, preventing the application of a load before it stabilizes.

The boost regulator supplies a nominal maximum current, as shown in Table 4-1, at a temperature of 85°C.

TABLE 4-1: VPOS NOMINAL MAX LOAD

V_{IN} (V)	I_{peak} (mA)	VposSel (V)	I_{load} (mA)
3	500	11.5	30
3	800	11.5	40
3	800	10.0	40

4.3 Horn Fault Testing

The Horn Fault Test feature can be conceptually viewed in Figure 4-1. During horn fault testing, the piezoelectric drivers are isolated by switches 1–4. The test codes, detailed in **Section 3.4** of this document, configure the appropriate control and connections for all switches, sources and measurement circuitry to stimulate and assess the connectivity of the piezoelectric horn disc.

To clarify, all fault conditions refer to the horn disc, not the pins of the RE46C305. This distinction is important when considering the feedback from the horn disc. In this document, FEED is the pin of RE46C305, while FEEDBACK refers to the horn disc node.

Note: In regards to using the TESTOUT signal, driving large capacitive loads leads to stability issues for voltage feedback operational amplifiers. As the load capacitance increases, the phase margin of the feedback loop decreases and the closed-loop bandwidth is reduced. This results in gain peaking in the frequency response, along with overshoot and ringing in the step response. A unity gain buffer (G = +1) is particularly sensitive to capacitive loads. When driving large capacitive loads with these operational amplifiers (e.g., > 50 pF at G = +1), adding a small series resistor at the output improves stability. This resistor helps to maintain the phase margin of the feedback loop by making the output load more resistive at higher frequencies.

The digital result of the horn fault test is available on HT TEST OUT (pin 10), while the analog result can be monitored on TESTOUT (pin 12). This allows adjustment of comparator trip points and sourcing supplies to accommodate variations in different piezoelectric horn discs.

The choice between digital (default) or analog output is controlled by register 3, bit 3 (HtEnOut). A high value enables the analog level response, which feeds into the comparator during the test pulse (HTENP) on pin 12 (TESTOUT). A low value provides the digital result of the fault test on pin 10 (HT TEST OUT), which can be sampled at the end of the test pulse. A high level indicates a pass, while a low level indicates a failure.

The first 3 bits of register 3 control these adjustments: HTsrcSel, HtRefSel, and HtPdSel. HTsrcSel selects a small voltage of either 0.9V or 1.0V, corresponding to a current-limited level used to stimulate the disc. HtRefSel adjusts the comparator reference trip point, allowing selection between 0.2V or 0.35V. HtPdSel modifies the pull-down currents (HTMPd) applied, with options of either 20 nA or 40 nA, to counter any weak parasitic leakages from the disc pins.

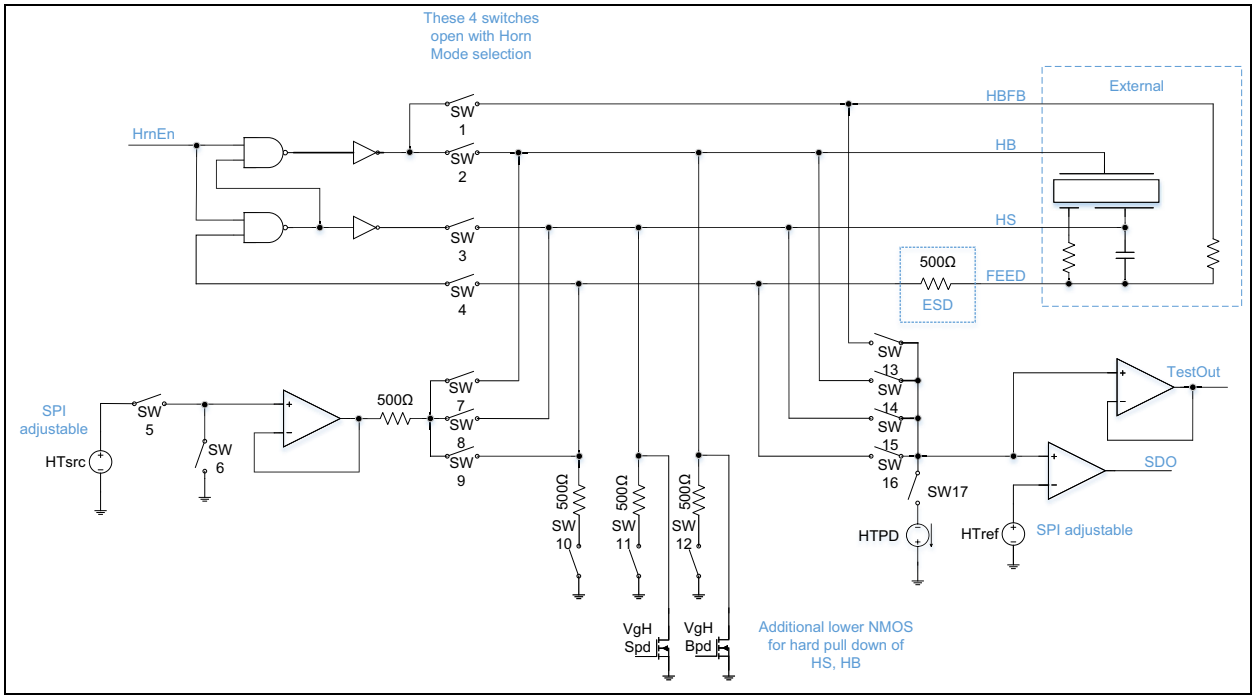
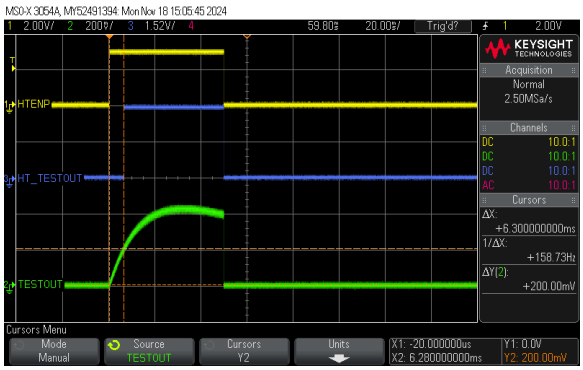


FIGURE 4-1: *Conceptual Schematic of the Horn Fault Test Feature.*

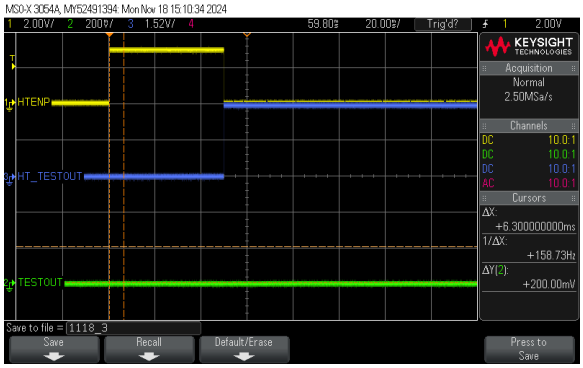
4.4 Plots

The following plots provide examples of both the analog and digital measurement results for a representative piezoelectric disc using each of the test codes. All measurements were taken using a three-terminal horn.



In the plot above, the RE46C305 is configured to output the analog level on TESTOUT (pin 12) by setting register 3, bit 3 (HtEnOut) to high. This corresponds to channel 2 (TESTOUT). The horizontal cursors are positioned at ground and the comparator trip point of 0.200V. As the analog level crosses this threshold, the vertical cursors show the activation of HT TEST OUT (pin 10) on channel 3. If register 3, bit 3 had been left at its default low, this pin would have output the digital result of the horn fault test. In digital mode, the test result is valid after the falling edge of the HTENP signal (channel 1).

Note: A logic high on HT TEST OUT indicates a passing test result. In digital mode, the TESTOUT signal is not output.



The following plots show a typical three-terminal horn (EAST – EFM-290ED) being exercised through each of the six test codes. There are no faults present in these plots, and both the analog and digital modes are demonstrated, with the test repeated for each mode.

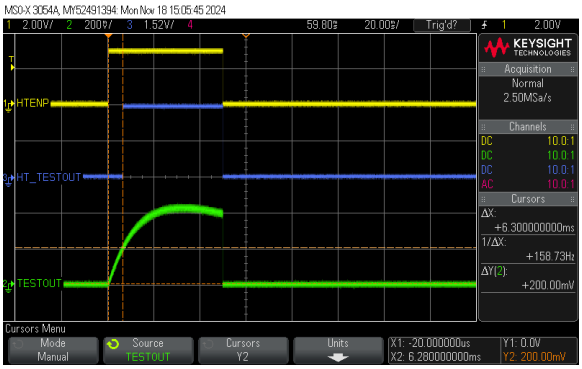


FIGURE 4-2: *Test 1, Code 75, Analog.*

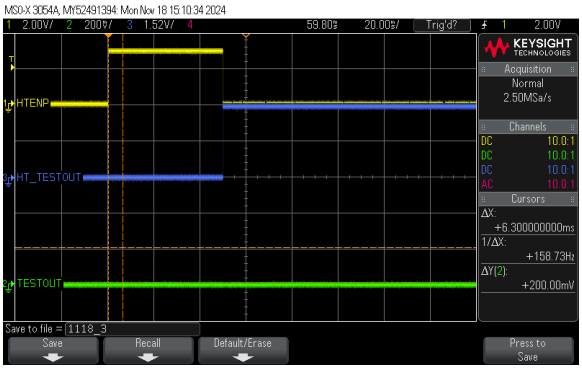


FIGURE 4-3: *Test 1, Code 75, Digital.*

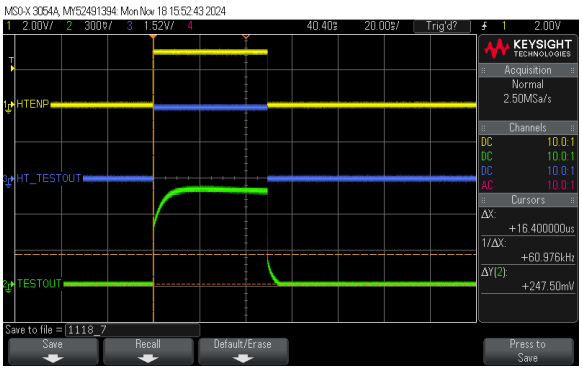


FIGURE 4-4: *Test 2, Code 5B, Analog.*

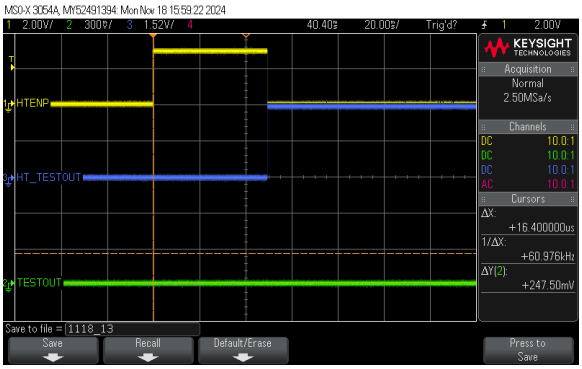


FIGURE 4-5: *Test 2, Code 5B, Digital.*

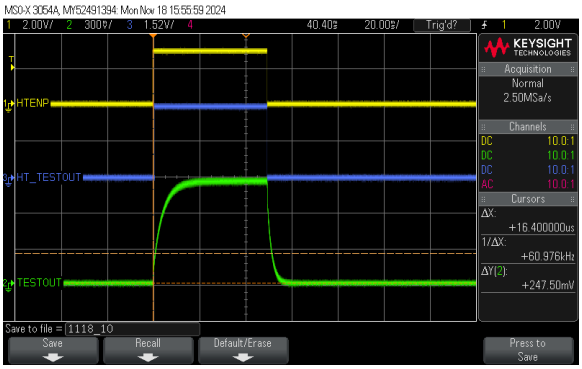


FIGURE 4-8: *Test 4, Code E1, Analog.*

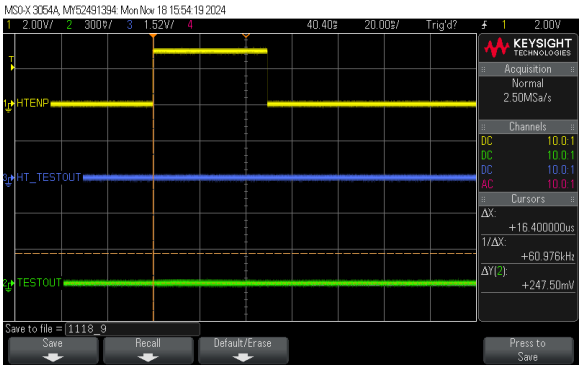


FIGURE 4-6: *Test 3, Code 74, Analog.*

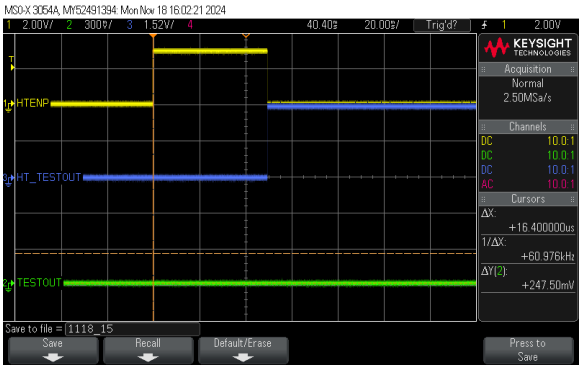


FIGURE 4-9: *Test 4, Code E1, Digital.*

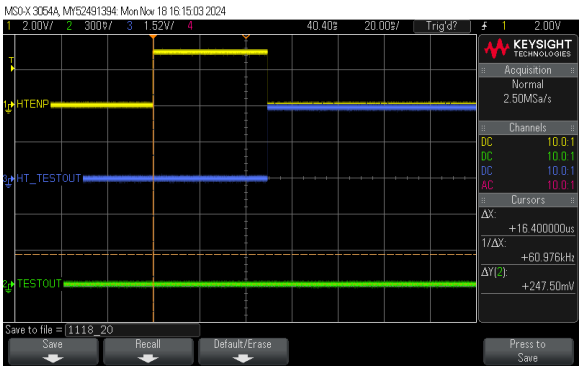


FIGURE 4-7: *Test 3, Code 74, Digital.*

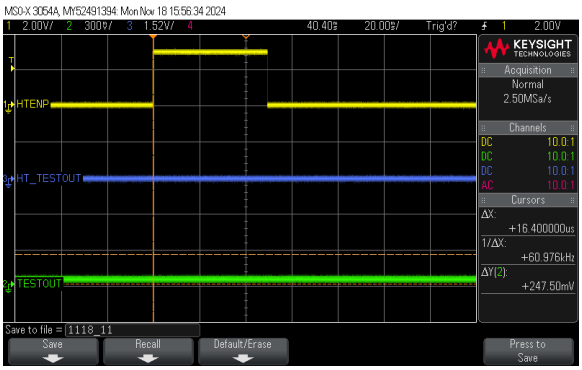


FIGURE 4-10: *Test 5, Code 4A, Analog.*

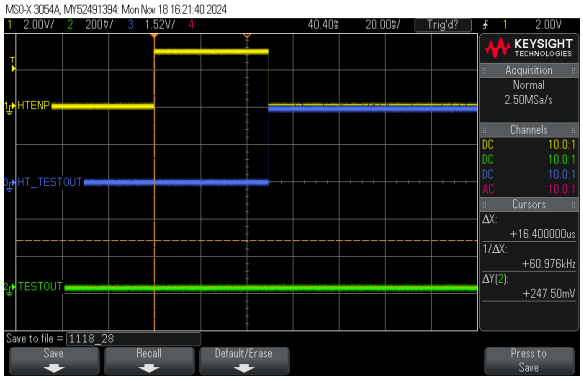


FIGURE 4-11: *Test 5, Code 4A, Digital.*

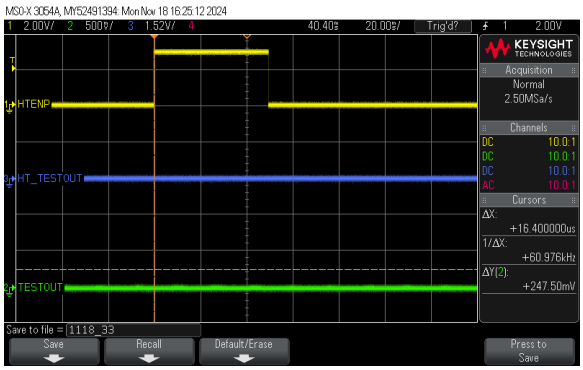


FIGURE 4-12: *Test 6, Code 5A, Analog.*

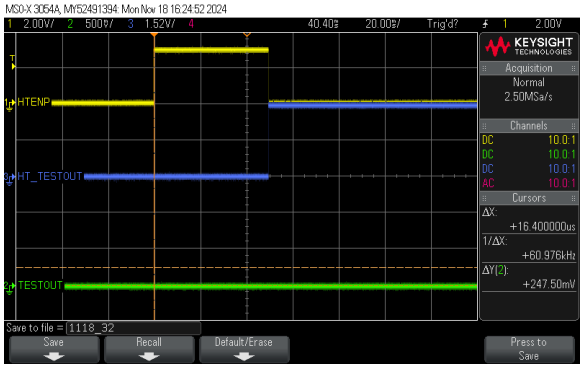


FIGURE 4-13: *Test 6, Code 5A, Digital.*

The digital response in all the above plots shows that no faults were detected in any of the tests, which makes sense given that this is a working horn configuration. However, in the analog results, the user should understand that the fault testing checks for various potential fault conditions, such as opens, shorts to other disc pins, shorts to power or shorts to ground. As a result, the analog response shows a variety of levels between the power rails, depending on the specific fault being tested.

As an example, this is a case of a short between HB and FEEDBACK.

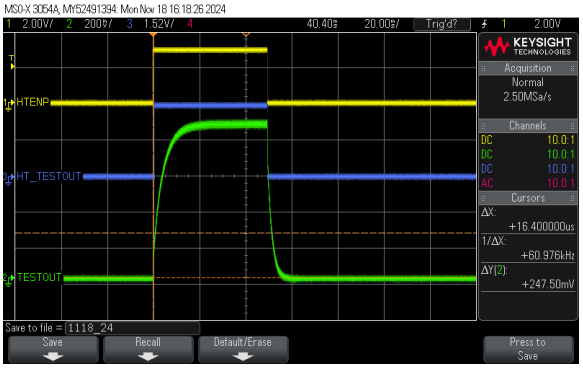


FIGURE 4-14: *Test 4, Code E1, Analog, No Fault.*

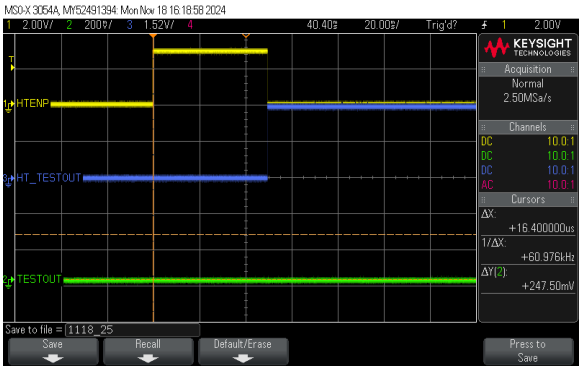


FIGURE 4-15: *Test 4, Code E1, Digital, No Fault.*

Next, the HB is shorted to the FEEDBACK. It is important to note that all faults are related to the piezoelectric disc and not the RE46C305 device.

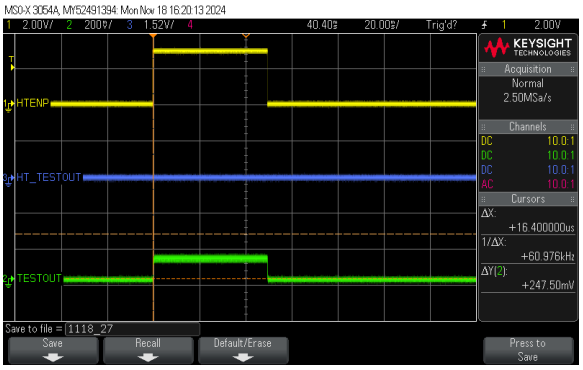


FIGURE 4-16: *Test 4, Code E1, Analog, HB shorted to FEEDBACK.*

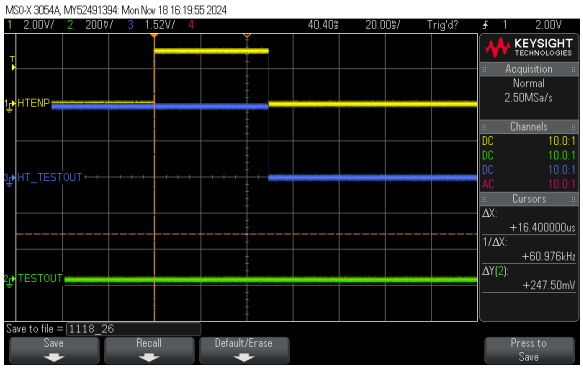


FIGURE 4-17: *Test 4, Code E1, Digital, HB shorted to FEEDBACK.*

What can be observed in the faulted analog signal is the short has severely attenuated the TESTOUT signal level, especially as compared to the no fault analog signal and it has not exceeded the comparator threshold of 0.20V.

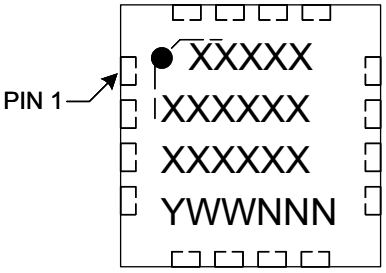
Equally observable is the digital low at the conclusion of the HTENP falling edge indication of a failure of this test.

Microchip has evaluated a variety of standard two- and three-terminal horns for proper operation, but this is not an exhaustive list. If a particular fault test does not provide the desired results, experimenting with the mentioned register while monitoring the analog signal into the comparator through the unity gain buffer may offer valuable design guidance and insights.

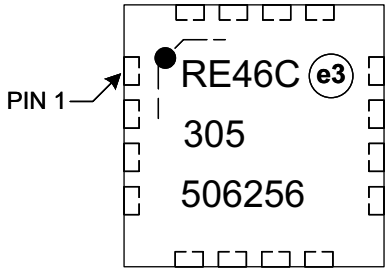
5.0 PACKAGE INFORMATION

5.1 Package Marking Information

16-Lead VQFN
4 x 4 x 0.9 mm Body



Example:



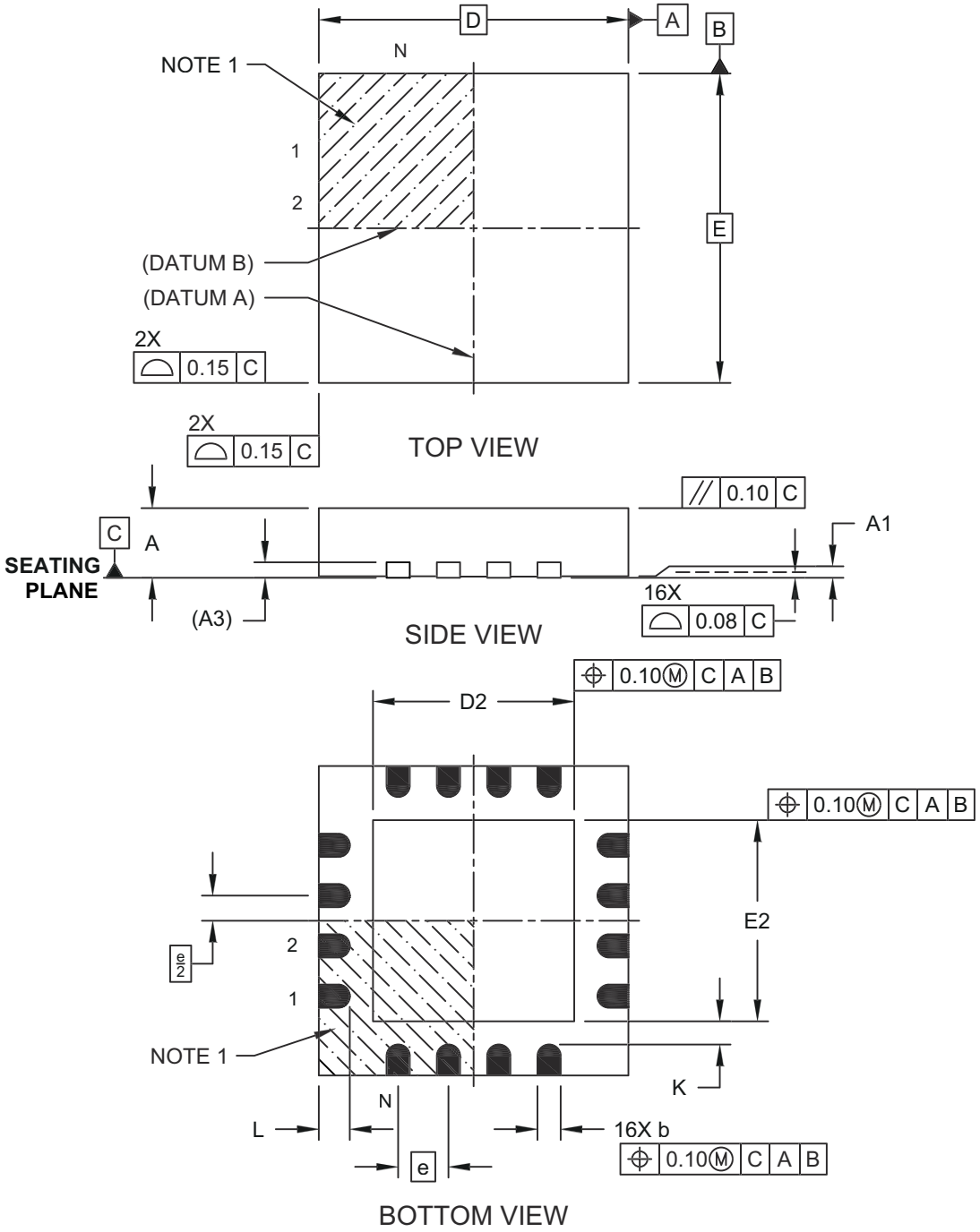
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5.2 Package Drawings

16-Lead Very-Thin Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [VQFN] With 2.60x2.60 Exposed Pad

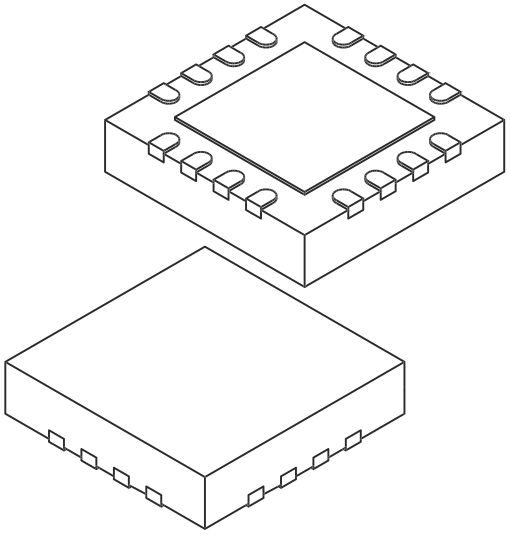
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00127-ML Rev E Sheet 1 of 2

16-Lead Very-Thin Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [VQFN] With 2.60x2.60 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

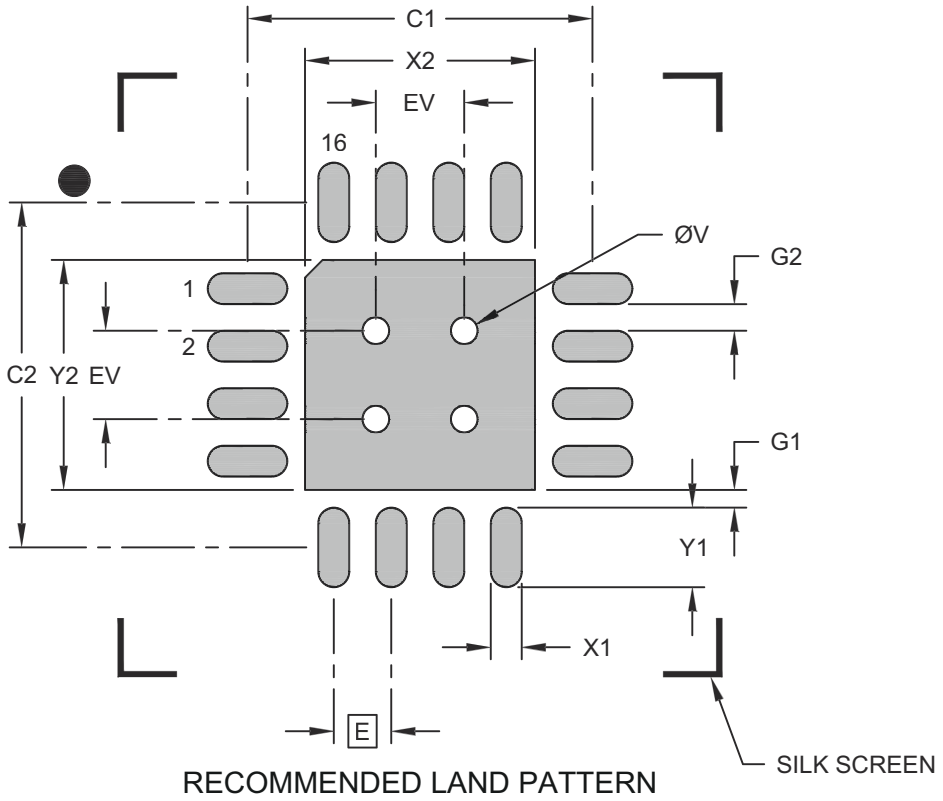
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-00127-ML Rev E Sheet 2 of 2

16-Lead Very-Thin Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [VQFN] With 2.60x2.60 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Center Pad Width	X2			2.60
Center Pad Length	Y2			2.60
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		3.90	
Contact Pad Width (X16)	X1			0.35
Contact Pad Length (X16)	Y1			0.90
Contact Pad to Center Pad (X16)	G1	0.20		
Contact Pad to Contact Pad (X12)	G2	0.30		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, pleease refer to current industry standard IPC-7093.

Microchip Technology Drawing C04-02127-ML Rev E

APPENDIX A: REVISION HISTORY

Revision A (March 2025)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	Q16	[X](1)
Device	Package	Tape and Reel

Device:	RE46C305	= Piezoelectric Horn Driver
Package:	Q16	= 16-Lead VQFN, 4x4x0.9 mm Body
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel(1)

Examples:

a) RE46C305Q16 = Piezoelectric Horn Driver, 16-Lead VQFN

b) RE46C305Q16T = Piezoelectric Horn Driver, 16-Lead VQFN, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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