Driving mSiC™ MOSFETs

AN4616

Introduction

This application note describes how to select gate driving voltages for Microchip's mSiC MOSFET products, along with related device performance and behavior.

Specifying Gate Drive Voltages for SiC MOSFETs

The manner in which gate drive voltages are specified on data sheets varies by manufacturer, but the majority of them use something similar to Table 1. The following is a list of the definitions of some terms:

- V_{GS} is the applied voltage between the MOSFET's gate and source terminals
- V_{GSon} is the Steady-state V_{GS} applied to turn the MOSFET on
- V_{GSoff} is the Steady-state V_{GS} applied to turn the MOSFET off
- V_{GSmax} is the manufacturer's maximum allowed Steady-state V_{GS}, shown for both negative and positive extremes
- $V_{GS,OP}$ is the manufacturer's recommended Steady-state values for V_{GSon} and V_{GSoff}

Some data sheets do not specify V_{GSon} and V_{GSoff}. Similarly to silicon MOSFETs, different applications require different optimal values.

The following table lists the gate-source voltage specification.

Table 1. Gate-Source Voltage Specification

Characteristic	Symbol	Conditions	Value	Unit
Gate-source voltage	V_{GSmax}	Absolute maximum DC values	−10 to 23	V
	$V_{GS,OP}$	Recommended DC operating values	−5 to 20	

Microchip Recommendations

For optimal device performance and system stability, mSiC MOSFETs are best driven using V_{GSon} = +20V and V_{GSoff} = −5V. The mSiC MOSFETs continue to perform well at lower absolute values of V_{GSon} and V_{GSoff}, but the additional losses associated with sub-optimal drive conditions should be analyzed and understood, as with any design. Thus, the reasoning behind optimal V_{GSon} and V_{GSoff} differs, and the expected tradeoffs for each case are described in the following sections.

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1. On State Gate Drive Voltage (V_{GSon})

Driving SiC MOSFETs with a lower V_{GSon} has the following effects:

- Increased On-state resistance, resulting in higher conduction loss
- Reduced peak (saturation) current capability
- Longer Short Circuit Withstand Time (SCWT)
- Extended gate oxide lifetime
- Increased switching loss under the same gate resistance

1.1 On State Resistance (R_{DSon})

The following four figures show how the normalized R_{DSon} (normalized to R_{DSon} at 25 °C and 20V gate voltage) increases with junction temperature (T_J) under different gate voltages. The figures show the data for Microchip's largest mSiC MOSFET die at each of four voltage classes: 700V, 15 mΩ; 1200V, 17 mΩ; 1700V, 35 mΩ; and 3.3 kV, 25 mΩ.

The following are some general observations:

- The increase of R_{DSon} with temperature for SiC MOSFETs is much lower than that of silicon MOSFETs (from 25 °C–175 °C, 50% increase for 1200V SiC MOSFETs and greater than 150% increase for 1200V Si MOSFETs)
- At V_{GSon} = 18V, R_{DSon} shows a minor shift, which gets even smaller at higher T_J
- At V_{GSon} = 15V, the increase in R_{DSon} is more substantial, particularly at lower T_J

Figure 1-1. Normalized R_{DSon} Vs. Temperature and V_{GS} (I_D: 40A) for 700V Family Devices

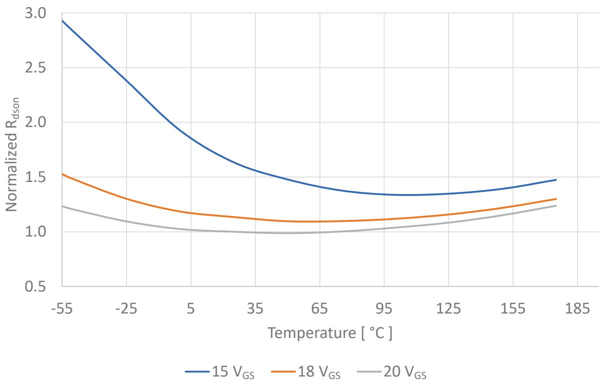


Figure 1-2. Normalized R_{DSon} Vs. Temperature and V_{GS} (I_D: 40A) for 1200V Family Devices

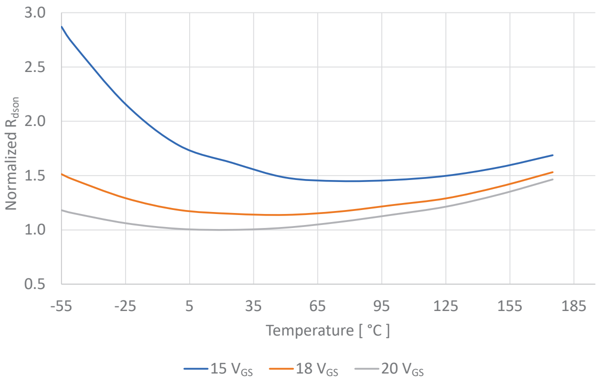


Figure 1-3. Normalized R_{DSon} Vs. Temperature and V_{GS} (I_D: 30A) for 1700V Family Devices

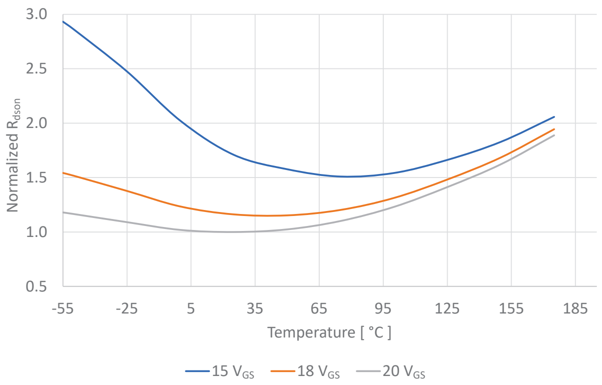
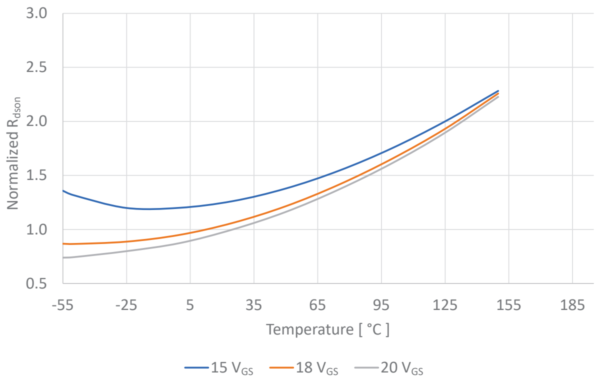


Figure 1-4. Normalized R_{DSon} Vs. Temperature and V_{GS} (I_D: 40A) for 3.3 kV Family Devices



1.2 Designing for V_{GSon} < 20V

Due to SiC's wide band gap, a higher electric field is required to invert the semiconductor of a MOS-gated transistor than is required for silicon. The electric field can be increased either by raising the applied V_{GSon} or by reducing the thickness of the gate oxide. Raising V_{GSon} requires a new gate driver design, while reducing the oxide thickness could make the device more susceptible to failure. A third way to get more current is to increase die size, but this increases the cost. A new gate driver design is clearly the best technical and commercial choice, but some compromises are made if the ideal V_{GSon} = 20V is impossible to achieve.

1.2.1 Effect on R_{DSon}

When driving a SiC MOSFET at lower values of V_{GSon}, designers should analyze how R_{DSon} changes across the junction temperature range of interest. If the R_{DSon} across relevant T_J is consistently within a close range of the R_{DSon} at V_{GSon} = 20V, the final design can accommodate these small differences and be extremely robust. For mSiC MOSFETs, production measurement of R_{DSon} shows V_{GSon} = 20V is an excellent predictor of R_{DSon} at V_{GSon} = 18V; in the case of a 1200V SiC MOSFET at T_J = 25 °C, a V_{GS} drive of 18V results in 11% higher R_{DSon}. However, at T_J = 175 °C, the penalty is only 2%.

In contrast, the comparison of R_{DSon} at V_{GSon} = 20V and V_{GSon} = 15V requires careful consideration. The variance is approximately four times higher for V_{GSon} = 15V and dependent upon device Threshold Voltage ($V_{GS(th)}$). For this reason, Microchip does not recommend driving mSiC MOSFETs of type MSCxxxSMAxxx at V_{GSon} = 15V. If they must be driven with 15V, a sufficient design margin for R_{DSon} should be considered. Contact your local Microchip sales office for support.

1.2.2 Parallel-Connected SiC MOSFETs

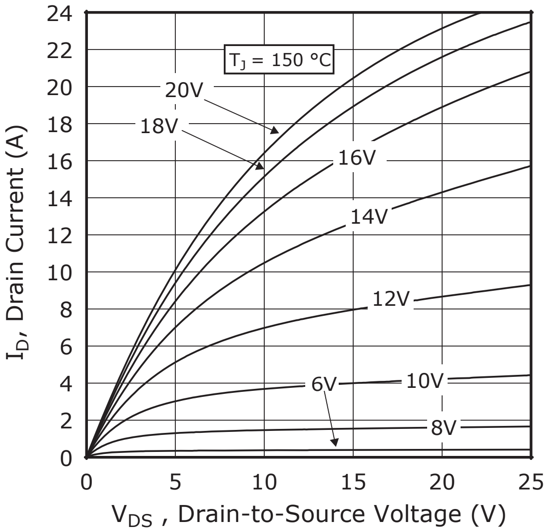
There is another point to be made about parallel-connected SiC MOSFETs and $V_{GSon} < 20V$. One can observe from the charts that the temperature coefficient of R_{DSon} is not positive across the entire range of relevant T_J. In an extreme example, consider the 700V SiC MOSFET at $V_{GSon} = 15V$. This gate drive situation results in a SiC MOSFET with a negative temperature coefficient up to T_J = 80 °C–100 °C. Ensuring that paralleled devices will evenly share current is a risk against which the design should be safeguarded. However, as stated in the previous paragraphs, using $V_{GSon} = 18V$ is the simplest solution and is well-suited for most applications.

1.2.3 Peak Current Capability

When driving with a lower V_{GSon}, the MOSFET channel is not fully enhanced, and the maximum current is reduced.

The following figure shows the I-V curve of MSC360SMA120B under different driving voltages at T_J = 150 °C.

Figure 1-5. I-V Curve of MSC360SMA120B Under Different Driving Voltages at T_J = 150 °C



Note the small separation between the R_{DSon} curves at V_{GSon} = 20V and V_{GSon} = 18V, and compare this to the bigger differences in R_{DSon} as V_{GSon} drops increasingly below 16V. The following are some important considerations:

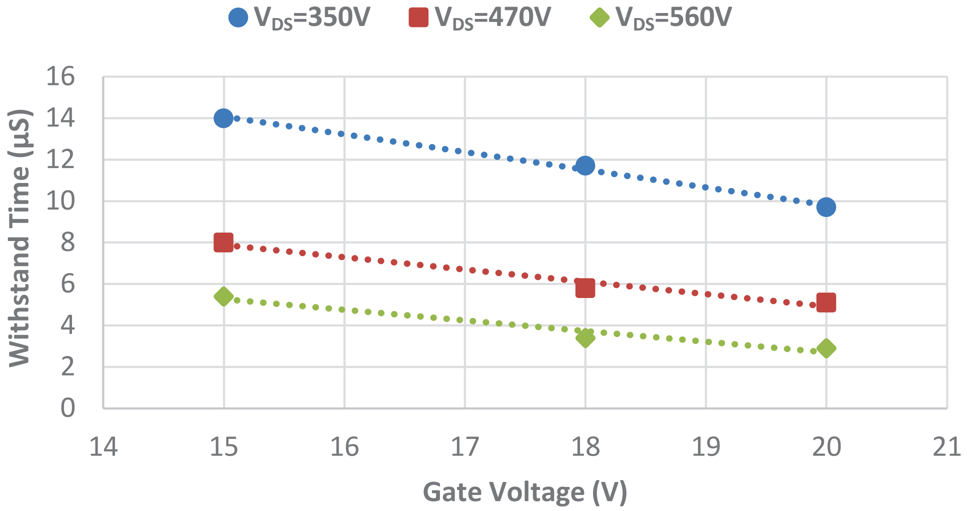
- An over-current protection scheme based on the maximum current may fail to trigger. Designers must account for the higher variability of R_{DSon} at lower V_{GSon}
- The small-signal transconductance (g_m) is higher at lower V_{GSon}. Because V_{GS} may be in the middle range in the presence of a high drain-source voltage, this effect can cause switching instability, resulting in device failure
  Note: The peak short circuit current is governed by the precise value and duration of V_{GSon}. For more information, see the following section.

1.2.4 Short Circuit Withstand Time

When driving with lower V_{GSon}, the maximum current will be lower under short circuit conditions, which can lead to a longer SCWT.

The following figure shows the SCWT in relation to gate and drain voltages for MSC035SMA070B measured with V_{DS} = 350V, 470V, and 560V and V_{GSon} = 20V, 18V, and 15V. As shown, the drain voltage is the most significant factor affecting SCWT, followed by V_{GS}.

Figure 1-6. SCWT of MSC035SMA070B



In applications where short circuits are possible, the following considerations must be made:

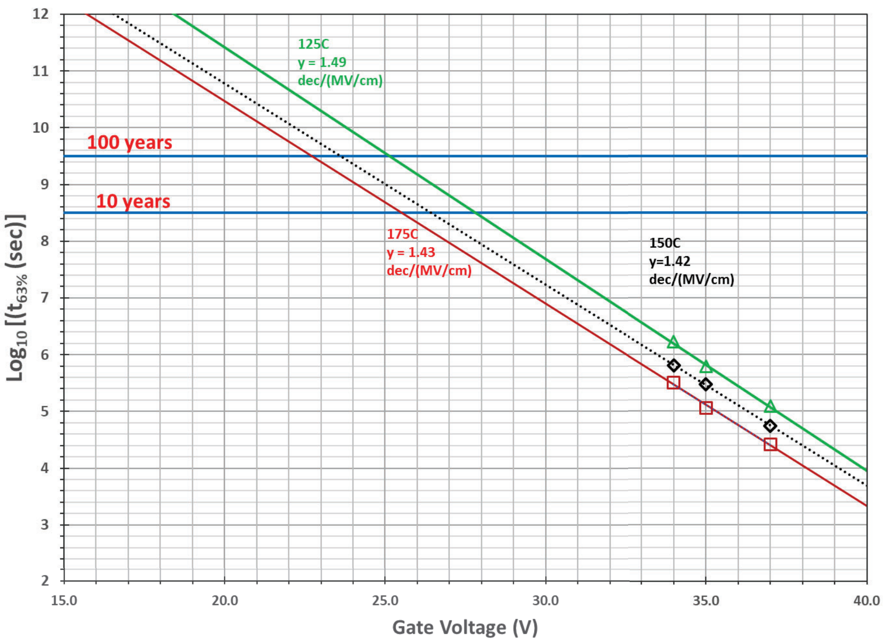
- The SCWT specified in the data sheet is the typical time to failure, as defined by the device no longer exhibiting proper electrical function. In reality, the actual failure occurs after the device is switched off, when the latent heat generated causes irreversible damage. In other words, the delay does not occur when the measurement indicates it does. Because of the delay, the SCWT in the data sheet can only be seen as a typical number
- A more reasonable requirement would be that a specified number of devices are still operational after a specified number of short circuit events
- SCWT can be extended by increasing the device size or using multiple devices designed to drive at a reduced current level with source degeneration

For additional guidance and insight, contact your local Microchip sales team.

1.3 Projected Lifetime

The following figure shows that every 2.5V increase in V_{GSon} reduces the projected lifetime of the gate oxide by an order of magnitude. This relationship applies over a wide range. It is a wear out mechanism caused by accumulated damage over time.

Figure 1-7. Projected Device Life Time Under Different Gate Voltage



The lifetime of the gate oxide is mostly determined by the Steady state gate ON drive voltage. The +23V maximum rating on the gate is a recommendation for Steady state gate voltage based on the projected lifetime of the device. Transient overshoots in V_{GSon} do not materially affect the device lifetime because of their brief duration. As an example, assume a rectangular overshoot for 20 ns at 25V with a nominal gate voltage of 20V. According to the oxide lifetime graph, the rate of degradation of the oxide during the pulse is 80 times higher. However, with a switching frequency of 100 kHz, the duty factor is 20 ns × 100 kHz = 0.002. The relative stress, then, is only 80 × 0.002 = 16%.

It should be noted that transient V_{GS} is not observable at the package pins. The gate and source lead inductances make it difficult to measure the actual V_{GS} overshoot. Due to the high capacitance of the gate, the gate drive is normally over-dampened, and overshoot is rarely a problem. This is easiest to determine in simulations.

1.4 Summary of V_{GSon}

Microchip’s mSiC MOSFETs can operate at +18V drive voltage with little loss in performance compared with the recommended +20V drive voltage. As shown in the preceding graphs, the increase in R_{DSon} is much larger at 25 °C than at 100 °C–150 °C. If the die is hot, a system is generally penalized less by conduction loss than would be implied by the difference at 25 °C. While the switching losses may be slightly higher under the same gate resistance and the saturation current will be lower, the positive tradeoff is a longer SCWT.

Operation at V_{GSon} < 18V gate drive comes with elements of risk and should only be used if there is sufficient margin in R_{DSon}. Current sharing between paralleled devices can be problematic at colder junction temperatures. If V_{GSon} < 18V is needed, contact your Microchip team for design support.

2. Off State Driving Voltage (V_{GSoff})

Microchip’s mSiC MOSFETs are normally-off power transistors. It is not necessary to have a negative V_{GSoff} to keep the switch off during Steady state. It is instead used to reduce switching loss and improve switching stability.

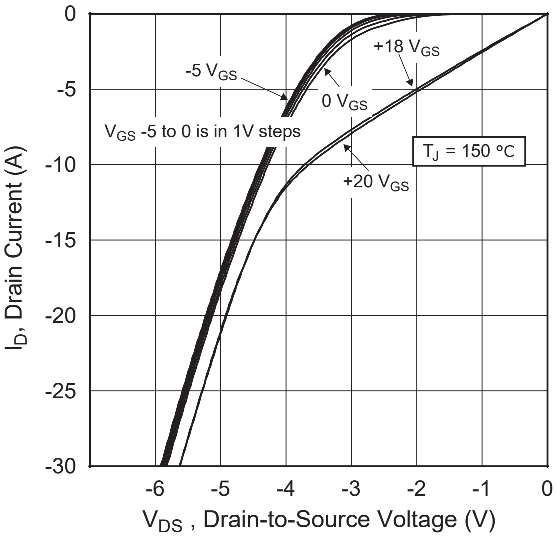
Driving SiC MOSFETs with a negative V_{GSoff} has the following effects:

- The presence of source inductance can slow the device turn-off process. A negative V_{GSoff} is used to overcome this effect
- A negative V_{GSoff} provides more margin to avoid false turn-on (also called shoot-through or cross-conduction) during switching transients
- A negative V_{GSoff} has been used for decades with silicon IGBTs. Negative gate drive is not unique to SiC
- More complex modules with distributed transistors need a higher (more negative) V_{GSoff} to avoid instability. Single transistor discrete designs can get by with very little negative V_{GSoff}

2.1 Third Quadrant Conduction Performance

Unlike a silicon IGBT, SiC MOSFETs can conduct current in both directions. The following figure shows the third quadrant performance of Microchip’s MSC360SMA120B; simply put, this is the drain current when the drain voltage is reversed. If the MOSFET's channel is turned off, the body diode carries reverse drain current. When $V_{GSoff} = -5V$, all current flows through the body diode. As V_{GS} increases, the channel begins to form but maintains a substantial voltage drop even at $V_{GS} = 0V$, indicating that the body diode still carries most of the reverse current. Following the switching transient, the channel can be turned on to conduct the reverse current to further improve conduction losses in a technique known as synchronous rectification.

Figure 2-1. Third Quadrant I-V Curve of MSC360SMA120B



2.1.1 Body Diode Robustness

There are no restrictions on the use of the body diode in mSiC MOSFETs, but this is not true for all SiC MOSFET suppliers. Recent third-party measurements have shown that competitors’ devices demonstrate body diode degradation to varying severity: in some cases, conduction losses increase by 20% after 168 hours, while in others, conduction losses more than double in less than 10 hours. For more information on body diode reliability of commercial SiC Power MOSFETs, see 5. Reference. The degradation mechanism is called recombination-enhanced dislocation motion; the phenomenon is well understood and has been observed in other semiconductors, such as SiGe, CdS, and GaAs. The effects on SiC can be mitigated with specific device knowledge.

We recommend to use mSiC MOSFET body diodes with confidence. For any questions, contact your local Microchip sales office.

2.2 Switching Noise Immunity

If using V_{GSoff} = 0V for SiC MOSFETs in high-speed and hard switching applications, there are important precautions to consider. Before diving into these precautions, some discussion about threshold voltage and pinch-off voltage is warranted.

The following table is from the datasheet of Microchip's 1200V, 80 mΩ mSiC MOSFET in the TO-247 package. Due to industry convention, the Nominal Threshold Voltage (V_{th}) is measured under the conditions of $V_{GS} = V_{DS}$, T_J = 25 °C, and a drain current of only 1 mA. Because the drain current associated with V_{th} is so low, the more relevant parameter to use for designs is known as the Pinch-Off Voltage (V_p). The V_p is the value of V_{GS} that produces a given drain current at a specific V_{DS}.

Table 2-1. Gate-Source Threshold Voltage of MSC080SMA120B

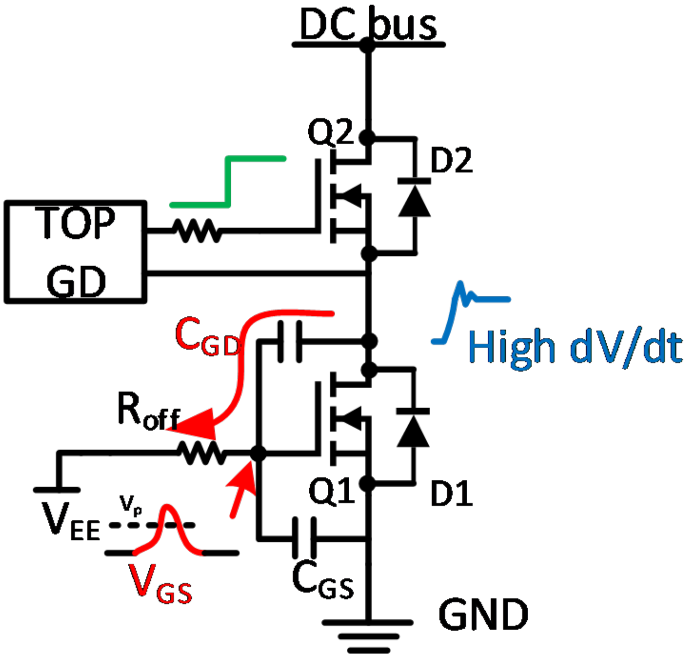
Symbol	Characteristic	Test conditions	Min.	Typ.	Max.	Unit
$V_{GS(th), 25\ °C}$	Gate-source threshold voltage at 25 °C	$V_{GS} = V_{DS}$, I_D = 1 mA, T_J = 25 °C	1.9	2.8	—	V

Accordingly, the value of V_p depends on V_{DS}, which varies depending on the MOSFET architecture. Trench MOSFETs have a much higher variation in V_p than planar MOSFETs. For this reason, to help ensure safe operation, trench MOSFETs are designed such that V_{th} at 25 °C is higher than needed. This means that planar MOSFETs offer greater design margin around V_p, which brings us at last to the key message on switching noise immunity.

The real margin for switching noise immunity should be set by V_p at the highest possible V_{DS} and the maximum allowed T_J. For our current family of mSiC MOSFETs, Microchip guarantees turn-off with V_{GS} = 0V at T_J = 175 °C. Using a negative V_{GSoff} provides more margin on V_p, which enhances switching stability and is the most certain way to prevent false turn-on.

The false turn-on in a half-bridge configuration is commonly induced by the Miller capacitance (Drain-to-Gate Capacitance (C_{GD})), as shown in the following figure. When top device Q2 is turned on, the high midpoint (phase leg output) dV/dt will induce current flow through C_{GD} that creates a voltage difference across Gate Resistor (R_{OFF}). This voltage difference will make the V_{GS} on bottom device Q1 higher than the Steady State Off Voltage (V_{EE}). This voltage can be high enough to turn Q1 on, but the margin on V_p prevents this false turn-on.

Figure 2-2. Switching Induced False Turn-On in a Half-Bridge Configuration



2.3 Summary of V_{GSoff}

Based on the previous discussion, Microchip does not recommend the use of V_{GSoff} = 0V. For single-ended topologies with no danger of shoot-through (for example, flyback, buck, or boost topologies), it is possible to use V_{GSoff} = 0V. If V_{GSoff} = 0V is absolutely necessary, proper gate-source loop design should be prioritized. Specifically, designers should try to minimize three factors in particular: parasitic drain-gate capacitance, gate-source loop inductance, and shared inductance between the gate-source loop and main current commutation loop.

3. Effect on the Device Switching Behavior

Driving the MOSFET at suboptimal V_{GSon} and V_{GSoff} voltages has clear implications on the device losses. With lower V_{GSon} and higher V_{GSoff}, the V_{GSon}- V_{GSoff} step will be smaller during the switching transient, and the charging and discharging current through the device gate will be lower under the same gate resistance, therefore switching speed will be lower. Meanwhile, lower V_{GSon} will increase the R_{DSon} of the switching device and also reduce the g_m of the switching device during the switching transient. Both will increase the discharge time of the MOSFET Output Capacitance (C_{OSS}) during the turn-on transient. Therefore, the device V_{DS} falls slower during turn-on as V_{GSon} decreases, especially at high current load conditions. Similarly, the device I_D rises slower with the decrease in V_{GSon}. In other words, the device experiences lower $\frac{d(V_{DS})}{dt}$ and $\frac{d(I_D)}{dt}$ as V_{GSon} is reduced. This argument is supported by the slew rate measurements of the MSC080SMA120B4 mSiC MOSFET during the turn-on switching event, as shown in the following figures.

Figure 3-1. d(V_{DS})/dt During Turn-On Slew Rates for MSC080SMA120B4 mSiC MOSFET (V_{DS} = 750V , R_G = 5Ω)

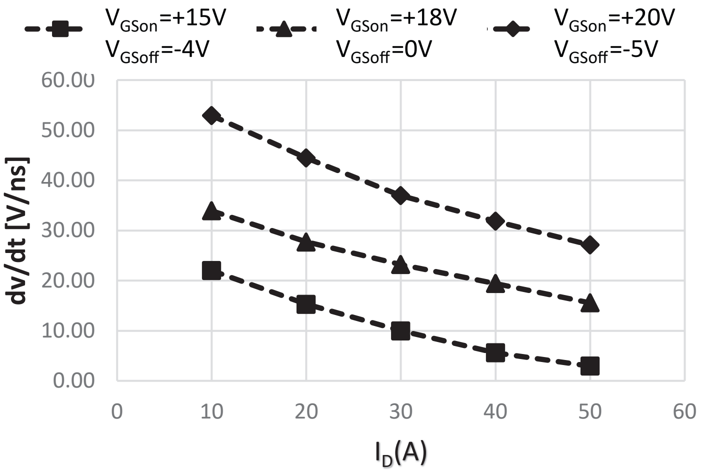
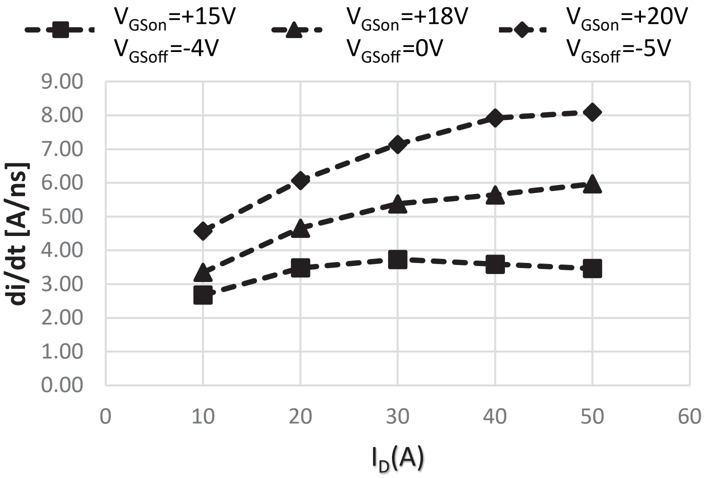


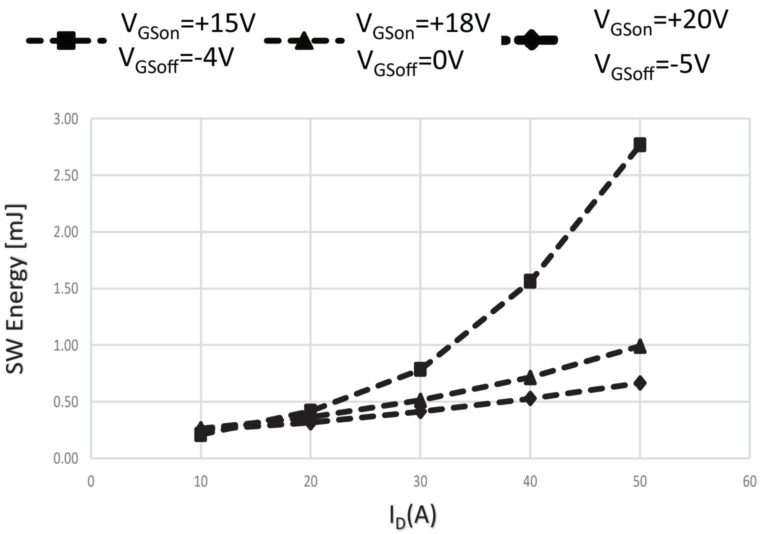
Figure 3-2. d(I_D)/dt During Turn-On Slew Rates for MSC080SMA120B4 mSiC MOSFET (V_{DS} = 750V , R_G = 5Ω)



In SiC MOSFETs, the turn-on switching loss often dominates the turn-off switching loss. Therefore, the total switching loss of the device is governed by the turn-on switching loss. Accordingly, as turn-on slew rates change significantly with different V_{GS}, it is expected that the total switching loss of the device also changes significantly.

The following figure shows the total switching losses of MSC080SMA120B4 mSiC MOSFET at different V_{GSon}.

Figure 3-3. Total Switching Loss of MSC080SMA120B4 mSiC MOSFET at Different V_{GSon} (V_{DS} = 750V , R_G = 5Ω)



The total switching loss increases with the decrease in V_{GSon} shown for the MSC080SMA120B4 mSiC MOSFET. As can be seen at I_D = 50A, a V_{GS} change from +20V/-5V to +18V/0V leads to about a 48% increase in total switching loss. While the total switching loss is suboptimal at V_{GSon} = +18V/0V, the switching loss increase is still manageable in most designs with a proper cooling system. Therefore, the use of V_{GSon} = +18V is still an acceptable choice for loss management, the V_{GSoff} = 0V could bring the concern of a false turn-on if the layout of the circuit is not optimized . On the other hand, for the same I_D = 50A, a V_{GS} change from +20V/-5V to +15V/-4V leads to about 313% increase in the total switching loss, which is unacceptable for most designs. If V_{GSon} < 18V is needed, contact your Microchip team for design support.

4. Key Takeaways

This application note provides guidance on mSiC MOSFET gate-source voltage specifications and design considerations for making the most effective gate driver circuit. The following are key takeaways:

- For the best possible switching and conduction performance, we recommend driving with V_{GSon} = +20V and V_{GSoff} = −5V
- It is permissible to deviate from these recommendations. mSiC MOSFETs can operate at +18V with slight reductions in current capability and turn-on efficiency, but come with the benefit of a longer SCWT
- Driving current-generation mSiC MOSFETs using V_{GSon} = 15V is not recommended. If this situation cannot be avoided, contact Microchip for design assistance
- Microchip guarantees turn-off with V_{GS} = 0V at T_J = 175 °C. However, using a negative V_{GSoff} provides a greater margin around V_p, which enhances switching stability and is the most certain way to prevent false turn-on

5. Reference Documents

The following document is referred in this application note:

- *M. Kang et al., "Body Diode Reliability of Commercial SiC Power MOSFETs," 2019 IEEE® 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2019, pp. 416-419*

6. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
B	08/2023	Added 3. Effect on the Device Switching Behavior.
A	04/2022	Initial revision

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ISBN: 978-1-6683-3035-7

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