

Description

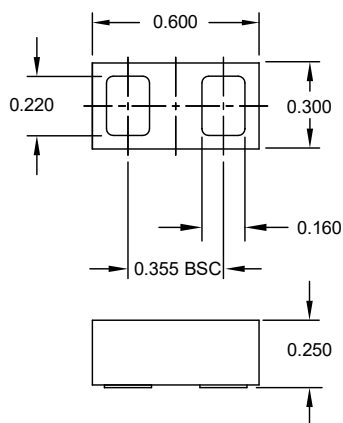
RClamp2461ZC is specifically designed to protect sensitive electronics from damage or latch-up due to ESD and EOS. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp2461ZC is in a DFN 0.60 x 0.30 x 0.25mm 2-Lead package. Leads are finished with lead-free NiAu. Each device will protect one high-speed data line operating up to 24V. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of working voltage, low dynamic resistance, and low capacitance makes this device ideal for use on NFC antenna circuits, RF signal lines, and FM antennas in portable devices.

Applications

- Near Field Communication (NFC) lines
- RF signal lines
- FM Antenna

Package Dimension



Nominal Dimensions in mm

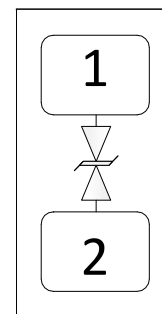
Features

- High ESD withstand Voltage
 - IEC 61000-4-2 (ESD): $\pm 10\text{kV}$ (Contact), $\pm 15\text{kV}$ (Air)
 - IEC 61000-4-5 (Lightning): 4A ($t_p = 8/20\mu\text{s}$)
- Ultra-small package
- Protects one high speed data line
- Working voltage: $\pm 24\text{V}$
- Low ESD clamping voltage
- Low capacitance: 0.27pF maximum
- Low dynamic resistance: 0.24Ω typical
- Solid-state silicon-avalanche technology

Mechanical Characteristics

- Package: DFN 0.60 x 0.30 x 0.25mm 2-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: Pb-Free
- Marking: Marking Code
- Packaging: Tape and Reel

Schematic & Pin Configuration



DFN 0.60 x 0.30 x 0.25mm 2-Lead (Bottom View)

Absolute Maximum Rating

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PK}	20	W
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V_{ESD}	± 10	kV
ESD per IEC 61000-4-2 (Air) ⁽¹⁾		± 15	
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

T=25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage	V_{RWM}				24	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1\mu A$	24.3	27	30	V
Reverse Leakage Current	I_R	$V_{RWM} = 24V$		<1	50	nA
Clamping Voltage ⁽²⁾	V_C	$t_p = 1.2/50\mu s$ (Voltage), 8/20μs (Current) Combination Waveform, $R_s = 12\Omega$	$I_{PP} = 1A$	2.5	3.5	V
				$I_{PP} = 4A$	3.5	
ESD Clamping Voltage ⁽³⁾	V_C	$t_p = 0.2/100ns$ (TLP)	$I_{TLP} = 4A$	3.4		V
		$t_p = 0.2/100ns$ (TLP)	$I_{TLP} = 16A$	6.3		
Dynamic Resistance ^{(3),(4)}	R_{DYN}	$t_p = 0.2/100ns$ (TLP)		0.24		Ω
Junction Capacitance	C_j	$V_R = 0V, f = 1MHz$		0.22	0.27	pF

Notes:

(1): ESD Gun return path to Ground Reference Plane (GRP).

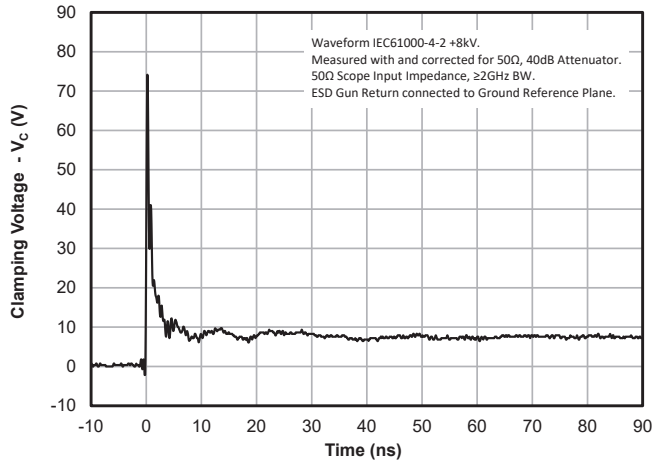
(2): Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, $R_s = 12\Omega$. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

(3): Transmission Line Pulse Test (TLP) Settings: $t_p = 100ns$, $t_r = 0.2ns$, I_{TLP} and V_{TLP} averaging window: $t_1 = 70ns$ to $t_2 = 90ns$.

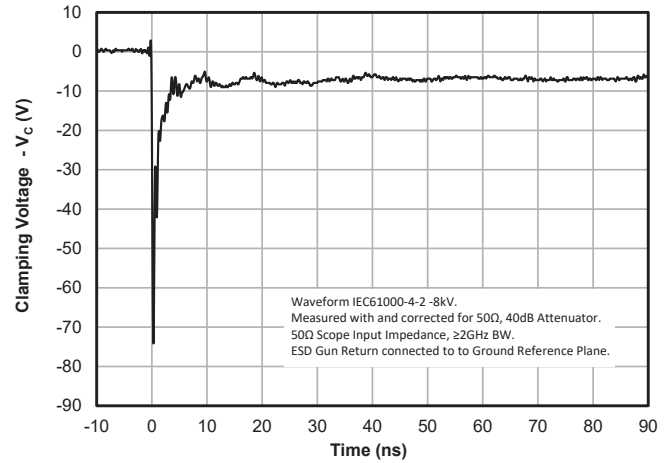
(4): Dynamic resistance calculated from $I_{TLP} = 4A$ to $I_{TLP} = 16A$.

Typical Characteristics

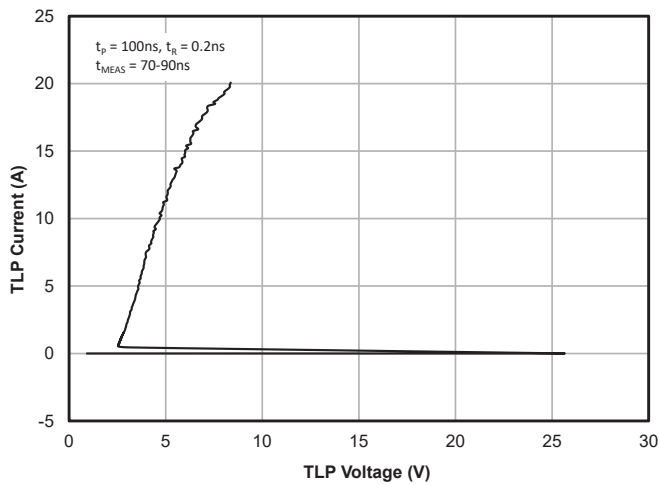
ESD Clamping (+8kV Contact per IEC 61000-4-2)



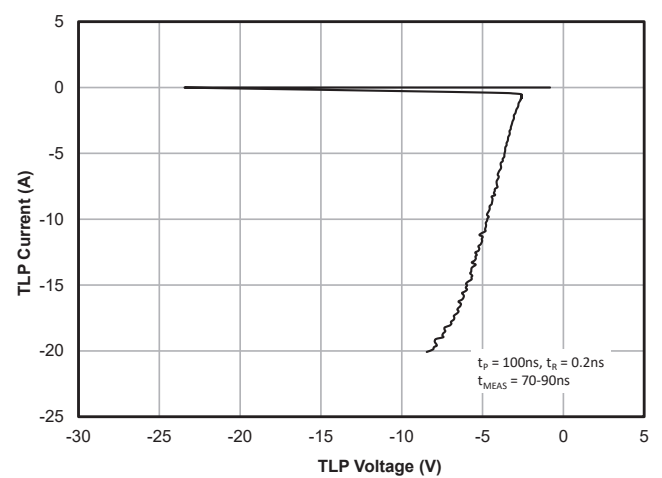
ESD Clamping (-8kV Contact per IEC 61000-4-2)



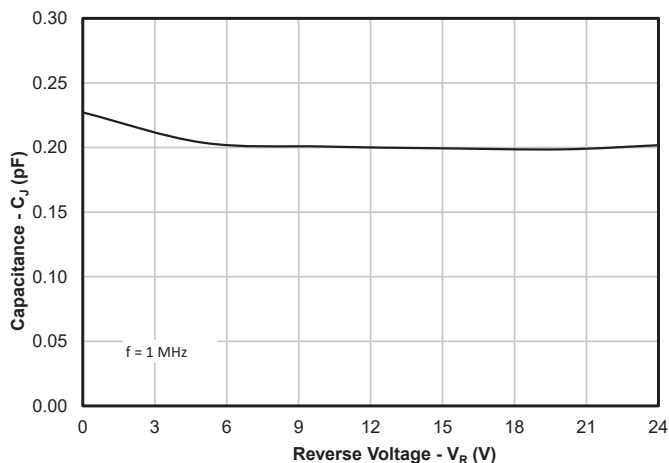
TLP Characteristics (Positive Pulse)



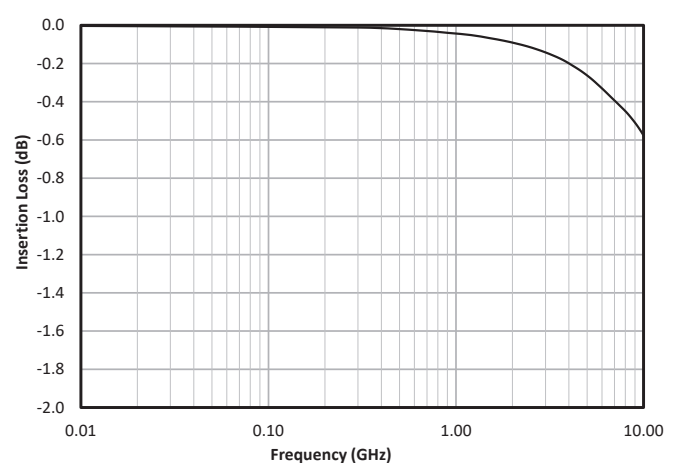
TLP Characteristics (Negative Pulse)



Capacitance vs. Reverse Voltage



Insertion Loss - S21



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

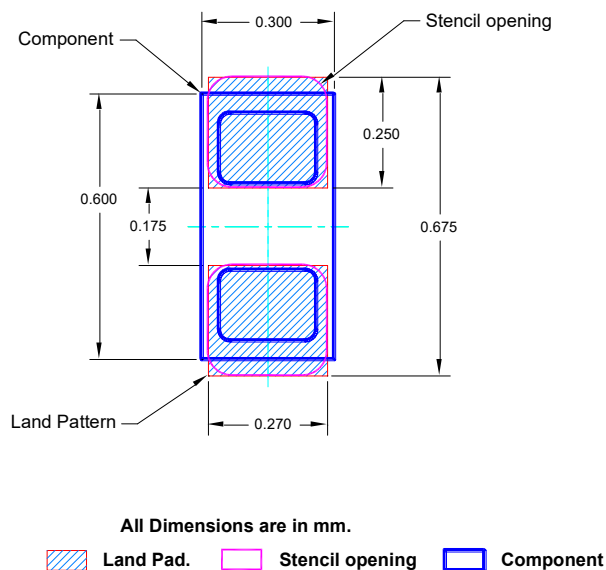
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electro-polished finish. A stencil thickness of 0.075mm (0.003") is recommended. A 0.100mm (0.004") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern



All Dimensions are in mm.

Land Pad. Stencil opening Component

Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003") or 0.100mm (0.004")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non Solder Mask Defined or Non Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Applications Information

ESD Protection of NFC Interfaces

The Near Field Communication (NFC) antenna is usually connected to the NFC controller IC via contact points on the phone. These contact points are user accessible and therefore may be subjected to ESD strikes. External protection (TVS) devices should be placed between the antenna and the NFC chip interface. The working voltage of the TVS should be high enough as not to clip the NFC signal. Additionally, the capacitance of the device should be minimized in order to avoid harmonic distortion of the RF signal.

RClamp2461ZC meets these requirements and also features extremely low dynamic resistance ($\sim 0.24\Omega$) resulting in low ESD clamping voltage. The low dynamic resistance also helps insure protection for Schottky diodes that may be used in the NFC circuit. RClamp2461ZC is designed to work on NFC circuits with AC signals as high as 24V. An example protection circuit using RClamp2461ZC is shown below in Figure 1.

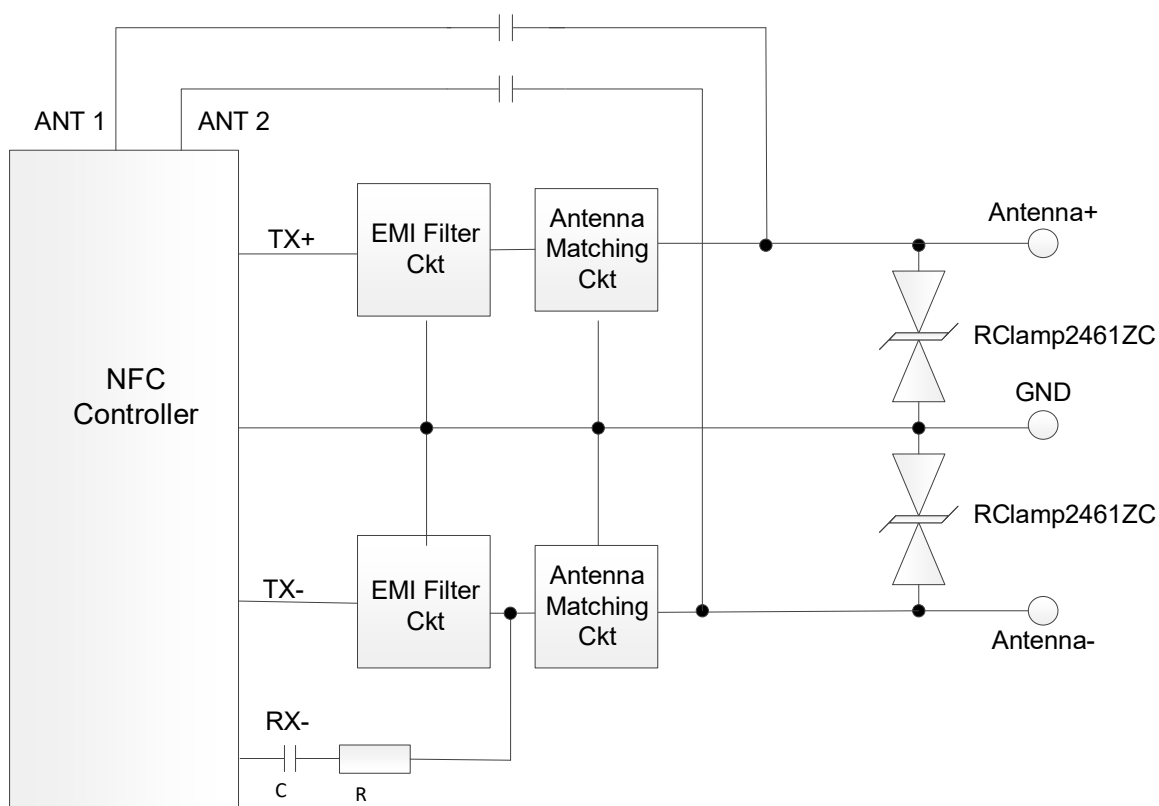
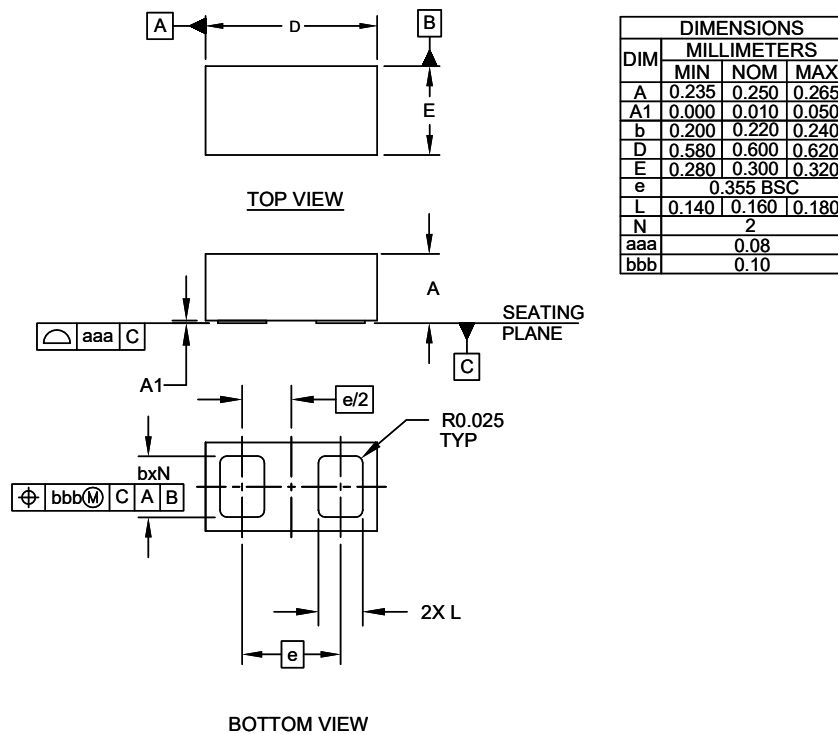
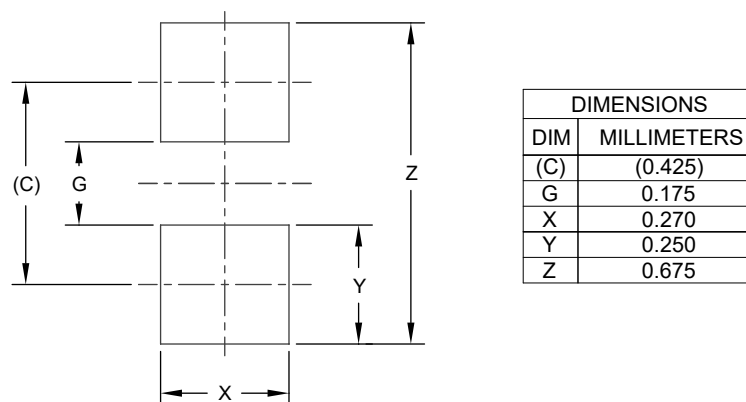


Figure 1 - NFC Protection Example

Outline Drawing - DFN 0.60 x 0.30 x 0.25mm 2-Lead



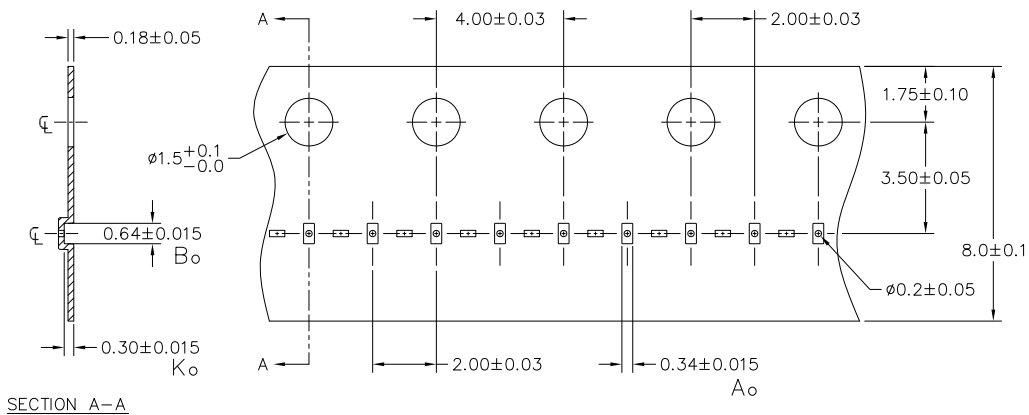
Landing Pattern - DFN 0.60 x 0.30 x 0.25mm 2-Lead



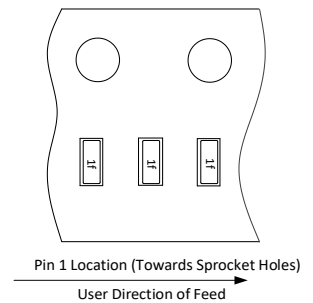
- NOTES:**
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Note: Device is electrically symmetrical.

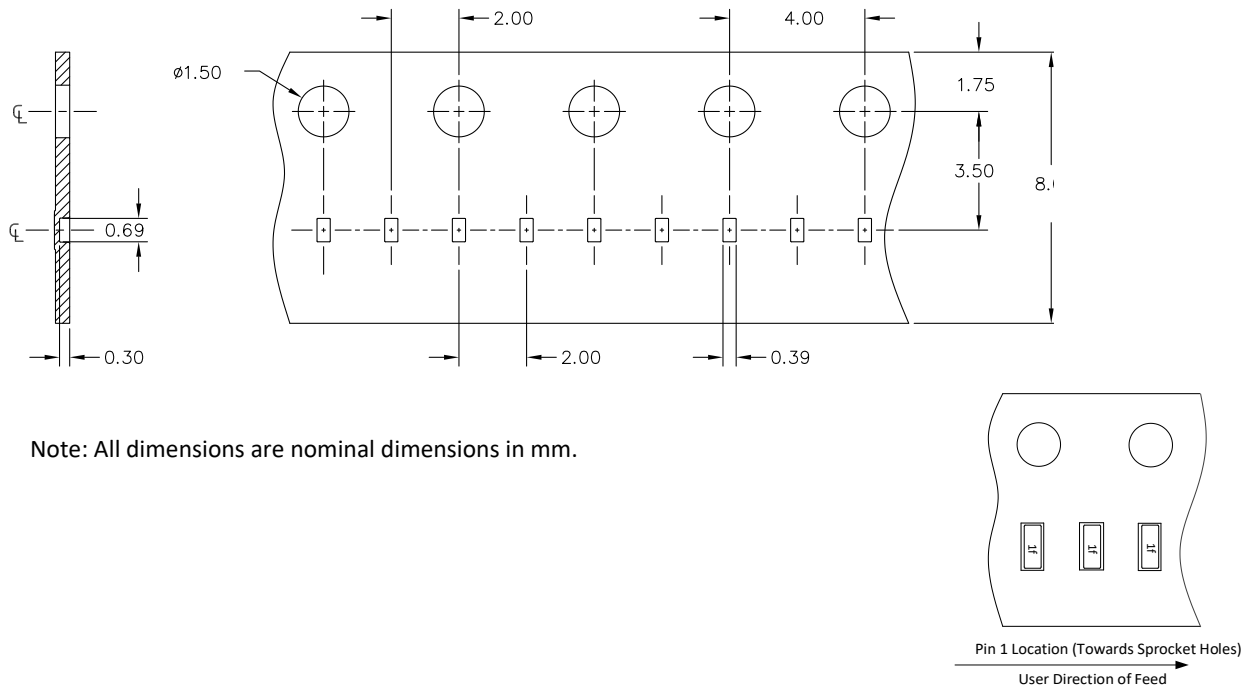
Tape and Reel Specification



NOTE: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Tape and Reel Specification



Order Information

PART NUMBER	QTY PER REEL	MATERIAL	REEL SIZE
RClamp2461ZC.N	10,000	Plastic	7"
RClamp2461ZC.F	15,000	Paper	7"

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