SERIAL PRESENCE DETECT

M392B1K73DM0-CF809/CH909/CK009/CMA09

Organization : 1G x 72
Composition : 512M x 8(st) * 18ea
Used component part # : K4B4G0846D-MCF8/MCH9/MCK0/MCMA
# of rows in module : 4 Row
# of banks in component : 8 Banks
Feature : 18.75mm height & double sided component
Refresh : 8K/64ms
Bin Sort : F8(DDR3 1066@CL=7), H9(DDR3 1333@CL=9), K0(DDR3 1600@CL=11), MA(DDR3 1866@CL=13)
RCD Vendor and Revision : Inphi UV GS02

Byte #	Function Described	Function Supported				Hex Value				Note
		CF809	CH909	CK009	CMA09	CF809	CH909	CK009	CMA09	
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	CRC coverage 0~116Byte, SPD Byte Total :256Byte, SPD Byte Use : 176Byte				92h				
1	SPD Revision	Version 1.1				11h				
2	Key Byte / DRAM Device Type	DDR3 SDRAM				0Bh				
3	Key Byte / Module Type	Registered DIMM				01h				
4	SDRAM Density and Banks	2Gb 8banks				03h				
5	SDRAM Addressing	Row : 15, Column : 10				19h				
6	Module Nominal Voltage, VDD	1.5V only				00h				
7	Module Organization	4Rank / x8				19h				
8	Module Memory Bus Width	ECC, 64bit				0Bh				
9	Fine Timebase Dividend and Divisor	1ps				11h				
10	Medium Timebase Dividend	1/8 (0.125ns)				01h				
11	Medium Timebase Divisor	1/8 (0.125ns)				08h				
12	SDRAM Minimum Cycle Time (tCKmin)	1.875ns	1.5ns	1.25ns	1.071ns	0Fh	0Ch	0Ah	09h	
13	Reserved	Reserved				00h				
14	CAS Latencies Supported, Least Significant Byte	6, 7, 8	6, 7, 8, 9	6, 7, 8, 9 , 10, 11	6, 7, 8, 9 , 10, 11, 13	1Ch	3Ch	FCh	FCh	
15	CAS Latencies Supported, Most Significant Byte	6, 7, 8	6, 7, 8, 9	6, 7, 8, 9 , 10, 11	6, 7, 8, 9 , 10, 11, 13	00h	00h	00h	02h	
16	Minimum CAS Latency Time(tAAmin)	13.125ns				69h				
17	Minimum Write Recovery Time (tWRmin)	15ns				78h				
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	13.125ns				69h				
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	7.5ns	6ns	6ns	5ns	3Ch	30h	30h	28h	
20	Minimum Row Precharge Time (tRPmin)	13.125ns				69h				
21	Upper Nibbles for tRAS and tRC	-				11h				
22	Minimum Active to Precharge Time (tRASmin), Least Significant Byte	37.5ns	36ns	35ns	34ns	2Ch	20h	18h	10h	
23	Minimum Active to Active/Refresh Time (tRCmin), Least Significatn Byte	50.625ns	49.125ns	48.125ns	47.125ns	95h	89h	81h	79h	
24	Minimum Refresh Recovery Time (tRFCmin), Least Significant Byte	160ns				00h				
25	Minimum Refresh Recovery Time (tRFCmin), Most Significant Byte	160ns				05h				
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	7.5ns				3Ch				
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns				3Ch				
28	Upper Nibble for tFAW	37.5ns	30ns	30ns	27ns	01h	00h	00h	00h	
29	Minimum Four Activate WIndow Delay Time (tFAWmin), Least Significant Byte	37.5ns	30ns	30ns	27ns	2Ch	F0h	F0h	D8h	
30	SDRAM Output Drivers supported	DLL off Mode, RZQ/6, RZQ/7				83h				
31	SDRAM Thermal and Refresh Options	No ODTS, No ASR				01h				
32	Module Thermal Sensor	with TS				80h				
33	SDRAM Device Type	Non-Standard Device				80h				
34	Fine Offset for SDRAM Minimum Cycle Time(tCKmin)	1.875ns	1.5ns	1.25ns	1.071ns	00h	00h	00h	CAh	
35	Fine Offset for Minimum CAS Latency Time(tAAmin)	13.125ns				00h				

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		CF809	CH909	CK009	CMA09	CF809	CH909	CK009	CMA09	
36	Fine Offset for Minimum RAS# to CAS# Delay Time(tRCDmin)	13.125ns				00h				
37	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	13.125ns				00h				
38	Fine Offset for Minimum Active to Active/Refresh Delay Time(tRCmin)	50.625ns	49.125ns	48.125ns	47.125ns	00h				
39~59	Reserved, General Section	Reserved				00h				
60	Module Nominal Height	18.75mm				04h				
61	Module Maximum Thickness	DDP Double sides(With Flat Type H/S)				33h				
62	Reference Raw Card Used	R/C V, 0.0				11h				
63	DIMM Module Attributes	1 Row of DRAM / 1 Register used				05h				
64	Heat Spreader Solution	with HS				80h				
65	Register vendor ID code(LSB)	Inphi				04h				
66	Register vendor ID code(MSB)	Inphi				B3h				
67	Register Revision Number	Inphi UVGS02				21h				
68	Register Type	SSTE32882				00h				
69	Register Control Word Functions(RC0/RC1)	Default				00h				
70	Register Control Word Functions(RC2/RC3)	R/C V				A0h				
71	Register Control Word Functions(RC4/RC5)	R/C V				55h				
72	Register Control Word Functions(RC6/RC7)	Default				00h				
73	Register Control Word Functions(RC8/RC9)	Default				00h				
74	Register Control Word Function(RC10, RC11)	Default				00h				
75	Register Control Word Function(RC12, RC13)	Default				00h				
76	Register Control Word Function(RC14, RC15)	Default				00h				
77~116	Reserved	-				00h				
117	Module Manufacturer ID Code, Least Significant Byte	Samsung				80h				
118	Module Manufacturer ID Code, Most Significant Byte	Samsung				CEh				
119	Module ID: Module Manufacturing Location	Onyang Korea				01h				
120	Module ID: Module Manufacturing Date	-				00h				
121	Module ID: Module Manufacturing Date	-				00h				
122~125	Module ID : Module Serial Number	-				00h				
126	Cyclical Redundancy Code	-	-			29h	6Bh	5Fh	0Ch	
127	Cyclical Redundancy Code	-	-			45h	ECh	33h	3Bh	
128	Module Part Number	M				4Dh				
129	Module Part Number	3				33h				
130	Module Part Number	9				39h				
131	Module Part Number	2				32h				
132	Module Part Number	B				42h				
133	Module Part Number	1				31h				
134	Module Part Number	K				4Bh				
135	Module Part Number	7				37h				
136	Module Part Number	3				33h				
137	Module Part Number	D-die				44h				
138	Module Part Number	M				4Dh				
139	Module Part Number	0				30h				
140	Module Part Number	-				2Dh				
141	Module Part Number	C				43h				
142	Module Part Number	F	H	K	M	46h	48h	4Bh	4Dh	
143	Module Part Number	8	9	0	A	38h	39h	30h	41h	

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		CF809	CH909	CK009	CMA09	CF809	CH909	CK009	CMA09	
144	Module Part Number	Blank				20h				
145	Module Part Number	Blank				20h				
146~147	Module Revision Code	-				00h				
148	SDRAM Manufacturer's JEDEC ID Code	Samsung				80h				
149	SDRAM Manufacturer's JEDEC ID Code	Samsung				CEh				
150~175	Manufacturer's Specific Data	-				00h				
176~255	Open for customer use	-				00h				